Master's Thesis

Development of Contacts for Vertical GaSb Nanowires using Transmission Line Measurements

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LUND UNIVERSITY

MASTER'S THESIS

Development of Contacts for Vertical GaSb Nanowires using Transmission Line Measurements

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Abstract

A processing method is developed to characterize contacts for vertical nanowire structures. The process is based around optical lithography and an organic spacer material in order to facilitate an easily repeatable processing flow. Substrates with MOVPE grown GaSb nanowires are processed into sets of resistor devices. Variation in resistance of the devices is achieved by adding contacts at different heights to the otherwise similar nanowire devices. Contact resistance R_C and specific contact resistivity ρ_c are extrapolated from a linear approximation of the measured resistance vs contact distance. The process is tested on samples with differently doped and dimensioned nanowires. Rapid thermal annealing is performed at temperatures 150 °C to 250 °C in order to study its effect on contact resistivity. The resulting ρ_c values are in the range of $30\,\Omega\,\mu m^2$ to $158\,\Omega\,\mu m^2$. Rapid thermal annealing at 150 °C to 200 °C shows improvement in contact resistivity, while RTA at 250 °C instead indicates a deterioration.

Contents

Abbreviations and Symbols

III-V Compound semiconductor of periodic table elements in group III and V.

EBL Electron Beam Lithography.

FIB Focused Ion Beam.

GaSb Gallium Antimonide.

InAs Indium Arsenide.

MOSFET Metal Oxide Semiconductor Field Effect Transistor.

MOVPE Metal Organic Vapor Phase Epitaxy.

RIE Reactive-Ion Etching.

RTA Rapid Thermal Annealing.

SEM Scanning Electron Microscope.

TLM Transmission Line Model.

q Elementary charge, $1.6 \cdot 10^{-19}$ $[C]$.

Acknowledgments

First and foremost, I would like to say thank you to my supervisor Johannes Svensson for his excellent guidance. I am grateful for the helpfulness and encouragement of everyone in the Nanoelectronics group. Additionally, I am grateful to the people at Lund Nano Lab for their technical help and for providing a friendly working atmosphere.

Chapter 1

Introduction

1 Background

The Moore's law describing transistor scaling is coming to an end due to physical limitations in Si-based transistor downsizing and integration. Various manufacturing tricks have been used to delay the "end of Moore's law" but it is indeed trending towards an end as can be seen in various technology road maps. New types of devices are continuously being developed to extend semiconductor development beyond the planar technologies [1, 2, 3, 4]. One such technology is FinFET, which is already present in personal computers. Significant amount of work is already being done in researching potential successive device architectures and materials (nanowires, carbon nanotubes) with a significant portion of those made of group III-V materials. A popular theme is to use a fundamentally different manufacturing principle for those new devices. Instead of being processed top-down in typically homogeneous layers, they are instead grown bottom-up. The potential for superior electrostatic properties of the vertical device architectures such as nanowires, combined with the increased electron velocity possible in the III-V type materials enable new types of devices that are able to operate faster and with a lower power consumption [1, 2].

Device contacts have shown to be a challenge and a bottleneck for performance, when the devices themselves are becoming smaller, while the contact is needed to interface the device with the other devices (wire interconnect). There is a growing demand for better performing contacts and with the emerging novel device technologies, also methods for characterization. This is in large due to the downsizing of device dimensions and their higher current consumption, along with the need for higher on-chip device density. In summary, the contact needs to be able to accommodate the devices current consumption while minimizing the area needed for the contact [5, 6, 7, 8, 9].

2 Project Goal

The goal of this project is to develop and evaluate a processing method which can enable iterative characterization of contacts to vertical nanowires, with minimum amount of complex processing steps. This type of method for extraction of specific contact resistivity ρ_c is of interest because it would simplify property evaluation of new contact materials. The developed method is based on optical lithography and use of organic resist as the spacer material.

3 Previous Work

Work on the subject has previously been done in the Nanoelectronics group at the Electrical and Information Technology department. In the project using vertical InAs nanowires, the TLM structures were designed using HSQ spacer material and with electron beam lithography[6]. The approach to extrapolate the resistivities (application of TLM) used in this project is adapted from it and other previous work which detailed the general procedure [10].

4 Structure of the Report

The underlying theory covering the fundamentals of the project is described in chapter 2. The processing methods that were used to manufacture the samples in this work are explained in chapter 3, while the characterization procedure is covered in chapter 4. The results from the processed measurement data is presented and discussed in chapter 5. Chapter 6 contains a summary of the project.

Chapter 2

Theory

1 Overview

The aim of this project is to devise a method for semiconductor contact characterization. Specifically, for contacts that interface metal to vertical GaSb nanowires. The main metric of interest is the specific contact resistivity ρ_c $[\Omega\mu m^2]$. This is a unit that specifically describes the resistivity of the metal-semiconductor interface. It is useful in order to make performance comparison between different contact materials easier. This chapter will attempt to explain the different metric values that must be obtained in order to derive ρ_c.

2 Group III-V Semiconductors

The compound semiconductor materials consisting of elements from periodic table groups III and V are commonly abbreviated **III-V**. Devices made of these specific materials are interesting in large part due to their transport properties, which become increasingly important as the technology miniaturization progresses towards 10 nm and beyond. In order for transistors to operate at a higher frequency and with a lower power consumption, when compared to their more traditional Si-based counterparts, III-V based technologies is a natural progression[1, 2].

3 Nanowires

Nanowires are structures which can be grown with Metal Organic Vapor Phase Epitaxy, MOVPE[11]. The MOVPE growth process can control the nanowire composition to a

high degree. This is especially suitable for III-V hetero structure compounds. Device fabrication by the bottom-up approach in general has the advantage of not requiring dry etching, which can create surface roughness. This processing technique enables devices such as single nanowire inverters [12, 13]. Nanowires have shown good potential for use in a wrap-around gate MOSFET design, where the applied gate potential can be used more effectively than in a conventional planar device. [1, 2, 14] This work uses GaSb nanowires with short InAs segment (figure 2.1). The samples have a small epitaxial InAs

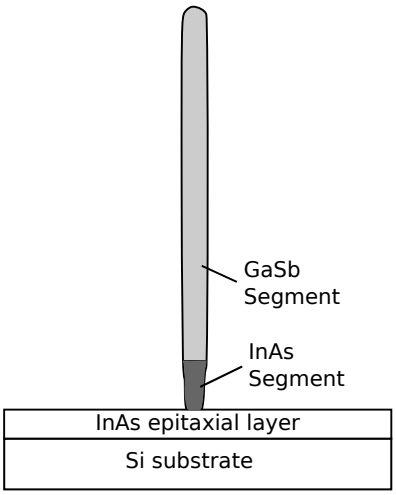


Figure 2.1: Illustration of the InAs and GaSb segments of the nanowire. The InAs epitaxial layer and Si substrate are not to scale.

layer on top of the bulk Si substrate.

4 Contacts

Semiconductor contacts can be split in two main parts. The metal of the contact (pad) itself and the metal-semiconductor interface. The pads connect the chip to the outside world by, for example, wire bonding a chip to a package capsule. In the current project, electrical probes at a characterization station contact the pads for I-V measurements.

When the metal-semiconductor interface exhibits a linear current-voltage relationship, the contact is often referred to as Ohmic, which is the preferred type of contact type for use in the interconnect. In contrast, an interface can behave non-linearly due to various types of junctions which only allow asymmetrical charge flow [15, 16].

5 Transmission Line Model

The purpose of TLM is to extrapolate contact and semiconductor resistivities from I-V measurements performed on a set of devices. The I-V measurements give the total resistance values of the respective devices. The contact (end-points) of the different devices are placed at different distances. The varying distance that the current needs to travel through the semiconductor results in different resistances for otherwise similar devices. Measurement of a set of devices with different contact distances makes it possible to separate metal-semiconductor interface (contact) resistance from semiconductor resistance. This is because that the resistance contributed by contacts to the total measured resistance does not change with varying contact distance [15].

Semiconductor Resistivity

The total measured resistance R_{NW} consists of the contact (the metal-semiconductor interface) resistance R_C, the metal-only part of the contact R_M and the semiconductor resistance R_S (figure 2.2a). This can be summarized as $R_{NW} = 2R_M + R_S + 2R_C$, with factor two in front of the R_M and R_C in order to account for that there are two contact pads. The R_M is the metal-only part of the contact, which is significantly lower than the other constituent resistances and therefore discarded for the purpose of TLM calculations.

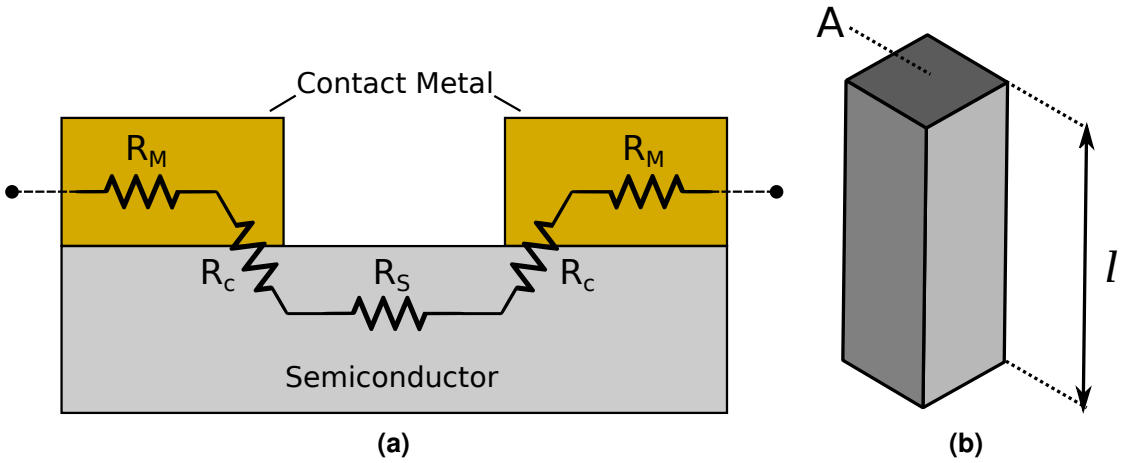


Figure 2.2: Different resistances of a metal-semiconductor interface (a) and the geometry of a semiconductor in context of resistivity calculation (b).

In order to be able to compare contact properties between different geometries, the semiconductor resistivity and the contact resistivity are introduced. The semiconductor

resistivity,

$$\rho_s = R\frac{A}{l} = R_{NW}\frac{\pi r^2}{L_{NW}}\ [\Omega \cdot \mu m]\ , \tag{2.1}$$

where the R, A and l are the generalized resistance, area and the length of the semiconductor (figure 2.2b). The R_{NW}, r and L_{NW} are the resistance, nanowire radius and the nanowire length used for calculations on vertical nanowires in particular. The semiconductor resistivity can also be expressed in terms of doping concentration and the majority charge carrier mobility as

$$\rho_s = \frac{1}{q \cdot (\mu_n n + \mu_p p)}\ [\Omega \cdot \mu m]\ , \tag{2.2}$$

where μ_n and μ_p are electron and hole mobility, with the electron and hole concentration denoted as n and p, respectively, with q being the elementary charge. It should be noted that p-type doped GaSb nanowires are used in this work. Therefore, the hole concentration and mobility are considered primarily while the corresponding electron metrics disregarded when using the above equation. The doping concentration of grown nanowires can be measured, for instance by Hall measurements. The use case for equation 5, in context of nanowire I-V characterization, can be to extract the mobility and the charge concentration factor after acquiring ρ_s using equation 5. An initial model, which does not take the metal-semiconductor interface into consideration, is made to illustrate the influence of spacer thickness variation on resistance (figure 2.3a). Doping concentration is estimated to $p = N_A \approx 10^{19}\ [cm^{-3}]$. The hole mobility μ_p for this type of doping concentration in GaSb is approximated to 300 $cm^2V^{-1}s^{-1}$. The figure 2.3 also shows the relationship of number of nanowires in the arrays and corresponding expected resistance relationship. The resistance decreases with increased number of nanowires since the added ones correspond to parallel resistances. If the assumption is made that the nanowires are identical, this scaling becomes linear.

Specific Contact Resistivity

The contact resistance R_C that is acquired experimentally is valid for contact dimensions of the specific contact being measured. To be able to compare the performance of the contact metal, a normalized figure of merit is necessary. If a uniform metal-semiconductor interface geometry is assumed, the contact resistivity ρ_c of a vertical nanowire contact can be expressed as

$$\rho_c \approx R_C \pi r^2\ [\Omega \cdot \mu m^2], \tag{2.3}$$

where r is the radius of the nanowire and R_C is the absolute contact resistance. The acquisition of R_C is the main goal of TLM. The application of TLM using vertical nanowire devices used in this project is derived from earlier work in the Nanoelectronics

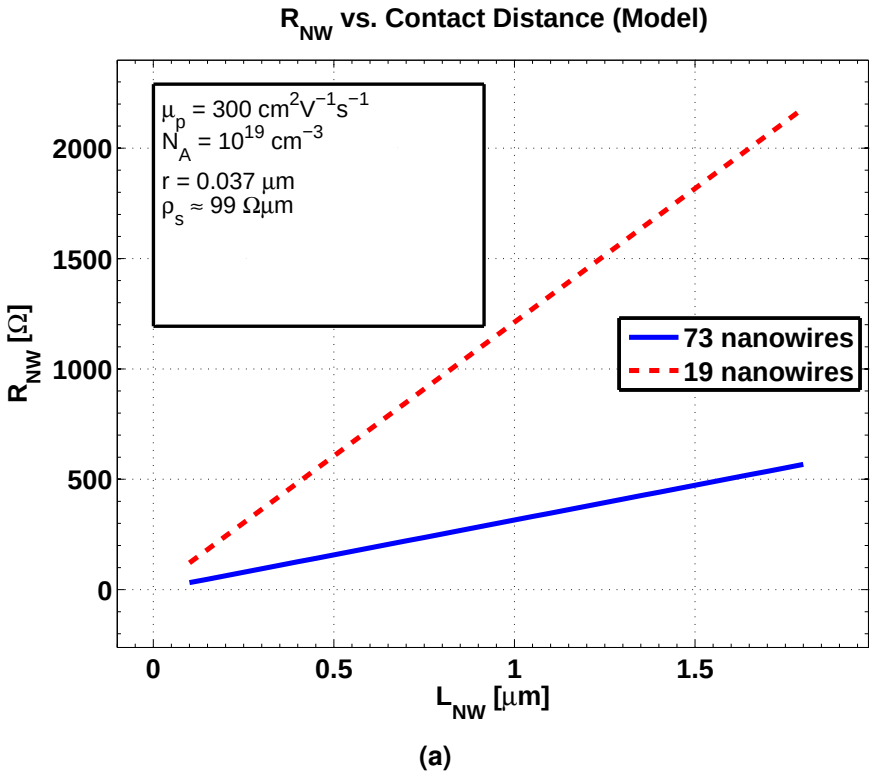


Figure 2.3: An approximation of how resistance can be expected to vary with different contact spacer thickness and amount of nanowires in a device array. The specific contact resistivity is assumed ideal, $\rho_c = 0$ (a).

group at Lund University [6]. Resistance is measured for a set of approximately identical devices. The distance between the contacts on each device in the set is increased (or decreased). Longer distance means that the current travels longer in the semiconductor portion of the device (the nanowire length between the contacts) longer and therefore experiences higher resistances. This set of resistances are plotted with respect to their contact distances. The approximated resistance which still exists at zero contact distance is the seeked contact resistance R_C (figure 2.4). Zero contact distance would, if realized in practice, result in a short-circuit and the resistance must therefore instead be extrapolated. When applying TLM to lateral contacts, the extracted value on the y-axis represents $2 \cdot R_C$. Due to the tunnel junction between the InAs and GaSb segments, the resistance of the bottom contact is likely significantly higher than the top contact.

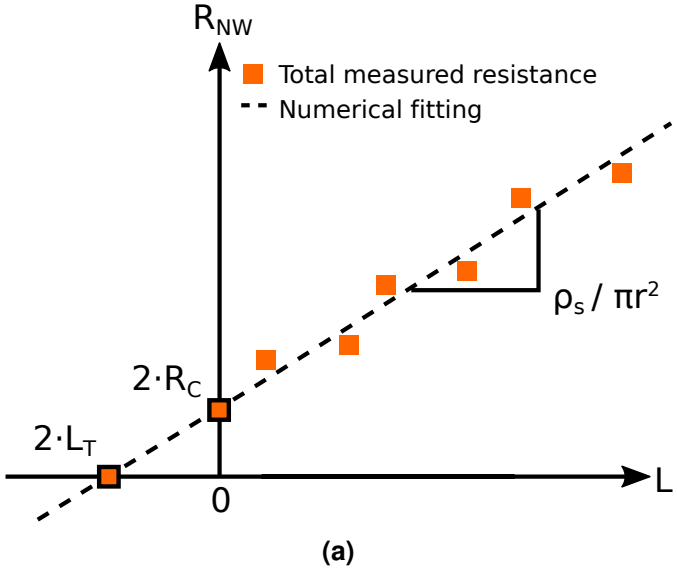


Figure 2.4: An illustration of a processed TLM data figure.

Transfer Length

An important notion in context of semiconductor contacts and TLM is the transfer length L_T. The transfer length is the distance the current reaches inside the contact boundary before the majority ($\approx 63\%$) of the current is able to be transferred through the contact interface. This is derived from the fact that the current drops off within the boundary of the contact according to $I(x) \propto e^{-x/L_T}$, where I is the current and x is the distance within the edge of the contact (figure 2.5) [15, 10]. In other words, transfer length is a quantity closely related to current crowding, which is a major challenge that comes with down scaling of semiconductor technologies [2, 17, 5]. As a guideline, in order to avoid issues with high R_C due to current crowding, the contacted length should be at least $3 \cdot L_T$. The transfer length can be determined from TLM data in figure 2.4 by reading

the value of the contact distance when the resistance reaches zero. The read-out value is negative but the minus sign is discarded since it has no physical relevance. Furthermore, the semiconductor resistivity ρ_s can be determined from the linear approximation by multiplying the slope of the linear fit with the nanowire area cross-section, πr^2. In terms of TLM parameters, the transfer length is expressed as

$$L_T = R_C \cdot \frac{\pi r^2}{\rho_s} \, [\mu m] \, . \tag{2.4}$$

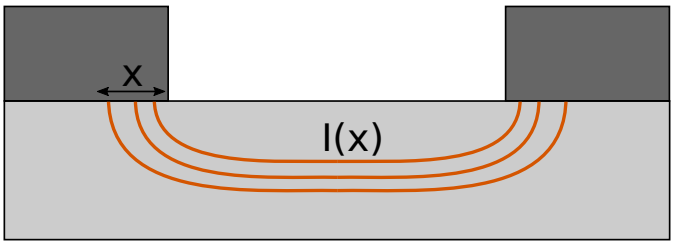


Figure 2.5: Transfer length geometry for a planar contact.

The specific contact resistivity ρ_c relates to the nanowire radius, the extracted L_T and ρ_s as

$$\rho_c = \frac{2L_T^2 \rho_s}{r} \, [\Omega \cdot \mu m^2] \, . \tag{2.5}$$

Vertical Nanowire Contact

In order to account for the distance between the top contact and the spacer material, in relation to the transfer length L_T, the expression for contact resistance becomes

$$R_C = \frac{\rho_s L_T}{\pi r^2} \coth\left(\frac{L_{Total} - L_{NW}}{L_T}\right) \, [\Omega] \, , \tag{2.6}$$

where L_{Total} is the length of the nanowire and L_{NW} is the distance between the top and bottom contacts, geometry of which is illustrated throughout the next chapter. The coth factor of the equation is unity unless the distance between the top contact and the top end of the nanowire (i.e., length of the nanowire that remains above the spacer) is less than one L_T [6].

5.1 Goodness of Fit

The accuracy of the values extracted using TLM depends strongly on the quality of the linear fit. An indicator of quality of the linear fit can be acquired by calculating Goodness

of Fit, using coefficient of determination R^2. The R^2 was calculated by first summing up the residuals (distance of the measured resistances from the linear fit) and then squaring the sum. This value is in the range of 0 to 1 (unit-less) and represents the fraction of the variance in the source data that the linear fit is able to predict. A R^2 value of 1 means that all the data points are perfectly predicted by the linear fit[18].

Chapter 3

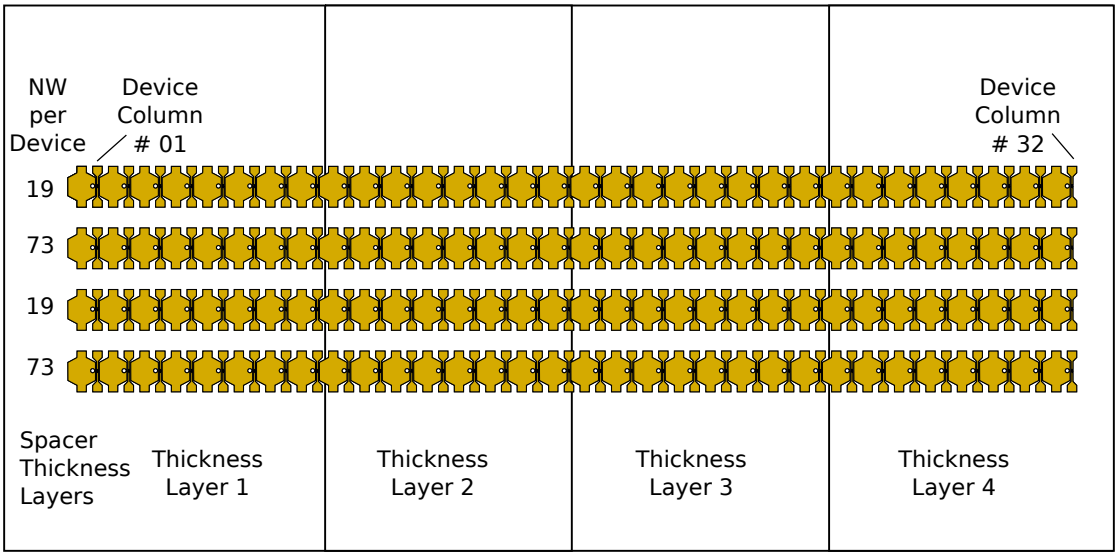
Manufacturing Process

1 Overview

The overall processing goal was to produce resistors using samples with vertically grown GaSb nanowires and to add contacts at different height to otherwise similar devices. The final spacer structure can be likened to a stair-case that covers the whole sample, with the total amount of devices on the sample being spread over the different stair-cases. A top-down representation of this structure is shown in figure 3.1. Optical lithography with various etching and depositing techniques were used to achieve this. Several different samples were manufactured, with variation in doping level and dimensions of the nanowires. The processing procedures that were performed are described in the following sections.

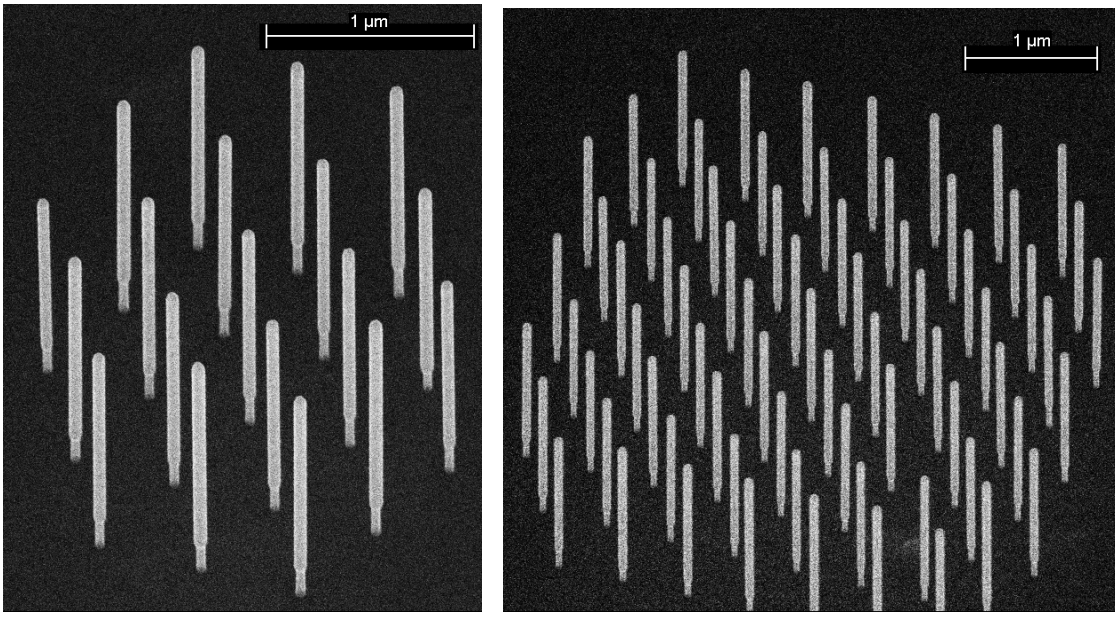
2 Nanowire Growth

The substrate with grown nanowires is the foundation and starting point of the processing. The mask design and nanowire growth [12] are courtesy of Johannes Svensson, Nanoelectronics group at the Electrical and Information Technology department of LTH. The structure of a single nanowire after growth can be seen in figure 3.3a and a SEM image of the grown nanowires can be seen in figure 3.2. What can be seen are arrays consisting of 19 nanowires and 73 nanowires, respectively. These are the array types that were used to construct the resistors. The process illustrations that follow use a single nanowire to represent a whole nanowire array (one device).



(a)

Figure 3.1: The top-down overview of the distribution of devices on the die over the different spacer thickness layers. In total, approximately 32 devices per thickness layer.



(a) **(b)**

Figure 3.2: SEM images of the two nanowire array sizes. One with 19 nanowires (a) and another with 73 nanowires (b).

3 Source Contact

On the substrate with the grown nanowires (figure 3.3a), a 30 nm tungsten bottom metal layer was sputtered (figure 3.3b). This was done in order to circumvent the tunnel-junction between the InAs and the GaSb segment of the nanowires. The InAs segment

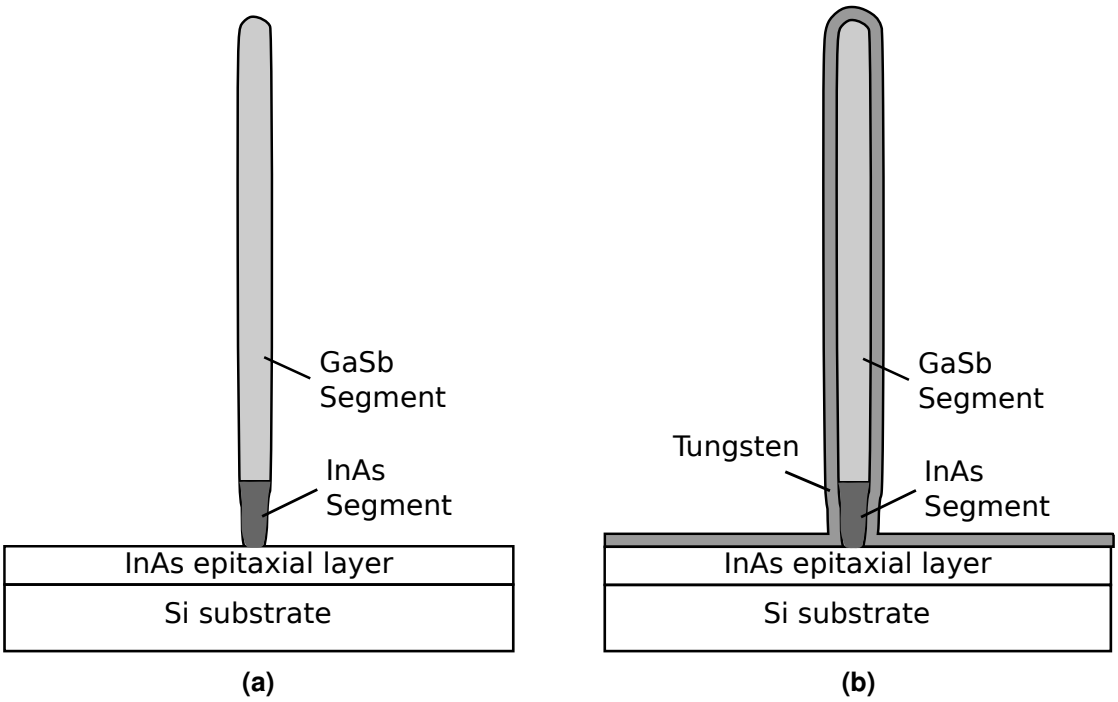


Figure 3.3: Structure of one nanowire after growth (a) and after sputtering with 30 nm tungsten (b).

and a small part of the GaSb segment was covered with photo resist (figure 3.4a) in order to mask the tungsten socket layer from the rest of the sputtered tungsten. The rest of the sputtered tungsten was removed using RIE. Thereby, a tungsten socket between the InAs and the GaSb segment was created (figure 3.4b). The layer of photo resist (spacer material) that is covering the tungsten socket indicates the minimum thickness at which a contact can be created, without short-circuiting with the socket.

4 Contact Spacer

At the start of this stage, the sample contains the grown (InAs-)GaSb nanowire arrays with tungsten socket connecting the InAs and the GaSb segment. The goal was to create a structure which would enable metal deposition at various heights throughout the sample. The nanowires are sensitive to the wet etching lithography steps and were

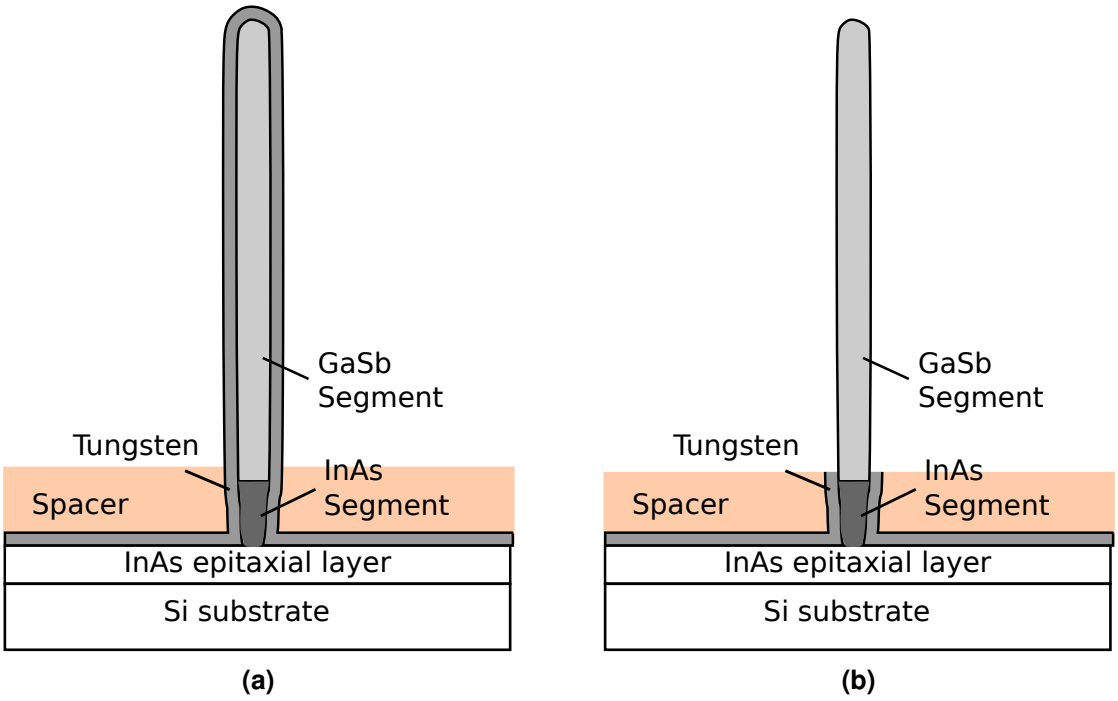


Figure 3.4: Photo resist covering the tungsten socket, which connects the InAs and the GaSb segments (a); tungsten removed by plasma-etching from the rest of the GaSb segment (b).

therefore first submerged completely, by spin-coating, in a layer of Shipley 1828 photo resist (S1828). The S1805 variation of the photo resist was used to fabricate the different spacer thickness levels (figure 3.5a). Baking of the sample was done in order to minimize left-over solvent and migration of the resist.

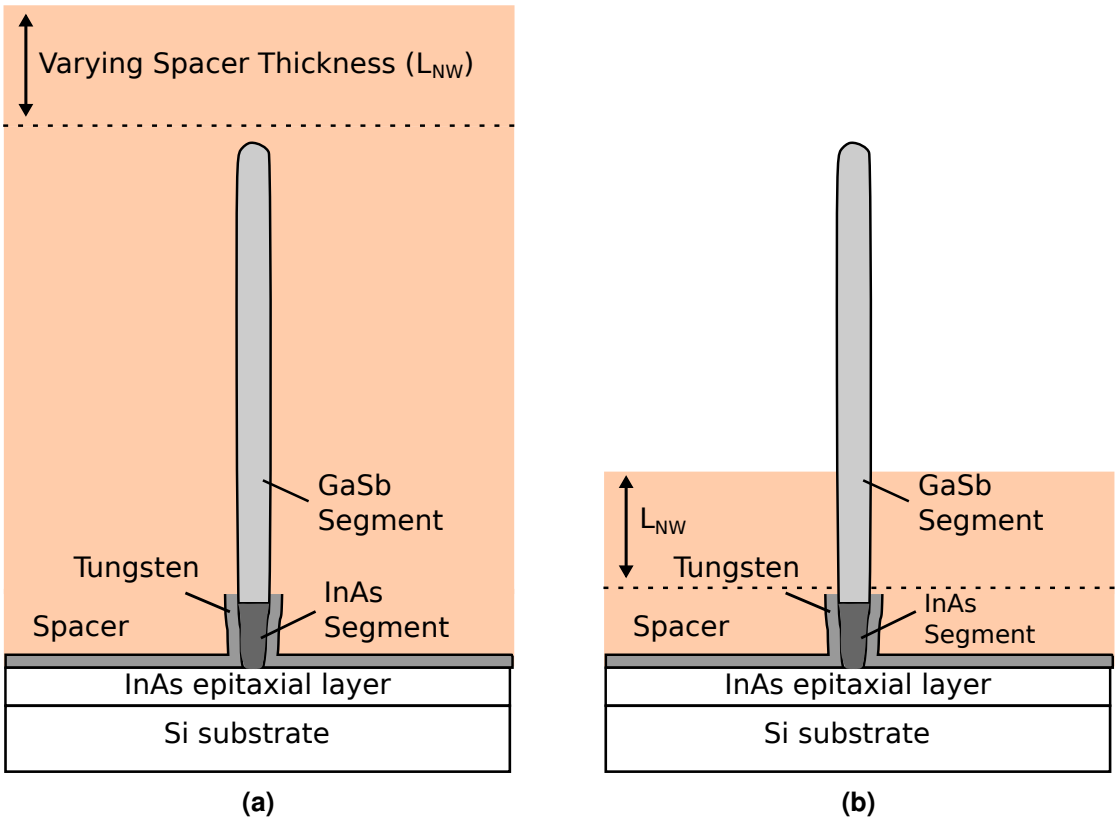


Figure 3.5: Staircase spacer constructed on top of the resist fundament (a) and staircase spacer etched down to intended spacer thickness (b). The spacer thickness L_{NW} varies depending on in which section of the die the nanowire (array) is situated.

A previously fabricated photo mask was used during the UV-exposure to control the boundary of the spacer thickness levels (*stair-cases*). The exposure was done for a duration dependent on the thickness of the applied resist. The lithographic steps using S1805 were repeated until the number of spacer thickness levels were reached. Figure 3.5a shows schematically the principle of how a spacer thickness level was constructed. The spacer thickness levels on the die at this stage, as seen through an optical microscope, are shown in figure 3.6. The spacer thickness was determined by measuring the reflectance of light as a function of wavelength, and a set of reference values was noted for the different thickness levels.

The entire resist spacer structure was etched down by Reactive-Ion Etching, using

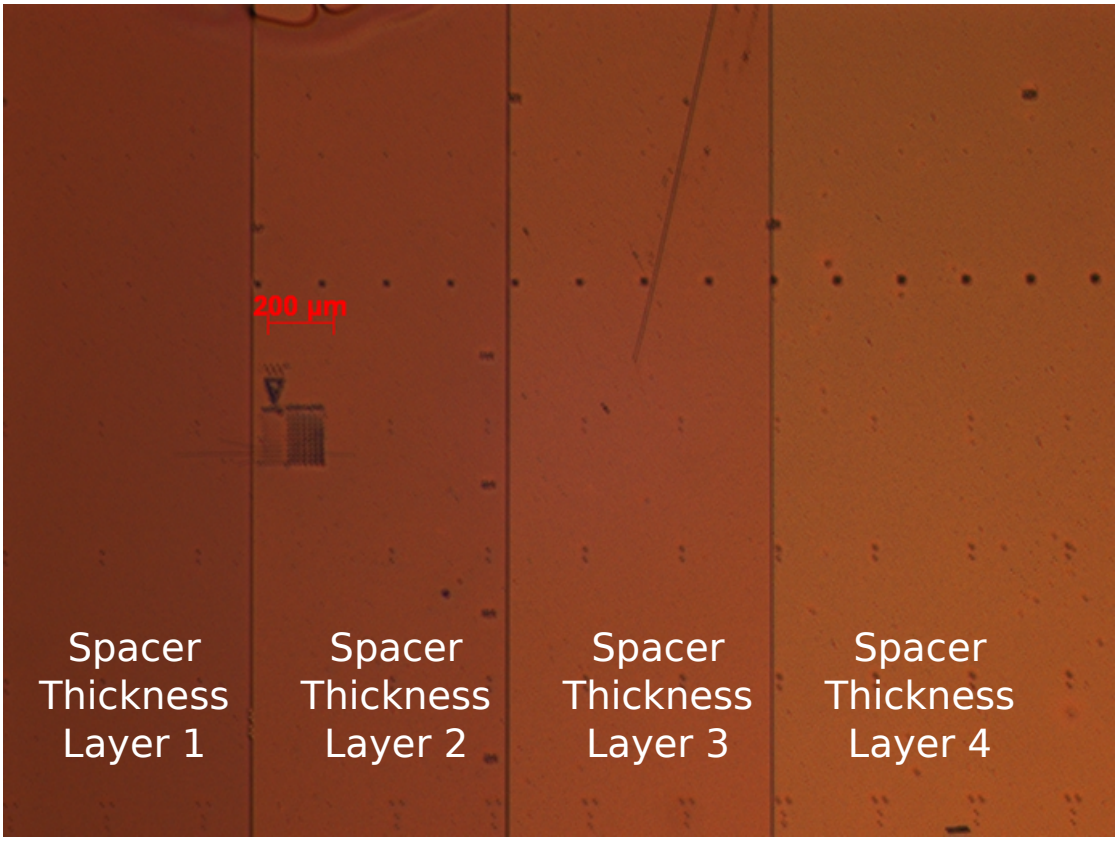


Figure 3.6: Spacer thickness levels on the die, as seen through optical microscope. Darker hue indicates a thicker spacer layer.

oxygen plasma (figure 3.5b). High RIE effect strength was used for a better degree of anisotropy. The disadvantage of using the higher effect was a more pronounced edge-effect, meaning that the etch rate is significantly higher along the edges of the sample. The RIE etching and the thickness (film reflectance) measurements were performed iteratively until the desired spacer thickness was reached. The thickness of the spacer adjacent to all resistor devices were, when satisfactory thickness was reached, measured with film metrics. These values were noted down and saved with the respective devices mapped to be used in the TLM procedure.

5 Source Via

In order to protect the stair-case structure that was constructed earlier from being etched away by RIE, a layer of S1828 was added (figure 3.7a). Like previously, lithographic steps exposed the regions where the holes for source vias needed to be accessible during metal deposition (figure 3.7b).

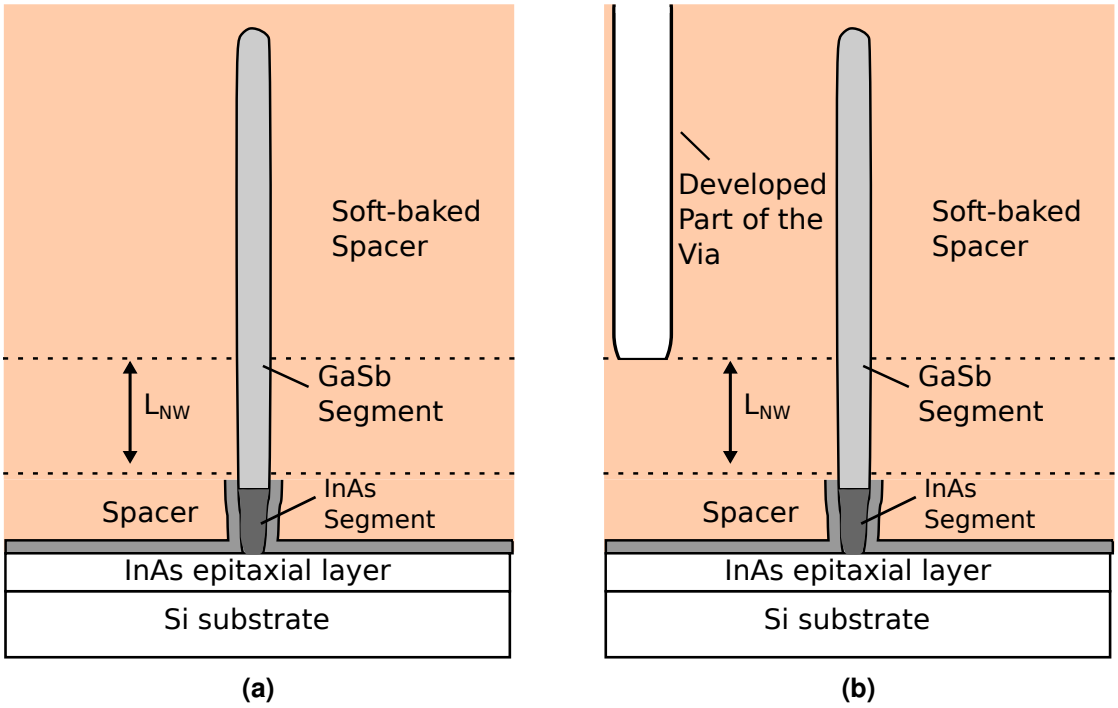


Figure 3.7: Spin-coated resist above the permanent-baked stair-case spacer layer L_{NW} (a); and the developed part of the Source-Via after the UV-exposure (b). The dimensions of the vias relative the nanowire are not to scale.

A layer of resist was spin-coated on top of the one already present. An important difference was that the newly applied layer was not heated enough during the baking

for cross-linking to take place, and therefore remained sensitive to UV-light. In this way, the source via pattern could be developed without risk of damaging the lower resist during exposure. After the development of the newly coated resist layer, the vias were etched out by RIE (figure 3.8a). In summary, a layer of resist was applied to cover the nanowires above the staircase structure. This new layer was patterned with source via holes using UV lithography. The same source via pattern was etched through the underlying stair-case resist, with the upper layer acting as a mask.

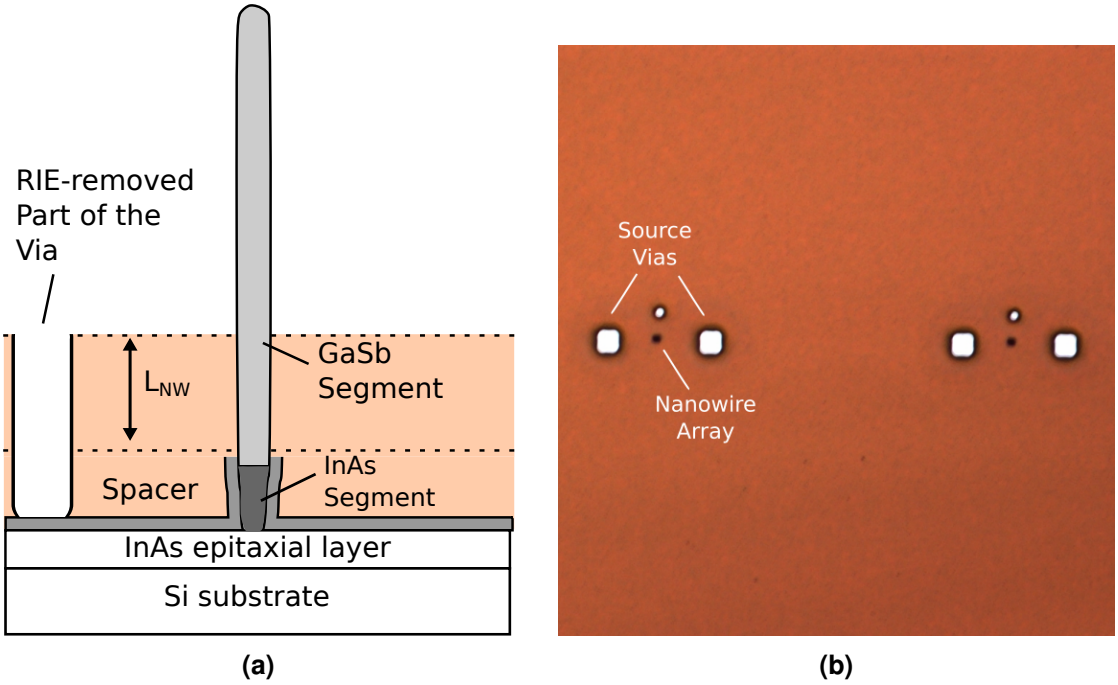


Figure 3.8: Process illustration: RIE of Source-Via holes through the permanent-baked resist layer (a) and the top-down view through optical microscope at 20x magnification (b).

An optical check was performed in order to verify that no left-over resist was present in the vias (figure 3.8b). In order to remove a possible thin photo resist layer that still could be left, the sample was processed by microwave excited oxygen plasma (*ashing*). Once the vias holes were verified as being etched thoroughly down to the source (bottom) contact, the thickness of the spacer at the different stairs was measured by reflectance spectroscopy. If the thickness measurements deviated from the previous measured set, the thickness mapping was redone and the new set of values were instead used as the reference values.

6 Contact and Via Metal Deposition

In order to remove native oxide, the sample was etched in a diluted HF solution. This was performed shortly before the metal sputtering. The contact metal consisted of a combination of nickel and gold. A 15 nm layer of nickel was sputtered first to form a good contact both to the epitaxial InAs (or the sputtered tungsten) layer at the bottom and to the nanowire (figure 3.9a). Immediately after the sputtering of the nickel layer, a 150 nm layer of gold was sputtered (figure 3.9b).

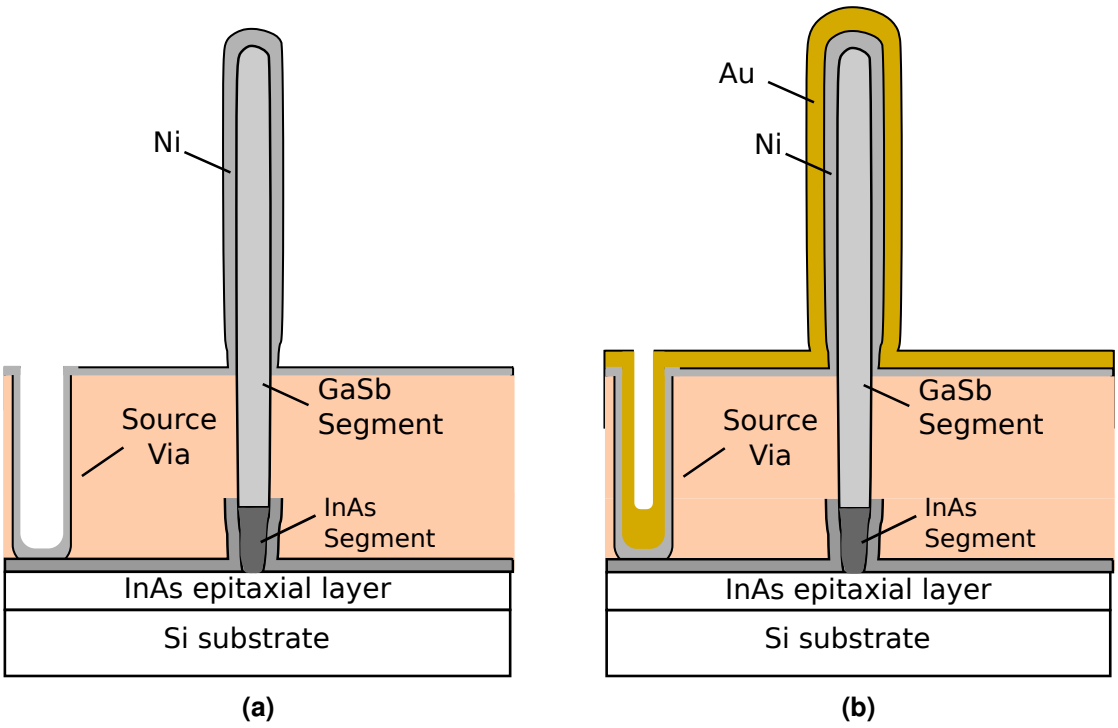


Figure 3.9: The nanowire after 15 nm Ni was sputtered (a) and after sputtering of 150 nm Au (b).

7 Contact Patterning

An illustration of the patterned contacts, with their position relative the source via and the nanowire array, is shown in figure 3.10a. A top-down view of the patterned contact is shown in figure 3.10b. In order to define the contacts, an etch-back mask was used on the area of metal that was to remain protected by resist. A layer of S1828 organic resist was applied by spin coating. The resist was baked longer than typically. Longer heating time at this stage has shown to result in a better area definition. For gold layer etching a

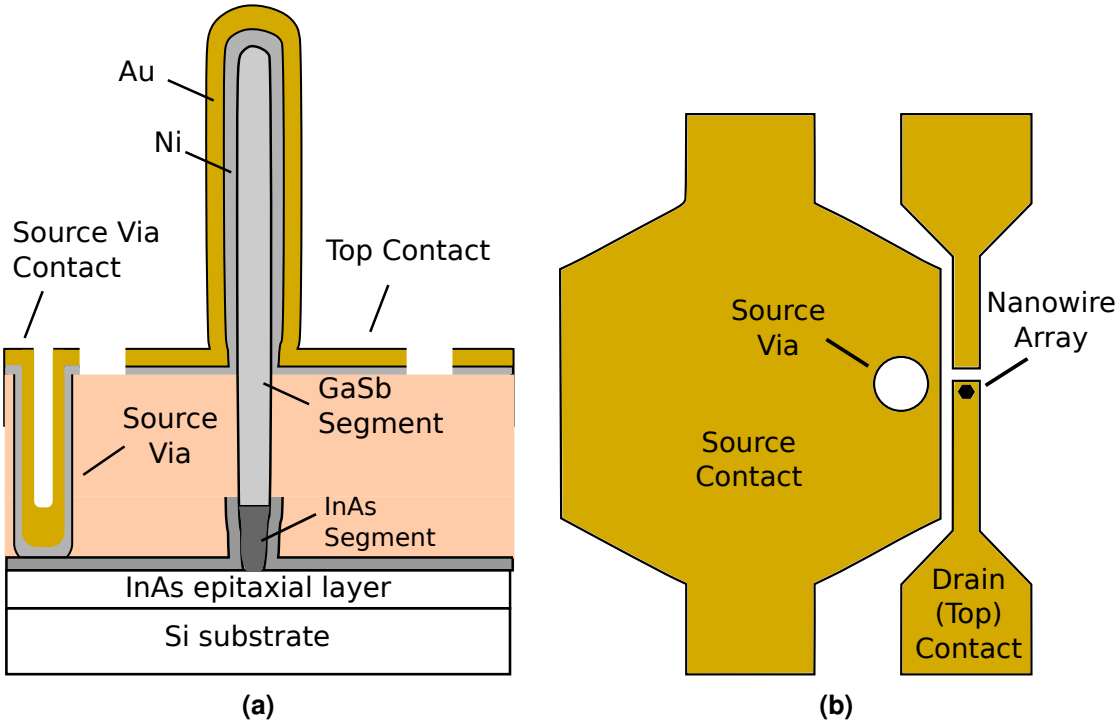


Figure 3.10: Top metal patterned by etch-back, the illustration with one nanowire (a). Contact layout of the source and drain pads, as seen from above (b).

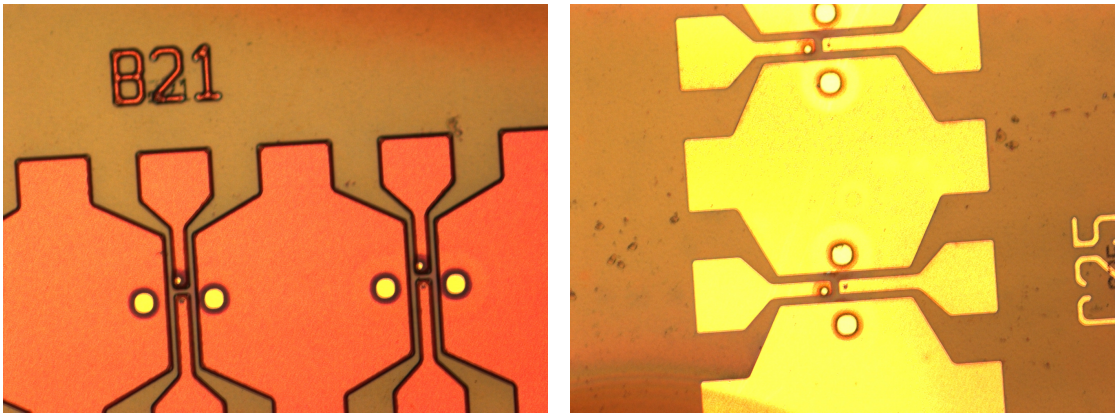
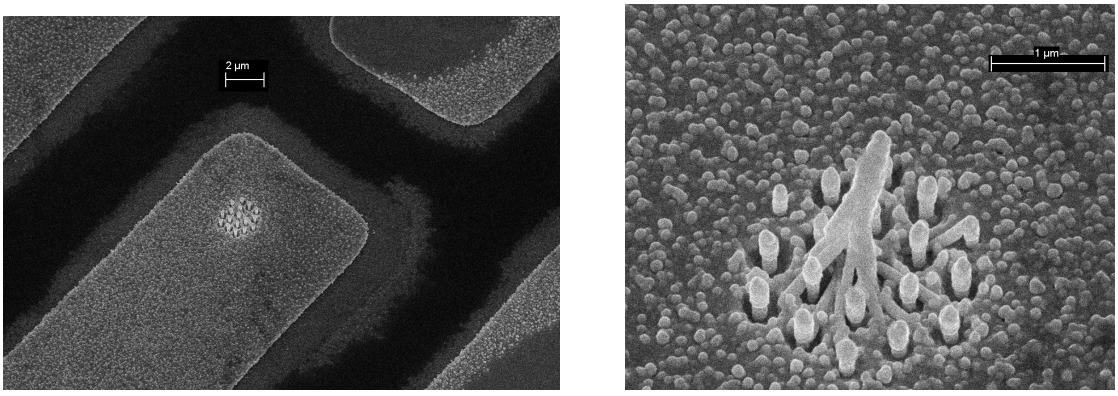


Figure 3.11: Microscope images after the top metal etch-back: Contact pads with resist that masked them during the etching process (a) and with the resist removed (b).

KI solution was used. This process is sensitive to concentration variations, which could result in etch rate variations. The gold layer etching was therefore verified by optical microscope (figure 3.11a). If no gold residue was encountered during the optical check, the nickel layer etching step followed. To this end, a solution of sulfuric, acetic and nitric acid was used. At this point, the etched areas were to only contain resist. This was confirmed by measuring the reflectance (which was distinctively different for S1800 resist and the metals). The resist, which still protected the now patterned metal, was removed and the sample rinsed in IPA. SEM images of a finished nanowire array can be seen in figure 3.12.



(a) **(b)**

Figure 3.12: A complete array as seen at a top-down angle through the SEM (a). A closer view of an array with a few nanowires clustered together (b).

8 Rapid Thermal Annealing

Rapid heating of the fabricated samples has previously shown to decrease specific contact resistivity, attributed to alloying between Ni and the III-V material. Two of the fabricated samples have undergone this procedure for temperatures ranging from 150 °C to 250 °C. An additional reason for performing RTA was possible accumulation of water vapor over time in stored samples. The resistivity of the nanowires increased over time and this could potentially be the cause. Performing RTA on degraded samples has shown to have some effect of restoring performance to levels measured shortly after fabrication.

9 Sample Variations

Three main types of samples have been fabricated. The parameters that were varied were nanowire doping, length and diameter. The GaSb nanowires were grown with an InAs segment. This segment served as a transitional layer between the InAs epitaxial layer on the Si substrate and the GaSb part of the nanowire. In addition, there was tuning of varying degree done to accommodate the different nanowire lengths. One sample contains highly p-doped GaSb nanowires, 2 µm long and with a diameter of 74 nm. Another one were grown to similar nanowire dimensions but with a significantly lower p-doping. The third main type had nanowires 4 µm long and with a diameter of 150 nm.

10 Processing Errors

A number of possible processing faults or errors have been encountered during the manufacturing of the samples. It should be noted that none of these were show-stoppers in regard to the overall development of the process but only a matter of fine tuning. One common defect was that nanowires in the arrays were damaged. Reason for this was likely surface tension, which could result in the nanowires in the arrays to cluster and collapse into each other. This was typically discovered during SEM imaging done between processing stages (figure 3.12b). The highest risk for damage to occur to the nanowire array is during wet-etching steps. For example when wet etching is performed while an array is not completely coated in resist. Furthermore, contact with wet-etchants is inevitable during the oxide removal by HF solution, which is performed shortly before top metal sputtering. Spacer thickness uniformity of the organic resist can also be a factor. In an attempt to mitigate the effects of the varying spacer uniformity, spacer thickness measurements were done as close to the nanowire array as possible.

Chapter 4

Characterization

1 General Procedure

A Cascade 11000B probe station, in combination with a Keithley 4200 parametric analyzer was used to perform I-V characterization of the vertical nanowire resistors on the fabricated samples. The samples contain four rows of GaSb nanowire array resistors each. Each row has 32 such resistor devices. Half of the rows are populated with 19-nanowire arrays and the other with 73-nanowire arrays.

The data from the measurements was stored on file system and processed using scripts written in Matlab. Total resistance of a device was acquired by *least-squares* linear fit of the measured data of the respective device. The measured resistance R_{NW} includes both the contact and the nanowire resistance. The resistance values derived in this way were mapped to the respective spacer thickness of each device. The spacer thickness are the measured values from the reflectance spectroscopy performed earlier. The resistance as a function of spacer thickness data was (least squares) linearly fitted. The resulting fit enabled approximation of nanowire resistance R_{NW}, the transfer length L_T and the contact resistance R_C with the accuracy of each value dependent on how close the measured data points are to the fitted line. The contact resistance is extrapolated from where the line crosses $L = 0$, i.e. no distance between contacts. Note that the extrapolation is necessary because a zero spacer distance in reality would imply a short-circuit. The transfer length L_T is the absolute of the value on the spacer thickness (x-axis) where the fit intersects the zero total resistance point (i.e., zero on the y-axis).

2 Processing of I-V Measurement Data

A two-point probe electrical characterization was done in the range of $-50\,\text{mV}$ to $50\,\text{mV}$. Occasional measurements in the $-1\,\text{V}$ to $1\,\text{V}$ range were performed to check for non-linearities in the measured values. The measured I-V data was used to create a least-squares linear fit for each device and taking the inverse of the slope produces the resistance (figure 4.1). The previously acquired spacer thickness values of each device were mapped to its corresponding resistance. Device resistances were plotted against

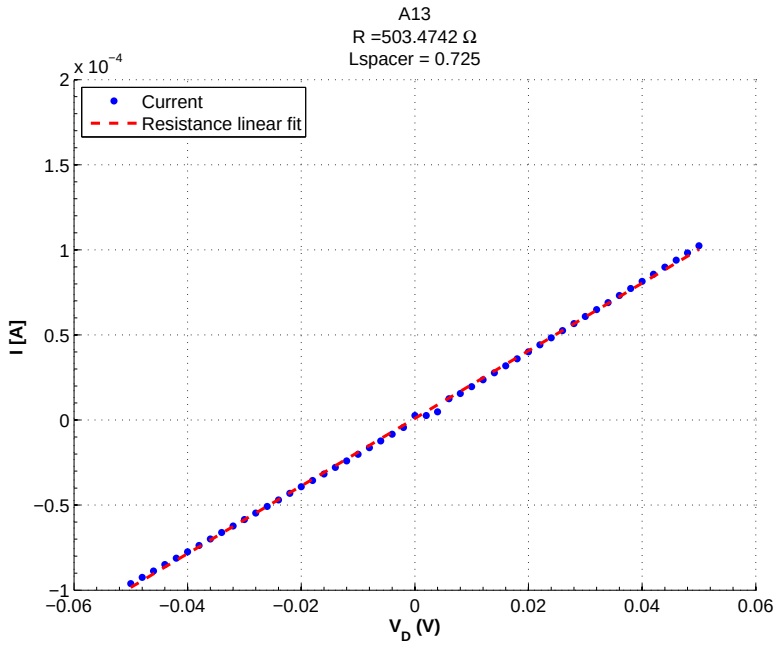


Figure 4.1: An example figure, showing the linearly fitted resistance using the I-V measurement data of a single nanowire array device.

their respective spacer thickness and a linear approximation was calculated. The TLM was applied on the resulting data; the R_C, ρ_s and L_T were extracted and ρ_c calculated, as explained in chapter 2. To minimize influence of process variation on the results, only devices from same row were used for the TLM calculations. The TLM figures from rows that did not produce usable data, typically due to low yield in that row, were discarded.

2.1 Data Sorting

For a number of device rows, there were indications that a number of devices possibly were non-functional, based on the extremely high or the extremely low resistance values

that were measured. These measurement values indicated a high probability of that no electrical path existed through the nanowires for the respective device that was measured. Such values were sorted out from the data-sets prior to application of the TLM. First sorting removed the extremely high resistance values, typically in the MΩ range. Further outliers of the measured resistances were discarded if an argument could be presented to do so. One such argument is indication of presence of a short circuit, which means an abnormally low resistance value. In order to acquire a point of reference for a possible short-circuit, the resistance between two adjacent contact pads, which are connected through the source vias and the tungsten layer, were measured to approximately 5 Ω to 15 Ω. The most common cause for removal of a measurement data point was very high resistance (probable open circuit). In an attempt to analyze this, a focused ion beam milling was performed on similar devices (figure 4.2). Inspection of the cross-section did not provide any conclusive information on whether a short-circuit is present, due to the difficulty of visually discerning the tungsten-nanowire boundary.

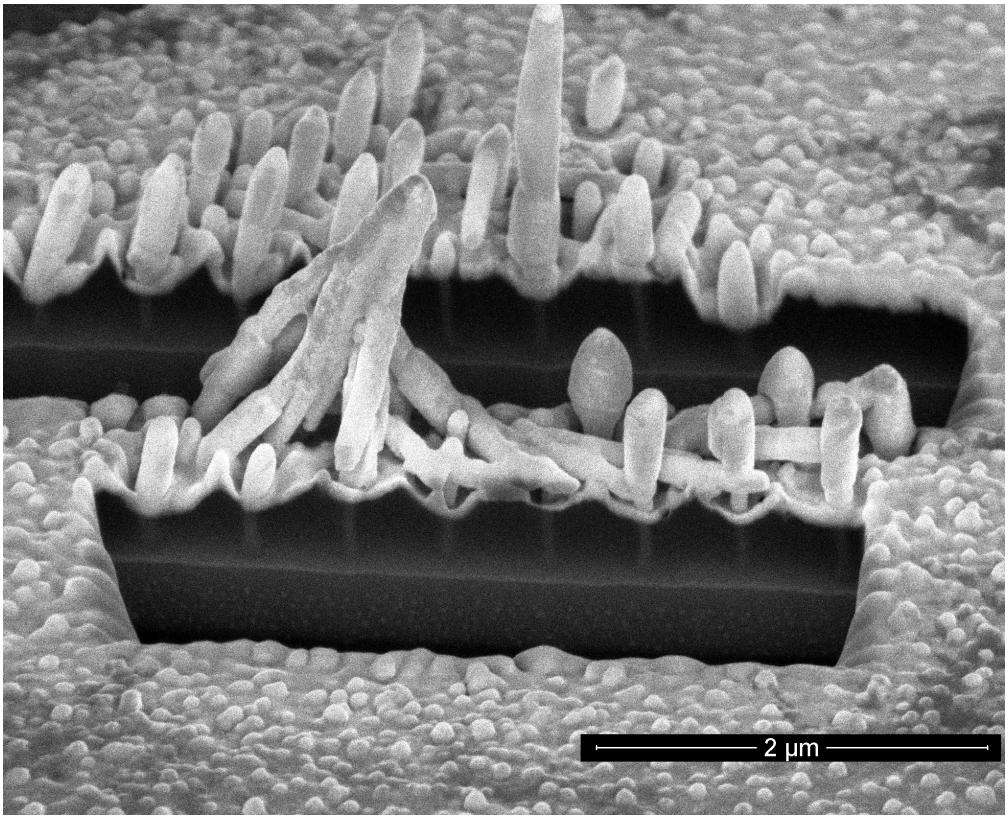


Figure 4.2: FIB milled cross-section of a device on the lowest spacer thickness level.

Chapter 5

Measurement Results

1 Overview

The TLM model has been applied on measured resistance vs spacer thickness data for each device. Measurement data has been sorted with extreme values removed in accordance to the previously explained guidelines. The accuracy of the extracted contact resistance R_C and specific resistivity ρ_c are dependent on the linearity of the measured data. The accuracy varied between measurement sets, possibly due to process variations. Goodness of fit was estimated using R^2 [18]. Results of measurements performed on two separate samples will be discussed. The two samples have similar dimensions (nanowire length around 2 µm, with a radius of 37 nm) but different doping concentration. Rapid thermal annealing at temperatures 150 °C to 250 °C has been performed in order to study its effect on the contact- and nanowire resistivities.

2 Highly P-Doped Nanowires

The nanowires on the sample are 2 µm long with a diameter of approximately **74** nm and a high p-type doping profile. A staircase was built on it with four thickness levels, with devices divided between the thickness levels. A tungsten socket was added in the beginning of the fabrication process to act as the source (bottom) contact to potentially improve the interface between the InAs segment and the GaSb part of the nanowire. The sample has spacer thickness non-uniformity along the edges, which is likely due to the edge-effect resulting from high effect RIE.

Initial Measurements

The I-V measurements were performed using 2-point probes shortly after the manufacturing. The results were verified using measurements with 4-point probes approximately within one week of the initial measurements and the results showed no discrepancies. The total resistance values that were acquired by the linear fit of the I-V measurements of the individual devices are plotted against their respective measured spacer thickness. The extracted ρ_s is approximately 87 Ω µm across four different measurement sessions, which may indicate a good approximation. A higher spread of values for specific contact resistivity ρ_c can be noted. The ρ_s is mainly dependent on the slope of the linear approximation in the TLM model, which may explain why it does not differ as dramatically as the ρ_c, which has the addition of a quadratic relationship with transfer length.

Annealing

Reference measurements were performed prior to the thermal annealing to establish a reference. A rapid thermal annealing procedure was performed in nitrogen atmosphere for 1 min at 150 °C to 250 °C, results of which can be seen in figure 5.1. The extracted contact resistance R_C is ranging from 2266 Ω to 2940 Ω with a decrease happening from 150 °C to 200 °C, after which it starts to increase significantly. The spread in the data results in a goodness of fit $R^2 \approx 0.56$. The extracted ρ_s and ρ_c based on the TLM based on the measured data after annealing at 150 °C to 250 °C can be seen in figures 5.2a and 5.2b, respectively. The average ρ_s remains approximately the same throughout the different temperatures of annealing. This is expected, since ρ_s is the resistivity of the nanowire itself and should ideally not be affected by change in the metal-semiconductor interface (which the RTA procedure is attempting to accomplish). The general trend appears to be an improvement with higher annealing temperature up to 200 °C, after which it starts to decline. The increase with higher temperature seems to be in accordance with similar procedures [6], with the exception of the decrease in ρ_c after 200 °C.

3 Undoped Nanowires

More of devices needed to be discarded on the sample with undoped nanowires, due to errors during processing where less spacer was removed than needed prior to metal deposition. The consequence is that the nanowires located on the thicker levels do not get properly connected by the metal layer.

As expected, the lower doping resulted in an increase in resistivity, as compared to samples with higher doping. A TLM figure based on I-V measurements done shortly after fabrication can be seen figure 5.3a. Measured resistance values which are several orders of magnitude above the mean are discarded. In practice, this refers to measured

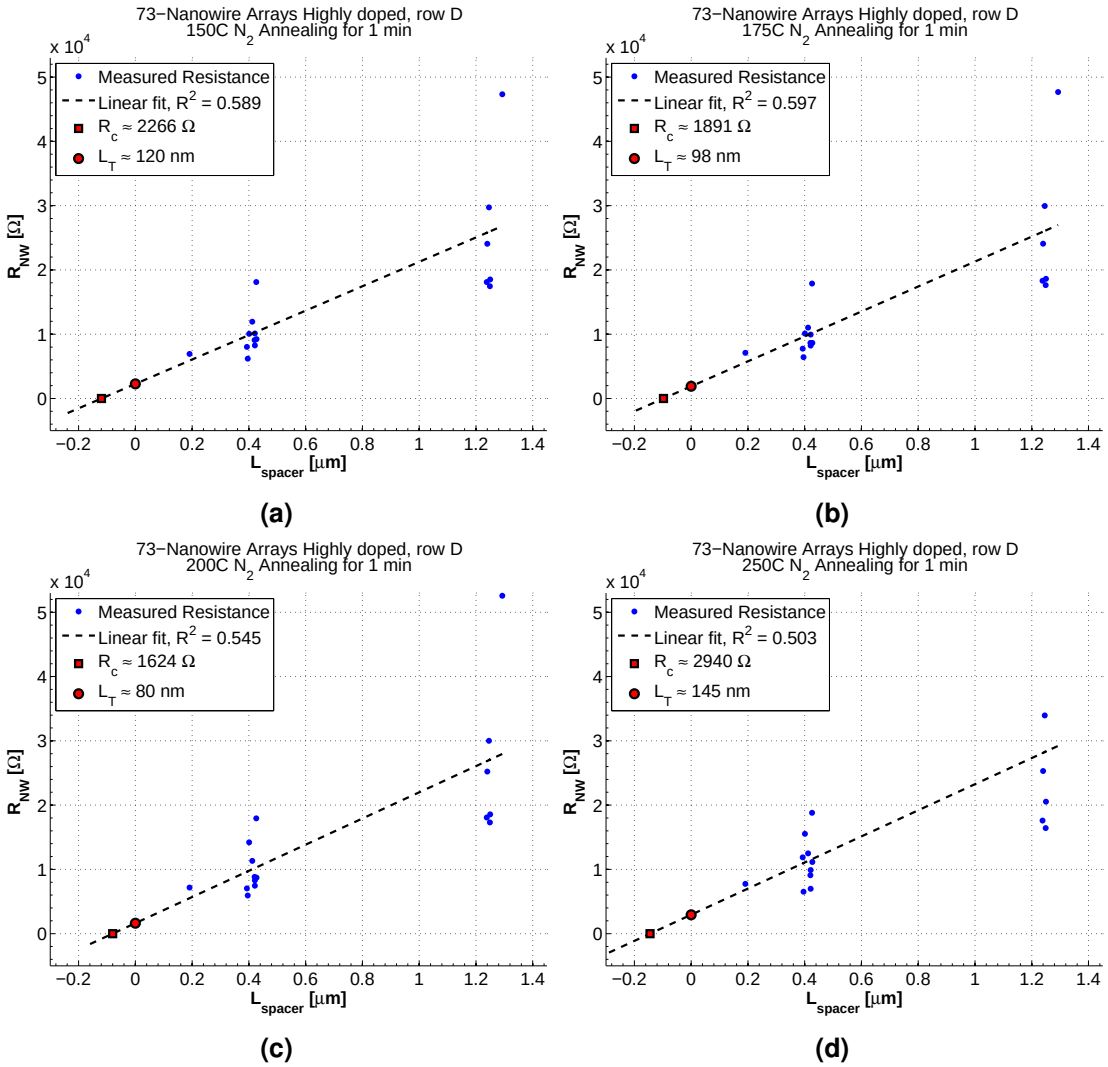


Figure 5.1: TLM figure of the highly doped nanowire devices annealed in N_2 for 1 min at 150 °C (a), 175 °C (a), 200 °C (c) and 250 °C (d).

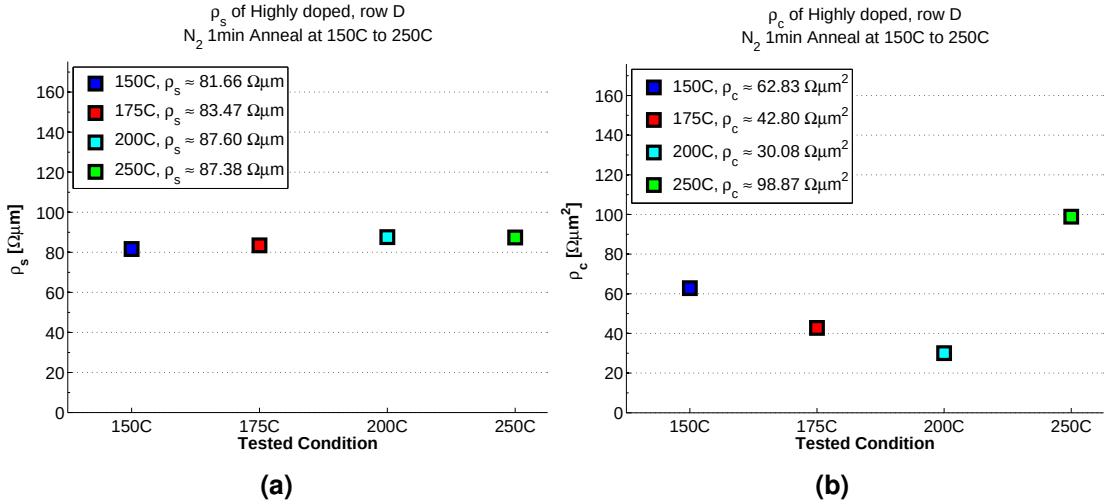


Figure 5.2: The extracted resistivity ρ_s (a) and the specific contact resistivity ρ_c(b) for annealing in N_2 for 1 min at 150°C to 250°C.

device resistances with values in the 100 kΩ to MΩ range. These devices are considered faulty, likely due to an open circuit arisen due to errors in processing. The TLM data of row D (figure 5.3d), containing devices with arrays of 73 nanowires, is selected for further analysis. The spread of data-points from the linear approximation appears to be less severe than the other rows. Possible reason is that the row D is closer to the middle of the sample, where uniformity tends to be better than the periphery. The outer edges of the sample are susceptible to accumulation of un-evenness during repeated RIE, in large part due to the edge effect. Physical wearing during tweezers handling and mask alignment are other factors that contribute to the higher degree of deterioration of edge devices. The accuracy of the approximation results in ρ_s and ρ_c data creates a challenge to estimate a reasonable error margin.

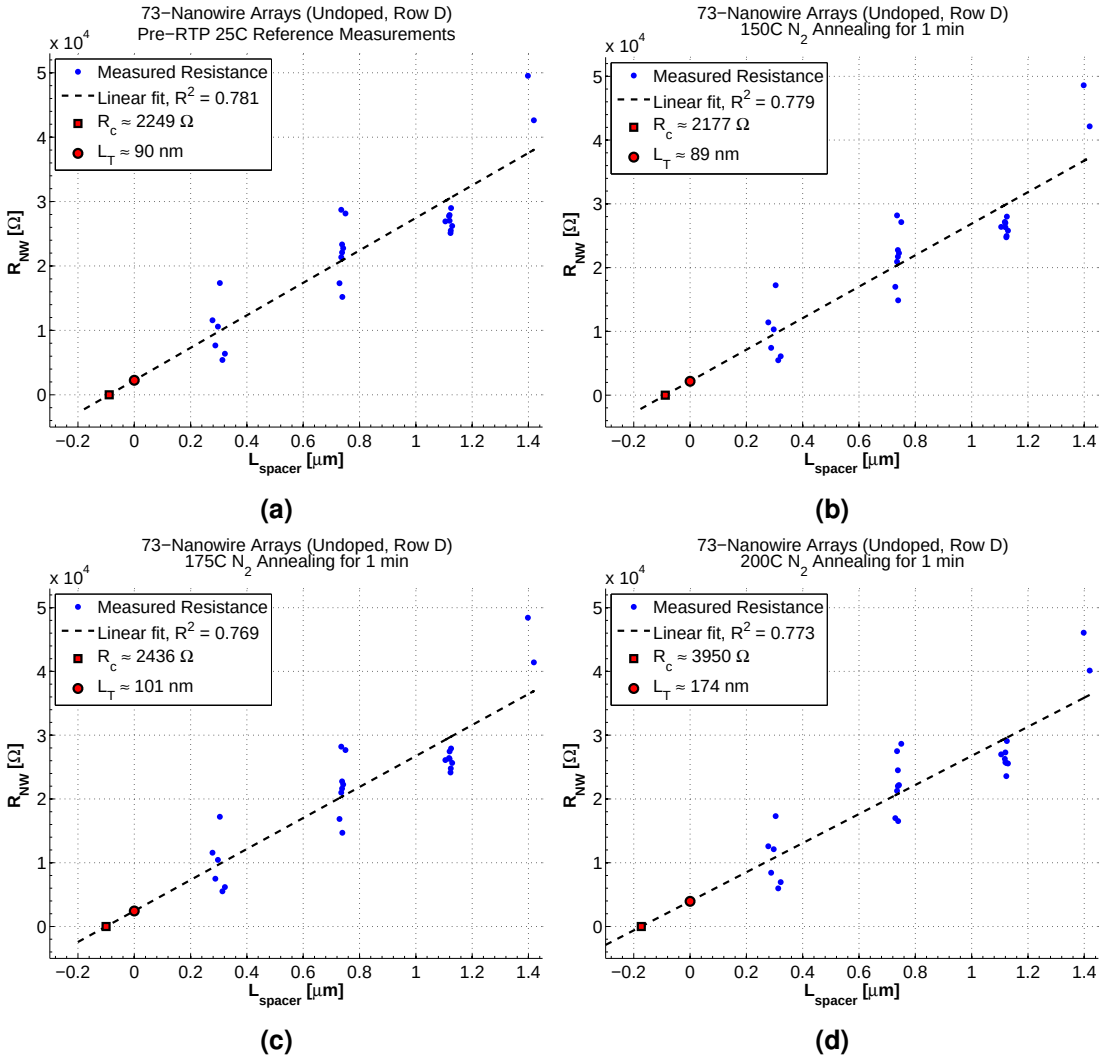


Figure 5.3: pre-RTP to 200C TLM data based on reference measurement prior to performing RTA, all rows.

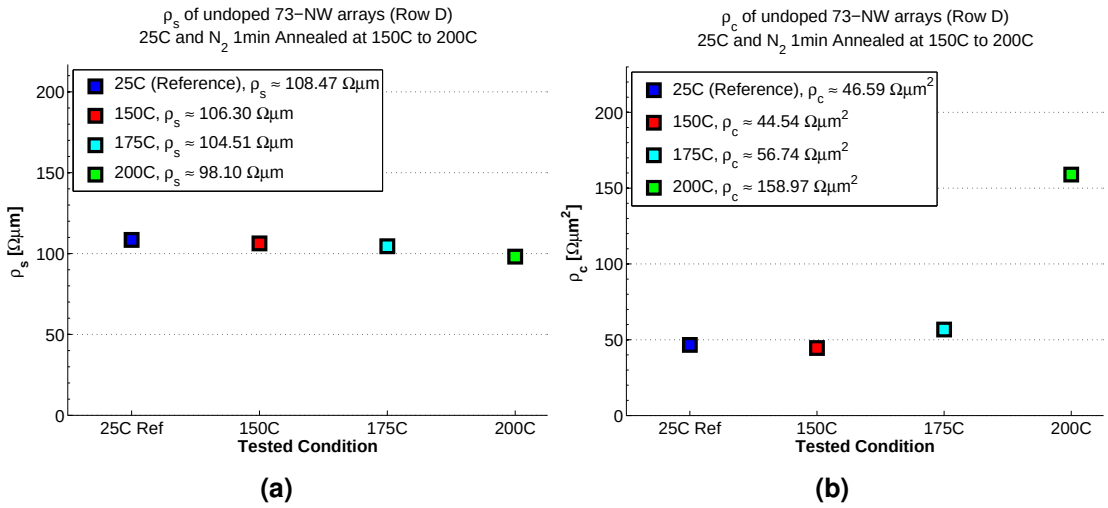


Figure 5.4: Undoped nanowire (73-nanowire arrays): ρ_s (a) and ρ_c (b).

4 Summary

The previously presented measurement results can be seen summarized in figure 5.5. The contact resistance which is extracted from the TLM model at the intersection of the y-axis, which typically is $2R_C$, may need to be slightly redefined. In this case, with a vertical nanowire structure, the dominant contribution to the contact resistance can be argued to originate from the bottom contact. This is possibly due to the tunnel junction present between the InAs and GaSb segments. It should be noted that the presented ρ_c values encompass both contact resistances and that the real ρ_c therefore may be lower.

Undoped Nanowires					Highly Doped Nanowires				
T (°C)	ρ_s ($\Omega\,\mu$m)	ρ_c ($\Omega\,\mu m^2$)	R_c (Ω)	L_T (nm)	T (°C)	ρ_s ($\Omega\,\mu$m)	ρ_c ($\Omega\,\mu m^2$)	R_c (Ω)	L_T (nm)
25	108.47	46.59	2249	90	25	-	-	-	-
150	106.30	44.54	2177	89	150	87.38	98.87	2266	120
175	104.51	56.74	2436	101	175	83.47	42.80	1891	98
200	98.10	158.97	3950	174	200	87.60	30.08	1624	80
250	-	-	-	-	250	87.38	98.87	2940	145

Figure 5.5: Summary of the TLM measurements on the undoped and highly doped 73-nanowire array devices.

Chapter 6

Conclusion

The fabrication of the TLM structure using optical lithography, on substrate with epitaxially grown GaSb nanowires, was performed successfully from a proof-of-concept perspective. The acquired figures-of-merit are within an order of magnitude of similar measurements. As a comparison, a ρ_c of 76 $\Omega\,\mu m^2$ has been reported for a direct Ni-GaSb interface [9]. The acquired ρ_c is in the approximate range of 30 $\Omega\,\mu m^2$ to 158 $\Omega\,\mu m^2$, with the 158 $\Omega\,\mu m^2$ point being a clear outlier. Rapid thermal annealing showed improvement in contact resistivity at 150 °C to 200 °C. This can be compared to the results from tests conducted on InAs nanowires [6].

Results from further variations of nanowire doping concentrations, annealing temperature and duration may be of interest as a follow-up. Additionally, production of several additional samples with similar parameters may be useful for determining the overall process accuracy.

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