

Master's Thesis

Designing and Maximizing Switch-Mode Efficiency of MODPSU, the Modular Power Supply

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Abstract

This work is an investigation into practical design and loss minimization of DC/DC-switched power supplies, enabling cooler operation, smaller size, and additional or wider areas of use.

There is an abundance of switch controller ICs on the market and a few of the manufacturers offer very sophisticated design tools that suggest operating parameters and grade components. However, one of the major losses (inductor AC loss) is not accounted for, so the engineer must combine these results with the ones from inductor manufacturers' loss calculators.

One obvious question is whether you can trust these recommendations and simulation results. This work takes a special interest in inductor losses in relation to input voltage, load current, and switching frequency for a few very common use cases (12V to 3.3V, 12V to 5V, and 9-20V to 12V), where total loss minimization is the greatest concern.

Both a combined simulation of inductor and FET transistor losses and a temperature rise experiment suggest that there is a switching frequency sweet spot (for a given load current and input voltage), where the total inductor and FET losses are at a minimum. However, the efficiency and loss measurement experiments show no sign of it and instead indicate that minimum losses occur at minimum switching frequency (in this case 200 kHz).

One conclusion is that the switch controller design tools recommend a higher switching frequency than what's optimal from a loss minimization perspective or suggest a too low inductance value that would give much higher core losses than what's possible to achieve. The steep left slope of the inductor loss curve is dangerous, so if in doubt choose a higher inductance value.

A comprehensive selection of off-the-shelf inductors from three manufacturers was tested. Only one vendor publishes core material specifications, which incidentally is the only one whose loss calculator stands up to scrutiny (Vishay).

All off-the-shelf inductors in this range come in either of two core materials; Mn-Zn ferrite and iron powder that are both cheap and easy to produce. On average, the iron powder inductors have significantly higher core losses than the Mn-Zn ferrite ones, although one of the iron powder inductors performed on a par with the ferrites but without suffering from the latter's known weaknesses (sudden and highly temperature dependent saturation).

Among the three tested iron powder sizes, size has very little impact on losses (except for the smallest one). The main difference is that smaller inductors heat up and saturate faster and that the lower DCR of a bigger one might result in a higher optimal inductance value.

Surprisingly, low rated inductor DCR correlates to high total losses, indicating a lower quality core material. The body diode of modern FETs is so good that there's no need for an external freewheeling diode. Due to idle losses, dual phase operation only becomes attractive at relatively high load currents. Real-world inductors are far from ideal, so beware of sour spots (unfortunate sets of winding turns, wire gauge, and core size).

As a result of this work, the MODPSU products perform significantly better than the competitor's closest counterparts, with 60% lower total losses.

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- Linear Technology Sweden (DC/DC-switch ICs and lab access)
 - Mats Hellberg and Thomas Ginell
- Infineon (FET transistors)
- Coilcraft (inductors)
- Vishay Dale (inductors)
- Würth Elektronik (inductors)
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CHAPTER 1

1 Introduction

1.1 Background and Motivation

Traditional AC/DC-switched ATX¹ PC power supply units (PSU) have a few disadvantages if you want to build small yet powerful computers:

- Their size and format are a limiting factor in the design and layout of the PC chassis.
- All conversion losses (heat generation) are placed inside the chassis, which creates a need for forced cooling that requires an additional fan that increases noise.
- If you need an uninterrupted power supply (UPS), you have to connect it to an external device that AC/DC switches to charge a battery and then DC/AC switches when discharging. This causes unnecessary conversion losses and bigger total size.

By using an external AC/DC power brick and internal DC/DC-switched PSU and UPS, you could get greater design freedom and less need for forced cooling, equating to smaller and quieter computers. At least the UPS would also benefit from lower losses. There are some existing products of this type on the market, but their power handling capability is insufficient for two important market segments:

- Powerful gaming computers and graphics workstations in a small physical format built with standard PC components.
- File servers with 4-6 mechanical hard drives with or without a built-in UPS.

This report is part of a greater design project aiming to develop a series of PC power supply products that support these additional segments. One of the most important aspects is to minimize DC/DC switch conversion losses, so that heat generation and the physical size of the circuit are no longer a

¹ (including variants such as SFX)

concern. It is hoped that this could be achieved through a more energy-efficient choice of off-the-shelf components, operating parameters, and PCB layout.

This paper presents relevant theory and a series of loss-minimization experiments that aims to give a general practical understanding of the area and determine suitable components and operating parameters for the actual products.

1.2 Problem Definition

A series of load experiments for the target use cases determine the necessary and desired properties for the MODPSU products.

A previous initial investigation of the design of switch-mode power supplies (SMPS) has shown that most circuits, component choices, and values are easily given by the switch controller manufacturers' design tool, but that the selection of optimal power inductor and switching frequency requires further evaluation. The inductor manufacturers' data on core materials is sometimes sparse or non-existing and often their inductor loss calculators report fantastic loss and temperature rise figures. The report's major analysis part will therefore aim to give the knowledge and understanding necessary for selection of optimal inductor and switching frequency, through power loss simulations, temperature rise measurement experiments, and efficiency and loss measurement testing of the finished products.

This report covers only a part of the entire MODPSU development project that involves a significant amount of electronic engineering, CAD work, soldering, testing, microcontroller and PC application programming, and so on. Instead, it focuses on the critical component and design choices for this type of power supply circuits.

1.3 Purposes and Goals

The purpose of the entire project is to define, design, and prototype working, sellable, products that bring something new and better to the market.

The purpose of the report part of the project is to collect, analyze, and compile the information required to make optimal designs for this very common type of DC/DC switch circuits:

- Present the main loss-related theory and properties of SMPS components (topologies, inductors, FET transistors, capacitors, and Printed Circuit Board (PCB) layout).
- Investigate the relationship between core material, core shape, core size, inductance value, winding DCR, switching frequency, and load current for a comprehensive selection of off-the-shelf power inductors available from European and US retailers.

The property summary, results from the simulations and experiments together with the efficiency and loss measurements of very common use cases should give the reader a broad understanding, enabling more well-informed design decisions. As a byproduct, it is also an implicit test of the accuracy of three tools that are potentially highly useful to the designer:

- Recommendations for inductance value and switching frequency given by DC/DC switch circuit design tools.
- Inductor manufacturer loss calculators.
- Switch controller manufacturer design tool efficiency calculation, especially FETs.

1.4 Delimitations

It would have been interesting to include an EMI evaluation of the inductors, but there is very little (if any) manufacturer material on this topic and I have access to only very rudimentary equipment for EMI measurements. Precautions were taken to design the PCBs in such a way as to minimize EMI, but this is as far as this work covers the topic. Please see e.g. the KTH second cycle degree paper by Takeshi Murase on EMI (1) for more information.

1.5 Environmental Aspects / Sustainable Development

Important benefits of these products are low power conversion losses, quiet operation, and reusability of existing components.

The MODPSU products are explicitly designed for long technical and economic life.

1.6 Ethical and other Considerations

I have been in contact with some of the participating manufacturers before the start of this project. There should be no risk of bias when it comes to the evaluation of power inductors (as no personal relationship or dependency exists) or the choice of FET transistors (as they were chosen on recommendation by the DC/DC switch circuit design tool and no evaluation or recommendation is made except to use whatever model is currently ranked the highest by the tool).

Through previous professional contact with the Swedish Linear Technology (LT) tech support, generous supply of product samples, and their kind acceptance to let me do four sets of efficiency measurement tests in their lab, there is potential risk for bias when choosing switch ICs. Part of the reason for choosing LT products is in fact their strong local representation in Sweden. There are two main switch controller decisions for this project. The reasoning is well documented and although the optimal design comprises both switch controller ICs and inductors (and FET transistors and capacitors), the dominating topic of this report is the evaluation of various (types of) power inductors.

This work is orthogonal to questions of discrimination based on gender, ethnic belonging, religious beliefs, and other such matters.

1.7 References

This thesis uses Zotero, Vancouver citation style.

CHAPTER 2

2 Method

2.1 Approach, Methodology, and Limitations

The work starts with a comparative simulation of PSU and UPS FET losses between my products and those of the competitor. The simulation is deterministic and only as good as the tool and my assumption of which components are used by the competitor's buck/boost and UPS products.

Then follow a set of simple load tests on typical use cases (gaming PC, file server, and firewall), used as input when formulating desired product properties. A clamp ampere meter is used on one rail at a time. It doesn't record the top value (and even if it did, there would still be a risk of missing peak values between samples) and only one set of readings is made. There are thus limitations to the accuracy of the results, but as the goal is to find rough estimates of current consumption during peak, idle, and active use onto which a sufficient margin is added, this is sufficient.

The electronic design, CAD work, and assembly part of the MODPSU project is extensive and requires great many decisions. The switch controller design tools are used repeatedly until a satisfactory circuit is found for PSU, UPS, and charger. The datasheet for many different component types are consulted, ultimately leading to a series of component choices. None of this is relevant for the efficiency optimization and hence not covered by this report.

The main topic for this work is application loss minimization through inductor evaluation (used in combination with FETs), which is made in three steps:

1. Inductor and FET loss simulation
2. Inductor and FET temperature rise measurement
3. Efficiency and loss measurement on the finished products

2.2 Design Tools Used

As the switch controller selection results in a choice of Linear Technology's products, their LTpowerCAD II v2² tool is used. It supports many of their active DC/DC switch controllers. Modern DC/DC circuit design tools such as this and e.g. Texas Instruments' WEBENCH³ have a database of currently available components. They also assist the user by ordering the database components by power loss, physical size, and other parameters for the current circuit.

The inductor manufacturers generally publish inductor loss calculators in aid of their customers:

- Coilcraft: Web tool.⁴
- Vishay Dale: Web tool⁵
- Würth Elektronik: WE Component Selector for Windows⁶
- Würth Elektronik: Web tool REDEXPERT⁷ (improved successor to Component Selector)

With the help of LTpowerCAD II v2, the range of usable inductance values and inductor current requirements for each of the circuits are determined. The tool also suggests actual inductors. Based on this, a number of types and models from the above manufacturers are selected.

² <http://www.linear.com/designtools/software/>

³ <http://www.ti.com/lstds/ti/analog/webench/overview.page>

⁴ http://www.coilcraft.com/apps/loss/loss_1.cfm

⁵ www.vishay.com/inductors/calculator/calculator/

⁶ <http://www.we->

[online.com/web/en/electronic_components/toolbox_pbs/Component_Selector_1.php](http://www.we-online.com/web/en/electronic_components/toolbox_pbs/Component_Selector_1.php)

⁷ <http://www.we-online.com/redexpert/>

2.3 Inductor and FET Loss Simulation

The first stage of the evaluation is a series of simulations using the above tools. For each circuit, every inductor is simulated at a number of operating points:

- UPS main 12V buck-boost rail: 4, 8, and 20 A loads at 20 V input (buck) and 200 - 600 kHz in 50 kHz increments and 20 A load at 9 V input (boost)
- PSU (buck): 1, 2, 4, 6, and 8 A loads for both rails (3.3 and 5 V) at 250, 300, and 350 kHz
- 12V SLA 14.6V charger (buck/boost): 1, 2, 4, and 6 A loads at 12 V (boost) and 20 V (buck) at 200 kHz to 400 kHz in 50 kHz increments

The total inductor losses are recorded for each instance and the total FET losses (for the chosen FETs) are added.

Each of these simulations includes those inductors that were assumed to be relevant for the respective circuit.

There are some known limitations and possible weaknesses:

- Simplifications in the manufacturer tools: E.g. the WE tool takes duty cycle into account, but the Coilcraft one doesn't. The Vishay tool assumes a basic circuit with a few additional user parameters that influence the simulation results.
- Unknown internal design of the manufacturer tools: Presumably, the tools are based on mathematical models rather than test data (?). It is unknown how accurate these models are.
- There's a risk of failure to enter suitable values for certain parameters.
- It's likely that there are some data entry errors when manually copying the tool data into the Excel sheet.
- The tools state that the simulation results are uncertain / invalid in some situations, often when the delta current exceeds a certain fraction of the average current and in particular when the operating point is outside of the continuous conduction region. This always happens at low load currents. Lower frequency and lower inductance means higher minimum continuous conduction load

current. In these cases, the results must be verified / adjusted experimentally.

There is no point in doing multiple runs of deterministic simulation tools.

2.4 Inductor and FET Temperature Rise Measurement

The second stage is an empirical experiment, in which a 16.5 V DC source feeds a buck-boost circuit that generates 12 V. As loads, four different halogen light bulb combinations are used: 10 W (0.83 A), 20 W (1.67 A), 50 W (4.2 A), and 100 W (8.3 A). Light bulbs have very low resistance when cold (i.e. not ignited), which is why a pre-heater consisting of four 0.47 Ω power resistors in series is used before the pre-heater is shorted by a switch.

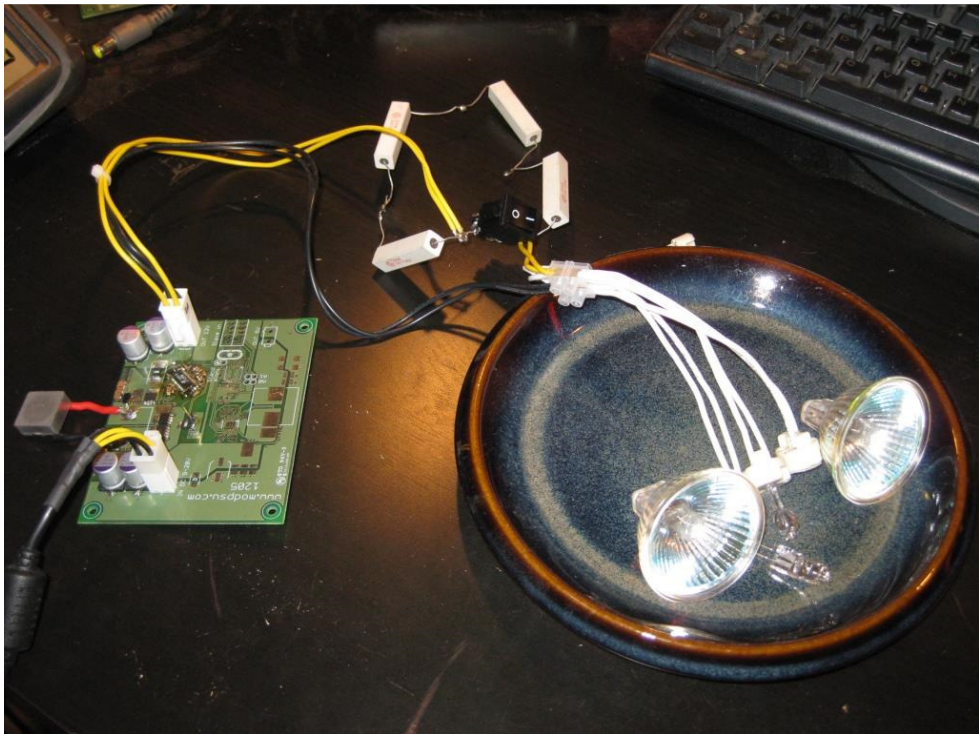


Figure 1: Temperature rise test setup

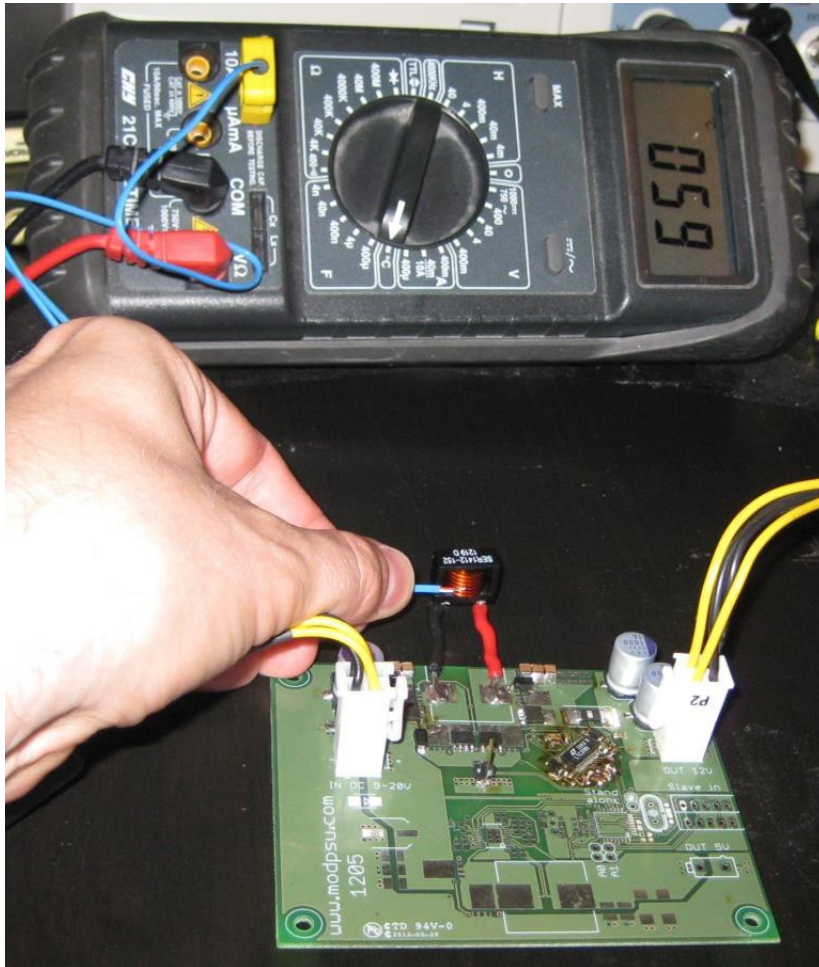


Figure 2: Test subject close-up

These experiments are carried out on one common board based on the earlier generation switch controller LTC3789. The controller itself is very similar to the one used for the actual design (LTC3790), but the circuit is slightly different:

- The 3789 bottom-FET sense resistor is 3 m Ω instead of 1.67 m Ω .
- The 3789 board has no input sense resistor, but the 3790 has one of 1.67 m Ω .
- The 3789 board is equipped with slightly less efficient FETs (PSMN2R2-30YLC and PSMN1R2-25YLC).

- The inductor being measured is not soldered directly onto the PCB, but via two 5 cm wires (1.5 mm²). The added inductance and resistance are negligible (0,015 μH). This makes inductor swapping much easier and enables some separation between inductor temperature and FET temperature measurement. In reality there is some degree of heat transfer.
- The test board is a 2-layer PCB based on 35 μm copper. The new board is a 4-layer PCB based on 70 μm on all layers.

All inductors deemed usable in the simulations (27 in total) are included in the experiment and tested at 3 different switching frequencies for the 4 loads mentioned above.

There are two reasons why this way of measuring / approximating power losses is chosen: It is a way of seeing how the inductor behaves in reality without expensive test equipment and I am explicitly interested in temperature rise, as this affects the need for cooling and the heat generation perceived by the customer.

The known and potential weaknesses are:

- It is difficult to know when the temperature has really stabilized. This is especially the case for the inductor types with a core that is not cast onto the coil, i.e. it has a gap between the coil and the core.
- There are differences in ambient temperature (which is recorded) and possibly also in air flow (which is not measured).
- There might be differences in heat dissipation between the various core materials, coatings, and designs. Some of the inductor cores are semi-shielded, which leaves part of the coil open to the surrounding air. In other words, an inductor with higher losses but better heat dissipation could perhaps give the same temperature reading as a more efficient inductor with worse heat dissipation.
- There is heat transfer between the inductor and the board.
- The board temperature is measured on the plastic (top) side of the buck bottom FET. In this case (buck operation), the main losses are in the buck top FET (switching and DCR losses) and the boost top FET (pure DCR conduction losses). However, the heat transfer on the board is quite good, so measuring close to the center of the FETs is a reasonable compromise.

- It is often desirable to do multiple runs of the same experiment, but it turned out that the inductor temperature measurement (where the temperature is read after I somewhat subjectively concluded that it had stabilized) was so time-consuming that it was not practically possible to do more than one run per experiment setup. Each measurement took roughly 30 minutes per experiment to complete, in total about 40 hours. The test results in some cases give reason to suspect that the particular experiment was terminated a bit too early.

As the same test board was used for all tests, one source of bias was avoided. However, proper testing would have required multiple samples of the same inductor model and multiple measurement runs in order to get an average. This must be taken into account when interpreting the results.

It is unclear how accurate and stable the multimeter temperature probe is, but as we are interested in comparative results rather than absolute values, this should be acceptable.

2.5 Efficiency and Loss Measurements on the Finished Products

Linear Technology kindly accepted to let me do efficiency measurements of the finished products in their lab in Kista. The test setup is:

- TTI EX1810R power supply that can source up to 18 V @ 10 A. (In the fourth measurement a 20 V, 170W power brick was used.)
- Four Agilent U1241B multimeters measuring current and voltage at input and output. Their accuracy is 0.09% + 2 digits (DC voltage) and 0.6% + 5 digits (DC current).
- TTI LD300 DC electronic load that can sink 300 W.

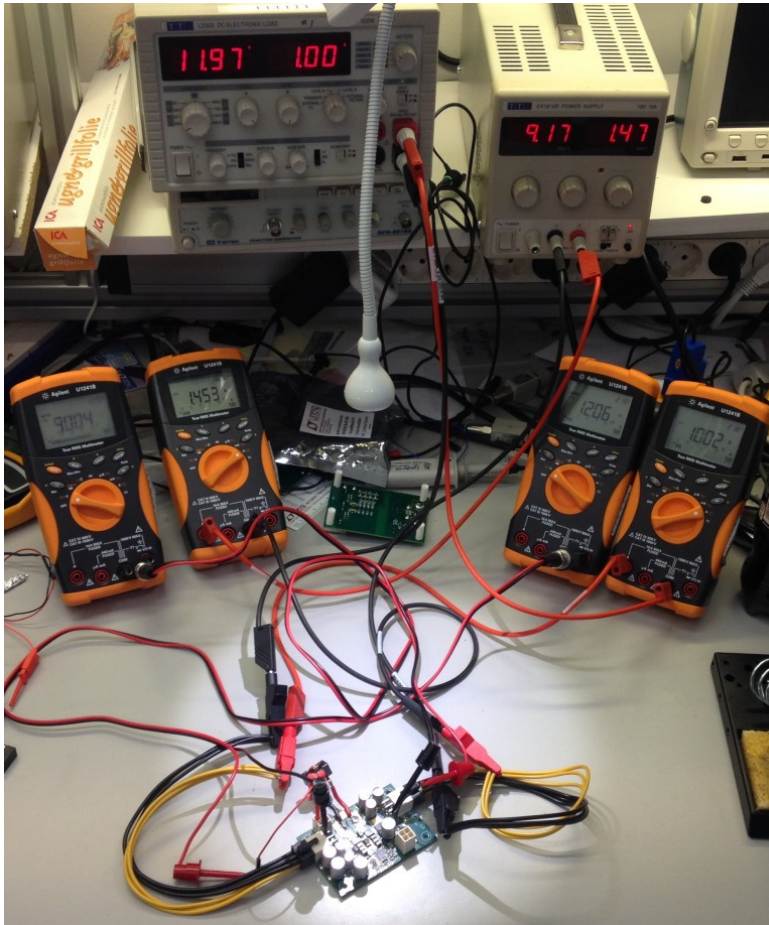


Figure 3: Efficiency and loss measurement test setup

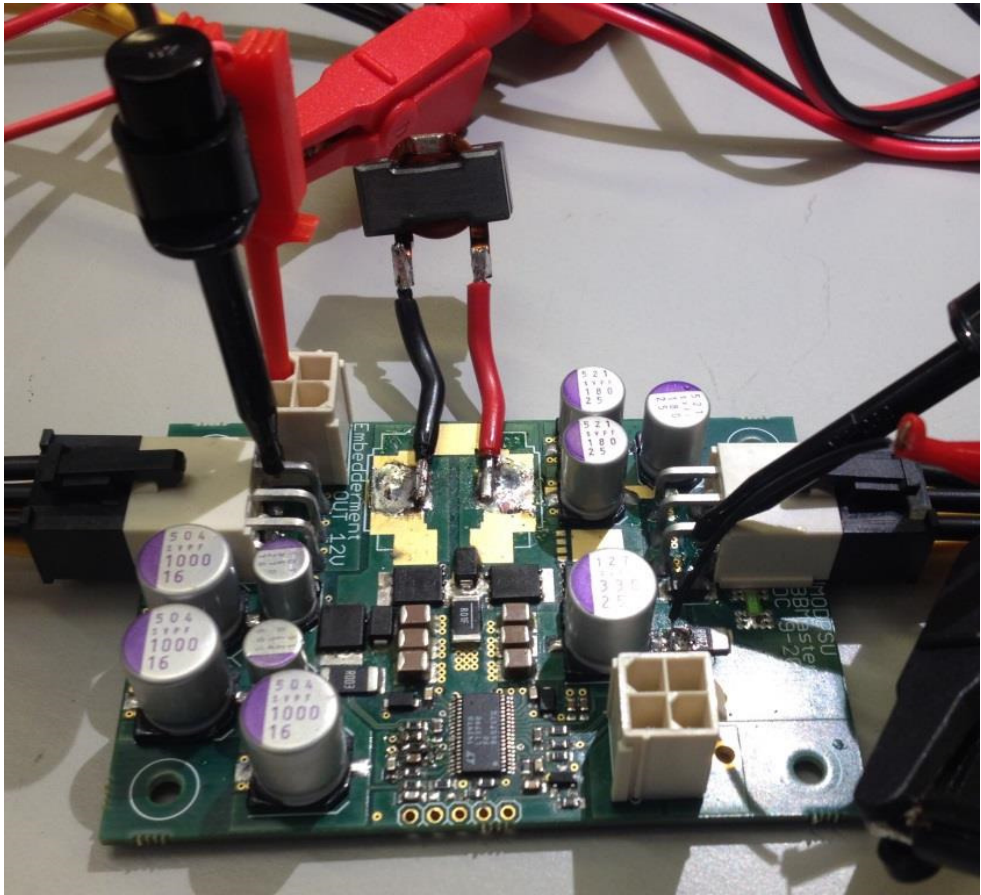


Figure 4: Buck/boost board test subject close-up

2.5.1 PSU 3.3 and 5.0 V Rails

The first revision of the finished PSUs is based on LTC3850 and designed for 12 V input and 8 A per output rail, all @ 250 kHz:

- MODPSU with 3.7 and 4.7 μH Würth Elektronik (WE) HCI1365 (7443551370 and 7443551470)
- MODPSU with 4.7 and 6.0 μH Würth Elektronik (WE) HCI1365 (7443551470 and 7443551600)
- MODPSU with Coilcraft (CC) XAL1010-472 and 562
- MODPSU with Vishay Dale IHL5050FD-3R3-01 and -4R7-
- PicoPSU-120-WI-25 with (probably) two TMP SSC-12880-5R6 HF (2)

The MODPSU PSUs boards are identical (except for inductors and a few small-signal components).

The main losses (per rail) occur in:

- 1.8 m Ω fuse at the input
- Two FET transistors
- The inductor
- Output connector losses (input voltage was measured after the input connector)
- PCB copper and via losses (?)

Each rail was tested independently at 1, 2, 4, and 8 A load.

2.5.2 UPS and Buck/Boost 12 V Rail

Four sets of tests were made. In the first two sets, the finished boards were used with their respective inductor. These are three UPS and two buck/boost (BB) boards based on LT3790 and designed for 12.1 V @ 20 A output from 9 to 20 V input. The BB boards are identical break-outs from the UPS main 12 V rail. The only difference (except inductor and a few small-signal components) is the inclusion of fail-over P-FETs in the input of the UPS.

The frequencies below refer to the first experiment, in which the switching frequency is chosen from the sweet spot found in the initial simulation:

- BB with 3.0 μ H Coilcraft (CC) XAL1580-302 @ 340 kHz
- BB with 2.6 μ H Würth Elektronik (WE) HCI1890 7443556260 @ 300 kHz
- UPS with 2.2 μ H WE HCF2013 7443630220 @ 200 kHz and dual 3.7 m Ω (=1.85 m Ω) fail-over P-FETs (TPCA8128)
- UPS with 2.0 μ H CC SER2011-202 @ 200 kHz and dual 3.7 m Ω fail-over P-FETs (TPCA8128)
- UPS with 2.2 μ H Vishay Dale (VD IH) IHL6767GZ-2R2-01 @ 340 kHz and single 1.6 m Ω fail-over P-FETs (Si7157DP)

The first test results are a bit uneven and as voltage was measured at the connectors, I feared that there might be a bias that I didn't compensate for properly. The fact that the inductors didn't perform as expected caused me to question my simulation results.

At this point I realized that Würth Elektronik's RED EXPERT (RE) tool reports radically higher losses than their Component Selector (CS). The CS results are very similar to Coilcraft's web tool's (especially for their PQ-ish core inductors), which is why I originally didn't question the initial simulation results. The RE results are quite in line with Vishay's tool's higher figures and both indicate that the sweet spot is at a higher frequency than CS and Coilcraft's web tool say. Not knowing who to trust, I decided to do a second set of measurements with all boards running at 368 kHz.

The second test results surprisingly show higher losses for all inductors and they also suffer from bigger random measurement errors that make them difficult to interpret.

The reason why I had chosen to select the best inductor of each type and manufacturer is that I wanted to see how they perform in the actual application. However, at this point I decided to eliminate any systematic bias by doing all measurements on one and the same BB board. A greater selection of inductors was tested at 295 kHz. Two of these were additionally tested at 392 kHz and three at 198 kHz. I also included smaller inductors already found fit for the PSU, in order to see the effect a smaller core has on losses. As a byproduct, this also gave me data for a comparison between single- and dual-phase operation.

Three input voltages (9, 12, and 16) and four output currents (1, 3, 6, and 8 or 12) were tested. Voltage was measured after the input shunt resistor and at the output connector.

A fourth set was made in search of the still elusive total loss minimum sweet spot. My expectations of optimum switching frequency had by this time shifted a few times and I had looked for it from 200 to 392 kHz. The third set surprisingly didn't show the left slope of the U-shaped total loss curve. As I couldn't decrease switching frequency further, I decided to do efficiency and loss measurements on the next few inductance values.

I also needed 20 V input data for the accuracy evaluation of the core loss simulation tools, so (only) this voltage was used instead. Output currents of 1, 2, 3, 4, 6, 8, and 12 A were tested for compatibility with simulations and previous measurements. Only 198 kHz switching frequency was tested.

The main losses occur in:

- 1.8 m Ω fuse at the input
- 1.85 m Ω or 1.6 m Ω fail-over P-FETs at the UPS input
- 2 m Ω input current sense resistor
- 1.67 m Ω inductor current sense resistor
- 3 m Ω output current sense resistor
- Four FET transistors
- The inductor

The efficiency measurements potentially suffer from two sources of errors due to the fact that only one reading was made per run:

- Reading or typing error when entering the multimeter reading into the Excel sheet.
- Concurrency error when collecting data (input voltage + current and output voltage + current) that might be fluctuating slightly in the middle of the reading.

In the third and fourth measurements I took great care to identify and amend these errors during the testing. The consistency of the results suggests that my efforts were rewarded.

All measurements were made on room-temperature equipment. The entire process is so quick that core heating has (probably) not had time to affect core losses to the full degree. A better test would take this into account, but that would have been quite time-consuming.

Doing multiple readings on each sample would give a more accurate average, as would testing several samples of each inductor. However, this would have taken far more time than what was available.

CHAPTER 3

3 Preparatory Work

There seems to be one established company selling this kind of products on the market, Mini-Box. It invented or at least was the first to commercialize this type of PSU and UPS products. The company dates back to 1996. (3) It filed for a US patent on a “Monolithic plug-in power supply” on 2005-12-15 (4), but it is not clear what part of this invention it aimed to protect. The only part that is not industry-standard technology is the soldering of the motherboard power connector directly onto the PSU PCB. It is a nice design idea but no rocket science. Either way, the patent expired in 2013 due to unpaid 4th year patent fees (5).

Throughout this work, I am benchmarking against some of the competing Mini-Box picoPSU products. This is partly to understand why they have such poor power handling capability (6) and partly to see how well my MODPSU products are doing.

3.1 FET Simulation Benchmarking

3.1.1 FET Losses

Does the power limitation of the Mini-Box products depend partly on their choice of FET transistors? Let’s do an LT PowerCAD II comparison of PSU FET losses. MODPSU uses the BSZ and BSC models. The pico-PSU-120WI-25V is equipped with FDS6680A and the picoPSU-160-XT with AO4420:

FETs	Top	Bottom	Total	Top	Bottom	Total
	3.3 V, 2 A			5 V, 2 A		
BSZ036NE2LS & BSZ018NE2LSI	0,07	0,03	0,1	0,07	0,03	0,1
FDS6680A	0,1	0,07	0,17	0,09	0,08	0,17
AO4420	0,11	0,08	0,19	0,12	0,07	0,19
	3.3 V, 8 A			5 V, 8 A		
BSZ036NE2LS & BSZ018NE2LSI	0,22	0,21	0,43	0,24	0,18	0,42
FDS6680A	0,5	0,74	1,24	0,61	0,62	1,23
AO4420	0,53	0,7	1,23	0,64	0,6	1,24

Table 1: PSU FET loss comparison MODPSU - picoPSU, Watts, 250 kHz

Below is a comparison of 12 V buck/boost FET losses:

FETs	Top	Bottom	Total	Top	Bottom	Total	Grand total
	Buck leg			Boost leg			
20->12V, 4A							
BSC024NE2LS & BSC010NE2LSI	0,25	0,04	0,29	0	0,02	0,02	0,31
FDD6680	0,31	0,15	0,46	0	0,28	0,28	0,74
20->12V, 12A							
BSC024NE2LS & BSC010NE2LSI	0,58	0,14	0,72	0	0,16	0,16	0,88
FDD6680	1,65	0,95	2,6	0	2,08	2,08	4,68
20->12V, 20A							
BSC024NE2LS & BSC010NE2LSI	1,1	0,31	1,41	0	0,43	0,43	1,84
FDD6680	4,07	2,48	6,55	0	5,69	5,69	12,24

Table 2: Buck/boost FET loss comparison MODPSU - picoPSU, Watts, 200 kHz

The difference for the PSU is great and for the buck/boost stage it is even greater. 12 A is the maximum rated continuous output current on the M4-ATX PSU that uses FDD6680. (It is not possible to read the component print in the low-resolution pictures of the DCDC-USB-200 buck/boost, but as it is using the same basic design as the M4-ATX 12 V rail, it is likely that they contain the same or similar FET transistors.)

There is thus much room for improvement, i.e. a possibility to build a range of products with quite a lot greater current handling capability.

3.2 Load Experiments

A small number of experiments were carried out in order to determine what currents must be delivered on system input and each of the separate output rails. The equipment used was:

- DELL DA-2 AC/DC power brick that supplies 12 V @ 18 A.
- Mini-Box pico-PSU-120WI-25V DC/DC-switched PC power supply that supplies 3.3 V, 5 V, 12 V, and -12 V to the motherboard.
- Slave devices that supply 12 V (and also 5 V for the hard drives).

Each set of experiments are made on different (generations of) motherboard, CPU, and RAM. These data are presented together with the experiment results.

I make a fair amount of extrapolation and assumptions in this section. While this may seem a bit lax at this point, this uncertainty is taken into account when (over-)dimensioning the actual products. This test is for ballpark figures.

3.2.1 High-Performance Gaming PC

It is a matter of opinion what constitutes a powerful gaming PC, but it is common knowledge that most games do not yet benefit much from more than four cores. (7) The current consumption test on the gaming PC was made on the following hardware:

- Intel i5-2500 quad-core, 3.3-3.7 GHz, Thermal Design Point (TDP) 95 W. It is one of the most powerful quad-core CPUs of its generation.
- Gigabyte GA-B75N mini-ITX motherboard
- ASUS GTX660 non-overclocked graphics adapter
- 2 * 4 GB DDR3 1333 CL9 RAM
- Intel SSD hard drive
- Windows 7 64 bit Home Edition

This platform (Sandy Bridge CPU and Ivy Bridge motherboard) is a few years old, but this is actually to our advantage in this case. Later generations have a lower TDP, which roughly put is the average power

consumption ceiling of the CPU. The test results are thus functionally valid with a margin for later generations as well.

Rail	Windows 7 Experience Index	Left4Dead 2 1920x1080 all maxed
Total current @12V	16.7	No data
GPU input @12V	5	2
ATX input @12V	2.2	2.5
PSU input @12V	7.1	5.8
3.3V PSU output	1.5	2
5V PSU output	2.3	2.2
12V PSU output	5.6	4

Table 3: Gaming PC current consumption, individual top readings, Ampere

I have not made a thorough search for the most power-hungry test suite, but I believe that the Windows 7 Experience index is a decent tool for this purpose. Its purpose is to grade the PC's hardware, supposedly so that applications can use these figures for default settings. Please note that the figures are not concurrent, but individual top readings. In some cases, the (somewhat dated) game taxes the individual rails harder.

Please also note that the motherboard has not been compared to other ones. There might be differences in terms of which rail is used to power e.g. the RAM, the CPU, and the chipset. A sufficient margin must be used for each output rail of the MODPSU PSU.

3.2.2 File Servers

Two file servers with very similar hardware were tested:

- Intel Core2Duo E8400, 3 GHz, TDP 65 W. This was one of the top dual-core models from two generations before the i5-2500.
- Zotac G43-ITX-A-E mini-ITX motherboard with gigabit ethernet
- 2 * 2 GB DDR2 800 CL5 RAM
- Mechanical hard drives in RAID5 configuration, either
 - 6 * 2 TB Samsung F4 HD204UI 5400 rpm or
 - 4 * 4 TB Hitachi Deskstar 7K4000 7200 rpm
- openSUSE Linux 12.3 Linux. One is 32 bit and the other is 64 bit.

Rail	6*5400 rpm startup	4*7200 rpm startup
Total current @12V startup peak	11	11.5
Total current @12V idle	5	5
5V HDD output startup peak	1	No data
5V HDD output idle	1	No data
12V HDD output startup peak	5	No data
12V HDD output idle	1.2	No data

Table 4: File server startup current, Ampere

There are many things to say about these two file servers:

- The E8400 is much more powerful (and power hungry) than what is really necessary for a RAID5 file server
- Both types of hard drives are desktop (not explicit Network Attached Storage (NAS)) drives. They are thus optimized for speed rather than low power. (But I have no knowledge of what is the peak current effect of that.)
- Other hard drives could potentially have higher current consumption, but roughly these figures should be generally applicable.
- The motherboard's SATA controller (Intel chipset) does staggered spin-up, i.e. starts the drives in sequence so as to minimize total concurrent spin-up current. I do not know whether all SATA controllers do this, but I assume that later generations have not lost this feature.
- A 6 * 7200 rpm configuration should also be supported, but the data is insufficient for certain predictions of this kind. It seems that the staggered spin-up takes care of much of the peak current problem. It is not unreasonable to think that the 4 * 7200 rpm output figures are similar to the 6 * 5400 rpm ones. That should mean that the idle currents for 6 * 7200 are within 150% of those for the 6 * 5400 configuration. With any luck, total 12 V idle current should be below 8 A and the total peak current well below 15 A.

The above test results are peak startup current and idle current. Another relevant measure is current consumption in active operation (write or read via gigabit Ethernet):

Total current @12V	6 * 5400 rpm	4 * 7200 rpm
Copy large files to SMB 6-drive RAID5	5.0-8.0	No data
Read large files from NFS 6-drive RAID5	5.0-7.0	No data
Read small files from NFS 6-drive RAID5	5.0-5.5	No data

Table 5: File server active operation current, Ampere

“Large files” in this case means 2-5 GB, while “small files” means the whole spectrum of program files and user data, from a few bytes to several MB.

- RAID5 does parity calculation when writing, which probably accounts for most of the difference for large files. There could be performance differences between the SMB and the NFS file transfer protocols that affect the network throughput (and hence the pressure on the disk subsystem).
- An educated guess suggests that the 4 * 7200 rpm figures are similar to the 6 * 5400 rpm ones, which should mean that the 6 * 7200 rpm configuration figures should be within 150% of the ones for 6 * 5400. It can be assumed that active operation doesn’t exceed start-up peak current consumption.

3.2.3 Firewall

The firewall is a general-purpose server that also handles low volumes of web-mail, DHCP, and routing.

- Intel Celeron G1610, 2 cores, 2.6 GHz, TDP 55 W. This CPU is the entry into the generation following the i5-2500 (Ivy Bridge). According to benchmarks, its performance is on a par with the E8400, but much more power conservative than the TDP suggests.
- ASUS H61M-F micro-ATX Sandy Bridge motherboard
- 3 Gigabit Ethernet interfaces
- 2 * 2 GB DDR3 1333 CL9 RAM
- 2 Intel SSD hard drives in RAID1

Total current	@ 16.5 V (actual)	@ 12 V (calculated)
Start-up peak	1.9	2.6
Idle and average operation	1.1	1.5

Table 6: Firewall start-up and average operation current, Ampere

This is clearly at the other end of the spectrum. Is it possible to maintain high efficiency across such different loads or should there be dedicated PSU and UPS products for this range?

3.3 *Desired Product Properties*

The load measurements show that the traditional ATX power supply requirements have very little to do with actual power consumption. Typically, the gaming computer such as the one in this test would need at least a 450 W ATX power supply to be able to deliver enough (startup) current on the 12 V rail(s). This is twice the actual top-level need, three times the average gaming power consumption, and much more than web browsing and office applications demand.

It is thus less relevant to talk about a common PSU power limit, as the 12 V rail is switched on/off and modern FET transistors are very low-loss. Both the 3.3 and the 5 V rails require fairly little power. For the gaming PC, workstation, and file server, 8 A maximum current on each of these two rails is quite enough. The firewall and office PC segment would do fine with about half of that.

3.3.1 PSU

In order to make the PSU small yet powerful enough, it must be fed by 12 V DC so that the rail that supplies the most is just switched on and off. This places most of the heat generation elsewhere. As concluded above, two models would cover the actual need; 4 A or 8 A maximum on each of the 3.3 and 5 V rails.

The PSU should have about 90% efficiency at 1 A (or 2 A) for both the 3.3 V and 5 V rails and about 95% maximum efficiency. It should run cool at 4 A average load per rail.

The PSU should (in all relevant aspects) conform to the current ATX specifications, especially in terms of signaling.

The PSU should indicate when connected to power and when switched on.

Standby current consumption should be low.

With the decision to use a 6-pin Molex Mini-fit JR or HCS connector for the power input (as this connector type is also used to power the GPU), there is one natural current limit at 24 A (3 * 8 A for 6-pin JR) and one at 33 A (3 * 11 A for 6-pin HCS). This boils down to slow-blow input fuses of

20 A (240 W) or 25 A (300 W). The current carrying of the PCB must be tested on the finished product. 20 A should be the initial design value.

3.3.2 UPS

The UPS must be able to operate on the entire voltage range of a 12 V SLA battery (which is from about 12.7 V when fully charged to 8-10 V at high-current discharge termination. (8) ⁸ The low-end limit depends on discharge current and the maximum capacity (“size”) of the battery. Very little capacity is left below 10 V. The UPS thus needs a buck/boost main rail.

The UPS has four main subsystems:

- Power conversion to 12 V output: The current measurements indicate that file servers, general-purpose servers, and gaming PCs have different power consumption needs. At this stage, only one product will be designed, for file servers with up to 6 * 7200 rpm hard drives. This means that it should run cool when idling at about 5-8 A, active at about 8-12 A, and provide sufficient (short-term) spin-up current delivery. The minimum supported input voltage must be the lowest usable battery discharge voltage (9 V, which leaves a design margin to 10 V) and the maximum supported input voltage must be high enough to support commonly available AC/DC power bricks. Although a 12 V brick is recommended, many laptop manufacturers have chosen 16 V or 19-20 V. For this reason, 20 V maximum input voltage was decided, which also enables use of 25 V bulk capacitors.
- Battery chemistry, voltage, and charging: Lithium-based batteries have been turned down due to safety precautions and shipment regulations. 12 V SLA (Sealed Lead-Acid) batteries are a de facto standard in UPS systems, they are safe to use and easily available. NiMH batteries were considered but they seem to offer little more than SLA, so the decision is to only support 12 V SLA batteries. They can typically be bulk charged at about 14.5 V and trickle charged at 13.5 V, as the battery chemistry absorbs low-current over-charging by heat generation. The bulk charge current should be user-selectable, capping it at a current that both the battery tolerates and the AC/DC power brick can deliver in excess of peak system current consumption. As a starting point, 6 A should be the

⁸ <http://www.yuasaeurope.com/images/uploads/uk/images/charts/NP/np-discharge-characteristic.jpg>

maximum charge current, but temperature rise might restrict this figure.

- Fail-over from AC/DC power brick to battery and back: This should be over-rideable so that the battery can be cycled (discharged and then charged) and hence the current battery capacity (expected run-time) can be determined. In order to avoid forcing the user to manually set the fail-over voltage, 12 V input from AC/DC power brick is chosen as the minimum supported one on this input. Fail-over should have hysteresis, so that it will be clearly in one state at any time.
- Micro controller for monitoring of voltages and currents, fail-over status, listening/responding to ATX signaling, and communication with PC application over either USB or RS232.

The UPS should both be able to operate in two modes:

- By serial communication with a PC application. (At least “PC has completed boot” and “battery discharged, do graceful shutdown”.)
- Completely independent from the load.

3.3.3 Buck/Boost Board

In order to be able to use the PSU together with an AC/DC power brick at another voltage than 12 V, power conversion is needed. As mentioned above, the laptop bricks typically supply 16 V to 20 V and the UPS should support 12 V to 20 V on the AC/DC brick input.

The problem is that the file server spin-up current exceeds what a typical laptop brick can deliver. A simple way around the problem of too high start-up current consumption in the UPS could be to force fail-over to battery at the beginning of the boot sequence and then fail-back to DC input. This would enable use of 120W AC/DC power bricks for the 6 * 5400 and 4 * 7200 drive configurations and provide a simple way to test the health of the battery at spin-up, when a failure would cause no or at least the least damage.

CHAPTER 4

4 SMPS Design and Component Properties

4.1 DC/DC Switch Topologies

The MODPSU products need to:

- Step down (buck) from 12 V to 3.3 and 5 V
- Convert an input of 9 - 20 V into 12 V (buck/boost)
- Convert an input of 12 - 20 V into 14.5 or 13.5 V (buck/boost)
- Invert +12 V to -12 V at very low load

All of these circuits are non-isolated. The inversion stage is a simple capacitor charge pump, so it is not covered here. Only steady-state operation is considered.

4.1.1 Basic Buck and Boost Topologies

Buck/boost is often considered a topology of its own, but the switch controller used by MODPSU is a four-switch design that transitions from pure buck to pure boost via two intermediate hybrid modes (and vice versa). Its operation is thus also better explained by the two basic modes:

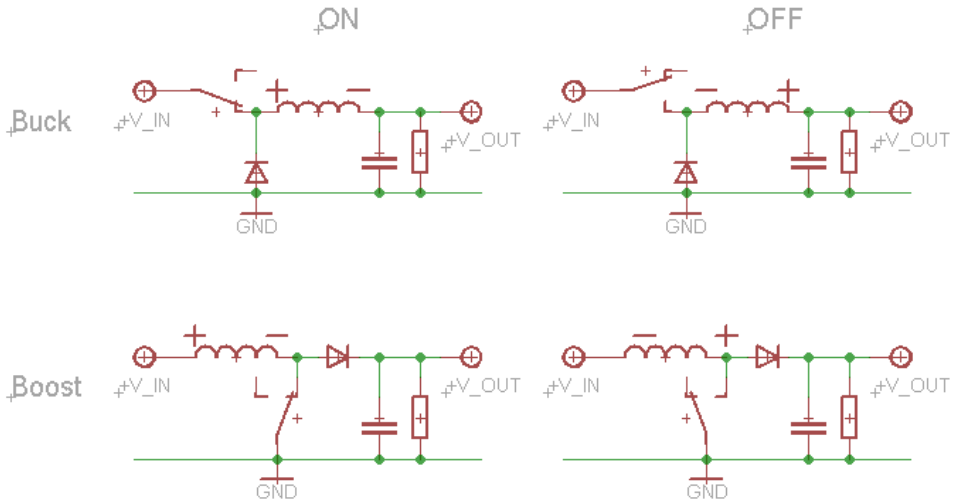


Figure 5: Basic buck and boost topologies (9)

Energy is stored in the inductor when the switch is ON and released into the output when the switch is OFF.⁹

In buck mode when going from ON to OFF, current instead flows through the diode until the energy is consumed.

In boost mode when going from ON to OFF, the previously built-up short-circuit inductor current is instead sent into the diode, which causes a higher voltage on the output side of the inductor than on the input side.

Both circuits have two main modes of operation; continuous and discontinuous (inductor) conduction:

⁹ Please see 4.3 for more information.

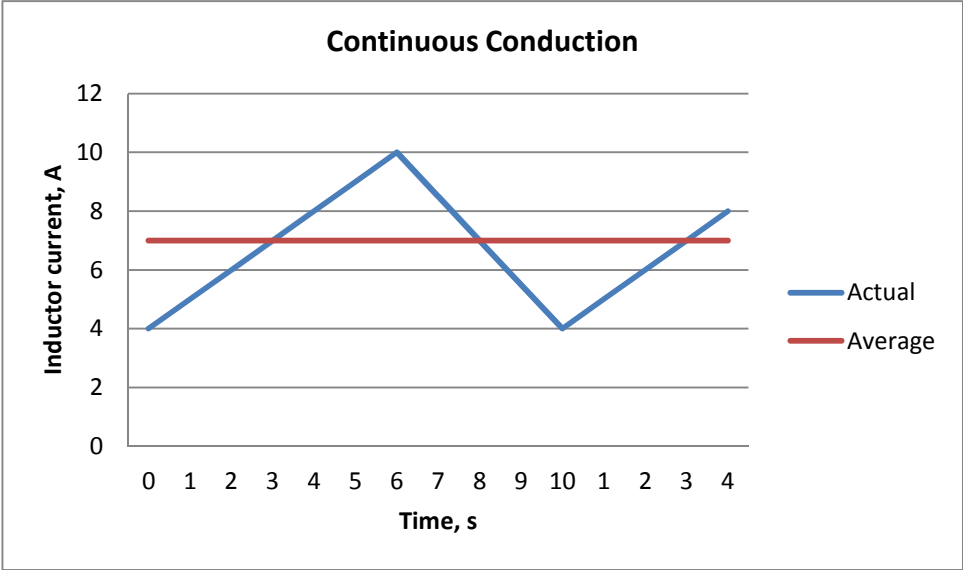


Figure 6: Continuous conduction

In continuous conduction, inductor current never reaches zero. When the average output current is reduced, at some point the load current becomes so low that no current flows through the inductor during part of the cycle. This is called discontinuous conduction.

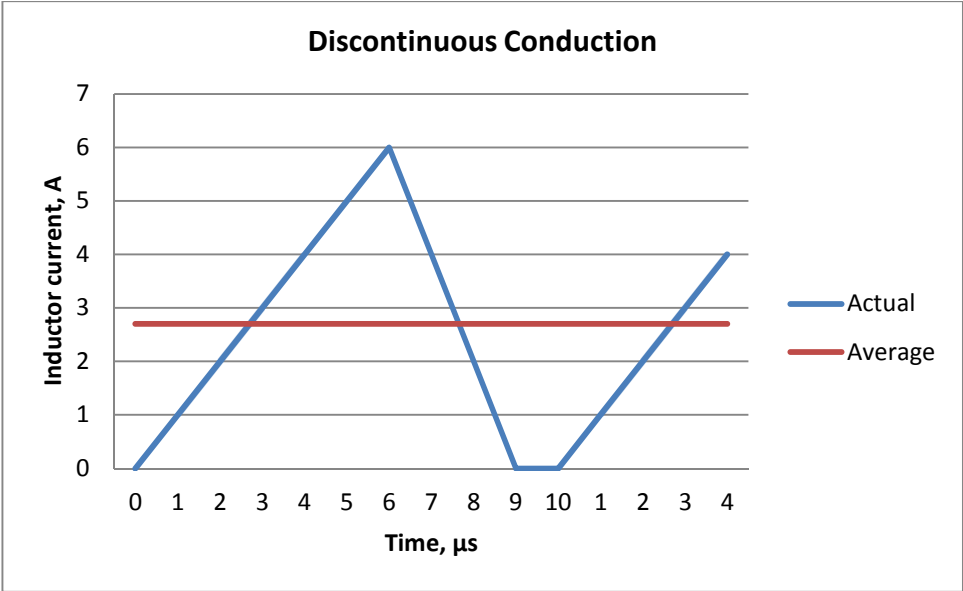


Figure 7: Discontinuous conduction

In both cases, inductor current is DC biased around its positive average.

Some terminology and definitions are required:

- T: One full cycle (10 μ s in the above charts), called commutation period length
- D: The duty cycle is the fraction (0 to 1) of T that the switch is ON (0.6 in the preceding charts)
- V_i : Input voltage (V_IN in the topology figures)
- V_o : Output voltage (V_OUT)
- L: Inductor inductance
- I_o : Average output current

The following formulas can be derived:

	Continuous	Discontinuous
Buck	$V_o = V_i D$	$V_o = \frac{V_i}{\frac{2 L I_o}{D^2 V_i T} + 1}$
Boost	$V_o = \frac{V_i}{1 - D}$	$V_o = V_i \left(1 + \frac{V_i D^2 T}{2 L I_o} \right)$

Table 7: Buck and boost transfer functions (10) (11)

Although discontinuous operation is unavoidable (and perfectly normal) at low loads, it is much more complex than continuous conduction. Circuit regulation is more difficult as it not only depends on duty cycle and input voltage but also on inductance, load current, and commutation period. Additionally, this affects inductor loss calculation, with the effect that available tools often limit their validity to continuous conduction.

4.1.2 Synchronous Rectification

The basic buck and boost topologies suffer from diode forward loss during the OFF (or $1 - D$) part of the commutation cycle. Synchronous rectification avoids this by replacing the diode by a second switch. Thus higher efficiency is gained at the cost of a more complex switch controller scheme. All switch controllers considered for MODPSU are based on synchronous rectification.

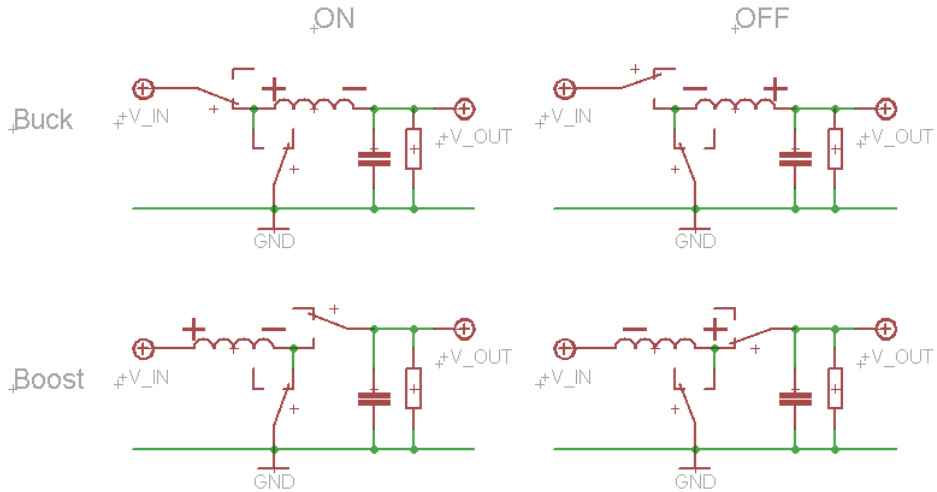


Figure 8: Synchronous rectification

In reality, the synchronous rectification scheme is a bit more complicated. It is necessary to avoid the case of both switches being on at the same time, or else a short-circuit condition called “shoot-through” will occur. For this reason, there must be a (dead) time gap between turning off one switch and turning on the other. Practically all modern switch circuits use enhancement mode power MOSFET transistors, in which the “switch” is paralleled with an integrated reverse-coupled diode called “body diode” that is added in order to guarantee controlled transistor behavior. It can typically handle large currents but has a relatively high forward voltage drop. (12) Therefore, some high-power circuits use an external schottky diode with a lower drop, but there is some debate how much is actually gained by this. ¹⁰

Please note that the synchronous switches must be paralleled by some type of diode. Otherwise, dead-time inductor current would cause voltage spikes that would break the switch transistors. In the following, every switch symbolizes a switch and its body diode.

¹⁰ Please see 4.2.3 for more information.

4.1.3 Synchronous Four-Switch Buck/Boost

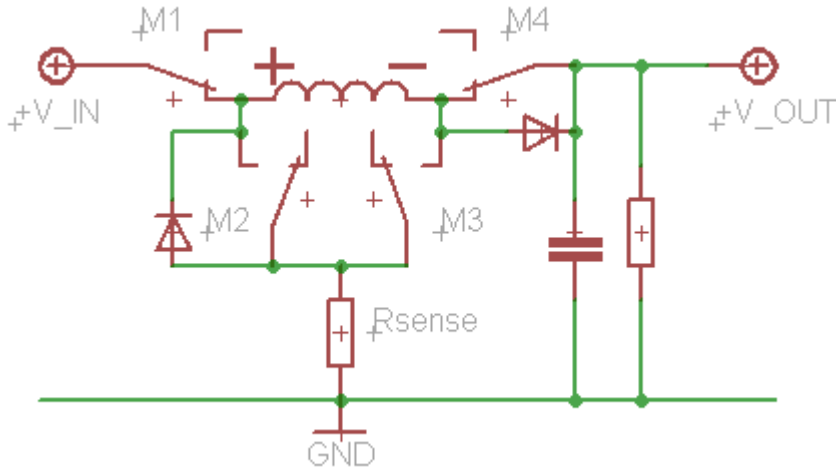


Figure 9: Four-switch buck/boost circuit (showing ON in buck mode)

The synchronous four-switch buck/boost circuit combines the switches from the buck and the boost topologies. External free-wheeling diodes have been included for (potentially) lower losses during the short period when both switches (M1 & M2 and M3 & M4 respectively) are OFF.

As previously mentioned, this topology transitions from pure buck to pure boost modes (or vice versa) via two hybrid modes:

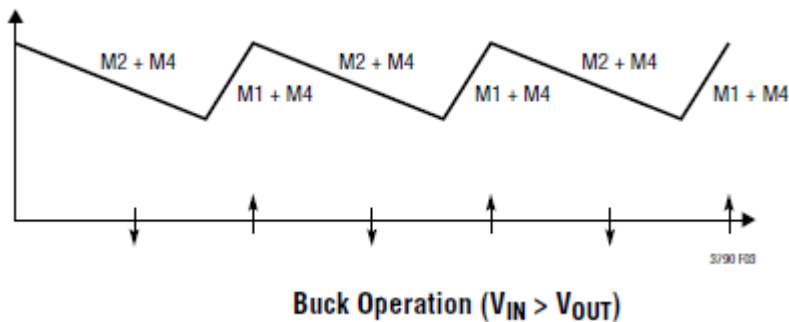


Figure 10: Pure buck operation (13) ¹¹ (copyright Linear Technology, reprinted with permission)

¹¹ Figure 10 - Figure 13: <http://www.linear.com/product/LT3790>

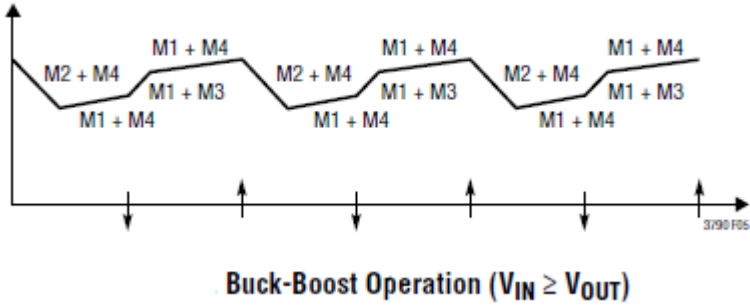


Figure 11: Buck and boost operation (13) (copyright Linear Technology, reprinted with permission)

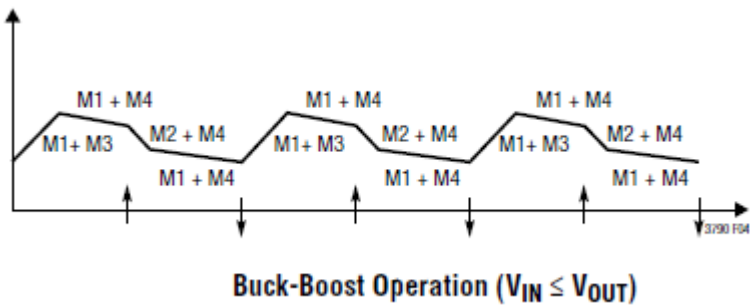


Figure 12: Boost and buck operation (13) (copyright Linear Technology, reprinted with permission)

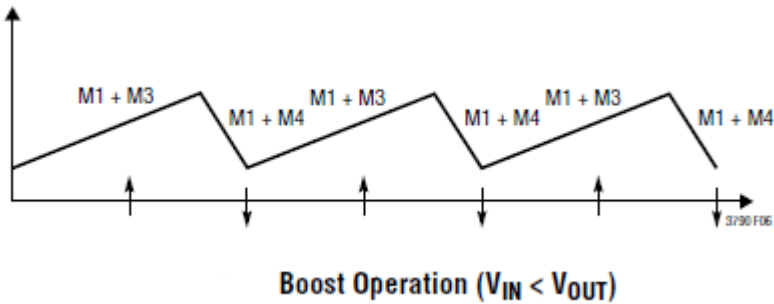


Figure 13: Pure boost operation (13) (copyright Linear Technology, reprinted with permission)

4.1.4 Switching Modes

The switch controllers used for MODPSU support two or three switching modes that should not be confused with the inductor conduction modes:
(14)

- Continuous mode: Every clock cycle triggers a switch commutation cycle. This results in the lowest ripple, audio noise, and RF interference. Reverse inductor current is permitted, i.e. some switches can dump current from the output when more energy is fed than what is wanted. This way output voltage spikes caused by quickly decreasing load current are reduced. The downside is relatively higher low-load switching losses in FETs. When operating at less than minimum duty cycle, it resorts to pulse-skipping.
- Pulse-skipping mode: This is a (non-idle) mode in which some clock cycles don't cause a switch commutation cycle. Reverse inductor current is not permitted, which means a greater risk for output voltage spikes. Switching losses and the need for low-load dumping are reduced compared to continuous mode. Thus, low-load efficiency is better than in continuous mode, but ripple voltage and current are higher.
- Burst mode: This is a sleep mode in which the output is monitored and a burst of commutation cycles is generated when the output drops below a threshold value. Reverse inductor current is not permitted. Ripple, audio noise, and RF interference are higher but switching losses and the need for low-load dumping are further reduced. Low-load efficiency is even higher in burst mode.

At regular and high load currents continuous mode is clearly the best in all aspects, while the two others are sometimes chosen for low-load operation. The LTC3790 used for the buck/boost circuits can be set to automatically switch to pulse-skipping mode at low load. (It doesn't support burst mode.) The LTC3850 or LTC3869-2 support all three modes but cannot automatically switch between them. The MODPSU PSU is designed so that the ATX ON/OFF signaling also controls transition between continuous and burst mode.

4.1.5 Parallelization / Multi-Phase Design

Multi-phase operation is a form of parallelization, in which two or more individual switch circuits are fed from the same power source and / or supply the same load. As the name suggests, these switch circuits are synchronized at a certain phase offset, e.g. 180 degrees for two or 120 degrees for three circuits.

For the case of supplying the same load, the advantages are:

- Faster response to load changes. With n circuits, response "speed" is n times the one-circuit case.
- Heat spreading over a larger PCB area (greater power handling capability and easier to cool).
- Lower ripple as the effective frequency increases. When $n * D$ is an integer, the ripple components cancel out.
- A multi-phase design has total losses that could (very) roughly be described as $(n * ((I/n)^2 * R + \text{idle losses}))$, while a single-phase has $(I^2 * R + \text{idle losses})$. At some point, single-phase design losses exceed multi-phase losses.

The drawbacks are:

- Larger PCB area.
- More components, i.e. more expensive.
- Higher effective frequency might require special capacitors.
- Low-load losses increase with the number of switch circuits (n).

Then there is an additional factor that is not clearly a pro or a con:

Dividing the load over several circuits means that smaller inductors can be used. A smaller inductor size requires a thinner wire. This equates to a higher DCR. Inductor properties also depend on factors such as magnetic path length and core cross-section area. In other words it is a trade-off that requires further investigation. It is tested empirically in the efficiency measurements.

The MODPSU PSU design benefits from another type of multi-phase; the two switch circuits supply independent loads clocked 180 degrees out of synch, thereby reducing input ripple.

4.2 SMPS Losses in MOSFET Transistors

This work does not intend to explain how MOSFET transistors work, as they are only used as building blocks recommended by an optimizing design tool and no “manual” calculation is done. If you are interested in more detail, see e.g. Wikipedia (12) (15) and manufacturers. (16)

Below is a short explanation of transistor-related losses in SMPS where n-channel enhancement type (active ON) MOSFETs are typically used. Only turn-on in synchronous buck conversion is covered as turn-off is analogue to turn-on. The main difference is that the driver strengths (low-high vs. high-low) might differ, which then results in different transition times (and hence losses). Constant gate driver current is assumed for simplicity. This section is largely based on Fairchild Semiconductor’s application note AN-6005 (17) unless otherwise specified.

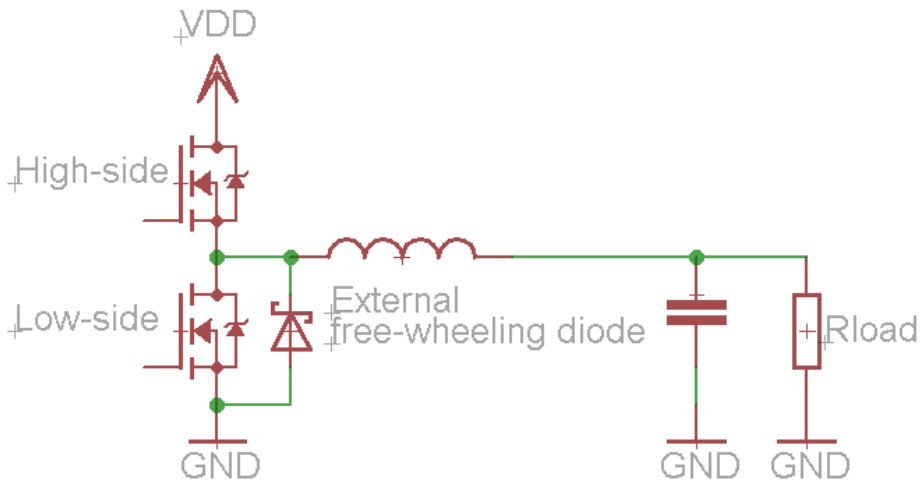


Figure 14: Simple illustrative synchronous buck converter

The losses can be divided into three categories:

1. High-side (top or forward) FET
2. Low-side (bottom or synchronous) FET
3. Dead-time (internal body diode or external free-wheeling diode)

4.2.1 High-Side FET

Switching losses typically far exceed conduction losses in the high-side FET, especially for low duty cycles.

4.2.1.1 Conduction losses

Conduction losses are similar to a resistor's dissipation for a fraction of the time (duty cycle):

$$P_{\text{cond}} = I_{\text{out}}^2 * R_{\text{ds(on)}} * \frac{V_{\text{out}}}{V_{\text{in}}} = I_{\text{out}}^2 * R_{\text{ds(on)}} * D$$

4.2.1.2 Switching losses

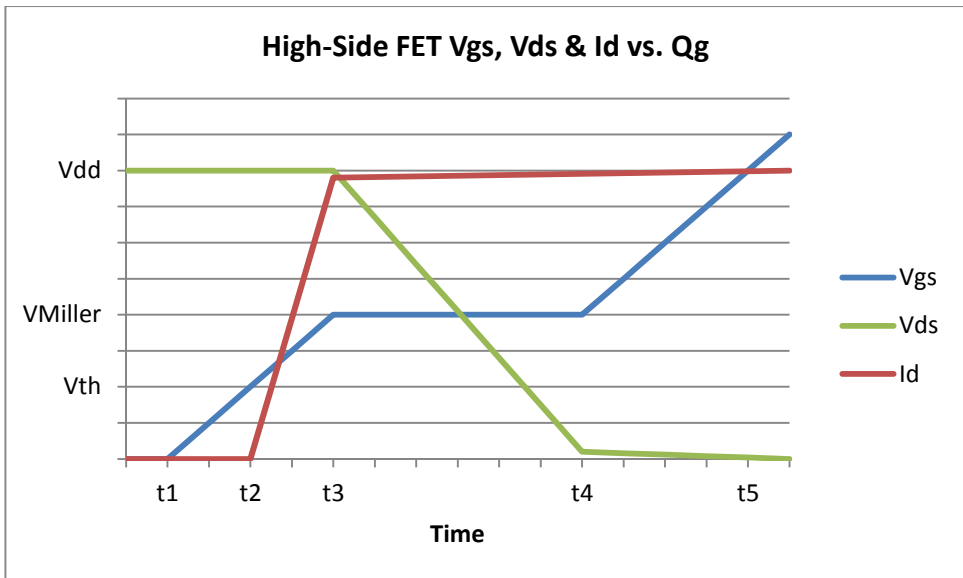


Figure 15: High-side V_{gs} , V_{ds} & I_d vs. total gate charge Q_g when driven by a constant current. (17) In reality, V_{Miller} is not constant.

The switching losses are more complex. The drain current and drain-to-source voltage depend on the gate-to-source voltage as depicted in figure 11. A number of distinct phases can be seen:

- t_1 to t_2 : V_{gs} has not yet reached its threshold, so no current flows through the drain terminal.
- t_2 to t_3 : V_{gs} continues to rise until it reaches V_{Miller} . V_{ds} remains unchanged but I_d ramps up from zero to near its maximum.
- t_3 to t_4 : V_{gs} stays at V_{Miller} until C_{gd} is fully charged. During this period, I_d continues towards saturation and V_{ds} falls to near zero.

- t_4 to t_5 : The transistor is gradually saturating.
- t_5 and above: The gate is driven to the driver voltage that might be higher than V_{DD} .

Most of the ‘main flow’ switching losses occur between t_2 and t_4 :

$$P_{sw} = \frac{V_{in} * I_{out}}{2} * (t_4 - t_2) * F_{sw}$$

There are however additional switching losses that are caused by the intrinsic capacitances and gate resistance. They can be expressed in a number of ways depending on which property you want to describe, but that is out of scope for this work. Much more detail can e.g. be found in these documents: (18) (16)

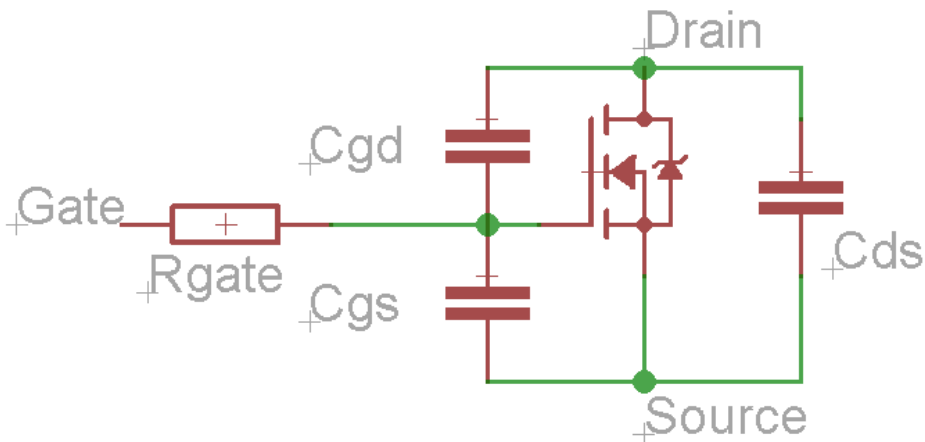


Figure 16: N-channel enhancement-mode MOSFET intrinsic capacitances and gate resistance, also called “the switching model” (18)

These losses are much smaller than those from the main flow at target load. They are mostly worth considering for two reasons: the place where they occur (e.g. the gate driver in the switch controller) and low load operation. The following are the most important, in descending order:

1. Charging the gate:

$$P_g = Q_g * V_{driver} * F_{sw}$$

In figure 11, Q_{gs} is charged between $t1$ and $t3$. Q_{gd} is charged between $t3$ and $t4$. Q_g is the total charge from $t1$ past $t5$ (up to the gate driver maximum). (16) (19) All of these are typically stated in the datasheet and relate to the intrinsic capacitances.

2. Charging the MOSFET's output capacitance:

$$P_{oss} \approx \frac{C_{oss} * V_{in}^2 * F_{sw}}{2}$$

$C_{oss} \approx C_{ds} + C_{gd}$ with C_{gs} 'shorted by a high-frequency capacitor'.

3. In case no external free-wheeling diode is used:

$$P_{Qrr} = Q_{rr} * V_{in} * F_{sw}$$

Q_{rr} is the body diode's reverse recovery charge, which is found in the datasheet.

4. If an external free-wheeling diode is used, this loss replaces the one in 3:

$$P_{C(Schottky)} = \frac{C_{Schottky} * V_{in}^2 * F_{sw}}{2}$$

4.2.2 Low-Side FET

The low-side FET only shorts the free-wheeling diode (roughly 0.6 V), so switching losses are very low and conduction losses dominate.

4.2.2.1 Conduction Losses

Conduction losses are expressed in the same way as for the high-side FET, but at the $1 - D$ fraction of the time:

$$P_{cond} = (1 - D) * I_{out}^2 * R_{ds(on)} = \left(1 - \frac{V_{out}}{V_{in}}\right) * I_{out}^2 * R_{ds(on)}$$

4.2.2.2 Switching Losses

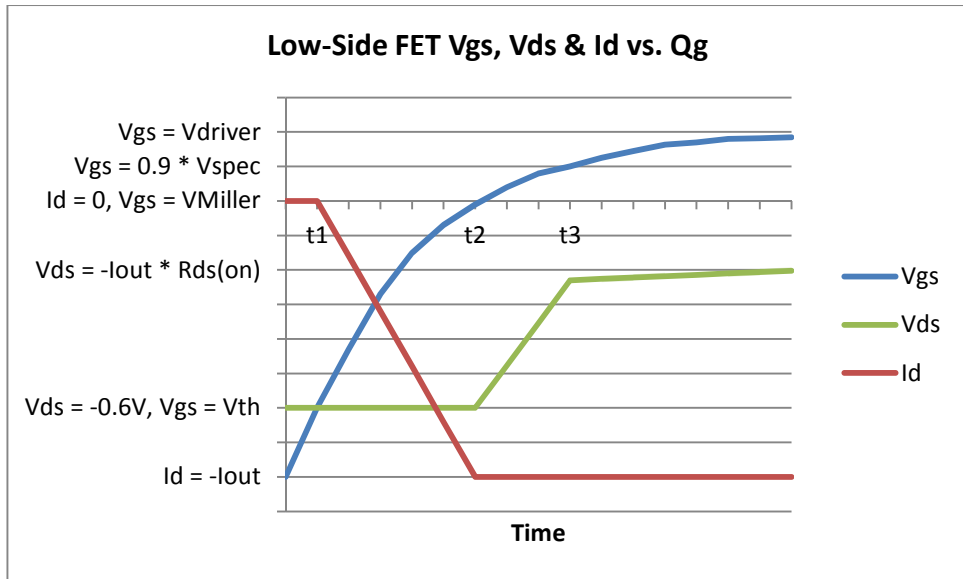


Figure 17: Low-side V_{gs} , V_{ds} & I_d vs. total gate charge Q_g when driven by a constant current (17)

The low-side FET is typically operating with reverse current and the Miller voltage plateau is not clearly visible, as V_{ds} becomes less negative when the device is being turned on. The V_{ds} drop is caused by a change in $R_{ds(on)}$ from $\frac{V_f}{I_{out}}$ when $V_{gs} = V_{Miller}$ to about 110% of the highest specified $R_{ds(on)}$. At this point, V_{ds} is 90% of V_{spec} , which is the V_{gs} for the highest specified $R_{ds(on)}$.

$$P_{sw} = \left((t_2 - t_1) * V_f + (t_3 - t_2) * \left(\frac{V_f + I_{out} * 1.1 * R_{ds(on)}}{2} \right) \right) * I_{out} * F_{sw}$$

4.2.3 Dead-Time (Body or Freewheeling Diode Time)

If both FETs are on at the same time, a fatal condition called shoot-through occurs. To avoid it, the controller ensures a certain short dead-time when both FETs are off. During this period, current flows from ground through the diode and the inductor to the output.

$$P_{diode} = t_{deadtime} * F_{sw} * V_f * I_{out}$$

Most switch controllers sense conduction through the FETs and adapts to the actual dead-time in order to minimize losses in the freewheeling diode.

The type of FET transistors used in SMPS has a built-in diode called “body diode”. According to the LT3790 datasheet (13), it is possible to improve peak efficiency by 1 to 2% at 500 kHz by using an external schottky diode with lower forward voltage drop. The LTC3850 datasheet (14) claims that as much as 3% of efficiency can be gained at high input voltage by using an external diode. Others play down its usefulness as dead-time losses are very small in comparison to other losses below 1 MHz (17) or because of stray inductances resulting in slow external diode activation making it only usable at lower frequencies. (19) These contradictions make it difficult to foresee the improvement from attaching an external free-wheeling diode, but perhaps technological advancements have rendered the topic moot. Modern enhancement MOSFET transistors have a “monolithic integrated schottky like diode” with low forward voltage drop and capacitance. (20) (21)

The usefulness of an external freewheeling diode for the 12V main buck/boost rail is tested empirically in the efficiency measurements.

4.2.4 FET Loss Summary

The main transistor-related losses come from the ‘main flow’:

- Switching losses especially in the high-side FET depending on V_{in} , I_{out} , switching transition time (FET capacitances and gate driver strength) and F_{sw} .
- Conduction losses especially in the low-side FET depending on I_{out}^2 , $R_{ds(on)}$, and duty cycle.

Fairchild Semiconductor application note AN-6005 (17) presents a circuit that supplies 1.5 V @ 15 A from a 12 V rail with a switching frequency of 300 kHz. 16% of the high-side losses and 79% of the low-side losses are conduction losses. The low-side should thus favor low $R_{ds(on)}$ over low charge property values, while the high-side should take an opposite view.

4.3 Inductor Properties and Losses

This section is based on chapters 1 and 2 of Col. McLyman's "Transformer and Inductor Design Handbook, 4th Ed." (22) unless otherwise specified.

Another extensive source of information is the web site www.vias.org where Leander W. Matsch publishes an online textbook named "Capacitors, Magnetic Circuits and Transformers". (23)

4.3.1 Introduction to the Force Fields

When a current flows through a wire, a magnetizing force field (H) and a magnetic flux field (B) are generated in circles around it. Initially we focus on DC and slowly changing signals. This paper uses the centimeter-gram-second (cgs) unit system.

Magnetic flux density is measured in gauss or tesla (1 tesla = 10⁴ gauss);

$$B_m = \frac{\Phi}{A_c}$$

where Φ is the magnetic flux (measured in weber) and A_c is the (core) cross-section area in cm².

The magnetizing force field is measured in oersteds;

$$H = \frac{I}{2 \pi * r}$$

where r is the distance from the wire to the point at which the force is measured.

The relationship between them is called permeability; the ability to conduct magnetic flux (or how easily the core is magnetized to a certain level of flux):

$$\mu = \frac{B}{H}$$

The air-core inductor has unity permeability in the cgs system. Some materials (iron, nickel, cobalt, and alloys of them) have a much higher permeability. By forming them into a core around which the wire is wound, the magnetic flux is greatly increased.

4.3.2 Magnetomotive Force and Reluctance

The magnetizing force field H depends on the magnetomotive force (MMF);

$$H = \frac{MMF}{MPL}$$

where MPL is the average magnetic path length in cm.

Magnetomotive force (or magnetic potential) is measured in gilberts or ampere turns;

$$MMF = 0.4\pi * N * I \text{ [gilberts]} = N * I \text{ [ampere turns]}$$

where N is the number of turns, but also (24)

$$MMF = \Phi * R_m$$

where R_m is the material's resistance to magnetic flux, called reluctance. It is analogous to electrical resistance, but where resistance dissipates energy, reluctance stores it:

$$\text{Electromotive force EMF } E = I * R \text{ [i. e. current * resistance]}$$

$$\text{Magnetomotive force MMF } F_m = \Phi * R_m \text{ [i. e. flux * reluctance]}$$

The reluctance of a magnetic core is a function of magnetic path length, cross-section area, and the permeability of the core material and air:

$$R_m = \frac{MPL}{\mu_r \mu_0 A_c}$$

Most of the flux is contained in the core, which means that the MPL is (fairly) well defined. The (change in the) magnetic field builds up (and saturates) from the shortest path outwards to the longest one and is then neutralized in the same fashion. At low magnetization the outer portion of the core is unused, but eventually the entire core will become saturated and more or less steeply permeability drops to that of air. This highly non-linear behavior is problematic in tuned circuits and often fatal in switch-mode power supplies. The electronics designer must avoid saturation at all costs.

4.3.3 Inductance and Energy Storage

When you apply a voltage (or EMF) to an inductor, the result will be a change to the current through it at a rate determined by the inductor's inductance (assuming zero DC resistance):

$$v(t) = L * \frac{di}{dt} \Leftrightarrow L = \frac{v(t)}{\frac{di}{dt}} \Leftrightarrow \frac{di}{dt} = \frac{v(t)}{L}$$

When the same flux links all turns, a property named flux linkage (measured in weber turns) is defined as (25):

$$\lambda = N * \Phi$$

With constant inductance and flux linkage coming only from the own circuit we have the following relationship (26) (27):

$$L = \frac{\lambda}{i} = \frac{N^2}{R_m} = \frac{N^2 * \mu_r * \mu_0 * A_c}{MPL}$$

With the above provisions and assuming constant relative permeability, the energy stored in the magnetic flux field is (26):

$$W_\phi = \frac{L * i^2}{2} = \mu * \frac{(N * i)^2 * A_c}{2 * MPL}$$

Inductors can be used to store energy thanks to a property commonly referred to as Lenz' law. It's original 1834 wording (28) is in German and in reference to (especially) Faraday's and Ampere's work, so it has numerous modern English interpretations and translations. It is perhaps best explained by self-induction:

A current flowing through an inductor sets up a magnetic field. A change in this current causes a corresponding change in the field which generates an induced EMF. The effect of this induced EMF has a direction that makes it oppose the change and act to maintain the original field density. This is known as self-induction. (9)

Lenz' saw that the induced current is of opposite direction, which counteracts the change that induced it (although in this early day his "Satz" speaks of moving wires rather than changing currents).

4.3.4 B-H Hysteresis and Fundamental Core Properties

The process of core magnetization and demagnetization is illustrated by the B-H hysteresis curve. Assuming that the core is initially completely demagnetized, the path starts at the origin and (if fully magnetized) eventually reaches the saturation asymptote B_s at which a further increase in magnetizing force results in practically no more flux.

When H is decreased from saturation to zero, the core has a residual (remanent) magnetization, B_r . H_c is the reversed coercive magnetizing force required to reduce B_r to zero. Similarly, coercivity is the reversed magnetizing force H_{cs} that resets the remaining flux at retentivity saturation B_{rs} to zero.

What actually happens is a (re-) orientation of (imaginative) tiny magnets called dipoles within the core, hindered by something that can be thought of as friction. This process can only go on for as long as there are dipoles left to turn.¹²

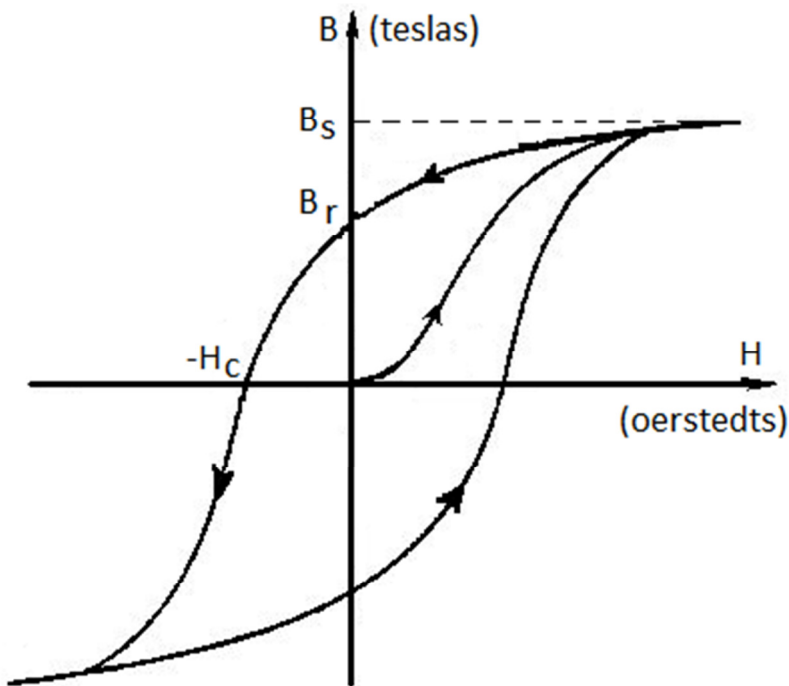


Figure 18: B-H hysteresis curve (29) (Copyright Wikipedia, adapted and reprinted in accordance with the Creative Commons Attribution 3.0 Unported license)

¹² This is based on the so-called domain theory of the nature of magnetism.

The B-H curve has great explanatory value for inductor core properties. The area enclosed by this path (or the corresponding one for a non-saturated core) is the actual energy lost in one switching (commutation) cycle. Hence, core loss is directly related to switching frequency (but also to the magnetizing force applied, which depends on the amplitude of the inductor current swing (ripple)). For at least the applications relevant to the MODPSU project, the diminishing ripple resulting from higher frequency causes a smaller decrease in core loss than the increase brought on by the higher commutation count.¹³

Permeability μ is not constant but a function of B and H. μ peaks at about the middle of the path from the origin to B_s and drops to zero at the beginning and end of this transition. Note the difficulty with which the transition starts and the gradual decline at the end.

The shape of the B-H hysteresis curve also reveals the “suddenness” of the core’s saturation. A sharper “knee” equates to higher and more even performance but also more dangerous operating conditions.

Core material permeability is sensitive to frequency, exciting voltage, temperature, and pressure. For this reason, an air gap is often incorporated into the core as a means to stabilize it, either as a minuscule straight-through cut or distributed in the core in the form of insulating coating or oxidation of the sintered powder from which it is made. The permeability of air is some 800 to 80 000 times lower than that of the core material, which means that the gap’s permeability will dominate and stabilize the combined core permeability. This is seen as a clockwise tilt or shearing of the B-H curve.

The air gap has another positive effect; the inrush current at turn-on can in some situations leave an un-gapped core biased for when the actual operation starts, which causes a series of saturation current spikes that can damage other components. The air gap shearing greatly reduces this problem (by lowering B_r and providing softer saturation).

A negative effect of the air gap is that fringing flux bridges the gap in a loop that is perpendicular to the flux at each end of the gap. This causes so called eddy currents (30) in the core that are pure heat loss. The insulating coating or oxidation of powder cores reduces this problem, as does the laminated design of a traditional EI-transformer core. Fringing flux can also be reduced by placing the winding as close as possible to the core, in an

¹³ Please see the inductor simulations and heat measurement experiments in this report.

even and covering fashion. A higher frequency means more fringing flux. A greater electrical core resistance means less fringing flux.

The energy distribution is proportional to the reluctance. For a gapped inductor this means that most of the energy is stored in the gap – not the core material. (31)

Please note that DC bias brings the average operating point closer to saturation.

4.3.5 Wire Losses

Eddy currents not only cause losses in the core. They also occur in the wires carrying alternating current (AC), increasing with frequency:

- Skin effect (32): The alternating current generates a changing magnetic field that induces opposing eddy currents in the wire. This pushes the flow of current to the surface of the wire, which effectively increases the AC resistance as the used copper cross-section area is reduced.
- Proximity effect (33): Parallel wires carrying the same alternating current will generate a magnetic field that induces longitudinal eddy currents in the other wires. The loop is directed so that it adds to the current on the far side and opposes the current on the adjacent side. This forces the current to flow on the surface of the far side of the wire, which increases the effective AC resistance.

These two AC wire losses can be reduced to some degree by using flat wire which has a greater surface area than a round wire with the same cross-section area.

Finally, there is wire loss due to DC resistance. It is the only type that is easy to measure and predict.

4.3.6 Core Materials

This section is based on chapter 2 of Col. McLyman’s “Transformer and Inductor Design Handbook, 4th Ed.” (22), a master’s thesis evaluating powdered inductor core materials at Chalmers University of Technology by Kindmark & Rosén (34), and a manufacturer paper on inductor material and shape choices by Swihart at Magnetics Inc. (35).

Core losses are among the most important in SMPS applications, so one might think that core materials should have a very prominent role in this paper. However, I am using off-the-shelf inductors, many of which have

non-disclosed specifications. Even the material itself is often a secret, so there is not much point in diving far into this very complex area.

Even with knowledge about core material and specifications, there is much uncertainty. In fact, col. McLyman presents some results from a program at the Caltech / NASA Jet Propulsion Laboratory to measure dynamic B-H loop characteristics. My humble inductor evaluation is in good company.

For high-performance DC/DC-switched power supplies, the most important core materials are ferrites and a few other powdered materials. They come in a variety of permeability grades. There are also a few amorphous materials that are made by rapid cooling of liquid metallic glass.

4.3.6.1 Ferrites

There are two families of powdered, ceramic, ferrites:

- Manganese-Zinc (Mn-Zn) has higher permeability. It is the most common and used below 2MHz.
- Nickel-Zinc (Ni-Zn) has higher resistivity (electrical resistance). It is used from about 1 MHz to hundreds of MHz.

Both are without aging effects but suffer from a comparatively high temperature dependency and sensitivity to thermal shock. Saturation is about 25 to 40 % lower at 100 °C compared to 25 °C. Its sharp saturation can be fatal, especially in combination with its strong temperature dependency. The practical consequence is that ferrite inductors must be chosen so that they are operating sufficiently below their peak current, which boils down to a physically bigger size. The inductance value is not current-dependent (until saturation).

Core resistivity is high due to the ceramic material, which gives ferrite low AC losses at high frequency. Ferrites typically have one discreet gap, which makes fringing flux and EMI greater than most of the powdered types. (34)

Ferrite powder cores experience an upward shift in frequency-related loss above some 400 kHz. (36)

4.3.6.2 Other Powder Materials

All have distributed air gaps.

- Molybdenum Permalloy Powder (MPP) (Ni 82%, Fe 16%, Mo 2%) is the best of all powder core materials, with an extremely narrow B-H loop and greater permeability/temperature, saturation/temperature, and aging stability. Its high nickel content and high-pressure process makes it comparably expensive. It is most common in toroid shape, but e.g. CWS makes MPP and HF in other shapes. (37)
- High flux (HF) (Ni 50%, Fe 50%) is almost as expensive as MPP, but more lossy than MPP and Kool M μ . It's mostly used in applications with high DC bias or AC peak currents, where its high B_{sat} and inductance stability are valued. It too is most common in toroid shape.
- Sendust (Kool M μ) (Fe 85%, Si 9%, Al 6%) is much cheaper than MPP and HF and has DC bias performance similar to MPP. It has higher AC losses than MPP, but comes in both toroid and E shapes. The latter means lower winding costs and possibly also lower winding losses.
- XFlux (Fe 93.5%, Si 6.5%) has even better DC bias characteristics but higher AC losses than HF. It is much cheaper than MPP and HF and comes in toroid, E, U, and block shapes.
- AmoFlux (Fe, B, Si) is made from pulverized amorphous tape that is pressed into a toroid (only). It has AC losses similar to Kool M μ but better DC bias performance, which means that smaller cores and / or fewer winding turns can be used for the same current handling capability.
- Iron powder (Fe 100%) has higher core loss than some more expensive materials and low permeability, which means that it requires a larger number of turns, i.e. bigger size and lower efficiency. It is not recommended for discontinuous conduction or large ripple operation. It is a cheap high-volume product.

4.3.6.3 Amorphous Materials

The metallic glass core materials are included here for completeness. They have very high performance in terms of permeability, inductance, and core losses, but they are still niche products.

- 2605SC (Fe 81%, B 13.5%, Si 3.5%)
- 2714A (Co 66%, Si 15%, Fe 4%)
- Nanocrystal Vitroperm 500F (Fe 73.5%, Cu 1%, Si 15.5%)

4.3.6.4 Some Highlights from Kindmark & Rosén (34)

- Iron powder performance is significantly worse than MPP, Sendust, and HF.
- Sendust performed better than MPP in all buck tests with high ripple.
- Efficiency is consistently dropping from 200 kHz to 1.9 MHz (which is their measurement frequency range).

4.3.7 Inductor Presentation with Core Design Overview

There is a multitude of core shapes, each with its own specific properties. I have only browsed this topic as there are only three types available off the shelf; PQ-ish cores, square pot cores, and molded. The otherwise common toroid shape is not available as an off-the-shelf product for the physical sizes and current ratings required by the MODPSU products.

See e.g. (38) and chapter 3 of Col. McLyman's book (22) for more information. (34) compares losses in three use cases with MPP, HF, and Kool M μ in toroid shape and Kool M μ in E core. Custom inductor design brings great additional complexity.

4.3.7.1 PQ and E-type Core



Figure 19: Würth Elektronik HCF2013 with PQ core (39) and Coilcraft SER201X with a hybrid PQ/EE core

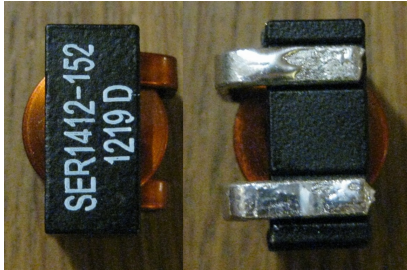


Figure 20: Coilcraft SER1412 (15.24 * 12.00 * 12.66 mm) with EI core

The PQ shape has optimized volume/winding area and volume/surface area, i.e. maximum power output with minimum weight and volume. The more uniform cross-section area results in fewer hot spots. (39) In other words, the PQ core has comparatively low core losses. As the winding is partly exposed, cooling is better than for closed types. It is called “magnetically shielded” by the manufacturer, but magnetic stray radiation is likely to be larger compared to closed ones due to the exposed winding. How much larger, neither WE nor Coilcraft is able to say.

All of these are MnZn ferrites.

4.3.7.2 Square Pot Core

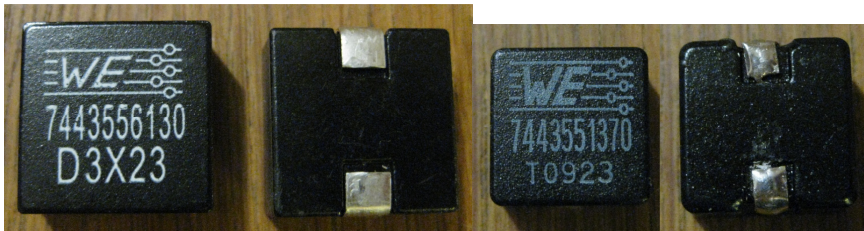


Figure 21: Würth Elektronik HCI1890 (18.2 * 18.3 * 8.9 mm) and HCI1365 (12.8 * 13.0 * 6.2 mm) with square pot core

The pot core consists of a lidless box with a center tap and a lid. The winding is attached to the bottom by glue. It is magnetically shielded as the core surrounds the winding but for the solder pins. Heat is transferred by glue or air to the core. It is unclear whether the glue has good heat transfer properties.

HCI1890 exists in two versions; one with core material WE-PERM2 for lower inductances and one with MnZn ferrite for slightly higher. This project only deals with the WE-PERM2 type, an unspecified core material. A marketing training presentation (40) refers to it as “iron powder”.

The HCI1365 is an unspecified material called WE-PERM.

4.3.7.3 Molded Core

By molding the core directly onto the winding, magnetic shielding and heat transfer are good and mechanical vibration (buzz noise) of the winding is minimal, as is the magnetic path length.



Figure 22: Coilcraft XAL1580(15.2 * 16.2 * 8 mm) and XAL1010 (10.0 * 11.3 * 10.0 mm)

Note the placement of the XAL connectors. It saves PCB real estate but it makes the component very difficult to solder manually, even with a hot air soldering station. I cut copper foil into T shapes and soldered them to the inductor so that the protruding wings could then be soldered to the PCB:

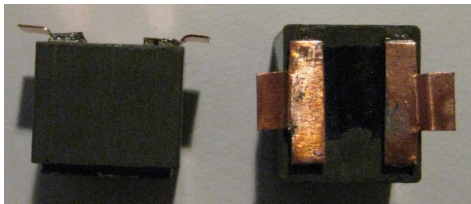


Figure 23: Coilcraft XAL1010 with custom “wings”

The two big inductors from Vishay Dale are of identical size and appearance. In fact, they have no other marking than what can be seen in the below picture... Their properties are listed in a public application note (41) with instructions (42).

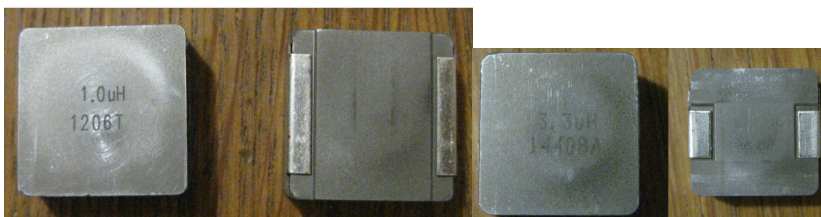


Figure 24: Vishay Dale IHLP6767GZ-01 and -11 (17.15 * 17.15 * 7 mm) and IHLP5050FD-01 (12.9 * 13.2 * 6.5 mm)

4.3.7.4 Composite Core

Col. McLyman uses the term “composite core” (p2-50) for two cases of core type combinations:

- Un-gapped inner and gapped outer loops
- Different materials for the inner (in his cases un-gapped) loop than for the (gapped) outer loop.

The idea is to minimize core losses at up to design current but also get soft saturation as a safety measure.

The above “molded” inductor models are marketed as “composite” by the manufacturers, but neither provides any information as to what that refers to. I assume that it actually means that the winding and core are composite, rather than that the core itself is composite.

4.3.8 Inductance vs. current

The various core materials have different inductance vs. current characteristics. The following two graphs show specified properties.

Most obvious are the ferrites, with nigh-on constant inductance value until saturation, after which it drops rapidly. The HCI1890, XAL1580, and IHLP6767GZ-01 have very similar shape, while the IHLP6767GZ-01 (dotted) stands out.

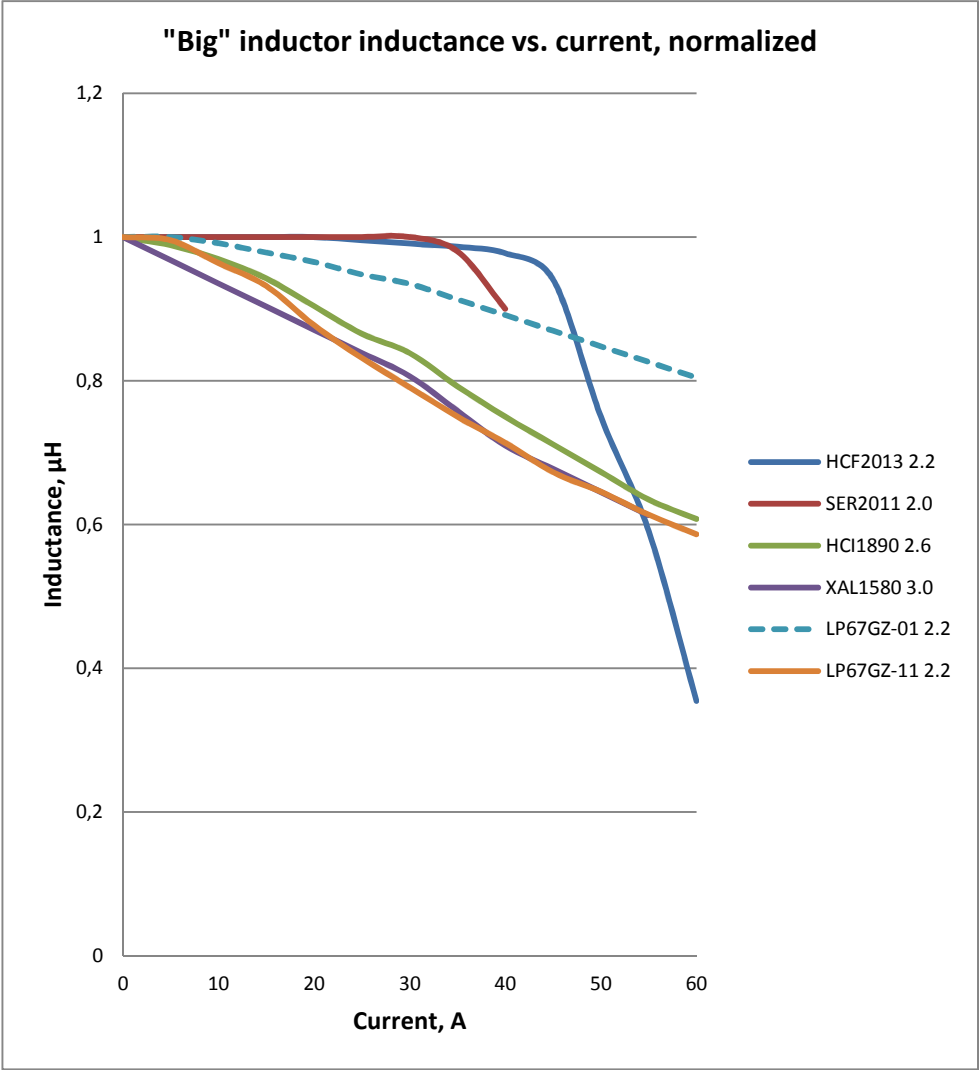


Figure 25: "Big" inductor inductance vs. current

The "small inductors" show similar behavior:

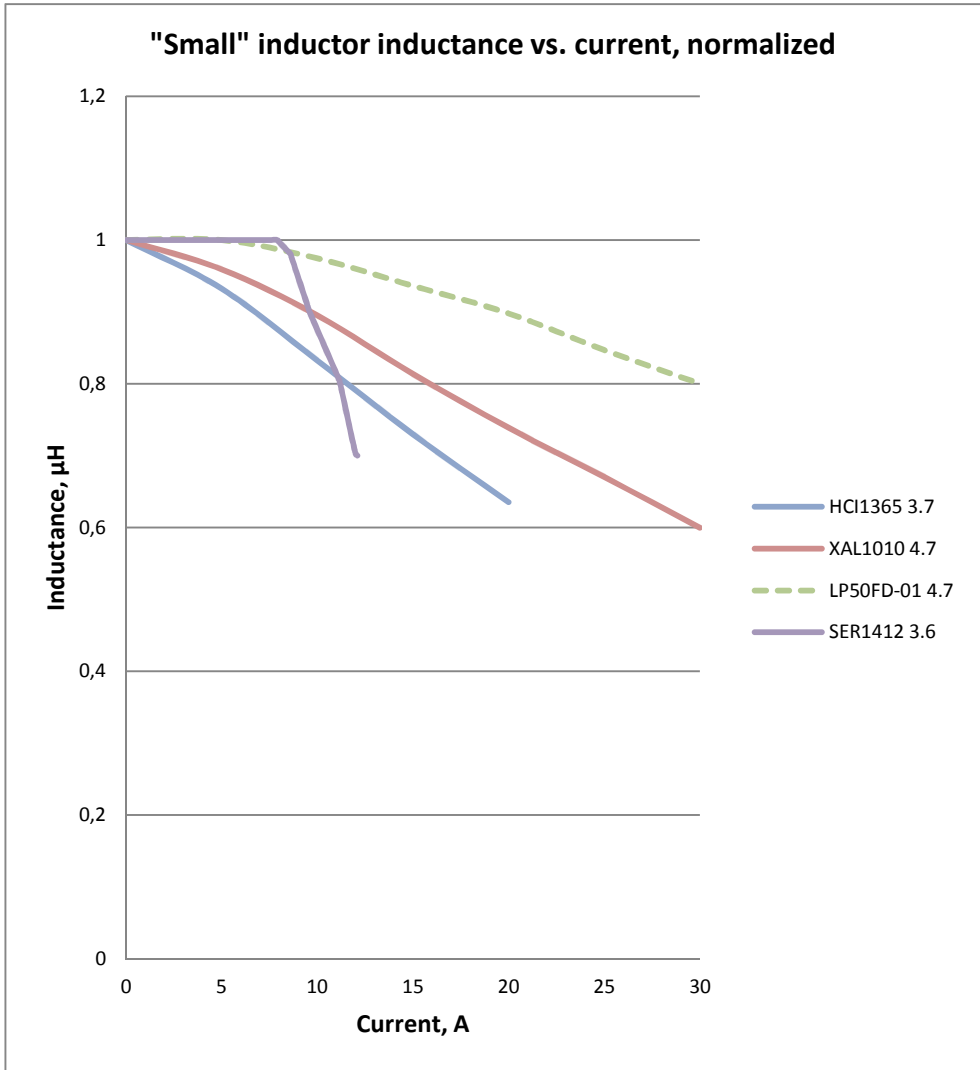


Figure 26: “Small” inductor inductance vs. current

4.4 Capacitor Properties

In this project, capacitors are used for the following purposes:

- Bulk energy storage for switch-mode input and output
- Low-ESR “switch-mode transient buffering”, typically ceramic multi-layer chip capacitors (MLCC)
- Decoupling
- RC filtering and timing

There has been great development in these areas too. Solid electrolyte polymer capacitors with low ESR are replacing liquid electrolyte aluminum capacitors for bulk energy storage. They are not as prone to leaking, they age better, and they perform better at higher temperatures. (43) Some of the leading types are Panasonic OS-CON, POSCAP, and KEMET KO-CAP. For legacy reasons, this project is using OS-CON SVPF and SVPG in surface-mounted “can” packages and KO-CAP T520 surface-mounted “tantalum chip” package. They are among the currently best-performing types on the market.¹⁴ SVPF and SVPG sport a rare 5000 h life expectancy at 105 ° C while the T520 has a more common one of 2000 h @ 105 ° C. Both have exceptionally low ESR and high capacitance for their size. This is not a capacitor evaluation, so focus is on properties that are believed to be generally applicable.

The “Capacitor selection for DC/DC converters” presentation by Texas Instruments (44) is a recommended read.

- Life expectancy at projected operating temperature = “Life @ 105” * 10^{((max temp - operating ambient temperature) / 20)}. (43) At 60 °C, the SVPF has a 139 year life expectancy and the T520 probably around 40 years. At 80 °C it’s 10 and 4 years respectively. That should be enough, especially since Mini-Box only uses 2000 h types.
- Frequency dependence for capacitance, ESR, and impedance: The OK-CAP T520 datasheet (45)¹⁵ contains plots of ESR, impedance, and capacitance vs. frequency for a few select models. One of them is the T520D337M006ATE009 that is used as combined bulk and transient output capacitor in the PSU. At roughly 200-300 kHz, the capacitance starts to decrease from the rated 330 μF to some 100 μF at 1 GHz. Worth noticing is that the same model with 15 mΩ (instead of 9 mΩ) starts to roll off at a lower frequency. This is in the middle of the frequency range for current DC/DC switch controllers. The ESR is invariable between a few kHz to a few GHz, but the impedance has a distinct minimum at about 200 kHz. The OS-CON behavior is similar (43), although the impedance dip center frequency differs from below 100 kHz to 1 GHz depending on model. The types used in this project are not included in the graphs. It was not (sufficiently easily) possible to find capacitance

¹⁴ The reader can easily verify this by doing a component search at one of the retailers’ web site.

¹⁵ http://www.kemet.com/Lists/ProductCatalog/Attachments/421/KEM_T2015_T520.pdf, p.3

vs. frequency information for the OS-CON types. The T520 datasheet states derating coefficients for maximum ripple vs. ambient temperature, while the SVPF datasheet contains derating coefficients for maximum ripple vs. frequency. (46)

- The capacitor models used (16SVPF1000M, 25SVPF330M, 16SVPG270M, 25SVPF180M, T520D337M006ATE009 all have very low ESR values (8-16 mΩ) and high maximum ripple current (4.65-5.8 A), which in some cases makes it ok to skip the ceramic “transient buffer” capacitor altogether. MLCCs typically have a higher center frequency for the impedance dip, which means that a combination of both types can give good transient response in a wider frequency range. (47)
- In some cases, MLCCs can be used both for bulk and transient capacitor, which is sometimes recommended by the TI WEBENCH design tool.

However, ceramic capacitors must be chosen with great care. The NP0/C0G (henceforth referred to as “NP0”) dielectric more or less behaves like you would expect. It is temperature stable and does not change much with DC or AC bias voltage. (48) Therefore it is often used where precision and consistency is needed, such as RC filtering and timing. The “problem” with this dielectric is that it has a low “volumetric efficiency”, which means that you at some point (when it is no longer feasible to change to a bigger package) must change to another dielectric.

Nowadays, X7R is probably the most common other dielectric, with X8R (higher temperature range) and X5R (lower temperature range but slightly higher maximum capacitance value than X7R) as common alternatives, henceforth referred to as “X7R”. This (family of) dielectric offers much higher capacitance value than NP0 in the same size, but they have greater temperature dependence than NP0, although X7R is often also called “temperature stable”. The main X7R weakness is its strong DC and AC bias. (49) (47) Energy storage capacitors are DC biased, e.g. at 12-20 or 12 V for the UPS in this project. At this level of DC bias, their actual capacitance is a fraction of the rated one. E.g. the TDK C3225X7R1E106M250AC (10 μF / 25V in 1210 package) has an actual capacitance of 6.73 μF at 16 V and 5.5 μF at 20 V DC bias. (50) The TDK C1608X5R1E106M080AC (10 μF / 25 V in 0603 package) has an actual capacitance of 0.788 μF at 16 V and slightly less at 20 V DC

bias, less than 10% of the rated value! This is before you take temperature dependency into account...

Generally, a smaller package means an earlier and steeper capacitance roll-off, but you cannot even expect the same performance from two equally-sized capacitors from the same manufacturer.¹⁶ Please note that this is not a TDK but an industry ‘problem’. The specification for the X7R dielectric leaves great levels of freedom for the manufacturer. (51) TDK products were chosen for this example simply because they have detailed datasheets for each model. Many manufacturers don’t even seem to publish any of this data. This phenomenon was emphasized by the introduction of the Base-Metal Electrode (BME) MLCC, which is cheaper to produce and enables bigger capacitance values in the same size than the Noble-Metal Electrode (NME). The NME has a less steep roll-off, which decreases with increased capacitor voltage rating (i.e. a bigger voltage rating is “better”). This isn’t always the case with BME. Vishay Vitramon is one of few manufacturers who have kept producing NME, but they also have a sister brand that produces BME so you need to be careful about which you get.

There is another dielectric with high volumetric efficiency that used to be common, the Y5V. Its capacitance value may change between +20% and -80% over the rated temperature range and its capacitance change vs. DC bias is even stronger than X7R’s. (48)

In many cases, a small-signal capacitor in a DC/DC switch circuit will only operate between 0 and, say, 2-3 V, so a BME would perform very well. The lesson is to always look at the individual datasheet of every capacitor model and to be prepared to change to a bigger package.

There is far more to know about ceramic capacitors, (52) but these are the properties most relevant to this project.

¹⁶ The reader is asked to verify this by looking at a few of the TDK capacitor at the company’s web site.

4.5 PCB Layout for SMPS

A good PCB layout is crucial when designing an SMPS and reducing Electro-Magnetic Interference (EMI) is of great concern. Practical design is a series of compromises where the importance of all the below factors are considered together with board size requirements and component choices.

Recommendations and checklists for the designer can e.g. be found in LT application note 139 and the switch controller datasheets: (53) (13) (14)

4.5.1 Current Loops

The buck and boost switch circuits form a series of loops that carry currents generally trapeze in shape. It's important to make the high-current traces wide and avoid routing other signals in such a way that they hinder this large flow of current.

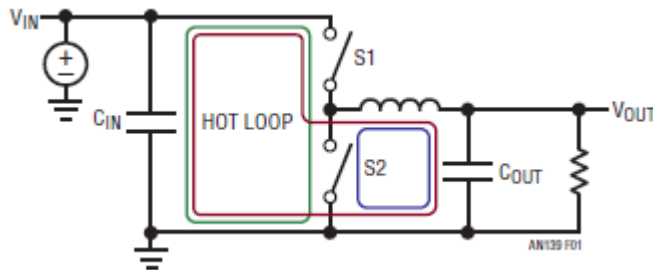


Figure 27: Buck current loops¹⁷ (Copyright Linear Technology, reprinted with permission)

When $S1$ is closed and $S2$ is open, current flows along the large red loop and in the opposite case current follows the small blue loop. However, the highest AC and EMI energy exist in the green loop that switches from zero to I_{peak} and back. This is called the hot loop. The boost circuit has corresponding loops and it is important to minimize the area of all such loops, especially the hot loop(s), in order to reduce radiation. Each of them acts like a magnetic antenna EMI emitter - the bigger the more powerful.

It's not only the high-current loops that are of concern. The same need applies to all AC-carrying signals, e.g. the gate drive traces.

Often, the switch controller is supplied from a self-generated $INTV_{CC}$ that's decoupled by a capacitor and together with signal ground and power ground is part of yet another loop that should be minimized.

¹⁷ Figure 27 - Figure 30: <http://cds.linear.com/docs/en/application-note/an139f.pdf>

4.5.2 Eddy Currents, Cancellation, and Shielding

A (ground) plane should be placed as close as possible to the signal layer. The hot loop generates eddy currents in the plane that produce a mirrored AC magnetic field of opposite direction to the hot loop field.

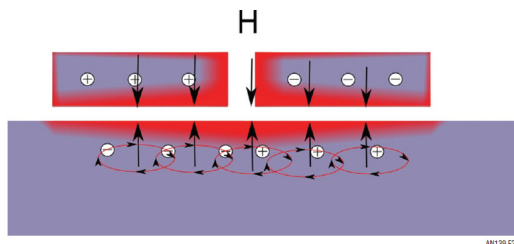


Figure 28: Eddy currents in the (ground) plane (53) (Copyright Linear Technology, reprinted with permission)

The cancellation effect is stronger the closer the two layers are. This means that SMPS PCBs should consist of more than two layers. A closely adjacent solid inner plane (like in a typical four-layer PCB) has less than 1/3 of the inductance of the bottom layer of a two-layer PCB and less than 1/14 of a single-layer board. Inductance is closely related to EMI emission.

The path of the ground plane loop current is the same as the signal layer path, in opposite direction but of equal strength. The resulting plane voltage manifests itself as ground bounce. So long as the plane is thicker than the skin and proximity effects, the plane also acts as a shield.

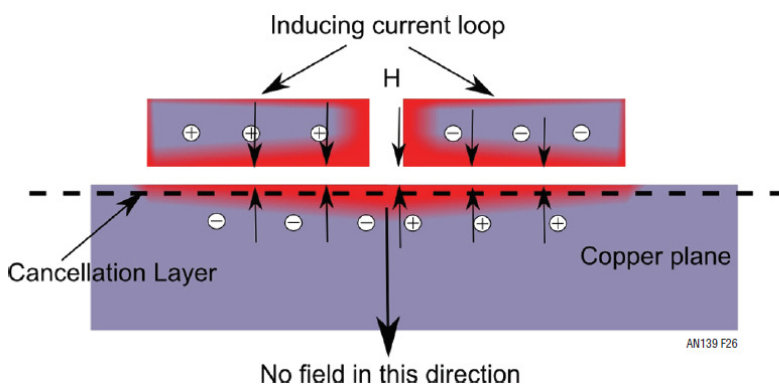


Figure 29: Cancellation and shielding (53) (Copyright Linear Technology, reprinted with permission)

The cancellation effect is even greater if the return current is routed through the plane. As the distance between the cancellation layer and the inducing trace is halved, so is the magnetic field for a doubled shielding effect.

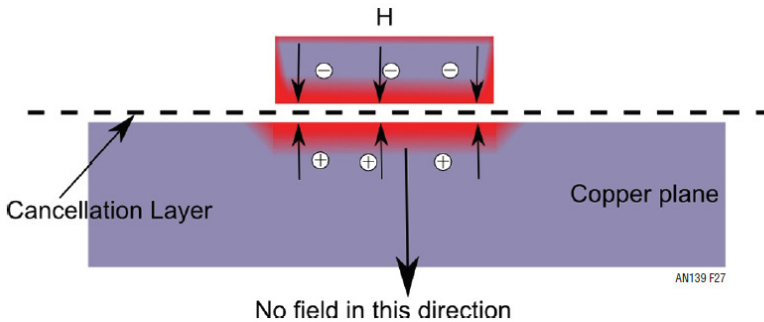


Figure 30: Cancellation layer with return current in the (ground) plane (53)
 (Copyright Linear Technology, reprinted with permission)

Filtering of input and output can be greatly improved by surrounding the SMPS with a ground ring connected with vias.

4.5.3 Inductor Placement and Routing

One should connect the inductor lead that goes to the inner-most or winding layer (or closest to the ground plane) to the hot loop. This provides some additional shielding and increases cancellation.

Inductors should be placed in such a way that their fields don't interfere with other power or filtering inductors.

4.5.4 Protecting Small-Signal Traces

The switch nodes generate large and varying currents that must be kept away from small-signal traces. For this reason, signal ground often forms an "island" around the switch controller that's connected to power ground close to the bottom switch(es).

Current monitoring is typically done with Kelvin sensing and the leads are routed as tightly as possible. If an RC network is used, the capacitor and parallel resistor should be placed as close to the switch controller and the serial resistor as close to the shunt resistor as possible. One must be very careful not to allow the sense leads to make contact with copper pours or other traces connected to the same node. They also mustn't couple with any of the loops, as duty cycle jitter can easily come from even sub-mV noise.

Signal traces should be routed as close as possible to the return trace (often the ground plane) for maximum cancellation and noise prevention.

4.5.5 Other Concerns

Unused PCB areas should be flooded with copper, often connected to ground or one of the rails. This improves heat dissipation.

The negative terminals of the input and output capacitors should be placed as close as possible.

For multi-phase operation the top N-channel MOSFETs must be placed within 1 cm of each other with a common drain connection to the input capacitor bank. Otherwise a resonant loop might occur.

Decoupling capacitors for e.g. INTVCC and the bootstrap circuitry should be placed close to the respective pins on the switch controller.

4.6 Device Package Selection

As far as possible, device packages with external pin-shaped leads should be used. It is easier to inspect solder joints that you can see without X-ray and failure data indicate that the solder joints of leg-based components have a far longer expected life than BGA and QFN packages: “A rough estimate of the number of cycles between -40 and 125 °C that the solder joints of the various components survive is for QFP >10 000, BGA 3 000 to 8 000, and QFN 1 000 to 3 000 cycles.” (55).

After some consideration, this advice is followed in all cases except the power FET transistors. This is because the current best performing models practically all have packages that are not leg-based. If and when the NXP LFPAK56 (56) FETs improve performance-wise, they should probably be used. In the long run, that means that only the PSU FETs will not be leg-based, but on the other hand the PSUs don't get very warm so thermal stress will be low.

4.7 Selection of DC/DC Switch Controllers

4.7.1 PSU

For the PSU, three models / families were considered:

- Linear Technology (LT) LTC3850 (14) (alternatively LTC3850-1/2 or LTC3869-2)
- Texas Instruments (TI) LM2642/LM5642/LM5642X (57) (58)
- Intersil (ISL) ISL6440 (59)

All are synchronous 2-phase current-mode buck regulators. The main properties are listed in the below table. One very interesting thing is that all three manufacturers have made a different design choice for the current sensing. LT senses the inductor or output series resistor, TI monitors the top FET or input series resistor, and ISL chose the bottom FET or series resistor to GND.

The TI decision to do current sensing over the top FET, with only the requirement that total current limit (DC bias + $\frac{1}{2}$ delta current) exceed 50 mV, could result in lower inductor losses. E.g. one of the best current top FET alternatives (BSZ060NE2LS) has an R_{DS-ON} of 6 - 8.1 m Ω , which at an 8 A load equates to a DC bias sense voltage of 48 - 64.8 mV. This would enable a lower inductor delta current (that causes core and AC losses) than the one required by LT. The LT design relies on a minimum 10-15 mV delta sense voltage drop for sufficient SNR, i.e. minimum inductor delta current. According to Swedish LT Field Application Engineers (FAE) (60), you may violate the recommendation, but at some point you will introduce duty cycle jitter that causes EMI spread-spectrum sub-harmonics.

Whether the above is a differentiator depends on the trade-off between inductor DCR losses and core + wire AC losses. The simulations indicate a tie, so according to the simulations there is no actual performance difference.

The LTC3850 family was chosen for the following reasons:

- Circuit designer-specified switch frequency, so that the optimum frequency could be used once the inductor test results were known.
- The possibility to automatically set the switch controller to the more energy-efficient burst mode when turned off, i.e. only outputting 5 V standby. This should be the state in which it will be spending the most of its active life, so it's an important energy-saving feature.
- Greater freedom in terms of sense voltage range. (Due to LT pin assignment decisions, the (more or less) pin-compatible alternatives have a fixed sense voltage range but instead enable the switch controller LDO to be fed from the 5 V standby output, which improves efficiency. For the prototype, the greater sense voltage freedom was preferred.)
- Excellent design tool support.
- A good working relationship with the Swedish Linear Technology FAEs.

Please see the below table for a feature comparison.

Property	LTC3850	LM2642	LM5642	LM5642X	ISL6440
Switch frequency, kHz	250-780	300	200	375	300
Switch modes	Burst mode Pulse-skipping Force continuous	Force continuous only?			Force continuous only?
Soft start	Yes, and voltage tracking	Yes, and sequenced start of channel 2 by dedicating PGOOD1 to ON/SS2 pin.			Yes
Output current limiting with over-current protection	Yes	Yes			Yes
Current sensing	Inductor DCR or sense resistor between inductor and output.	Top FET RDS-ON or sense resistor between input and top FET.			Bottom FET RDS-ON or sense resistor between bottom FET and GND.
Sense voltage recommendation	Customer selects 30 mV, 50 mV, or 75 mV threshold. A 15 mV p-p delta is recommended for good SNR. (10 mV probably ok.)	50 mV recommended sense voltage drop for good SNR. 200 mV max.			None?
Self discharge of output capacitor	No?	Yes			No?
Package	28-pin narrow SSOP (6*9.9 mm) QFN (4*4 or 4*5 mm)	28-pin TSSOP (6.4*9,7 mm) Optional thermal pad			24-pin QSOP (6*8.7 mm)
Over- and under-voltage protection	Only over-voltage protection	Yes			Only under-voltage protection
Digikey SEK	41.85	N/A	37.66	38.77	45.52
Mouser SEK	N/A	31.50	37.19	44.64	48.56
Farnell SEK	53.35	38.70	26.58	56.30	N/A

Table 8: PSU DC/DC switch controllers considered, unit price on 2015-08-20

4.7.2 UPS Buck/Boost for the Main 12 V Rail

For a long time, Linear Technology (LT) was the only manufacturer of switch controllers for high-current four-switch, one-inductor, buck/boost circuits. In 2005, the LTC3780 (61) was introduced as the first 4-switch controller. (62) In 2010, the slightly improved LTC3789 (63) (64) was released. A few years later, the LT3791-1 (65) included C/10 charge termination signaling, output of average input and output current signals to ADC, and the explicit ability to also connect one or more current-mirroring slave circuits for high-current multi-phase operation.¹⁸ Finally, the LT3790 (13) is a minor revision of LT3791-1 with e.g. lower sense voltage requirements, which enables use of smaller resistors, i.e. lower power losses and higher possible current delivery.

This year, Texas Instruments (TI) released its first comparable controller, the LM5175. (66) Its features are similar to LTC3780 and LTC3789. TI has older buck/boost controllers, e.g. the LM25118, (67) but it is a 2-switch design with schottky diodes instead of synchronous FETs, which means high-current operation is not possible (without excessive cooling). The product web site specifies 4 A as the maximum output current. Although the LM5175 should be able to handle large load currents, the WEBENCH design tool doesn't support a circuit that outputs 12 V, 16 A.

	LM5175	LTC3789	LT3790
Mouser	92.73	N/A	N/A
Farnell	114.60	100.65	75.85
Digikey	93.68	81.56	86.68

Table 9: Buck/boost controller unit price 2015-08-21, SEK

The choice between suppliers is easy. You don't pay more for a first-generation product without design tool support for your application needs. As LTC3789 and LT3790 are similarly priced, the choice was to use LT3790 for the UPS main rail and buck/boost boards.

¹⁸ This had been possible with the previous two as well by sharing the control loop RC network, but that could in some cases experience current delivery imbalances between the participating controllers, especially in the so called "buck/boost region". An unofficial LT application note discusses this and suggests an alternative interconnection approach.

4.7.3 UPS Battery Charger Switch Controller

The battery charger has to be a buck/boost circuit. The LT3790's support for C/10 signaling and automatic switch-over to the lower-loss pulse-skipping mode and change from high-current 14.5 V bulk to 13.5 V trickle charge are valuable here, as is the possibility to set a current delivery ceiling via a (DAC-controlled) voltage on the CTRL pin. This enables the customer to easily specify maximum bulk charge current. The built-in average output current ADC signal eliminates the need for a separate current monitor (such as the AD8219 (68) or similar).

In a previous design, the simpler LT1513-2 (69) was used. As it has an integrated switch transistor, it has a considerably lower maximum charge current (slightly more than 1 A for the UPS operating points) and gets warmer than an LT3790 circuit at the same charge current. It might therefore require a small heat sink, but it has a much smaller component count. It is possible to control the charge current ceiling via DAC or simple transistor-based resistor parallelization, but you need a separate current monitor and base C/10-related mode changes on that, typically from a microcontroller.

The LT3790 was chosen for the first MODPSU UPS and the LT1513-2 could perhaps be used for a future smaller version of the UPS.

CHAPTER 5

5 Simulations and Experiments

5.1 UPS 12 V main rail FET Losses

We have seen how FET transistor switching losses depend on frequency, load current, and input rail voltage, but reading formulas is not the same as seeing the manifestation of a phenomenon.

The most heavy-duty of the switch circuits is the UPS 12 V main rail. It will only be clearly in the boost region for a short period at the end of the battery discharge. UPS battery charging is done very rarely and the PSU is a pure buck circuit. For this reason, I did a buck simulation of FET UPS 12 V main rail losses @ 20 V input using two of the transistors with the lowest buck losses at the lower end of the frequency range:

- Buck top and boost bottom: BSC024NE2LS
- Buck bottom and boost top: BSC010NE2LSI

This FET loss simulation was done with the Coilcraft SER2010-202, a 2.0 μH inductor. The simulations were based on the PowerDesign Excel Tool for LT3791-1. For the sake of simplicity, the same FETs are used for all simulations (frequencies and loads) even though slightly lower losses might be achievable for other FET combinations in certain situations.

By parallelizing the top FET, you can sometimes trade lower conduction losses for higher switching losses. For this reason, the buck simulation includes both one and two top FETs.

These one-FET losses were added to the inductor losses in the buck/boost simulations. All UPS 12 V main rail simulations are done at 20 V input, which is higher than most users will use but it tells us the worst-case scenario's losses.

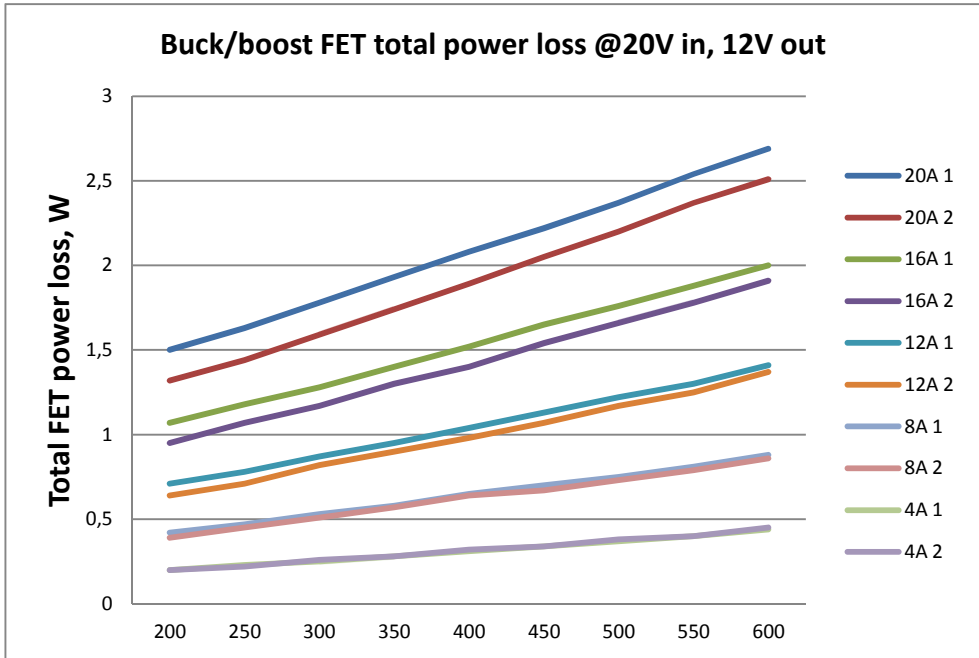


Figure 31: 20 to 12 V buck FET losses as a function of frequency and load

5.2 Combined PSU FET Losses

The PSU inductor selection is more restricted than the one for the UPS 12 V main rail. The desire to use a specific type of tantalum chip-format polymer capacitors for the two outputs (3.3 and 5 V) puts an upper limit to the switching frequency somewhere at 300 to 350 kHz, with an unknown precise location.

The choice to use a switch controller from Linear Technology introduced a demand for 10-15 mV minimum delta sense voltage, which is largely dependent on the inductor ripple current. In practice, there is thus a fairly small range of viable inductance values and switching frequency combinations, from 2.2 to 6.0 μH and from 350 to 250 kHz.

Two of the transistors with the lowest buck losses at 250 kHz were chosen:

- Top: BSZ036NE2LS
- Bottom: BSZ018NE2LSI

The FET loss simulation was done with the actual inductor, but the figures are in almost all cases identical between the different inductors. The simulations are based on the LTPowerCAD II tool for LTC3850.

These FET losses were added to the inductor losses in the simulations. The deviating number for 1 A @ 300 kHz is assumed to be caused by a tool bug.

It is possible to switch to another top FET at higher frequencies, but the effect of that is marginal in this small frequency range.

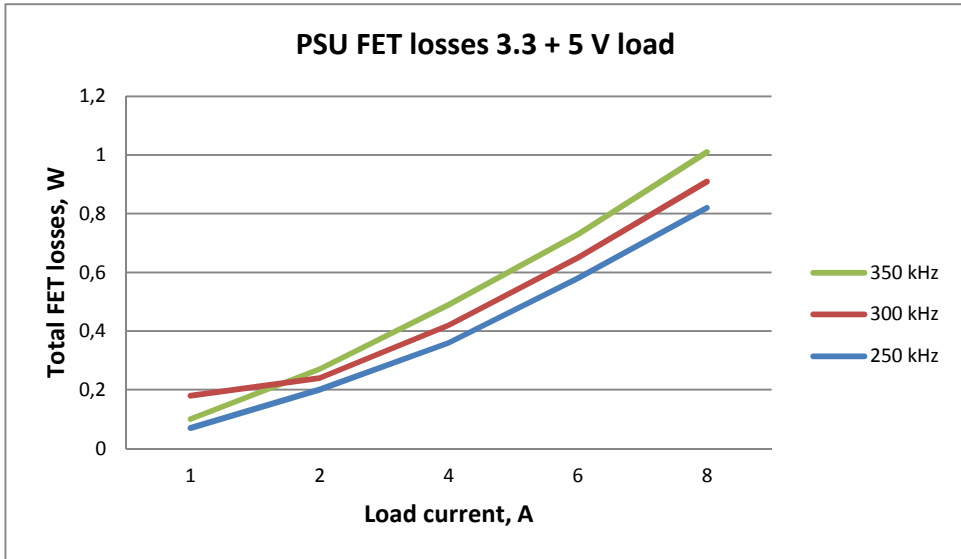


Figure 32: PSU FET losses

5.2.1 Charger FET Losses

The same FET transistors as those used for the PSU were chosen.

The FET loss simulation was done with the WE HCI1365 7443551370, a 3.7 μH inductor. The simulations were based on the LTPowerCADII Tool for LTC3789.

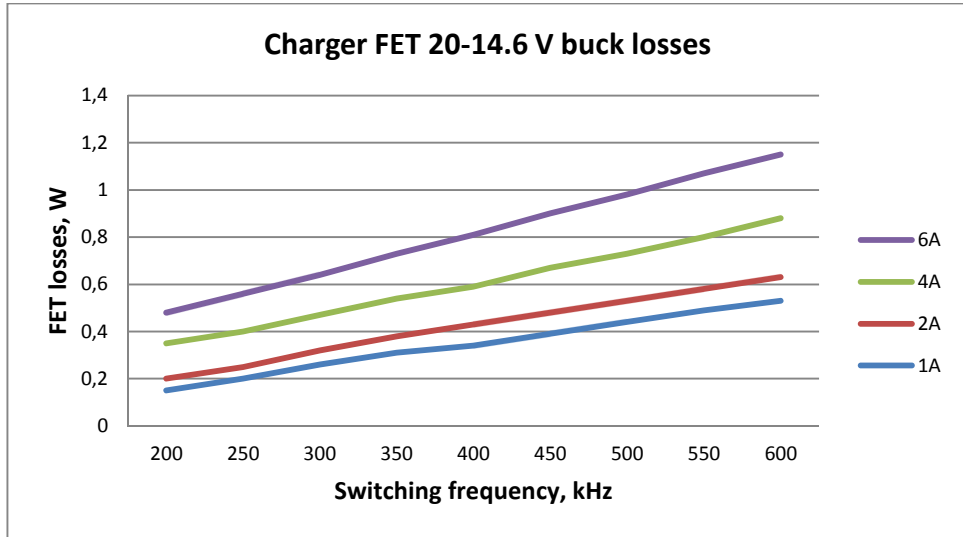


Figure 33: Charger FET buck losses

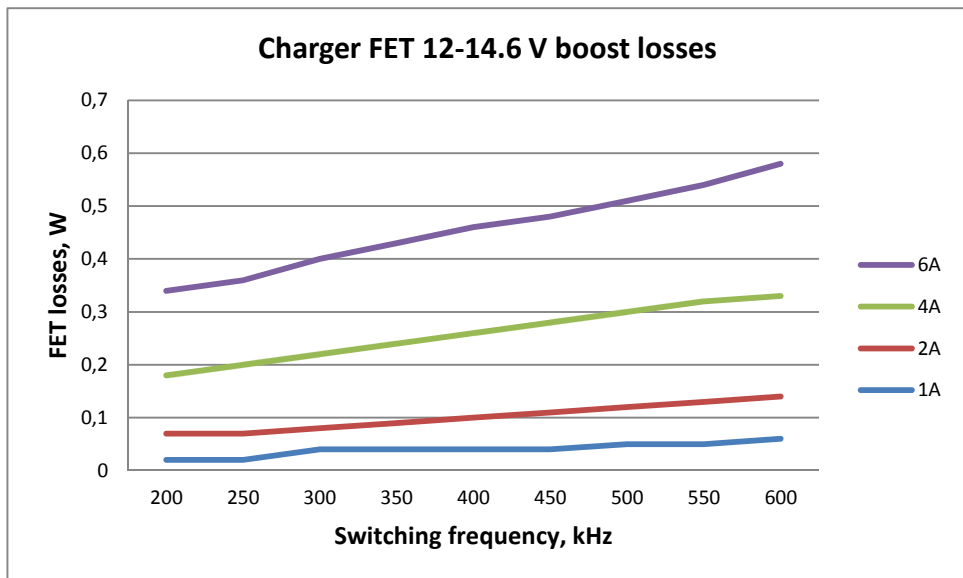


Figure 34: Charger FET boost losses

5.3 Comparison of different charger top FETs

Doing the simulation with the same FETs for all parts of the simulation makes the process easier and also demonstrates how one specific model behaves over a certain frequency range, but it in this case it biases the simulation results in favor of lower frequency operation. The question is how great this bias is. For the charger, the most “lossy” transistor is the top buck FET. In the following table, the two best alternatives over the frequency range are compared at a 6 A load. The naming convention for these component is such that “036” and “060” relate to $r_{ds(on)}$, where the higher of these has lower capacitances:

Frequency, kHz	BSZ036NE2LS	BSZ060NE2LS
200	0.28	0.31
250	0.32	0.34
300	0.37	0.37
350	0.41	0.41
400	0.46	0.44
450	0.50	0.47
500	0.55	0.51
550	0.59	0.54
600	0.63	0.58

Table 10: 20-12 V @ 6 A buck top FET loss comparison, W

In this particular case, the transistor chosen for the simulation is the best one in the entire considered frequency range (up to 350 kHz). In the 3.3 * 3.3 mm package (BSZ), the number of alternatives isn’t as large as for the 5.6 * 5.6 mm (BSC), but it is at least an indication that the simulations give usable information.

5.4 Accuracy of Inductor Loss Calculators, pt. 1

At the end of chapter 5, I will compare simulation results to actual loss measurements. This short note is necessary background to the presentation of the simulation results.

5.4.1 Comparison of WE Component Selector and REDEXPERT

My initial WE simulation was done with Component Selector (CS). When the first efficiency and loss measurements showed very contradictory results, I contacted WE for a discussion on 2015-09-12 (70). I had earlier been recommended to use the (not yet publicly released) online tool RED EXPERT (RE) instead of the PC software CS, but I hesitated as I had already done much simulation work with CS and I also don't like the way companies collect ever more information about their users.

I sent the below comparison, made at 20 V in, 12 V 10 A out, 355 kHz, 48% ripple, and 0.3 V diode drop:

	RED EXPERT			Component Selector			Difference	
	DCR	AC	Total	DCR	AC	Total	Absolute	Fraction
7443551280	340	467	807	347	265	612	195	76%
7443556260	158	1410	1568	162	232	394	1174	25%
7443630220	150	574	724	155	2	157	567	22%
7443630310	209	407	616	212	1	213	403	35%

Table 11: WE Component Selector vs. REDEXPERT, mW, 2015-09-12

The numbers speak for themselves. Presumably WE had already realized the need for an extreme makeover and RE was officially released 2015-08-05 as “the world's most precise AC loss calculation”. (71)

Both CS and RE results are included for the UPS 12 V main rail and the PSU, but only CS for the charger.

5.4.2 Vishay and Coilcraft Core Loss Simulator Results

The Vishay core loss calculator consistently presented the highest figures.

The SER201X (PQ-ish core) results from the Coilcraft core loss calculator are similar to the WE CS HCF PQ ones. I reported my findings to them in September 2015 and was told that “We do plan to review and revise our loss calculations for SER (and other) inductor series in the near future”. (72) However, 2016-05-09 this is still on their to-do list.

5.5 Inductor Simulation Example

I spent great many hours on simulations of several inductance values for each of the competing inductors @ 2, 4, 8, and 20 A load current @ 200 – 600 kHz @ 20 V input and 12 V output. In retrospect it is clear that its value is highly questionable, so I will only present an example that clarifies my approach and goal:

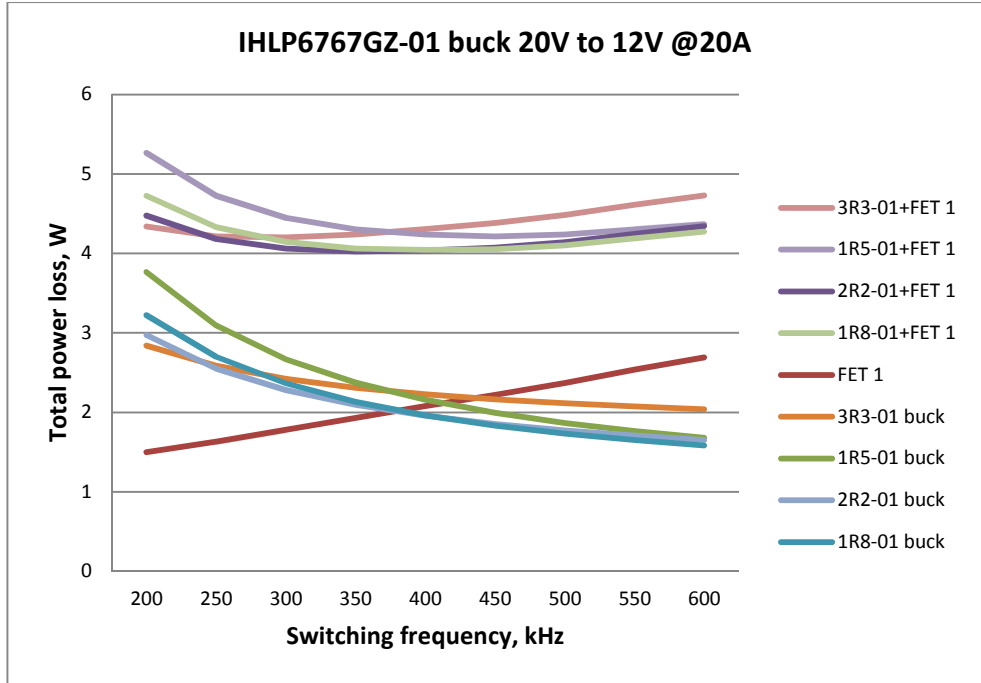


Figure 35: Loss simulation in pursuit of the “sweet spot” where the combined inductor and FET losses are at a minimum

The idea was to use these simulations to find the inductance value and switching frequency that yield the best compromise between low and high-current operation.

The sweet spot shifts to the right at lower load currents, which is demonstrated by the next graph:

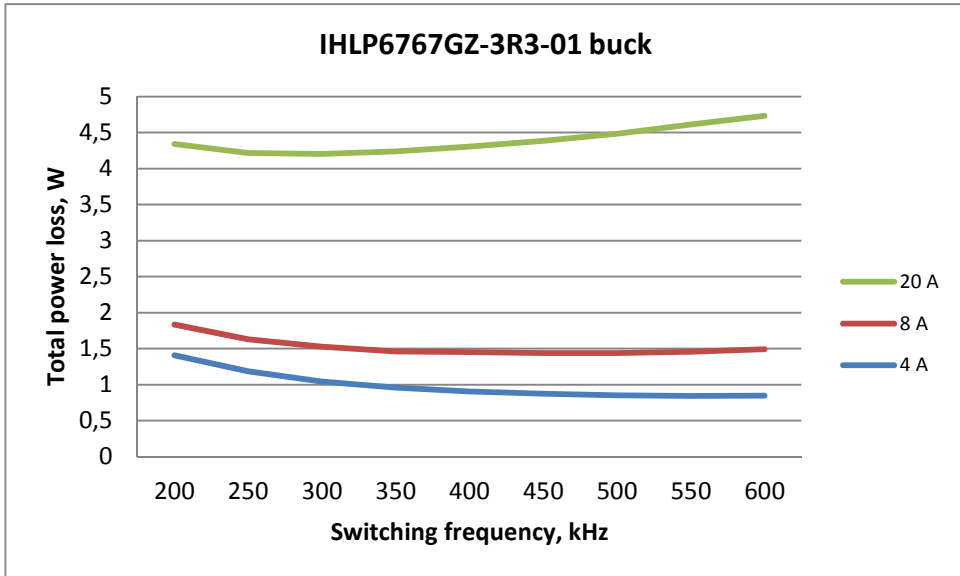


Figure 36: Total losses at different load currents

In this example, the 2.2 or the 3.3 μH versions switched at about 300 to 350 kHz look like a good choice. There is a similar graph for each model. The more “optimistic” core loss calculation, the lower the sweet spot. This is the reason for the different switching frequencies in the first efficiency and loss measurement and the subsequent change to 368 kHz for all inductors in the second test.

5.6 Summary of the UPS Simulation Results

The loss data for the “best” inductor of each type was combined into three graphs, 4, 8, and 20 A load for a 20 to 12 V buck application.

Model	Inductance, μH	DCR, $\text{m}\Omega$	Saturation current
SER2011-202	2.0	1.34	37.0 A @ 10% drop
HCF2013 7443630220	2.2	1.50	52.0 A @ 30% drop
HCI1890 7443556260	2.6	1.58	50.0 A @ 30% drop
XAL1580-302	3.0	1.91	43.0 A @ 30% drop
IHLP6767GZ-3R3-11	3.3	2.79	27.0 A @ 20% drop
IHLP6767GZ-3R3-01	3.3	3.68	54.0 A @ 20% drop

Table 12: Inductor properties

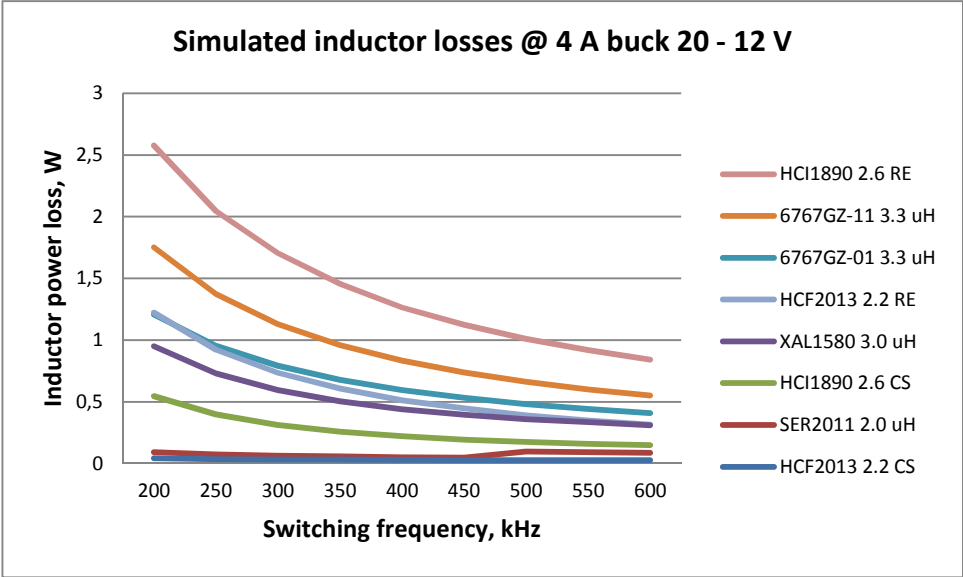


Figure 37: Simulated inductor losses at 4 A load (RE 2015-09)

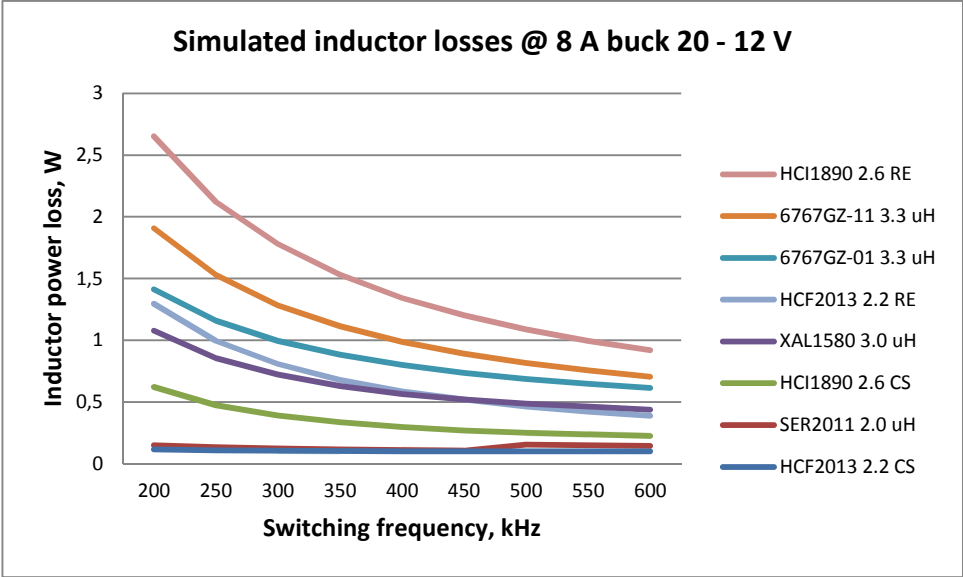


Figure 38: Simulated inductor losses at 8 A load (RE 2015-09)

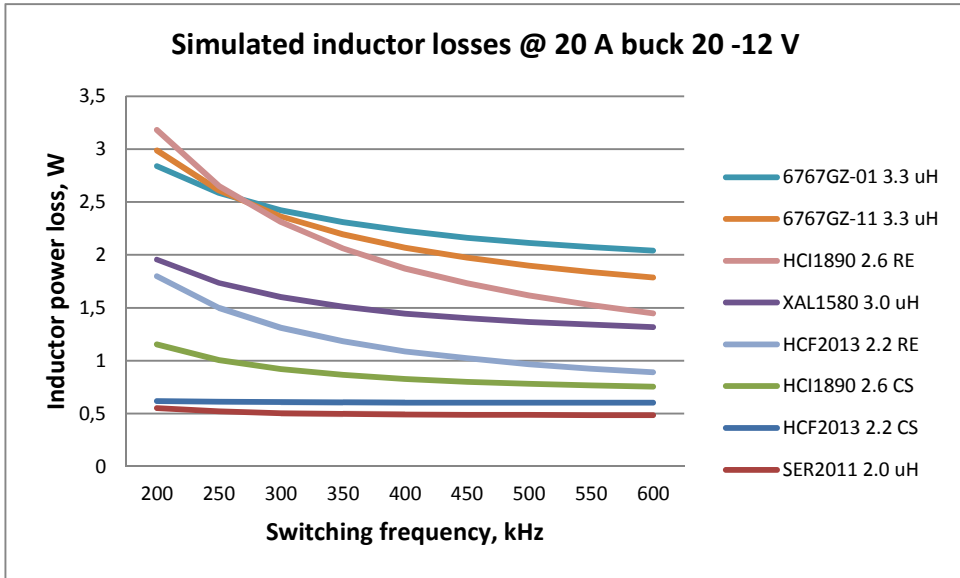


Figure 39: Simulated inductor losses at 20 A load (RE 2015-09)

The difference between the Würth Elektronik Component Selector (CS) and RED EXPERT (RE) creates uncertainty about all simulated inductor losses. Instead of summarizing this data further, let's wait until we have the temperature rise and efficiency measurements results.

5.7 Summary of the PSU Simulation Results

According to the simulation, the best XAL1010 combination is 4.7/5.6 μH @ 250 kHz. 5.6/6.8 is slightly better below 4 A but then loses at higher currents. 2.2/3.3 requires 350 kHz but has much higher losses throughout.

When FET losses are taken into account, all IHLP5050FD-01 combinations are fairly similar. It stands between 4.7/5.6 and 3.3/4.7 μH depending on preferred trade-off between low and high load currents.

For HCI1365, all three simulated combinations are very alike. 3.7/4.7 is slightly worse than 4.7/6.0 μH below 4 A and clearly better above. The former would give a better sense voltage signal to noise ratio, while the latter would keep it in continuous inductor conduction down to about 1 A per rail, 0.25 A less than the 3.7/4.7 μH design.

Judging by these simulations, the inductor ripple currents required by the Linear Technology switch controllers don't result in higher total losses.

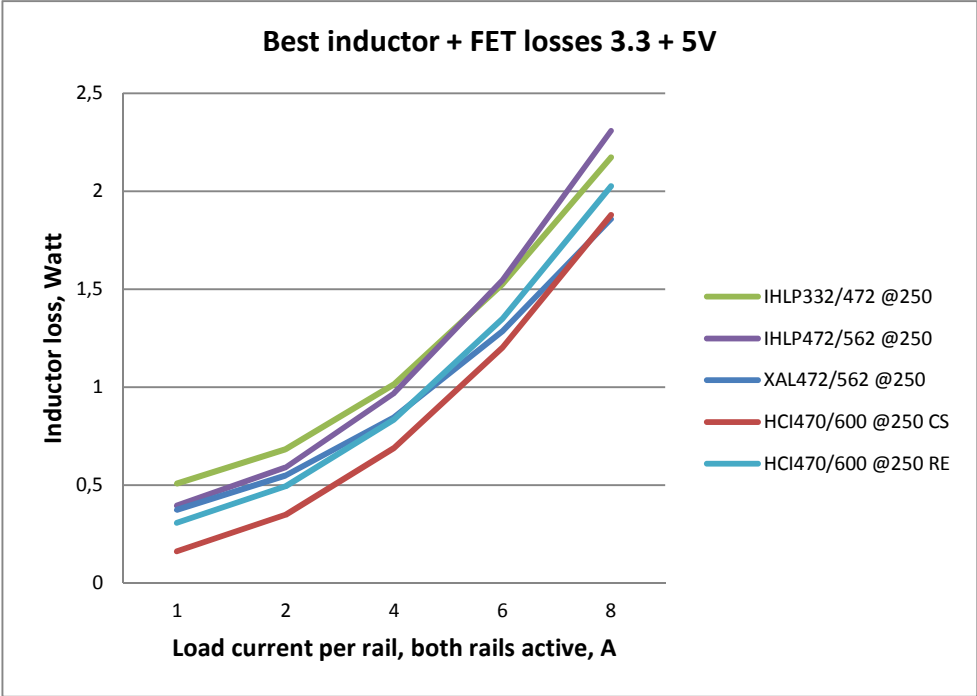


Figure 40: Total losses of the best alternatives from all manufacturers

When the best inductor(s) from each manufacturer are compared, the WE HCI1365 combination has better simulation results. As in the UPS 12 V buck/boost simulation, the Coilcraft XAL comes in second followed by the Vishay Dale IHLP.

5.7.1 Summary of the Charger Simulation Results

The loss data for the “best” inductor of each type was combined into two graphs; one for buck 20-14.6 V and one for boost 12-14.6 V.

Model	Inductance, μH	DCR, $\text{m}\Omega$	Saturation current
SER1412-362	3.6	1.30	12.1 A @ 30% drop
HCI1365 7443551370	3.7	4.90	16.0 A @ 30% drop
XAL1010-472	4.7	5.20	17.5 A @ 30% drop
IHLP5050FD-4R7-01	4.7	8.00	32.0 A @ 20% drop

Table 13: Charger inductor properties

The charger is the least critical of the three switch circuits and the results from the UPS 12 V main rail evaluation are applicable to the charger as well. When I had to get to the bottom with the contradictory simulation and

measurement results, the charger was demoted and I did not update the charger simulations with WE RED EXPERT data.

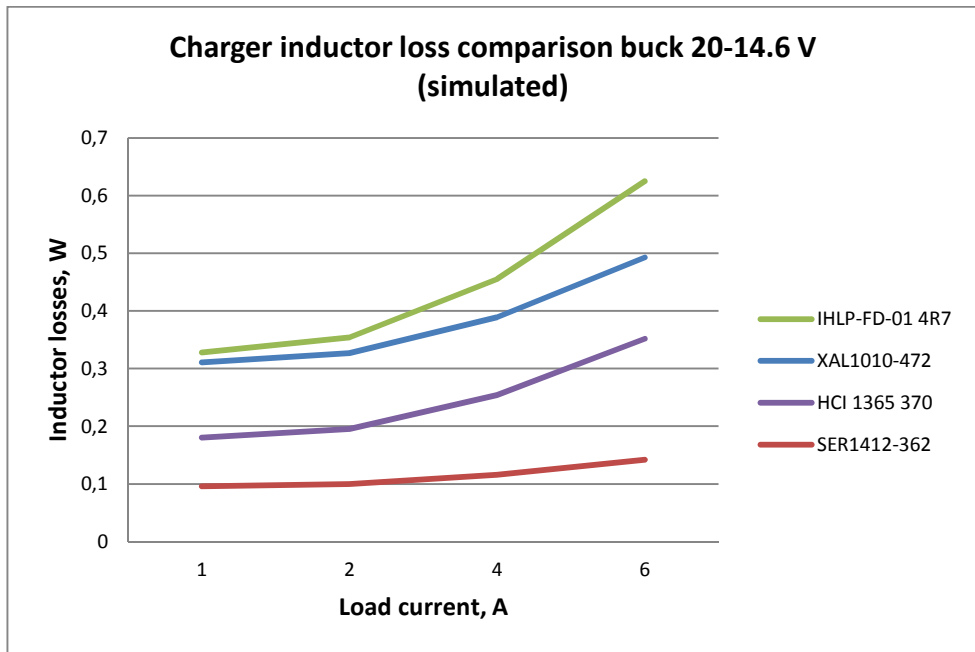


Figure 41: Charger inductor loss comparison buck 20-14.6 V, HCI from CS

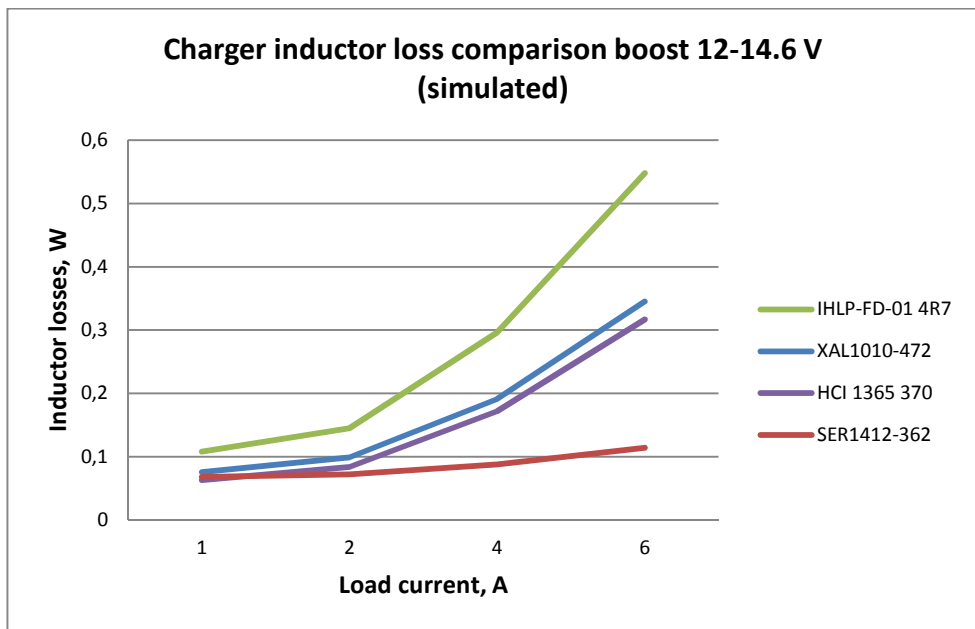


Figure 42: Charger inductor loss comparison boost 12-14.6 V, HCI from CS

5.8 Temperature Rise Measurement Results

The temperature rise measurements were made on the top of the inductor (T), on the outside middle of the exposed coil (C) and on the plastic top of the bottom buck FET (F). Ambient temperature was recorded and the figures are temperature rise. Actual inductance at zero DC bias was measured. I don't have access to equipment for mΩ measurement.

The loads are four configurations of halogen light bulbs, with the specified load current stated in the table header.

Three different switching frequencies were tested: 237 (non-linear result of frequency setting 200), 304, and 404 kHz.

Company	Model	Ind typ, μH	Inductance measured @ 23 ° C	DCR typ, mΩ
Würth	HCI1890 7443556190	1.9	2.16	1.20
Würth	HCI1890 7443556260	2.6	2.68	1.58
Würth	HCI1890 7443556350	3.5	3.66	3.10
Vishay Dale	IHLP6767GZER1R5M01	1.5	1.74	1.78
Vishay Dale	IHLP6767GZER1R8M01	1.8	2.02	1.96
Vishay Dale	IHLP6767GZER2R2M01	2.2	2.56	2.40
Vishay Dale	IHLP6767GZER1R5M11	1.5	1.81	1.54
Vishay Dale	IHLP6767GZER1R8M11	1.8	2.09	?
Vishay Dale	IHLP6767GZER2R2M11	2.2	2.58	1.85
Coilcraft	XAL1580-182	1.8	1.99	1.61
Coilcraft	XAL1580-202	2.0	2.03	1.91
Coilcraft	XAL1580-302	3.0	3.09	2.62
Würth	HCF2013 7443630220	2.2	2.23	1.50
Würth	HCF2013 7443630310	3.1	3.12	2.09
Coilcraft	SER2010-202	2.0	2.19	0.90
Coilcraft	SER2011-202	2.0	1.98	1.20
Coilcraft	SER2013-362	3.6	3.99	1.70
Würth	HCI1365 7443551370	3.7	3.93	4.90
Würth	HCI1365 7443551470	4.7	5.48	7.00
Vishay Dale	IHLP5050FDER3R3M01	3.3	3.65	5.70
Vishay Dale	IHLP5050FDER4R7M01	4.7	4.98	8.00
Coilcraft	XAL1010-222	2.2	2.26	2.55
Coilcraft	XAL1010-332	3.3	3.39	3.70
Coilcraft	XAL1010-472	4.7	4.86	5.20
Coilcraft	XAL1010-562	5.6	6.03	6.30
Coilcraft	SER1412-152	1.5	1.69 (1.71 @ 50 ° C)	1.30
Coilcraft	SER1412-362	3.6	3.71	1.30
Average inductance		2.81	3.03 (7.76% higher)	

Table 14: Inductor temperature measurement properties

Model	Amb. ° C	10 W 0,83 A typ 0,82 A meas			20 W 1,67 A typ 1,58 A meas			50 W 4,17 A typ 4,02 A meas			100 W 8,33 A typ 8,25 A meas				
		T	C	F	T	C	F	T	C	F	T	C	F		
		HCI1890 7443556190	22	21		9	22		10	24		13	26		19
HCI1890 7443556260	22	18		10	18		10	21		13	24		20		
HCI1890 7443556350	22	13		10	17		12	20		13	22		20		
IHLP6767GZER1R5M01	22	16		10	17		10	18		11	23		19		
IHLP6767GZER1R8M01	22	14		8	14		8	15		11	21		18		
IHLP6767GZER2R2M01	22	13		8	13		7	15		11	21		19		
IHLP6767GZER1R5M11	22	22		8	22		10	23		12	26		19		
IHLP6767GZER1R8M11	21	19		8	20		10	20		13	23		19		
IHLP6767GZER2R2M11	22	18		9	17		8	19		12	22		19		
XAL1580-182	22	19		8	19		9	20		13	24		20		
XAL1580-202	21	22		8	22		8	22		11	25		19		
XAL1580-302	21	12		8	13		8	15		11	22		18		
HCF2013 7443630220	22	11	13	8	11	12	8	12	14	10	14	20	16		
HCF2013 7443630310	21		9	9	7		9	10	8	10	12	11	11	14	17
SER2010-202	22	11	12	7	12	13	9	12	14	11	15	17	18		
SER2011-202	22	11	13	8	11	13	8	12	14	10	14	17	16		
SER2013-362	21	10	10	8	10	10	8	11	12	11	12	14	17		
HCI1365 7443551370	22	11		8	11		8	14		11	21		20		
HCI1365 7443551470	22	9		7	9		8	13		11	25		20		
IHLP5050FDER3R3M01	22	11		8	12		8	14		10	29		19		
IHLP5050FDER4R7M01	22	10		8	10		8	15		10	31		21		
XAL1010-222	22	24		10	24		10	24		14	29		20		
XAL1010-332	22	14		9	16		9	17		11	26		20		
XAL1010-472	22	11		7	11		7	16		11	25		18		
XAL1010-562	22	10		6	12		7	14		10	27		18		
SER1412-152	22	28	40	11	30	42	13	31	47	16	36	47	24		
SER1412-362	22	10	12	8	12	13	9	13	14	10	19	17	19		
Average	22	15	16	8	15	16	9	17	18	12	23	21	19		

Table 15: Temperature rise readings (° C), buck 16.5-12 V @ 237 kHz

Model	Amb. ° C	10 W 0,83 A typ 0,82 A meas			20 W 1,67 A typ 1,58 A meas			50 W 4,17 A typ 4,02 A meas			100 W 8,33 A typ 8,25 A meas		
		T	C	F	T	C	F	T	C	F	T	C	F
		HCI1890 7443556190	23	16	8	19	10	22	14	23	19		
HCI1890 7443556260	23	16	8	17	10	18	13	20	19				
HCI1890 7443556350	23	13	8	14	9	15	12	16	19				
IHLP6767GZER1R5M01	23	14	8	14	9	15	11	19	18				
IHLP6767GZER1R8M01	23	11	7	12	7	11	10	16	17				
IHLP6767GZER2R2M01	23	9	7	10	7	12	11	18	18				
IHLP6767GZER1R5M11	23	19	9	19	10	20	12	23	19				
IHLP6767GZER1R8M11	23	14	7	15	8	16	11	19	18				
IHLP6767GZER2R2M11	23	14	8	15	9	17	13	21	19				
XAL1580-182	23	15	9	16	9	16	11	19	22				
XAL1580-202	23	17	8	17	9	18	12	22	20				
XAL1580-302	23	10	8	11	9	13	11	18	20				
HCF2013 7443630220	23	9	10	7	8	10	7	9	12	9	11	16	18
HCF2013 7443630310	23	6	8	6	8	8	7	8	9	9	9	12	15
SER2010-202	22	11	11	8	11	11	8	11	12	10	16	18	18
SER2011-202	22	11	12	8	11	12	8	12	13	12	15	17	19
SER2013-362	22	9	9	8	9	10	8	10	11	11	11	14	17
HCI1365 7443551370	21	9	7	10	8	13	11	22	19				
HCI1365 7443551470	22	8	7	8	8	11	10	24	20				
IHLP5050FDER3R3M01	22	11	8	11	8	14	11	30	22				
IHLP5050FDER4R7M01	22	8	7	10	9	14	11	30	22				
XAL1010-222	22	16	8	17	9	20	14	25	22				
XAL1010-332	22	13	8	13	9	15	13	26	22				
XAL1010-472	22	12	9	12	9	14	13	25	22				
XAL1010-562	23	11	8	11	8	14	12	26	20				
SER1412-152	23	23	30	10	24	30	11	25	34	16	29	40	23
SER1412-362	23	8	9	7	9	11	9	12	13	12	16	19	19
Average	23	12	13	8	13	13	9	15	15	12	20	19	19

Table 16: Temperature rise readings (° C), buck 16.5-12 V @ 304 kHz

Model	Amb. ° C	10 W 0,83 A typ 0,82 A meas			20 W 1,67 A typ 1,58 A meas			50 W 4,17 A typ 4,02 A meas			100 W 8,33 A typ 8,25 A meas		
		T	C	F	T	C	F	T	C	F	T	C	F
		HCI1890 7443556190	23	14	9	16	11	16	14	20	22		
HCI1890 7443556260	23	13	9	13	10	14	12	17	22				
HCI1890 7443556350	23	12	9	12	10	13	13	21	24				
IHLP6767GZER1R5M01	23	10	8	11	8	14	13	21	26				
IHLP6767GZER1R8M01	23	10	8	11	9	12	12	20	22				
IHLP6767GZER2R2M01	23	8	7	8	7	11	12	20	22				
IHLP6767GZER1R5M11	22	17	9	17	10	18	14	24	23				
IHLP6767GZER1R8M11	22	14	9	15	11	18	15	21	25				
IHLP6767GZER2R2M11	23	13	9	14	10	15	14	22	24				
XAL1580-182	23	12	8	13	9	14	13	18	22				
XAL1580-202	23	13	8	14	9	15	13	22	23				
XAL1580-302	23	10	8	10	9	12	13	18	21				
HCF2013 7443630220	22	5	8	7	7	9	8	9	11	13	12	16	23
HCF2013 7443630310	22	7	8	7	8	9	9	9	11	13	11	16	22
SER2010-202	22	9	10	9	9	10	10	11	12	13	17	18	24
SER2011-202	22	10	11	9	10	11	9	11	13	12	15	17	23
SER2013-362	22	8	9	9	9	10	10	10	11	13	15	17	23
HCI1365 7443551370	23	9	9	10	9	12	13	20	22				
HCI1365 7443551470	24	7	8	9	9	11	12	26	23				
IHLP5050FDER3R3M01	24	9	8	9	8	12	12	25	23				
IHLP5050FDER4R7M01	24	6	7	8	8	13	12	29	24				
XAL1010-222	24	14	8	15	10	17	13	24	23				
XAL1010-332	24	11	9	11	9	14	12	24	23				
XAL1010-472	24	9	8	9	8	12	12	24	23				
XAL1010-562	24	9	9	9	8	13	12	25	23				
SER1412-152	24	19	23	10	19	23	10	20	25	15	24	28	23
SER1412-362	24	8	9	9	8	9	9	10	11	12	15	18	23
Average	23	11	11	8	11	12	9	13	13	13	20	19	23

Table 17: Temperature rise readings (° C), buck 16.5-12 V @ 404 kHz

	237 kHz	304 kHz	404 kHz
Top 0.82 A	14.7	12.3	10.6
Top 1.58 A	15.3	13.0	11.3
Top 4.02 A	17.0	14.6	13.2
Top 8.25 A	22.7	20.3	20.4
Coil 0.82 A	15.6	12.7	11.1
Coil 1.58 A	16.1	13.1	11.6
Coil 4.02 A	18.1	14.9	13.4
Coil 8.25 A	20.9	19.4	18.6
FET 0.82 A	8.3	7.8	8.4
FET 1.58 A	8.8	8.6	9.1
FET 4.02 A	11.5	11.7	12.9
FET 8.25 A	19.0	19.5	23.0

Table 18: Average temperature rise summary, °C

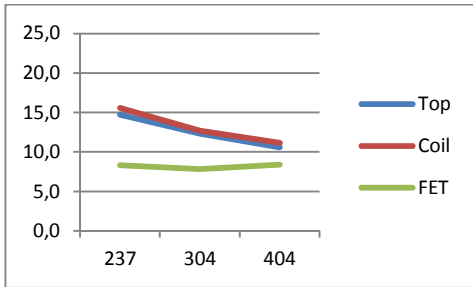


Figure 43: Avg. temp. rise, 0.82 A load

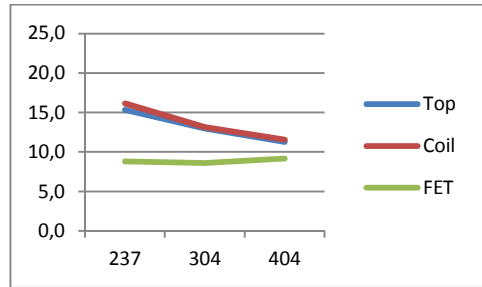


Figure 45: Avg. temp. rise, 1.58 A load

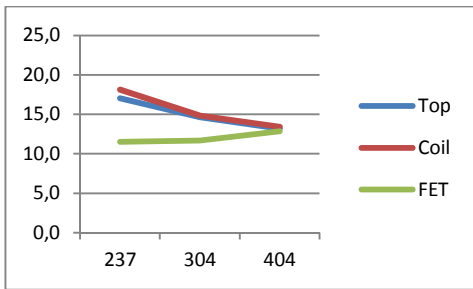


Figure 44: Avg. temp. rise, 4.02 A load

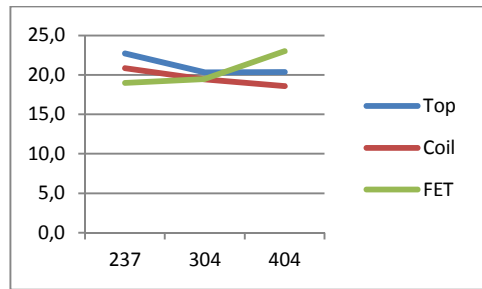


Figure 46: Avg. temp. rise, 8.25 A load

5.8.1 Discussion of the Temperature Rise Measurement Results

The "non-inductor" (here referred to as "FET") heat generation consists of power dissipation in FET transistors, shunt resistors, capacitors, schottky diodes, PCB copper, wires, connectors, and some losses in the inductor test wires. The distribution between these is unknown, but most of the frequency-related difference is assumed to come from the FETs.

In the average test application (16.5 V to 12 V buck), the FET rise catches up with inductor rise at about 300 kHz and 8 A load. At 4 A, the sweet spot is at 400 kHz and at 2 A (and below) the optimum frequency has shifted to some 500 kHz. At loads greater than 8 A, the sweet spot will be at a decreasing frequency, while FET rise will continue to increase faster than inductor losses decrease. It is worth noticing that below 2 A, very little decrease in rise occurs, i.e. it is actually a baseline for running the system without load in forced continuous conduction mode. (In pulse-skipping mode, this minimum rise is lower.)

Bear in mind that this is based on an average of the various types and models of 27 inductors with slightly different properties. Even though there is a fair bit of uncertainty about the simulation tools' accuracy, I thought it likely that some types are comparatively better at lower frequencies and others at higher. The experiment demonstrates how FET losses depend on both load and switching frequency and that higher load causes a stronger frequency dependency.

The inductor temperature measurement experiment indicates a smaller difference between the various inductors than the simulations suggest, although the ferrite PQ and EI core inductors generate a smaller temperature rise than most of the pot core and composite types.

There is too great variation in the experiment results to draw firm conclusions about optimum switching frequency and inductance, but the simulation conclusion that a 2-3.6 μH inductor is the best choice for the 12 V buck/boost main rail seems to hold.

Some experiment results stand out:

- SER1412-152: This inductor has a very high temperature rise, not even close to the loss simulation results. Does the test sample have invisible damage or is the core to blame?
- XAL1580-202: It has higher temperature rise than both the -182 and the -302. Inductance measurement of the experiment sample showed a -182 no-load inductance of 1.99 μH (compared to 2.03 μH for the -202).
- SER201X: The Coilcraft PQ-ish models have a slightly higher temperature rise than the WE HCF2013 PQ, despite lower DCR. This could only be caused by core losses not accounted for by the simulation.
- SER1412-362: This inductor has a very low temperature rise, but it would be nice to have a “bigger” core, which would give a better balance between coil dimension (very low DCR) and saturation current.

5.9 Temperature Measurement when Gaming

Inductors	Ambient temperature			
	Idle	3.3 V	5 V	
HCI1365 3.7/4.7	24.5	13.5	15.5	
HCI1365 4.7/6.0	22	14	16	
XAL1010 4.7/5.6	23.5	15.5	16.5	
IHLP5050FD-01 3.3/4.7	22	10	20	20

Table 19: PSU temperature rise in degrees C when gaming

The PSU gaming temperature measurement suggests a greater temperature rise difference than in the big initial buck/boost measurement. The IHLP feels noticeably hotter to the touch.

Inductor	Top	Coil
XAL1580-302	43	
IHLP6767GZ-2R2-01	43	
SER2011-202	38	40

Table 20: Buck/boost 12 V main rail @ 16.5 V input and 7-9 A output when gaming

The simple gaming 12 V buck/boost test indicates a lower temperature rise in the PQ-ish core inductor than in the two composite core inductors.

5.10 Total Efficiency and Loss Measurements

5.10.1 UPS and Buck/Boost 12 V Rail, part 1

The following graphs are from the third experiment. All competing inductors were tested at 295 kHz, from which the loss comparison graph data is taken. Three inductors were additionally tested at 198 kHz, two of which were also tested at 392 kHz. Efficiency is greatest at 198 kHz:

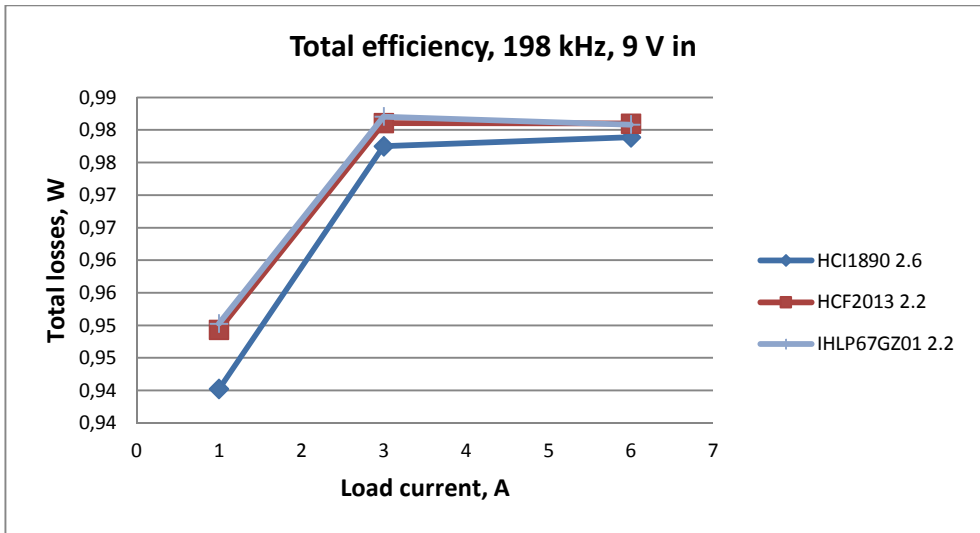


Figure 47: Efficiency @ 198 kHz, 9 V input

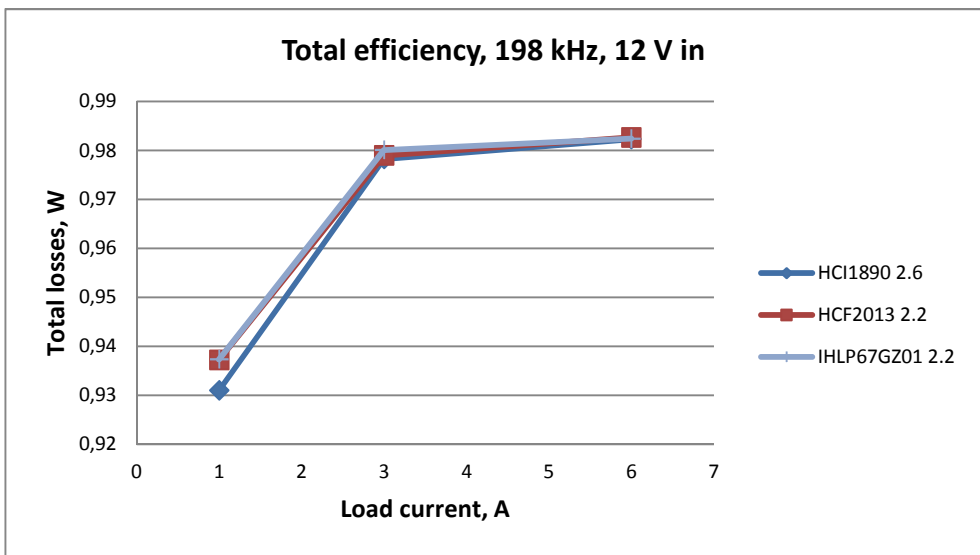


Figure 48: Efficiency @ 198 kHz, 12 V input

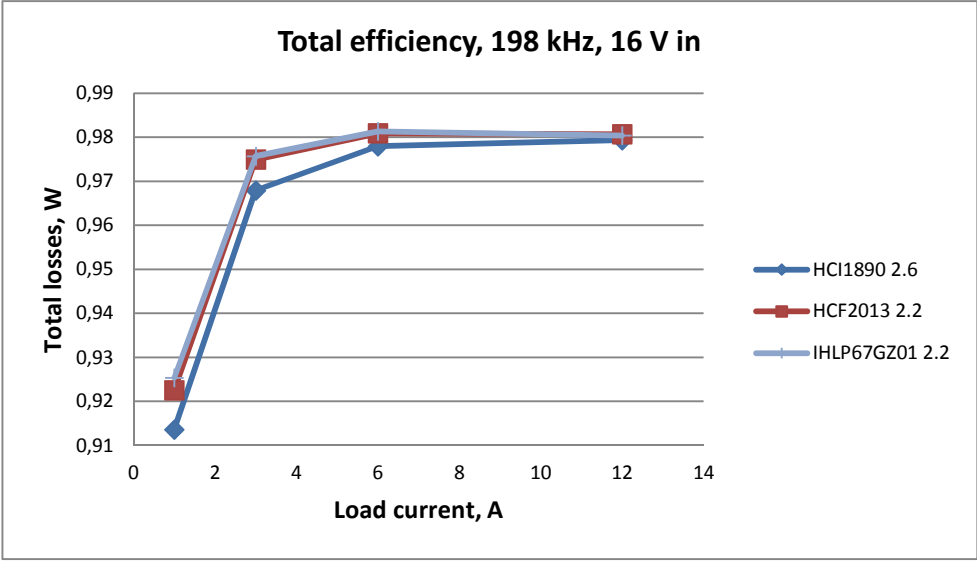


Figure 49: Efficiency @ 198 kHz, 16 V input

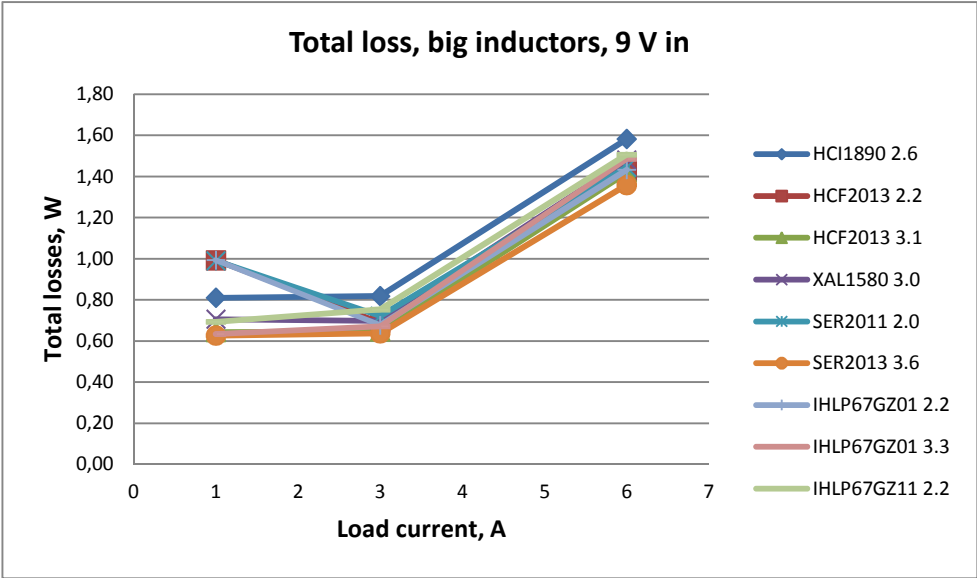


Figure 50: Total board losses @ 9 V input, 295 kHz

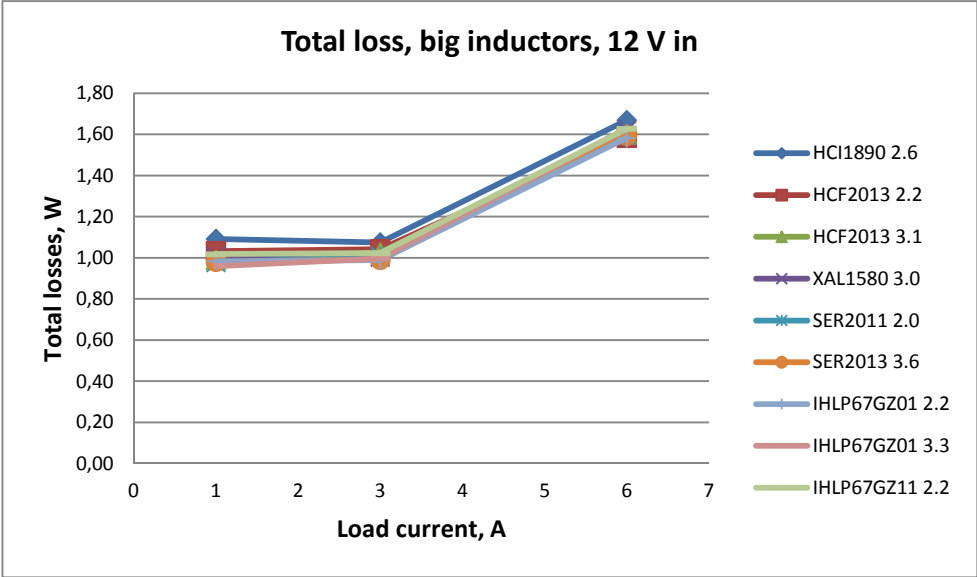


Figure 51: Total board losses @ 12 V input, 295 kHz

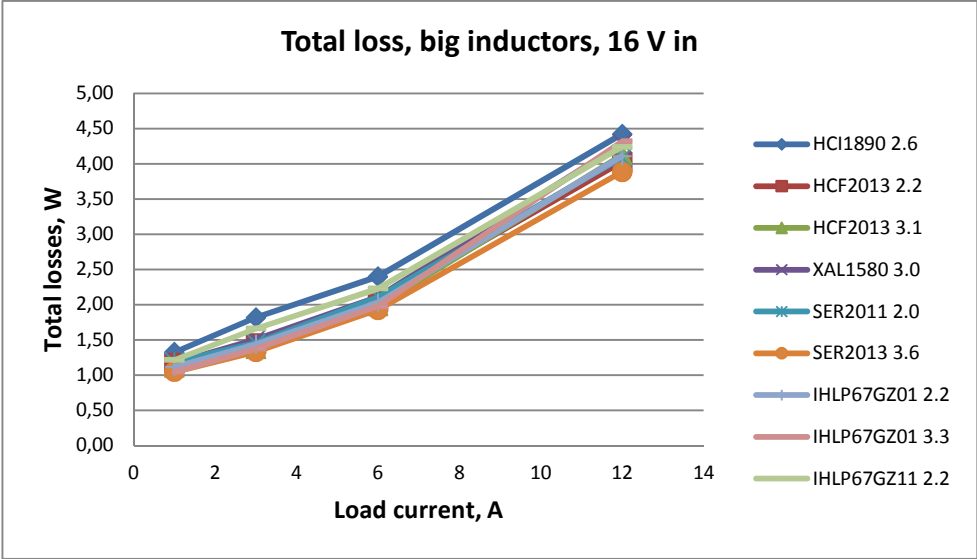


Figure 52: Total board losses @ 16 V input, 295 kHz

The loss graphs are a bit cluttered, so here is the data in tabular form:

	9 V			12 V			16 V			
	1 A	3 A	6 A	1 A	3 A	6 A	1 A	3 A	6 A	12 A
HCI1890 2.6	0,81	0,82	1,58	1,09	1,07	1,67	1,32	1,82	2,40	4,42
HCF2013 2.2	0,99	0,69	1,43	1,03	1,04	1,58	1,17	1,45	2,05	4,02
HCF2013 3.1	0,64	0,65	1,42	0,99	1,03	1,60	1,11	1,37	1,98	4,12
XAL1580 3.0	0,71	0,70	1,48	1,01	1,00	1,62	1,17	1,51	2,11	4,28
SER2011 2.0	0,99	0,72	1,44	0,98	1,01	1,60	1,19	1,45	2,11	4,08
SER2013 3.6	0,63	0,64	1,36	0,98	0,99	1,60	1,05	1,33	1,92	3,88
IHLP67GZ01 2.2	0,99	0,68	1,43	0,98	0,99	1,58	1,11	1,43	2,02	4,11
IHLP67GZ01 3.3	0,63	0,67	1,49	0,96	1,00	1,63	1,05	1,37	1,98	4,32
IHLP67GZ11 2.2	0,69	0,75	1,51	1,02	1,02	1,63	1,21	1,66	2,23	4,24

Table 21: Big inductor total losses @ 295 kHz

5.10.2 What Happened to the Sweet Spot?

The simulations and the temperature rise measurement suggest that there is a sweet spot, but there is no sign of it in the actual application in the frequency range of 198 to 392 kHz. Instead of entering a “valley”, the decrease accelerates from 295 to 198 kHz:

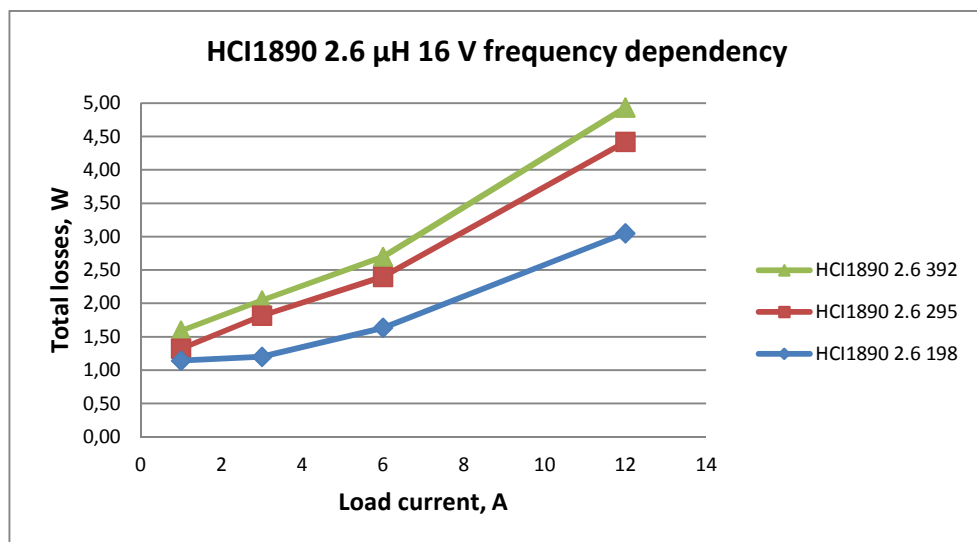


Figure 53: Total HCI losses vs. frequency. (HCF and IHLP losses show the same behavior.)

5.10.3 UPS and Buck/Boost 12 V Rail, part 2

For the third efficiency and loss measurement, I was expecting the sweet spot to be somewhere around 300 to 500 kHz depending on input voltage, inductance value, and load current. As it's not possible to decrease frequency, I had to resort to testing lower inductance values.

I needed the 20 V to 12 V @ 8 A @ 198 kHz actual loss data for the inductor loss simulator evaluation, which is why the fourth efficiency and loss measurement is done at a higher input voltage.

Between 1 and 2 A, there is an automatic transition from pulse-skipping to forced continuous mode.

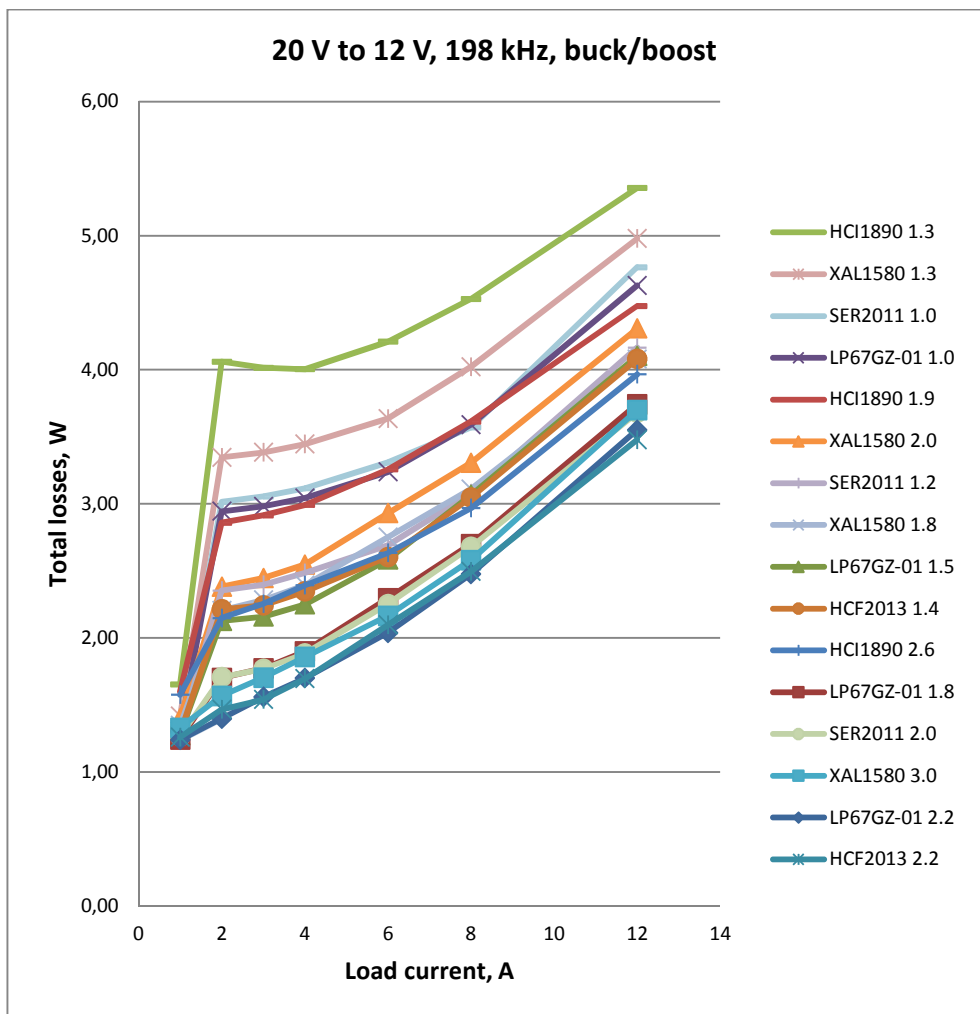


Figure 54: Total losses, 20 V to 12 V @ 198 kHz

	Load current, A						
	1	2	3	4	6	8	12
LP67GZ-01 2.2	1,24	1,40	1,56	1,70	2,04	2,48	3,55
LP67GZ-01 1.8	1,24	1,70	1,77	1,90	2,29	2,70	3,74
LP67GZ-01 1.5	1,27	2,13	2,16	2,25	2,58	3,07	4,10
LP67GZ-01 1.0	1,30	2,94	2,98	3,04	3,24	3,59	4,63
HCF2013 2.2	1,26	1,47	1,54	1,70	2,10	2,50	3,48
HCF2013 1.4	1,28	2,21	2,24	2,35	2,60	3,05	4,08
HCI1890 2.6	1,58	2,15	2,25	2,39	2,63	2,97	3,97
HCI1890 1.9	1,60	2,86	2,91	2,99	3,26	3,61	4,48
HCI1890 1.3	1,65	4,06	4,01	4,00	4,21	4,53	5,36
HCI1890 0.82	1,78	6,99	6,89	6,81	6,76	6,81	7,57
XAL1580 3.0	1,33	1,57	1,70	1,86	2,16	2,58	3,70
XAL1580 2.0	1,40	2,38	2,45	2,55	2,93	3,31	4,31
XAL1580 1.8	1,35	2,21	2,28	2,39	2,75	3,11	4,08
XAL1580 1.3	1,42	3,35	3,38	3,45	3,64	4,02	4,98
SER2011 2.0	1,26	1,71	1,77	1,88	2,25	2,68	3,68
SER2011 1.2	1,29	2,35	2,40	2,48	2,69	3,08	4,17
SER2011 1.0	1,32	3,01	3,05	3,12	3,31	3,57	4,76

Table 22: Total losses, W, 20 V to 12 V @ 198 kHz

5.10.4 Discussion of the BB 12 V Rail Loss Results

It is nice to see that, from an efficiency and loss perspective, one UPS design will cover all computer segments at > 90 % efficiency. A “smaller” UPS model would only add the benefits of smaller size and lower cost.

There is no real need for dual phase. The single-phase buck/boost 12 V rail handles all use cases at a modest temperature rise.

The third measurement showed that 16 V to 12 V @ 295 kHz benefits from an inductance value of about 2 to 3.6 μH . In the fourth measurement, converting 20 V to 12 V @ 198 kHz, it is clear that core losses increase dramatically with inductance values below some 2 μH . It is far better to “play safe” and choose a slightly larger inductance than risk finding yourself on the steep “left” slope of the U-shaped total loss curve.

These results also mercilessly demonstrate weaknesses of some inductor types and models. As we’ve already seen, the WE-PERM2 HCI1890 series has significantly higher losses. The exceptionally low DCR can’t make up for its sky-rocketing core losses. (See the HCI 0.82 μH in Table 22.) The

2.6 μH HCI competes with the 1.4 μH HCF and the 1.8 μH IHLP6767GZ-01, both of which operate with much greater ripple currents.

In the temperature rise measurement, the XAL1580-202 mysteriously performed worse than its 1.8 μH and 3.0 μH neighbors. This result is confirmed here. At first I considered the possibility of Coilcraft changing to a worse (still undisclosed) core material, but then I noticed a similar phenomenon in the core loss simulation of Vishay IHLP4040DZ-01 3.3 μH . According to the web tool, the 3.3 μH has much higher losses than both 2.2 μH and 4.7 μH . I will return to this in 5.15 Sour Spot.

5.10.5 Crowning the Winners

The SER2013 3.6 μH consistently performs very well in the third measurement, but it saturates too early to be usable in the 20 A buck/boost circuit. With a bigger core, it would have been the clear winner.

The XAL1580 3.0 μH performance is similar to the IHLP6767GZ-01 3.3 μH , but unfortunately none of the other XL1580s are an alternative. Their performance is too close to the HCI1890's.

Of the inductors participating in this test, the best practical choices are:

- IHLP6767GZ-01 2.2 μH
- HCF2013 2.2 μH
- HCF2013 3.1 μH
- SER2011 2.0 μH (but a higher-saturating SER2013 - SER2014 should probably be used instead)

Three of these are MnZn ferrites with sharp saturation that is fairly temperature dependent. Before going into production, this must be thoroughly tested. The IHLP composite core (and possibly the XAL1580 3.0 μH) might be safer choices. The awkward placement of the XAL solder terminals makes me hesitant to use them, but maybe that wouldn't be a problem in factory production.

5.10.6 Efficiency and Losses in the PSU 3.3 and 5.0 V Rails

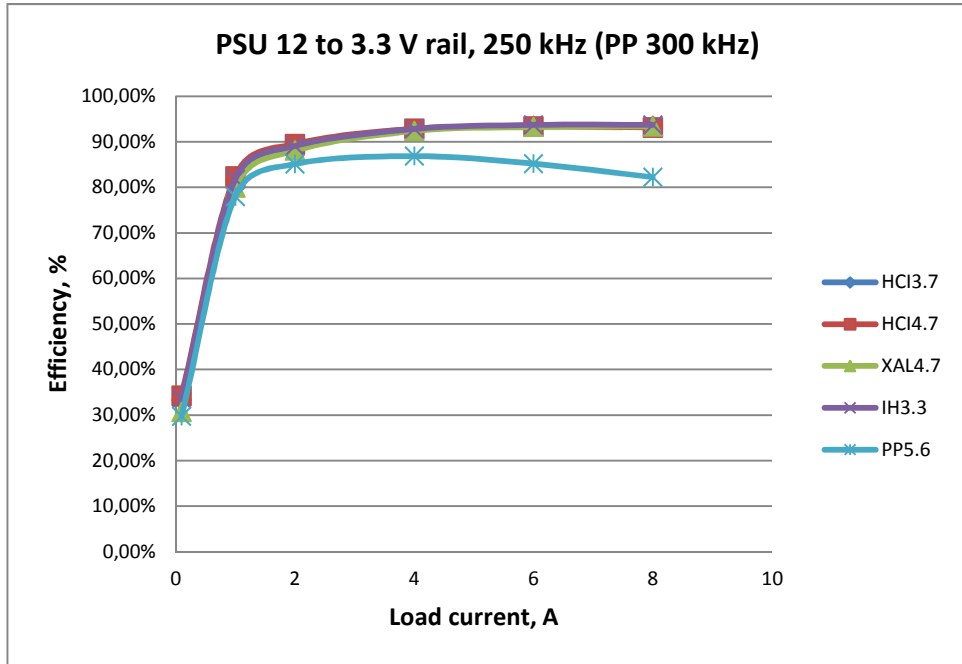


Figure 55: Efficiency of the PSU 3.3 V rail

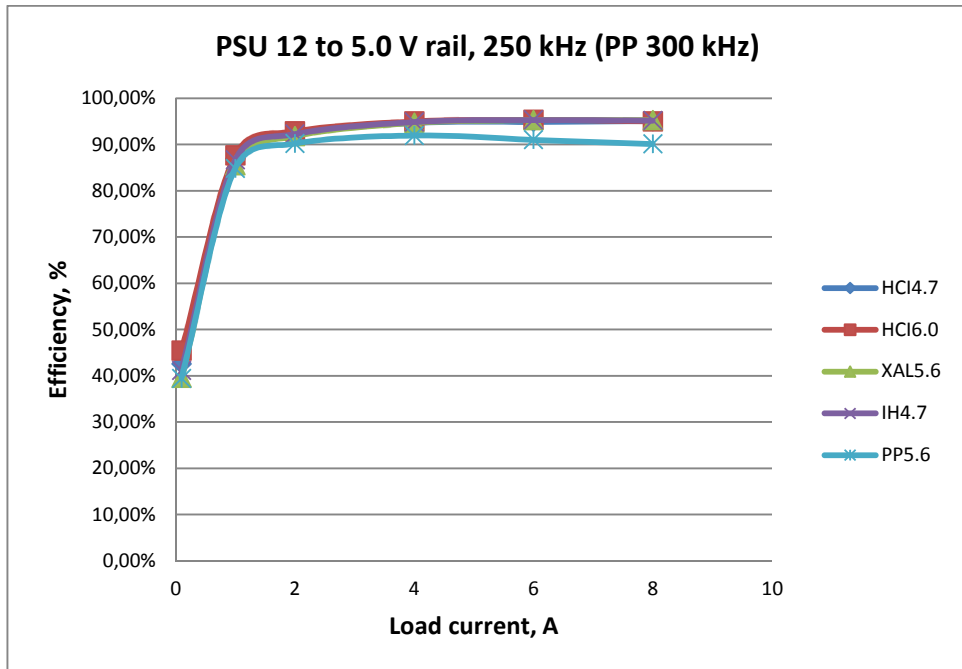


Figure 56: Efficiency of the PSU 5.0 V rail

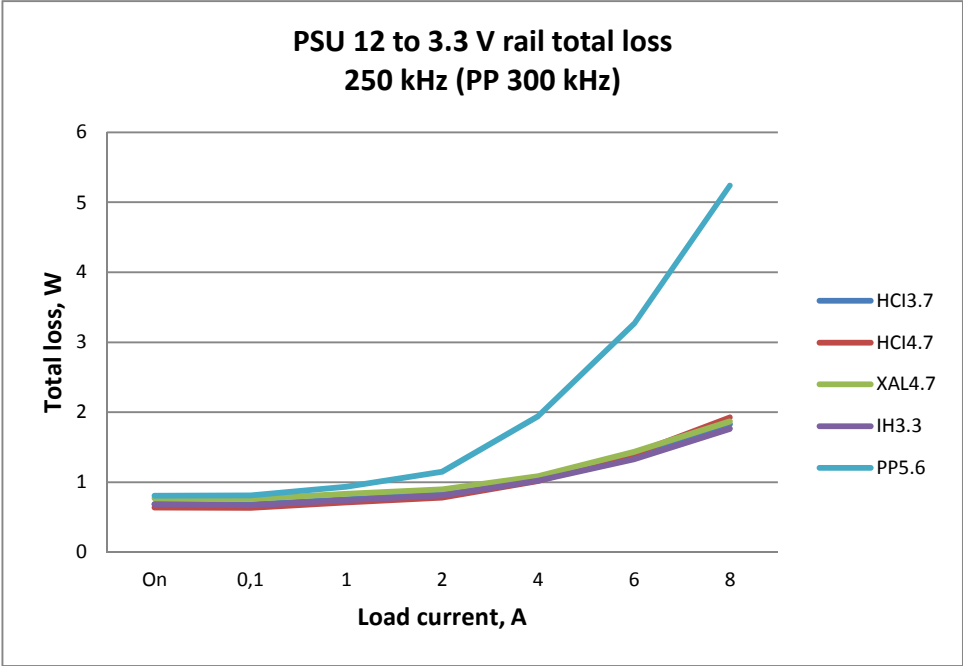


Figure 57: Total 3.3 V rail loss, including no load

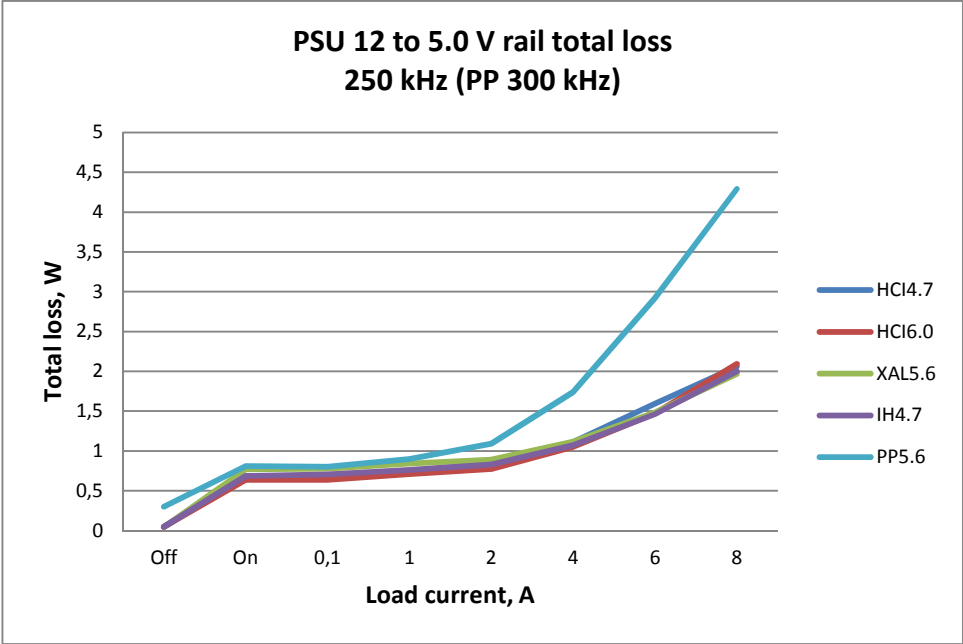


Figure 58: Total 5.0 V rail loss, including off state and no load

Let's add the losses from both rails and zoom in:

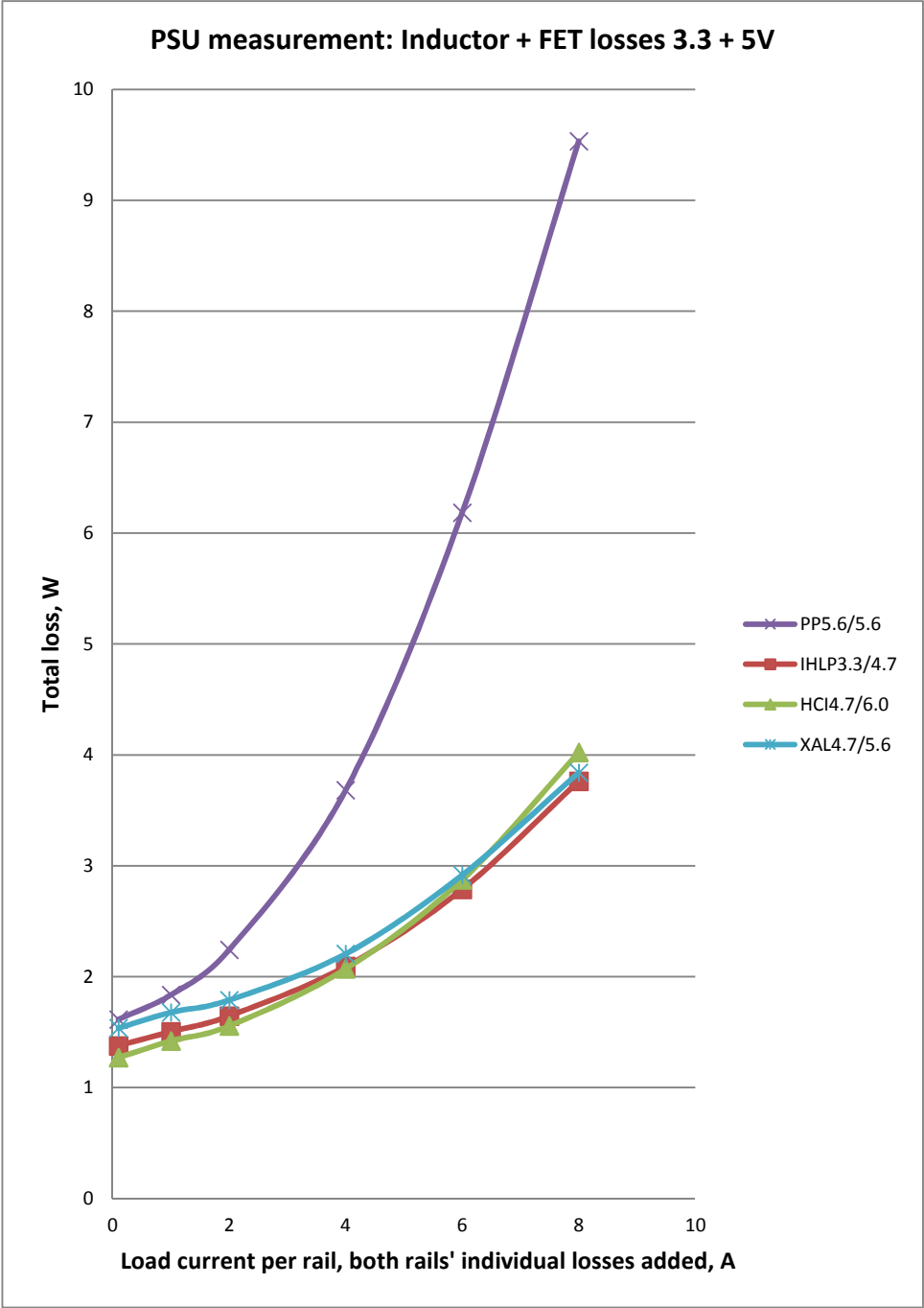


Figure 59: PSU measurement, both rails' individual losses added

I was anticipating significantly lower losses than the picoPSU, but this is a much greater difference than I could have hoped for. What is causing it?

5.10.7 Discussion of the PSU Efficiency Measurement Results

Comparing the results from the simulation to the actual losses, we see that the relative positioning doesn't hold true. Please note that I don't have access to equipment to test which simulation is the most accurate, but relatively speaking the Vishay IHLP inductor simulator over-estimates losses, while the Coilcraft XAL simulator under-estimates losses:

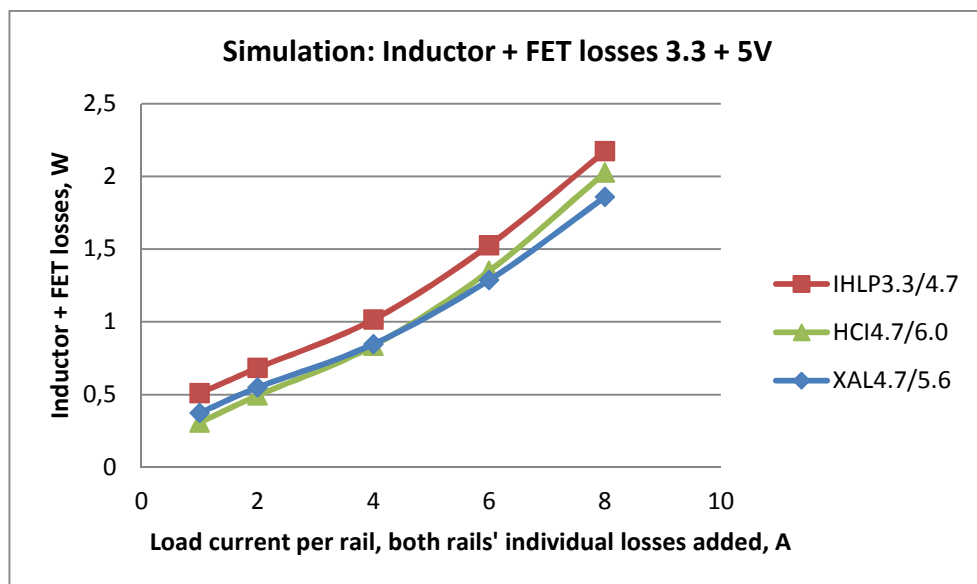


Figure 60: PSU simulation, both rails' individual losses added, RED EXPERT HCI

In both the temperature rise experiment and the gaming temperature rise measurement, the IHLP MODPSU was noticeably hotter, but it is in fact one of the most efficient, with losses similar to the HCI 3.7/4.7 combo.

The XAL low-load losses surprise me. I had expected a curve slope similar to the HCI combo as the inductance values are so similar. Instead it looks like a worse core material being saved by a lower DCR.

The WE-PERM HCI1365 is more successful than the WE-PERM2 HCI1890. Could it be that the ripple current is so low that the HCI1365 has much more agreeable living conditions, or is WE-PERM a "better" core material than WE-PERM2?

Inductor	DCR	
	Inductance	typ., mΩ
IHLP5050FD-01	3.3	5.7
IHLP5050FD-01	4.7	8.0
HCI 7443551470	4.7	7.0
HCI 7443551600	6.0	8.4
XAL1010	4.7	5.2
XAL1010	5.6	6.3

Table 23: PSU inductor inductance and DCR

Either way, it is clear that inductor DCR says little about actual performance. The specified XAL1010-562 DCR is only $6.3 / 8.4 = 75\%$ of the HCI 744355160 DCR (93% of the inductance), but the XAL combo doesn't win over the HCI until above 6 A.

The good thing is that performance is so similar that you don't need to worry about being trapped with only one source. Price and PCB layout compatibility are the main differentiators.

5 V rail efficiency is higher than 3.3 V efficiency. I was hoping for a better result between 1 and 2 A, especially for the 3.3 V rail, but maybe that could be remedied by a lower-rated PSU variant.

Let's take a closer look at losses:

Per rail	Efficiency & loss		Difference, fraction
	Simulation	measurement	
1 A	0.4 W	1.7 W	23.5%
8 A	2.0 W	3.8 W	52.6%

Table 24: Total PSU loss comparison, sum of both rails

At first glance this looks like a big difference, but the simulations only include inductor and FET losses and there are many other losses in the real board. Making a rough estimate of the additional losses at 8 + 8 A and 1 + 1 A, the simulation is not that bad at the higher load:

		8 + 8 A		1 + 1 A	
	R, Ω	I Loss, W		I Loss, W	
Cin		0.020		0.020	
Switch controller LDO		0.048		0.048	
Control FET driving 3.3 V		0.011		0.011	
Sync FET driving 3.3 V		0.024		0.024	
Control FET driving 5 V		0.011		0.011	
Sync FET driving 5 V		0.024		0.024	
Fuse	0.002	5.533	0.061	0.692	0.001
Output connector 3.3	0.010	8.000	0.640	1.000	0.010
Output connector 5	0.010	8.000	0.640	1.000	0.010
Cout 3.3 V	0.009	?		?	
Cout 5 V	0.009	?		?	
PCB		?		?	
Sum of additional losses		1.479		0.159	
Simulated losses		2.000		0.400	
Total losses		3.479		0.559	
Measured total losses		3.800		1.700	

Table 25: Additional PSU losses @ 8 + 8 A vs. 1 + 1 A. (Loss data for Cin through Sync FET driving 5 V are taken from LTpowerCAD II IHL5050 design.)

The sum of the simulated and estimated high-current losses is fairly close to the measured losses but the low-current losses are a different story. Note that I have just copied the 8 + 8 A losses for Cin through Sync FET driving 5 V, but they should be similar and certainly not bigger at 1 + 1 A. 0.559 W is far from the measured 1.7 W.

5.10.7.1 Benchmarking against the picoPSU

The contending picoPSU has two LM2642 switch controllers, with a total of 3 rails (including the buck 12 V rail that is permanently on when input is 12 V). This doesn't affect the "off" losses, where we see the benefit of LTC3850's automatic switch-over to the energy-efficient burst mode.

It would be interesting to know why the picoPSU is so much worse. According to the FET loss simulation in 3.1.1, only some 1.62 W of the 5.7 W difference between the MODPSUs and the picoPSU could be explained by FET losses at the same frequency. The additional FET switching losses due to the picoPSU running at 300 kHz (compared to the MODPSUs' 250 kHz) should not be this high.

I included the picoPSU inductor in the third efficiency and loss measurement, wanting to know if it is perhaps a cheap low-quality component. Is the picoPSU using a second-rate inductor?

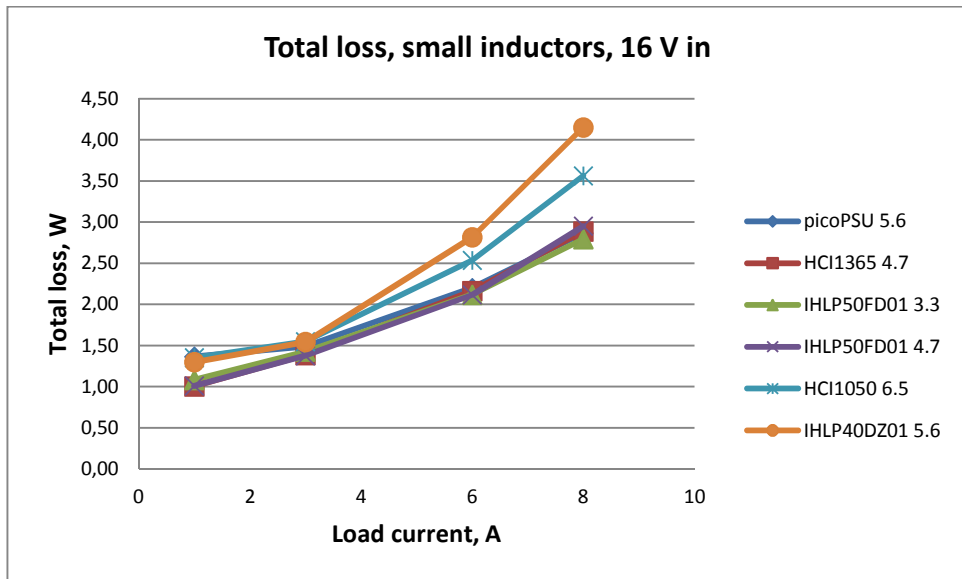


Figure 61: Comparison of the PSU (small) inductors

The answer is a clear “no”. The picoPSU inductor’s performance is indistinguishable from the MODPSU inductors with the same PCB footprint area. The picoPSU capacitors are fine polymer types, so we probably need to look for other explanations.

Mats Hellberg and Thomas Ginell (73) suggest shoot-through, too long dead-time period, weak gate driver, or excessive gate capacitance as potential switch controller and FET reasons. Apparently shoot-through was a common problem in early DC/DC switch designs.

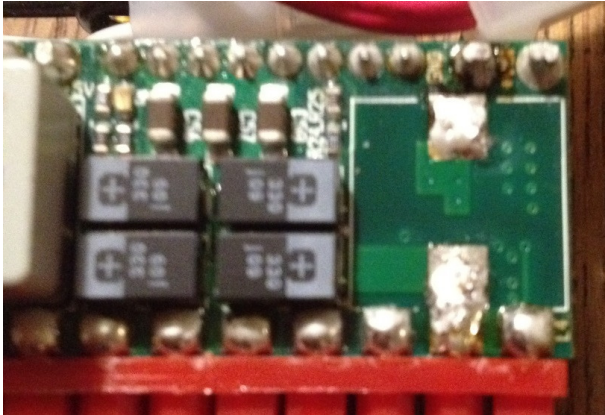


Figure 62: picoPSU PCB layout beneath the inductor

Judging by the above photo, PCB layout (many layer changes, thin copper, narrow traces, and few tiny vias) is another possible cause.

5.11 Effect of External Freewheeling Diode

The BSC010NE2LSI (21) datasheet in tabular form states a typical V_F of 0.56 V @ 12 A @ 25 °C and a reverse recovery charge of 5 nC. At a first glance this looks like a sufficiently high V_F to make it worth trying to “replace” it with an external freewheeling diode. The first version of the UPS and buck/boost boards are thus equipped with B340LA (74) diodes. With a typical forward voltage drop (V_F) of 0.31 V @ 1 A @ 25 °C and a total capacitance (C_T) of 180 pF they are an improvement over the B240A that is suggested in the datasheet of the LTC3789 (63) switch controller. However, at a closer look the BSC010NE2LSI datasheet also has a V_F graph that reads 0.4 V @ 1 A @ 25 °C.

The following graphs show the actual losses, measured in the second round @ 375 kHz. It is hard to say if all differences are due to measurement errors, but it does seem like modern FET transistors have such a good body diode that the benefit of adding an external freewheeling diode is minuscule at best:

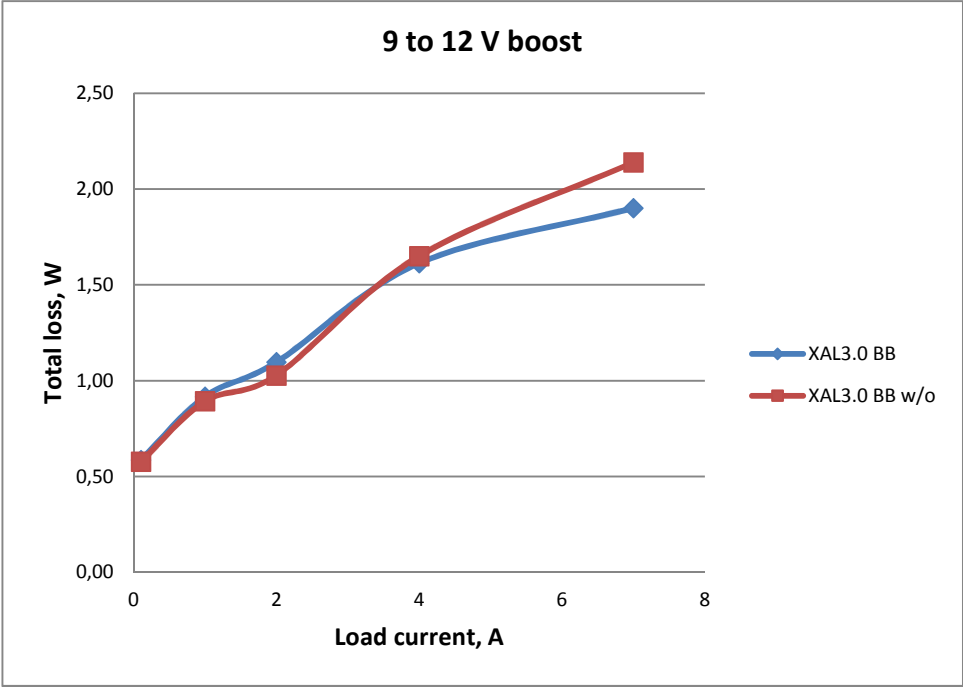


Figure 63: Freewheeling diode effect, 9 to 12 V boost

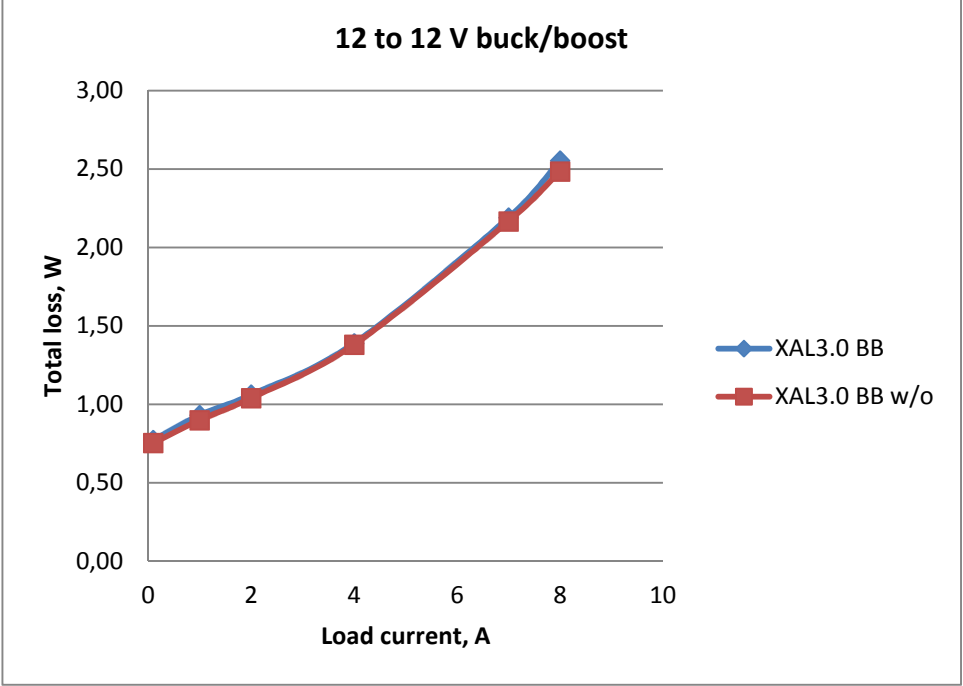


Figure 64: Freewheeling diode effect, 12 to 12 V buck/boost

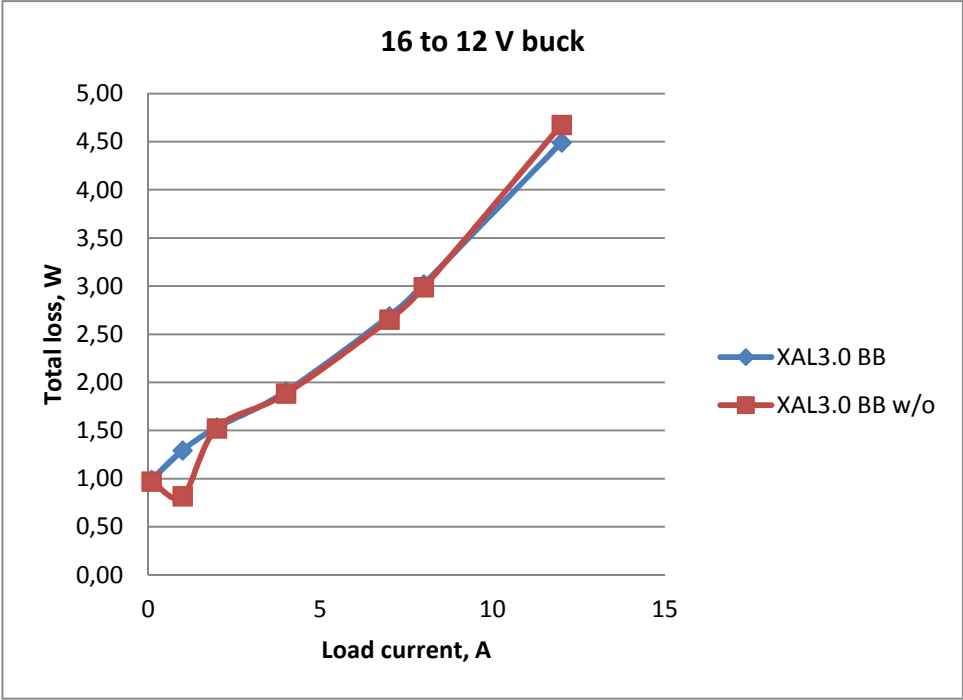


Figure 65: Freewheeling diode effect, 16 to 12 V buck

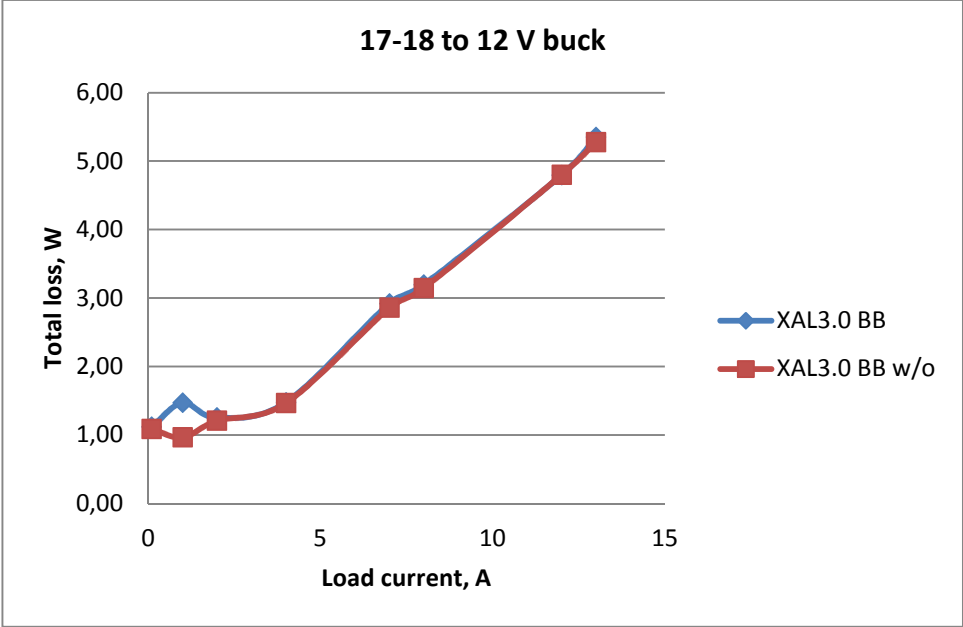


Figure 66: Freewheeling diode effect, 17-18 to 12 V buck

5.12 Correlation between DCR and Total Losses

I have already touched on the subject in the PSU result discussion and the following buck/boost graph completes the picture. The correlation between DCR and total losses is very weak:

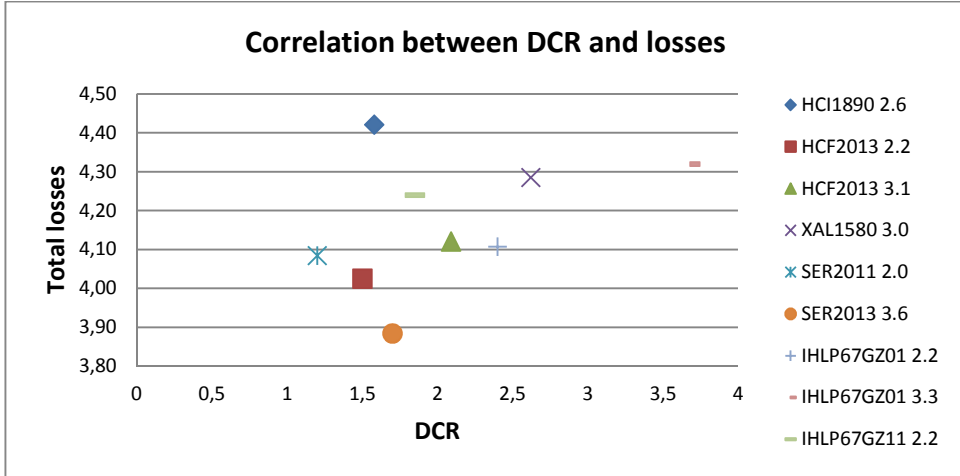


Figure 67: Correlation between DCR and total losses, 16 to 12 V @ 12 A @ 295 kHz

5.13 Inductor Losses vs. Physical Size

A smaller inductor typically has greater DCR than a larger one, but it also has a shorter magnetic path length and a smaller cross-section area. What does this amount to in terms of losses?

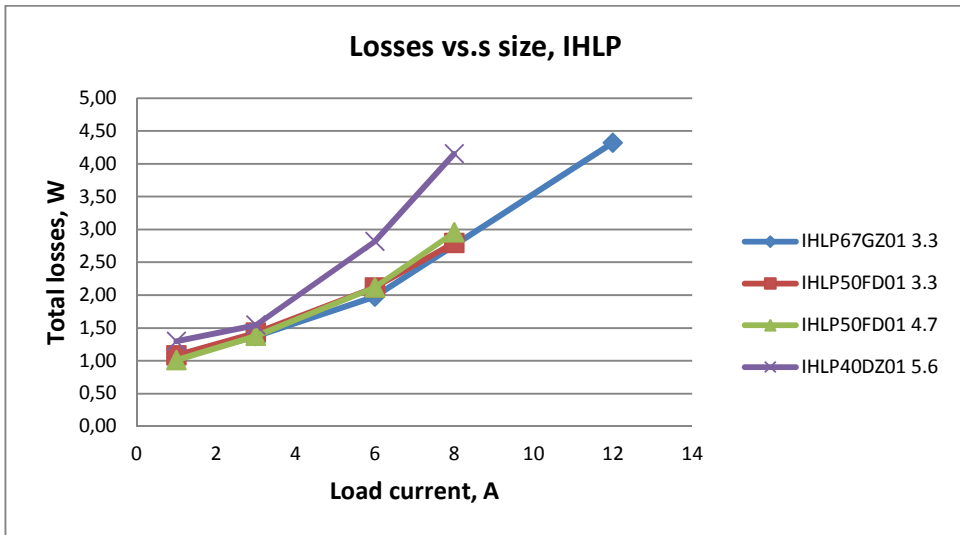


Figure 68: IHLP losses vs. size

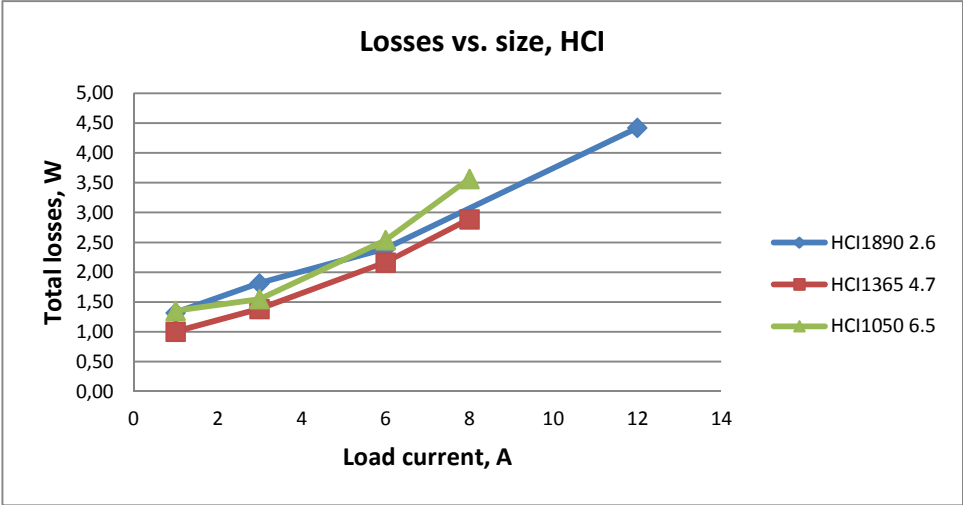


Figure 69: HCI losses vs. size

The selection is too small for a firm conclusion, but my interpretation is that you should think twice before using a “bigger” inductor than your application really needs.

	DCR, mΩ	Saturation current, A	Core base, cm ²	Total volume, cm ³
IHLP6767GZ-01 3.3 μH	3.68	54	2.94	2.06
IHLP5050FD-01 3.3 μH	5.70	35	1.66	1.08
IHLP5050FD-01 4.7 μH	8.00	32	1.66	1.08
IHLP4040DZ-01 5.6 μH	17.60	16	1.06	0.42
HCI1890 2.6 μH	1.58	50	3.33	2.96
HCI1365 4.7 μH	7.00	15	1.64	1.06
HCI1050 6.5 μH	12.50	10	1.07	0.52

Table 26: Inductor DCR

I assume that the loss increase in the smallest two inductors is due to the much higher DCR. Please note that the usable range for the smallest two inductors is up to some 5 - 6 A (before the temperature gets too high). Considering their small physical size, they keep up amazingly well.

5.14 Single-Phase vs. Dual-Phase Operation

At what point does the single-phase circuit's loss exceed that of the dual-phase?

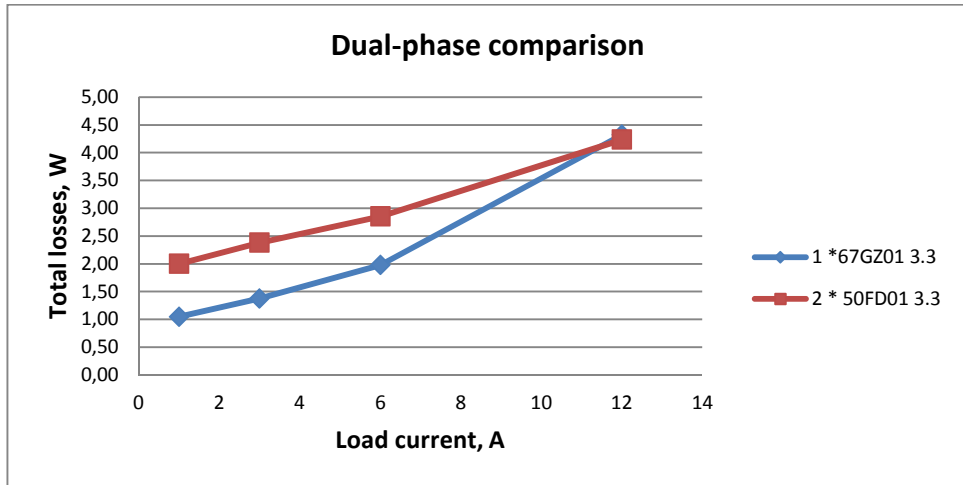


Figure 70: Single-phase vs. dual-phase losses in 16 to 12 V buck circuit

For the 16 to 12 V conversion using a four-switch synchronous switch circuit, break-even is at 12 A load current. The file server I have designed for almost never exceeds this. The gaming PC peaks at 16.7 A, with an average active load around the 12 A break-even. In this range, dual-phase is just a waste of money, energy, and PCB real estate.

For dual-phase to become interesting, we need a higher average load current and/or the ability to disable one phase at low loads.

It's worth noticing that Mini-Box' most powerful dual-phase buck/boost board DCDC-USB-200 (75) has a maximum continuous rating of 12 A (15 A peak). Please see 3.1.1 for a FET loss simulation where the Mini-Box FETs are found to have five times as high single-phase losses as the MODPSU FETs at this current. Add to that the completely unnecessary losses from the second phase and you have a great need for cooling.

5.15 Sour Spot

The Coilcraft XAL1580 2.0 μH has much greater temperature rise and measured losses than its 1.8 μH and 3.0 μH neighbors (Figure 54). This also seems to apply to Vishay IHLP4040DZ-01 3.3 μH :

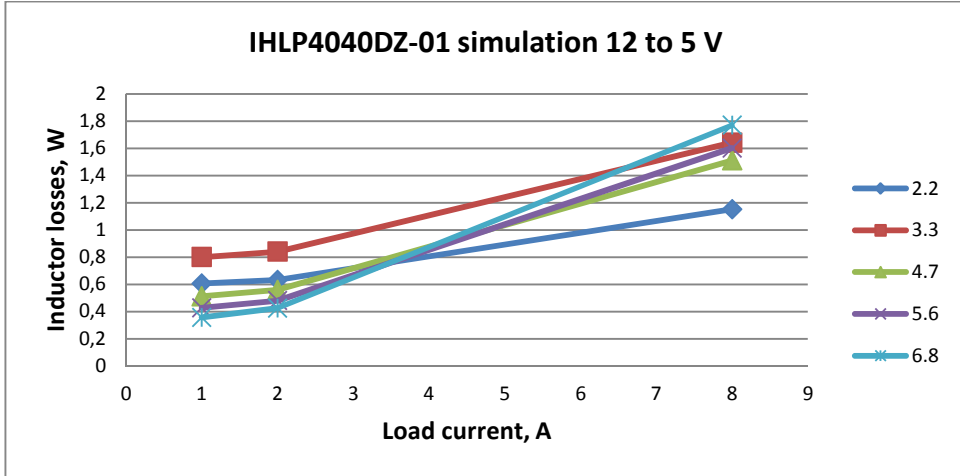


Figure 71: IHLP4040DZ-01 simulation 12 to 5 V

The Vishay IHLP selection application note (41) shows deviating properties for the 3.3 μH model. Apparently some inductance values (the number of winding turns and wire cross-section area that fit in a specific physical size) are more fortunate while others are less so.

Unfortunately, the Coilcraft loss calculator fails to recognize it:

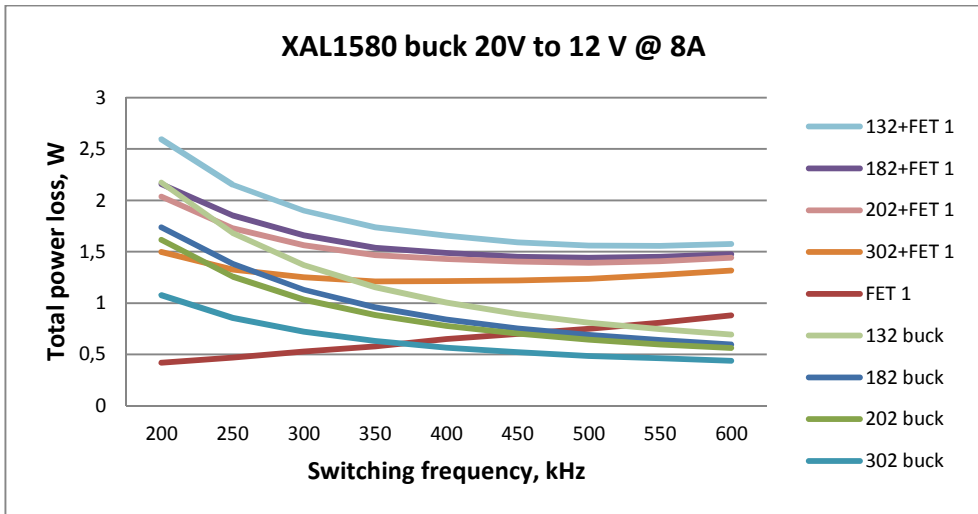


Figure 72: XAL1580 simulation 20 to 12 V

5.16 Accuracy of Inductor Loss Calculators, pt. 2

There is a much greater difference between the manufacturers' core loss calculators than between their products' actual performance:

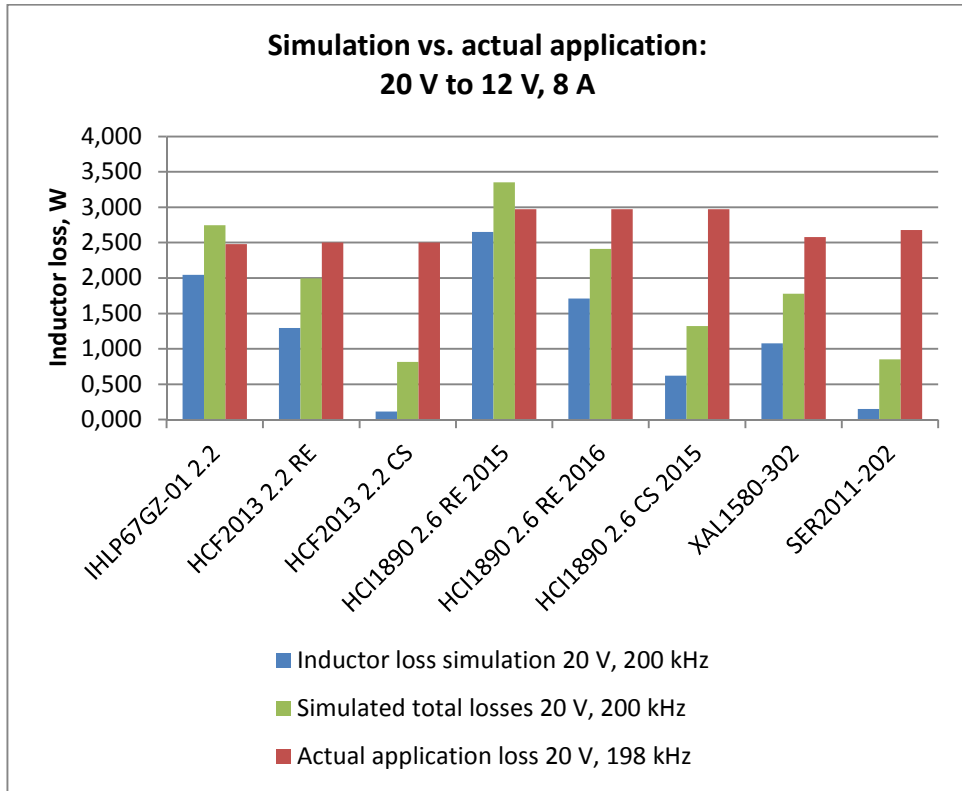


Figure 73: Example of inductor loss simulation results vs. actual application loss measurements

An LT3791-1 simulation with a 2.2 μH inductor using one BSC024NE2LS and three BSC010NE2LSI from 20 to 12 V @ 8 A @ 200 kHz estimates FET losses to $0.33 + 0.08 + 0.03 + 0.07 \text{ W} = 0.51 \text{ W}$. The major remaining losses are in the 3 m Ω output shunt resistor (0.192 W) and the bottom 1.67 m Ω sense resistor. In the above graph, 0.7 W has been added to the simulated inductor losses to get data for a rough comparison.

	IHLP67	HCF	HCF	HCI	HCI	HCI		
20V to 12V 8A, 200 kHz	GZ-01	2013	2013	1890	1890	1890	XAL1580-	SER2011-
	2.2	2.2 RE	2.2 CS	2.6 RE	2.6 RE	2.6 CS	302	202
DCR loss	0.177	0.096	0.111	0.101	0.101	0.112	0.168	0.077
Core loss	1.106						0.907	0.060
AC winding loss	0.761						0.002	0.012
AC losses		1.200	0.003	2.550	1.610	0.510		
Total loss	2.044	1.296	0.114	2.651	1.711	0.622	1.077	0.149

Table 27: Loss simulation distribution for Figure 73

This is disturbing. As of today ¹⁹, I have made three runs with Würth Elektronik’s tools that present different results for the same inductor and operating parameters (HCI1890 2.6 μ H). The first one was Component Selector (CS) in mid-summer 2015, then RED EXPERT (RE) in September 2015 and finally RE again 2016-02-04. For some reason, the HCI simulation results have changed but not the HCF ones.

In September 2015, Coilcraft engineering informed me that they were planning to update their tool shortly (72), but nothing has happened yet (2016-05-09).

In this study, the Vishay web tool is consistently the least optimistic, yet the Vishay products are in the lead in all cases except for the really small-size inductor. Coincidentally, Vishay also publishes core material specifications.

For future simulations I will run the Vishay tool for a similar size and inductance value and use this result as a starting point, regardless of brand.

5.17 Switch Controller Design Tool Recommendations

The optimum inductance value is a trade-off between low- and high-load efficiency and also input voltage, so there is not one best choice. For a buck/boost circuit, the higher inductor current in the boost region makes DCR more important than in buck operation, so you must also decide on which input voltage range you should optimize for. This is also a trade-off between conduction losses in boost and switching losses in buck (or vice versa).

¹⁹ 2016-02-04

If you enter 11-14 V input and 5 V @ 10 A + 3.3 V @ 8 A output for LTC3869-2 into LTpowerCAD II v2, it suggests a switching frequency of 460 kHz and a 1.5 μH inductor. All my measurements indicate that this frequency will cause large unnecessary losses.

At 250 kHz it recommends 3 μH for 10 + 8 A, about 6 μH for 5 + 4 A, and roughly 12 μH for 2.5 + 2 A. All of these are good recommendations for each individual case, but what is the “best” compromise? Figure 59 shows that the pivot point is at 4 A. This is where the loss lines of the 3.3 + 4.7 and 4.7 + 6.0 μH combinations intersect. In this case, the average load will be at 2 to 4 A per rail, so 4.7 to 5.6 μH would be a good trade-off.

The same tool suggests 409 kHz and 1.03 μH for 9 to 20 V input and 12.1 V @ 20 A output for LTC3789. Figure 53 tells us that this would lead to more than 60-70 % higher losses than 200 kHz. At this lower frequency the recommended inductance value shifts to 2.12 μH , which is spot on.

The Excel tool for LT3790 starts at minimum frequency, 200 kHz. I don't know if this is an intentional recommendation or just the initial value. For this frequency it recommends 1.33 μH . The fourth efficiency and loss measurement (Figure 54) tells us that this is about half of the optimum inductance value and that it could give you as much as 172 % more than the minimum losses at 2 A and 54 % more at 12 A.

To summarize, from an efficiency-maximizing perspective, LTpowerCAD II v2 recommends a too high frequency. (This is by the way also my previous experience of Texas Instrument's WEBENCH for LM3150MH.) When you yourself set the frequency, LTpowerCAD II v2 gives good recommendations in the above examples, provided that you know how to properly interpret them. The Excel tool suggests a too low inductance value.

Now, there are other benefits from using a higher frequency and lower inductance value; you can sometimes choose a physically smaller inductor. So long as you stay in the optimal frequency range for your capacitor, a higher frequency (alone) means you get lower ripple and hence can use fewer, smaller, or cheaper capacitors. A higher frequency means a faster response to load changes, which must otherwise be handled by a greater total bulk capacitance. However, great bulk capacitance means more smoke in case of a short circuit.

CHAPTER 6

6 Conclusions

There are many aspects to this work on SMPS efficiency maximization, some of which I have touched on only lightly and others just as far as what was necessary to optimize my particular designs. For these reasons it is not possible to state any finding as an absolute and universal fact. I do however think that the experiments shed quite a lot of light on a number of practically relevant topics, so that the readers will have a much better “entry assumption” for their own applications. Designers using off-the-shelf inductors should find my comparisons useful for their own component and operating point decisions.

Bear in mind that higher losses are not a problem in every application. Sometimes a low purchase price can make a higher-loss inductor an attractive choice.

After I had completed this work, I came into proper contact with Vishay and learned that the “core material of the IHLP is powdered iron”. (76) I had been expecting greater variety in terms of core material among the selection of off-the-shelf inductors:

- Academia and text books are very interested in more exotic materials than iron powder and ferrite.
- Würth Elektronik has invented their own names such as WE-PERM, WE-PERM2, and Superflux.
- The IHLP6767GZ-01 performs noticeably better than the other iron powder inductors.

In the end it is highly likely that all contending inductors in this comparison are either iron powder or Mn-Zn ferrite.

6.1 Inductor and Inductance Selection

Investigate the relationship between core material, core shape, core size, inductance value, winding DCR, switching frequency, and load current for a comprehensive selection of generally available power inductors.

A few topics stand out:

- **Core loss-related qualities:** On average, the Mn-Zn ferrite inductors have lower losses than iron powder ones. However, this is not clear cut and even among iron powder inductors it is perfectly clear that there are “better” and “worse”. As only Vishay publishes core parameters (41) (42), it is impossible to say how much depends on differences in permeability, composite vs. pot core, and other factors that might come down to build or material “quality”. To some extent a very low DCR can make up for the higher core losses at higher loads. In Table 21 (16 to 12 V @ 1 A @ 295 kHz) we see that HCI1890 2.6 μH (iron powder) has 12.8 % higher total losses than HCF2013 2.2 μH (ferrite). They are 18.9 % higher than IHLP6767GZ-01 2.2 μH (iron powder). At 8 A the difference is 10.0 % and 7.5 % respectively.
- **The left slope of the X-shaped total loss curve:** Increasing ripple currents mercilessly reveal the AC loss-related qualities of the core material when the next few lower inductance values are tried below the optimal value. Table 22 shows that picking a too low inductance value can be just as bad as choosing a poor inductor type. If in doubt, it is safer to choose the next higher inductance value.
- **Optimal switching frequency (desperately seeking sweet spot):** The temperature rise experiment demonstrates the X shape of decreasing inductor losses and increasing FET losses with frequency, but the 12 V buck/boost sweet spot (if it exists) is obviously at a lower frequency than the simulations and temperature rise experiment indicate.

It should be noted that the sweet spot is per inductor and inductance value. Over all inductance values, it seems that FET losses increase faster than inductor losses decrease with frequency, at least for the currents I have been testing. For some reason my BB losses rise much faster between 198 and 295 kHz than between 295 and 392 kHz. I have not had the time to try to figure out why.

Some factors are far less important than you might expect:

- **DCR:** The DCR of an inductor says little about its total losses. Except for the PQ-ish ferrites, it actually seems that low rated DCR correlates to high actual AC losses for off-the-shelf inductors, which effectively means that the optimum inductance value is higher for poor-core inductors. For the 12 V buck/boost application it equates to the next higher value than what would have been optimal for a low-loss core (2.6 μH vs. 1.9 μH for the HCl1890 and 3.0 μH vs. 2.0 μH for the XAL1580). The PQ-ish ferrites and the IHLP6767GZ-01 are optimal at 2.0 or 2.2 μH inductance.
- **A bigger size doesn't automatically mean lower losses:** The experiments have told us that, within the same or similar core types, the evaluated inductors have fairly similar performance regardless of core size and DCR, at least in the applications that were tested (which represent very common use cases). The main difference is that smaller cores saturate and heat faster (and the lower DCR of a bigger type might result in a higher optimal inductance value).

Not really addressed in this work:

- **Core shape:** Among off-the-shelf inductors for this purpose there are practically only two types – PQ-ish Mn-Zn ferrite and molded or pot core iron powder. There is thus very little ground for an analysis of the core shape's effect on losses. It seems that the PQ-ish ferrite has slightly better heat dissipation but also worse EMI qualities due to its discreet air gap.

Please see Swihart's document on core shape and material for a few application examples comparing toroid and E shape in MPP, High Flux, and Kool M μ (Sendust). (34)

- **Temperature dependency:** This evaluation has disregarded the temperature dependency of core saturation as that would have made efficiency measurements much more time-consuming. Furthermore, I assume that this can be verified in the pre-production tests. Ferrite core saturation is quite temperature dependent, so it definitely is an important factor due to ferrite's sharp saturation. The PQ-ish ferrites perform slightly better than the majority, but less so than expected. In the temperature rise measurements they have shown lower heating, which I assume is due to the partly exposed copper winding.

Beware of sour spots:

- Some inductance values (combinations of winding turns and wire cross-section area that fit in a specific physical size) are more fortunate than others. We have seen how XAL1580 2.0 μH measurements and IHLP4040DZ-01 3.3 μH simulation suffer from much greater losses than their next lower and next higher inductance value neighbors.

The Vishay product specifications confirm this deviation, but unfortunately Coilcraft's core loss calculator misses it completely. This means that you absolutely must verify your inductor candidates in real tests or risk finding yourself in a sour spot.

6.2 Switch Controller Design Tool Recommendations

Recommendations for inductance value and switching frequency given by DC/DC switch circuit design tools

From an efficiency-maximizing perspective, LTpowerCAD II v2 recommends a too high frequency. When you yourself set the frequency, it gives good recommendations in the tested applications, provided that you know how to properly interpret them. The Excel tool suggests a too low inductance value for the MODPSU buck/boost board.

6.3 Accuracy of Inductor Loss Calculators

Vishay consistently is the least optimistic. Their tool has given no reason to mistrust it and overall gives an impression of a serious intent to provide a conservative engineering tool.

In the UPS inductor evaluation, the Würth Elektronik RED EXPERT HCI1890 estimation of September 2015 is about as conservative as Vishay's, but the February 2016 edition is a lot more optimistic. Component Selector should not be used at all for this purpose. All of them heavily underestimate HCF2013 (PQ ferrite) losses.

Coilcraft's web tool is far too optimistic about the XAL1580 series and it shouldn't be used at all for the SER (PQ ferrite) core inductors.

A similar pattern can be seen for the PSU inductors (IHLP5050FD-01, HCI1365, and XAL1010). Both WE and Coilcraft report significantly lower inductor losses than Vishay, despite the fact that actual performance is quite similar.

6.4 Accuracy of Switch Controller Design Tool FET Losses

I was probably overly ambitious to think that I could size up both the inductor and the FET loss simulation tools in the same evaluation. What I have found out is that the 12 V buck/boost frequency / load current / inductance sweet spot is at a lower frequency than where I had expected it to be (if it exists). The PSU low-load losses were clearly higher than anticipated, but I don't know how much the FET loss calculator is to blame for this.

Hopefully the FET loss simulators make an accurate judgement on the FETs' relative positioning.

6.5 Single vs. Dual Phase

The 16 to 12 V buck / boost example only reaches break-even at 12 A, which is higher than I had assumed. The exact location of break-even is application specific, but you must really be designing for high average currents for dual phase to be worth considering.

It would be good to be able to automatically switch between single and dual phase depending on load.

6.6 External Freewheeling Diode

It seems that modern FETs have such a good body diode that the benefit from adding an external freewheeling diode is minuscule at best.

6.7 Outcome of the MODPSU Loss Minimization

The PSU benchmarking shows an astonishing improvement over the picoPSU (60% lower losses at 8 + 8 A), which is partly due to modern FETs and a lower switching frequency but probably also a consequence of better PCB layout and perhaps a better switch controller.

I have not done measurements on the Mini-Box buck/boost board, but from their choice of FETs, the fact that it is a dual-phase design, and its low rated maximum continuous load current (12 A), it is highly likely that the single-phase MODPSU buck/boost board also has significantly lower losses.

I have achieved my goal to construct a range of power supply products that runs very cool and enables the new PC computer types I was aiming at. I think that I have taken this as far as what is possible with today's off-the-shelf components.

CHAPTER 7

7 Future Work

There are numerous topics within this area that need better engineering data, so a systematic generation of it would have great practical value. (See 4.3.6.) This would require construction of a test rig for automated testing at all relevant operating points and temperatures, in both buck and boost mode.

In addition to testing all relevant off-the-shelf inductors, comparisons could be made to custom-made ones in:

- toroid, PQ-ish, and pot core shape,
- across core materials and permeability grades, also comparing
- round wire to flat wire (skin and proximity effects).

This is not a small task, but with the great decrease in FET losses, inductor losses are becoming more important.

It would also be interesting to compare switch controllers (sum of losses due to overly safe dead-time elimination, shoot-through, and (weak) gate driver strength).

Finally, it would be interesting to see how accurate LTpowerCad II v2 and WEBBENCH are in terms of FET loss simulation accuracy, at least to find out if the relative positioning of the FETs is correct.

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