

Master's Thesis

**Direct Conversion Front End for  
LTE and LTE-A with  
Frequency-Translational Feedback,  
Harmonic Rejection Mixer and  
Input Matching Compensation**

Douglas Andersson Hägglund



Direct Conversion Front End for LTE and LTE-A  
with Frequency-Translational Feedback, Harmonic  
Rejection Mixer and Input Matching  
Compensation

Douglas Andersson Hägglund  
douglasanderssonhagglund@hotmail.com

Supervisors:  
Anders Nejdell  
Markus Törmänen

Department of Electrical and Information Technology  
Lund University

May 31, 2016

Printed in Sweden  
E-huset, Lund, 2016

---

# Abstract

---

This thesis covers the design of a wideband, flexible front end for LTE and LTE-A in a 65 nm CMOS process. A topology with global frequency translational feedback is investigated and a harmonic rejection mixer is implemented. To compensate for parasitics at the RF input, a variable phase shift is used in the global feedback to improve input matching and prevent loss of noise performance. Combinations of these techniques are compared to a standard quadrature implementation. The suitability of three different baseband amplifiers for the circuit is also evaluated.

The full system is functional between 700 MHz and 3.7 GHz and has a noise figure of between 1.5 and 1.3 dB depending on frequency of operation. The system provides 43 dB of gain and has an out-of-band IIP3 and  $CP_{1dB}$  of -8 and -23 dBm, respectively. The current consumption is 21 mA from a 1.2 V supply and includes the consumption of the LNTA and baseband amplifiers.



---

# Acknowledgments

---

It is finally done! This thesis is the result of hard work, the proverbial blood, sweat and tears as well as countless hours of CPU time. It certainly wouldn't be here, were it not for a lot of great people for whom I would like to dedicate a few lines.

First of all I would like to thank my supervisors, Anders Nejdell and Markus Törmänen, for their assistance from day one with all questions, no matter how large or small. Valuable input on the project has also been given by Mohammed Abdulaziz, Waqas Ahmad and Therese Forsberg. I would also like to thank Stefan Molund and Erik Jonsson for their rapid help whenever problems with disk quotas and access to software arose.

All my friends have been great supporters of me during this endeavor providing input and creating an atmosphere full of laughter and overall awesomeness. Lars Johan Björkman, being a native English speaker, has also helped keep language related errors to a minimum through proofreading.

Last, but certainly not least, I want to give a shout-out to my greatest supporters, my mom, dad and brother. I love you all and could not have done this without you.



---

# Table of Contents

---

<b>1</b>	<b>Introduction</b>	<b>1</b>
1.1	Thesis outline . . . . .	3
<b>2</b>	<b>Theory</b>	<b>5</b>
2.1	Definition of performance metrics . . . . .	5
2.2	Frequency-translational feedback front ends . . . . .	8
2.3	Noise folding and harmonic blockers . . . . .	11
2.3.1	Harmonic-rejection mixer . . . . .	13
2.4	Global loop closing and input matching compensation . . . . .	15
2.4.1	Quadrature system . . . . .	16
2.4.2	Full 16% and 33% systems . . . . .	16
2.4.3	Hybrid system . . . . .	19
<b>3</b>	<b>Circuits</b>	<b>23</b>
3.1	LNTA . . . . .	23
3.2	Mixers . . . . .	24
3.3	Amplifiers . . . . .	26
3.3.1	Purely complementary amplifier . . . . .	26
3.3.2	Complementary amplifier with tail current source . . . . .	28
3.3.3	Combiner amplifier . . . . .	30
3.4	Phase shifting network . . . . .	31
<b>4</b>	<b>System simulation results</b>	<b>35</b>
4.1	Quadrature system . . . . .	35
4.2	Full 1/6 duty cycle system . . . . .	37
4.2.1	Resistor tuning and performance . . . . .	37
4.2.2	Impact of 33% duty cycle . . . . .	39
4.3	Hybrid system . . . . .	41
<b>5</b>	<b>Conclusion</b>	<b>43</b>
5.1	Future work . . . . .	45
5.1.1	Noise-cancelling path . . . . .	45
5.1.2	Full 16 % system with feedback of Quadrature signals . . . . .	45



<b>References</b>	<b>47</b>
<b>A Test bench schematics</b>	<b>51</b>

---

## List of Figures

---

1.1	Principal schematics of a voltage-mode, narrowband superheterodyne (top) and a current-mode, wideband, direct conversion (bottom) front end working with TDD. For FDD systems the SAW-filter is replaced by a duplexer . . . . .	2
2.1	Intermodulation products . . . . .	6
2.2	Illustration of the non-linearity performance metrics . . . . .	7
2.3	Points and symbols used in the derivation of the expression of the IIP3	8
2.4	Principal architecture of a current-mode frequency-translational feed-back front end . . . . .	9
2.5	Baseband gain translation and its determination of input matching .	10
2.6	Input matching of the front end. Blue depicts the ideal scenario, red depicts the frequency-shifted peak . . . . .	10
2.7	Noise folding . . . . .	11
2.8	Effective 25%, 33% and 16% duty cycle waves of arbitrary units used for calculation of Fourier coefficients . . . . .	12
2.9	Harmonic blockers mixing with harmonics of the LO down to baseband	13
2.10	Schematic of 6-phase harmonic rejection mixer . . . . .	14
2.11	Construction of the voltages in (2.11). 1st harmonic on the left and 3rd harmonic on the right . . . . .	14
2.12	Full quadrature system with bondwire and pad model at the input . .	17
2.13	Construction of vectors of arbitrary phase through linear combinations of TIA outputs . . . . .	18
2.14	Construction of vectors of arbitrary phase through linear combinations of quadrature outputs . . . . .	19
2.15	Full 6-phased system with bondwire and pad model at the input . . .	20
2.16	Full hybrid system with bondwire and pad model at the input . . . .	21
3.1	Transconductor circuit . . . . .	24
3.2	LNTA transfer characteristics . . . . .	25
3.3	Linearity of LNTA . . . . .	25
3.4	Double balanced passive mixer . . . . .	26
3.5	Purely complementary amplifier with CMFB-amplifier at the bottom	27

3.6	Schematic of OP-amp with CMFB-amp to the right. . . . .	29
3.7	Gains of the amplifiers as a function of input frequency . . . . .	30
3.8	IIP3s of amplifiers as a function of offset frequency . . . . .	30
3.9	Harmonic rejection combination amplifiers . . . . .	31
3.10	Global feedback phase shifting network . . . . .	33
3.11	Global feedback phase shifting network in the hybrid system . . . . .	34
4.1	Various characteristics of the quadrature system . . . . .	36
4.2	S11 with phase-shifting feedback turned on (blue) and off (red) . . .	37
4.3	Various characteristics of the full 16% system. With feedback compensation in blue and without in red . . . . .	38
4.4	Various characteristics of the 33% system . . . . .	40
4.5	Various characteristics of the hybrid system . . . . .	42
5.1	Various characteristics of all systems compared. Quad system in black, 33% system in magenta, 16% system in red and hybrid system in blue	44
A.1	Test bench for simulating the linearity and frequency response of the LNTA with ideal components in green. Details regarding port termination omitted . . . . .	51
A.2	Test bench for simulating the linearity of the amplifiers with ideal components in green. Details regarding port termination omitted . .	52
A.3	Test bench for simulating the open loop characteristics of the amplifiers with ideal components in green. Details regarding port termination omitted . . . . .	52

---

## List of Tables

---

2.1	Fourier coefficients of the 33% and 16% waves in figure 2.8 . . . . .	12
3.1	Properties of the LNA . . . . .	24
3.2	Properties of purely complementary amplifier in figure 3.5 . . . . .	28
3.3	Properties of amplifier in 3.6 . . . . .	29
3.4	Values of combiner amplifier resistors . . . . .	32
4.1	Values of system critical variables . . . . .	35
4.2	Optimal resistor values for the global feedback in figure 3.10 . . . . .	39
4.3	Optimal resistor values for the global feedback in figure 3.11 . . . . .	41
5.1	Final system metrics. All measured at 1 GHz and an 80 MHz offset where applicable. 3rd order blocker tolerance at zero offset . . . . .	43



---

## Commonly used abbreviations

---

LTE-A: Long-Term Evolution Advanced  
FDD: Frequency Division Duplexing  
TDD: Time Division Duplexing  
LNA: Low Noise Amplifier  
LNPA: Low Noise Transconductance Amplifier  
NF: Noise Figure  
IIP: Input-referred Intercept Point  
CP: Compression Point  
BB: Baseband  
RF: Radio Frequency  
CS: Common-Source  
CG: Common-Gate  
HRR: Harmonic Rejection Ratio  
LO: Local Oscillator  
IF: Intermediate Frequency  
BJT: Bipolar Junction Transistor  
MOSFET: Metal-Oxide Semiconductor Field-Effect Transistor  
NMOS: N-Type MOSFET  
PMOS: P-Type MOSFET  
TIA: Transimpedance Amplifier  
CMRR: Common-Mode Rejection Ratio  
TX: Transmitter  
SAW: Surface Acoustic Wave  
ADC: Analog-to-Digital Converter



---

# Introduction

---

The 4th generation of cellular communication is upon the world. More and more devices are connected to the cellular network and the bandwidth demands of the average user increases as music and high-definition video streaming becomes more popular. In order to meet the demands, advances need to be made in all research areas of wireless communication including the analog front end which sets a limit for the sensitivity and thus the bit-error-rate.

LTE and LTE-A, which are the actual communication standards that implement 4G [1], work with 42 different frequency bands (at time of printing, more bands are planned) in the span between 452.5 MHz and 3.8 GHz. Both TDD, when both receiver and transmitter are working at the same frequency but at different times, and FDD, for which the transmitter and receiver work at the same time but at different frequencies, duplexing methods are available. Bandwidths vary from 5 MHz to 200 MHz and the magnitude of the duplex spacing varies between 10 MHz and 400 MHz. Channel bandwidths are typically between 1.4 MHz and 20 MHz. In order to be economically viable any front-end must be extremely flexible and support as many frequency bands and configurations as possible. This rules out the use of inductors as having a single inductor for every band would take up a huge chip area. Even if some inductors can be shared between some bands, it is not viable [2][3][4]. Instead a wideband approach has to be taken.

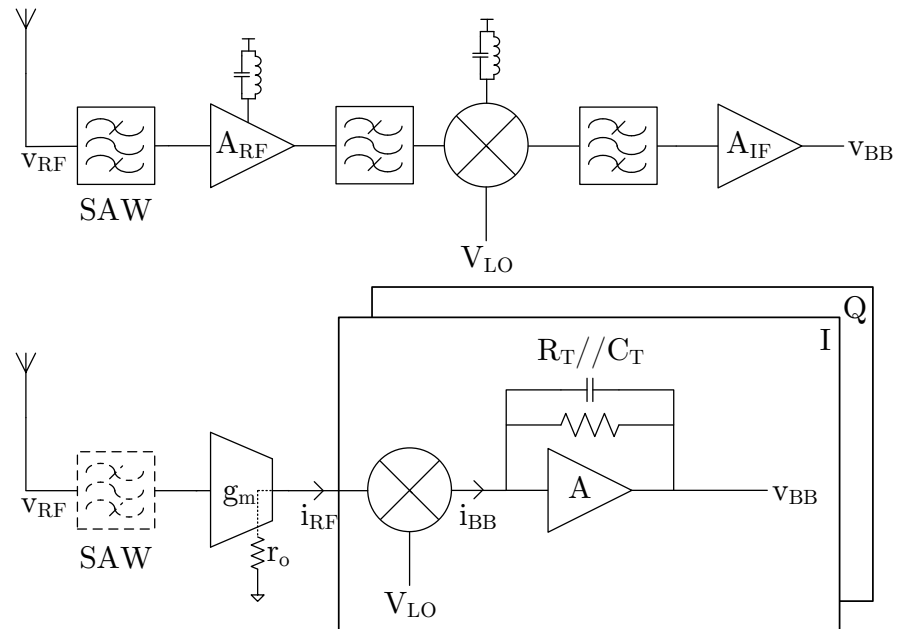
In recent years direct-conversion front-ends, meaning that the LO's frequency is tuned to the frequency of the input signal, have become popular for a number of reasons [5][6][7]. This architecture has many advantages compared to the superheterodyne, the most important of which is that no off-chip IF-components are needed and that the requirements on baseband filtering and the analog-to-digital converter therefore are reduced. Since the communication in LTE uses both sidebands symmetrically, the image of the incoming signal is itself and what is a problem for a superheterodyne is actually exploited in direct-conversion receivers [8, p. 711].

Direct-conversion receivers are not without disadvantages, however. Even if double-balanced passive mixers are used some of the LO voltage will leak to the input port. The leakage will mix with itself and create a DC-offset at the output which is amplified by the baseband circuitry. This can lead to a complete desensitization of the amplifiers and limit the dynamic range of the ADC. High second-order linearity is also of prime importance since incoming, adjacent chan-



nels or distortion from the LNA itself can intermodulate down to baseband [9][10].

Because of the low supply voltage in modern process nodes, 1.2 V for 65 nm, the voltage swing capabilities of amplifiers are small. This fundamentally limits the voltage compression point of radio receivers. In a wideband design, filtering is reduced at RF and strong blockers from the environment or the transceiver's own TX in an FDD system will in a voltage-mode LNA lead to large voltage swings at the output. This leads to compression of the receiver. A way to alleviate the problem is by minimizing the input voltage to the mixer by using a low-noise transconductance amplifier as the front-end input stage. This converts the input voltage to a current and the mixers are then run in current-mode. The signal is converted back to a voltage by a transimpedance amplifier with a low input impedance where the blocker's current contribution will be at a higher frequency and can thus be filtered by a pole in the TIA transimpedance[11][12].



**Figure 1.1:** Principal schematics of a voltage-mode, narrowband superheterodyne (top) and a current-mode, wideband, direct conversion (bottom) front end working with TDD. For FDD systems the SAW-filter is replaced by a duplexer

A true wideband receiver does not employ a SAW-filter and efforts are being made in the research community to avoid them. Without any input filtering the requirements on blocker tolerance and linearity are raised immensely as any blocker will be amplified by the wideband LNTA and if close enough in frequency to the LO, or a harmonic of the LO it might be downmixed to baseband by phase noise or

harmonic mixing [13][14][7]. In FDD systems, however, transmitter and receiver are electrically connected to each other at all times and the system therefore needs a duplexer.

## 1.1 Thesis outline

The goal of this thesis is to implement a current-mode direct-conversion front end, save the oscillator, working at most LTE frequencies. A frequency-translational feedback approach is taken and harmonic-rejection mixers are used. The process used is ST Microelectronics' 65 nm process, and a supply voltage of  $V_{DD} = 1.2 V$  is utilized. The design takes place strictly in the schematic domain and no layout is produced.

In chapter 2 the theory of operation of the front end is explained and performance metrics are defined. In chapter 3 the circuits that implement the different blocks in chapter 2 are analyzed, discussed and the performance and properties of them are listed. In chapter 4 system-wide simulations on noise, matching and linearity and the effect of various architectural choices on these metrics are presented. Lastly, in chapter 5 conclusions are drawn from the results and possible future improvements are discussed.



## 2.1 Definition of performance metrics

Noise figure ( $NF$ ) and noise factor ( $F$ ) are two of the most important performance metrics for any component in a wireless receiver. They are defined in (2.1) where  $SNR_{out}$  and  $SNR_{in}$  denote the signal-to-noise ratio of the input and output signals of the block.

$$F = \frac{SNR_{out}}{SNR_{in}} \quad (2.1)$$

$$NF = 10\log_{10}(F) = SNR_{out}(dB) - SNR_{in}(dB)$$

If several blocks are cascaded the contribution of each block to the total noise figure is suppressed by the gain of preceding stages. Such a system's noise factor is given by Friis's formula which is stated in (2.2).  $F_i$  and  $A_i$  represent the noise factor and the amplification of the  $i$ :th stage, respectively, where  $i$  goes from 1 to  $n$  [15].

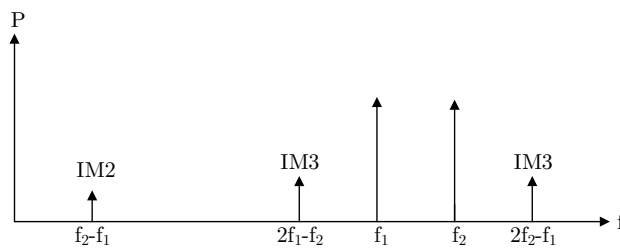
$$F_{total} = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \dots + \frac{F_n - 1}{A_1 A_2 \dots A_{n-1}} \quad (2.2)$$

This equation shows that the first gain stage reduces the noise of all stages and that only the first component's noise is unaffected. It is therefore the most important to optimize the first stage's gain and noise performance.

Noise figure in this thesis will always be presented as a function of LO frequency and the actual number is an average across the whole 10 MHz baseband bandwidth. This corresponds to an average noise figure across a full LTE20 channel.

Any real electronic system will have some nonlinearities associated with it. For example an amplifier goes into compression and clips the output signal as the output signal approaches the supply rail voltages. Its gain is often slightly higher during the time period when the input signal is large, which can be traced back to the square or exponential transfer characteristic of FETs and BJTs, respectively. Another cause is that some small-signal parameters such as output resistance and transconductance also varies over the duration of a signal period. These nonlinearities are often called weak distortion. Strong distortion, clipping, is present for very large signals and occurs whenever output signals approach the supply rails of the circuit.

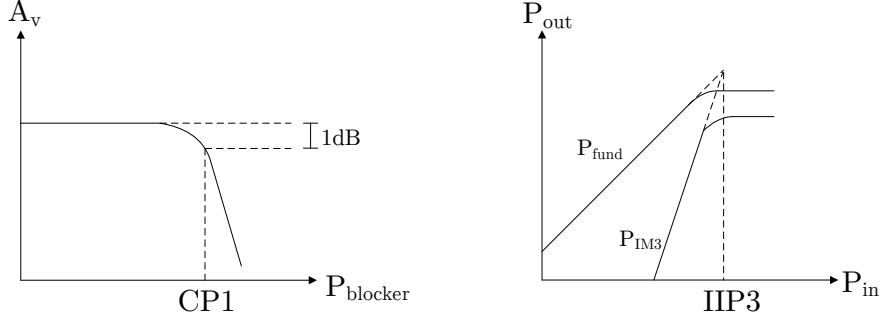
In the frequency domain, distortion can be seen in various ways. Harmonic distortion occurs when signals with frequencies that are integer multiples of the input signal's appear in the output. In most communication systems these signals are outside the bandwidth of the system and can be disregarded in most cases. Another, more problematic type of distortion is intermodulation distortion which is present whenever more than one tone is present at the input. The tones will intermodulate and produce additional components at frequencies that are sums and differences of the harmonics of the input signals, but the sums are often disregarded for distortion orders higher than 2. The most commonly seen are IM2 which is located at  $f = f_1 - f_2$  and  $f = f_1 + f_2$  and IM3 at  $f = 2f_1 - f_2$  and  $f = 2f_2 - f_1$ . The IM2 product is especially problematic in direct-conversion receivers since if  $f_1$  and  $f_2$  are closely spaced, which is the case with an incoming signal of interest and strong, modulated TX leakage in an FDD system, the resultant IM2 is close to DC where it goes through the receiver chain unfiltered.



**Figure 2.1:** Intermodulation products

Two different figures of merit are usually used to measure the level of non-linearity in a circuit, the compression point (CP) and the intercept point (IP). These can be defined in a variety of ways, but the ones used in this thesis are crosscompression CP1 ( $CP_{1dB}$ ), IIP2 and IIP3. The CP1 of a circuit is acquired by sweeping the input power of an interfering signal at a specified frequency and noting the point at which the small-signal voltage gain has dropped by 1 dB. The IIP2 and IIP3 are measured in a similar way. Two tones with the same power are input, but the power of the output intermodulation products, IM2 and IM3, are measured. From the linear operation region of the circuit, asymptotes are drawn and the point at which they intercept is called the IP2 or IP3 depending on what intermodulation product is measured. Most frequently the point is taken on the input power axis and is therefore called the input referred IP2 (IIP2) or IP3 (IIP3).

It is important during simulation of IPs that the offset frequencies used are given since the measured value typically varies with frequencies. In this thesis whenever an IP is mentioned, it is measured with an IM frequency of 1 kHz and the frequency in figures refers to the lowest frequency of the two fundamentals. Since all circuits have limited bandwidths the IPs presented have been adjusted for the lower gain at higher frequencies by simply assuming that the fundamental output power is the amount of attenuation larger than what is measured. In other words the intermodulation power is always compared to the power of an in-band



**Figure 2.2:** Illustration of the non-linearity performance metrics

signal and if the graphs are not compensated for the attenuation this becomes impossible.

In logarithmic units the in-band power gain,  $A_{IB}$ , is measured and the intermodulation power,  $P_{IM3}$ , is checked at a power point,  $P_{in,0}$ , where the gain curve is linear. The equations for the extrapolated lines are seen in equations 2.3, 2.4 where  $P_{o,fund}$  and  $P_{o,IM3}$  are the in-band, fundamental and 3rd order output power and  $m_{fund} = A_{IB}$  and  $m_{IM3}$  are the lines' intersections with the output power axis respectively.

$$P_{o,fund} = 1P_{in} + m_{fund} \quad (2.3)$$

$$P_{o,IM3} = 3P_{in} + m_{IM3} \quad (2.4)$$

At the intercept point the output and input powers are equal for the two lines which leads to the following equation:

$$P_{in} + A_{IB} = 3P_{in} + m_{IM3} \quad (2.5)$$

$P_{in}$  is in this case the sought input-referred intercept point and can be written as:

$$IIP3 = \frac{A_{IB} - m_{IM3}}{2} \quad (2.6)$$

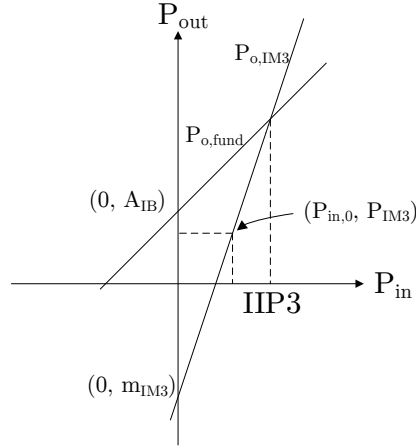
Inserting the measured power point  $P_{o,IM3} = P_{IM3}$  and  $P_{in} = P_{in,0}$  into the equation in 2.4 yields:

$$m_{IM3} = P_{IM3} - 3P_{in,0} \quad (2.7)$$

Which results in a final equation for the IIP3:

$$IIP3 = \frac{A_{IB} - P_{IM3} + 3P_{in,0}}{2} \quad (2.8)$$

Since differential signaling in theory completely cancels all second order nonlinearities, the IIP2 will be dependent only on mismatch introduced in layout and



**Figure 2.3:** Points and symbols used in the derivation of the expression of the IIP3

by process variations. Since no layout is produced in this thesis and Monte Carlo simulations are very time consuming, no IIP2 simulations are run.

Also of interest in this thesis is the resilience to harmonic blockers, specifically to third order blockers. To measure this another compression point is simulated but instead of sweeping input power at a certain offset around the LO frequency, power is swept at frequencies around 3 times the LO frequency. The harmonic blocker tolerance is defined as the 3rd order input power at which small signal gain has dropped by 1 dB.

According to the theorem of maximum power transfer the highest power is delivered to a load if the load impedance equals the source impedance. This is doubly true at radio frequencies since the input feeding system to the load is typically a transmission line and impedance mismatches between load, line and source will lead to power reflections. High sensitivity therefore requires correct impedance matching. To quantify the matching the first element of the system's S-matrix,  $S_{11}$ , is used, which is defined as the amount of power coming out from the input port divided by the incoming power.

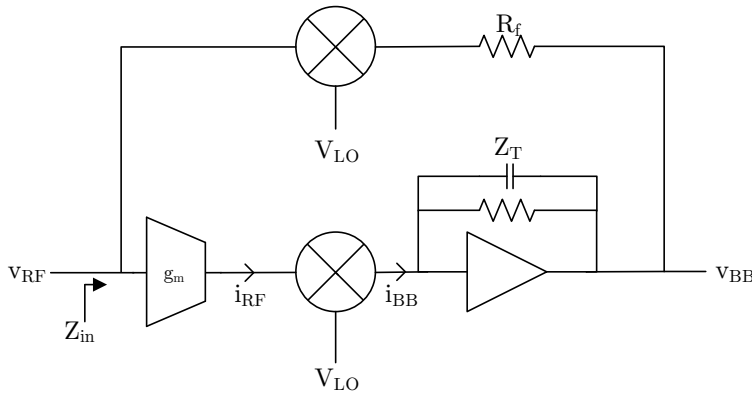
## 2.2 Frequency-translational feedback front ends

For a traditional front end the impedance matching between the antenna interface and the receiver is set by the input impedance of the LNA. A common approach to this problem is using inductively degenerated CS stages. As previously mentioned the frequency bands used in LTE and LTE-A vary greatly from one another in terms of carrier frequency. The use of inductors automatically makes the design narrowband which means that several gate and source source inductors have to

be supplied on the chip (or worse, outside the chip) which warrants a very large chip size. Chips intended for an international market would become prohibitively expensive and therefore this approach is not good enough.

Another classically viable technique is to use only a CG stage as the LNTA. The CG at first looks like an excellent alternative because of the simple, wideband matching ( $r_{in} = \frac{1}{g_m}$ ). It can fall short, however, since the transconductance of the transistor is fixed and therefore inflexible. The noise performance is also low and the noise figure is typically larger than 3 dB even for long channel devices [16, p. 21].

A recent advance in the field uses a CS-stage with an intentionally large input impedance and then feeding back the baseband signal to RF through a resistance and an upconverting set of mixers. From feedback theory we know that a shunt-shunt connected amplifier's input impedance is  $Z_{in} \approx \frac{R_f}{A}$ , i.e. the feedback resistance divided by the forward gain. Since a resistor is easily tuned it is possible to achieve a good match for many different gain configurations of the forward path. The principal architecture is displayed in figure 2.4

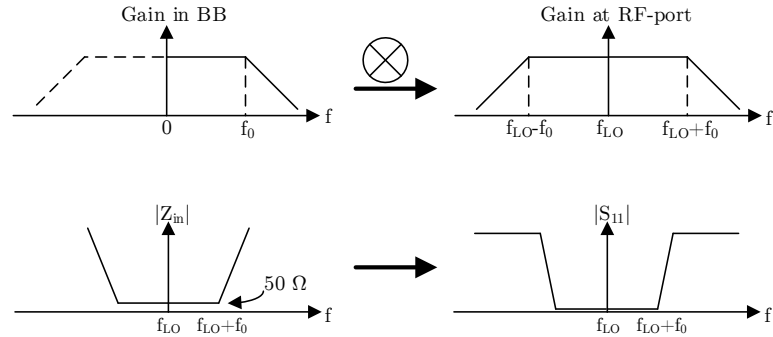


**Figure 2.4:** Principal architecture of a current-mode frequency-translational feedback front end

Assuming a reciprocal mixer and disregarding the mixer gain and resistance, the forward gain of the receiver is approximately equal to  $A_v = g_m Z_T$ . For an RF-signal at  $\omega = \omega_{LO} + \Delta\omega$ , the frequency of the baseband signal will be  $\Delta\omega$  and the gain will be  $A_v = g_m Z_T(\Delta\omega)$ . Assuming that the resistor in the feedback path is tuned for maximum gain, the input impedance of the receiver will be  $50 \Omega$  for every  $\Delta\omega$  that is smaller than the bandwidth of the RC-pole that implements  $Z_T$ . For  $\Delta\omega$  that are larger than  $\frac{1}{RC}$ , the transimpedance will fall, which leads to a smaller gain and therefore a larger input impedance. This means that the baseband frequency response is translated up to  $\omega_{LO}$ . The entire concept can be seen in figure 2.5.

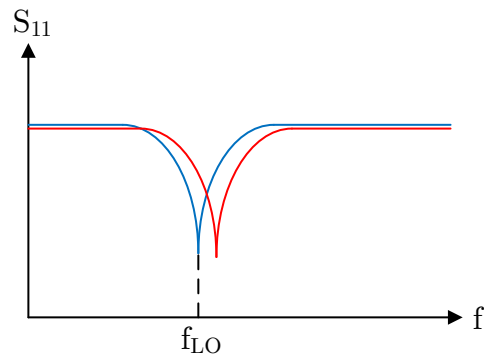
This is ideal for a flexible front end since the narrowband matching can be moved to any frequency by simply changing the frequency of the LO. Unfortunately





**Figure 2.5:** Baseband gain translation and its determination of input matching

parasitics, bondwires and various phase shifts in the forward path leads to a shift in the frequency of the matching peak [17], an example of which can be seen in figure 2.6. Matching will still be perfect in magnitude if the resistor is tuned properly

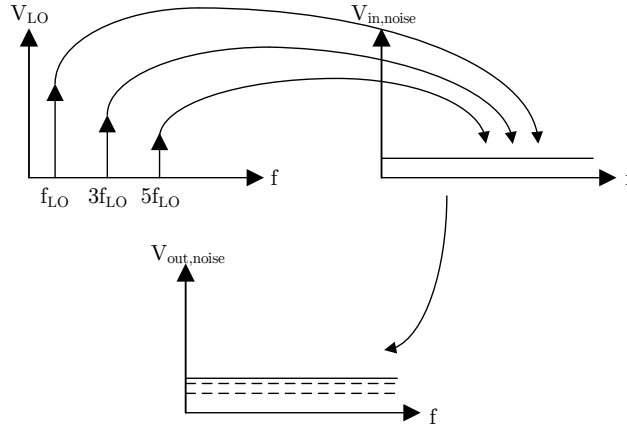


**Figure 2.6:** Input matching of the front end. Blue depicts the ideal scenario, red depicts the frequency-shifted peak

but the frequency at which this happens will change. The shifts can reach sizes of several MHz which can lead to neighboring channels leaking information across channel borders and a reduction in receiver sensitivity. This warrants a solution which is proposed in section 2.4

## 2.3 Noise folding and harmonic blockers

In theory any waveform can be used to switch RF-signals and mix them to a lower frequency. In reality, however, square waves are almost always used since they maximize the switching speed, improve the noise performance and are easy to generate [16, p. 16]. From Fourier analysis it is known that square waves apart from the fundamental tone also contain odd harmonics which also mix with the signal at the RF-input. In a direct-conversion receiver, the mixing products of RF-signals and the harmonics of the LO are almost always out-of-band and are filtered out, but this is not true for the noise floor of the LNA output signal. One extra copy of the noise floor will be added for every harmonic in the LO which is illustrated in figure 2.7.



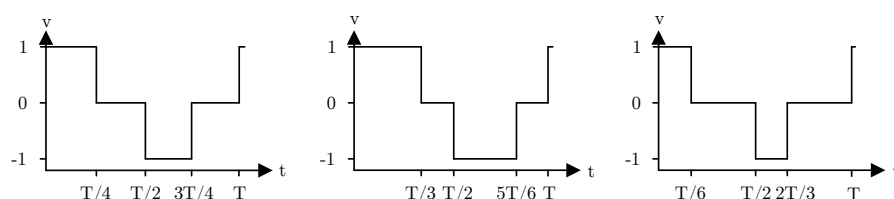
**Figure 2.7:** Noise folding

In order to calculate how big this noise folding penalty is, the ratio between the powers of the LO harmonics must be determined. There are many ways of representing a signal's harmonic content, but in this thesis the trigonometric representation of Fourier series is used. This means that voltages  $v(t)$  are represented by the coefficients  $a_0$ ,  $a_n$  and  $b_n$  with the following relationship, where  $T$  is the signal period and  $\omega T = 2\pi$ :

$$\begin{aligned}
 a_n &= \frac{2}{T} \int_{t_0}^{t_0+T} v(t) \cos(n\omega t) dt \\
 b_n &= \frac{2}{T} \int_{t_0}^{t_0+T} v(t) \sin(n\omega t) dt \\
 v(t) &= \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t)
 \end{aligned} \tag{2.9}$$

The top two equations in (2.9) are of the biggest importance since waves known in the time-domain will be deconstructed into their Fourier coefficients. The bottom equation shows how to get back to the time-domain and that  $a_i$  corresponds to a cosine wave and  $b_i$  to a sine wave, respectively.

Three types of waveforms are used in this thesis and can be seen in figure 2.8. While the waves are active half, two-thirds and one-third of the time, respectively, they are still called 25%, 33% and 16% waves since they are constructed by such waves in a differential manner. Applying the bottom two formulas in (2.9) yields



**Figure 2.8:** Effective 25%, 33% and 16% duty cycle waves of arbitrary units used for calculation of Fourier coefficients

the spectral content of the waves. Firstly, all even coefficients are 0 in every function since the signal is symmetrical around a constant term. For the 25% wave the ratios between the fundamentals and the  $k$ :th harmonics are simply  $\frac{a_k}{a_1} = \frac{(-1)^{(k-1)/2}}{k}$  and  $\frac{b_k}{b_1} = \frac{1}{k}$ ,  $k$  uneven. The formulae for the 33% and 16% are more complicated and do not lead to any profound insights and so a few values are presented in table 2.1 instead. Note that since the signals are symmetric all coefficients of even order are 0 and that the numbers have been normalized by multiplication with  $\frac{\pi}{2}$ .

	33%	16%
$a_0$	0	0
$a_1$	0.87	0.87
$b_1$	1.5	0.5
$a_3$	0	0
$b_3$	0	0.67
$a_5$	-0.17	-0.17
$b_5$	0.3	0.1

**Table 2.1:** Fourier coefficients of the 33% and 16% waves in figure 2.8

Using the voltage ratios the NF-penalty can easily be calculated by simply squaring them to get the power ratios and then summing them. For the standard

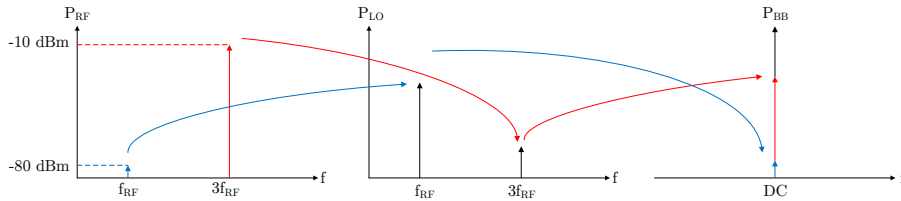
quadrature system with 25% duty cycle the penalty is:

$$NF_{penalty} = \sum_{n>0, n \text{ odd}}^{\infty} 1/n^2 = \frac{\pi^2}{8} \approx 1.2337 = 0.91 \text{ dB} \quad (2.10)$$

It is important to note that this is a penalty in total receiver noise figure and not in the individual mixer's. This is because the penalty is not in any way related to the noise added by the mixer components and hence the gain of the LNTA does not suppress it. This doesn't invalidate Friis's formula, however, as one can see the mixer as extending the gain-weighted noise bandwidth of the entire receiver.

The calculation in (2.10) is slightly inaccurate because it assumes that the input voltage is a pure square wave, which is never the case, and that the LO-port of the mixer has infinite bandwidth. The number of overtones that fall into the bandwidth of the mixer naturally depends on what the fundamental frequency is. A more reasonable estimate with no harmonics higher than 5 or 7 yield penalties of 0.61 and 0.69 dB respectively.

Another issue with square wave mixing is that strong interferers at frequencies that are harmonics of the LO will be mixed down to baseband. These will be amplified by the baseband transimpedance amplifiers and can lead to complete desensitization of them [18]. Figure 2.9 demonstrates how strong harmonic interferers can completely drown the desired signal at baseband.



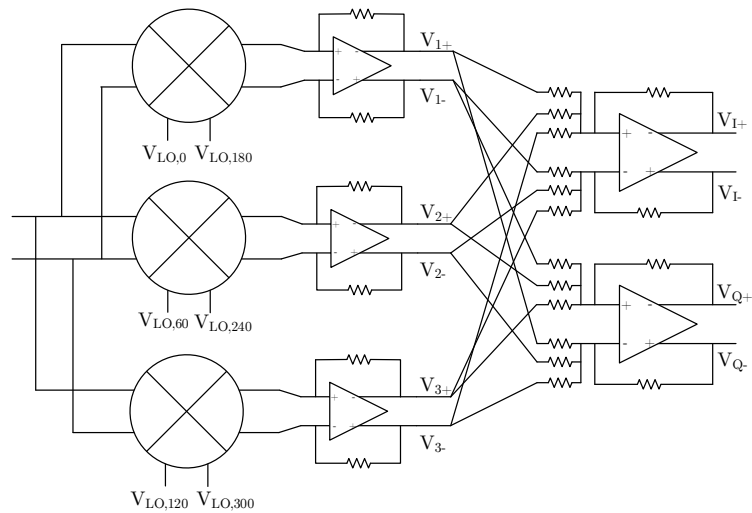
**Figure 2.9:** Harmonic blockers mixing with harmonics of the LO down to baseband

In order to alleviate the aforementioned problems harmonic-rejection mixers have become commonplace in direct-conversion receivers [19][20][21].

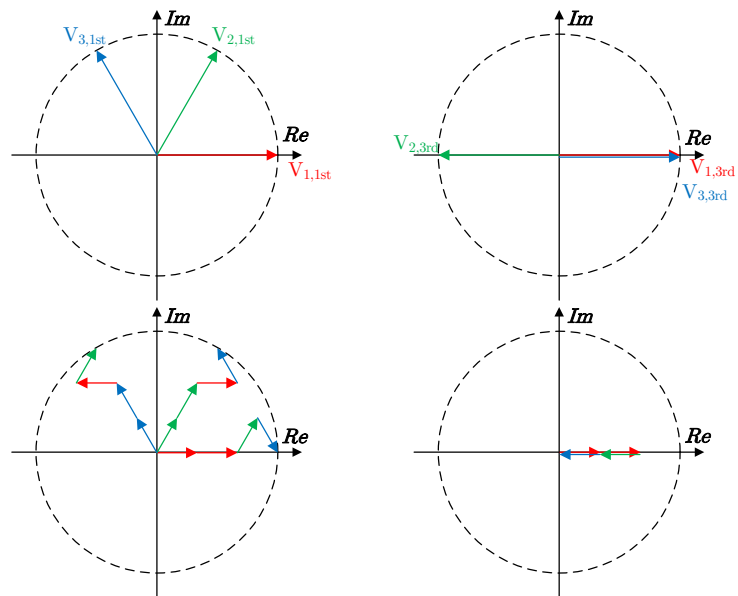
### 2.3.1 Harmonic-rejection mixer

Harmonics of the LO can efficiently be suppressed by using a harmonic rejection mixer. The idea of harmonic rejection is based on the fact that the phase rotation in time by the harmonics is faster than that of the fundamental. Several copies of the RF-signal are mixed with different phases and then added together with various gains so that the fundamental tone is unaffected or amplified and the harmonics are canceled.

The mixer utilized in this work uses 6 different phases with a  $60^\circ$  difference between them and a duty cycle of 16% in the normal case but the system with overlapping 33% LO signals will also be investigated [22]. The principal architecture can be seen in figure 2.10.



**Figure 2.10:** Schematic of 6-phase harmonic rejection mixer



**Figure 2.11:** Construction of the voltages in (2.11). 1st harmonic on the left and 3rd harmonic on the right

Consider the voltages in (2.11). In figure 2.11 it is shown that these voltages have the same amplitude and phase at the fundamental tone as the components but are lacking the third harmonic. Note that only  $v'_1$  is shown for the third harmonic due to figure congestion, it is trivial, however, to show that the same cancellation occurs in  $v'_2$  and  $v'_3$ . While each of these signals could serve as outputs on their own, two outputs phase-shifted  $90^\circ$  relative to each other are desired. Since none of the voltages contain a spectral component at the third harmonic, any linear combination of them will not have this content either. To arrive at the target, two new vectors  $v_I$  and  $v_Q$  that are shifted  $15^\circ$  and  $-15^\circ$  from  $v_1$  and  $v_3$ , respectively, are introduced in equations (2.12).

$$\begin{aligned} v'_1 &= (2v_1 + v_2 - v_3)/3 \\ v'_2 &= (2v_2 + v_3 + v_1)/3 \\ v'_3 &= (2v_3 - v_1 + v_2)/3 \end{aligned} \quad (2.11)$$

$$\begin{aligned} v_I &= (1 + \sqrt{3})v'_1 + v'_2 \\ v_Q &= (1 + \sqrt{3})v'_3 + v'_2 \end{aligned} \quad (2.12)$$

Combining the equations (2.11) and (2.12) yields the equation in (2.13).

$$\begin{aligned} v_I &= 1/\sqrt{3}((\sqrt{3} + 2)v_1 + (\sqrt{3} + 1)v_2 - v_3) \\ v_Q &= 1/\sqrt{3}(-v_1 + (\sqrt{3} + 1)v_2 + (\sqrt{3} + 2)v_3) \end{aligned} \quad (2.13)$$

This shows that it is possible to implement harmonic rejection with only 2 combination amplifiers. The rejection does not show however until after the base-band TIAs and recombination amplifiers. This can lead to desensitization of the amplifiers if the environment has strong harmonic blockers present and the system is actually more sensitive to this than a standard quadrature system since a 16% duty cycle wave has a higher level of the 3rd harmonic than a 25% wave. The solution to the problem lies in using overlapping 33% duty cycle waves instead, which eliminates the third harmonic from the LO voltage, completely at the price of increased noise.

If rejection is performed in accordance with the aforementioned equations cancellation is perfect. In practical circuits however the amount of the 3rd harmonic that can be canceled is limited by phase errors in the oscillator and mismatches between the mixers and the combining resistors. To get an accurate estimate is impossible without access to actual layout implementations of the circuit blocks, including the oscillator and its frequency divider, and without running Monte Carlo simulations. Because of these reasons the harmonic rejection ratio is not simulated in this thesis. Typically the HRR ranges from -40 dB to -70 dB if no calibration is used [22][23][7].

## 2.4 Global loop closing and input matching compensation

There are a variety of options to consider when closing the global loop. Signals from the harmonic rejection mixer in figure 2.10 must be fed back to the input in

some manner and in this thesis three configurations are tested.

As mentioned in section 2.2, non-idealities in the RF-source may lead to a non-50  $\Omega$  source impedance which shifts the matching peak's frequency. To counter this the feedback signal should be phase shifted which can be implemented in two different ways. The most intuitive way is phase shifting the local oscillator voltage going to the feedback mixers. While this leads to very low performance loss for the receiver it is incredibly difficult to design a variable-phase square-wave oscillator on-chip controllable to a precision of a few degrees, which renders this solution impractical. The other alternative is to phase shift the baseband voltage that is fed back. The outputs from the TIAs and I/Q combination amplifiers can all be used to create linear combinations of arbitrary phase and a few of the possibilities as well as the overall system schematics are presented in this section.

### 2.4.1 Quadrature system

The simplest possible configuration of a frequency translational feedback front end is not using a harmonic rejection mixer but instead using separate I and Q paths. This quadrature system provides a standard case to which the other systems can be compared. No matching compensation is performed in this system but it has been successfully implemented in previous work by cross-coupling the baseband signals to each other [17]. The schematic can be seen in figure 2.12

### 2.4.2 Full 16% and 33% systems

One option is feeding back the signals from the TIA through a network of resistors to create new voltages of arbitrary phase. Since all six signals are used the mixers in the feedback have to use the same oscillator voltages as the feedforward mixers. Since all oscillator signals have a duty cycle of 16% this system is called the full 16% system. This system can also be used to test the 33% duty cycle harmonic rejection use case and when this is done, the system will be referred to as the 33% system. The schematic of these systems, including a pad model, along with timing diagrams of the used LO voltages can be seen in figure 2.15. The resistor networks preceding the combination I/Q amplifiers and in the feedback have been omitted for clarity and the implementation of the latter is discussed in 3.4.

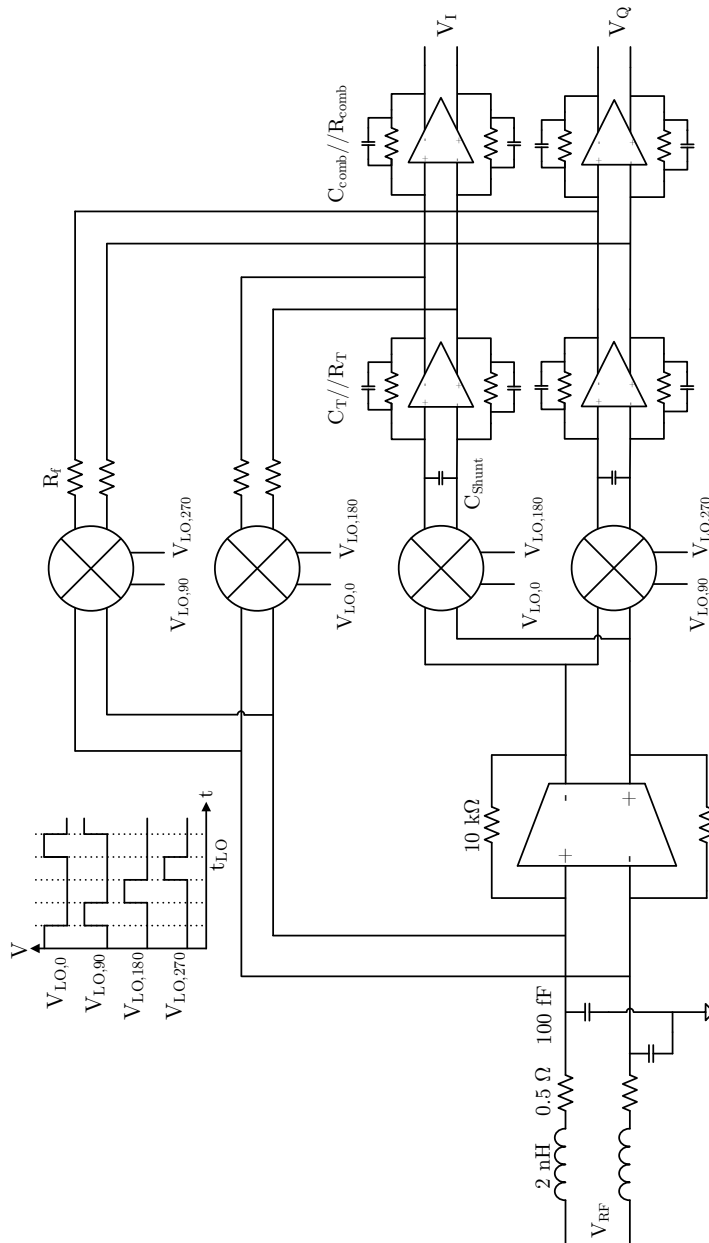
From the TIAs three complex voltage vectors and their negative differential copies, in equation (2.14) are available.

$$V_1 = Ae^{j0}, V_2 = Ae^{j\pi/3}, V_3 = Ae^{j2\pi/3} \quad (2.14)$$

The vectors in quadrature to the ones in (2.14) are introduced in (2.15).

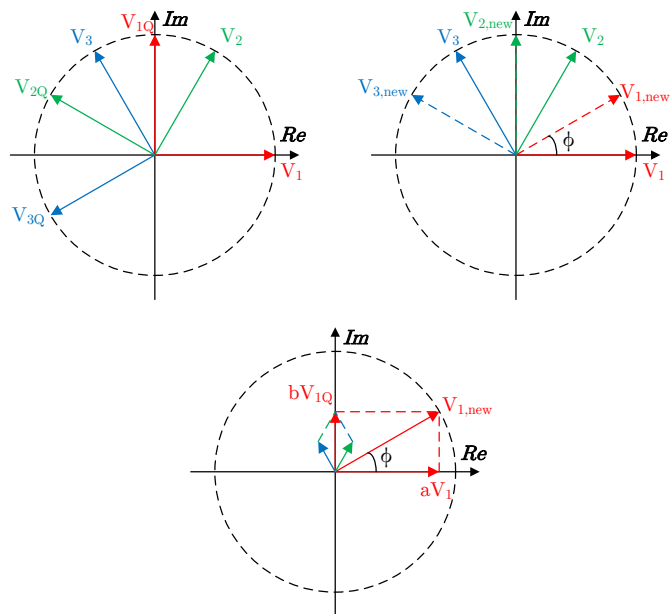
$$\begin{aligned} V_{1Q} &= Ae^{j3\pi/6} = (V_2 + V_3)/\sqrt{3} \\ V_{2Q} &= Ae^{j5\pi/6} = (-V_1 + V_3)/\sqrt{3} \\ V_{3Q} &= Ae^{j7\pi/6} = (-V_1 - V_2)/\sqrt{3} \end{aligned} \quad (2.15)$$

From the vector diagram in figure 2.13, the construction of a new set of vectors with an arbitrary phase difference from the original system can be seen. Only the

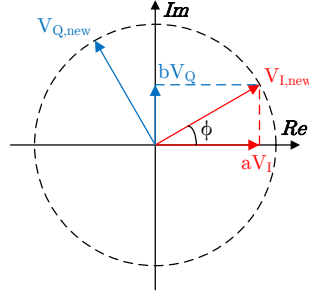


**Figure 2.12:** Full quadrature system with bondwire and pad model at the input





**Figure 2.13:** Construction of vectors of arbitrary phase through linear combinations of TIA outputs



**Figure 2.14:** Construction of vectors of arbitrary phase through linear combinations of quadrature outputs

synthesis of  $V_{1,new}$  is shown, but the others are derived in an analogous way. The equations are technically only valid for an angle between  $-90^\circ$  and  $90^\circ$  because of the use of the inverse tangent function but can be extended to the full circle by rotating the entire system  $180^\circ$ , e.g. completely reversing the feedback.

$$\begin{aligned} V_{1,new} &= aV_1 + bV_{1Q} = aV_1 + b(V_2 + V_3)/\sqrt{3} \\ V_{2,new} &= aV_2 + bV_{2Q} = aV_2 + b(-V_1 + V_3)/\sqrt{3} \end{aligned} \quad (2.16)$$

$$\begin{aligned} V_{3,new} &= aV_3 + bV_{3Q} = aV_3 + b(-V_1 - V_2)/\sqrt{3} \\ \phi &= \arctan(b/a) \end{aligned} \quad (2.17)$$

$$1 = a^2 + b^2 \quad (2.18)$$

### 2.4.3 Hybrid system

Another option is, while keeping the harmonic rejection mixer in the forward path, feeding back the quadrature output signals instead through mixers running at 25% duty cycle. The resultant system can be seen in figure 2.16 and will henceforth be called the hybrid system since it requires both 25% and 16% duty cycle LO signals.

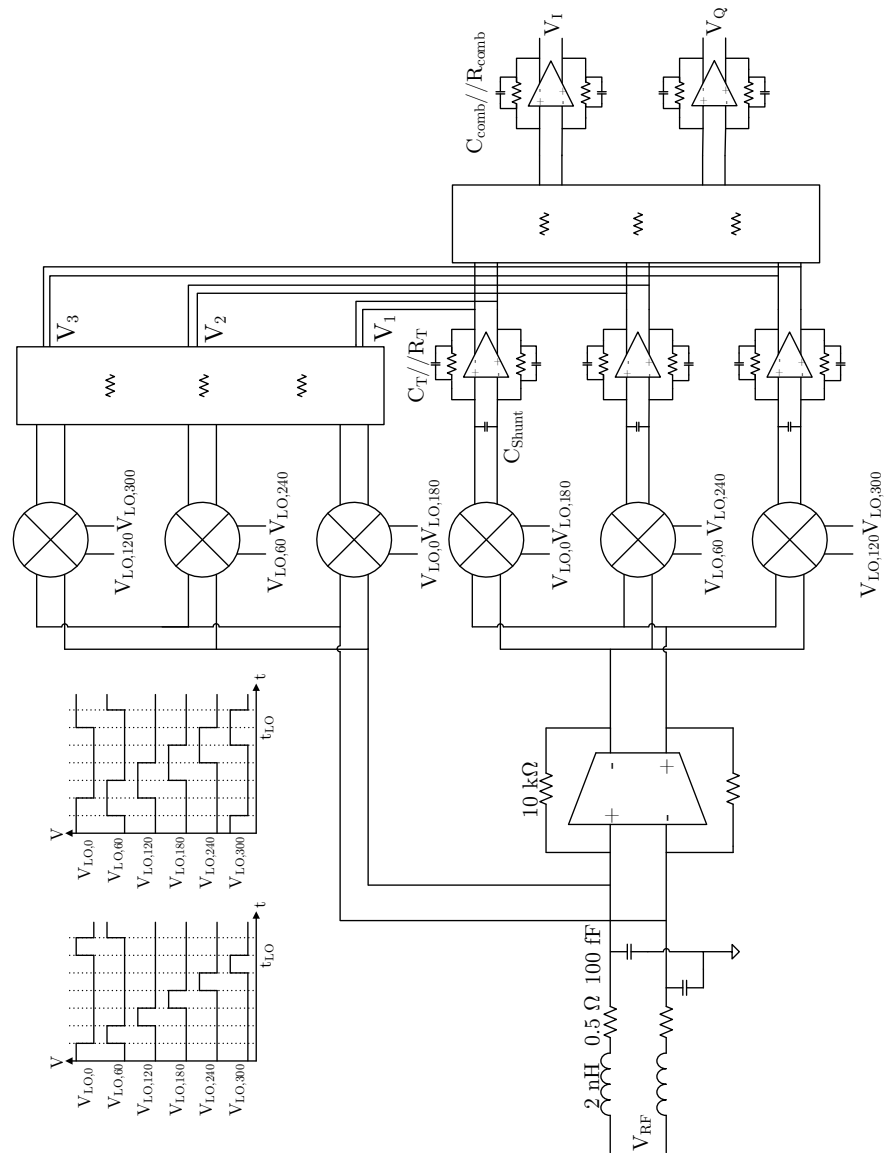
Since only two vectors need to be phase-shifted in the hybrid system the construction simplifies considerably. With the notation in 2.14 the equations of the desired vectors become:

$$\begin{aligned} V_{I,new} &= aV_I + bV_Q \\ V_{Q,new} &= aV_Q - bV_I \end{aligned} \quad (2.19)$$

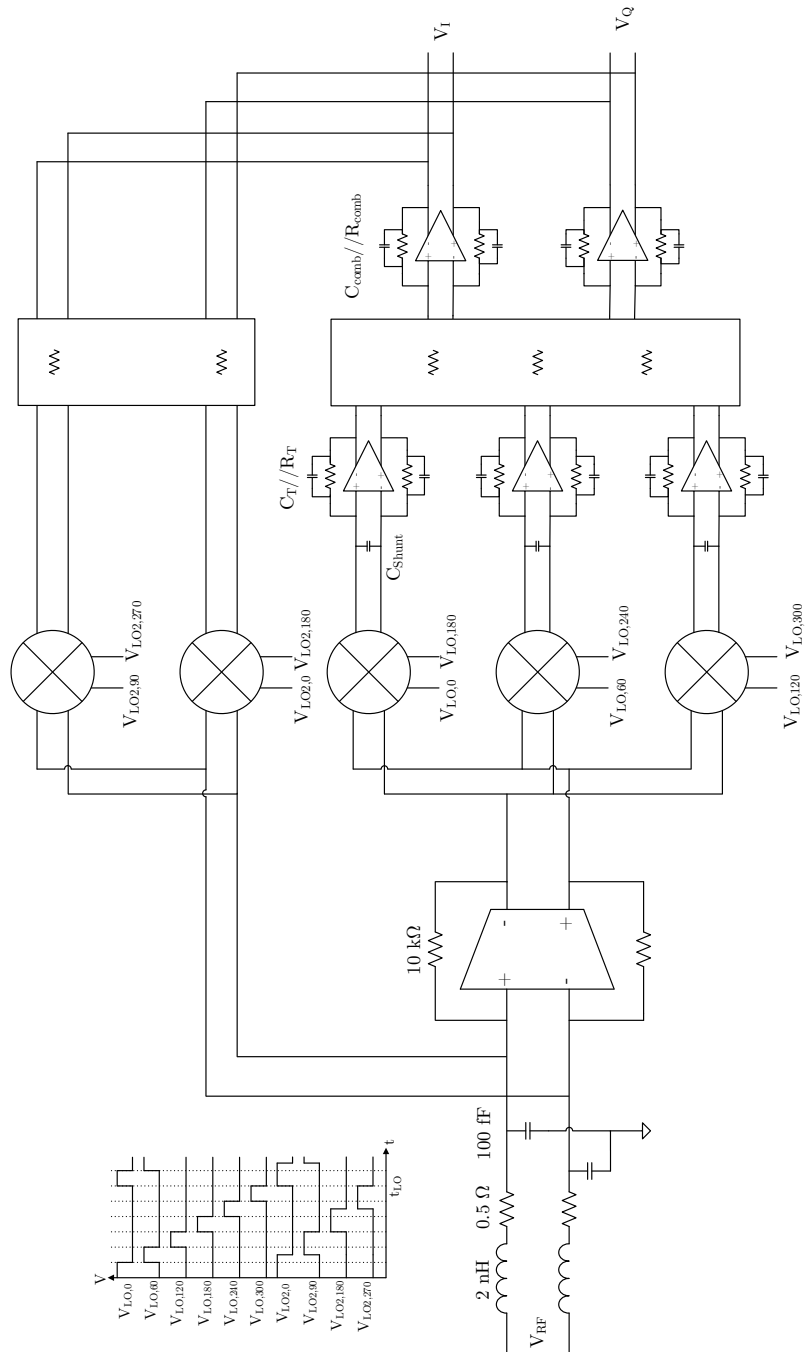
$$\phi = \arctan(b/a) \quad (2.20)$$

$$1 = a^2 + b^2 \quad (2.21)$$

The same angle restrictions apply to this system as the 6-phased system.



**Figure 2.15:** Full 6-phased system with bondwire and pad model at the input



**Figure 2.16:** Full hybrid system with bondwire and pad model at the input



Overall there are some topology choices that are consistent throughout the entire circuit. Most importantly, the system is fully, or pseudo differential which achieves automatic cancellation of all even-order harmonics and intermodulation products. This is, by definition, an improvement in linearity but also reduces overall noise figure since the eliminated harmonics would have added their own noise folding to the mixing stage.

Also present at many points are complementary stages. The complementary structure improves linearity because it, in presence of feedback, eliminates the need for bias transistors. This maximizes output voltage swing room at the price of reduced CMRR.

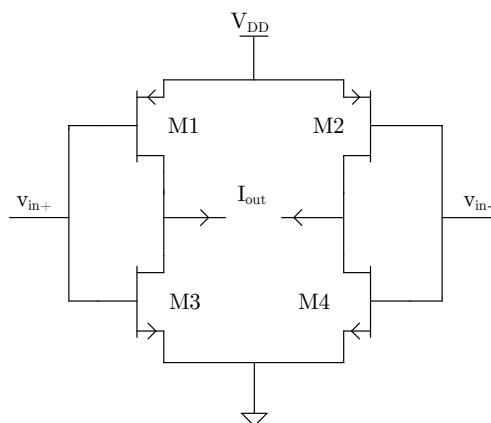
The test benches used to simulate the various figures and properties in this chapter can be found in appendix A.

All components have been designed to generate and work with a 600 mV common-mode DC voltage.

## 3.1 LNTA

The LNTA used is a differential and complementary CS stage and employs low-power standard low- $V_T$  transistors. This topology offers high linearity in accordance with what was discussed earlier in this chapter.

Self-biasing resistors are applied to give the amplifier a rudimentary form of common mode rejection. The resistor values are set to 10 k $\Omega$  which is high enough to not affect the output impedance and NF of the LNTA but low enough to allow the amplifier to recover from the common mode disturbances introduced by the mixers. Transistor sizing is a delicate balance between transconductance, power consumption, output impedance and bandwidth. A large transconductance is desired since it reduces the noise figure of the system in accordance to Friis's formula in equation (2.2) which is achieved by increasing the width of the transistors. This, however, leads to a deterioration of the other performance metrics. In practical circuits it is common to split the LNTA up in parallel cells that can be digitally enabled and disabled. This makes the circuit flexible and gives the possibility of letting the circuit adapt to unusually small or large input signals. As a normal case the transistor sizes in table 3.1 are used in this thesis. Using non-minimum



**Figure 3.1:** Transconductor circuit

length transistors only slightly increases output impedance but improves possible matching in a real, layout implemented circuit.

M1, M2 W/L	170/0.12 $\mu\text{m}/\mu\text{m}$
M3, M4 W/L	65/0.12 $\mu\text{m}/\mu\text{m}$
Transconductance (Diff.)	30 mS
Output impedance (Diff.)	440 $\Omega$
Current consumption	9.7 mA
Bandwidth	4.6 GHz

**Table 3.1:** Properties of the LNA

The frequency response of the LNTA and its IIP3 can be seen in figures 3.2 and 3.3 respectively.

## 3.2 Mixers

The mixers used are double-balanced passive NMOS mixers. The low input resistance of this type of mixer is key to achieve the frequency translation from baseband to RF and to maximize the current delivered to the TIA. The passive mixers will lead to a conversion gain that is less than unity in accordance with equation (3.1), where  $G_c$  denotes the conversion gain and  $D$  the duty cycle of the LO signals.

$$G_c = \frac{2}{\pi} \sin(\pi D) \quad (3.1)$$

Since the mixers are essentially only switches, they carry next to no DC-current under a rectangular LO drive, and hence there is no flicker noise present at the

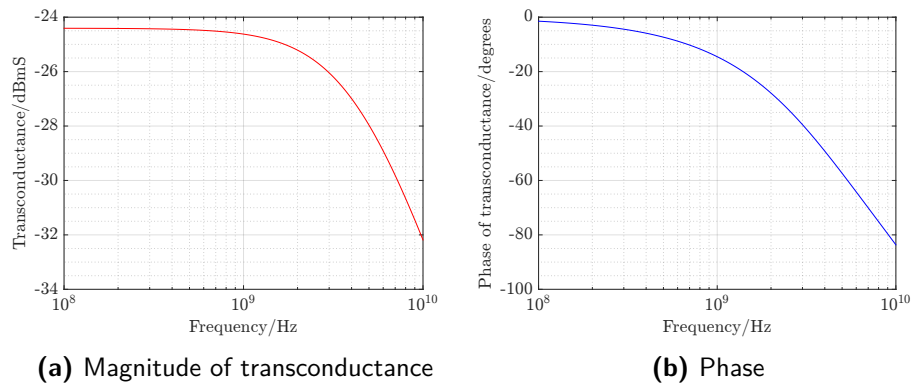


Figure 3.2: LNTA transfer characteristics

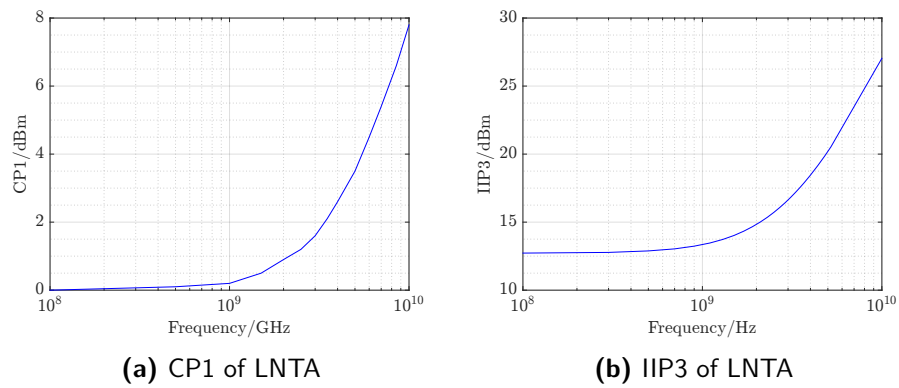
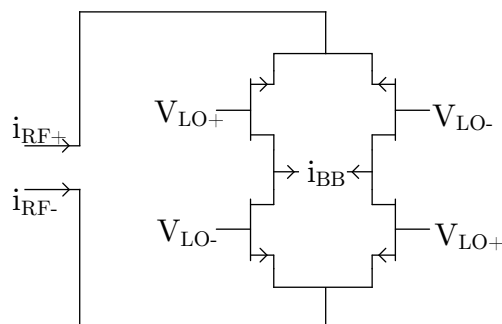


Figure 3.3: Linearity of LNTA



output port that would otherwise raise the noise figure considerably. The only noise that the mixers contribute is the channel thermal noise when the switches are on. In addition to this, the linearity is much higher than in an active mixer since every transistor is either fully on or off, and being in between only very short periods of time. NMOS transistors are used because of their higher gain and consequently higher switching speed and lower channel resistance. Sizing of the transistors is a delicate balance between switching speed, channel resistance, leakage and matching. The latter two can only be accurately checked if a full layout is completed along with Monte Carlo simulations. On account of long simulation times, these are not thoroughly investigated and sizes are instead set to  $W/L = 20/0.12 \mu\text{m}/\mu\text{m}$  which has been used before in a similar design [3]. To decrease channel resistance further, the mixers are driven between gate voltages of 0.6 and 1.8 V. Since the drain and source terminals of the mixers are biased at 0.6 V the maximum voltage rating of the transistor is not exceeded.



**Figure 3.4:** Double balanced passive mixer

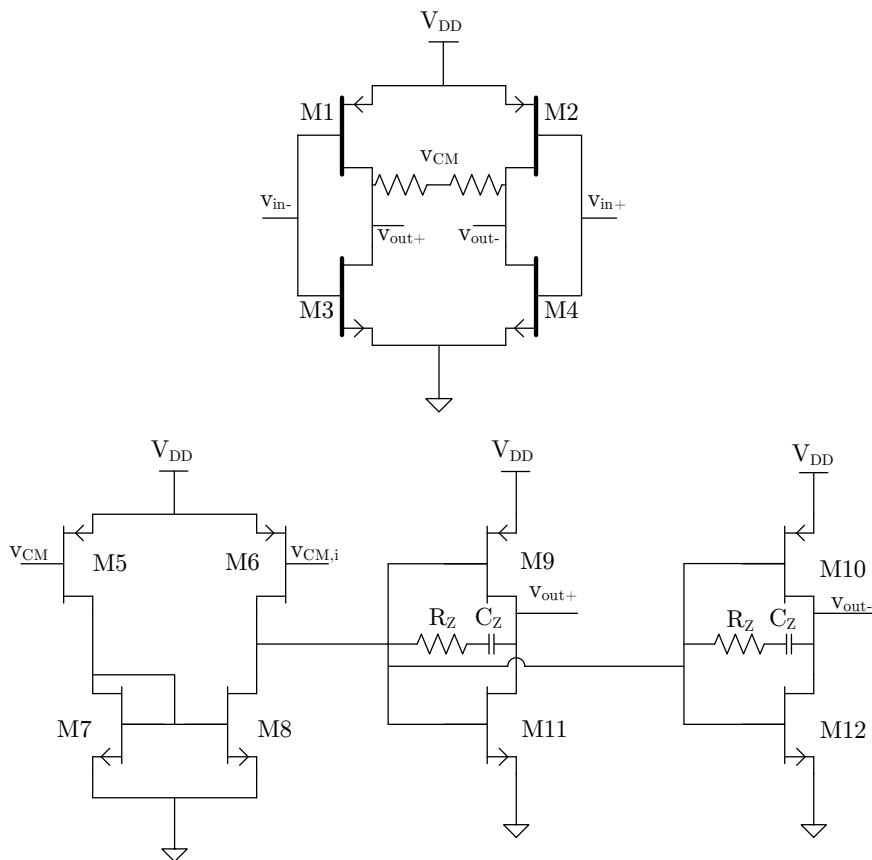
### 3.3 Amplifiers

The most straight-forward technique of improving the linearity performance of an amplifier is to increase its loop gain. The higher the gain of the open-loop amplifier is, the higher the loop-gain of the closed loop amplifier will be which directly improves linearity. In this particular system, it also improves the noise figure of the whole circuit. This is because higher gain also lowers the input impedance of the TIA and thus improving the current division between it and the LNTA's output impedance.

#### 3.3.1 Purely complementary amplifier

In the process used, transistors with thick oxide gates are available. These not only tolerate higher voltages but also lack the halo implants at the source and drain terminals that degrade the output impedance of the transistor [24]. Because of the higher output impedance the maximum intrinsic gain of the transistor,  $A_{v,max} =$

$g_m r_o$ , is increased. They also have much higher threshold voltages (about 450 mV) than normal transistors and are therefore biased close to sub-threshold. This leads to a high transconductance-to-current ratio, but also highly reduced bandwidth, and thanks to this a 1-stage amplifier might be a viable option. Using only one stage improves the noise performance of the amplifier and if designed correctly it can also increase the linearity. The amplifier in figure 3.5 was designed and a



**Figure 3.5:** Purely complementary amplifier with CMFB-amplifier at the bottom

common-mode feedback amplifier consisting of a CS-stage cascaded with inverters was put in. While the amplifier achieves 30 dB of gain under ideal conditions (large load impedance) its performance is reduced in the real circuit. This is because the global feedback resistance and the input impedance of the combining amplifier are in the same order of magnitude as the output impedance of the TIA. In a receiver lacking the global feedback this would not be an issue as a designer is free to use any input resistance to the combiner amplifiers. Setting them very high would enable high gain at the price of slightly increased noise. The feedback resistance, however,

M1, M2 W/L	170/1 $\mu\text{m}/\mu\text{m}$
M3, M4 W/L	65/1 $\mu\text{m}/\mu\text{m}$
M5, M6 W/L	10/0.28 $\mu\text{m}/\mu\text{m}$
M7, M8 W/L	5/0.28 $\mu\text{m}/\mu\text{m}$
M9, M10 W/L	20/0.28 $\mu\text{m}/\mu\text{m}$
M11, M12 W/L	10/0.28 $\mu\text{m}/\mu\text{m}$
$R_Z, C_Z$	500 $\Omega$ , 500 fF
Output impedance (Diff.)	26 k $\Omega$
Open-Loop gain	29.7 dB
Current consumption	590 $\mu\text{A}$
Open-Loop bandwidth	22 MHz

**Table 3.2:** Properties of purely complementary amplifier in figure 3.5

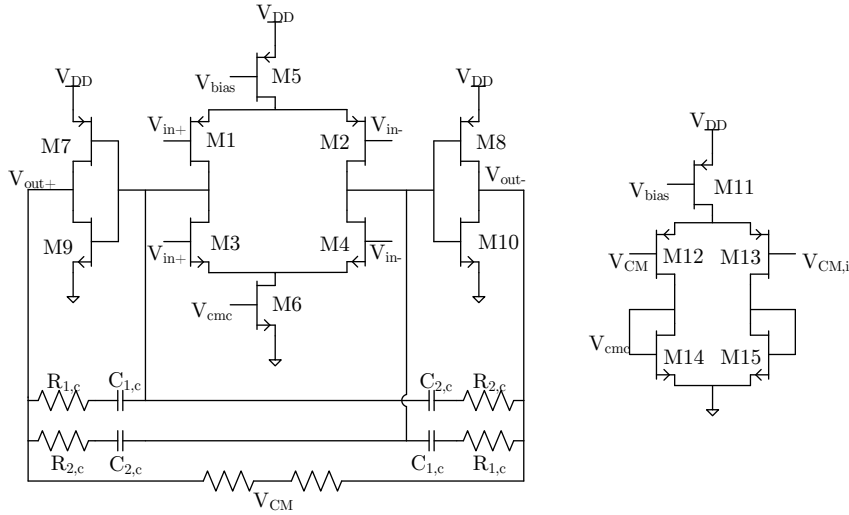
is set by the impedance matching value and the gain of the receiver chain and the effective gain of the amplifier is therefore dramatically reduced which makes it unusable.

### 3.3.2 Complementary amplifier with tail current source

From the impedance related failure of the amplifier in the previous section, the conclusion can be drawn that another stage is needed in order to keep the gain. Adding another complementary stage with its own local common-mode feedback loop does not work, however. This is because the amplifier in the real system has feedback and when two inverting stages are used this feedback automatically becomes positive, inevitably leading to common-mode oscillations. This can be solved by adding a transistor that ensures that the first stage common-mode is non-inverting. A tail-current source also raises the CMRR enough to enable the elimination of the local loop at the output. The circuit is first implemented with standard transistors which has been used in an existing design and is illustrated in figure 3.6 [16, p. 34].

In order to boost gain even more, another version, referred to as the second amplifier, is tested with M1-M4 implemented as thick oxide transistors in the input stage. Due to their high threshold voltages the input stage is therefore put in the sub-threshold region. In this region the transistor behaves like a bipolar transistor which intrinsically has higher transconductances and output impedances than MOSFETs, which increases the gain from 60 dB to 71 dB all the while consuming less current. The price for this is reduced open-loop bandwidth by a factor of 10, but since the entirety of this reduction takes place in the first stage no compensation is needed. This is not necessarily a problem per se since the feedback improves the bandwidth of the amplifier and the smallest pole present in the closed-loop system will be the one in the feedback. As will be evident later the out-of-band linearity suffers a large penalty, however.

The IIP3, with the component values in figure A.2, of the two different am-

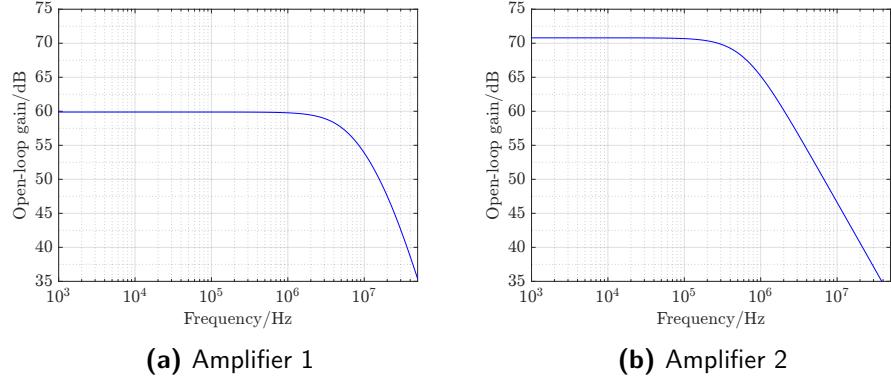


**Figure 3.6:** Schematic of OP-amp with CMFB-amp to the right.

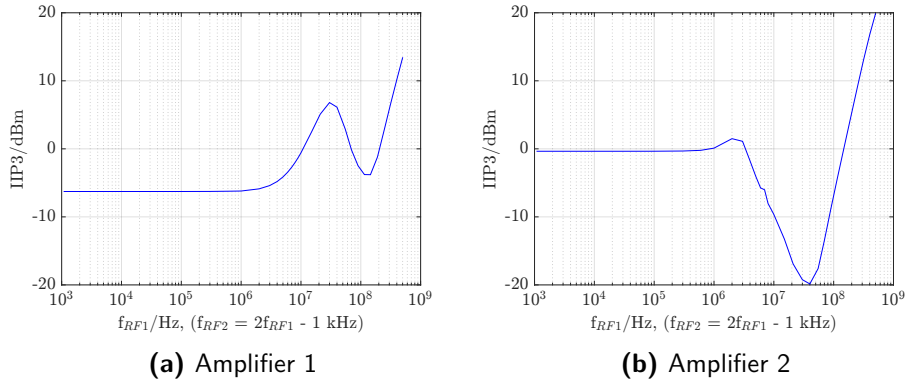
	Amplifier 1	Amplifier 2
M1, M2 W/L	80/0.25 $\mu\text{m}/\mu\text{m}$	50/0.5 $\mu\text{m}/\mu\text{m}$
M3, M4 W/L	120/0.25 $\mu\text{m}/\mu\text{m}$	125/0.5 $\mu\text{m}/\mu\text{m}$
M5 W/L	120/0.4 $\mu\text{m}/\mu\text{m}$	120/0.4 $\mu\text{m}/\mu\text{m}$
M6 W/L	40/0.4 $\mu\text{m}/\mu\text{m}$	40/0.4 $\mu\text{m}/\mu\text{m}$
M7, M8 W/L	150/0.25 $\mu\text{m}/\mu\text{m}$	150/0.25 $\mu\text{m}/\mu\text{m}$
M9, M10 W/L	50/0.25 $\mu\text{m}/\mu\text{m}$	50/0.25 $\mu\text{m}/\mu\text{m}$
M11 W/L	11/0.4 $\mu\text{m}/\mu\text{m}$	11/0.4 $\mu\text{m}/\mu\text{m}$
M12, M13 W/L	3/0.25 $\mu\text{m}/\mu\text{m}$	3/0.25 $\mu\text{m}/\mu\text{m}$
M14, M15 W/L	2/0.4 $\mu\text{m}/\mu\text{m}$	2/0.4 $\mu\text{m}/\mu\text{m}$
$R_{1,c}, C_{1,c}$	250 $\Omega$ , 800 fF	Uncompensated
$R_{2,c}, C_{2,c}$	1 k $\Omega$ , 800 fF	Uncompensated
$V_{bias}$	670 mV	750 mV
Open-Loop gain	60 dB	71 dB
Open-Loop bandwidth	6.0 MHz	610 kHz
Current consumption	2.3 mA	2.1 mA

**Table 3.3:** Properties of amplifier in 3.6

plifiers is shown in figure 3.8 and the open-loop gain in figure 3.7. It is obvious from the figure that the in-band linearity of the second amplifier is a couple of dB higher than the first. Because of the reduced bandwidth of the open-loop amplifier the loop gain drops dramatically around 1 MHz and hits bottom at an abysmal



**Figure 3.7:** Gains of the amplifiers as a function of input frequency



**Figure 3.8:** IIP3s of amplifiers as a function of offset frequency

-20 dBm at 40 MHz. In FDD systems this is one possible frequency, relative to the carrier frequency, at which the transceiver will send information. Since no duplexer is perfect some of it will leak to the receiver side. And since the transmitting power is often orders of magnitude larger than what is received, high linearity is the most crucial at this frequency. The second amplifier is therefore useless in this system.

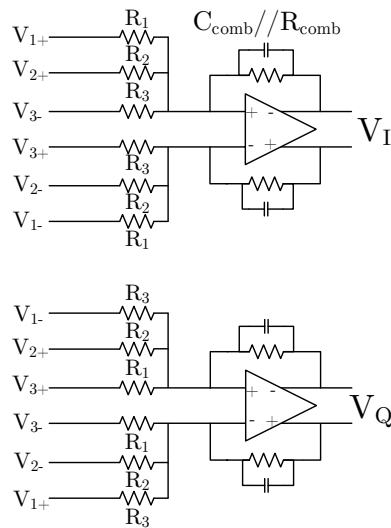
### 3.3.3 Combiner amplifier

In order to achieve harmonic rejection the different voltages need to be combined in accordance with the equations in (2.13). This is done by the simple combining amplifiers in figure 3.9. The component gain of this configuration is  $A_i = -R_{comb}/R_i$ .

The most important ratio to keep is the one between the input resistors since any deviation will lead to a reduction of the HRR of the architecture. To keep linearity  $R_{comb}$  is set so that total gain is unity which sets the ratio between it and the input resistors. While all the ratios are set the actual values are not and are

the subject of a trade-off between noise, linearity and impedance matching. The amplifier's input impedance is simply  $R_{in} = R_i$  and should be as large as possible in order to take as much of the voltage as possible in the division between it and the preceding stage's output impedance. This output impedance is on the order of 5 k $\Omega$ , and setting  $R_i$  much higher than this doesn't help and will incur a penalty in the linearity and noise performance of the output stage.

A small capacitor is connected in the feedback loop to provide additional filtering and to improve the out-of-band linearity. The pole is placed higher in frequency than the transimpedance pole so that overall system bandwidth is not affected too much.



**Figure 3.9:** Harmonic rejection combination amplifiers

The values of the components along with the feedback pole frequency are listed in table 3.4. The reason for the pole being significantly higher in frequency than the bandwidth of the system is that it leads to a smaller system gain reduction at higher frequencies and thus to a lower increase in the NF of the system.

### 3.4 Phase shifting network

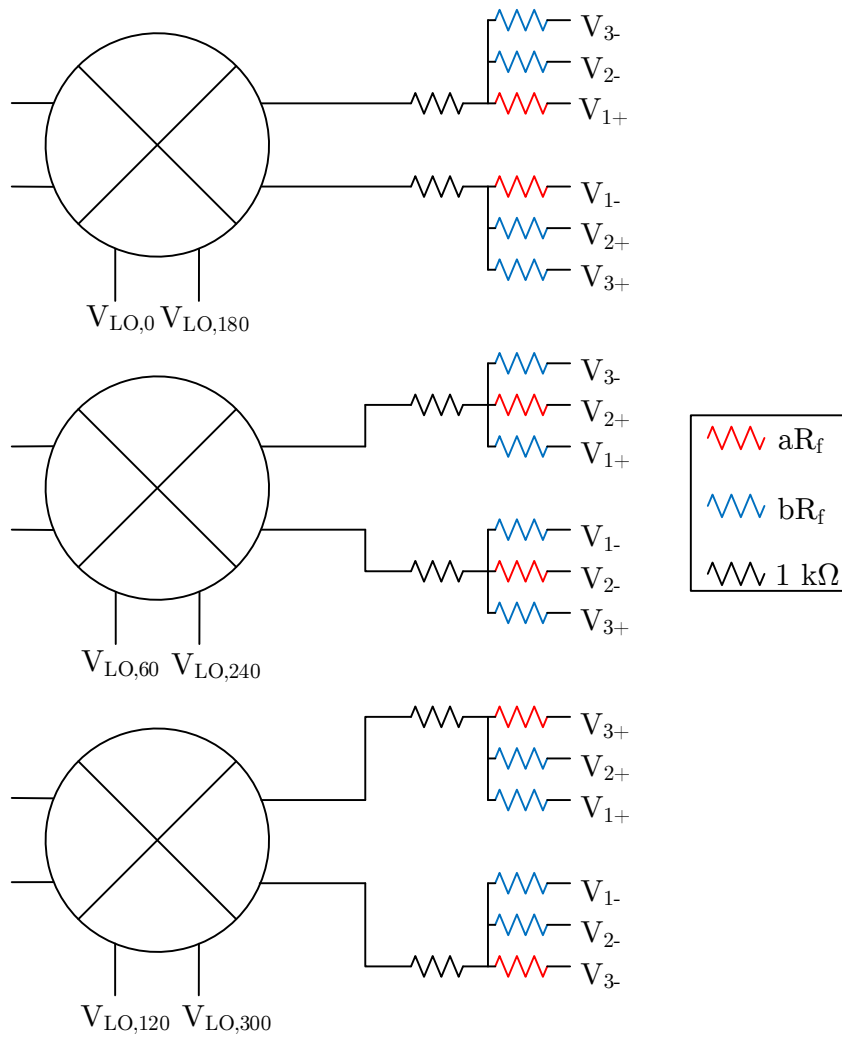
To implement the first phase shifting compensation described in section 2.4 the resistance network in figure 3.10 is used. Voltage vectors with phases differing 60° from each other are available. The idea is that an arbitrary feedback phase can be achieved by adding the different phases with varying proportions. This is implemented by adding two extra parallel resistors to the normal feedback resistors to make every phase connect to each mixer in the feedback path. Which phase is input to the mixers is controlled by the proportions between the resistors in

Component	Value
$R_{comb}$	6 k $\Omega$
$R_1$	7 k $\Omega$
$R_2$	9.5 k $\Omega$
$R_3$	26 k $\Omega$
$C_{comb}$	600 fF
$\frac{1}{2\pi R_{comb} C_{comb}}$	44 MHz

**Table 3.4:** Values of combiner amplifier resistors

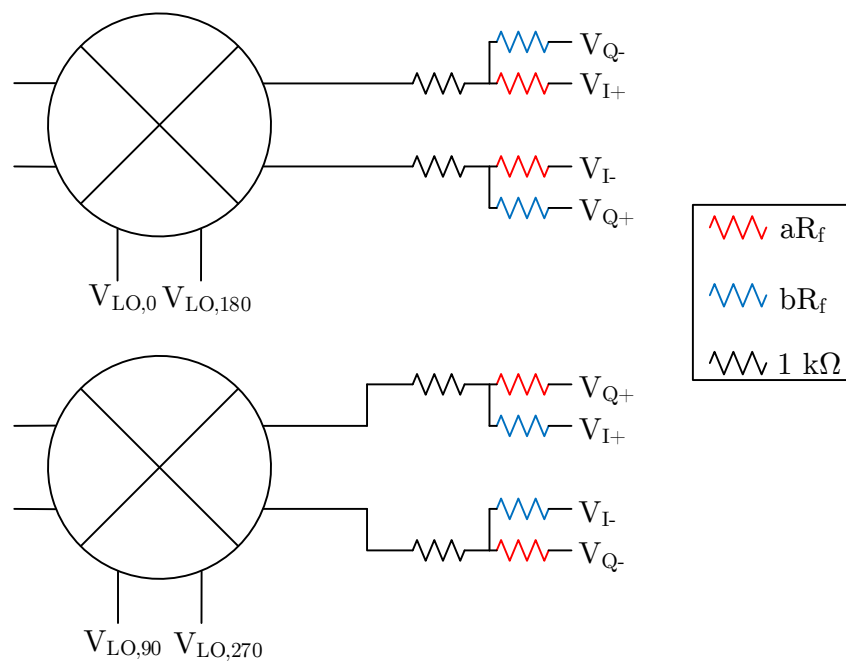
accordance with equations (2.16). What is actually fed back are current vectors that are the division between the available voltage vectors and the resistance, implying that the amount of signal fed back is proportional to the inverse of the resistance. Looking into any mixer branch, the effective resistance will be lowered by the added parallel resistance and so the average resistance value needs to be proportionally increased to keep the impedance matching intact.

The phase shifter for the hybrid system is implemented in an analogous way to first one and can be seen in figure 3.11. Here only two mixers are used however which simplifies the design. This approach has a significant drawback compared to the other in that it requires both 16% and 25% duty cycle LO waves. This adds a fair amount of complexity to the oscillator design and could raise the power consumption of it considerably.



**Figure 3.10:** Global feedback phase shifting network





**Figure 3.11:** Global feedback phase shifting network in the hybrid system

---

## System simulation results

---

This chapter deals with simulations on the system as a whole to investigate the impact of the architectural choices on performance. Complete system schematics can be found in appendix A. Unless anything else is given, these are the configurations that are used during simulations. Note that a model of a bondwire and pad has been included in the system models so that a more realistic estimate to the performance of an eventual fabricated circuit is obtained.

Component	Value
$C_{Shunt}$	5 pF
$R_T$	4 k $\Omega$
$C_T$	2.2 pF
$R_{Comb}$	6 k $\Omega$
$C_{Comb}$	600 fF

**Table 4.1:** Values of system critical variables

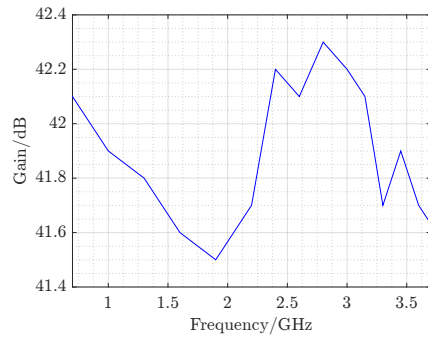
A periodic steady state (PSS) simulation is used as a baseline simulation for all figures. The shooting engine is used for all metrics except for the linearity measures which uses the harmonic balance engine to reduce simulation time.

### 4.1 Quadrature system

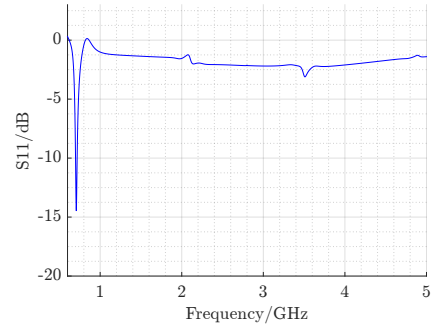
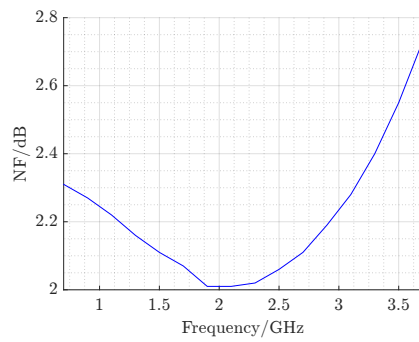
The quadrature system in figure 2.12 serves as a baseline example to which the other systems will be compared. Simulations for gain, matching, noise and linearity are run without adjusting for the phase errors of the forward path and the results can be seen in figure 4.1.

Ripples can be seen in the S11 around 2.1 and 3.5 GHz, corresponding to the 3rd and 5th overtones to the LO fundamental. This shows that the levels of the harmonics are high enough to actually make the receiver input sensitive to harmonic blockers.

There is a strong dip in the IIP3 around 100 MHz which can be traced back to the individual amplifier's IIP3 in figure 3.8. It is however much smaller, around 4 dB, for the full system compared to almost 10 dB for the single amplifier.



(a) Gain versus LO frequency

(b) S11 versus frequency when  $f_{LO} = 700 \text{ MHz}$ 

(c) Noise figure versus frequency

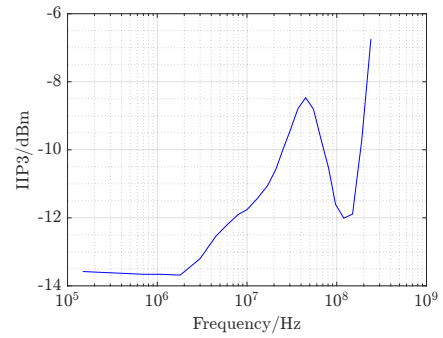
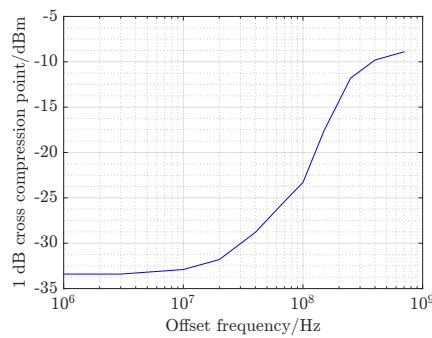
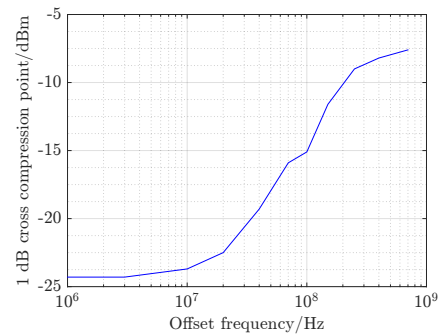
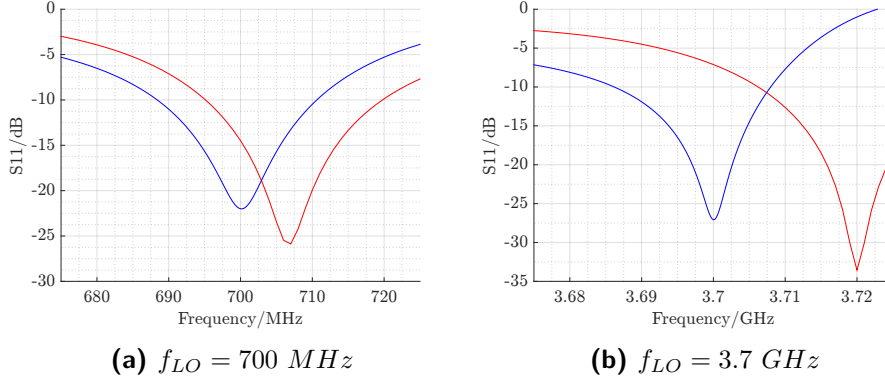
(d) IIP3 versus offset frequency from  $f_{LO} = 1 \text{ GHz}$ (e) Compression point versus offset frequency from  $f_{LO} = 1 \text{ GHz}$ (f) 3rd order harmonic tolerance versus offset frequency from  $3f_{LO} = 3 \text{ GHz}$ 

Figure 4.1: Various characteristics of the quadrature system



**Figure 4.2:** S11 with phase-shifting feedback turned on (blue) and off (red)

## 4.2 Full 1/6 duty cycle system

### 4.2.1 Resistor tuning and performance

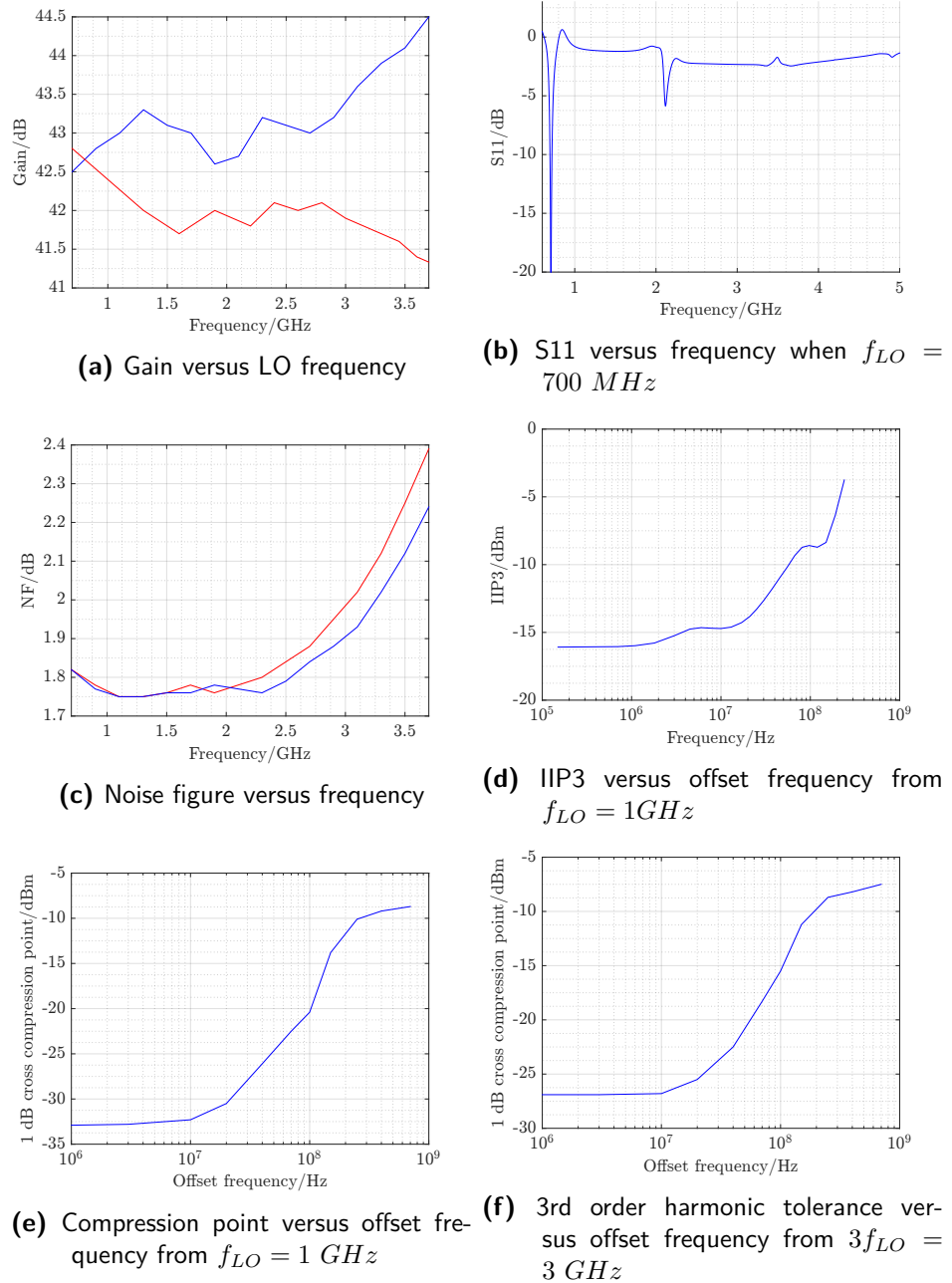
There are possible configurations of the resistor feedback to push the matching peak into the correct position for all frequencies of interest, which figure 4.2 shows for carrier frequencies of 700 MHz and 3.7 GHz.

Using the names from figure 3.10, the easiest method of tuning the resistors is keeping  $a$  constant at  $a = 1$  while figuring out how big the phase shift,  $\phi$ , needs to be.  $b$  can then be calculated as  $b = \frac{\sqrt{3}a}{\tan(\phi)}$ , and to compensate for the lower equivalent resistance mentioned in section 3.4,  $R_f$  is increased until good matching is achieved. Optimal resistor values and angles for a couple of frequencies are displayed in table 4.2

One of the purposes of the adjustment network is to improve the noise performance of the system and therefore the noise figure of both the unadjusted and the adjusted system is simulated. It and other performance characteristics can be seen in figure 4.3. From this we see that the improvement only occurs in the higher frequency range of operation and that the adjustment also causes a slight peaking in the system's transfer function. The peaking is likely caused by non-real poles in the system transfer function. No real frequency compensation is performed for the whole system and the effect is boosted by the phase shifter. The peaking is not necessarily a problem but the increased gain might lead to a reduction of the linearity at the affected frequencies. It is possible to compensate for this, however, by lowering the transimpedance.

One reason for the non-improvement in noise at lower frequencies is that while the matching peak is pushed to the right place, the S11 of the unadjusted system is still around -15 dB at the tested frequency according to figure 4.2. For a fabricated circuit it is unlikely however, based on another system [3], that matching will be that exact and an improvement at lower frequencies can therefore still be expected.

Compared to the quadrature system, there is an improvement of the noise



**Figure 4.3:** Various characteristics of the full 16% system. With feedback compensation in blue and without in red

Frequency/GHz	$\phi/^\circ$	$b$	$R_f/\Omega$
0.7	21	4.5	4000
0.9	21	4.5	4000
1.1	21	4.5	4000
1.3	21	4.5	4000
1.5	21	4.5	4000
1.7	21	4.5	4500
1.9	22	4.3	4500
2.1	23	4.1	5000
2.3	25	3.7	6000
2.5	28	3.3	6000
2.7	31	2.9	6000
2.9	34	2.6	6500
3.1	38	2.2	7000
3.3	43	1.9	7000
3.5	48	1.6	7200
3.7	53	1.3	7500

**Table 4.2:** Optimal resistor values for the global feedback in figure 3.10

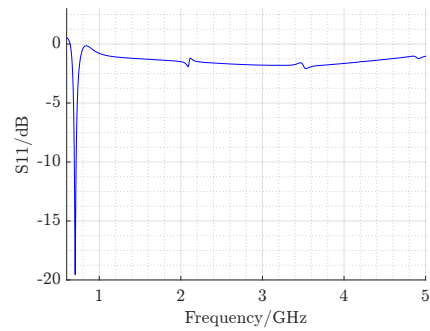
figure between 0.2 and 0.5 dB depending on frequency of operation which can be attributed to the harmonic rejection architecture. The 16% system also has a slightly improved compression and out-of-band intercept point but worse in-band intercept point. The increased level of the 3rd harmonic in the LO-signals, as shown in section 2.3, can be seen in the wideband S11 since no harmonic rejection is present in the nodes that are fed back to the input, and leads to a lower tolerance to 3rd order harmonic blockers.

#### 4.2.2 Impact of 33% duty cycle

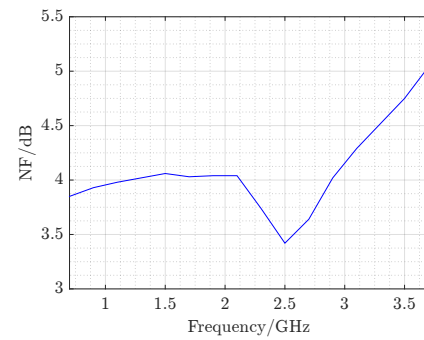
Due to the low tolerance to a 3rd order blocker the system in 2.15 is also tested with 33% duty cycle LO signals. Matching, linearity and noise performance can be seen in figure 4.4. The gain of the system is about 40 dB.

The lack of a 3rd harmonic component in the LO signal is evident from the vast reduction of the matching peak at that frequency compared to the full 16% system and the fact that the blocker tolerance is vastly increased. The slight ripples that still exist in the S11 may be caused by non-zero rise time of the LO waves. The now overlapping LO signals also leads to an increase of the noise figure by a tremendous 2-2.5 dB. 1st order compression is also slightly increased due to the lower gain of the system.

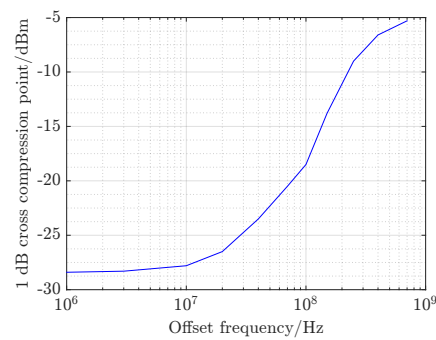
Due to excessive simulation time, no IIP3 is simulated for the 33% system.



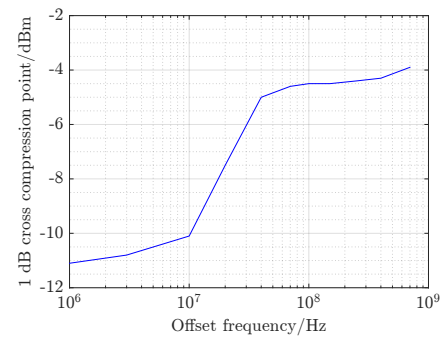
(a) S11 versus frequency when  $f_{LO} = 700 \text{ MHz}$



(b) Noise figure versus frequency



(c) Compression point versus offset frequency from  $f_{LO} = 1 \text{ GHz}$



(d) 3rd order harmonic tolerance versus offset frequency from  $3f_{LO} = 3 \text{ GHz}$

**Figure 4.4:** Various characteristics of the 33% system

### 4.3 Hybrid system

The resistor tuning method in section 4.2.1 is reapplied to the hybrid system successfully and the proper values can be found in table 4.3.

Frequency/GHz	$\phi/^\circ$	$b$	$R_f/\Omega$
0.7	15	3.7	4000
0.9	15	3.7	4000
1.1	15	3.7	4000
1.3	15	3.7	4000
1.5	15	3.7	4000
1.7	15	3.7	4500
1.9	16	3.5	5000
2.1	17	3.3	5500
2.3	18	3.1	6000
2.5	19	2.9	6000
2.7	21	2.6	6500
2.9	25	2.1	6500
3.1	29	1.8	7000
3.3	33	1.5	7000
3.5	37	1.3	7500
3.7	42	1.1	7500

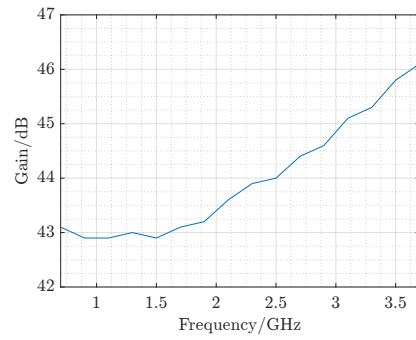
**Table 4.3:** Optimal resistor values for the global feedback in figure 3.11

The results of the simulations on the hybrid system can be seen in figure 4.5. Note that the systems are only run for the compensated system. Notably the noise figure is the lowest of all the systems tested in this thesis, dropping under 1.3 dB in the mid-band and the linearity is similar to the full 16 % system albeit with a slightly lower tolerance to harmonic blockers.

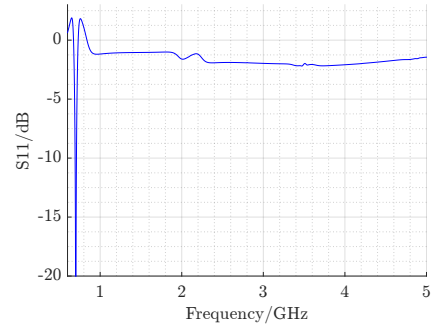
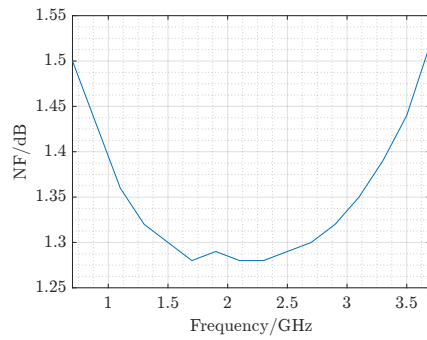
The S11 of the hybrid system is the smoothest of all systems tested. This is because it is the only system in which the signals fed back come from the output of the harmonic rejection combination amplifiers. This does not lead to a higher blocker tolerance unfortunately since a harmonic blocker can still manifest itself as a voltage at the output of the TIAs.

Even stronger peaking is present in the gain function of the system than in the full 16% system. Having an additional amplifier in the loop compared to the 16% system leads to a larger phase shift in the forward path which enlarges the phenomenon.





(a) Gain versus LO frequency

(b) S11 versus frequency when  $f_{LO} = 700 \text{ MHz}$ 

(c) Noise figure versus frequency

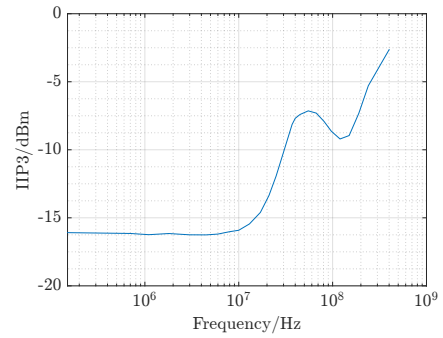
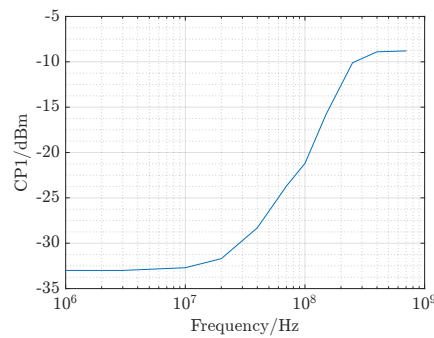
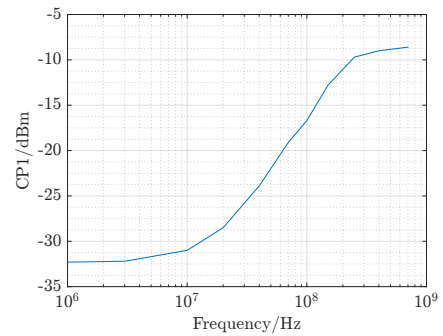
(d) IIP3 versus offset frequency from  $f_{LO} = 1 \text{ GHz}$ (e) Compression point versus offset frequency from  $f_{LO} = 1 \text{ GHz}$ (f) 3rd order harmonic tolerance versus offset frequency from  $3f_{LO} = 3 \text{ GHz}$ 

Figure 4.5: Various characteristics of the hybrid system

---

## Conclusion

---

Summarized in table 5.1 and figure 5.1 are some of the performance metrics presented in chapter 4 for closer comparison. It is easily seen that the hybrid system is the superior system in terms of raw performance if the problems of implementing a mixed duty cycle oscillator can be solved. Compared to the other systems, the noise is lower and the linearity is very similar. One may interject that the blocker tolerance is lower which is true but matters very little since additional filtering is required for every system tested. Harmonic blockers can deliver powers of up to 10 dBm which is enough to desensitize even the 16% system ran with 33% LO-signals by a large margin.

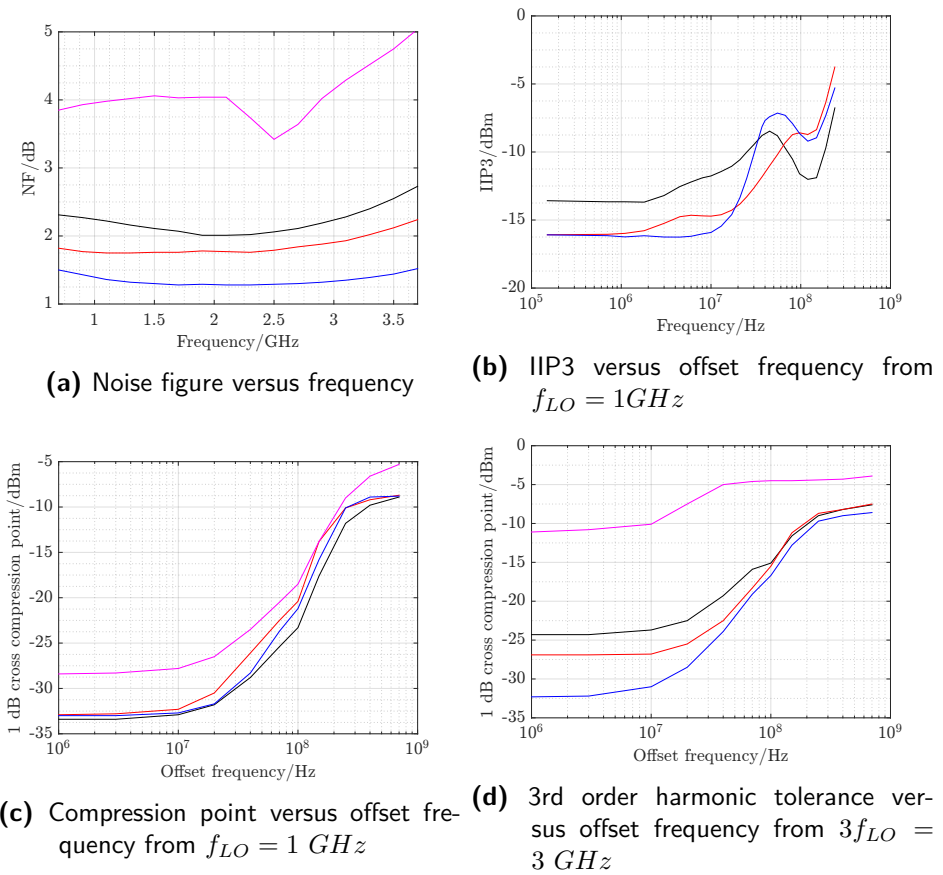
It terms of performance/power it is remarkable that the noise performance can be increased by up to 0.8 dB by adding only one amplifier with an extra current consumption of 2.3 mA. In reality the oscillators of these systems will have a higher power consumption though because of increased complexity in the circuitry and a larger load in the form of 5 or 6 mixers instead of 4. This improvement also comes with no reduction, but a small increase, in linearity as well.

System	Quadrature	Full 16%	33%	Hybrid
Gain	42	43	40	43
Noise figure/dB	2.25	1.75	3.95	1.40
IIP3/dBm	-11	-9	N/A	-7.9
CP1/dBm	-25	-21	-20	-23
3rd order tolerance/dBm	-24	-27	-11	-32
Current consumption/mA	18.9	21.2	21.2	21.2

**Table 5.1:** Final system metrics. All measured at 1 GHz and an 80 MHz offset where applicable. 3rd order blocker tolerance at zero offset

Linearity in absolute terms is rather low which can be attributed to the focus on optimizing the design for noise performance. Bandwidths of the low-pass filters in both TIAs and combiner amplifiers can be decreased to increase the linearity at the price of noise performance.

Overall the hybrid system is a suitable candidate for further research, optimization and eventually a full layout and verification of a fabricated circuit.



**Figure 5.1:** Various characteristics of all systems compared. Quad system in black, 33% system in magenta, 16% system in red and hybrid system in blue

## 5.1 Future work

### 5.1.1 Noise-cancelling path

An auxiliary forward path can be added in parallel to the main path. By carefully tuning the transconductance and transimpedance, noise sources from both paths that are correlated can be canceled [3]. While this can considerably reduce noise figure and increase the linearity it requires another LNTA and at least three additional amplifiers if the harmonic rejection technique in this thesis is used. This, together with the larger load on whatever oscillator is used, will considerably raise the power consumption of the system.

### 5.1.2 Full 16 % system with feedback of Quadrature signals

Another way of feeding back the output signals to the input is to synthesize waveforms phase-shifted  $60^\circ$  from one another using the output quadrature signals and a larger resistor network in the feedback. This way the problem of implementing a dual duty-cycle oscillator is eliminated while still possibly retaining all the positive features of the hybrid system.



---

## References

---

- [1] 3GPP TS 36.101 V12.5.0 (2014-11), “User Equipment (UE) radio transmission and reception (Release 12).”
- [2] S. Asaad Wahba Marzouk, F. Hussien, and A. Shousha, “A 3db nf 0.1-6.6ghz inductorless wideband low-noise amplifier in 0.13 um cmos,” in *Circuits and Systems (MWSCAS), 2014 IEEE 57th International Midwest Symposium on*, pp. 953–956, Aug 2014.
- [3] A. Nejedel, H. Sjoland, and M. Tormanen, “A noise-cancelling receiver front-end with frequency selective input matching,” *Solid-State Circuits, IEEE Journal of*, vol. 50, pp. 1137–1147, May 2015.
- [4] F. Belmas, F. Hameau, and J. Fournier, “A 1.3mw 20db gain low power inductorless lna with 4db noise figure for 2.45ghz ism band,” in *Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE*, pp. 1–4, June 2011.
- [5] T.-K. Nguyen, S.-G. Lee, and D.-K. Kang, “A 900 mhz cmos rf direct conversion receiver front-end with 3-db nf and 30-khz 1/f noise corner,” in *Asian Solid-State Circuits Conference, 2005*, pp. 349–352, Nov 2005.
- [6] Y. Feng, G. Takemura, S. Kawaguchi, and P. Kinget, “Design of a high performance 2-ghz direct-conversion front-end with a single-ended rf input in 0.13  $\mu$  m cmos,” *Solid-State Circuits, IEEE Journal of*, vol. 44, pp. 1380–1390, May 2009.
- [7] I. ud Din, J. Wernehag, S. Andersson, S. Mattisson, and H. Sjoland, “Wideband saw-less receiver front-end with harmonic rejection mixer in 65-nm cmos,” *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 60, pp. 242–246, May 2013.
- [8] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2004.
- [9] A. Abidi, “Direct-conversion radio transceivers for digital communications,” *Solid-State Circuits, IEEE Journal of*, vol. 30, pp. 1399–1410, Dec 1995.
- [10] B. Razavi, “Design considerations for direct-conversion receivers,” *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 44, pp. 428–435, Jun 1997.

- 
- [11] S. Rodriguez and A. Rusu, "A 65nm cmos current-mode receiver front-end," in *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on*, pp. 530–533, May 2011.
- [12] D. Murphy, M. Mikhemar, A. Mirzaei, and H. Darabi, "Advances in the design of wideband receivers," in *Custom Integrated Circuits Conference (CICC), 2013 IEEE*, pp. 1–8, Sept 2013.
- [13] C.-k. Luo, P. S. Gudem, and J. F. Buckwalter, "0.4-6 ghz,17-dbm b1db, 36-dbm iip3 channel-selecting, low-noise amplifier for saw-less 3g/4g fdd receivers," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2015 IEEE*, pp. 299–302, May 2015.
- [14] S. Hu, W. Li, Y. Huang, and Z. Hong, "Design of a high-linearity rf front-end with ip2 calibration for saw-less wcdma receivers," in *ASIC (ASICON), 2011 IEEE 9th International Conference on*, pp. 1090–1093, Oct 2011.
- [15] H. Friis, "Noise figures of radio receivers," *Proceedings of the IRE*, vol. 32, pp. 419–422, July 1944.
- [16] A. Nejdell, *Flexible Receivers in CMOS for Wireless Communication*. PhD thesis, Faculty of Engineering, Lund University, 2015.
- [17] M. K. Lenka, A. Agrawal, V. Khatri, and G. Banerjee, "A wide-band receiver front-end with programmable frequency selective input matching," in *2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID)*, pp. 168–173, Jan 2016.
- [18] D. Murphy, H. Darabi, and H. Xu, "3.6 a noise-cancelling receiver with enhanced resilience to harmonic blockers," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, pp. 68–69, Feb 2014.
- [19] J. Weldon, R. Narayanaswami, J. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and P. Gray, "A 1.75-ghz highly integrated narrow-band cmos transmitter with harmonic-rejection mixers," *Solid-State Circuits, IEEE Journal of*, vol. 36, pp. 2003–2015, Dec 2001.
- [20] H.-K. Cha, S.-S. Song, H.-T. Kim, and K. Lee, "A cmos harmonic rejection mixer with mismatch calibration circuitry for digital tv tuner applications," *Microwave and Wireless Components Letters, IEEE*, vol. 18, pp. 617–619, Sept 2008.
- [21] A. Rafi, A. Piovaccari, P. Vancorenland, and T. Tuttle, "A harmonic rejection mixer robust to rf device mismatches," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, pp. 66–68, Feb 2011.
- [22] A. Nejdell, M. Tormanen, and H. Sjoland, "A 0.7 to 3.7 ghz six phase receiver front-end with third order harmonic rejection," in *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, pp. 279–282, Sept 2013.

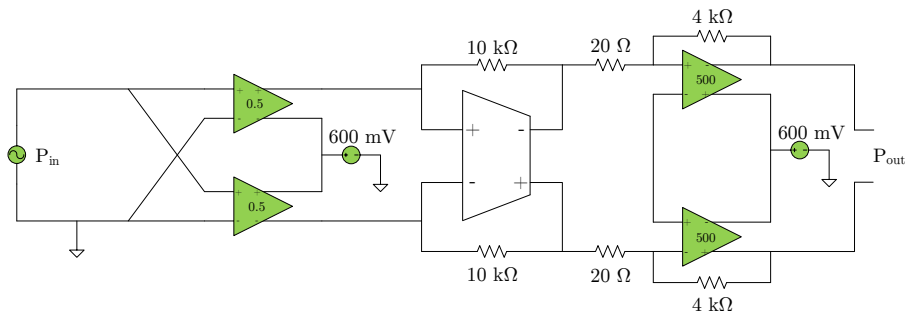
- 
- [23] Z. Ru, E. Klumperink, G. Wienk, and B. Nauta, "A software-defined radio receiver architecture robust to out-of-band interference," in *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, pp. 230–231,231a, Feb 2009.
- [24] S. Mudanai, W. kai Shih, R. Rios, X. Xi, J.-H. Rhew, K. Kuhn, and P. Packan, "Analytical modeling of output conductance in long-channel halo-doped mosfets," *Electron Devices, IEEE Transactions on*, vol. 53, pp. 2091–2097, Sept 2006.



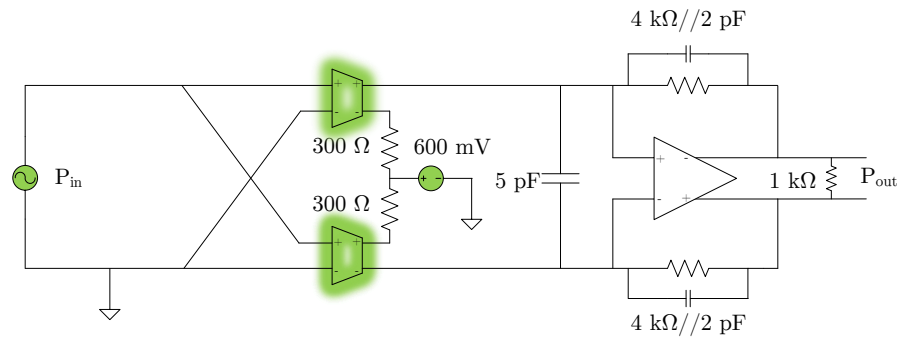


## Test bench schematics

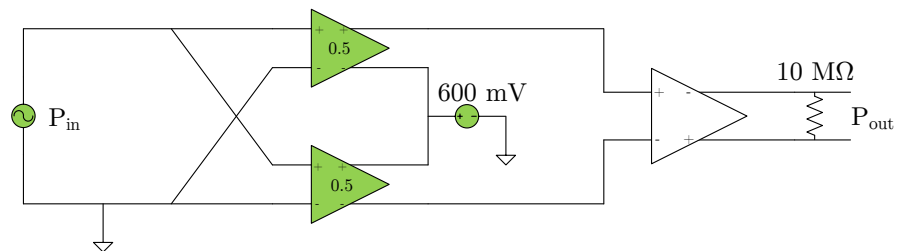
In this appendix test benches used during individual block simulations are collected.



**Figure A.1:** Test bench for simulating the linearity and frequency response of the LNTA with ideal components in green. Details regarding port termination omitted



**Figure A.2:** Test bench for simulating the linearity of the amplifiers with ideal components in green. Details regarding port termination omitted



**Figure A.3:** Test bench for simulating the open loop characteristics of the amplifiers with ideal components in green. Details regarding port termination omitted



**LUND**  
UNIVERSITY

Series of Master's theses  
Department of Electrical and Information Technology  
LU/LTH-EIT 2016-504

<http://www.eit.lth.se>