Popular Science Summary of Master Thesis

Design of a 30 GHz PLL for use in Phased Arrays

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Introduction

The road to achieving extremely high data (GB/s) rates in next generation 5G multiple input multiple output (MIMO) networks is paved by the use of multiple antennas to effectively form a beam of the wireless signal from one location to another. This is done at very high frequencies from 30 GHz and beyond. We call the range of frequencies between 30 GHz and 300 GHz millimeter wave (mm-wave) frequencies. By operating at a high frequency, an abundance of unlicensed spectrum, or, an allocation of free space in the frequency domain will be available. This stems from the current low-frequency spectrum being expensive, used up, and low bandwidth[1].

The process of creating the focused beam is called beamforming. As the frequency of the wireless signal increases, the signal itself becomes weaker as it travels over some distance. This can be due to things such as weather, the atmosphere, or buildings. By forming a beam, we concentrate the signal in one direction to increase the strength of the signal as it appears at its destination. In addition to concentrating the beam in one direction, we can also reject interference from other directions. So, we increase the signal frequency to unlock the wide bandwidth unlicensed spectrum and we include beamforming to increase the strength of the signal as it goes from point A to point B[1].

In one method of beam forming, which is called local oscillator (LO) beamforming, the array of antennas are controlled using something called a phase-controlled phase-locked loop (PC-PLL). The beam is formed, basically, by forcing each antenna in the array to emit the signal at slight phase shifts from one another. We can think of the PC-PLL as being a signal generator which outputs, say, a sine wave with some frequency at some phase. The exception, though, is that the PC-PLL takes an input which is another sinusoid. Its purpose is to copy the input sinusoid (which may be imperfect) to the output with a much more perfect sinusoid. Here, the input sinusoid is often called the reference signal. One of the cool things about the PC-PLL, is that although it is copying the reference to the output, it has the ability to change the frequency of the reference signal as well as to add a phase offset. However, the PC-PLL locks its output phase with respect to the reference phase[6].

Many antennas can be made to be relatively small and packed into a dense area. This array of antennas, when phase controlled, is called a phased antenna array. In 5G MIMO applications, the phased antenna arrays can be used, for example, as smart base-stations (or miniature cells) for mobile networks. In this way, the wireless signals can be relayed from one location to another[1].

This thesis project investigates and implements the design of a 30 GHz PC-PLL while meeting some basic design requirements[2]. Additionally, bottlenecks expected to be encountered for increased operating frequency were discussed. Fig. 1 depicts an example of beamforming from a transmitter to two users, or for example, from a cellular phone tower to two cellular phones.

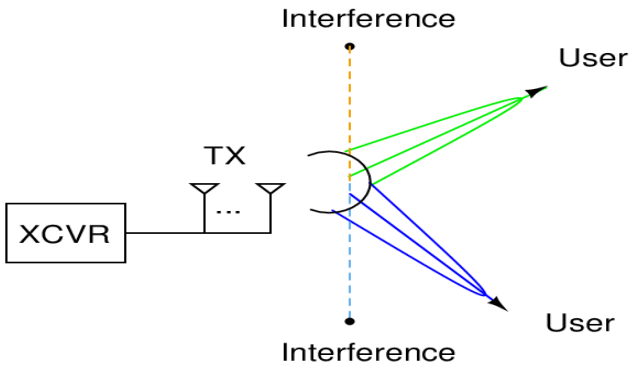

Fig 1. Beamforming example

Design Challenges

Designing the PC-PLL isn't so straightforward. Some care must be taken to make sure that the sinusoid at the output of the PC-PLL is as pure a sine-wave as possible. That means, ideally, exactly a 30 GHz sine wave at exactly some phase. In reality, this is not possible and there will always be some error due to the process of the integrated chip being manufactured. In order to account for the error, we add controls to the PC-PLL so that we can dial-in the frequency and add some phase offset as necessary. The signal at the input to the phased antenna array should be able to have its phase offset by at least 360 degrees[3].

The frequency tunability of this project's PC-PLL is 30 GHz ± 10% and the phase can be offset by up to 417 degrees with a resolution of 10 degrees. In addition to the phase control requirement, often times a quadrature output signal is desired for better spectral efficiency[4]. This means that, instead of simply generating a signal at some phase of 0 degrees, we will also generate that signal at 90, 180, and 270 degrees. This allows us to do some processing which allows us to take better advantage of the spectrum we have available to us. There are many ways to obtain the quadrature signals, but they often come with design trade-offs. A study has been done which compares and contrasts these design trade-offs[5]. This project's PC-PLL takes the study into consideration when choosing the best architecture to use.

Phase noise is an important metric for how well the PC-PLL works. The lower the phase noise, the more ideal the signal is. If the phase noise is not low enough, the signal that we may hear while talking to someone on the phone could be either bad quality or not of use to us at all. Synthesizing low-noise mm-wave frequencies is no easy task. Special circuits are necessary for low phase noise but the efficiency of the special circuits tend to diminish as the operating frequency increases[7]. Due to diminishing effect of frequency on the phase noise, the tasks of designing the highest frequency parts of the circuit are the most challenging. Luckily, cool techniques exist, such as inductive source degeneration[8] and discrete frequency tuning to drastically improve the phase noise! Furthermore, the phase noise of the reference signal can also have an influence in the phase noise of the PC-PLL[6].

Results

In the completion of this project, a 30 GHz PC-PLL was designed and implemented in the 65 nm ST Microelectronics technology. Quadrature outputs with a phase noise of -101.1 dBc/Hz at a 1 MHz offset from the carrier were generated using a current consumption of 4.93 mA and a supply voltage of 1.2V. Three digital bits facilitate the discrete frequency tuning and 7 digital bits were used for phase control. The feedback path divides the output frequency by 32 using a current-mode latch architecture and digital frequency dividers.

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