Master's Thesis

Highly Linear Attenuator and Mixer for Wide-Band TOR in CMOS

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HIGHLY LINEAR ATTENUATOR AND MIXER FOR WIDE-BAND TOR IN CMOS

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Abstract

In this thesis work, a highly linear passive attenuator and mixer were designed to be used in a wide-band Transmission Observation Receiver (TOR). The TOR is a low IF receiver that accepts RF frequencies from 2GHz to 7GHz, and produces corresponding IF bandwidths of 280MHz to 990MHz respectively, using low side LO injection. The dynamic range is maximized by using passive topologies for both the attenuator and the mixer. The system is dealing with different power levels ranging from -30dBm to +1dBm, and hence, a programmable digital step attenuator is used to attenuate large signals. It provides a maximum of 31dB of attenuation in 1dB steps. Different mixer architectures were compared, including CMOS mixer, mixer with dummy switches and quadrature mixer. Also, the performance of the mixer in both voltage mode and current mode was investigated. A double balanced passive mixer in voltage mode, with dummy switches was adopted in the final system since it proved to be the best in terms of meeting the requirements. The work was carried out in Ericsson in Lund, using Cadence, 65nm process. The circuit is true differential and it uses a supply voltage of 1.2V. The final results show a spurious free dynamic range of higher than 85dBc, minimum in band IIP3 of +15dBm , maximum IIP3 of +50dBm and a worst input return loss of less than -10dB. The amplitude and phase precision over the observation bandwidth were quite good, a worst phase error of less than 3 degrees was recorded and an amplitude error of 0.5dB.

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List of Acronyms

ADC	Analog to Digital Converter
TOR	Transmission Observation Receiver
DCR	Direct Conversion Receiver
RF	Radio Frequency
SNR	Signal to Noise Ratio
IF	Intermediate Frequency
LTE	Long Term Evolution
LO	Local Oscillator
PSP	Surface-Potential-Based MOSFET Model for Circuit Simulation
CMOS	Complementary Metal Oxide Silicon
NMOS	Negative-Channel Metal Oxide Semiconductor
PMOS	Positive-Channel Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
TIA	Trans-impedance Amplifier
NF	Noise Figure
CP1	1dB Compression Point
IL	Insertion Loss
VGA	Variable Gain Amplifier
IBW	Information Band-Width
PA	Power Amplifier
DAC	Digital to Analog Converter
DPD	Digital Pre-Distortion
IM2	Second-order Inter-modulation
IM3	Third-order Inter modulation
IIP2	Second-order Input referred Intercept Point
IIP3	Third-order Input referred Intercept Point
OIP3	Third-order Output referred Intercept Point
SFDR	Spurious Free Dynamic Range

Chapter 1

Introduction

1.1 RF receivers

Receivers are essential part of any wireless device, the analog signal is first passed through the RF receiver for initial processing, and then converted in to a digital signal via ADC for more processing. There are homodyne and heterodyne receivers. The choice of the type of the receiver to be used depends on the system requirements. In a homodyne (also called direct conversion receivers or zero IF receivers), the incoming RF signal is down-converted to baseband directly by mixing with an oscillator LO signal that is identical to the RF input signal. The resulting baseband signal is then filtered with a low-pass filter to select the desired channel.

The main advantage of the homodyne receiver is that it does not suffer from the image problem as the incoming RF signal is down converted directly to baseband without any IF stage. Moreover, it is simple, since it does not require any high frequency band-pass filter, which is usually implemented off-chip in the super-heterodyne receiver for appropriate selectivity. The major disadvantage of direct conversion receiver is the DC offsets which can be generated at the output of the mixer when the leakage from the local oscillator is mixed with the local oscillator signal itself. This could saturate the following stages and affect the signal detection process. The removal of the dc offset by means of a high-pass filter proves difficult. Also, since the mixer output is a baseband signal, it can easily be corrupted by the large flicker noise of the mixer, especially when the incoming RF signal is weak [2].

Heterodyne receiver, on the other hand, can be of high IF or low IF type, where the RF signal is mixed down to a non-zero low or moderate intermediate frequency. Super heterodyne receiver avoids the DC offset and 1/f noise problems of the direct conversion receiver.

The use of low IF receiver introduces the image problem. However, when there are relatively relaxed image and neighboring channel rejection requirements, they can be satisfied by carefully designed low-IF receivers. If the intermediate frequency is high, the image then appears far away from the desired signal band and can easily be suppressed by a bandpass filter with typical cutoff characteristics. However, the

channel selection filter now requires a very high Q-factor, which is defined as the ratio of the center frequency to the 3dB bandwidth, and filters with very high Q are difficult to design. If the IF is low, the channel selection has more relaxed requirement, but proper image suppression becomes harder to achieve [3].

More than one IF mixer stage can be used to solve the contradiction between sensitivity and selectivity, such as dual-IF heterodyne receiver, where the RF signal is first down converted to an IF that is high enough to allow easy suppression of the image. It is then down converted to a second IF that is much lower than the first one to ease channel selection. For image rejection, image-reject receivers can be used [3]. In this work, since the TOR is used for linearization applications, in band fidelity is required but image rejection is not critical, that is why a low IF receiver type is selected.

1.2   Transmission observation receiver

There is an increasing need for high data rates and capacities for the modern wireless communication systems, the advanced LTE as an example uses 100MHz which requires wide band transmit signals. This large bandwidth makes the design of the power amplifiers(PA) challenging. The PA is a critical block in an RF system as it dominates the sources of nonlinearity and power consumption, and it is difficult to meet the performance specifications while maintaining low in band distortion over the whole bandwidth. In order to circumvent this issue in the base stations, transmission observation receiver (TOR) is used, where the transmitted signal is fed to the TOR chain through a test attenuator (TA). The TOR is supposed to be very linear to be used as a reference receiver. Since the output spectrum of the PA is usually wider than its input due to nonlinearities, the TOR should also have a bandwidth that is many times larger than the input signal to the PA to capture all the harmonics. The output from the TOR is then fed to a digital pre-distortion circuit (DPD) which is one of the advanced linearization techniques that compensates for nonlinear distortion in RF PAs by inverting their nonlinear behavior using digital circuits. In other words, DPD creates a compensation signal that pre-distorts the input of the PA so that, the output appears non distorted and perfect. DPD allows PAs to be highly efficient without linearity degradation, which is nowadays one of the essential requirements in high-power wireless base stations [4]. The aim of this thesis work is to investigate and design a highly linear wide band TOR in CMOS technology to be used for linearizion of PA in the base stations. It has been implemented as a low IF receiver.

1.3   Thesis Objectives

In this thesis project, the design of a high linear and wide band low IF TOR was investigated and different design approaches were compared to achieve very high linearity in the orders of -90dBc. The focus of the thesis was on the attenuator and

mixer parts of a low IF TOR. The receiver should satisfy the linearity specification for an input frequency range of 2GHz to 7GHz with an IF of 280MHz to 990MHz respectively, and for input power levels range from -30 to +1dBm. Passive topologies are adopted to meet the stringent linearity requirements. The TOR is intended to be used in the base stations of 5G mobile technology, to allow for PA linearity correction using DPD to ensure efficient PAs over the wide bandwidth of modern transmitters. The noise figure is not of concern when designing TOR, since the signals are relatively strong, so, the noise requirement was very relaxed in this work.

1.4 Outline

The rest of this report is organized as follows:
Chapter 2 provides explanation of the general target specifications and related concepts.
Chapter 3 is about reviewing the related prior art and theory.
Chapter 4 gives a brief analysis of the circuits used in this project work.
Chapter 5 illustrates the design of every stage in the system and presents the intermediate results and comparison between different adopted design alternatives.
Chapter 6 presents the final system results along with some conclusions.
Chapter 7 concludes the thesis and suggests some future trends to improve this work.

Chapter 2

System Target Specifications

Transmission observation receiver is often used in wireless base stations to improve the linearity of power amplifiers (PA), which leads to power efficient base station, by having PAs that can meet the required dynamic range performance with out consuming large power. The receiver captures the PA output, which later on will be converted in to digital stream and the distortion will be analyzed in DPD block. A complementary distortion is then sent back to the transmit DAC, and pre-distorting the signal. That means the TOR should have very good linearity. A significant factor in PA linearity is the distortion caused by the odd order intermodulation (IM) products. The bandwidth to be captured and fed to DPD is equivalent to the signal bandwidth multiplied by the order of the IM product to be canceled. In this work, the concern is about canceling the third order intermodulation products and hence the TOR should work for about three times the bandwidth of the original signal at the PA input.

This masters thesis is about designing a high linear wide-band transmission observation receiver. The focus was around the first stage attenuator and the mixer. The functional blocks of the TOR are illustrated in the dashed box in figure 2.1.
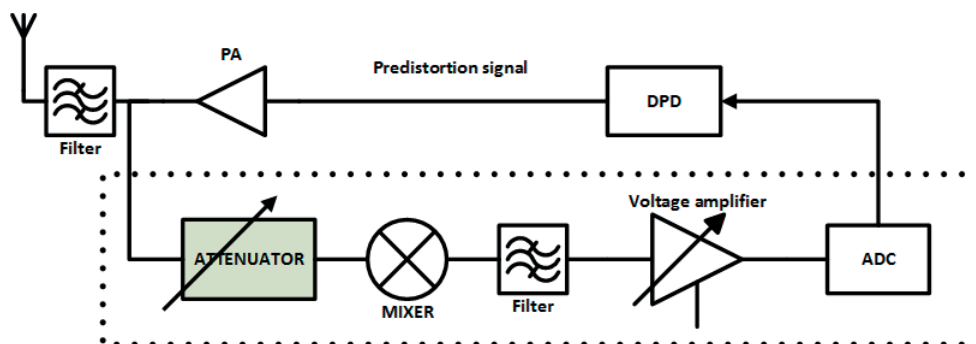
Figure 2.1: TOR functional blocks represented in the dashed box

The most important defined specifications for the system are listed in Table 2.1.
More detailed specifications for each block will come in the system Design chapter.

Table 2.1: Target specifications

Parameter	Target
S11,S22	$< -10dB$
SFDR	$\leqslant -90dBc$
Input power	-30 to +1dBm
IIP3	>+14dBm
Out of band Emission at the antenna	$\leqslant -100dBm$
Differential Source impedance	100Ω
Supply voltage	1.2V
RF input frequency range	2GHz to 7GHz
LO frequency range	Low side injection, 1.72GHz to 6.01GHz
IF frequency range	280MHz to 990MHz
Amplitude error/1GHz	$\leqslant 0.2dB$
Phase error/1GHz	<6 deg
NF @ 7GHz(input power = 0dBm)	$< 50dB$
NF @ 7GHz(input power = -30dBm)	$< 19dB$
NF @ 2GHz(input power = 0dBm)	$< 56dB$
NF @ 2GHz(input power = -30dBm)	$< 25dB$

The related concepts are defined and analyzed in the following sections.

2.1   Matching and return losses

2.1.1   Matching

Impedance matching is one of the important issues in the design of RF circuits.
Matching in general can refer to current matching, where the load impedance is low
compared to the source impedance, or voltage matching, where the load impedance
should be high in comparison with the source impedance, or power matching where
the source and load impedances should be equal. Power matching results in higher
voltages and currents than what is possible with current and voltage matching. Usu-
ally, in RF circuits design, the interest is to get the maximum possible transfer of the
power. The remaining of this section is a summary from [5]. Given a source and load
impedances as depicted in figure 2.2, the equations below define the maximum power
transfer [5].
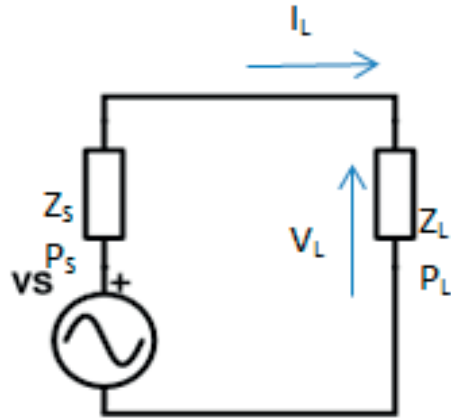
Figure 2.2: Source and load impedances

$$I_L = \frac{V_S}{Z_S + Z_L} \tag{2.1}$$

$$V_L = \frac{V_S * Z_L}{Z_S + Z_L} \tag{2.2}$$

$$P_L = V_L * I_L = \frac{V_S^2 * Z_L}{(Z_S + Z_L)^2} \tag{2.3}$$

It is clear from the equations that the maximum power transfer can be achieved when the source and load impedances are equal if they are pure resistive, or when they are conjugate matched if they are complex values. The maximum power transfer is referred to as the available power from the source which is defined by the following equations.

$$P_{AVS} = \frac{V_S^2}{4R_S} \tag{2.4}$$

It is obtained by substituting in equation (2.3) $R_S = R_L$ when the load is purely resistive and $Z_L = Z_S^*$ when the load is complex. Where

$$Z_L = R_L + jX_L$$

$$Z_S^* = R_S - jX_S$$

2.1.2   S-parameters

A common way to describe a two-port network in RF systems is by the use of S parameters. In figure 2.3, a_i represents the incident wave at each port and b_i is the reflected wave. However, b_i contains contribution from both incident waves as they scatter through the two-port. This is where the name scattering parameters comes from. S-parameters are defined by the following equations:

$$b_1 = S_{11}a_1 + S_{12}a_2 \qquad\qquad (2.5)$$
$$b_2 = S_{21}a_1 + S_{22}a_2 \qquad\qquad (2.6)$$

or in a matrix form:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$
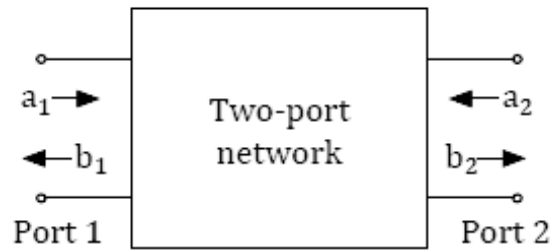
Figure 2.3: Two port network power waves

In S parameters, usually the power carried by the wave is used rather than the voltage or current. S11 describes how much of a_1 is reflected back to b_1, or, how well the input is matched and is a measure of the input impedance. S12 is a measure of how much of a_2 scatters through the system, or, how well the output is isolated from the input. S22 is the same as S11 but at the output and S21 is a measure of how much the incident wave at the input affects the reflected wave at the output, or, how the input signal affects the output signal. It represents the gain of the two-port. If we have an incident wave V^+ and a reflected wave V^- at one port, then we can define the following:

The total voltage at the port:

$$V = V^+ + V^- \qquad (2.7)$$

The total current at the port:

$$I = I^+ - I^- = \frac{V^+}{Z_0} - \frac{V^-}{Z_0} \qquad (2.8)$$

Where Z_0 represents the reference impedance, and the voltages and currents are given as peak values. The reflection coefficient of the port can be defined as:

$$\Gamma = \frac{V^-}{V^+} \qquad (2.9)$$

If we define some normalized quantities:

$$v = \frac{V}{\sqrt{2Z_0}}$$

$$i = \sqrt{\frac{Z_0}{2I}}$$

$$a = \frac{V^+}{\sqrt{2Z_0}}$$

$$b = \frac{V^-}{\sqrt{2Z_0}}$$

This leads to :

$$\begin{aligned} v &= a + b \\ i &= a - b \\ b &= \Gamma * a \end{aligned} \qquad (2.10)$$

Which means the normalized voltage and current can be rewritten in terms of power waves a and b. The squared absolute values of a and b gives the power of the wave as illustrated in the following equations.

$$\begin{aligned} P^+ &= \frac{|V^+|^2}{\sqrt{2Z_0}} \quad = |a^2| \\ P^- &= \frac{|V^-|^2}{\sqrt{2Z_0}}| \quad = |b^2| \end{aligned} \qquad (2.11)$$

The power delivered to a port can be expressed as :

$$P^+ - P^- = |a^2| - |b^2| \tag{2.12}$$

S parameters are measured while one port is terminated with a perfect matched load as follows:

$$S_{11} = \left.\frac{b1}{a1}\right|_{a_2=0}$$

$$S_{12} = \left.\frac{b1}{a2}\right|_{a_1=0}$$

$$\tag{2.13}$$

$$S_{21} = \left.\frac{b2}{a1}\right|_{a_2=0}$$

$$S_{22} = \left.\frac{b2}{a2}\right|_{a_1=0}$$

2.2 Nonlinearity in RF systems

This section is a summary from RF Micro-Electronics book by Behzad Razavi. A system is considered to be nonlinear if it has an input-output relation similar to what is shown in 2.14 for any input x(t).

$$y(t) = \alpha_1 * x(t) + \alpha_2 * x^2(t) + \alpha_3 * x^3(t)..... \tag{2.14}$$

2.2.1 Harmonic distortion

If a sinusoid input at a certain frequency is applied to a nonlinear system, that will result in output signals at the multiples of the input frequency in addition to the fundamental frequency, suppose the input is $A\cos(\omega t)$. see 2.15, 2.16 and 2.17

$$y(t) = \alpha_1 * A cos(\omega t) + \alpha_2 * A^2 cos^2(\omega t) + \alpha_3 * A^3 cos^3(\omega t) \tag{2.15}$$

$$= \alpha_1 * A cos(\omega t) + \frac{\alpha_2 * A^2}{2}(1 + cos(2\omega t)) + \frac{\alpha_3 * A^3}{4}(3cos(\omega t) + cos(3\omega t)) \tag{2.16}$$

$$= \frac{\alpha_2 * A^2}{2} + (\alpha_1 * A + \frac{3\alpha_3 A^3}{4})cos(\omega t) + \frac{\alpha_2 * A^2}{2}cos(2\omega t) + \frac{\alpha_3 * A^3}{4}cos(3\omega t) \tag{2.17}$$

The DC offset arises from the even order harmonics. Even order harmonics can be canceled by having differential circuit, but in reality, mismatches will lead to some finite even order harmonics in differential circuits.

Odd harmonics are very important if they fall within the desired bandwidth, designers should make sure that the harmonics level is far less than the fundamental desired signal.

2.2.2   Gain compression

Referring to equation 2.17, it is clear that the input signal will be subject to a gain of $(\alpha_1 * A + \frac{3\alpha_3 A^3}{4})$, and given that the factors α_1 and α_3 have different signs in most cases, the gain will compress as A gets larger, a common way to express the compression is (1dB compression point) which is defined as the input signal level that causes the gain to reduce by 1dB. It can also be expressed as the output power level where the gain drop by 1dB. It is usually plotted in logarithmic scale, with either voltage or power signals as figure 2.4 illustrates.

To calculate the compression point, the compressed gain is equated to the ideal gain as follows:

$$20log\left|\alpha_1 + \frac{3}{4}\alpha_3 A_{in,1dB}^2\right| = 20log|\alpha_1| - 1dB \tag{2.18}$$

Hence

$$A_{in,1dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.19}$$
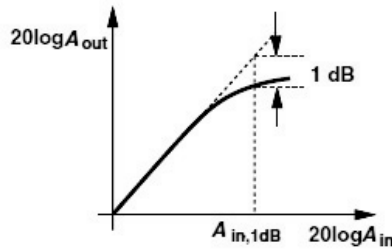
Figure 2.4: 1dB compression point illustration

2.2.3   Inter modulation

Inter modulation is a phenomena occurs when two interferes are applied to a non-linear system, because then new frequencies will be produced. Some of them will be very close to the fundamental signal frequency, and can not be filtered out. The idea can be better understood by looking at 2.20

$$y(t) = \alpha_1(A_1cos(\omega_1 t) + A_2cos(\omega_2 t)) + \alpha_2(A_1cos(\omega_1 t) + A_2cos(\omega_2 t))^2$$
$$+ \alpha_3(A_1cos(\omega_1 t) + A_2cos(\omega_2 t))^3 \tag{2.20}$$

By expanding Equation 2.20, we will get the following inter modulation terms expressed by2.21

$$.....+ \frac{3\alpha_3 A_1^2 A_2}{4}cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4}cos(2\omega_1 - \omega_2)t$$
$$+\frac{3\alpha_3 A_1^2 A_2}{4}cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_1^2 A_2}{4}cos(2\omega_2 - \omega_1)t + ...$$

(2.21)

The signals at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are the most important because they are very likely to fall in the desired bandwidth. They are referred to as third inter modulation products(IMD3).

The two tone test method is used to evaluate the IMD3 by applying two sinusoid tones with the same input power levels and a small frequency offset to make sure the third inter-modulation product will be within the band of interest. Denoting each tone by A. So the relative IMD will be [3]:

$$RelativeIM = 20Log\left(\frac{3\alpha_3 A^2}{4\alpha_1}\right) dBc$$

(2.22)

Where dBc stands for decibels with respect to the carrier. In order to use the relative IM measurement, the input power level should be known. Another way to quantify the nonlinearity due to inter modulation is the use of Input third Intercept Point(IIP3), which is defined as the input level where the IMD3 becomes equal to the fundamental tones at the output. In a similar way, Output Third Intercept Point (OIP3) can be used. By equating the fundamental and IMD3, one can get [3]:

$$A_{in,1dB} = \left|\frac{3\alpha_3 A_{IIP3}^3}{4}\right|$$

(2.23)

hence,

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}$$

(2.24)

From the equations, a relation between the IIP3 and 1dB gain compression can be derived as in 2.25

$$\frac{A_{IIP3}}{A_1 dB} = \sqrt{\frac{4}{0.435}} \approx 9.6dB$$

(2.25)

In order to measure the third intercept point, the fundamental and IM tones are plotted in logarithmic scale, the curves are then extrapolated to find the IP3. Extrapolation is needed because both of them will compress 10dB before reaching IP3 point. See figure 2.5 [3]. A mathematical expression can be derived to serve as a sanity check for the extrapolated IIP3 results, starting from the idea that, the change
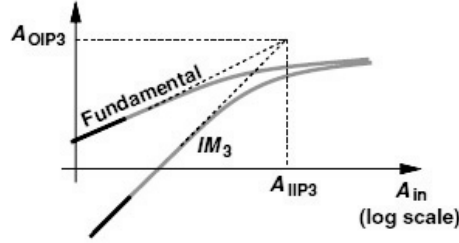
Figure 2.5: IIP3 and OIP3 definition

of the input power level from A_{IIP3} to some arbitrary lower level A_{in} is corresponding to a relative difference between the fundamental tone and IIP3 with a slope of 2. which can be written as [3]:

$$\Delta P_{dB} = A_{fund,dBm} - A_{IM,dBm} \qquad = 2(A_{IIP3,dBm} - A_{in,dBm}) \qquad (2.26)$$

$$A_{IIP3,dBm} = \frac{\Delta P_{dBm}}{2} + A_{in,dBm} \qquad (2.27)$$

Both the extrapolated IIP3 and the calculated IIP3 should agree if the circuit does not exhibit dynamic nonlinearity. For accurate results, mathematical expressions were used to check IP3 and IP2 in this thesis.

2.2.4   Nonlinearity in cascaded stages

To analyze the IIP3 in cascaded stages, assuming a system with three stages, with a gain of the first stage α and a gain of the second stage β according to RF Microelectronics book by Behzad Razavi, we can conclude that, the linearity of each stage is degraded as the gain of the preceding stage increases, see equation2.28.

$$\frac{1}{A_{IP3}} = \frac{1}{A_{IP3,1}} + \frac{\alpha_1^2}{A_{IP3,2}} + \frac{\alpha_1^2 \beta_1^2}{A_{IP3,3}} \qquad (2.28)$$

In this work, cascaded attenuators are used to reduce the input signal. The stage with worst IIP3 is located last, to ensure good IIP3.

2.3   Emission requirement at the antenna

Since in the transmitters, the PA is the dominant nonlinear component, its output bandwidth is wider than it is input as illustrated in figure 2.6. The TOR observation bandwidth is assumed to be 3*times the information band width (IBW), to cover this extended bandwidth and capture all the harmonics for later compensation in digital pre-distortion blocks.

The required overall out of band emission at the antenna is to be below the noise floor over relevant bandwidth, which is estimated to be -100dBm for a typical LTE bandwidth of 25MHz, given that the noise spectral density is -174dBm/Hz. The coupler (T) which taps off the PA signal to the TOR input adds 20dB attenuation from PA port to TOR port. Also, the signal will pass through a filter directly before reaching the antenna. The filter intended to be used, suppresses the out of band spectrum by 30dB on one side and 40dB on the other side. So, in order to meet the requirement of an out of band emission of maximum -100dBm, a value of less than -50dBm for out of band emission should be targeted when measured at the input port of the TOR, the total LO leakage is then $-50dBm - 20dB - 30dB = -100dBm$. The antenna will filter the far away signals from the desired band even more according to its selectivity. For the in-band emission(emission within the IBW range), it should be less than $-85dBc$. Figure 2.6 shows a transceiver partial building blocks which utilizes TOR for nonlinearity correction. The spectrum at the output of the different blocks is depicted.
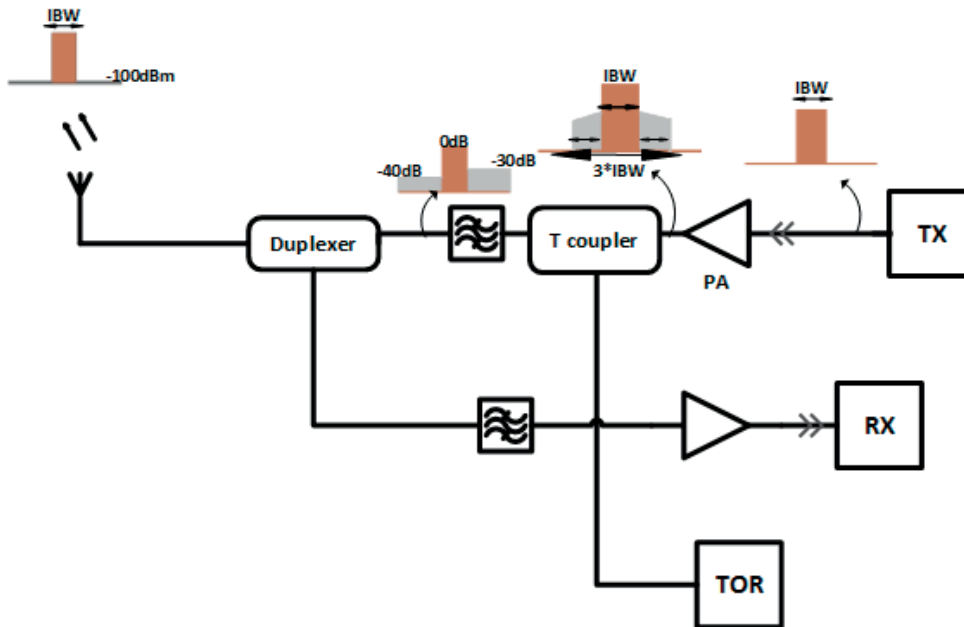
Figure 2.6: The block diagram for a transceiver using TOR

Chapter 3

Literature Review

3.1   Attenuator topologies

Attenuators are devices used to reduce the signal power, there exists active and passive attenuators. The active attenuators are mainly variable gain amplifiers(VGA) which are not suitable for todays design concerns because of their large power consumption and linearity problems, with VGA, in order to reach high level of linearity, the power consumption will be huge, i.e, in ranges of hundreds of milliwatts. CMOS passive attenuators, on the other hand, are progressively replacing variable gain amplifiers nowadays because of their high dynamic range, larger bandwidth, lower power consumption, and power handling capability. Attenuators are characterized by their return losses, insertion loss when they are in the reference state, maximum attenuation, amplitude and phase variation across the frequency range and their linearity [6]. Two main topologies of passive attenuators will be analyzed and compared based on these parameters in this thesis. Variable analog attenuators in this chapter and digital step attenuators in the next chapter as digital step attenuator is selected for the implementation of this project.

3.1.1   Variable analog attenuators

Variable analog attenuators utilize the MOSFET in their linear region to realize the resistors, the most common types of these attenuators are Pi and T architectures. They are shown in figure 3.1a and figure 3.1b. By changing the control voltage in the gates of the switches, the switch resistance R_{on} will change accordingly and hence the attenuation level.

Insertion loss

Insertion loss IL Refers to the signal loss due to the insertion of an attenuator in its path, mainly due to R_{on} of the transistors for lower frequencies. For higher frequencies, the capacitors come in to play to add to the loss. The insertion loss should be

(a) PI-Attenuator
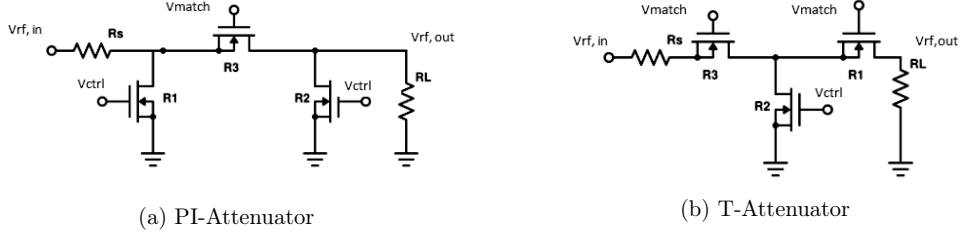
(b) T-Attenuator

Figure 3.1: Passive analog attenuator types

kept as minimum as possible.

For Pi variable attenuators, a high frequency model is shown in figure 3.2a for the minimum attenuation case where the shunt devices are both off. The parasitic capacitances shown are mainly due to the gate oxide capacitance, gate-drain overlap, gate-source overlap, the junction capacitance between source and p-substrate and the capacitance between drain and p-substrate. By accumulating the capacitances, the model can be redrawn as in figure 3.2b [6].

(a) lumped resistor-capacitor-model

(b) Accummulated capacitors- model
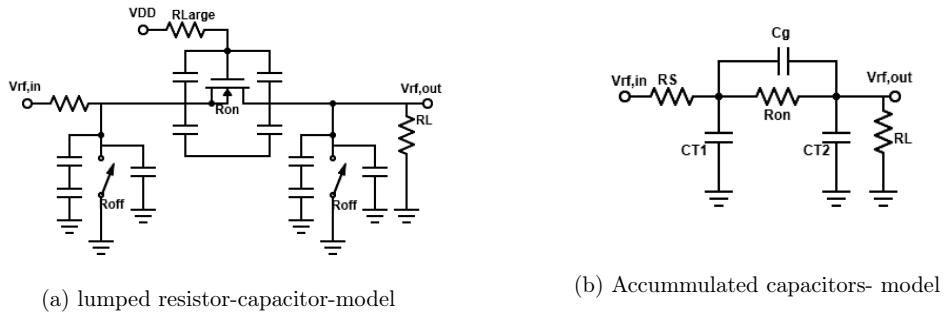
Figure 3.2: Pi attenuator model in minimum attenuation settings

It is clear that minimizing the series resistor by increasing the series device width will minimize the loss, that is true for low frequencies. For higher frequencies, the capacitances will contribute significantly to the loss. It can be seen from figures that a large resistor is added in series with the gates to isolate them from the ground, hence minimizing the effective capacitances and the loss. It can be shown that this resistor will help the linearity as well by acting as bootstrapping resistor. The insertion loss can be expressed as equation (3.1) [6] .

$$IL = \frac{R_s}{\frac{R_s+R_{on}}{2}} \frac{(1+sC_gR_{on})}{(1+sC_gR_{on})(1+s\frac{(C_T+2C_g)R_{on}R_s}{2R_s+R_{on}})} \tag{3.1}$$

where :

$$C_T = C_{T1} = C_{T2} = C_{db1} + C_{db2} + \frac{C_{gd2}}{2} \tag{3.2}$$

The first part of the equation represents the IL in low frequencies, where R_{on} is given by:

$$R_{on} = \frac{1+\theta(v_{GS}-v_t)}{\mu C_{ox}(\frac{W}{L})(v_{GS}-v_t-\eta v_{DS})} \tag{3.3}$$

where:
$\theta \equiv$ drain to source resistances
$\mu \equiv$ the exponential behavior of the drain current in the subthreshold region.
$v_{GS} \equiv$ The gate to source voltage.
$v_{DS} \equiv$ The drain to source voltage

For T attenuators, model shown in figure 3.3, the minimum attenuation is when the two series switches are on while the shunt switch is off. Therefore, making these switches larger will minimize the IL [6].

(a) lumped resistor-capacitor-model

(b) Accummulated capacitors- model
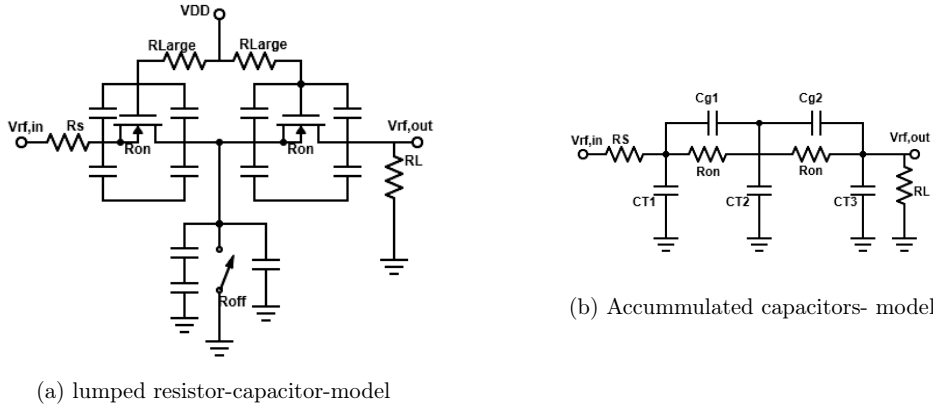
Figure 3.3: T attenuator model in minimum attenuation settings

The parasitic capacitors also affect the IL and can be characterized using the model as [6]:

$$C_T = C_{T1} = C_{T3} = C_{db1} \tag{3.4}$$

$$C_g = C_{g1} = C_{g2} = \frac{C_{gd1}}{2} = \frac{C_{gs2}}{2} \tag{3.5}$$

$$C_{T2} = C_{sb1} + C_{db2} + C_{db3} + \frac{C_{gd3}}{2} \tag{3.6}$$

R_{large} is used for the same purpose as in T attenuators. Hence, the total IL is given by:

$$IL = \frac{R_s}{R_s + R_{on}} \frac{1}{(1 + s(C_T R_s + C_{T2} \frac{R_s + R_{on}}{2}))} \tag{3.7}$$

It is worth mentioning that, the IL for T attenuators is worse than the Pi ones, since for T attenuator, two transistors determine the IL compared to one in Pi attenuator. There is a trade off between the minimum IL and the bandwidth, since increasing the transistors sizes to minimize the IL will introduce parasitic capacitances which will reduce the bandwidth. T attenuators are not as broad band as Pi alternatives, since the switches are very large; the series switches are usually made large to minimize the IL while the shunt switch is made Large to increase the maximum attenuation level. These larger switches result in larger parasitics [6].

Maximum attenuation

For Pi attenuator, the maximum attenuation is achieved by turning off the series switch completely. The shunt devices are controlled so that they have equivalent resistances of R_S and R_L for perfect matching, assuming that the series switch off resistance is high enough. Figure 3.4 shows the model of this attenuator under maximum attenuation settings, the model includes the effect of channel leakage through parasitic inductance and resistance on the isolation, however, acceptable level of isolation can be reached with careful chip layout [6]. Capacitors in this model, can be approximated by [6]:

$$C_T = C_{T1} = C_{T2} = C_{db1} + C_{db2} + \frac{C_{gd2}}{2} \tag{3.8}$$

$$C_g = \frac{C_{gd1}}{2} \tag{3.9}$$

(a) lumped resistor-capacitor-model

(b) Accumulated capacitors- model
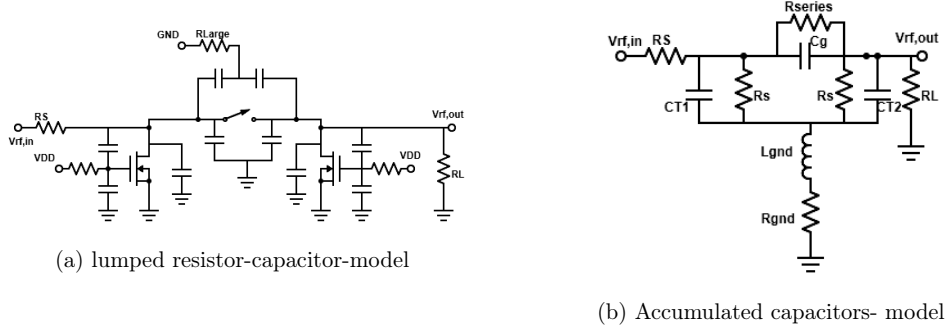
Figure 3.4: Pi attenuator model for maximum attenuation settings

The maximum attenuation can be calculated as follows:

$$\frac{1}{Att_{MAX}} = R_s \frac{Z_s(2Z_{gnd} + Z_s) + Z_{series}Z_{gnd}}{(2Z_{gnd} + Z_s + R_s)(2Z_sR_s + Z_{series}R_s + Z_{series}Z_s)}$$

$$Z_s = \frac{R_s}{1 + sC_TR_s},$$

$$Z_{series} = \frac{R_{series}}{1 + sC_gR_{series}},$$ (3.10)

$$Z_{gnd} = R_{gnd} + sL_{gnd}.$$

By assuming low frequency and ignoring the ground parasitics in equation (3.10) the maximum attenuation can be written as:

$$\frac{1}{Att_{MAX}} = R_s \frac{2R_{gnd} + R_s) + R_{series}R_{gnd}}{(2R_{gnd} + R_s)(R_s + R_{series})} \approx \frac{R_{gnd}}{2(R_{gnd} + R_s)}$$ (3.11)

For T attenuators, the maximum attenuation is achieved by shorting the shunt branch to ground, so, the shunt switch should be made large to minimize the R_{on}. The maximum achievable attenuation is a direct function of the shunt switch width. The series switches will also be on with an equivalent resistance equal to $R_s - R_{on}$ to ensure good impedance matching. In the maximum attenuation case, T attenuators are considered wide band, since the intermediate node has very low impedance to ground as depicted in figure 3.5, so the capacitances attached to this node will create a pole magnitude at very large frequencies [6]. The maximum attenuation is given

(a) lumped resistor-capacitor-model

(b) Accummulated capacitors- model
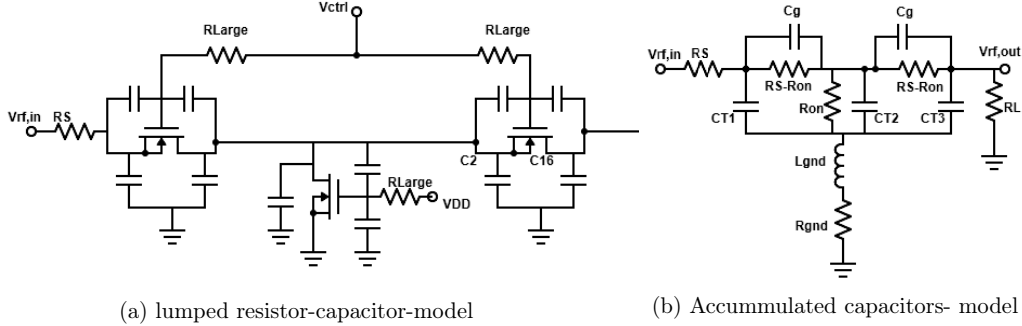
Figure 3.5: T attenuator model for maximum attenuation settings

from:

$$\frac{1}{Att_{MAX}} = \frac{Z_s^2(Z_{T2} + Z_{gnd})}{R_s(Z_s + Z_{series})(2Z_{T2} + 2Z_{gnd} + Z_{series} + Z_s)}$$

$$Z_s = \frac{R_s}{1 + sC_T R_s},$$

$$Z_{T2} = \frac{R_{on}}{1 + sC_{T2}R_{on}},$$

$$Z_{series} = \frac{R_s - R_{on}}{1 + sC_g(R_s - R_{on})},$$

$$Z_{gnd} = R_{gnd} + sL_{gnd}.$$

(3.12)

For low frequencies, the gain is given by:

$$\frac{1}{Att_{MAX}} = R_s \frac{(R_{gnd} + R_{on})}{2(2R_s - R_{on})(2R_s + 2R_{gnd} + R_{on})} \approx \frac{R_{gnd} + R_{on}}{2(R_s)}$$

(3.13)

Impedance matching

While shunt transistors are controlled by an external signal to change attenuation level, the series transistors will be controlled by a feedback circuit that ensures proper impedance matching. Attenuation can be increased by increasing the gate control voltage to reduce the channel resistance of the shunt transistors, thus reducing the output swing. Simultaneously, the feedback circuit will lower the gate voltage of the series resistor to increase the channel resistance of the series transistor so as a total of 50Ω input impedance is always maintained.

For lower frequencies, the input impedance is defined by resistors only, when the frequency gets higher, the capacitors will be added to form the impedances in the circuit and hence the matching will drift away from the ideal values. It can

be seen that for both types of attenuators, the worst scenario of capacitances is in the minimum attenuation settings, when the attenuator is passing signal with out attenuation since R_{on} of the series switch will be added to the load resistor as seen from the input and the capacitors will add up together to form a pole magnitude at relatively low frequencies [6].

For Pi attenuator the input impedance can be calculated as [6] :

$$Z_{in} = \frac{R_L + R_{on}}{1 + 2sC_T R_L}$$ (3.14)

The same for T attenuator:

$$Z_{in} = \frac{R_L + 2R_{on}}{1 + s(2C_T + C_{T2})R_L}$$ (3.15)

Linearity

The attenuation is a linear function of switch series resistance, and the resistance of the MOSFET is a nonlinear function of the its gate voltage and the input and output level differences (v_{DS}) according to equation (3.3). To analyze the linearity, it is convenient to define three regions of operations: when the attenuator is in low attenuation, mid attenuation and high attenuation settings. For low attenuation range, the shunt switches will be fed with a small voltage close to V_{th}, so, even small variation in the input power level will result in significant change in the channel resistance. The same analysis applies for high attenuation range, since the series switch will be biased with a small gate voltage. When the attenuator is set to mid attenuation range, both series and shunt switches will be biased at the same point roughly and the impedances will cancel out, resulting in a very good linearity [7]. So, if the attenuator is to be used for low or high attenuation in such a system like TOR with stringent requirement in linearity, there will be a need for some linearity correction techniques which might add to the circuit complexity.

3.2   Mixer topologies

Mixers perform frequency translation by multiplying two wave forms. Mixers have three different ports. In receivers, a down-conversion mixer has an RF port that senses the RF input signal, the LO port is for the local oscillator waveform input and the output port is fed to the base-band for processing [3]. Multiplication will result in output signals with sum and difference frequencies of the input as illustrated in equation (3.16). If the LO is constant, any modulation in RF signal is transferred to the IF signal [8].

$$Acos(\omega_1 t)Bcos(\omega_2 t) = \frac{AB}{2}[cos(\omega_1\omega_2)t + cos(\omega_1 + \omega_2)t]$$ (3.16)

Mixers are categorized as active and passive mixers, each of which can be unbalanced, single balanced or double balanced. Double balanced mixers are the most common type of mixers used today. In this section different active and passive topologies are discussed.

3.2.1 Active mixers

Active mixers commutate the signal in the current domain and comprise of a transconductance stage to provide some gain to compensate the power lost during switching [9].

Unbalanced mixer The simplest and the lowest in the noise figure. It can be implemented using a single or dual gate transistor, see figure 3.6. Mixing is performed by using nonlinear square law characteristics of MOS transistor. Conversion gain of this mixer is independent of the bias current [10].

(a) Single transistor unbalanced Mixer

(b) Dual gate unbalanced mixer
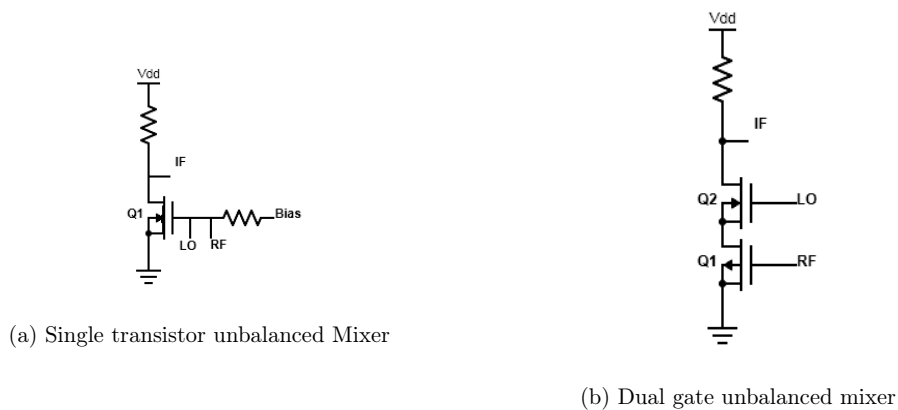
Figure 3.6: Active unbalanced mixer topologies

Unbalanced mixers provide no feed through rejection and hence, LO signal need to be injected into the RF port through some RF filter. The drain of the transistor is biased just at the edge between triode and saturation region to maximize the transconductance variation due to large LO signal [9].

Single balanced mixer The LO signals are balanced in this mixer type architecture(see figure 3.7). Single balanced mixers have lower noise figure than double-balanced mixers. This is because there are fewer noise contributors in the single-balanced design [9].
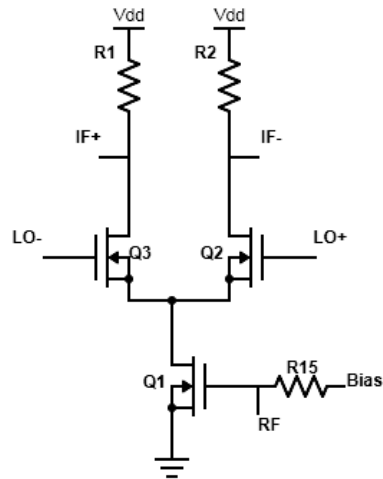
Figure 3.7: Single balanced active mixer, Q1 converts the RF input voltage to current which will split into the differential pair Q2 and Q3, while the resistors convert the output current into a voltage.

Double balanced active mixer
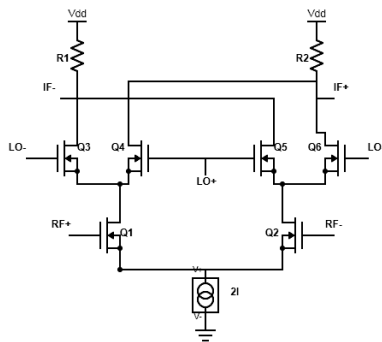
Figure 3.8: Double balanced active mixer, the same principle of operation as single balanced but both RF input and LO signals are differential

Double balanced mixer (also known as Gilbert mixer) provides twice the conversion gain of the single balanced one. Also, there are little RF and LO feed through signals at the IF output ports of the double balanced mixer compared to single balanced [9].

Active mixer Linearity Linearity is a function of the overdrive voltage. The linearity of active mixers degrades if the switching transistors enter the triode region. If both switching transistors operate in saturation, then the division of I_{RF} between the two transistors is given by their transconductance and is independent of their drain voltages. Thus, the LO swings cannot be arbitrarily large, although large LO amplitudes minimize the noise figure [3].

To improve the linearity in Active mixers, degeneration can be implemented by using a resistor, capacitor or inductor. The reactive source degeneration has lower NF than that with resistive degeneration. In general, with active mixers, high linearity is demanding in terms of power consumption [3, 9].

3.2.2 Passive mixers

Passive mixers, also known as switching mixers, are simple in construction. These mixers don't consume any dc power and have conversion loss due to the absence of transconductance stage. The mixer performs a multiplication between the RF signal and the LO signal ideally represented by a square wave switching between +1 and -1. The passive mixers require good switches with minimum on-resistance for reduced conversion loss. Similarly the switch must have a maximum high resistance when off, to provide good isolation. One of the disadvantage in such mixers is the need of large LO drive signal to turn the MOS switches on/off [10].

MOS transistor are very good switches for such high frequency applications. When the MOS transistor is on, it operates in triode region and when off it is in cut off region. For precise switching, ideally, the transistor should be biased such that the gate-source voltage V_{GS} is equal to the threshold voltage V_T of the transistor. The conversion loss is proportional to R_{on} of the switch. The drain-source of passive mixers transistors are slightly biased with positive V_{DS} for optimum conversion loss and optimized IMD performance [10].

Single balanced passive mixers Figure 3.9 shows the single balanced passive mixer. Both the transistors in the mixer switch on alternatively during the positive and negative LO cycles.
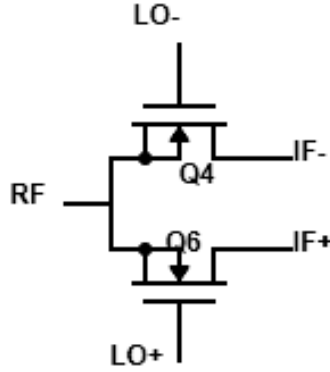
Figure 3.9: Single balanced passive mixer

Double balanced passive mixers A double-balanced passive mixer, as shown in figure 3.10 is adopted in this work. It is composed of four NMOS transistors operating in the linear region. LO, RF, and base-band signals are all differential signals. During the positive LO cycle, the RF is coupled to the IF port with positive phase, whereas during the negative phase, RF is inverted at the IF. Large LO signals are needed for high linearity and minimum conversion loss. The double-balanced structure helps with LO-IF and RF-IF isolation [11].

According to the model in figure 3.10, the conversion gain is given by:

$$Gain = 20log\left(\frac{2}{\pi}(\frac{Z_L}{Z_L + Z_{off} \parallel R_{on}}) - \frac{2}{\pi}(\frac{Z_L}{Z_L + Z_{off}})\right) \tag{3.17}$$
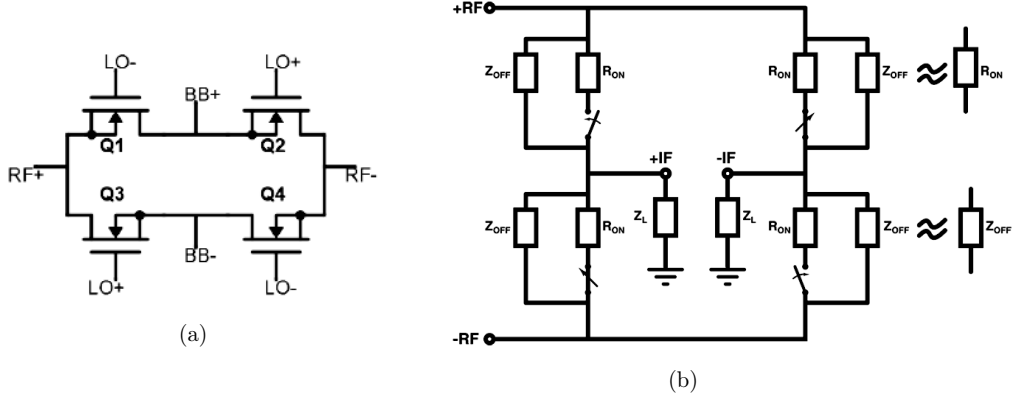
Figure 3.10: (a) Double balanced mixer and (b) the model for it

R_{on} is clearly the limiting factor in obtaining a conversion gain that is as close to the ideal value of $2/\pi$. The tendency is to increase the width of the NMOS in order to reduce the value of R_{on}, however, the intrinsic capacitance increase proportionally to the width, thus reducing the value of Z_{off} and creating a frequency limitation in the mixer [11].

Passive mixer linearity The major source of non-linearity is the transconductance stage. Since there is no transconductance stage and MOS transistor is fairly linear in triode region when switched on, MOS passive mixers exhibit excellent linearity, that is why they are chosen to be implemented in this TOR design, since the linearity is crucial.

For even order nonlinearity cancellation, balanced transmission gate may be used instead of a single NMOS transistor [1, 12].

Port isolation The isolation between LO and RF ports of the mixer is important as LO-to-RF feed through results in LO signal leaking through the antenna. The leaked LO signal should be small enough to avoid corrupting the desired signals of other RF systems. LO-to-IF and RF-to-IF isolations are not important because the high-frequency feed through signals can be rejected by the high IF filter easily. However, large LO and RF feed through signals at the IF output port may saturate the IF output port, and decrease the linearity of the mixer. Leakage of the LO waveform to the input of a mixer is added to the RF signal and mixed with the LO, generating a dc offset at the output. The double balanced mixers are the best to minimize the port to port coupling [9].

Chapter 4

Circuit Analysis

4.1 Attenuator analysis

Pi ant T attenuators are the most common types of digital attenuators, both of them will be analyzed in this chapter, Pi architecture was used in the final design. A differential topology was adopted to reject the in-band common mode coupled RF leakage (RFleak), so as it will not degrade the IMD2 and IMD3 performance.

4.1.1 PI attenuator

Principle of operation

PI attenuator is composed of three digitally controlled NMOS switches and some resistors, as depicted in figure 4.1. When the attenuator is working in the bypass state , the series switch will be conducting while the shunt switches will be completely off. In the attenuation state, the series switch will be off, while the shunt switches will be conducting, the series resistor will determine the amount of the attenuation while the shunt resistors will set the impedance matching [13].
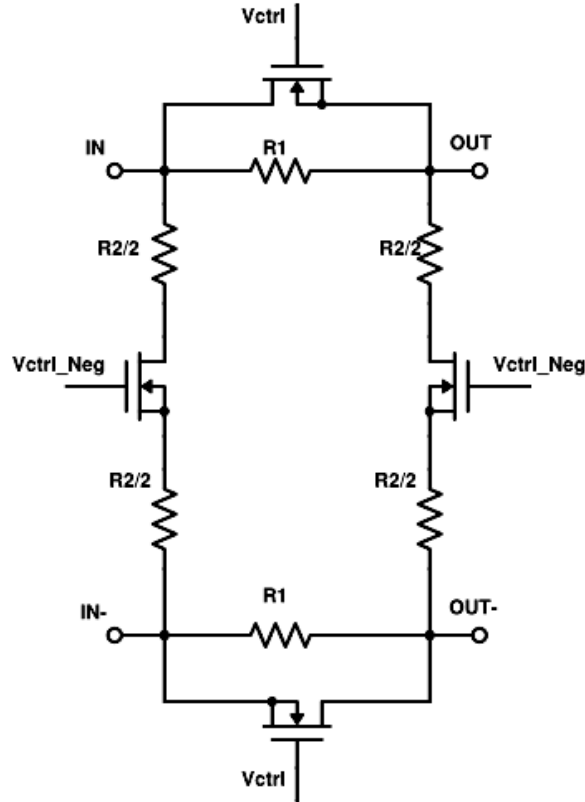
Figure 4.1: Digitally controlled Pi attenuator

The high frequency models and equations are some what similar to the variable Pi attenuator discussed in Chapter 3(Section 3.1.1).

Minimum insertion loss

Can be obtained by minimizing the on resistance of the series switch and the leakage through the off shunt transistor.

Neglecting the effect of the parasitic capacitors in the switches, the values of the resistors can be calculated for the desired attenuation and perfect input and output impedance matching of 100Ω differentially.

By looking at figure 4.2, one can conclude the attenuation and the input and output impedance as follows:

$$Gain(dB) = 10 * log\frac{R2 \parallel 100}{2R1 + R2 \parallel 100} \tag{4.1}$$

$$R_{in} = R_{out} = R2 \parallel 2R1 + R2 \parallel 100 \tag{4.2}$$
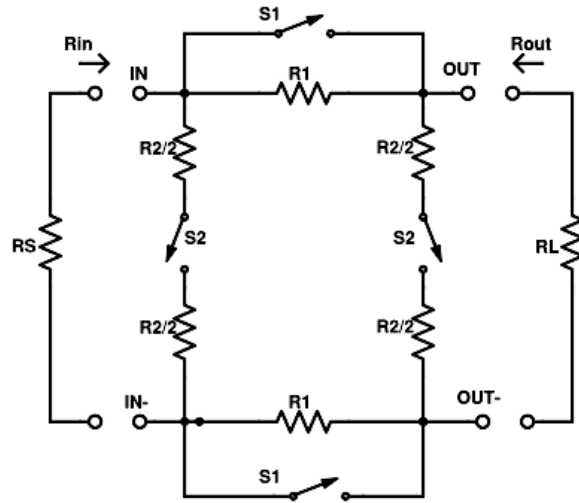
Figure 4.2: Digital Pi attenuator with ideal switches

4.1.2   T attenuator

Princible of operation

T attenuator as depicted in figure 4.3 contains resistive elements which are chosen to ensure that the input impedance and output impedance are matched, while giving the desired attenuation. The switches swap between the attenuation and reference state, when the shunt switch is on and the series is off, the attenuator is in function. Only the series switch is conducting when the reference state is required. A digital input drives the switches with either 0 or 1.2V, according to the situation. Unlike the Pi attenuator where the series resistors determine the attenuation while the shunts are for impedance matching, all the resistors here are effective for the attenuation and impedance matching [14, 15].

Minimum insertion loss

Choosing larger widths for the series switches will improve the insertion loss in the reference state by minimizing the triode resistance of the transistors. On contrary, the parasitic capacitances of the switches will also contribute to the bypass loss.
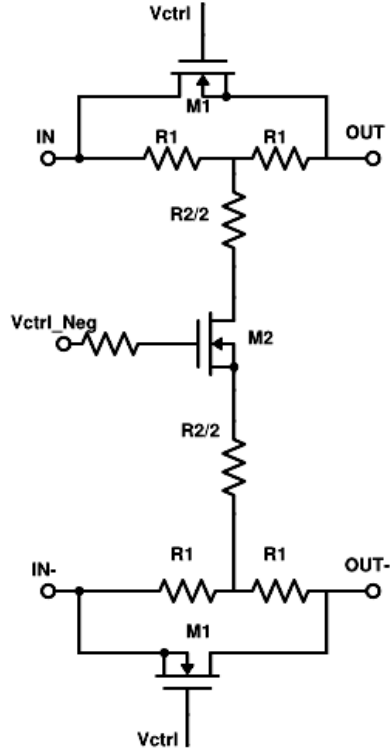
Figure 4.3: Digital T attenuator

Assuming ideal switches, the equations for input, output impedances and attenuation can be characterized as follows:

$$R_{in} = R_{out} = 100 + 2R1 \parallel R2 + 2R1 \tag{4.3}$$

$$Gain(dB) = 10 * log\left(\left(\frac{(100 + 2R1) \parallel R2}{(100 + 2R1) \parallel R2) + 2R1}\right)\left(\frac{100}{100 + 2R1}\right)\right) \tag{4.4}$$

High frequency models and equations are similar to the variable T attenuator discussed in Section 3.1.1.

4.1.3 Linearity analysis

Digital controlled attenuators are highly linear because of the large gate voltage, which results in high intercept points. For both Pi and T attenuators, at any time, part of the transistors will be in deep triode region while the others will be off. The dominant nonlinearity is the third-order output conductance nonlinearity for the transistors in

deep triode. In general, the wider the transistors, the better the linearity up to certain sizes.

The MOS transistor resistive nonlinearity can be extracted in many ways in time domain or in frequency domain. A PSP model is used in this thesis work because it is able to correctly fit at least up to the third derivative and accurately smoothen measurement results [16].

Assuming minimum transistor length, and very wide transistors, the nonlinearity parameters will depend on port voltages, and thus the attenuation level, the higher the attenuation, the more nonlinear the circuit becomes. A slight dc bias on the port sides will improve the linearity. Also, a large resistor is usually used in series with the gates to minimize the source-gate voltage swing, and hence improve the linearity.

4.2   Mixer analysis

A double balanced passive mixer is used in this work, since it is the best for achieving the required high linearity while minimizing the port to port coupling. Different variants were compared, the mixer using dummy switches, the mixer with out dummies and the mixer using pass transistor logic or transmission gates. Also, the mixer in both voltage and current mode is tested. It is worth mentioning that image rejection is not of any importance in TOR, since any uncorrelated data will be suppressed by the digital pre-distortion algorithms.

4.2.1   Dummy switch technique

This technique comprises adding one dummy transistor at the source side of the basic transistor, and another one at the drain side. The active switch and dummies are switched with inverted gate voltages. Figure 4.4 shows how the dummies are connected to the active transistor. Each dummy transistor is injecting half of the active transistor's channel charge but with opposite signs. If the impedances on the drain and source side of the switch are identical, this means that the active switch pushes exactly half of its stored channel charge into each side, where it can be completely compensated by the dummy transistors. The dummy is usually designed half as wide as the active switch, which results in a gate capacitance of $C_{G,dummy} = C_{G,active}/2$. Since the drain and source terminals of the dummy are connected together, it acts simply as a capacitor. The channel charge partitioning of the active switch depends in general on V_s and V_d and the switch-off slope [17]. In this work, half width did not give the perfect results, so, the widths of the dummies were swept to find the optimum width that will cancel the capacitance. Canceling capacitance is essential in our TOR design, since good LO to RF isolation is required.

(a) Dummy switch configuration

(b) The capacitance when the active switch in the 'ON' state

(c) The capacitance when the active switch in the 'OFF' state
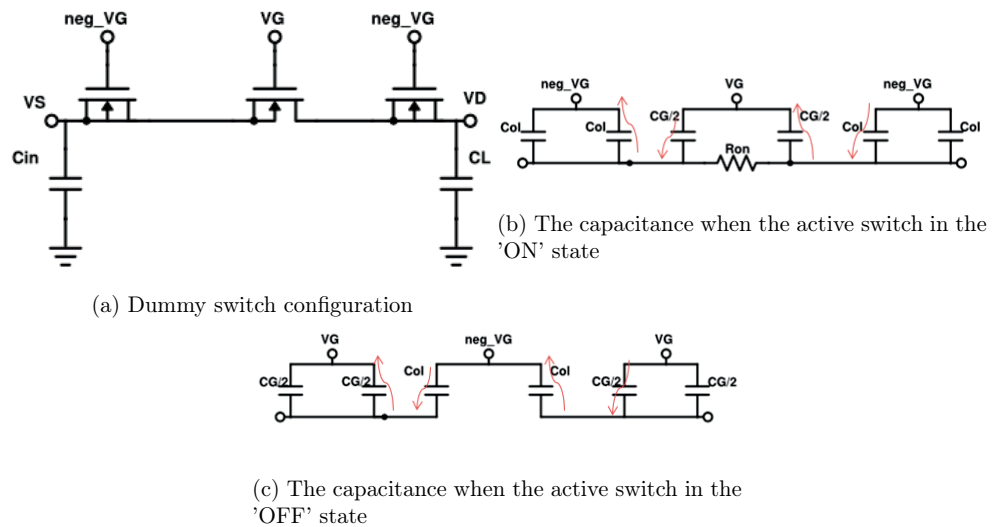
Figure 4.4: Capacitance cancellation using dummy switches, the arrows show the direction of charge flow

4.2.2   LO isolation

The emission at the antenna of this TOR mainly arises from the mixer. Recalling from the target specifications chapter, that the required overall out of band emission at the antenna is to be below the noise floor over relevant bandwidth, which is estimated

to be -100dBm, poses a challenge in mixer design, but the fact that there is a filter prior to the antenna, and 20dB attenuation in the coupler which feeds the PA output to the TOR will relax the LO isolation requirements in the mixer. Thanks to the symmetrical attenuator, at the worst case, the signal emitted from the mixer will be attenuated by attenuator insertion loss value before passing through the coupler and filter to the antenna.

4.2.3   Linearity

The design bottleneck is the linearity performance of the mixer. Passive mixers have the highest dynamic range among the other mixer implementation options. The non-linearity in a passive mixer which is driven by a square-wave LO is mainly due to the switching transistors and the modulation of R_{on} by higher input signal levels. Non-linear device capacitances will degrade the linearity as the frequency gets comparable to the transistor unity current gain frequency (f_T), the mixer linearity performance degrades due to the nonlinear charging and discharging of the gate to source and gate to drain capacitors. The nonzero rise and fall time of the LO will also come in to play to make the linearity worse at very high frequencies [18].

By using the CMOS switch(see figure 4.5b), the dynamic range in the passive mixer can be improved due to the distortion cancellation of even order nonlinearity. If the NMOS and PMOS device are matched and biased at the same operating point, the second harmonics will be canceled. Therefore, in an ideal situation without any mismatch, the linearity of a passive mixer can be improved by using a CMOS [1].

When it comes to linearity analysis, either for mixer or attenuator, it is essential to choose the correct MOS model for nonlinearity, so, the latest surface potential-based model, PSP is selected for accurate results. Other models have some discontinuities in the higher order derivatives of drain current, and hence will not give good results [16].
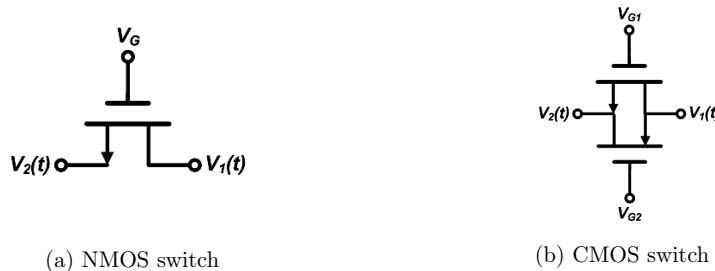

(a) NMOS switch

(b) CMOS switch

Figure 4.5: Different switch implementations for mixer [1]

Also, a significant IIP3 performance improvement in the mixer can be obtained with low LO amplitudes, but then the conversion loss will get higher, and this loss should be avoided in the mixer [19].

Voltage versus current mode mixer linearity

In current mode mixer, low pass filters are realized by trans-impedance amplifiers (TIAs). The output of the mixer including both the in-band signal and out-of-band interferer is fed to the TIA input as current waves. The common-mode feedback loop of the TIA provides the dc bias to the input and output terminals of the mixer. The signal amplification and channel selection are delayed after the filtering of the blockers and unwanted signals, and hence high linearity can be achieved [20]. Also, the source has a large output impedance whereas the load has an input impedance that is very small, this leads to a small voltage swings in a current-mode passive mixer. Small voltage swings minimize the MOSFET nonlinear transconductance and on-conductance effect. The current-mode mixer should therefore be more linear than its voltage mode counterpart. Resistors in series with the mixer switches are connected in current mode mixers for further linearity improvement. If the series resistors are large in comparison to the on-conductance, the switch characteristics will then be largely defined by the resistors. More over, the series resistors give the mixer core a higher output impedance as seen from the input of the TIA which lowers its noise contribution. It should however be mentioned that the resistor itself will contribute to noise in the mixer circuit which may degrade the total noise figure [21]. Fortunately, noise figure is not a critical issue in the TOR.

Never the less, in such a wide-band low IF TOR, it is difficult to design a TIA with good dynamic range without consuming large power. Voltage mode mixers, on the other hand, are more power efficient, since they eliminate the need for TIA, but have lower linearity. Figure 4.6 gives a clue about both kinds of mixers.

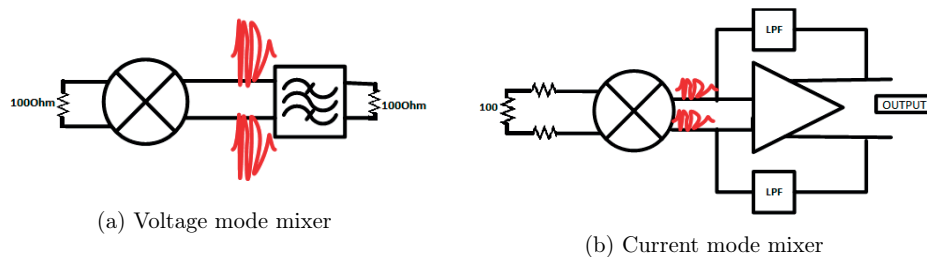(a) Voltage mode mixer

(b) Current mode mixer

Figure 4.6: Mixer in voltage and current mode

In this thesis work, both current and voltage mixers are implemented, but the final solution exploits the voltage mode mixer to eliminate the need for TIA and enable the use of a passive filter to filter unwanted signals, hence achieving the required linearity at no power consumption cost.

Chapter 5

Circuit Design

5.1 Attenuator design

The attenuator is a necessary part of the transmission observation receiver since the input power levels vary in a relatively wide range, the attenuator will ensure that the input power to the mixer is always low enough so as the mixer nonlinearities will not affect the performance.

5.1.1 Target specifications

The specifications for the attenuator are listed in Table 5.1

Table 5.1: Target specifications for attenuator

Parameter	Target
S11,S22	$< -10dB$
SFDR	<-90dBc
IIP3	>20dBm
RF frequency range	2GHz to 7GHz
Input power levels	-30 to +1dBm
Output power levels	<-30dBm
S21,S12	1-31dB
Insertion loss	The lowest possible value
Phase shift	$< 5deg$
Amplitude variation over 1GHz interval	$\leqslant 0.2dB$

5.1.2 5-Bit Digital step attenuator

The design comprises of 5 stages of R-to-R attenuators, PI attenuator type is implemented. Each stage is optimized individually to achieve certain level of attenuation.

then all the stages were integrated together. A high level view is provided in figure 5.1. The attenuator provides attenuation from 1dB to 31dB in 1dB steps using digital input control word.
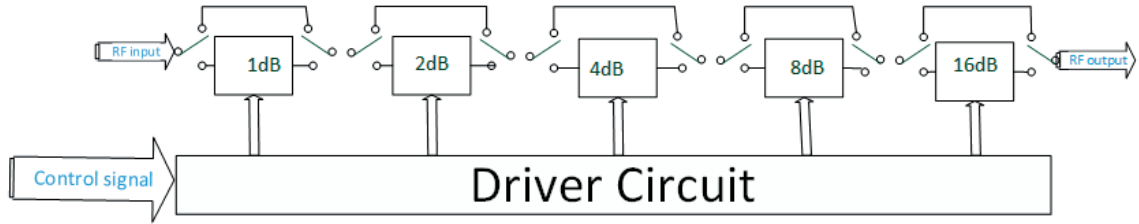

Figure 5.1: Block Diagram of 5 bit digital step attenuator

Table5.2 provides the control signals combinations and the corresponding level of the attenuation. In the subsequent sections, each stage design parameters and the

Table 5.2: Attenuation levels based on the control signals

Control word	Attenuation(dB)
00000	0
00001	1
00010	2
00011	3
.....	.....
......	......
11111	31

results will be presented. The important parameters to keep track of while designing each stage were the insertion loss, phase shift, precision over the frequency, input and output matching and linearity. All these parameters should be within the acceptable range, which was challenging since most of them were contradicted.

A resistor in series with each gate was included to help reducing the variation of amplitude over frequency range by shifting the poles to higher frequencies and improve the linearity by doing bootstrapping, since the gate voltage will no longer be shorted to ground after the addition of the gate resistor. Figure 5.2 shows how each stage will look. The design starts by calculating the resistors R1 and R2 based on equation (4.1) and equation (4.2), and plugging them into the circuits. NMOS switches were used to implement the attenuators due to their lower R_{on} and parasitic capacitance. R_{gate} is set to very large value, and then simulations were carried out to come up with suitable widths of the switches to meet all the specifications. Each stage

was optimized to give exactly the desired attenuation at 4.5GHz, the attenuation will deviate a bit from this value as the frequency changes. The precision of the amplitude will be given in the tables for each stage. Due to the circuit symmetry, S11 is equal to S22 while S21 is equal to S12.

Generally, there was a contradict between the matching, loss and linearity. Simulations show that linearity gets better with wider transistors. Optimizing the linearity deteriorates the matching and bypass loss and vice versa, so, the design task was challenging. Since linearity is the main concern of the TOR, relatively larger widths were chosen for meeting the linearity requirement, although they led to higher loss.

It was observed that as the attenuation gets higher, linearity gets worse, since the swing difference between the source and drain of the transistors will get larger which gives rise to distortion currents.

The results were taken with an applied input frequency of 7GHz, with a blocker at 10MHz offset to measure the nonlinearities, LO signal of 6.01GHz and IF of 990MHz. According to the simulation, the higher the frequency, the worse the phase shift and amplitude precision, and since the precision on gain and phase is important over the band of observation which is 1GHz, these quantities were evaluated between 6GHz and 7GHz. The results for each stage as well as for the integrated attenuator are summarized in the following figures and tables.
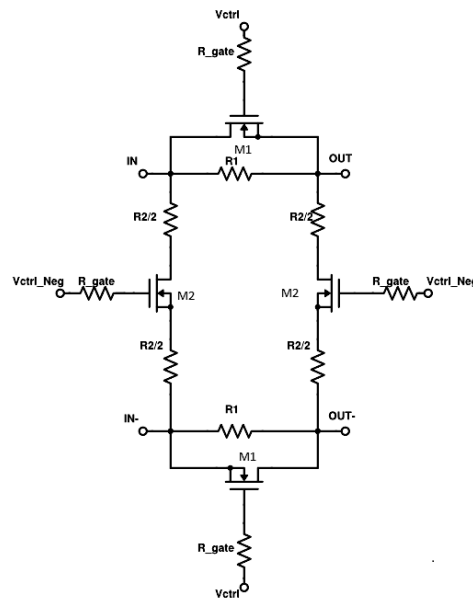

Figure 5.2: Pi stage

1dB stage

Design parameters The design parameters are summarized in Table 5.3

Table 5.3: Design parameters for 1dB stage

Parameter	Value
M1 (W/L)	130/0.06
M2(W/L)	100/0.06
R1	13.6Ω
R2	4KΩ
R_{gate}	10kΩ

Results

Table 5.4: Results for 1dB stage

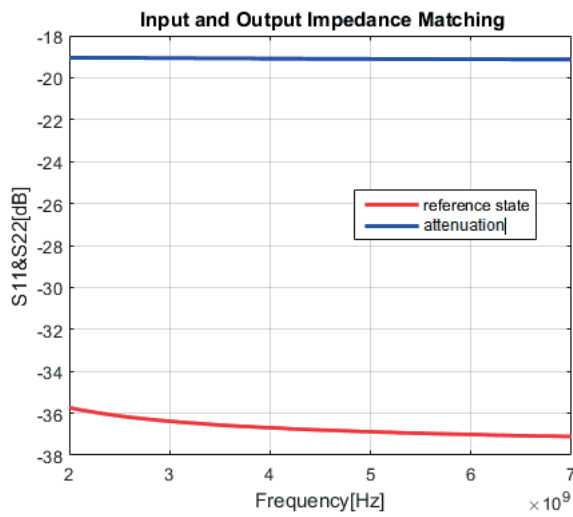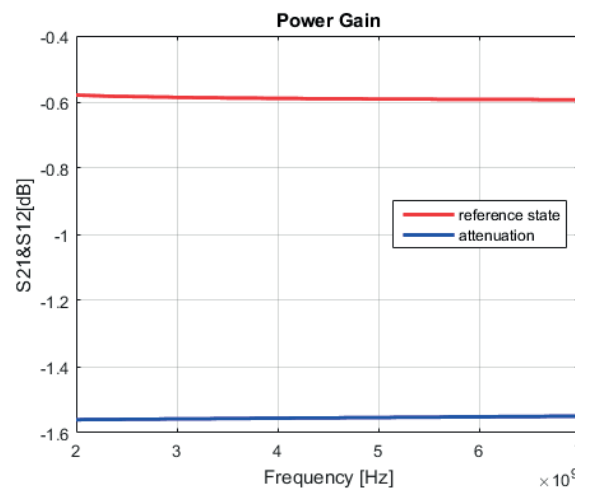|	Reference state	Attenuation state
Worst phase shift within 1GHz interval	11mDeg	0.106Deg
Amplitude variation within 1GHz interval	922udB	2.05mDB
IIP3	42.67dBm	61.47dBm

Figure 5.3: S11/1dB Stage

Figure 5.4: S21/1dB Stage

2dB stage

Design parameters The design parameters are summarized in Table 5.5

Table 5.5: Design parameters for 2dB stage

Parameter	Value
M1 (W/L)	400/0.06
M2(W/L)	400/0.06
R1	22.3Ω
R2	850 Ω
R_{gate}	10kΩ

Results Table5.6 gives the results of 2dB stage. Also the figures emphasize S parameters results.

Table 5.6: Results for 2dB stage

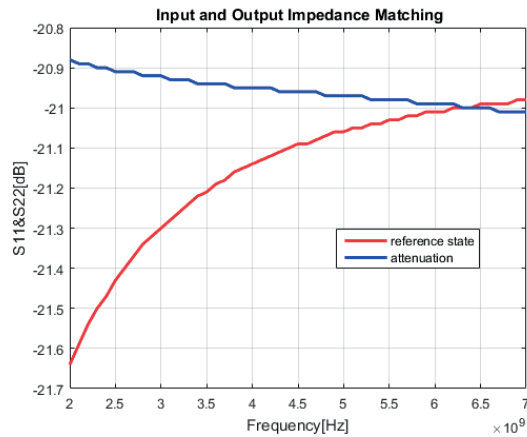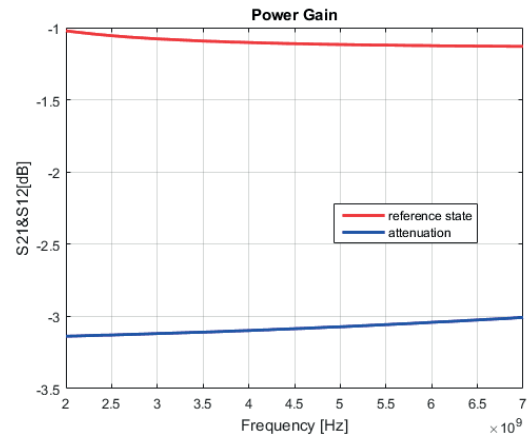|	Reference state	Attenuation state
Worst phase shift within 1GHz interval	9.87mDeg	0.672Deg
Amplitude variation within 1GHz interval	5mdB	34mdB
IIP3	51.29dBm	52.14dBm

Figure 5.5: S11/2dB Stage

Figure 5.6: S21/2dB Stage

4dB stage

Design parameters The design parameters are summarized in a Table 5.7

Table 5.7: Design parameters for 4dB stage

Parameter	Value
M1 (W/L)	170/0.06
M2(W/L)	200/0.06
R1	44.2Ω
R2	433Ω
R_{gate}	10kΩ

Results

Table 5.8: Results for 4dB stage

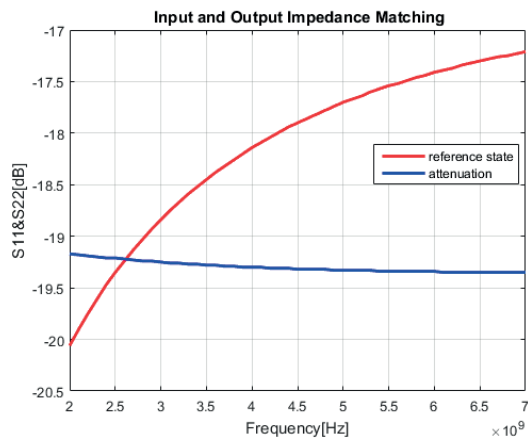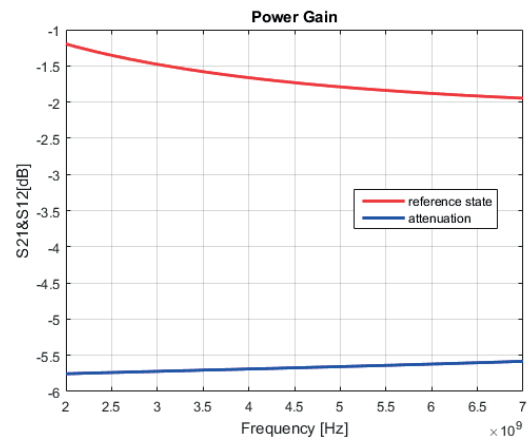|	Reference state	Attenuation state
Worst phase shift within 1GHz interval	41mDeg	0.8Deg
Amplitude variation within 1GHz interval	66mdB	38mdB
IIP3	41.8dBm	46dBm

Figure 5.7: S11/4dB Stage

Figure 5.8: S21/4dB Stage

8dB stage

Design parameters The design parameters are summarized in a Table 5.9

Table 5.9: Design parameters for 8dB stage

Parameter	Value
M1 (W/L)	300/0.06
M2(W/L)	50/0.06
R1	64.3Ω
R2	207Ω
R_{gate}	10kΩ

Results

Table 5.10: Results for 8dB stage

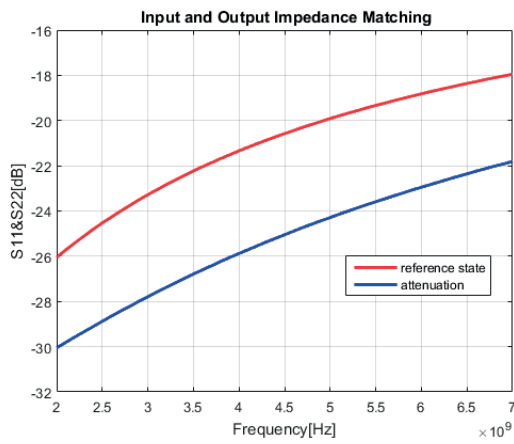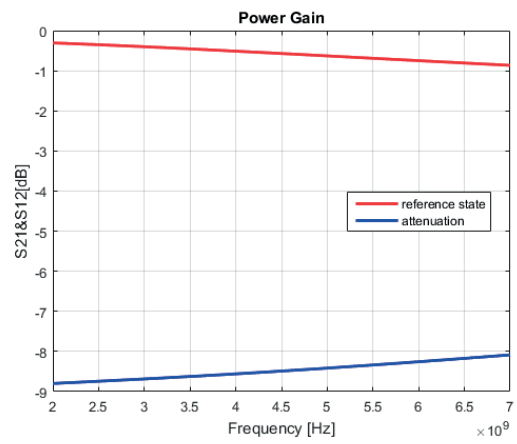|	Reference state	Attenuation state
Worst phase shift within 1GHz interval	23.6mDeg	1.8Deg
Amplitude variation within 1GHz interval	0.116dB	0.171dB
IIP3	29.9dBm	39.06dBm

Figure 5.9: S11/8dB Stage

Figure 5.10: S21/8dB Stage

16dB stage

Design parameters The design parameters are summarized in Table 5.11

Table 5.11: Design parameters for 16dB stage

Parameter	Value
M1 (W/L)	100/0.06
M2(W/L)	73/0.06
R1	155.2Ω
R2	101Ω
R_{gate}	10kΩ

Results

Table 5.12: Results for 16dB stage

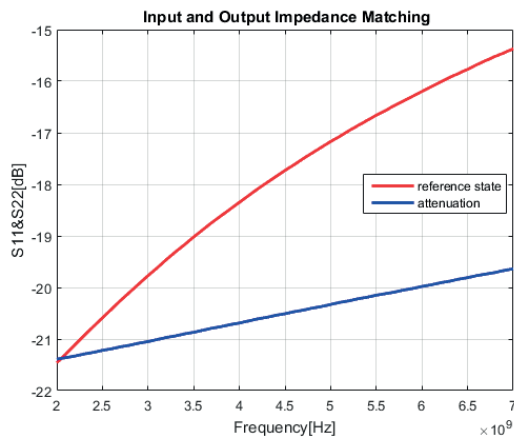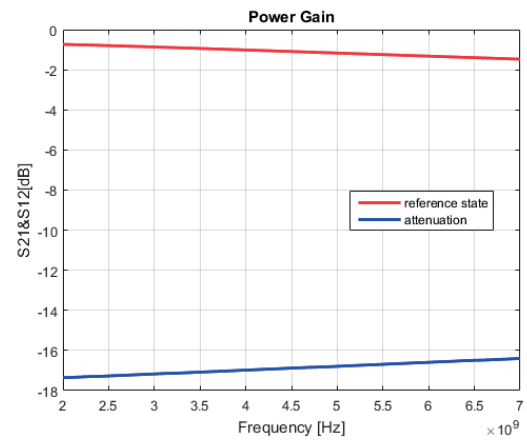|	Reference state	Attenuation state
Worst phase shift within 1GHz interval	0.122Deg	2Deg
Amplitude variation within 1GHz interval	0.152dB	0.196dB
IIP3	28.13dBm	32.77dBm

Figure 5.11: S11/16dB Stage

Figure 5.12: S21/16dB Stage

The 5-bit integrated digital step attenuator

Design procedure The 5 stages were integrated together and a driver circuit was used to provide the control signals. Common Mode input voltage was used in the input and output of the differential circuit, to improve the linearity and impedance matching, since the biasing will determine the capacitance and hence the input and output impedance matching. The stages were ordered starting with the highest linear

first, to ensure the highest possible linearity(see Section 2.2.4). The order was 1 2 4 8 16.

Driver circuit An analog input was fed to an analog to digital converter (ADC) to provide the digital input stream to control the circuit level of attenuation. After integration, some resistors values were tweaked to maintain the performance, so the attenuation at 4.5GHz is optimal in all cases.

Results The following figures show the overall attenuation, precision, impedance matching and linearity versus all the different combinations of the control signals. All the results were collected when applying an input frequency of 7GHz. As in each individual stage, the precision was calculated as the difference in the amplitude between 6GHz and 7GHz as the worst case variation. The spurious free dynamic range was good only for low input powers and low attenuation settings or high input powers with high attenuation settings as will be illustrated in the figures. So, in order to meet the specification of -90dBc, when the input power is high, the attenuation should be set to large value. This makes sense since the attenuator is mainly introduced to reduce the large input powers, so as the mixer afterwards would not compress due to its nonlinearity.
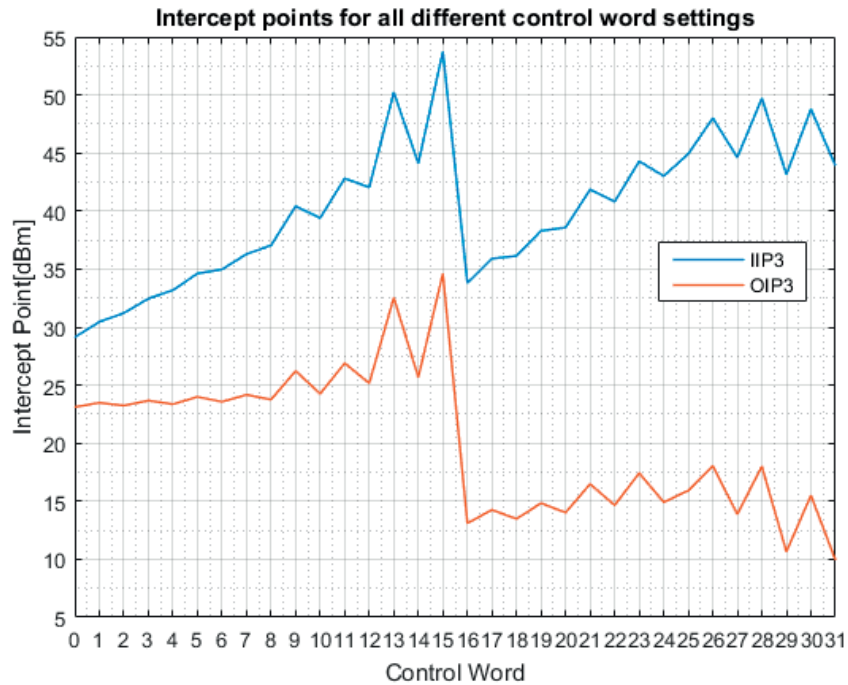
Figure 5.13: Intercept points versus control words

By referring to Equation 2.27, Section2.2.3, it is concluded that the IMD3 level is well below the required specifications of -90dBc for all IP3 values in the figure 5.13, given that, the attenuator should be set to get an output power of -30dBm for all different input power levels.
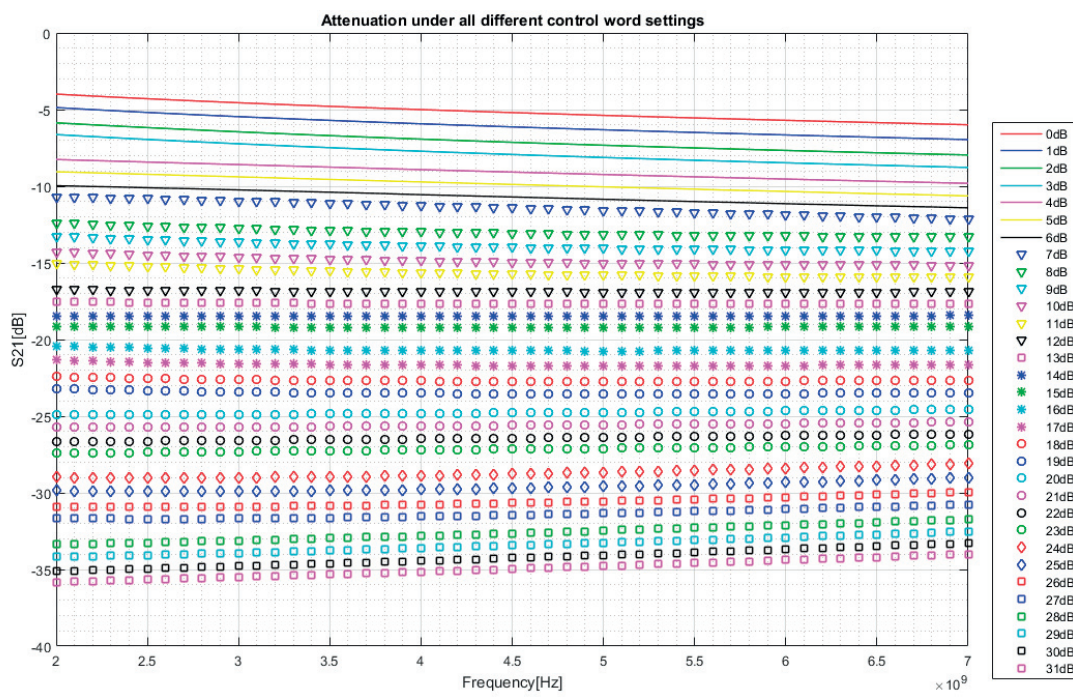
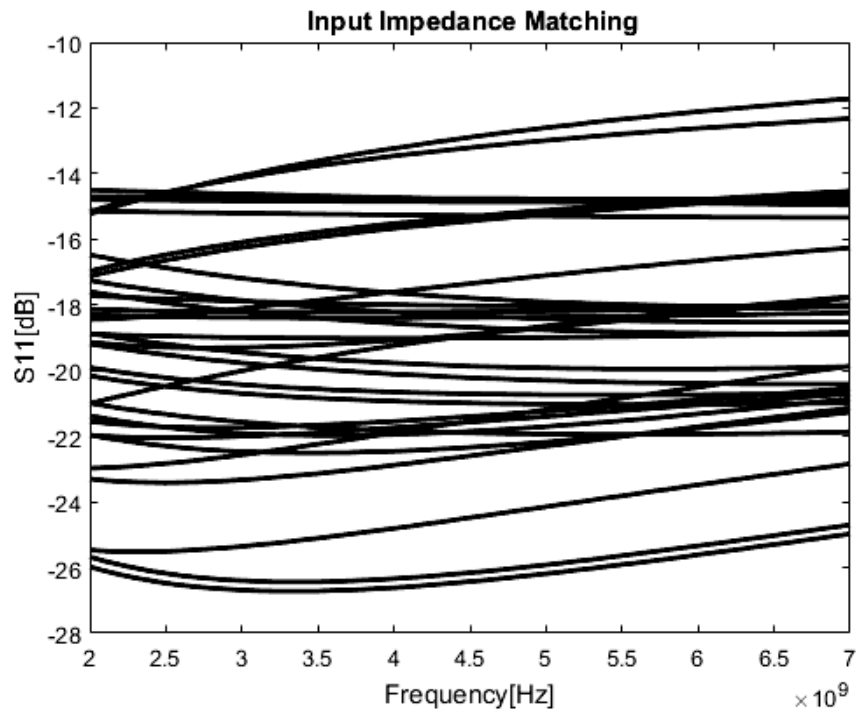Figure 5.14: Attenuation versus frequency under different attenuation levels

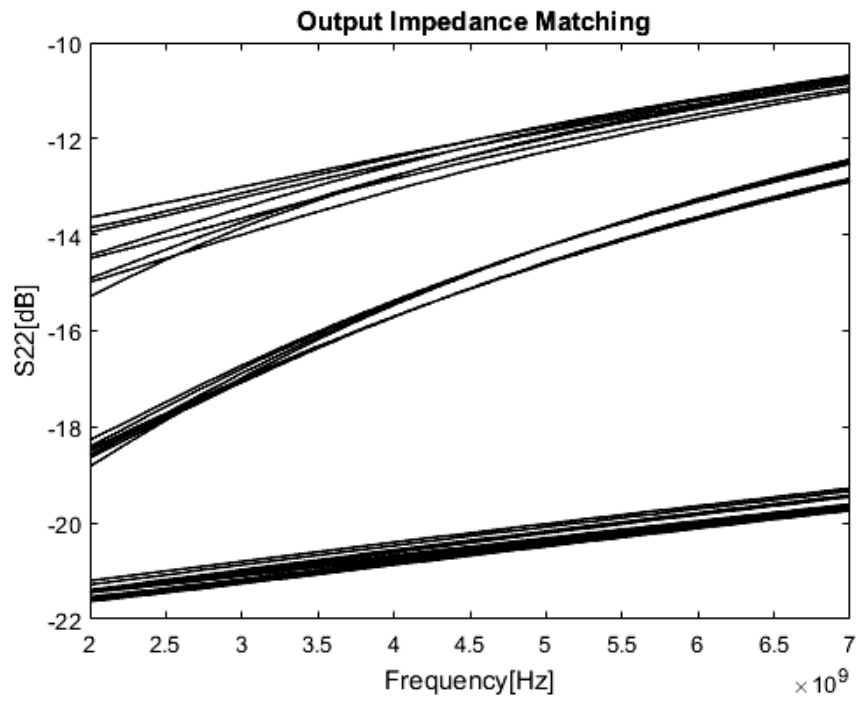Figure 5.15: Input matching for different attenuator settings

Figure 5.16: Output matching for different attenuator settings
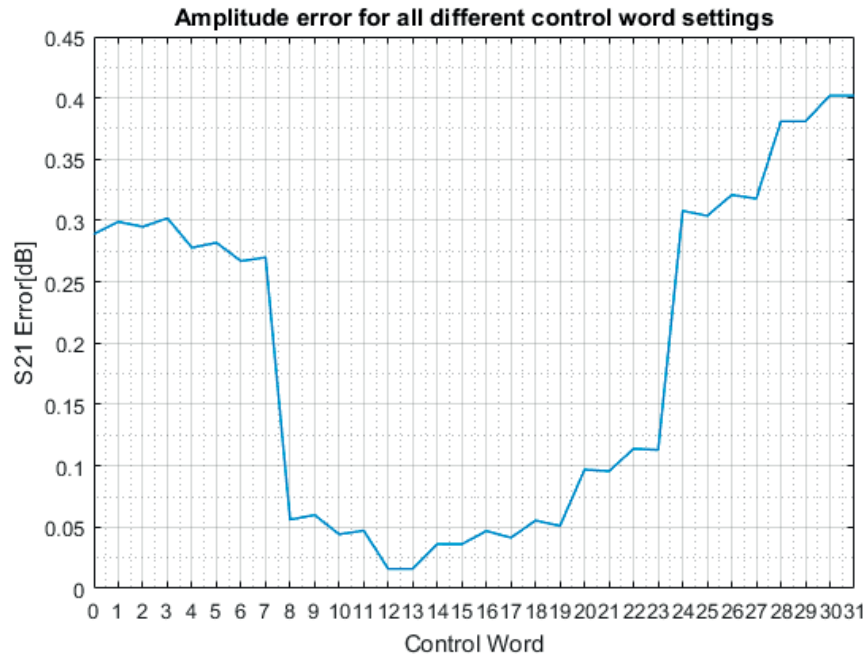
Figure 5.17: Amplitude variation from 6GHz to 7GHz under different control words
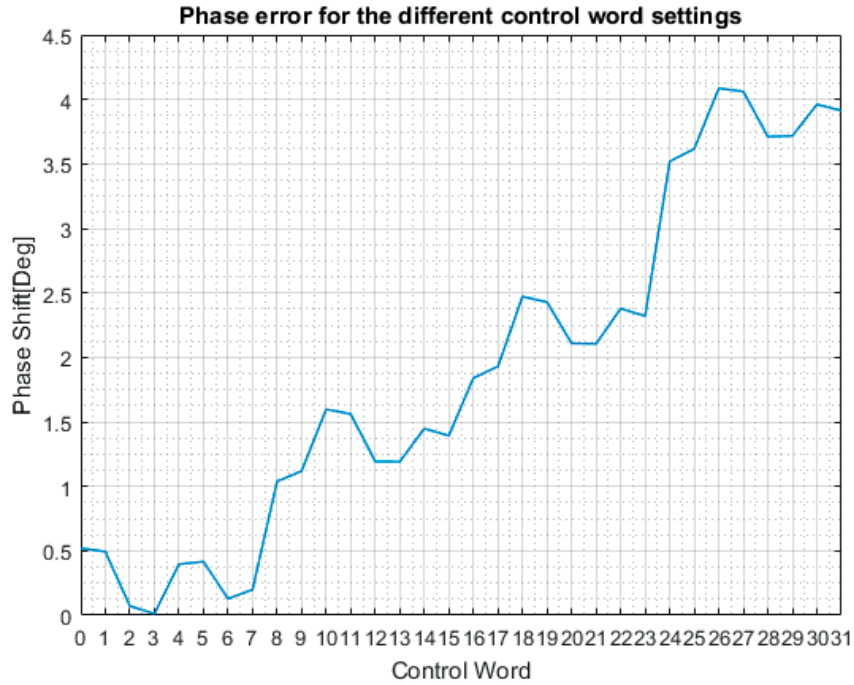
Figure 5.18: Phase variation from 6GHz to 7GHz under different control words

Conclusion The total insertion loss of this attenuator is about 5dB. The input and output impedance matching meet the specification of less than -10dB. The amplitude error deviates from the desired error of 0.2dB stated in the specifications. Methods to improve that will be given in the Future work chapter. The phase error is within the accepted range. The IIP3 shows much better values than what is targeted.

5.2   Mixer design

The mixer is the bottle neck for linearity in this passive TOR, so the input power levels should be kept low to improve the dynamic range, and that is the main purpose of the preceding attenuator. The important parameters to keep track of while designing a mixer is the conversion loss due to the passive nature of the mixer, the LO to RF coupling, since it will radiate through the antenna and form an interferer to other systems in the base station. The LO to IF and RF to IF are benign since they can be easily filtered afterward. The input and output impedance matching is also of interest. The specifications of the mixer are shown in Table 5.13

5.2.1   Target specifications

Table 5.13: Target specifications for the mixer

Parameter	Target
S11,S22	< -10dB
SFDR	<-90dBc
IIP3	$> 10 dBm$
RF frequency range	2GHz, 4.5GHz, 7GHz
LO frequency range	1.72GHz, 3.86GHz, 6.01GHz
IF frequency range	280MHz, 640MHz, 990MHz
Input power levels	$< -30 dBm$
S21,S12	The lowest possible loss(dB)
Phase shift	$< 1 Deg$
Amplitude variation over 1GHz interval	$< 0.2 dB$
LO to RF coupling	$< -50 dBm$

Different ways of implementing a mixer were explored and compared, including voltage mode mixer, current mode mixer, and quadrature mixer technique. A small DC bias for the gates of the mixers is applied in all the cases to improve linearity and impedance matching.

5.2.2   Voltage mode mixer

Design procedure A basic mixer was designed, its performance was compared to a design with transmission gates and the design with dummy switches. A dummy switch technique was adopted in the final design of the mixer because it gives the best results for LO isolation by providing opposite capacitance polarity.
The common mode voltage and gate biasing are swept and tweaked to get the best

possible combination of impedance matching and linearity.

Design parameters

Table 5.14: Design parameters for the mixer in voltage mode

Parameter	Value
(W/L) for all switches	40/0.06
common mode voltage	0.4V
DC bias at the gates	0.3V

Mixer with dummy switches The dummy switches suppressed the LO level at the input RF port to below the noise floor, but still there was a spur at 2LO - RF, this spur will be filtered away with the pre-antenna filter, since it is less than -55dBm for all the different input frequencies. The dummy switch mixer is depicted in figure 5.19
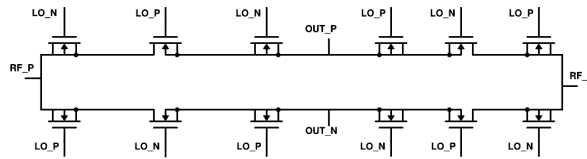

Figure 5.19: Double balanced passive mixer using dummy switches to improve LO to RF isolation

The results of implementing a mixer with dummies are summarized in Table5.15

Table 5.15: Results for mixer in voltage mode, using dummy switches

	7GHz	4.5GHz	2GHz
Input power(dBm)	-30	-30	-30
IIP3(dBm)	10.5	11.2	11.8
IMD3(dBc)	-81	-82.3	-83.6
LO to RFleakage(dBm)	-115.5	-111.7	-110.6
(2LO - RF)leakage	-56	-59.7	-64.6
S11(dB)	-12.3	-13.4	-14.6
S22(dB)	-12.5	-13.8	-14.7
S21(dB)	-6.8	-6	-5.6
S21 error over IF bandwidth (dB)	-0.14	-0.1	-0.03

CMOS mixer   The mixer is also implemented with the transmission gates as illustrated in figure 5.20, both NMOS and PMOS transistors were equally sized, and the results were collected and listed in Table5.16
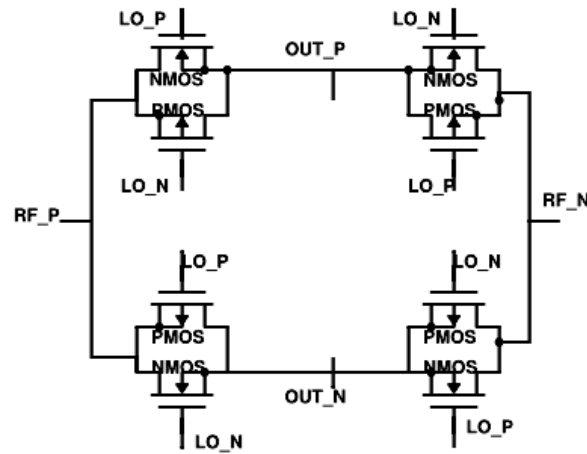

Figure 5.20: Double balanced passive CMOS mixer

Table 5.16: Results for CMOS mixer in voltage mode

	7GHz	4.5GHz	2GHz
Input power(dBm)	-30	-30	-30
IIP3(dBm)	11.3	11.6	14.6
IMD3(dBc)	-82.5	-83.2	-89.3
LO to RFleakage(dBm)	-39	-45.3	-58.8
S11(dB)	-11.6	-13.2	-14.6
S22(dB)	-15.4	-15.2	-15
S21(dB)	-6.1	-5.7	-5.5

A very slight improvement on linearity is observed when using the CMOS mixer, but the LO emission is large and does not meet the final specifications.

Basic mixer The results of the implementation of the basic double balanced passive mixer of 4 NMOS switches (see figure 5.21) are listed in Table 5.17
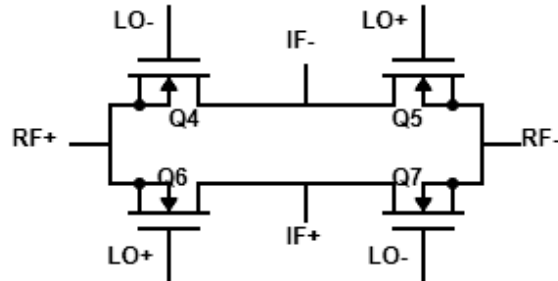
Figure 5.21: Basic double balanced passive Mixer

Table 5.17: Results for basic mixer in voltage mode

	7GHz	4.5GHz	2GHz
Input power(dBm)	-30	-30	-30
IIP3(dBm)	11.1	11.4	13
IMD3(dBc)	-82.2	-82.8	-86
LO to RF leakage (dBm)	-38.6	-45.5	-59.14
S11(dB)	-13.1	-14	-14.7
S22(dB)	-14.1	-14.5	-14.8
S21(dB)	-5.9	-5.6	-5.5

This implementation also failed to meet the out of band emission at the antenna due to large LO coupling.

5.2.3   Quadrature mixer

Quadrature mixer is formed of two mixers, in phase and quadrature phase mixer. Each mixer is fed with the differential RF signals and two LO signals with 180°phase shift. The I- channel mixer is fed with 0°and 180°while the Q-channel mixer is fed with 90°and 270°phase shifted signals. Ideal non-overlapping LO signals of 25%duty cycles each are used to drive the mixers, with some small rise and fall times to emulate the real quadrature LO signals. In order to maintain an acceptable impedance matching, a small resistor was introduced in the input of the mixer, as shown in the figure 5.22. The quadrature mixer was implemented in voltage mode. The results with/without using dummy switches were compared.
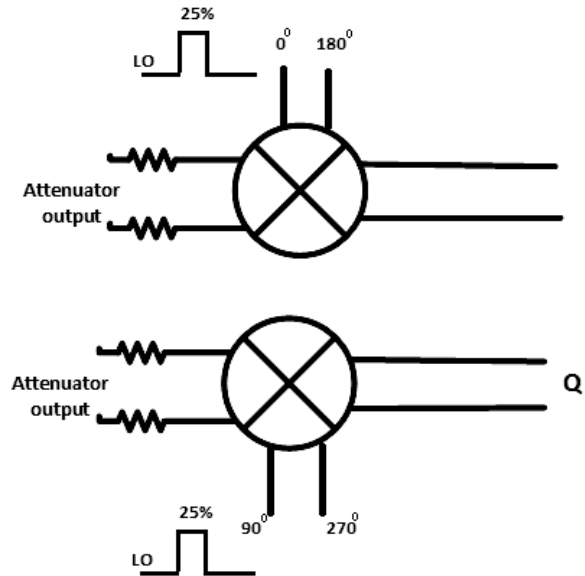
Figure 5.22: Quadrature mixer implementation

Design Parameters

Table 5.18: Design parameters for quadrature mixer in voltage mode

Parameter	Value
(W/L) for all switches	50/0.06
common mode voltage	0
DC bias at the gate	0.3V
R_{match}	16Ω

The results of implementing a quadrature mixer in its simple form are listed in Table 5.19

Table 5.19: Results for basic quadrature mixer in voltage mode

	7GHz	2GHz
Input power(dBm)	-30	-30
IIP3(dBm)	8.2	9.3
IMD3(dBc)	-76	-78.5
LO to RF leakage(dBm)	-38.6	-39.5
S11(dB)	-18.6	-18.9
S22(dB)	-12.1	-8.2
S21(dB)	-11.5	-9.6

Quadrature mixer with dummy switches
The quadrature mixer is also implemented with dummy switches, as Table5.20 displays.

Table 5.20: Results for quadrature mixer with dummy switches in voltage mode

	7GHz	4.5GHz	2GHz
Input power(dBm)	-30	-30	-30
IIP3(dBm)	12.2	10.6	9.7
IMD3(dBc)	-84.4	-81.2	-79.5
LO level at the input (dBm)	-	-	-
2LO-RF level at the input (dBm)	-	-	-
4LO-RF level at the input (dBm)	Out	-65.3	-58
S11(dB)	-15	-18.1	-22
S22(dB)	-19.4	-30.5	-12.7
S21(dB)	-13.4	-11.4	-9.8

(Out) in Table5.20 means that 4LO-RF when the input frequency is 7GHz is at around 17 GHz, which is far away and will be totally suppressed by the antenna.

Comparison It can be seen that the dummies suppressed the LO coupling while the quadrature architecture eliminates the spurs at 2LO -RF. At 4LO-RF, there is a spur but it is still within the range of the values that can be below noise floor after filtering. The results also show that the linearity is much better when using the dummy switches with the quadrature mixer compared to a quadrature mixer with out dummies. The conclusion is that the dummies are important for quadrature implementation in voltage mode. Since this circuit is susceptible to mismatches, a Monte-carlo simulation was carried out to check the levels of (4LO -RF) at 2GHz and 4.5GHz. The results are given in Table5.21. The minimum and maximum levels are calculated as the $(Mean - 6*\sigma)$ and $(Mean + 6*\sigma)$ respectively where σ is the standard deviation.

Table 5.21: Monte-carlo results for LO leakage in quadrature mixer

	Mean(dBm)	Min(dBm)	Max(dBm)
2GHz	-58.05	-58.1	-58
4.5GHz	-65.3	-65.3	-65.2

According to the data in Table5.21, the LO leakage will not be affected with mismatches.

5.2.4   Current mode mixer

Current mode mixer is implemented and its linearity is tested with an ideal TIA circuit. A resistor in series with the mixer is connected for degeneration.
Design parameters

Table 5.22: Design parameters

parameter	value
W/L	30/0.06
R-series	500Ω
R-ideal TIA	500Ω

Results The results are given in Table5.23 for different frequencies.

Table 5.23: Current mode mixer linearity results

	2GHz	4.5GHz	7GHz
IIP3(dBm)	24	21.5	19.3
IMD3(dBc)	-108.6	-103	-98.6
LO leakage(dBm)	-74	-75	-75
S11(dB)	-28.8	-28.8	-29
S21(dB)	-5.8	-6.4	-7
S21 error(dB)	-59m	199m	370m

Significant improvement in linearity is observed in comparison with voltage mode mixer which complies to the theory. But the current mode mixer needs a TIA afterwards which will consume large current to be linear for the whole targeted bandwidth. Therefore, this circuit was not selected for the final design.

5.2.5 General comparison table

Table 5.24 compares the performance of all the investigated mixers with an input frequency of 7GHz and an input power of -30dBm :

Table 5.24: General comparison between mixers

	Voltage mode mixer					Current mode mixer
	Without dummies	With dummies	CMOS mixer	Quadrature mixer		
				Without dummies	With dummies	
IIP3(dBm)	11.1	10.5	11.3	8.2	12.2	19.3
IMD3(dBc)	-82.2	-81	-82.5	-76	-84.4	-98.6
LO leakage(dBm)	-38.6	-115.5	-39	-38.6	-	-
2LO -RF leakage(dBm)	-	-56	-	-	-	-75
4LO -RF leakage(dBm)	-	-	-	-	-	-
S11(dB)	-13.1	-12.3	-11.6	-18.6	-15	-29
S21(dB)	-5.9	-6.8	-6.1	-11.5	-13.4	-7
S22(dB)	-14.1	-12.5	-15.4	-12.1	-19	-

Chapter 6

System Simulations

The final simulations are taken with a single channel mixer in voltage mode since it gives very good results for linearity , enable for a power efficient TOR and robust to mismatches. The final circuit is shown in figure 6.1. The source and load resistors were 100Ω differentially.
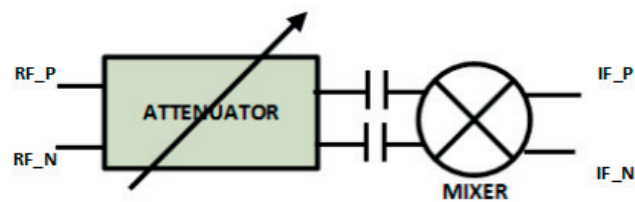
Figure 6.1: Final circuit(attenuator and mixer)

The system accepts input frequencies from 2GHz to 7GHz. Some results were captured at three different frequency check points of 2GHz, 4.5GHz and 7GHz, others were checked for only 7GHz and 2GHz. CP1dB was only checked at 7GHz.

6.1 Linearity

6.1.1 IIP3

IIP3 was measured using a two tones, with 10MHz offset. It was recorded for 7GHz and 2GHz input frequencies.
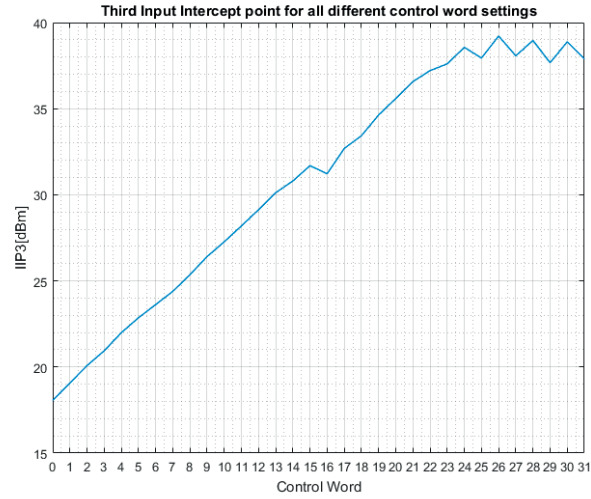
Figure 6.2: IIP3 versus attenuation/RF=7GHz
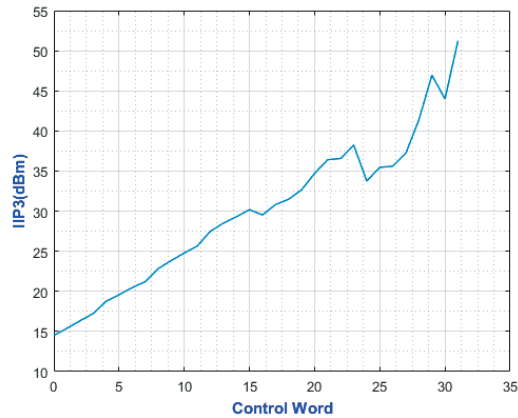
Figure 6.3: IIP3 versus attenuation/RF=2GHz

The fluctuation in the curves is due to the switching between different attenuator stages. The simulated IMD3 with harmonic balance tool is given in the following table.

Table 6.1: IMD3 in terms of dBc for selective practical conditions/RF=7GHz

Input power(dBm)	Attenuation	IMD3(dBc)
-30	0	-94.2
-25	5	-94.2
-20	10	-87.5
-15	15	-90
-10	21	-88.8
-5	25	-86.6
0	31	-87.5

6.1.2   IIP2

IIP2 was measured for 2GHz and 7GHz input frequencies. A blocker was applied so that the resulting $|f_{blocker} - f_{fund}|$ will be in-band. Since IIP2 in differential circuits is proportional to the mismatch, a Monte-carlo simulation was done to evaluate the IIP2 value. The mismatch results will be given in Appendix A.
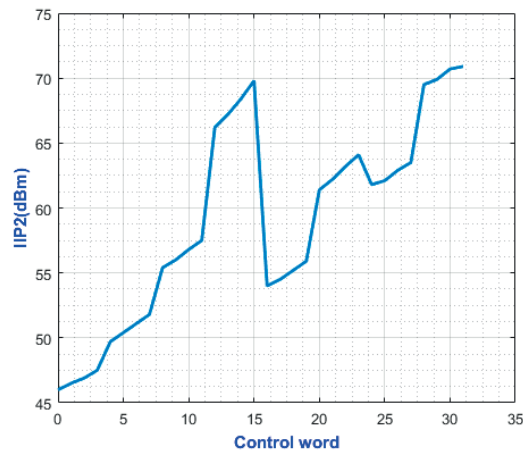
Figure 6.4: IIP2 versus attenuation/RF=2GHz
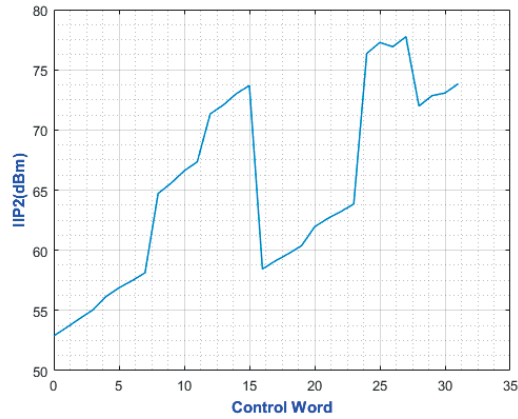
Figure 6.5: IIP2 versus attenuation/RF=7GHz

6.1.3   CP1dB

The in-band signal compression due to the presence of a blocker was checked at an input frequency of 7GHz, when the attenuation is set to 0.
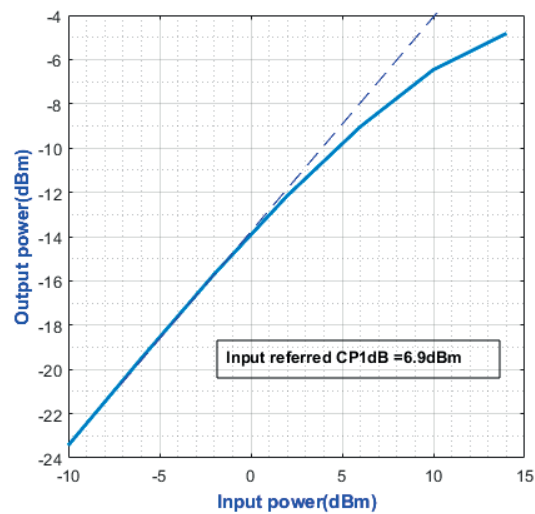
Figure 6.6: 1dB compression point/RF=7GHz

It is exactly 10dB lower than the corresponding IIP3 which is around +17dBm.

6.2   Amplitude precision

The results show that the higher the input frequency, the worse the amplitude error, because of the parasitics in the circuit. The error is measured as S21 variation over the whole IF band. The worst reported error is 0.5dB when the input frequency is 7GHz.

(a) Amplitude error @ RF= 7GHz

(b) S21 versus frequency @ RF= 7GHz

(c) Amplitude error @ RF= 4.5GHz

(d) S21 versus frequency @ RF= 4.5GHz

(e) Amplitude error @ RF= 2GHz

(f) S21 versus frequency @ RF= 2GHz
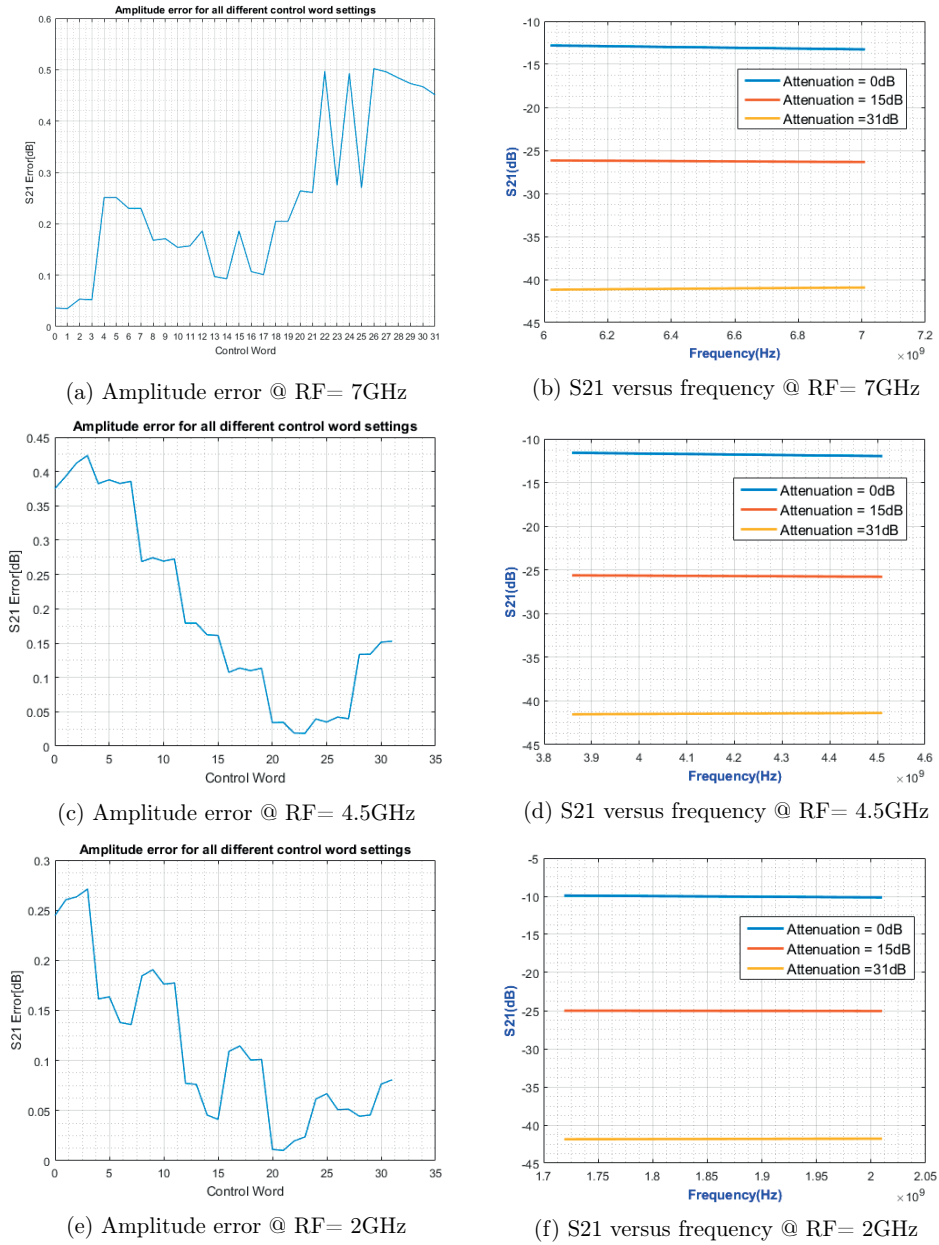
Figure 6.8: S21 simulations

6.3 Phase precision

The final phase error shows results that are much better than the phase error exhibited by the attenuator alone. and that is due to the phase cancellation caused by integration. Generally, the phase error is much better than what is stated in the system specifications for all the input frequencies as the figures emphasize.
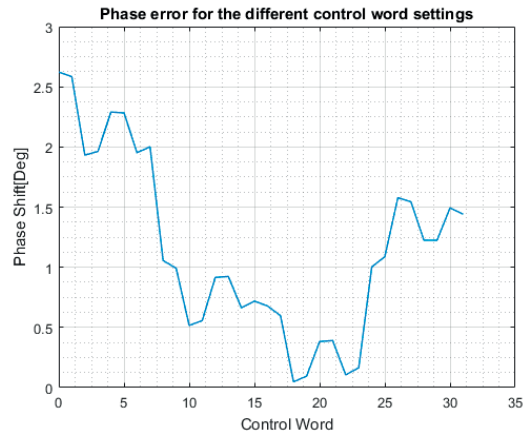
(a) Phase error @ RF= 7GHz
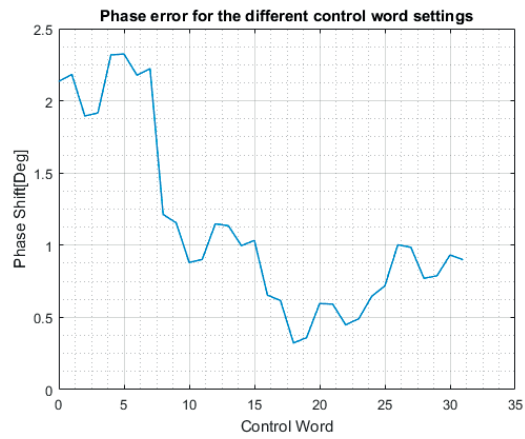
(b) Phase error @ RF= 4.5GHz
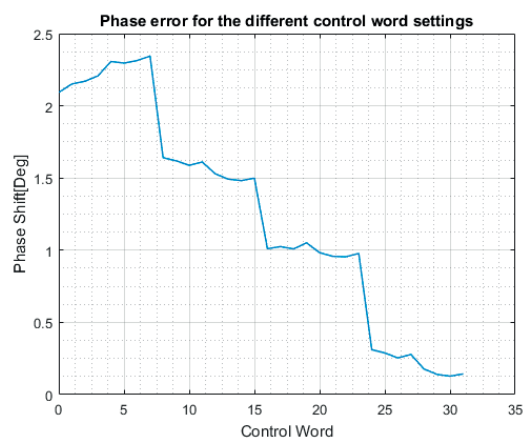
(c) Phase error @ RF= 2GHz
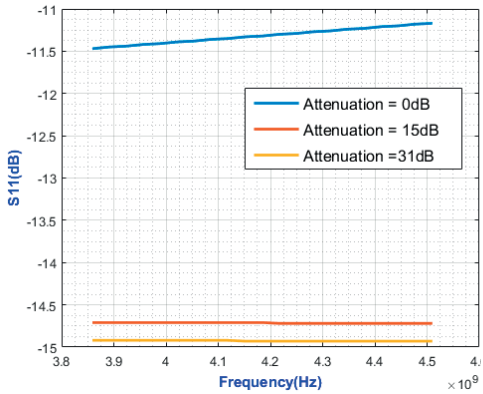
Figure 6.10: Phase Simulations

6.4 Input and output Impedance matching

The typical and extreme values of the input and output return losses are displayed in the figures in this section. The detailed graphs will be attached in appendix A. The worst case S11 is less than -10dB.
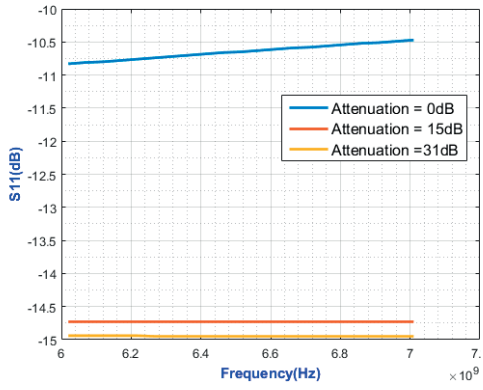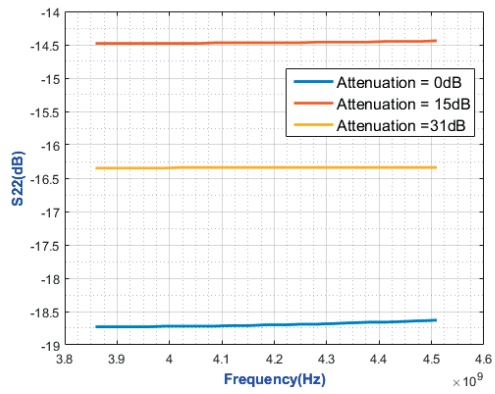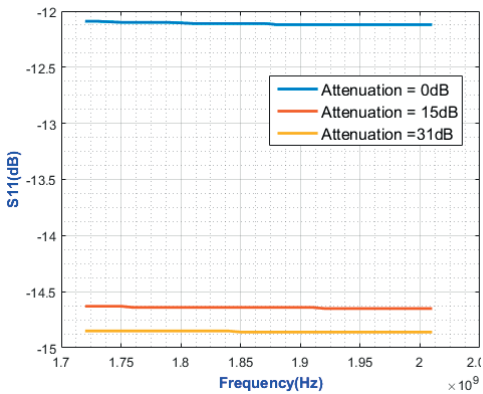
(a) Input return loss @ RF= 7GHz
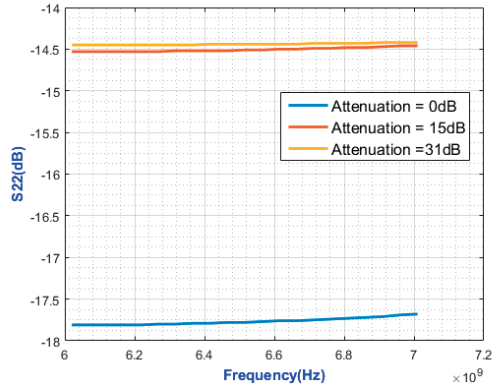
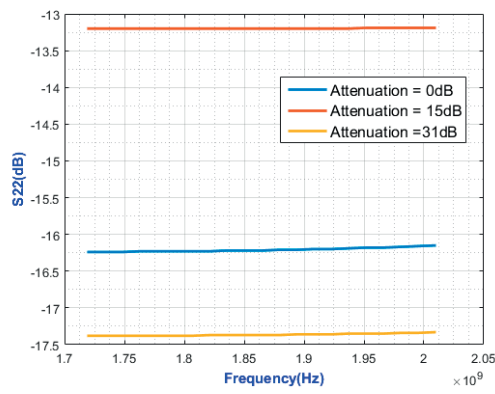(b) Output return loss @ RF= 7GHz

(c) Input return loss @ RF= 4.5GHz

(d) Output return loss @ RF= 4.5GHz

(e) Input return loss @ RF= 2GHz

(f) Output return loss @ RF= 2GHz

Figure 6.12: Return losses simulations

6.5 Current consumption

The circuit designed is all passive, the voltage supply was 1.2V. Since the mixer was derived with an ideal signals. The current was measured by averaging half of the absolute transient current at the mixer gates. The current consumption is reported along with the temperature variation.
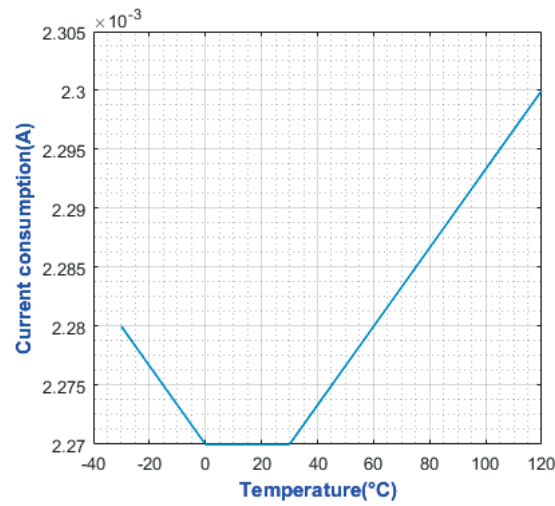

Figure 6.13: Current consumption versus temperature

6.6 Noise figure

Noise figure is a measure of how much the signal to noise ratio (SNR) is deteriorated. This is called the noise factor (F) or noise figure (NF), where the noise figure is the noise factor expressed in dB. The noise factor of a circuit is the ratio between the SNR_{out} and SNR_{in}. Noise figure was so relaxed parameter in this work, since the TOR has relatively strong input power levels. It would have been critical if the receiver is used as a generic reference receiver for another receivers where the expected signals are weak. The noise figure is recorded at an input frequency of 2GHz and 7GHz for all the different attenuation settings. The results were exactly as expected; the noise figure is almost equal to the total attenuation .
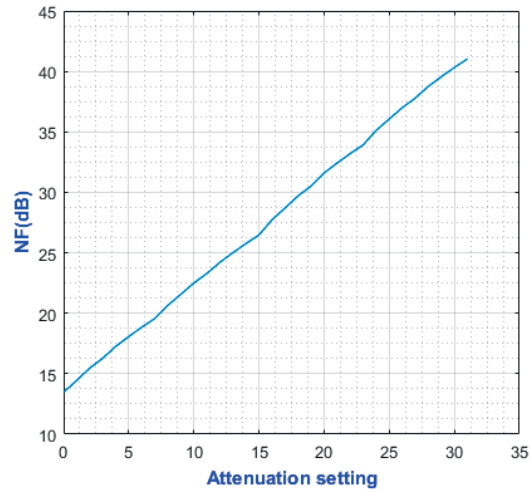
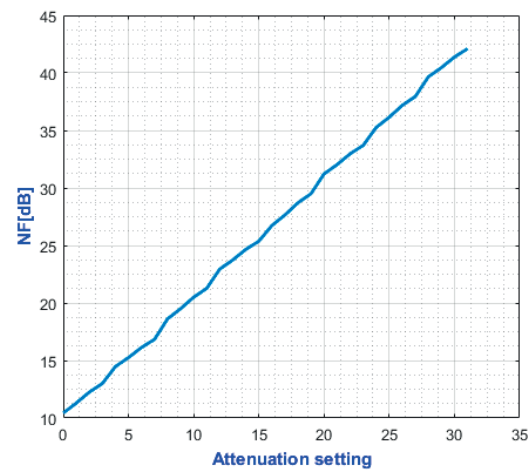Figure 6.14: Noise figure versus attenuation/RF=7GHz

Figure 6.15: Noise figure versus attenuation/RF=2GHz

6.7 Temperature variation

The worst results conditions for S parameters and phase shift were selected and checked versus temperature variation from -30°C to 120°C.

Table 6.2: Some results with temperature variation/RF=7GHz

Temperature(°C)	Worst S11(dB)	Worst S22(dB)	S21 error(dB)	Insertion loss(dB)	phase error(Deg)
-30	-9.777	-13.3	0.431	-12.22	2.535
0	-10.08	-12.71	0.44	-12.6	2.576
30	-10.37	-12.18	0.448	-12.99	2.627
60	-10.64	-11.69	0.456	-13.38	2.676
90	-10.9	-11.26	0.462	-13.78	2.721
120	-11.14	-10.87	4.67	-14.19	2.761

Table 6.3: Some results with temperature variation/RF=2GHz

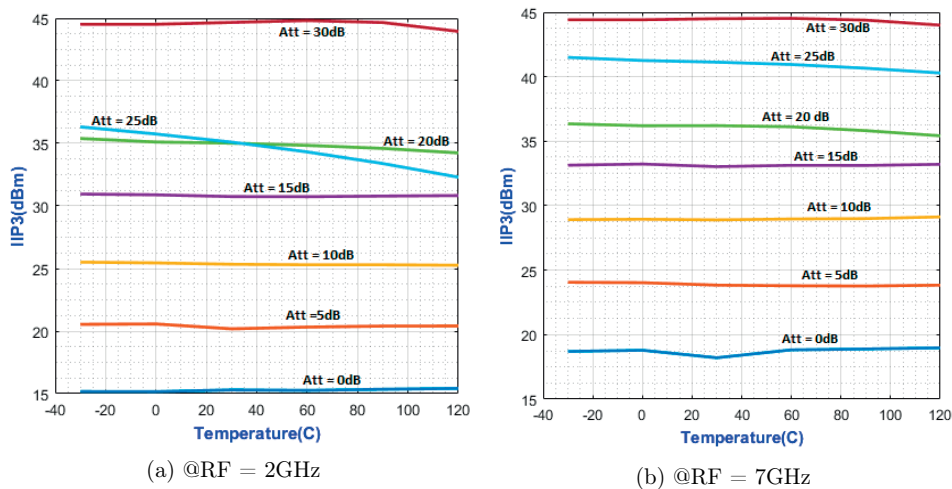| Temperature(°C)	Worst S11(dB)	Worst S22(dB)	S21 error(dB)	Insertion loss(dB)	phase error(Deg)
-30	-11.83	-13.3	0.234	-9.453	2.535
0	-11.99	-12.71	0.241	-9.691	2.576
30	-12.1	-12.18	0.247	-9.932	2.627
60	-12.18	-11.69	0.253	-10.17	2.676
90	-12.24	-11.26	0.259	-10.41	2.721
120	-12.29	-10.87	0.265	-10.65	2.761

(a) @RF = 2GHz

(b) @RF = 7GHz

Figure 6.16: IIP3 versus temperature

Chapter 7

Conclusion and Future Work

7.1 Conclusion

Passive programmable digital step attenuator was successfully implemented and integrated with a double balanced passive mixer in voltage mode, aiming for a linear wide band TOR, and the results show that the final circuit exhibits IIP3 of 15 and 18dBm in bypass state for 2GHz and 7GHz input frequencies respectively. The IIP3 increases as the attenuation is increased resulting in an SFDR of higher than 85dBm for all the different input powers from -30dBm to +1dBm. The limitation of this work was to achieve high amplitude precision over the bandwidth, since the bandwidth is relatively high. Some ideas to overcome this problem will be suggested in the next section. The phase shift was much better than what specified for the circuit.

Also, in this thesis work, different mixer topologies were compared, and the results confirmed that the current mode mixer is the most linear topology. Using dummy switches for voltage mode mixers proved to be excellent for improving the LO to RF isolation. The quadrature mixer can further improve the isolation, but may be subject to mismatches if the circuit is implemented with a real VCO circuitry.

Table7.1 summarized the final achieved results versus the required specifications. It also gives the minimum and maximum expected values after manufacturing, by taking the process corners and mismatches into account. All the results in the table were measured at 7GHz, when the attenuation is set to 0dB, since most of the parameters have their worst values with this setup, except IIP3 and IIP2, they have their worst values at 2GHz, which are 15dBm and 46dBm respectively. The noise figure is worst at 2GHz when the attenuation is set to the highest value. It is 42dB which is still much better than what is specified for this worst condition. The noise figure specifications are different for different input power levels and hence attenuation settings.

Table 7.1: Comparison between the required and achieved results/RF=7GHz

Parameter	Achieved			Target	Unit	Evaluation
	Min[1]	Typical	Max[2]			
S21 error	0.376	0.5	0.56	$\leqslant 0.2$	dB	0.3dB off the specification
S11	-12	-10.34	-9.2	$\leqslant -10$	dB	passed for typical conditions only
S22	-27.1	-17	-8.3	$\leqslant -10$	dB	passed for typical conditions only
Phase shift	1.97	2.65	3.28	$\leqslant 6$	degrees	passed
Insertion loss	-16.7	-12.5	-11.7	-	dB	-
IIP3	16.47	18.2	18.75	$\geqslant 14$	dBm	passed
IIP2	42.6	52.8	53.9	$\geqslant 30$	dBm	passed
LO emission	-70.4	-69.96	-69.6	$\leqslant -50$	dBm	passed
Current consumption	2.18	2.23	2.29	-	mA	-
Noise figure	11.98	13.47	16.14	<19	dB	Passed

1$\equiv \min(6\sigma$ minimum value, minimum process corner value)
2$\equiv \max(6\sigma$ maximum value, maximum process corner value)
Passed for typical conditions indicates that it is not passed for the extreme process corners variation.

7.2 Future work

Some recommendations for future work are suggested in this section.

7.2.1 Integration with filter and Layout

The circuit is yet to be integrated with a passive filter to make an overall passive TOR and layout should be done using RF layout techniques so as the TOR be ready for manufacturing in silicon.

7.2.2 Amplitude precision improvement

In order to tackle the amplitude variation over the frequency, the suggestion is to use low attenuation stage in the attenuator such as 1dB or 2dB stage and duplicate it to achieve higher attenuation. That way we can get rid of high attenuation stages like 8dB and 16dB, since it is clear from the individual stages results of the attenuator that the variation is coming mostly from the high attenuation stages.

7.2.3 T - Digital step attenuator

Bridged T attenuators can be implemented to achieve better impedance matching, since the number of switches in T attenuators is less compared to PI attenuators.

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Appendix A

Monte-Carlo and process corners simulations

The results of mismatches and process corners variation are given here for the condition of 0 dB attenuation with 7GHz input frequency.

A.1 Monte-carlo Simulations

Table A.1: Mismatch simulations results/RF=7GHz

Parameter	Min[1]	Mean	Max[2]
S21 error(dB)	0.446	0.448	0.449
S11(dB)	-10.4	-10.34	-10.3
S22(dB)	-17.9	-17.5	-17.2
Phase shift(Deg)	1.97	2.62	3.28
Insertion loss(dB)	-13.4	-13.4	-13.4
IIP3(dBm)	17.4	17.47	17.5
IIP2(dBm)	42.6	51.12	53.9
LO Emission(dBm)	-70.4	-69.96	-69.6

1≡ 6σ minimum value   2≡ 6σ maximum value

A.2 Process Corners Simulations

Table A.2: Circuit results with Process corners variation/RF=7GHz

Parameter	Min	Max
S21 error(dB)	0.38	0.56
S11(dB)	-12.01	-9.194
S22(dB)	-27.14	-8.322
Phase shift(Deg)	2.233	3.165
Insertion loss (dB)	-16.73	-11.73
IIP3 (dBm)	16.47	18.75
IIP2 (dBm)	50.47	51.13
Current consumption(mA)	2.18	2.29
Noise figure(dB)	11.98	16.14

Appendix B

Some detailed Simulation Graphs

B.1 Attenuator Results
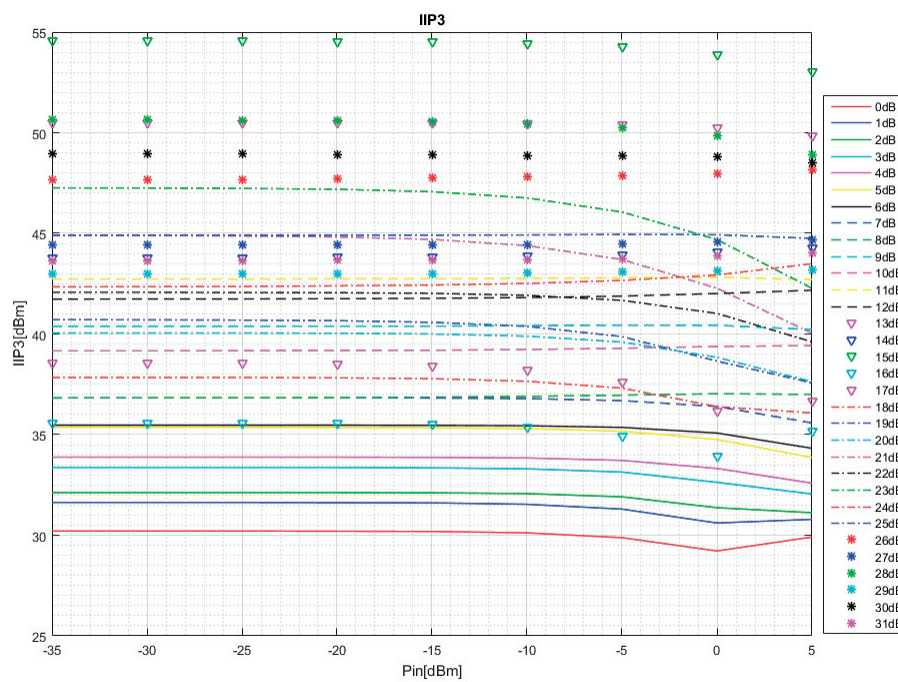
Figure B.1: Input referred intercept point with different attenuation settings and input power levels
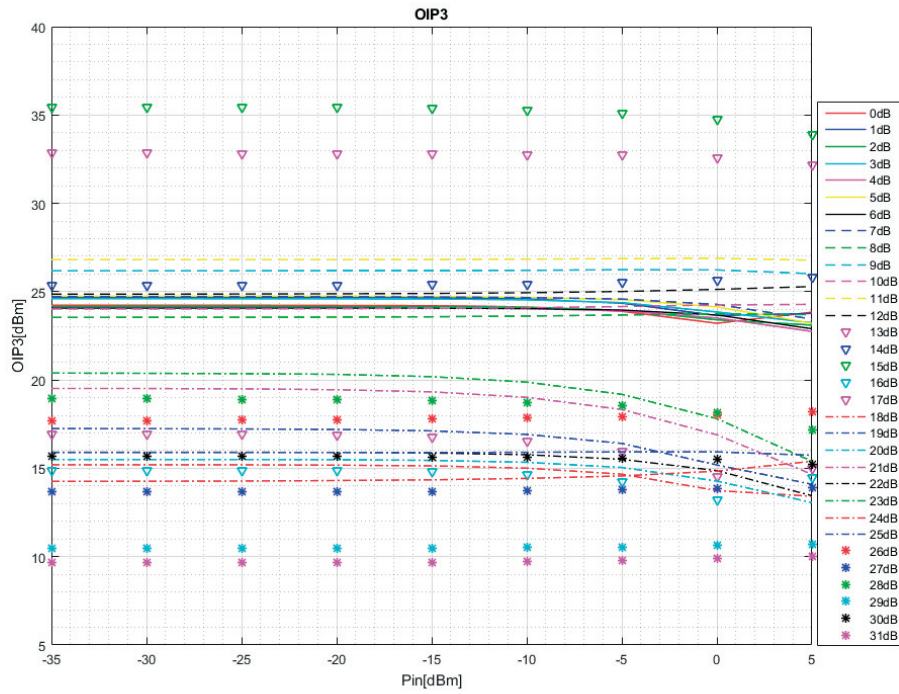
Figure B.2: Output referred intercept point with different input powers and attenuation settings
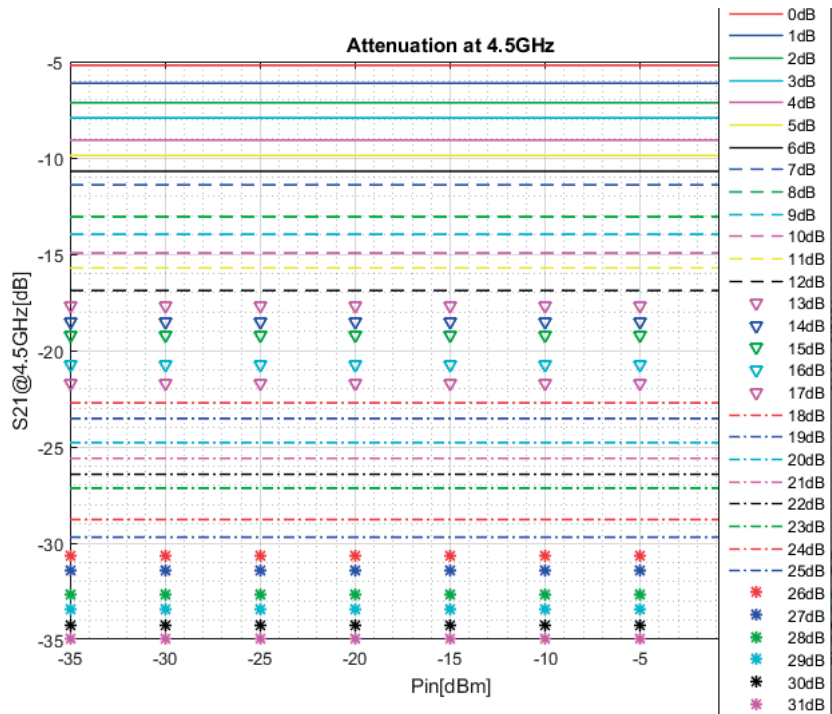
Figure B.3: The attenuation at 4.5GHz with all control words combinations
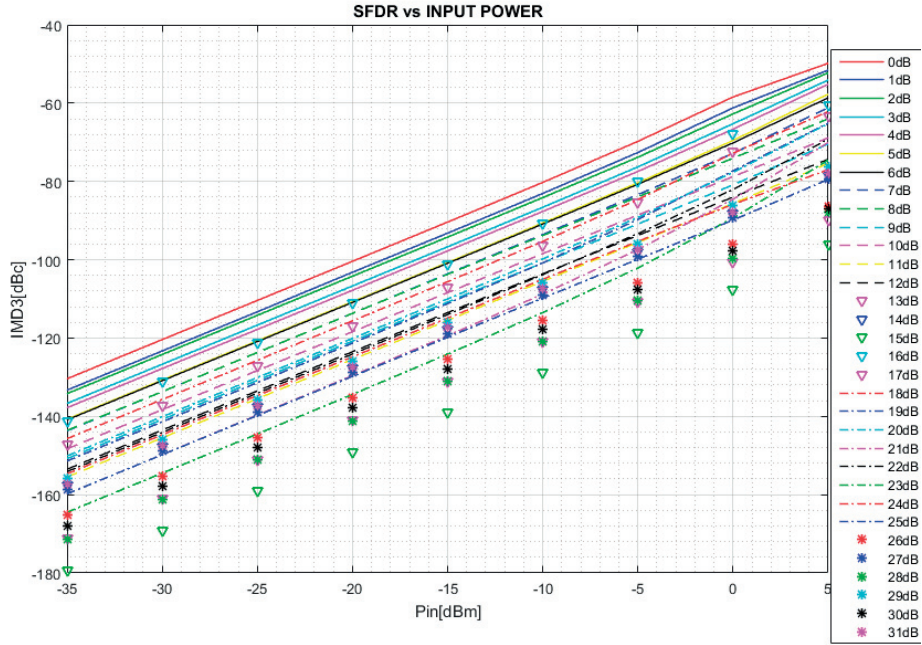
Figure B.4: IMD3 at 7GHz for different input powers and attenuation settings

B.2 Final circuit Results
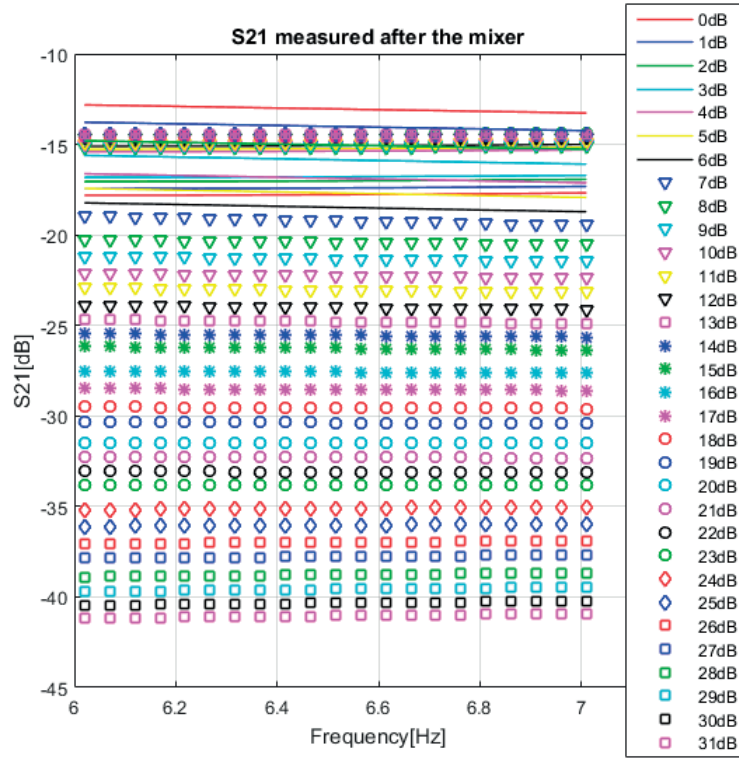
Figure B.5: S21 versus Frequency @ RF= 7GHz
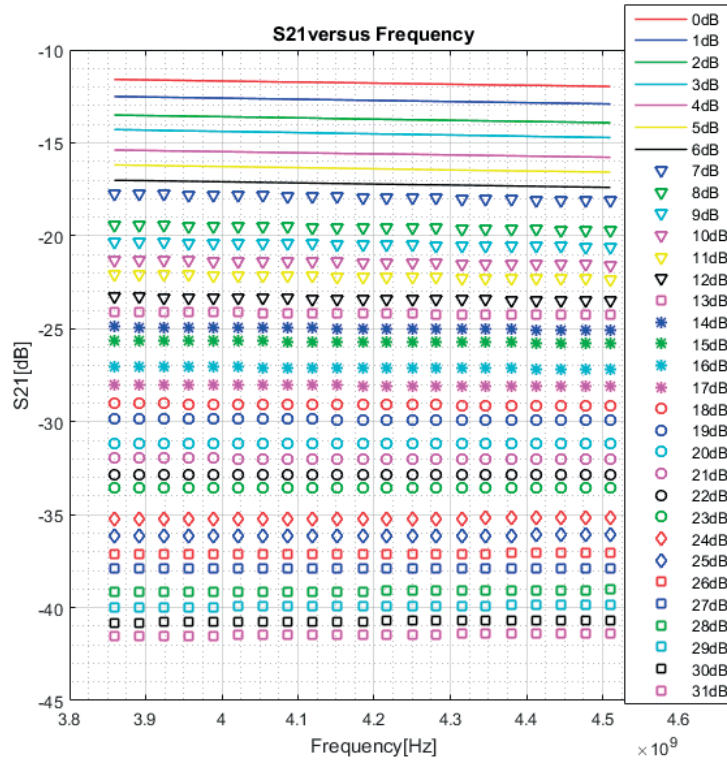
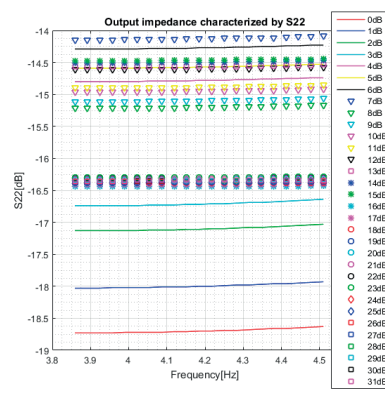Figure B.6: S21 versus Frequency @ RF= 4.5GHz
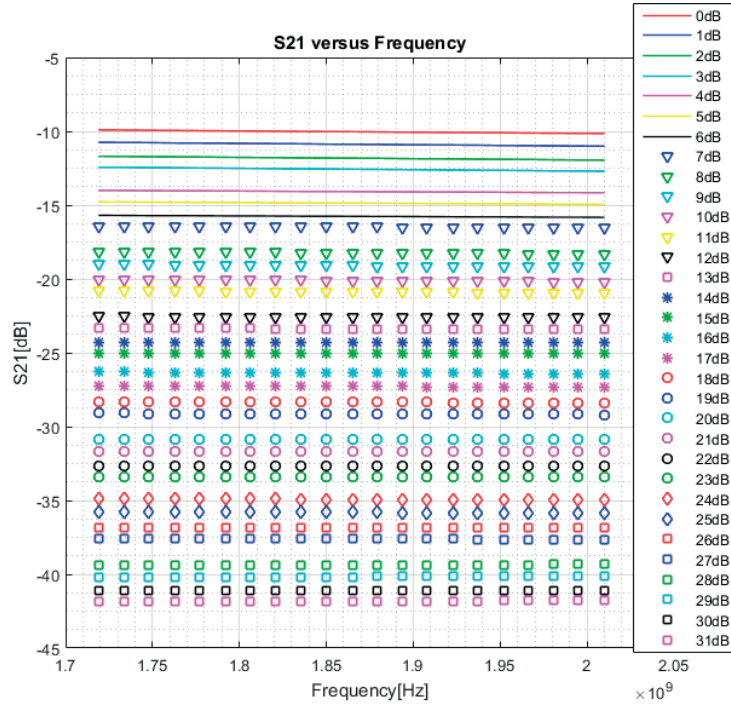
Figure B.7: S21 versus Frequency @ RF= 2GHz
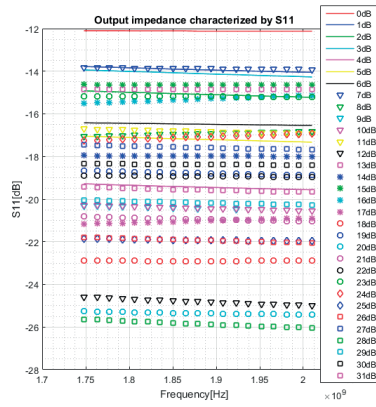
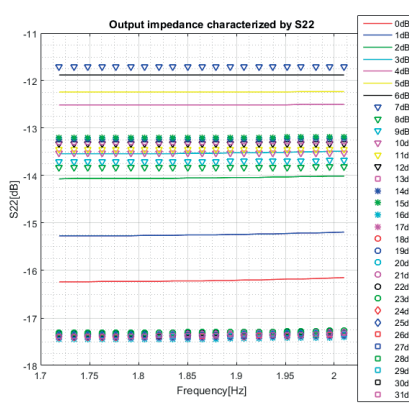(a) Input return loss @ RF= 7GHz

(b) Output return loss @ RF= 7GHz

(c) Input return loss @ RF= 4.5GHz

(d) Output return loss @ RF= 4.5GHz

(e) Input return loss @ RF= 2GHz

(f) Output return loss @ RF= 2GHz

Figure B.9: Return losses Simulations