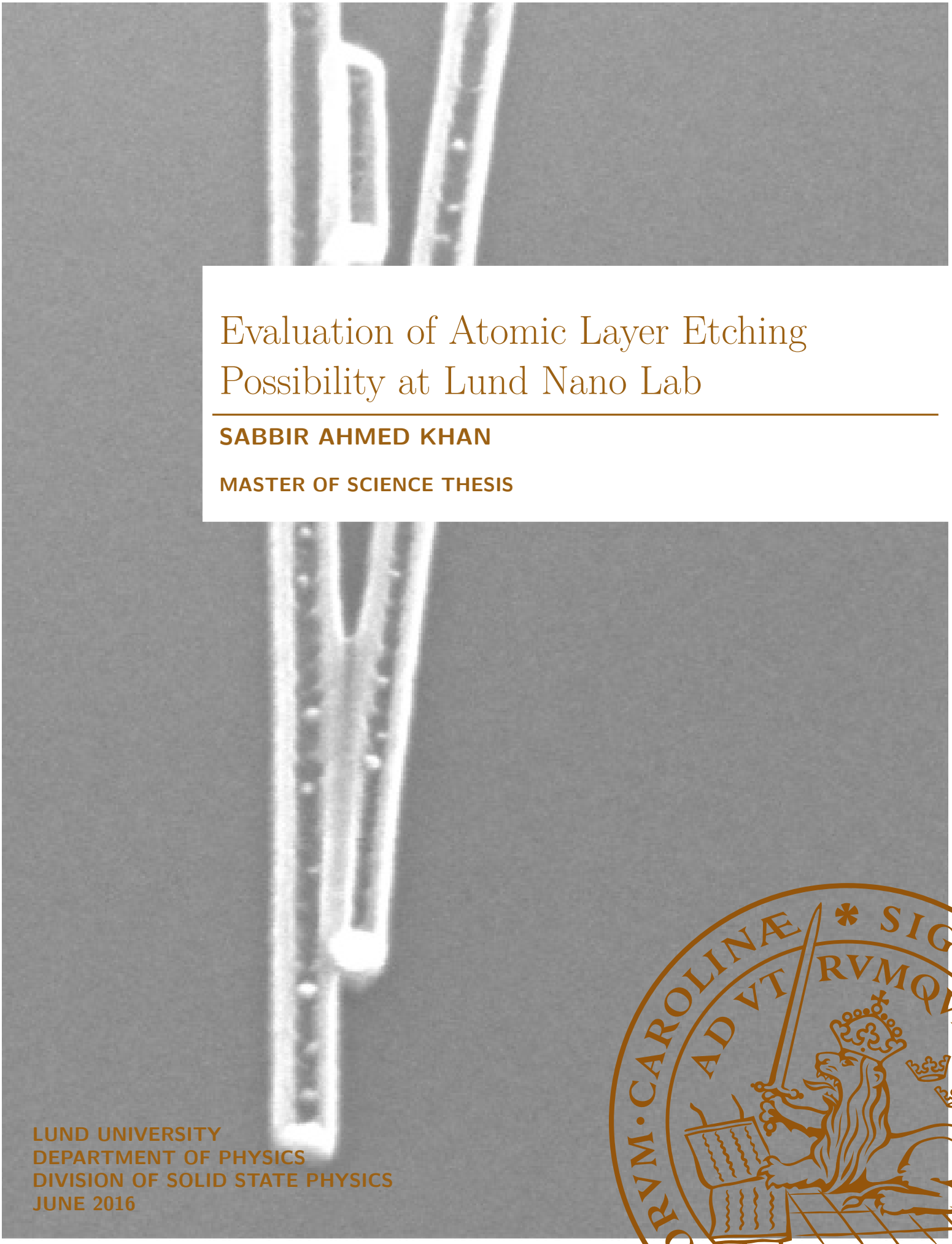

Evaluation of Atomic Layer Etching Possibility at Lund Nano Lab

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MASTER OF SCIENCE THESIS

LUND UNIVERSITY
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JUNE 2016

LUND UNIVERSITY
Faculty of Science

Evaluation of Atomic Layer Etching Possibility at Lund Nano Lab

Master's Thesis, 60 Credits
Presented by
Sabbir Ahmed Khan
to
The Department of Physics

in partial fulfillment of the requirements
for the degree of
Master of Science
in the subject of
Physics, Nanoscience

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Lund University
Lund, Sweden
June 2016

Abstract

In modern electronics, device downscaling demands atomic precision control and Atomic Layer Etching (ALE) can provide this prime capability with minute device damage. ALE, also known as layer-by-layer etching, is a technique of removing atomically thin layers from the surface of materials in a controlled way. This technique is now very crucial for nanofabrication and semiconductor industry in order to achieve atomic scale resolution. This is why the overall goal of this diploma project was to investigate the possibility for ALE at Lund Nano Lab and to reveal different limitations with our current equipment. In order to achieve this goal we have done experiments with conventional system used for reactive ion etching. In addition, the ALE has been done on GaP nanowires and on Si surface patterned with high-resolution Electron Beam Lithography (EBL). The results of these experiments indicate that the process can be used to make stamps for nanoimprint lithography in a highly controlled way and that the low ion energy etching process can be used for direct nanowire splitting. We show different limitations for ALE with our current equipment and provide recommendations for new equipment dedicated for this process. In this way, the work presented here opens up the possibility for further studies of ALE with conventional equipment, shows some aspects of it's importance for nanofabrication and suggests new applications for the ALE processes.

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To my mother and my wife....

Acknowledgments

This research project has been performed in my scholarship period at Lund University. Hence, I want to thank Swedish Institute (SI.) scholarship for providing me opportunity to be a part of this prestigious university. I want to thank the department of Physics for constructing such a research-oriented environment. I also want to thank the people working hard to maintain Lund Nano Lab facilities.

I want to convey my gratitude to both of my supervisors, Dr. Dmitry Suyatin and Dr. Jonas Sundqvist for their continuous support and motivation. They are not only my supervisors but also my guardians and friends here in Sweden. I should also mention Associate Prof. Dan Hessman, my co-advisor and program coordinator, who supported me in my whole study period and guided me to find a perfect research project that met with my credentials.

My thank goes to Associate Prof. Ivan Maximov, our team leader, for the discussions and suggestions to our research project. Dr. Maria Huffman provided all the lab supports in our experiments. I want to thank Nicklas Nilsson for helping me mastering ellipsometry measurements. I also want to thank Dr. Peter Blomqvist for training me with Atomic Force Microscopy (AFM). Anders Kvennefors suggested and helped us to select silicon on insulator samples for this project and provided a valuable input in our regular discussions. Mariusz Graczyk performed nanoimprint lithography with the stamp processed by ALE and also provided important input to the project in our discussions.

Andy Goodyear, Ralf Olemann, Colin Welch and Mike Cooke from Oxford instruments supported us with hardware and provided recommendations on process details. I want to acknowledge Prof. Walter Weber from Namlab (Nanoelectronic Materials Laboratory) for providing us Si nanowires. Marcel Junige from Technical University of Dresden (TUD) helped us with X-ray Photoelectron Spectroscopy (XPS) measurement. Etch experts from the Microelectronics division of Skobeltsyn Institute of Nuclear Physics of Moscow State University helped us with their opinion on our process. Finally, NanoLund supported us by providing grant for conferences, workshops and through the lab support.

Dr. Maryam Olsson and Göran Asketorp from LU Innovation System provided help with our patent application and commercialization of our research results.

My friends in Lund supported and inspired me all the way in my regular life. My colleagues from the

Solid State Physics division were very helpful and charming. In my work break, I really enjoyed traditional Swedish 'Fika' with colleagues from the lab. Last but not the least, I want to thank my mother and my lovely wife, for their encouragement in my hard times.

List of abbreviations

ALE	Atomic Layer Etching
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
EPC	Etch Per Cycle
EBL	Electron Beam Lithography
GaP	Gallium Phosphide
GaAs	Gallium Arsenide
HSQ	Hydrogen Silsesquioxane
ICP	Inductively Coupled Plasma
InP	Indium Phosphide
LNL	Lund Nano Lab
MOVPE	Metal Organic Vapor Phase Epitaxy
NW	Nanowire
nm	Nanometer
NIL	Nanoimprint Lithography
PALE	Plasma Atomic Layer Etching
RIE	Reactive Ion Etching
Si	Silicon
SOI	Silicon on Insulator
SEM	Scanning Electron Microscope
XPS	X-ray Photoelectron Spectroscopy

There's Plenty of Room at the Bottom.

Richard Feynman

1 Introduction

Nowadays technology in many respects decides our way of life. More precisely, we are surrounded by technical equipment. Hence, evaluations of smart technologies are very important. Around the middle of the last century, when scientists made a revolution on computing systems, we entered into a new era: 'The era of computers'. From advanced robotics system to smart phones, all the devices we are using now are evolved from that first monster computer developed by some brilliant minds. The first desktop computer came to my family when I was five or six years old. I still remember that, we needed to empty some space to setup that big computer! Few years later, when I bought a new one that was almost one-third in size of the previous one, but double in speed and performance! Beginning of my bachelor study, I found the faster version of computer in my lap and almost no space was required to set it up. Finally, a smartphone in my grip, much more efficient than everything I used before. Isn't it really surprising, how we are having thousand times faster devices in our hand compared to one big room size computer in 1950's? Or, aren't we get puzzled to know that the smart watch in our hand contains thousand times more components than a big truck or train? Moreover, scientists have not stopped yet; they are going towards smaller and more compact devices. Here I get my inspiration to do research with such technique that can accelerate the motion of going towards smallest.

There's plenty of room at the Bottom (Richard P. Feynman, APS Meeting, Caltech, 1959). With this motivation, the scientist community is still digging deep to find the space to fill. However, it has never

Figure 1.0.1: Lund Nano Lab (LNL): the most modern cleanroom facility in Sweden. LNL consists of two main parts: Nano-process lab and Nano-epitaxy lab.

been an easy job to shape structures at such small dimensions. One of the vital challenges is to cut the materials into precise structures that a scientist needs. Suppose a carpenter needs to build a statue with wood. His first job will be cutting the wood pieces into perfect sizes to fit nicely in the base structure of the statue. Fabricating materials and devices works in the same way. A processing scientist needs to cut the material in such a way that it can fit the structure properly. In material fabrication, this cutting is popularly known as 'Etching Technology'. For modern compact devices, materials need to be etched at the nanometer (nm) scale, since a single chip contains billions of transistors. Now the question is how small is this nanometer scale? A human hair is approximately 100,000 nanometer wide! So, it is now understandable how challenging it is to control etching in that small structure. However, scientists made it possible through wet and dry etching techniques. In fact, this is just the beginning of the story. As I said, scientists haven't stopped yet, they need to explore deep in down. For more efficient electrical and optical properties and also for further device shrinking, sub 10 nm devices are in demand. But to make it possible atomic precision etching is needed. Here it comes Atomic Layer Etching or simply ALE, which is a self limiting layer by layer etching technique containing steps like- surface modification of the material, purging and removal of modified layer [1]. The details of ALE are discussed in chapter 3.

For the last 25 years, scientists have been exploring new materials to replace Si and adhere to Moore's

law [2]. In fact, different materials such as compound semiconductors, nanotubes, nanowires, graphene are very promising for semiconductor industry. However, one of the main limitations is the etching process. After the invention of ALE technique by Yoder in 1988 [3], several researchers have performed different experiments with different materials to explore ALE. Few different materials such as Si, GaAs, InP and InAlAs have already been explored with ALE [4–7]. However, plenty of materials are yet to be investigated. Recently, researchers have started studying 2D materials such as graphene, MoS_2 with ALE [8–14]. Now, structures like nanowires (NWs) or nanotubes can be potential candidate to investigate with ALE. In spite of having impressive prospects, this etching technique has several challenges. One of the main challenges is long process duration. In fact, this is a big limitation for industrial applications. In addition, no dedicated tools have yet been developed for ALE. Considering all this, a wide range of studies can be conducted with this technique and the development of this process may enable future devices with atomic level control. Atomic Layer Deposition, counterpart of ALE, became popular in an industrial context almost twenty-five years after it's birth and now it is almost the same time after the first ALE patent. For these reasons, our research team believes that, it is the right time to develop the ALE technique in our lab. Hence, an ALE possibility of Si has been evaluated in Lund Nano Lab (Fig. 1.0.1), using a conventional plasma etching tool. The etching results have been investigated with Atomic Force Microscopy (AFM), Scanning Electron Microscopy (SEM), Ellipsometry and X-ray Photoelectron Spectroscopy (XPS). ALE has also been performed on GaP NWs. Controllable etching of NWs is very important for Lund Nano Lab, since the core research is done on nanowires and nanowire based devices. Moreover, high-resolution pattern transfer with ALE was successfully performed for nanoimprint lithography stamp fabrication.

In this report, Chapter 2 describes the history and development of ALE till now. This chapter will also cover the materials that have been investigated with ALE so far. Chapter 3 deals with the theory and basic physics behind the ALE. The experimental details and measurement procedure have been also discussed in Chapter 4. Results and their analysis are delivered in Chapter 5. Finally, Chapter 6 summarizes the whole work and provides suggestions for further work.

If I have a thousand ideas and only one turns out to be good, I am satisfied.

Alfred Nobel

2

History And Development of ALE

ALE technology has been studied for almost 30 years. The first patent was filed by Yoder in 1988 [3], where he revealed the technique of doing ALE with crystalline diamond. Another early contribution was done by Maki and Ehrlich in 1989 [15], reporting GaAs 'bilayer etching', possibly the first atomic precision etching for III-V semiconductor materials. In early 90's publications, ALE technique was referred by different names such as Plasma Atomic Layer Etching (PALE), Layer-by-Layer Etching, Digital Etching, Single Layer Etching, Atomic Layer Removal, Molecular Bilayer Etching and Thin Layer Etching. Different ALE names and corresponding references were listed by Kanarik et al. (2015) [16]. Till now more than 20 materials have been inspected using ALE including silicon, III-V semiconductor materials, different oxides, 2D materials and some polymers; a list of different materials can be found in Oehrlein et al. (2015), page: 5045 [1]. In the early period, silicon and GaAs were the most studied materials for the ALE technique [16] since both needed Cl_2 based chemistry for etching. However, for the last 15 years, other III-V semiconductor materials have been also investigated extensively. In addition to the experimental works, some computational modeling was also performed in the late 90's [16].

Basically, ALE contains two major phases: modification of surface and removal of modified surface layers. Researchers used few different approaches for both steps. For surface modifications chemisorption, deposition and conversion have been used [16]. On the other hand, for removal, ion bombardment, chemical reaction and thermal desorption has been used [16]. Details of these approaches and the motivations

behind the preferred one for this research is discussed in Chapter 3. A brief history of ALE experiments with different materials is reviewed bellow:

Silicon: Since the invention of ALE, Si is the most investigated material, due to its industrial value. In this study, we also used Si samples for exploring ALE possibility in LNL. First Si ALE was reported by Horiike et al. in 1990 using fluorine based chemistry to modify a sample surface [17]. However, nowadays Cl_2 is most common to modify a sample surface through chemisorption. The first Cl_2 based ALE with silicon was reported by Matsuura et al. in 1993 [18]. In that report, energetic ion Ar^+ was used in the removal step. In 1995, Imai et al. used heating (thermal desorption) instead of ion bombardment in the removal step for Si ALE [19]. Because of Ar^+ bombardment damage on the surface, in 2005 Part et al. suggested neutral beams for removal of the modified layer [20]. In addition to fluorine and chlorine based surface modification, other halogens such as bromine were also studied by Aldao and Weaver [21][16].

III-V Semiconductor: III-V semiconductor materials are the most probable candidates for replacing Si in integral semiconductor circuits due to their high electron mobility. Hence, from the beginning, ALE experiments with III-V compound semiconductor materials were as popular as Si, however the surface properties of these compound materials are more complicated than the surface properties of Si [16]. Different III-V compounds have been investigated till now and a complete list can be found from Oehrlein et al. (2015) page: 5045 [1] and etching chemistry detail from Kanarik et al. (2015) page:11 [16]. It seems that a greater number of III-V compound semiconductors have been explored with anisotropic ALE comprising energetic ion bombardment in the removal step and Cl_2 for surface modification [5–7, 22, 23]. In addition to that, in 1998, Otsuka et al. introduced Tertiarybutylphosphine for surface modification and halogen lamp for modified surface removal [24]. Finally, researchers have also investigated wet chemical ALE for different III-V compound semiconductors where they oxidized the surface in the first phase and then submerged the wafer into a wet acid bath to remove the topmost layer [16, 25, 26].

Oxides: Silicon dioxide (SiO_2), Hafnium oxide (HfO_2), Titanium dioxide (TiO_2), Zirconium dioxide (ZrO_2), Aluminum oxide(Al_2O_3), and Beryllium oxide(BeO) are common oxides for electronic device technology. Hence, the capability of doing ALE with these materials is important. Yeom's research group at Sungkyunkwan University has been playing an important role in investigation of ALE for high K oxides [16, 27–30]. In most cases, chemisorption technique is used to modify the surface and then it is followed by energetic ion bombardment in order to remove the modified layers. Boron trichloride BCl_3 and Cl_2 are the common gases used to modify the surfaces of high dielectric oxides and Ar neutral beam was reported mostly for removal step [27–30]. ALE for SiO_2 was reported by Rauf et al. (2007), Agarwal et al. (2009) and Metzler et al. (2014) [31–33]. For all the cases, a fluorocarbon deposition approach was used to modify the surface and anisotropic Ar ion bombardment to remove the modified layers.

Other Materials: In addition to the above materials, ALE has been investigated with polymers, different metals, nitrides, 2D materials such as Graphene and molybdenum disulfide(MoS_2) [8–14]. Vogli et al. (2013) explored ALE with polystyrene-based polymer where they used O_2 to modify polymer surface

followed by Ar plasma to remove modified layers [8]. Kuo et al. (2000) investigated Cu ALE with Cl_2 and diluted HCl bath [9]. Ge ALE can be done with Cl_2 and Ar ion bombardment, similar to Si [10]. Matsuura et al. first demonstrated Si_3N_4 ALE in 1997; in this case H_2 gas was used to form ammonia (NH_3) gas byproduct and then ion bombardment in the removal step [11]. In 2014, Posseme et al. showed another approach for the removal step for Si_3N_4 ALE where they used wet etching in aqueous HF solution [12]. Finally, Lim et al. showed the application of ALE for graphene and graphene based devices [13]. O_2 plasma and Ar ion bombardment were used for the surface modification removal of single graphene layer per cycle. Most recently, Li et al. demonstrated ALE of (MoS_2) with Cl_2 adsorption and Ar ion bombardment [14].

A summary of the materials investigated with ALE is given in table 2.0.1

Materials Name	Gases , Energy Source	References
Crystalline Diamond	NO_2 , Excited ions	[3]
HfO_2, TiO_2, ZrO_2, Al_2O_3, BeO	BCl_3 and Cl_2 , Ar Neutral	[27–30]
SiO_2	C_4F_8 , Ar^+	[31–33]
Si	Cl_2 , Ar^+ / Ar Neutral	[18, 19]
GaAs, GaInAs, AlInAs, InP	Cl_2 , Ar^+	[5–7, 22, 23]
Cu	Cl_2 , HCl	[9]
Ge	Cl_2 , Ar^+	[10]
Polystyrene Polymer	O_2 , Ar^+	[8]
Graphene	O_2 , Ar^+	[13]
MoS_2	Cl_2 , Ar^+	[14]
Si_3N_4	H_2 , Ar^+ / H^+	[11]

Table 2.0.1: Investigated materials with ALE

In summary, ALE research has been developing steadily in the last few years. However, there is plenty of materials left to be examined with ALE and many more doors are yet to be open. From this review, it is also clear that ALE of NWs, which is our main target, has not been reported yet. The next section will discuss the theory behind ALE and the process which was used in our study.

A theory can be proved by experiment; but no path leads from experiment to the birth of a theory.

Albert Einstein

3 Theoretical Background

ALE is the controlled process of removing a well defined, atomically thick layer at the time. The process is well controlled due to a self-limiting nature of basic steps in the ideal ALE process. As discussed earlier, the ALE process contains two major steps: surface modification and removal of modified layer. Also there are typically two intermediate steps comprising: pumping out the remaining gases after the surface modification and byproducts after selective removal of the modified layer.

Fig. 3.0.1 shows a schematic diagram of the ALE process. As shown in the figure, the sample surface needs to be modified uniformly with either neutrals, radicals or molecules [34]. There are four different ways to activate the surface: chemisorption, deposition, conversion, extraction [16]. A well-defined thin layer forms on the surface after it's modification and this layer is easier to etch than unmodified material, which leads to the selective material removal. Usually, chemisorption and deposition processes are used to activate the surface. However, for few materials, like- for Si_3N_4, a conversion method (such as oxidation) was demonstrated, see e.g. Posseme et al. [12]. Stickney et al. [35] used the extraction method for the compound semiconductor, cadmium telluride (CdTe).

The idea of the extraction is somewhat different from other three approaches. The Extraction method can only be used for compound materials. In other processes, no etching happens in the surface activation step. However, in extraction, one of the materials from the topmost surface is removed while the surface

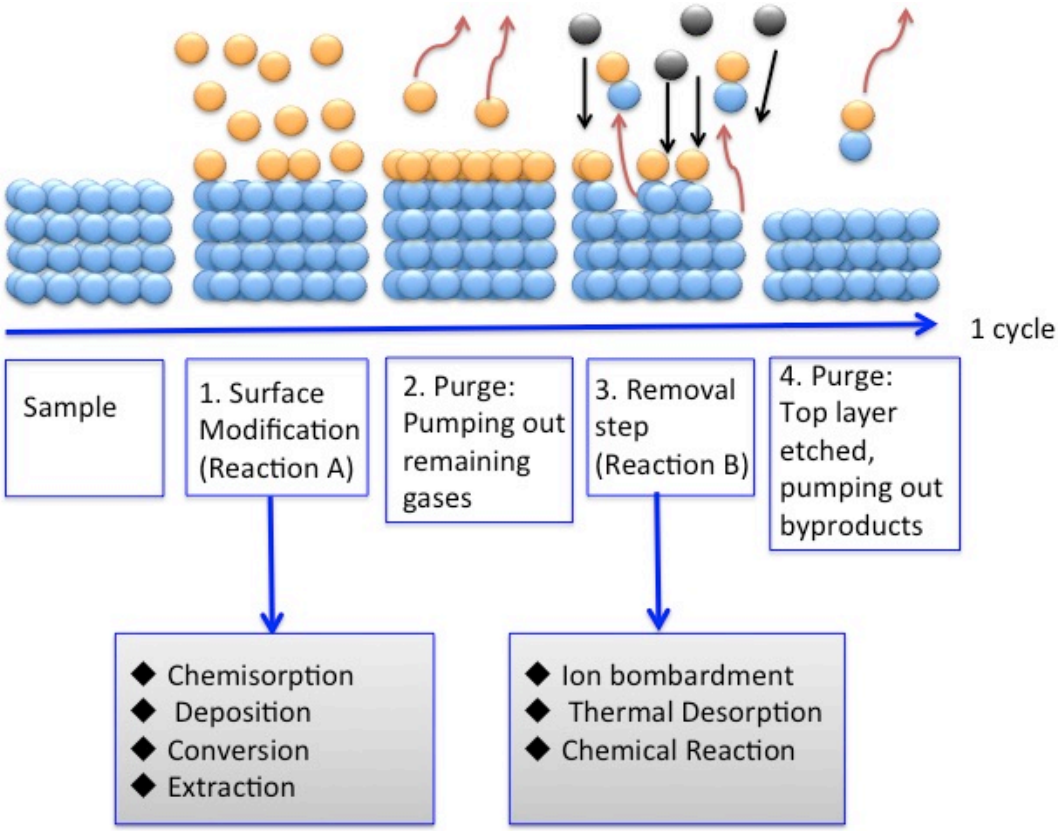

Figure 3.0.1: A schematic of the atomic layer etching process [16].

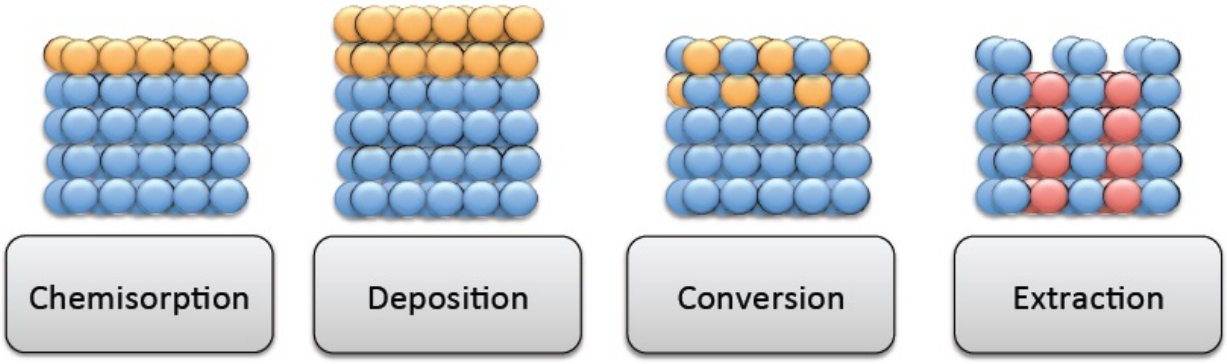

Figure 3.0.2: A schematic of four different surface modification approaches used for ALE.

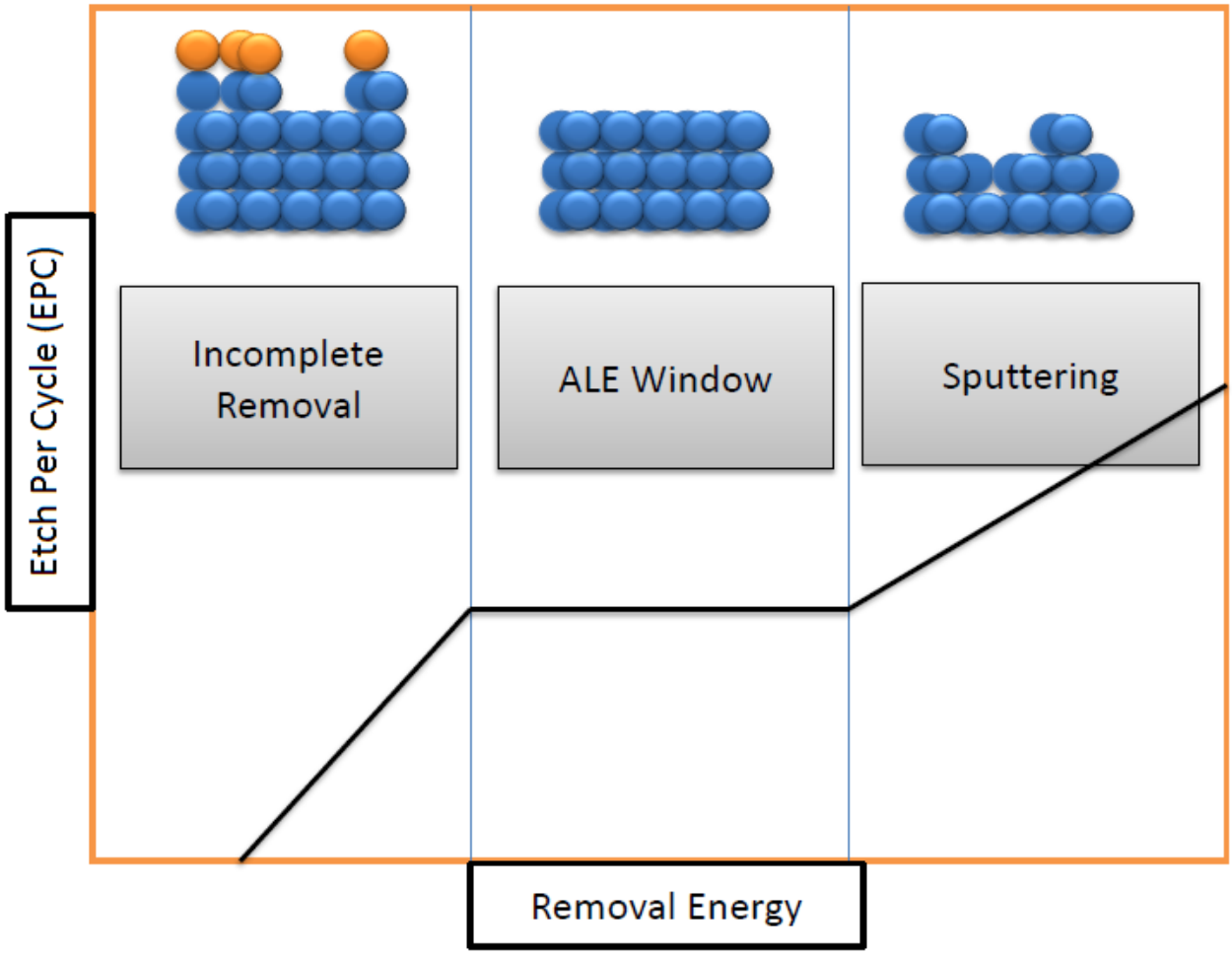

Figure 3.0.3: A schematic plot of an energy scan in removal step (Reaction B). The range of energies suitable for atomic layer etching is indicated as 'ALE Window' [16].

activation and the other material is etched in the removal step [16]. A schematic of the all four methods is given in Fig 3.0.2. After pumping out the remaining gases, following surface modification, the activated surface layer is removed in the removal step (Reaction B). There are three ways to remove the modified layer. The most common way is energetic ion bombardment. Usually, Ar neutral beam or low-energy Ar^+ ions are used for the bombardment and consequently this leads to a very anisotropic process. The other two methods of selective removal thermal desorption and chemical reaction are isotropic approaches.

Requirements and Characteristics of Atomic Layer Etching: There are few criteria to follow in the ALE process. First of all, the so called **Synergy test**: the two major steps (Reaction A and Reaction B) should not etch when done separately from each other. In practice, there could be some etching in individual steps, however, this etching rate should be negligible in comparison to the etching rate when both Reaction A and Reaction B are combined [1, 16]. In the removal step (Reaction B), the removal energy should not go beyond the threshold of the **ALE Window** shown in Fig 3.0.3. The ALE window is often

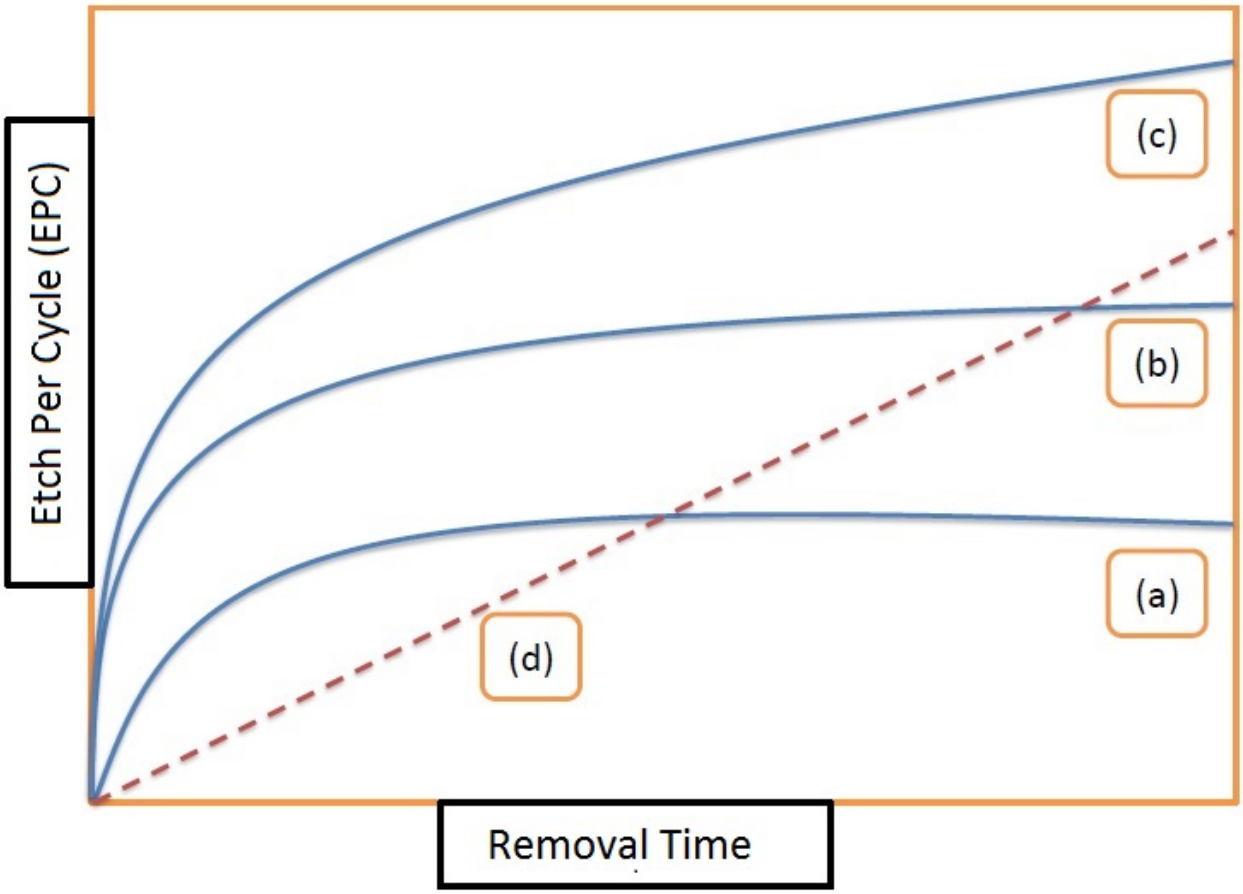

Figure 3.0.4: Schematic plot of different types of saturation curves for removal step (Reaction B): (a) saturation for small etching rate, (b) saturation for larger etching rate, (c) quasi self-limiting saturation curve, (d) conventional continuous etching for comparable etching time [16].

used for the characterization of the ALE process. Low removal energy, below the threshold, results in incomplete removal of the modified layer. High removal energy, above the threshold, results in sputtering of the unmodified material. However, the width of this window depends on the specific reactant, target and energy combination [16].

The self-limiting nature of all the basic steps in the ALE process is an important advantage for ALE. It means that the process ensures a steady etching rate and small deviations in process conditions will not lead to large etch rate deviations. Different **Saturation Curves** are typically used as a proof of the self-limiting behavior, see Fig 3.0.4. In Fig 3.0.4, three different saturation curves are compared with conventional continuous etching. In fact, achieving this saturation is interconnected with operating in the ALE window. If the process operation occurs in the ALE window range, then only the volatile products formed on the modified surface should be removed. Even if the removal time is increased, there should be no additional etching (Reaction B), since the removal energy is not sufficient for etching of the unmodified material. In contrast, there is no etching limit for continuous etching.

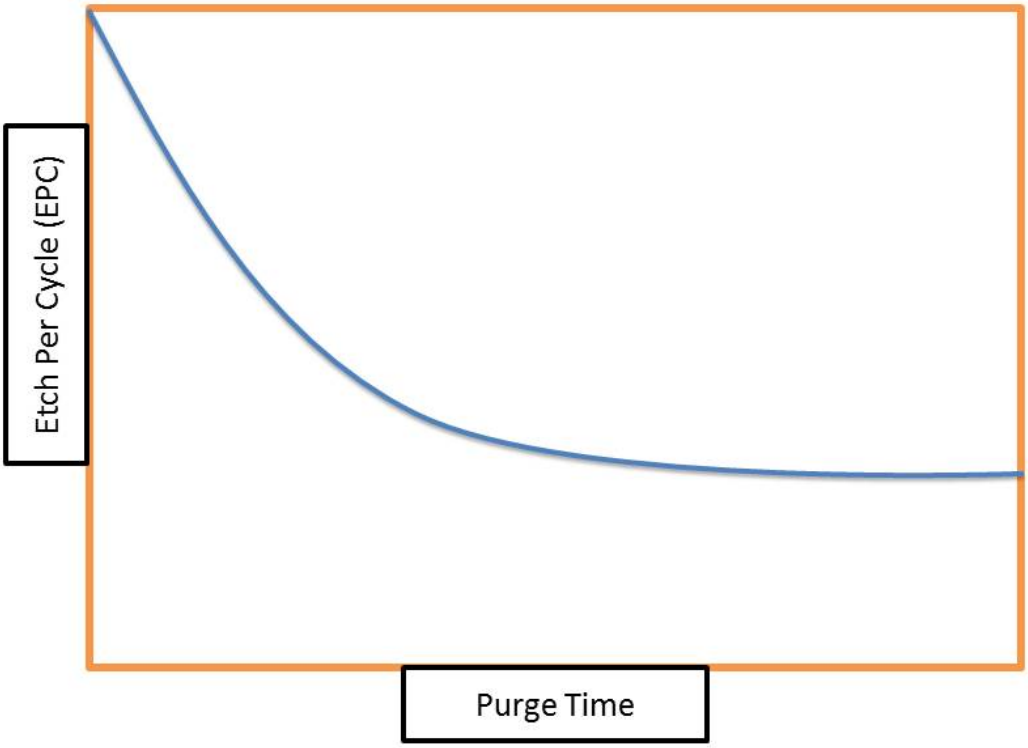

Figure 3.0.5: Etch rate as a function of purging time. The etch rate saturates for extended purging time. Similar curves are typically observed for purging after both Reaction A and Reaction B [36].

In real processes, the etch rate often does not get saturated like it does for the ideal process shown in Fig 3.0.4 (a) or (b). Depending on the reactor condition, ion energy, precursor reaction and byproduct pumping, the process may not saturate like it is shown Fig 3.0.4 (c). In this case, we refer to this process as quasi saturation behavior. However, operating in this quasi-saturation mode is still very interesting and important for industrial processes as this enables faster ALE processes [16].

The Purging time for both pumping out remaining gases after surface modification (Reaction A) or after removal of the modified layer (Reaction B) is another important parameter for ALE. As discussed earlier, there is a time gap needed in between the surface modification and the removal step in order to pump out the byproducts from the reactor avoiding parasitic etch reactions [36]. This time should be sufficient to take out all the gases left after the surface modification from the chamber. Fig 3.0.5 shows a schematic plot of the etch per cycle (EPC) as a function of purging time, where EPC gets saturates after a certain time.

The scientist only imposes two things, namely truth and sincerity, imposes them upon himself and upon other scientists.

Erwin Schrodinger

4

Experimental Details

ALE experiments in this research project were carried out at the Lund Nano Lab. Conventional Inductively Coupled Plasma-Reactive Ion Etching (ICP-RIE) Plasmalab System 100 from Oxford Instruments was used in this work. For characterization of the process, we used Ellipsometry, Scanning Electron Microscopy (SEM), Atomic Force Microscopy (AFM), X-ray Photoelectron Spectroscopy (XPS). Silicon on insulator (SOI) samples were used for basic characterization of the etching processes. In our experiments, we also used GaP NWs and Si samples with a mask made of hydrogen silsesquioxane (HSQ).

The ICP-RIE Plasmalab System 100 is a quite common etching tool. Fig 4.0.1 shows the ICP-RIE in LNL and its schematics. A sample holder can carry samples on 4 inch or 6 inch sample carriers. This is one of the two plates of a large plate condensator fed with a radio frequency (RF) generator. The RF power applied generates plasma and cause the plasma based etching. There is also a large coil surrounding the top of the chamber, which inductively couples RF power to the plasma inside the chamber, so called Inductively Coupled Plasma (ICP). Different gas bottles are situated just outside the system and the lines from those gas bottles are connected to the vacuum chamber. Each gas line contain a valve which is opened depending on gas needed for a particular process [37]. A computer controls the tool. There are few limitations of this system for ALE: (1) chamber walls are made of aluminum which can adsorbs some Cl_2, (2) the ion energy cannot be controlled directly and (3) switching of the gases inside the chamber is slow which makes ALE process slower.

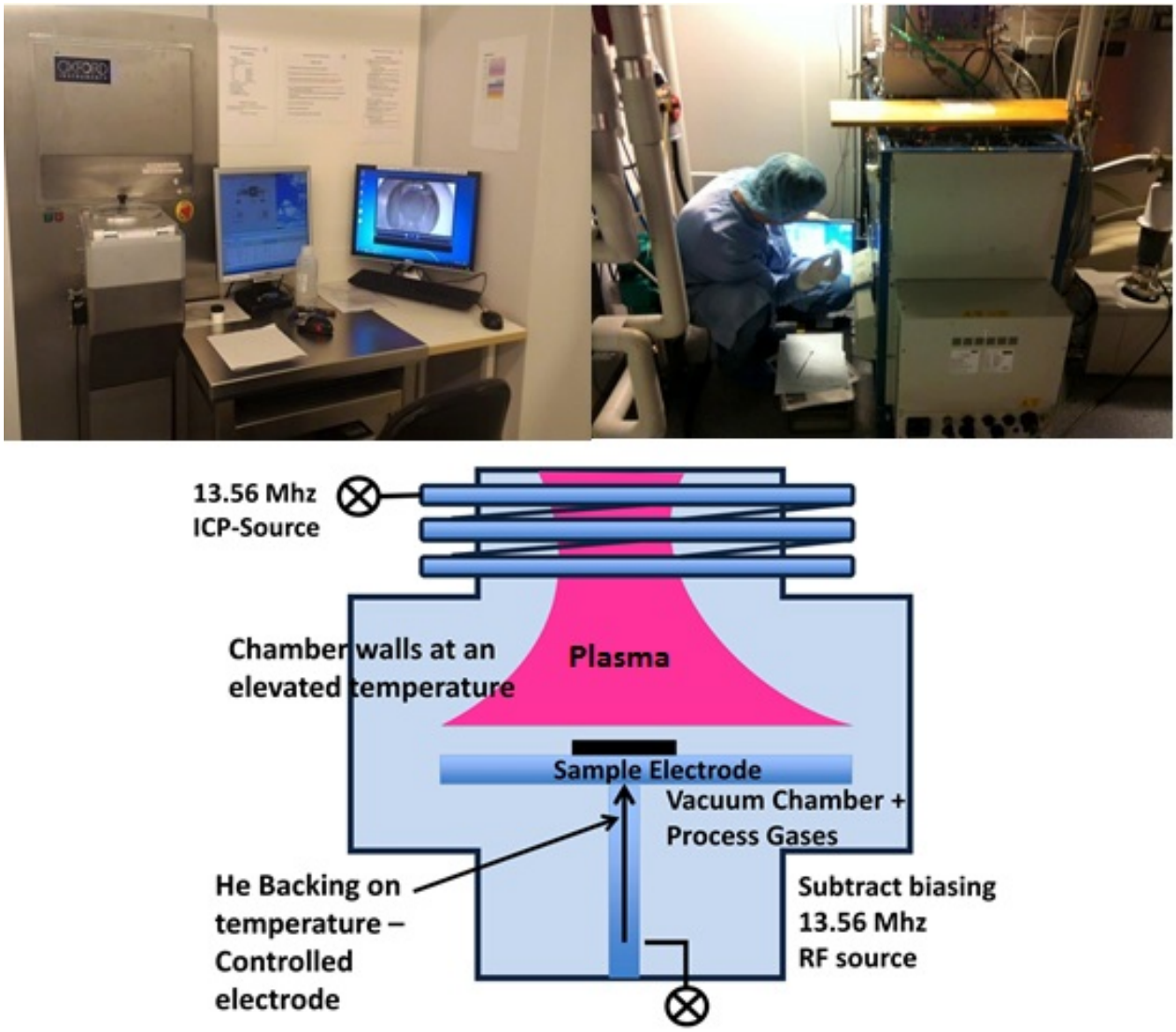

Figure 4.0.1: ICP-RIE Oxford Plasmalab system 100 at LNL and the central part of the system [37].

The Ellipsometer was used to measure (1) thickness of the top Si layer of SOI samples, (2) thickness of the top SiO_2 layer for native oxide and for deliberately oxidized Si samples, (3) surface roughness. SOI samples were checked by ellipsometry before and after etching to measure the etch rate. The ellipsometer uses the basic principle of light that goes through some polarization change when reflected from the surface of a material. In the ellipsometer, a light from the source hits the sample surface at different angles and is reflected back with some polarization changes. A detector at the other end recodes this change of polarization. Since, the change of the reflected signals depends on the thickness of the materials, different layers thickness can easily be measured with the ellipsometer [38]. Fig 4.0.2, shows the basic principle of the ellipsometry operation and M-2000VI Spectroscopic Ellipsometer tool by J.A. Woollam Company at

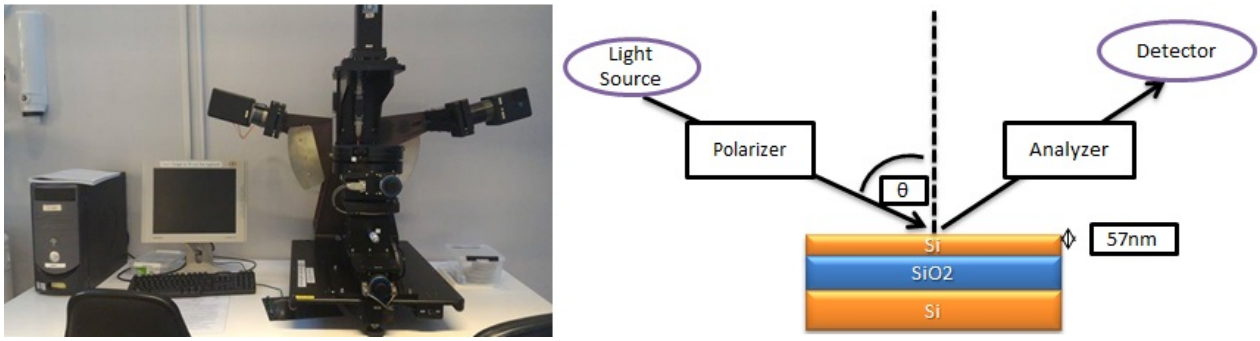

Figure 4.0.2: The ellipsometer used for this project at LNL and the basic principle of this system.

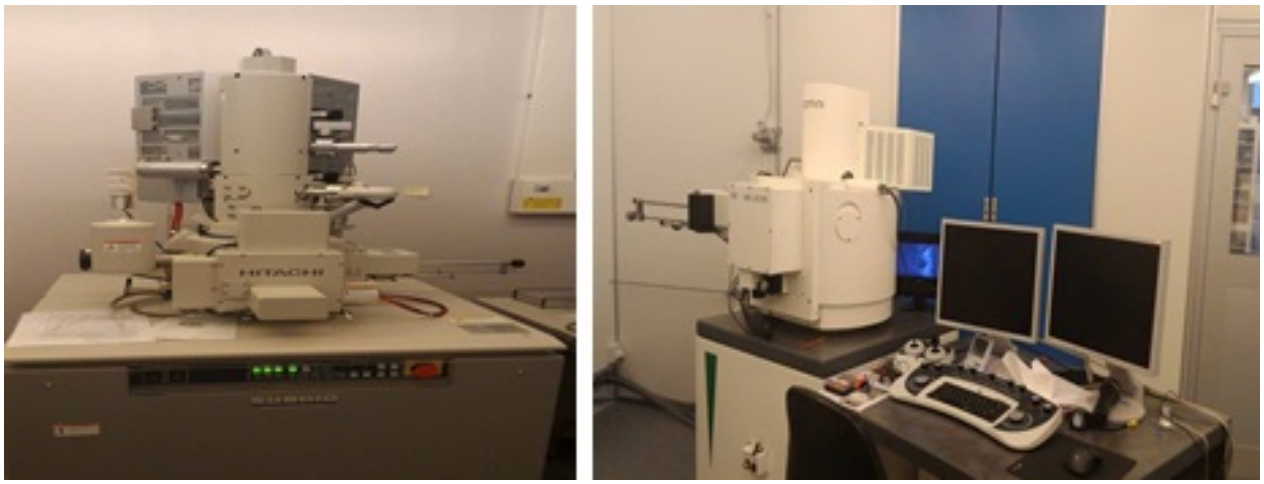

Figure 4.0.3: Hitachi SU8010 (left) and Leo 1560 (right) SEM used in this work at LNL.

LNL.

Scanning electron microscopy (SEM) was used for imaging nanowire samples, Fig. 5.0.5, and patterned samples, Fig. 5.0.7. In SEM, we have a source of electrons, which is called electron gun. The speed of electrons emitted from the gun is controlled by the potential applied to the cathode and anode. The condenser lens controls the size of the beam and the amount of electrons travelling down the column. The objective lens then focuses the beam into a spot on the specimen. The electron beam spot size is very important for high-resolution images. In SEM, a focused beam with a small spot size is used to scan over the sample surface. At the same time scattered and secondary electrons coming back from the sample surface are detected. This detected signal is then used to reconstruct the surface image [39]. SEM was the most frequently used tool in this work. Used SEM tools at LNL are shown in Fig. 4.0.3.

The sample surface was also investigated by **Atomic Force Microscopy (AFM)**. AFM allows high-resolution topographical imaging of the sample surface and can be operated in different modes: contact mode, non-contact mode and tapping mode. In the contact mode, the tip at the end of the probe cantilever scans over the sample surface and monitors the change of the cantilever deflection. A photodiode detec-

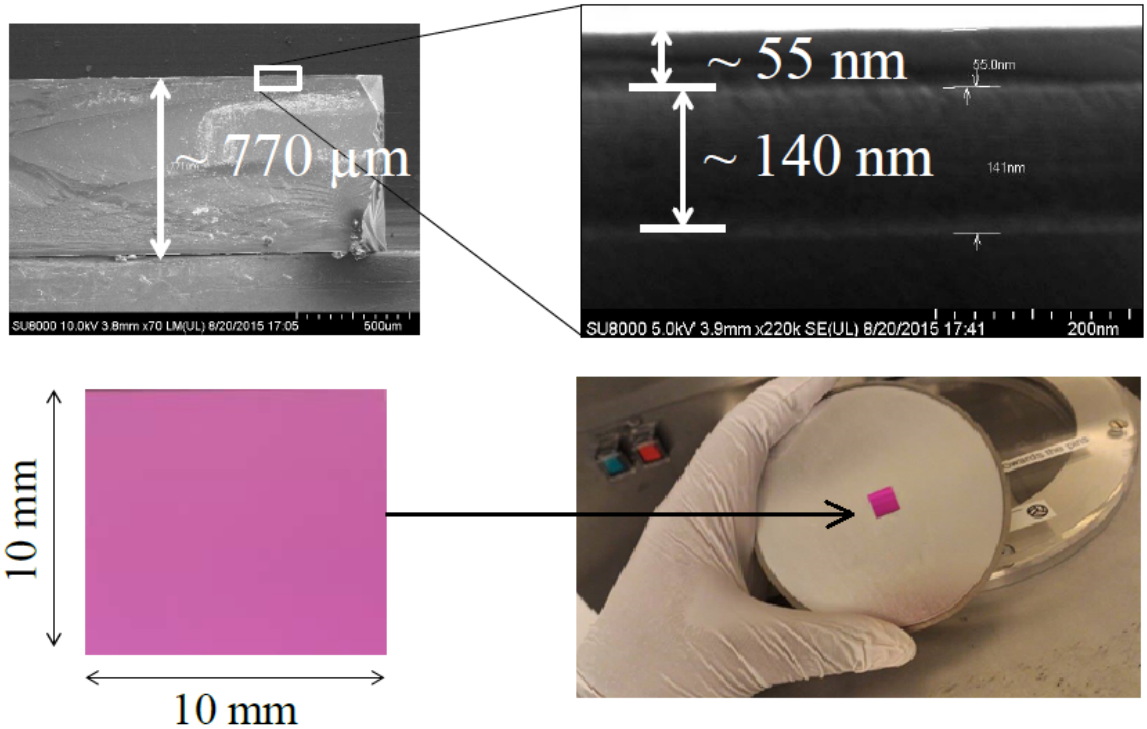

Figure 4.0.4: Silicon on insulator samples: SEM images of the side view (top images) and the top view (bottom images).

tor records the deflection. This mode is very fast and can allows- 'atomic resolution'. However, there is a possibility that- shear forces can distort features in the images and the sample surface can also be damaged during this imaging. In the non-contact mode, the tip doesn't get in contact with the surface. In this mode, the cantilever oscillates above the surface and a constant oscillation amplitude is maintained by moving the scanner vertically. In this case, the operation speed is much slower and the lateral resolution is lower than in other two operation modes. But the advantage of this mode is that no force is applied to the sample surface and there is no surface damage. Finally, in tapping mode- AFM probe tip lightly "taps" on the sample surface and that's the reason for the name of tapping mode. Although the scan speed of this mode is slower, higher lateral resolution on most samples can be achieved with low sample damage [40]. In this work, the samples were examined by AFM in the tapping mode. The core reason to check with AFM was to examine whether the surface roughness changes after ALE. Hence, the same sample was checked with AFM before and after ALE.

In addition, XPS was performed at the Technical University of Dresden in order to compare the sample surface condition before and after ALE.

SOI samples detail: To simplify the measurements, Silicon on insulator (SOI) was used instead of bulk Si. There were 3 different layers of this sample: Si-SiO_2-Si, hence an ellipsometry model was built in

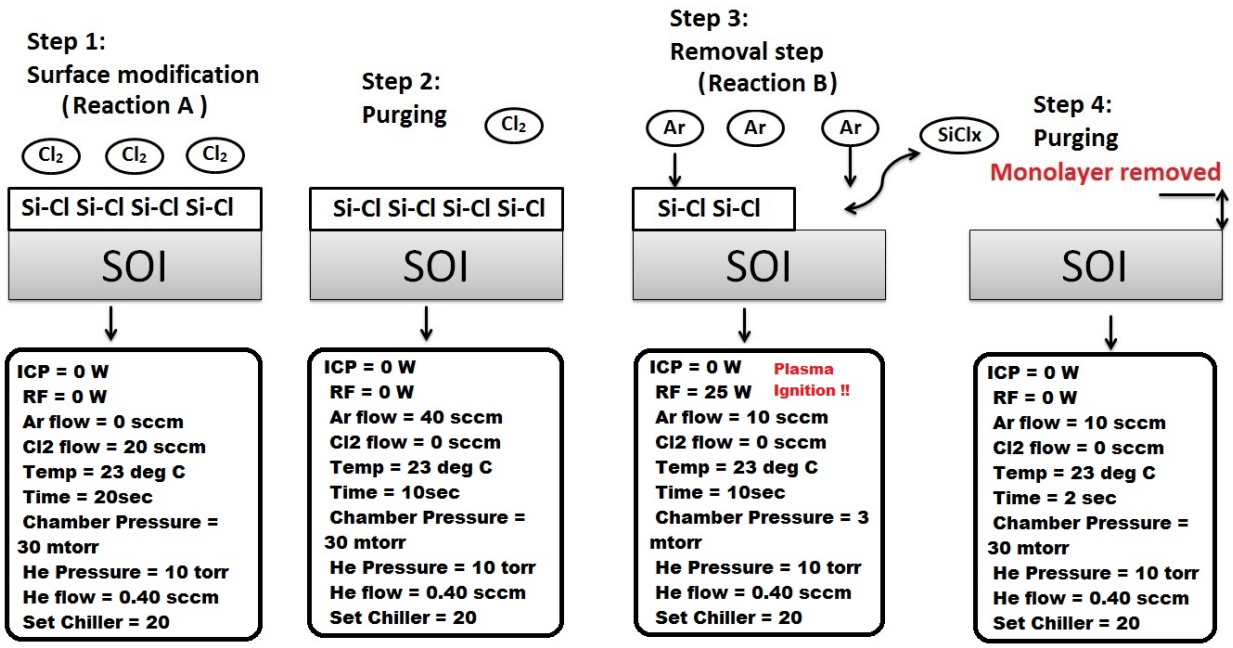

Figure 4.0.5: Schematic diagram of ALE process and parameters used in this study. Compare with Fig. 3.0.1.

such a way that can fit for all three different layers. However, our concern about thickness was the top Si layer, which was 57 nm. Moreover, a 15 Å layer for the native oxide was added on the top of the model so that the native oxide should not interrupt our thickness measurement. This native oxide has an additional advantage to check surface roughness. Fig. 4.0.4 shows the SOI sample thickness and SEM image used in the experiment.

ALE process recipe for Si: To perform Si ALE, Cl_2 was used for surface modification, followed by Ar bombardment for modified surface removal. With the Cl_2 flow, the top layer of Si becomes $SiCl_3$; as a result, Cl_2-Cl_2 bonding gets easy to break with small energy. In the removal step, energetic Ar ions knock out the top layer of $SiCl_3$ from the surface with approximately one layer of Si removal. Fig. 4.0.5 shows a schematic diagram with parameters selected for our ALE process.

Experimental setup for GaP NWs ALE : GaP nanowires used in this research project were fabricated as described elsewhere [41] with gold aerosol particles as growth catalysts on GaP (111) substrates by Metal Organic Vapor Phase Epitaxy (MOVPE). The ALE was performed with GaP NWs on GaP substrate. Then, the GaP NWs were transferred on SOI samples before processing using a tissue paper. Fig. 4.0.5 shows the ALE process parameters which were used to perform ALE for GaP NWS with 35 cycles, 55 cycles, 70 cycles, 105 cycles and 210 cycles. It is reported by different researchers [5–7, 22, 23] that the etching chemistry of the III-V materials and Si with Cl_2 is similar, hence the recipe described for Si can be expected to work for GaP NWs also. Our synergy tests indicate that indeed, the process is an ALE process for GaP NWs.

Fig. 4.0.6 shows the placement of the sample with NWs and reference SOI samples on the sample

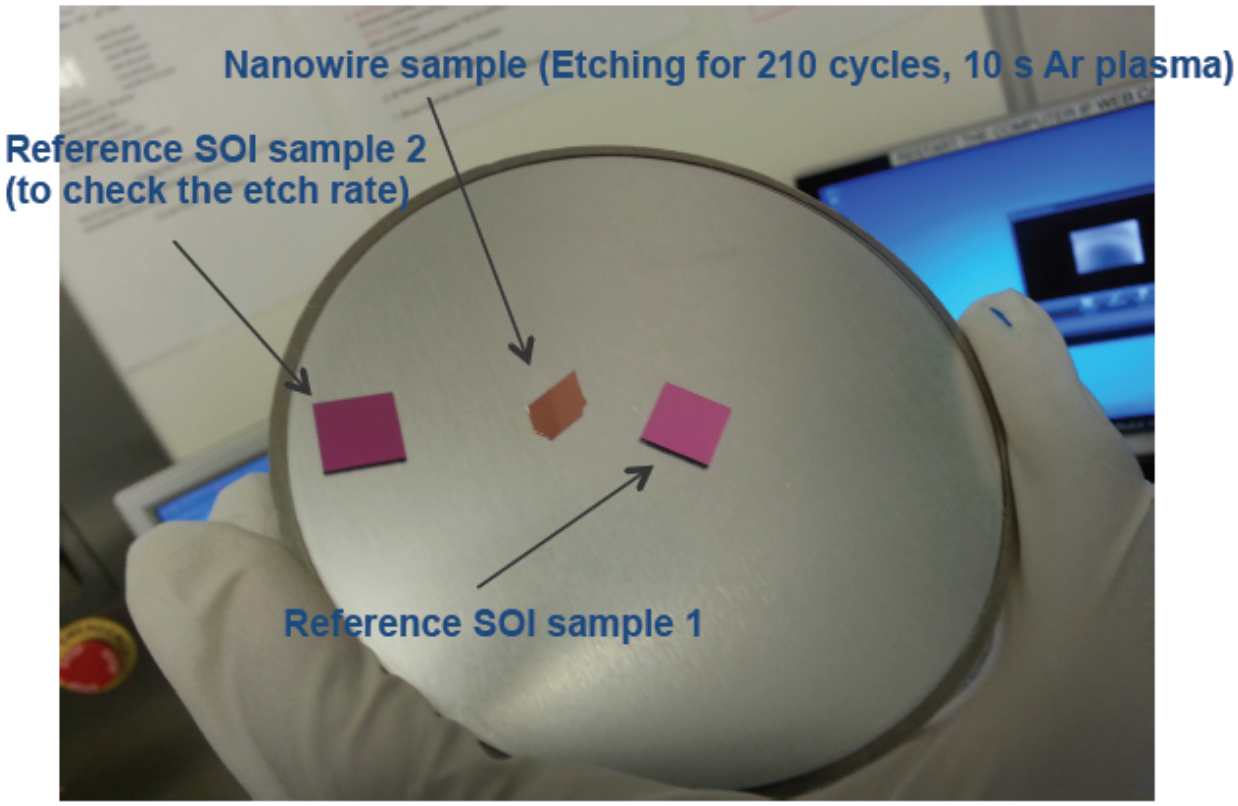

Figure 4.0.6: A sample with nanowires and a reference Si sample on the sample holder before ALE.

holder before the ALE process. Another SOI sample was placed at the periphery of the sample holder to examine the etch uniformity throughout the sample holder. NWs were placed nearer to the central reference sample.

Experimental setup for pattern transfer: Pattern transfer is one of the most important applications for any dry etching process. For an efficient pattern transfer a good etch selectivity between masking material and the substrate material is essential. Selectivity tests for our ALE process were performed for samples with a SiO_2 top layer and for Si samples as shown in Fig. 4.0.7. SOI, only Si and SiO_2 samples were mounted in the sample holder in order to check the selectivity.

The pattern transfer experiment were done with 50 nm thick HSQ (hydrogen silsesquioxane) patterns (essentially SiO_2) made with electron beam lithography (EBL) on Si surface. EBL was done as follows: 2 inch silicon (100) wafer, Dow Corning XR-1541 50 nm thick electron sensitive resist exposed with a system for electron beam lithography (Voyager, Raith GmbH) with 50 kV accelerating voltage. After exposure, the resist was developed in aqueous solution of NaOH (1 wt %) and NaCl (4 wt %) for 10 min at 24 °C. Post exposure sample surface cleaning with ozone at room temperature for 10 min was done in an UV-ozone cleaning system (UVOH 150, FHR Anlagenbau GmbH).

HSQ patterned sample was mounted on the sample holder with a reference SOI sample as shown

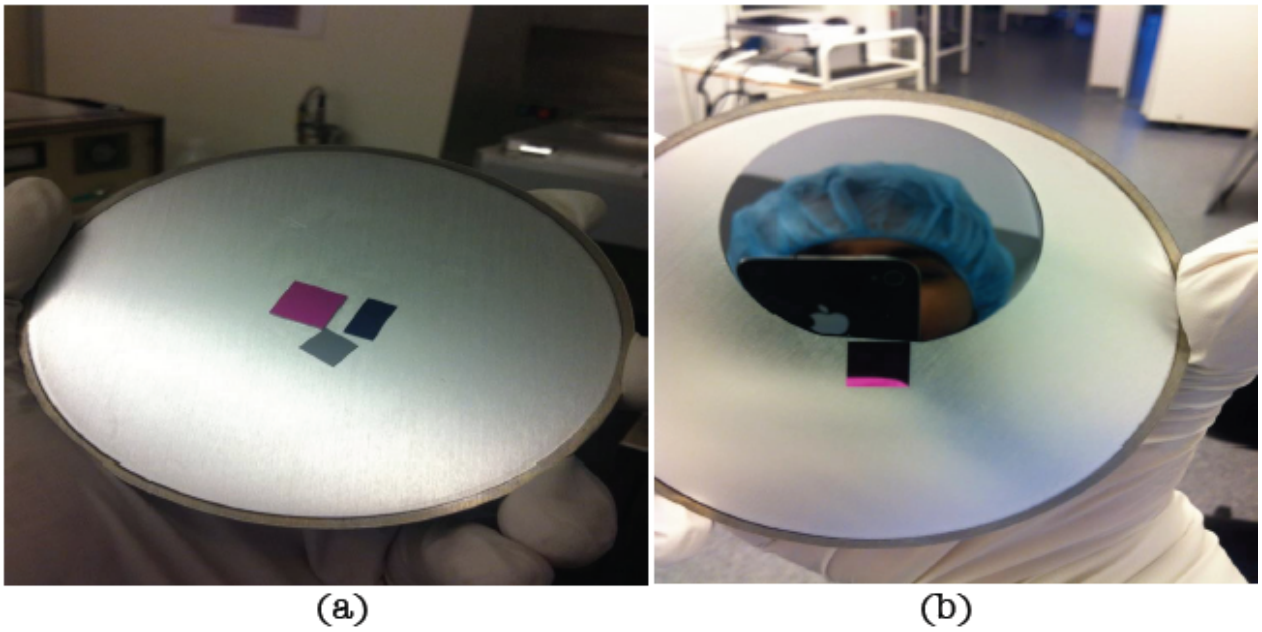

Figure 4.0.7: (a) Selectivity test of Si with SiO_2 (b) SiO_2 pattern on Si sample and SOI reference sample.

in figure Fig. 4.0.7.

Finally, Nanoimprint lithography was done by hot embossing with 50 bar pressure at 170°C in 250 nm thick PMMA layer using NIL-6 imprinter system from Obducat AB.

A scientist in his laboratory is not a mere technician: he is also a child confronting natural phenomena that impress him as though they were fairy tales.

Marie Curie

5 Results and Discussion

The ALE recipe in our experiment was optimized for Si, since this case is well established and easier for characterization. The desired etching rate was achieved with low RF power and low chamber pressure. The same recipe was used later for ALE of GaP NWs and for testing the ALE pattern transfer to Si substrate. Detailed results are presented below:

ALE process development with SOI samples: Initially, synergy test were performed to verify the background etching. As discussed in Chapter 3, any of the individual steps should not result in material etching. The SOI samples were exposed in the chamber for 15, 35, 70 and 105 cycles to only Cl_2 (step 3, removal step was excluded in this case) flow resulting in no measurable etching (bellow detection limit). Processed sample were checked in the Ellipsometer. The same number of cycles was performed with Ar plasma irradiation (step 1, surface modification was excluded in this case) in the chamber causing an etch rate of 0.03-0.04 Å/cycle. This small amount of etching is likely due to Ar ions sputtering on the sample surface and constant with respect to the number of etch cycles.

However, the combination of both steps leads to the etch rate in the range of 2.00-2.28 Å/cycle. Hence, the background etching due to the Ar bombardment is negligible compared to the combined etch rate. It was also observed in the experiments that it takes a few seconds to stabilize the plasma after plasma ignition and the background etching could be due to ion energy fluctuations during the plasma stabilization time. Other researchers also reported this effect [16].

No. of Cycles	Etch Depth (Å)	Etch Depth (Å) (reverse)	Etch Rate (Å/cycles)	Etch Rate (Å/cycles) (reverse)	Background Etching rate(Å/ cycles)
15	30	--	2.10	--	0.040
35	80	70	2.28	2.00	0.040
70	150	160	2.14	2.28	0.030
210	460	455	2.19	2.16	0.028

Table 4.0.1: The original data of etch depth and etch rate for our ALE process

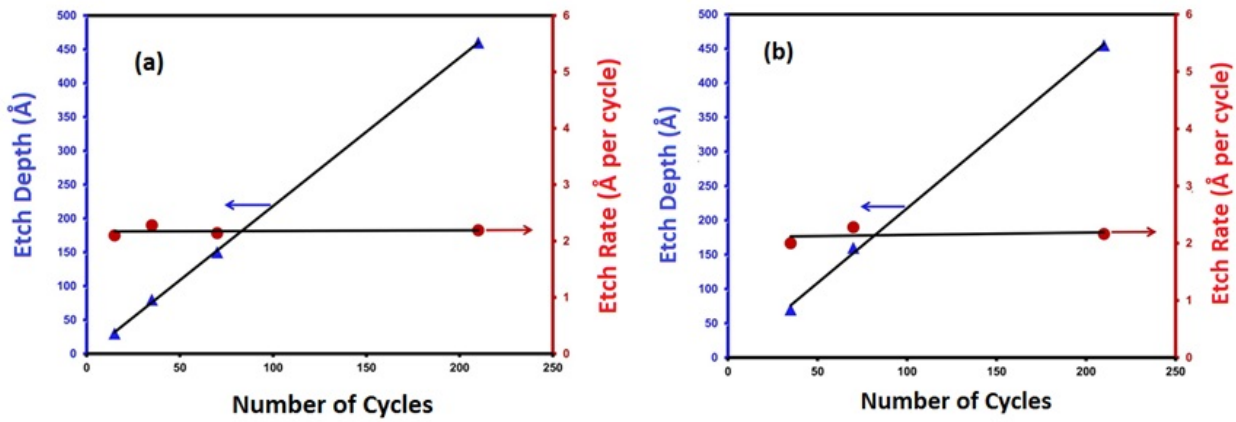

Figure 5.0.1: (a) Etch depth and etch rate as a function of number of cycles: ascending order (b) descending order.

Fig. 5.0.1, shows that the etch rate is stable and the etch depth is linearly increasing with number of cycles. The experiments were performed in both ascending and descending order of cycles. Comparing both cases, the etch rate doesn't seems to deviate significantly.

After ALE, the etch rate of SOI sample on holder periphery, (reference 2, see Fig. 4.0.6) was 1.90 Å/cycles and the etch rate of the central SOI sample (reference 1, see Fig. 4.0.6) was 2.23 Å/cycles. Hence, the etch rate is not uniform and it decreases by shifting the sample position from center to the periphery of the sample holder.

The etch rate of the ALE process should saturate with respect to Ar bombardment time in removal step (Reaction B) as shown in Fig 3.0.4. The saturation phenomena observed in our case, see Fig. 5.0.2, is similar to the quasi-saturation mode shown in Fig 3.0.4 (c), which means additional etching can be obtained for longer Ar bombardment time. This indicates that, the aluminum chamber walls desorb Cl_2 during Reaction B. In Fig. 5.0.2, the high etch rate for 120 sec and 180 sec ALE process time, performed after ALE process with 900 sec of Ar bombardment, corresponds to Cl_2 desorption during the process.

Fig. 5.0.3, shows an etch rate per cycle as a function of Cl_2 purging time in the ALE process. With low purging time, remaining Cl_2 gas in the chamber participates in the etching process during Reaction B, resulting in higher etch rate. In our ALE process, the purging time typically was 10 sec and, as it can be seen from Fig. 5.0.3, we operate outside of the saturation region and some of the remaining Cl_2 in the chamber

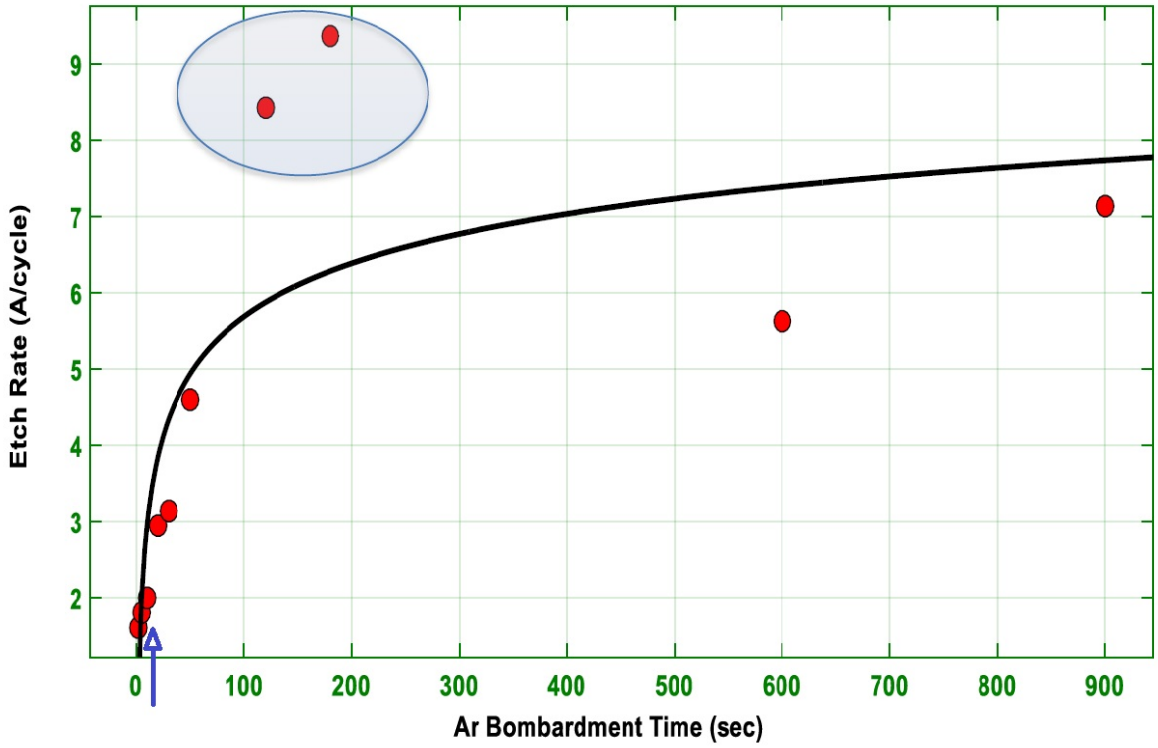

Figure 5.0.2: Etch rate as a function of Ar bombardment time. The arrow indicates the operational point.

participates in the ALE process which makes our ALE non-ideal.

An ideal ALE process should not damage the etched structures and the sample surface should be smooth and clean after ALE. In our experiments, the sample surface roughness was verified before and after ALE with AFM, SEM and an ellipsometer. It was found that the surface roughness after ALE does not exceed the roughness of intact SOI samples (< 1 nm). In addition, XPS analysis revealed no change in surface chemical composition after the ALE process.

ALE of GaP nanowires: The NWs sample images before etching are shown in Fig. 5.0.4.

After ALE, Fig. 5.0.5 demonstrate that, individual NWs are split into two different NWs. This was observed on NWs all over both of the GaP and Si substrates.

The mechanism of dividing NWs is described in Fig. 5.0.6. Since the NWs have hexagonal shape, the etching rate at the top of the surface is higher than the etching rate of the facet resulting a channel formation in the middle. Ion interaction with surface depends on the impingement angle and on the ion energy, which depends on local electric field. Sharp corners like NWs broken edges change the local electric field. As a

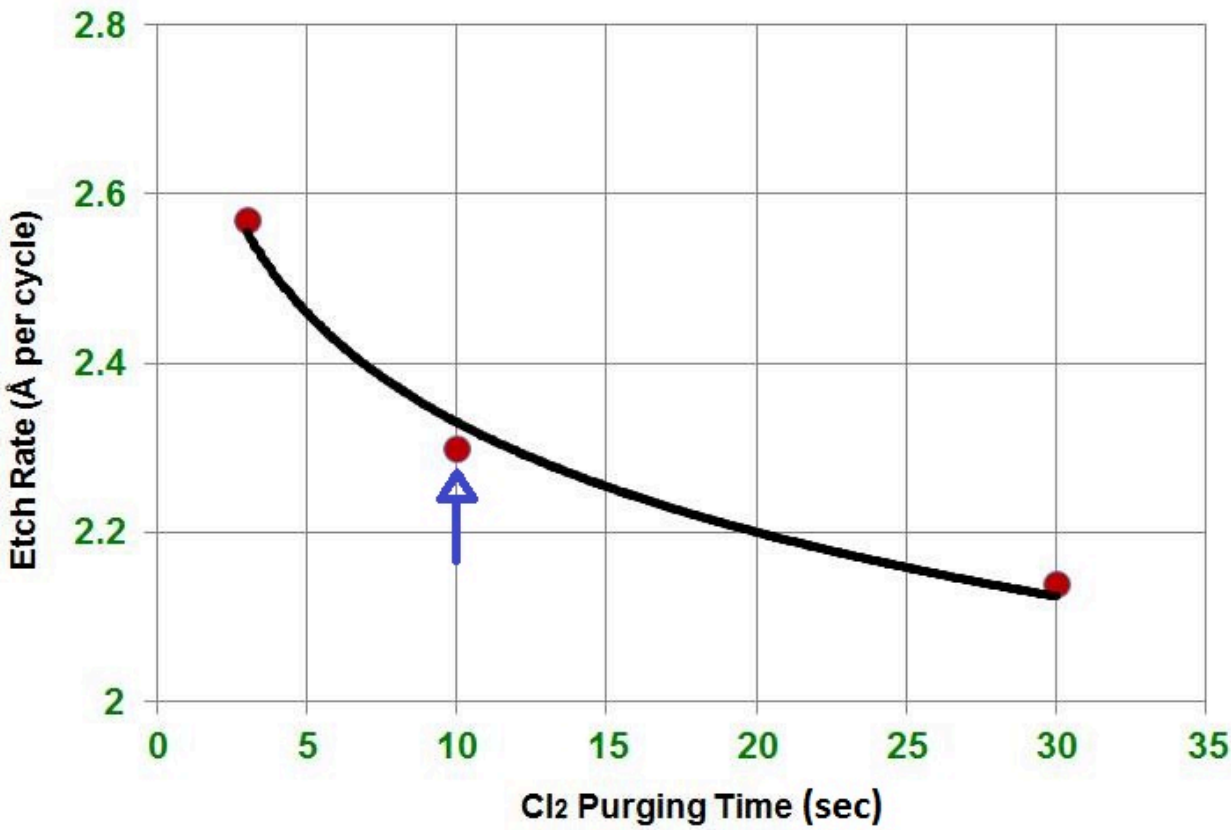

Figure 5.0.3: Etch rate as a function of Cl_2 purging time. The arrow indicates the operational point.

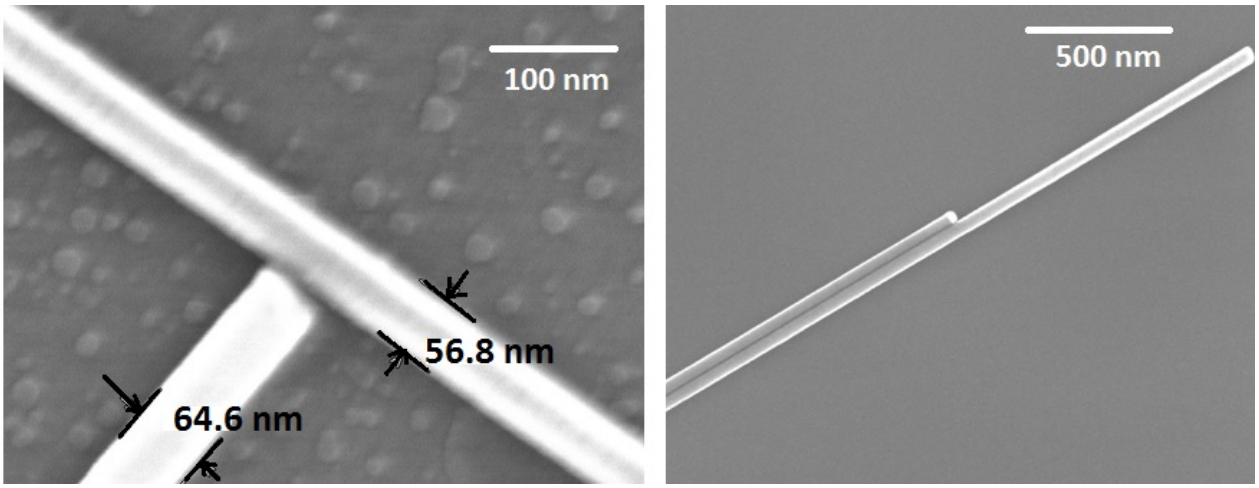

Figure 5.0.4: SEM images of GaP nanowires sample before etching. The nanowires were grown in a very controlled way with diameter varying 40-65 nm. The left image shows GaP nanowires on GaP substrate and right image shows GaP nanowires mechanically transferred on SOI substrate.

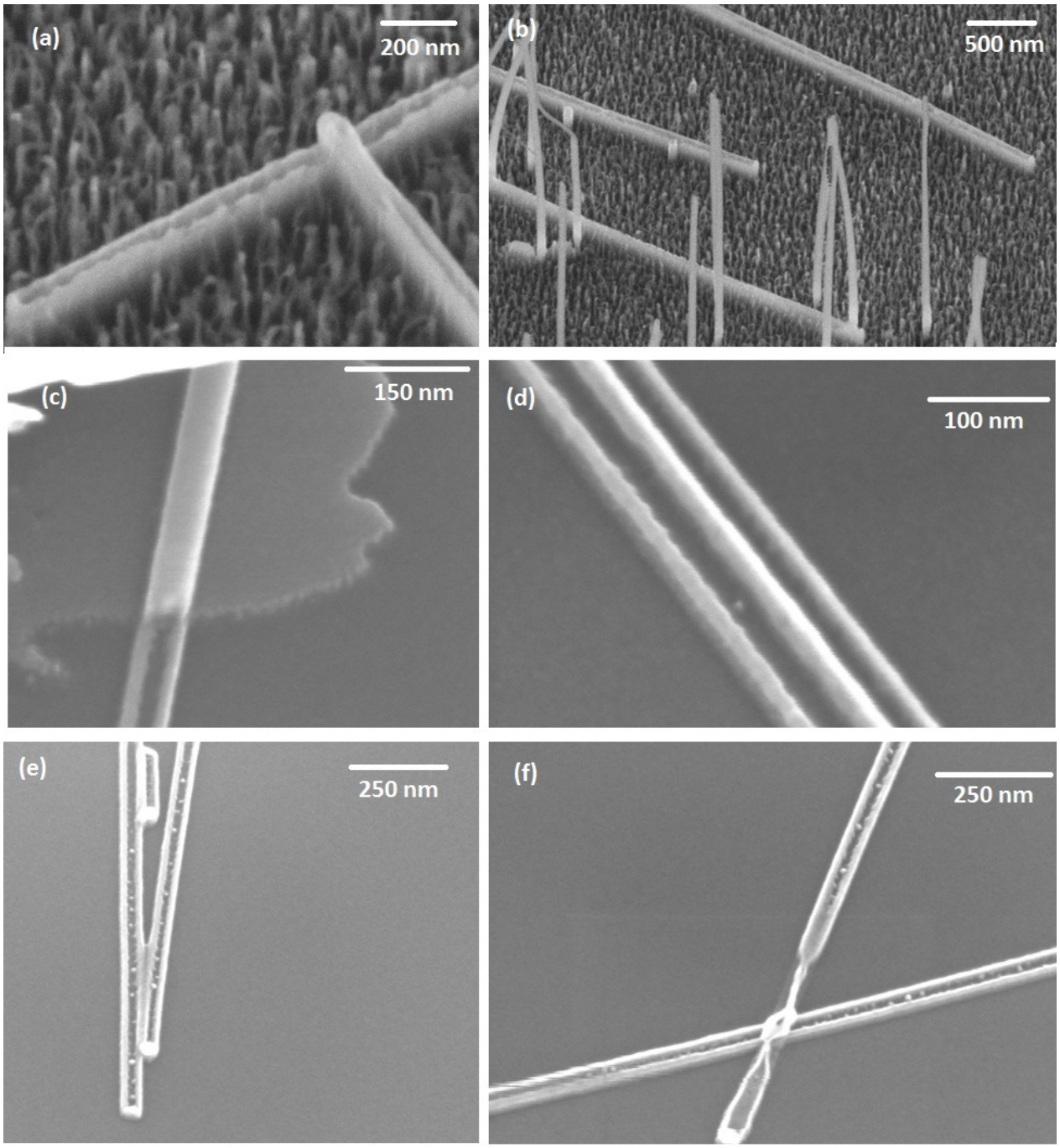

Figure 5.0.5: SEM images of nanowires after the ALE process (a) GaP nanowires on GaP substrate. Nanowires are divided into two parts (b) The process is very anisotropic: vertical nanowires are not affected by the process while horizontal nanowires are etched, (c) Part of the nanowire has not been etched due to a hanging mask, (d) Etching profile of attached nanowires (e) GaP nanowires on SOI substrate after ALE demonstrating that the result of NW ALE does not depend on NW length (f) One NW on top of the another NW, the double NW masking effect resulted in a hole formation.

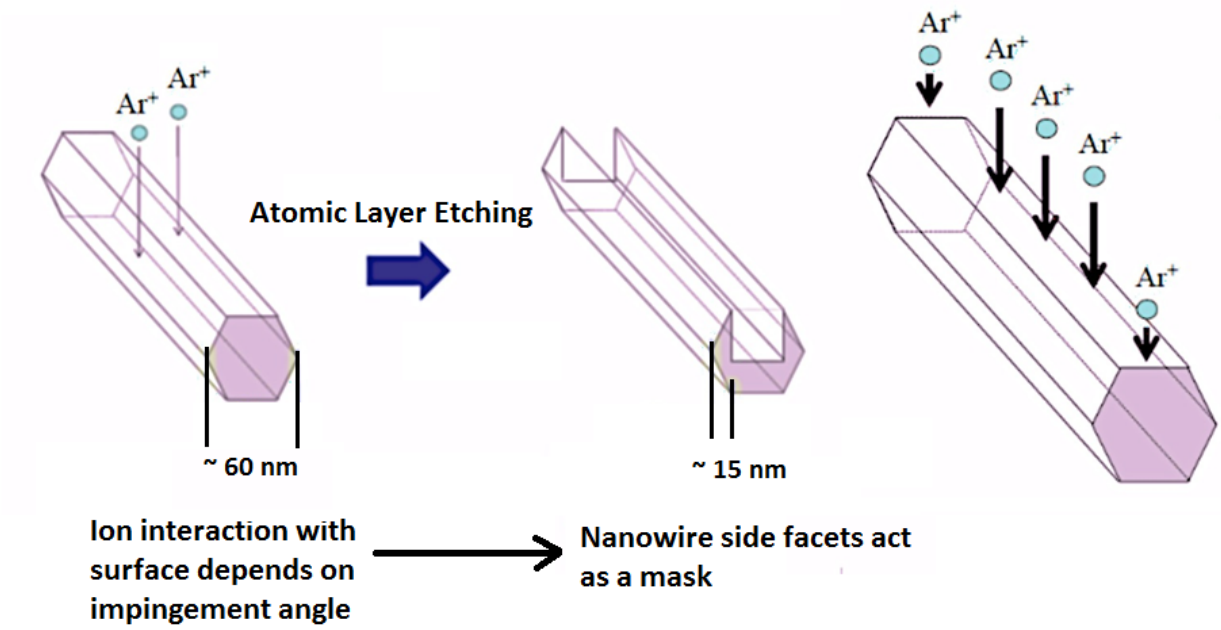

Figure 5.0.6: Mechanism of nanowires etching.

result, Ar ion cannot transfer sufficient energy to the surface that means these edges and facets act as a mask during ALE process. This is why the middle portion of NWs are etched faster leaving two thin NWs on the border.

Fig. 5.0.5 (f), shows a twisted NW edge which acted as a mask over another nanowires. In addition, the process exhibits strong anisotropic behavior as shown Fig. 5.0.5 (b), where some of the vertical NWs seem to be unaffected during the process while etching phenomena on the horizontal nanowires are similar. According to Fig. 5.0.5 (e), the ALE result does not depend on the longitudinal NWs size and arrangement, since small nanowires are etched in a similar manner as long nanowires.

Pattern transfer with ALE and ALE application for nanoimprint lithography: In the selectivity test (see Fig. 4.0.7), for 210 cycles of the ALE process, the etch rate of reference Si and SOI sample was 2.16 Å/cycle whereas the etch rate for SiO_2 was 0.133 Å/cycle. For 70 cycles, the etch rate for Si and SOI sample was 2.28 Å/cycle whereas the etch rate of SiO_2 was below detection limit in the ellipsometer which means that the etch selectivity between Si and SiO_2 was more than 10.

In the pattern transfer experiment, the HSQ patterns acted as a mask and the sample was etched almost 200nm with 850 cycles of ALE process, so that the pattern transfer can be clearly visible in SEM. In addition, the Si surface was checked to confirm that the process is stable during the ALE process.

As shown in Fig. 5.0.7, the pattern was successfully transferred to the Si substrate. The SEM images (a) and (b) show two different types of HSQ pattern on the sample which were used for testing pattern transfer with ALE. From the images we conclude that, HSQ patterns are well preserved and Si beneath the

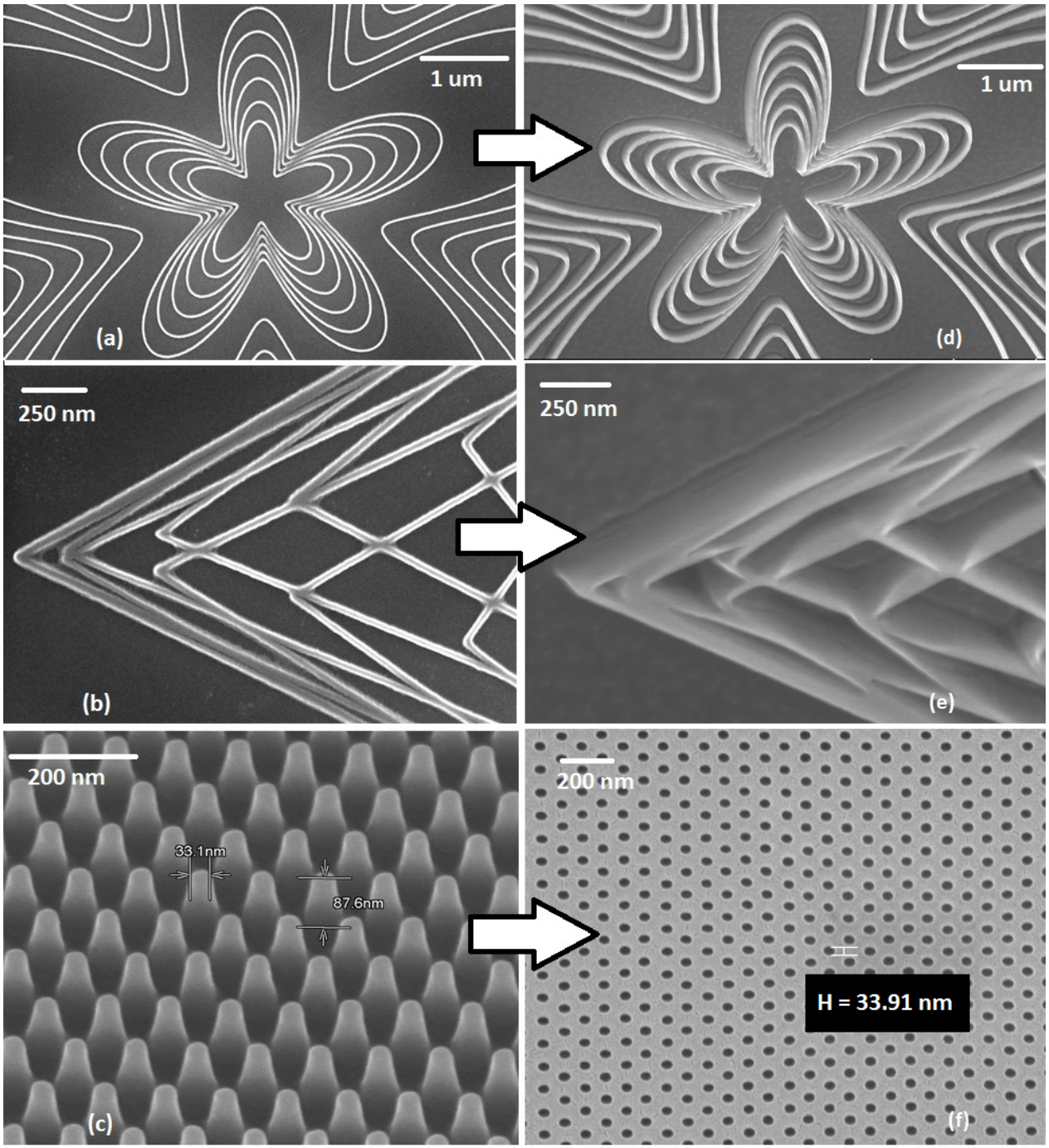

Figure 5.0.7: SEM image of high resolution pattern transfer with ALE. (a) and (b) two different types of HSQ pattern on Si before etching. These patterns are 50 nm thick and made with EBL technique. (d) and (e) show, 3-D shape HSQ patterns after 200 nm (850 cycles) of ALE. HSQ patterns are intact and about 200 nm Si has been etched beneath HSQ and the pattern has been nicely transferred. In (c), dot pattern used as a stamp to perform nanoimprint lithography and (f) the nanoimprinted structure.

HSQ was etched resulting in pattern transfer to Si substrate. These etched structures were used as a stamp for nanoimprint lithography as shown in Fig. 5.0.7 (c) and (f). Hence, ALE can be used for high-resolution fabrication of stamps for nanoimprint lithography.

A scientific truth does not triumph by convincing its opponents and making them see the light, but rather because its opponents eventually die and a new generation grows up that is familiar with it.

Max Planck

6 Conclusion

The ALE possibility at Lund Nano Lab has been investigated and ALE of Si was successfully performed in this research project. We have also revealed different limitations of ALE with our current equipment and provided recommendations for new equipment needed to set up ALE at LNL. As discussed in Chapter 4 and Chapter 5, the optimal process recipe achieved in the system was not ideal atomic layer etching due to the additional Cl_2 desorption from Al chamber walls. But the process can be referred as atomic layer etching. The process was found to be highly anisotropic. We observed the following limitations: the process occurs slowly and controlling the ion energy is difficult. However, the ALE process in a conventional ICP-RIE tool may be useful for research projects. To our best knowledge, this is the first time that the ALE process in conventional ICP-RIE has been reported.

Splitting horizontal NWs was one of the most fascinating outcomes of this work which indicates that ALE can be used for nanofabrication below 20 nm. One application of this NWs splitting could be advanced processing for FinFET fabrication. Two NWs can be replaced in the same FinFET architecture perhaps having better electrical properties. However, further examination is needed to prove the enhanced electrical properties of this split feature. Due to the time restriction and NWs availability, the splitting was only observed for GaP NWs. However, it will be really interesting to continue ALE experiments on NWs and see if the same phenomena can be obtained with other NWs also.

In addition, the procedure of shrinking or dividing NWs is limited by the size of the mask. Due to

the optical lithography limitation, it is very difficult to fabricate extremely small structures. On the other hand, our ALE process doesn't need any mask to divide NWs, which means that it may be possible to split transistor gates in a simple and economical way. Finally, high-resolution pattern transfer is a significant step of ALE application for nanofabrication, which could be very suitable in stamps fabrication for nanoimprint lithography.

All these findings have a potential to guide future development of ALE for nanofabrication of extremely downscaled devices and structures with atomic scale resolution. Anisotropic ALE process, especially for III-V semiconductor NWs, is another very important process for LNL which could enable controllable shrinkage of NWs diameter with minimal damage.

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