LUND UNIVERSITY
Faculty of Science

Characterization of single InP Nanowire-based Avalanche Photodetectors

Virgínia Boix

Thesis submitted for the degree of Bachelor of Science
Project duration: 2 month

Supervised by: Magnus Borgström
Co-supervised by: Vishal Jain

Department of Physics
Division of Solid State Physics
January 2016

ABSTRACT

Nanoscience is an emerging field of technology where the bottom-up fabrication techniques are utilized instead of the traditional top-down approaches for enhancing the performance of different optoelectronic devices. One such material is a semiconductor nanowire (NW) which holds immense potential in nanophotonic applications, such as solar cells, LEDs, lasers, sensors and photodetectors. In particular, detection of infrared (IR) radiation emitted by all bodies has wide applications in medical imaging, environmental monitoring, surveillance, security and optical communication.

This Bachelor's thesis fits in the purpose of developing novel devices which is part of a bigger project, aiming towards the fabrication and integration of efficient InP/InAsP NW Avalanche Photodetectors (APD). The NWs are designed with a Separate Absorption Multiplication (SAM) geometry in a vertical array pattern, but for a fundamental understanding single NWs are contacted in lateral geometry and characterized individually. The characterization setup used is a Cascade 11000B probe station equipped with a Keithley 4200 semiconductor characterization module.

Our efforts were focused on determining experimentally the breakdown voltage for two different samples of NW APDs, as an initial step of establishing the dependance of the breakdown voltage with the temperature. A study of the contacts was also addressed in order to provide more data to the design of an optimized ohmic contact in the p-segment of the NWs.

We could demonstrate that growing NWs with longer p-segments overcome the contacting issues previously reported. Additionally, we could recognize the influence on our results of the Schottky barrier present in the contact with the p^+-segment, especially in the values obtained for the ideality factor ($n = 1.2 \pm 0.1$ and $n = 1.53 \pm 0.12$). Therefore, we conclude that optimizing the p-segment contact should be prioritized on further research.

Finally, regarding the avalanche processes, the measurements performed were successful and in agreement with previous research on other materials. Nevertheless, the values obtained for the breakdown voltage ($V_{br} \sim -45$V on average) should be complemented with more measurements within the same samples, and with analysis on devices with different dopping profiles, in order to have a more reliable result and a trend in our data.

ACKNOWLEDGEMENTS

Writing this thesis has been one of the most exciting challenges that I have ever faced in my career. First of all, I would like to thank Lund University for giving me the opportunity to do my thesis in its facilities. When I came to Lund for the first time in January, I was not expecting how much it would change my life. Studying in Lund made me fall in love with physics again, and doing my thesis in the amazing environment that is the NanoLund facilities in the Solid State Division was the icing on top of the cake.

I would like to express my gratitude to Lassana Ouattara, who first welcomed me to the Physics faculty, and Tomas Brage, who encouraged me to continue studying in Lund and opened the doors to do my thesis here.

I also want to thank my supervisor, Magnus Borgström, who welcomed me into the solid State department, helped me to find an exciting project to work in, and besides his busy schedule, always found a moment to meet me when I was having doubts.

A very special thanks goes to my (co)-supervisor, Vishal Jain. Thank you for including me in your research project, for helping me in the laboratory and for being there whenever I needed you, even if it had to be through a Skype meeting. Without your guidance I would never have been able to finish this project.

I would also like to make a special mention to Håkan Pettersson, who welcomed me into the research group from the first day by sharing all of his enthusiasm about his work. In addition, Mohamad Karimi was always there to offer me a helping hand in the lab.

All this would not have been possible without the great work environment that is the Solid State Division. I especially appreciated the Friday meetings that provided me with a great opportunity to have an insight of the on-going projects. It truly was a wonderful way to keep in touch with top research in Nanoscience.

I finally would like to make a special mention to my family and friends. Thanks for your support and for encouraging me during this process.

CONTENTS

ABBREVIATIONS

SC	Semiconductor
PD	Photodetector
RT	Room Temperature
IR	Infrared
IC	Integrated Circuit
CMOS	Complementary-Metal-Oxide-Semiconductor
R&D	Research and Development
NW	Nanowire
SEM	Scanning Electron Microscope
APD	Avalanche Photodetector
SAM	Separate Absorption-Multiplication
VLS	Vapour-Liquid-Solid
LPE	Liquid-Phase Epitaxy
VPE	Vapor-Phase Epitaxy
MOVPE	Metal-Organic Vapor-Phase Epitaxy
EBL	Electron Beam Lithography

1. INTRODUCTION

Photodetectors (PDs) are among the most common devices that integrate our technology nowadays. Their working principle is rather simple; using the photovoltaic effect they can convert a photon flux (also called radiation or optical signal) into an electrical signal. This effect is characteristic of semiconductor materials, where the electrons are bound to the nuclei with a finite energy (higher than in a metal, and lower than in an insulator). If we apply enough energy, through radiation for example, we can excite the atoms and get free electrons which will create a current flow.

Manufacturing photodetectors with the desired characteristics is relatively simple, and since they can be used to detect a wide range of radiation, their applications are unlimited. We can find PDs in devices that automatically open doors or receivers on television remote controls. Photodetectors are also used in fiberoptic connections or present in huge arrays that detect radiation from the other side of the universe. They are also a common element in Integrated Circuits (IC) used in virtually all electronic equipment today.

One of the challenges that researchers face today in this field is the integration of non-silicon-based photodetectors in silicon-based ICs. Photodevices based on Silicon (Si), which would integrate perfectly, are not effective enough, and it has been suggested that the current state-of-the-art Si CMOS technology (Complementary-Metal-Oxide-Semiconductor, a technology used for constructing integrated circuits used in microprocessors, microcontrollers and other digital logic circuits) is approaching the physical lower limit of beneficial scaling[3].

Compound semiconductors have shown to exhibit more efficient light-emission and absorption characteristics among other advantages, and several studies consider them as the future of this technology. But developing another material for IC compatible with this compound semiconductors is not the solution either. Currently the Si industry spends around $45 billion/year for research and development (R&D) and reaching the level achieved in Si-based devices in 50 years is an impossible goal. Therefore, the integration of materials on Si will likely remain the dominant trend in the foreseeable future.

In the last decade, one dimensional or quasi-one dimensional nanostructures (Nanowires) have been researched as potential building block for nanoelectronic

circuits. Nanowires (NWs) can be defined as structures that have a lateral size of the order of tens of nanometers and an unconstrained longitudinal size. One of their advantages is that they can be used to built up semiconductors of different elements, like InP, GaAs, etc. It has been shown that one dimensional or quasi-one dimensional nanostructures offer several potential advantages over their bulk or thin film counterparts, like dense device integration, discrimination of light polarization, large photosensivity, the possibility to integrate functionality within single NW devices and the heterogeneous integration of NWs and substrates of different materials, among others[4].

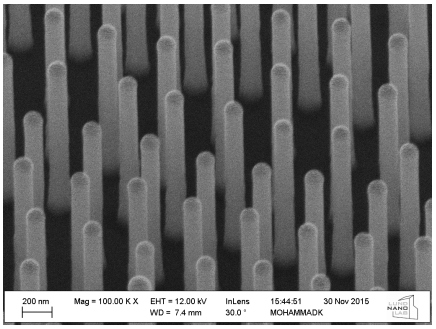

Figure 1.1: SEM[1] image of InP NW array, recorded at 30°.

These unique properties and in particular their easy integration into CMOS compatible substrates would further enhance the integration of this technology in the semiconductor foundries. But in order to reach that objective, a better understanding of the NW photoconductive properties has to be achieved.

This thesis is part of a bigger project, started in the collaboration of Lund University, Halmstad University and Harvard University, that aims to develop and integrate efficient NW-based Avalanche Photodiodes composed of InP (Indium Phosphide) and InAsP (Indium Arsenide Phosphide), which has already been demonstrated in Si-based devices[5].

This work is a continuation of the Master thesis of Lorenzo Bosco[6], where single NWs where fabricated and characterized. In order to complement his data we will analyze the electrical properties of single InP NWs of two different samples. The thesis will be organized as follows:

First, we introduce the theoretical concepts behind the working principles of photodiodes together with a description of Nanowires, some of their principal advantages and their growth techniques. Second, we describe in detail the experimental setup used in this thesis. Finally, we explain the results obtained, without missing the opportunity to discuss them, finishing with a separate chapter with the conclusions reached during this work.

[1]Made by Mohammed Karimi (Division of Solid State Physics, Lund University)

2. THEORETICAL BACKGROUND

2.1 Photodetectors

A photodetector is a semiconductor-based device capable to detect optical signals and convert them into electrical currents. In this thesis, we are going to focus on photodiodes and, more specifically, the ones with internal photoelectric effect, with an increase in photoconductivity due to photon absorption. To understand better their working principles, we will introduce first the basis of the Semiconductor physics, which includes the band theory, an explanation of the notion of doping and the p-n junction. With these concepts we will introduce the photodiode, making a special emphasis on avalanche devices.

2.1.1 Energy Band Theory

To understand the nature of semiconductor material we must go back to the model for the hydrogen atom proposed by the physicist Niels Bohr at the beginning of the twentieth century. In his model, Bohr postulated that the electrons around the nucleus could only lie in one of a fixed number of possible "orbitals", each one corresponding to a specific energy level. The meaning of this energy can be thought as the energy that must be given to the electron in order to separate it from the atom. Although this model is rather simple compared to the real behavior of an electron orbiting an atom, it explains the major scientific observations in this field.

In the case of a crystalline solid, the orbitals described by Bohr are modified. Instead of having a series of discrete energy levels, a solid is characterized by a series of energy bands, separated by an energy gap (See Figure 2.1).

The energy bands have the same basic meaning as the energy levels in the Bohr model; the energy of a particular level is the energy necessary to make the electrons in that level escape from the solid.

In the semiconductor devices, the most important quantity is not the energy required to remove the electrons completely from the material, but rather the energy required to get the electrons to move from an inner energy band to the outermost energy band. This energy is called energy band gap, E_g.

For a pure semiconductor at zero kelvin (0K), all the inner energy bands are fully occupied, and the outer energy bands are completely empty. The highest occupied

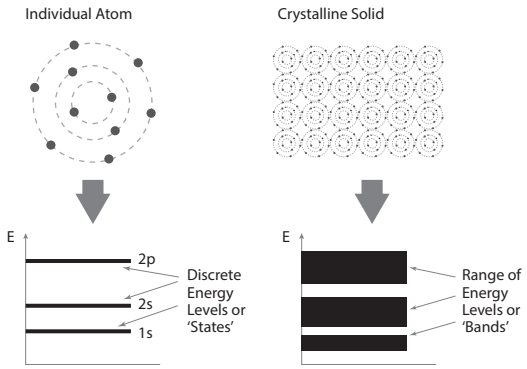

Figure 2.1: Comparison between Bohr model and Energy band model (simplified schema)

band is called Valence band, and the lowest empty band is the Conduction band, and, as we said before, the energy intervalbetween these levels is the energy gap. As we raise the temperature some electrons gain enough thermal energy to occupy the conduction band, but it can still be considered almost empty, that is why it can be described as the outermost partially filled energy band.

Another important parameter for defining a semiconductor is its Fermi level, defined as the energy at which the probability of occupation by an electron is exactly one-half (E_F). The Fermi level helps us to understand the nature of the semiconductor and how it changes upon contact with other semiconductors, for example.

The conduction band is where the electrons contribute to conduction of electric current. This occurs by the movement of the electrons to available (or empty) energy states as the result of the application of an electric field. If a band is full no current can flow. For temperatures higher than 0K there will appear some thermally excited electrons in the conduction band that create empty spaces in the Valence band [1]. These available states in the valence band are called holes. In order to study the current due to the electrons in the valence band it is simpler to consider the movement of these so-called holes, defined as "particles" with a positive charge +e.

The current that flows through the semiconductor is due to the movement of the electrons in the conduction band and the holes in the valence band, so both have to be taken into in account. We will adopt the nomenclature of calling the free electron concentration n and the hole concentration p, both expressed as the number of particles per cubic centimeter.

[1] The temperature at which the electrons can be thermally excited depends on the material and its bandgap.

2.1.2 Doping

One of the biggest advantages of using semiconductor materials is the fact that we can control the number of carriers (i.e. electrons and holes) during the fabrication of the device by a process called doping.

To illustrate the doping process, we can consider a Silicon-based device. Silicon (Si) belongs at the fourth column of the periodic table; therefore it has four valence electrons in the outer shell. In order to generate an excess of free electrons we introduce to the Si lattice an element from column V of the periodic table (like Phosphorus, P), such an element can fit into the crystalline structure giving up its extra fifth electron which will be called a donor (Figure 2.2).

This kind of doping creates an n-type material, because the dominant charge carrier is the electron. For this type of semiconductor, the Fermi level introduced before will be closer to the conduction band (Figure 2.3). This can be understood as the fact that the presence of free electrons in the conduction band is more probable (due to the impurities added).

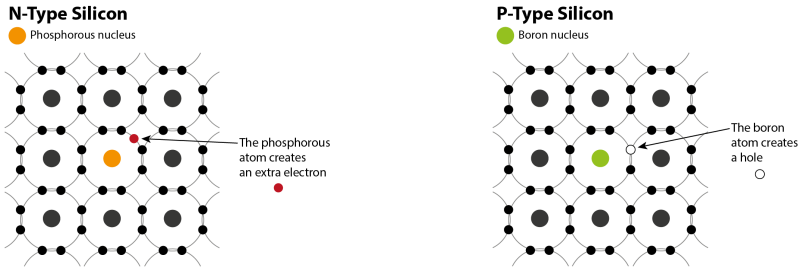

Figure 2.2: Schematic representation of doping process. N-doping, using P as a donor (left) and P-doping, using B as an acceptor (right).

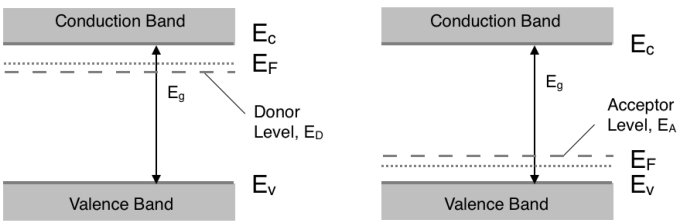

Figure 2.3: Energy bands diagram for an n-type SC (left) and a p-type SC (right). E_c, E_F, and E_v state for the lowest energy level for the Conduction Band, the Fermi energy level and the highest energy level for the Valence Band respectively.

With an analogous process, if we introduce atoms of an element belonging at the third column of the periodic table (like Boron, B) it will only accept three electrons from the Silicon lattice, thus adding a hole (figure 2.2). This kind of element is

called acceptor, and a material doped with it is called a p-type material, because the dominant charge carriers are holes (Figure 2.3).

2.1.3 pn-junction

A pn-junction is the union of two semiconductors with different doping. As the name indicates, one is doped with acceptors (the p-segment) and the other is doped with donors (the n-segment). In this work we will only consider the case of homojunctions, i.e. the same semiconductor material, therefore the energy gap, E_g, will be the same in the whole device.

As we introduced above, before the contact the majority carriers in the p-side are holes, and the main ones in the n-side are electrons. When these two come in contact, electrons close to the contact region on the n-side diffuse to the p-side, and the holes from the p-side to the n-side, leaving behind their ionized impurities (positively charged in the n-side and negatively charged in the p-side) and forming a depletion region. As the impurities are usually fixed in the crystal lattice of the material [2], an electric field is generated in the depletion region due to the charge distribution. This electric field will oppose the diffusion current, I_{diff}, generating a drift current, I_{drift}. The equilibrium is reached when there is no effective current through the device; $I = I_{diff} - I_{drift} = 0$. (Figure 2.4)

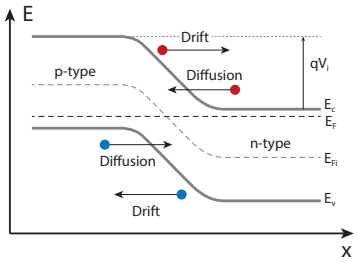

Figure 2.4: Energy bands diagram for a pn-junction. The Fermi level is constant in the whole system, forcing the bands to bend and generating the drift and diffusion currents. The red dots represent electrons and the blue represent holes.

2.1.4 Photodiodes

As stated at the beginning of this chapter, photodiodes are based on the photoelectric effect, which is the transfer of photon energy to an electron of the material. In order to create an electron-hole pair, the incident photon must have an energy ($h\nu$) equal or greater than the energy band gap E_g, so that it can transmit enough energy

[2] Sometimes impurities can move through the crystal lattice, which leads to conduction problems on the device.

to the electron to move from the Valence to the Conduction band (process known as internal photoelectric effect in solid state physics).

Using a p-n junction as a photodetector brings different advantages; the internal electric field reduces the transit time of the carriers inside the material, and, as we will see, applying a reverse bias increases the intensity of this field, making the transit time shorter and also widening the depletion region, which allows to collect more light. The typical structure employed is an p-i-n junction[3], in order to have an even wider depletion region, due to the presence of the intrinsic region.

The typical way to describe the characteristics of a diode is its current-voltage ($I(V)$) behavior (Figure 2.5). As we can see in the Figure 2.6, when a reverse bias is applied to the device, the external field is added to the built-in electric field, making the potential barrier higher. In this case the current rapidly achieves a constant value I_0 called saturation current. On the other hand, when a forward bias is applied to the device, the external electric field counteracts the junction electric field, lowering the effective potential barrier, and the diffusion current increases exponentially with the bias.

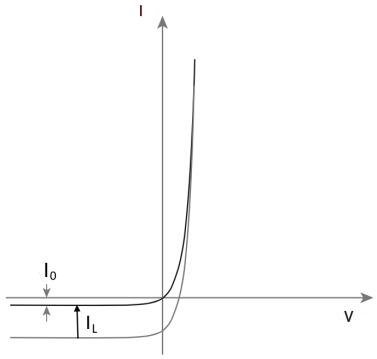

Figure 2.5: Ideal current voltage curve of a pn junction in forward and reverse bias (dark conditions) (black line). It is also included the shift due to the light generated current I_L (gray line).

The theoretical behavior of an ideal diode is given by the relation 2.1, where I_0 is the saturation current, q the charge of the electron, V the external voltage, K_b the Boltzmann constant and T the temperature.

$$I = I_0[e^{(\frac{qV}{k_B T})} - 1] \tag{2.1}$$

The photo response of the pn-junction shifts the I-V curve as sketched in Figure 2.5. Under illumination, an additional light generated current I_L is subtracted:

$$I = I_0[e^{(\frac{qV}{k_B T})} - 1] - I_L \tag{2.2}$$

[3]"i" states for intrinsic semiconductor.

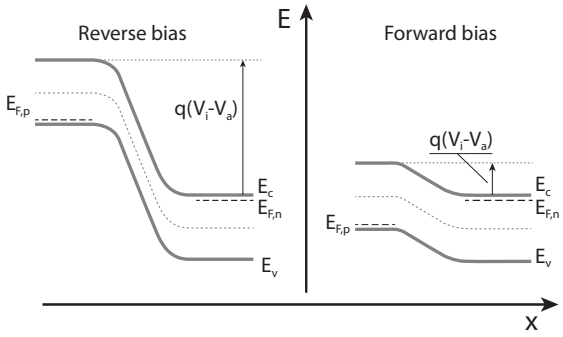

Figure 2.6: Energy bands diagram for a pn junction under reverse and forward bias.

In a real device, several influences have to be taken into account. The relation 2.1 was deduced by making some assumptions, such as the depletion region has abrupt boundaries and the rest of the device is considered neutral, which makes the real current lower than the expected at high forward bias, or that there is neither generation nor recombination of carriers in the depletion region, which makes the current at very low forward bias higher than the ideal one. A more realistic plot of the $I - V$ curve its shown in the Figure 2.7.

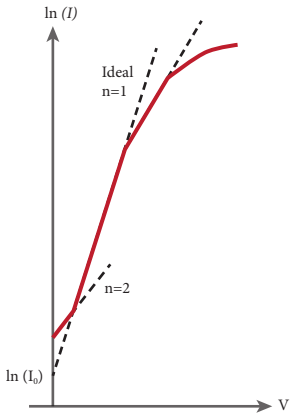

Figure 2.7: Real current voltage curve for a diode (or pn junction) for forward bias. At low voltages the generation-recombination current dominates, and the currents are higher than the ideal ones. At high voltages we can see the high-injection region, followed by the series resistance effect, with lower currents than the expected.

In order to express the ideal-like behavior of a real device and compare between the different configurations, the ideality factor, n, is introduced. It highlights the correspondence between the measured data and the ideal curve. Then the current can be described as:

$$I = I_0[e^{(\frac{qV}{nk_BT})} - 1] \tag{2.3}$$

2.1.4.1 Avalanche Photodiodes (APD)

When a large reverse bias is applied to a Diode, the junction breaks down and conducts a very large current. The process itself is not destructive, but the currents have to be limited to avoid excessive junction heating.

There are two processes that lead to breakdown; tunneling effect and avalanche breakdown. The first one only happens if both the built-in electric field and the doping are very high. This, combined with a high applied bias, allows the electrons in the valence band to penetrate through the energy gap by tunneling, as shown in Figure 2.8a. The avalanche multiplication process is also illustrated in Figure 2.8b.

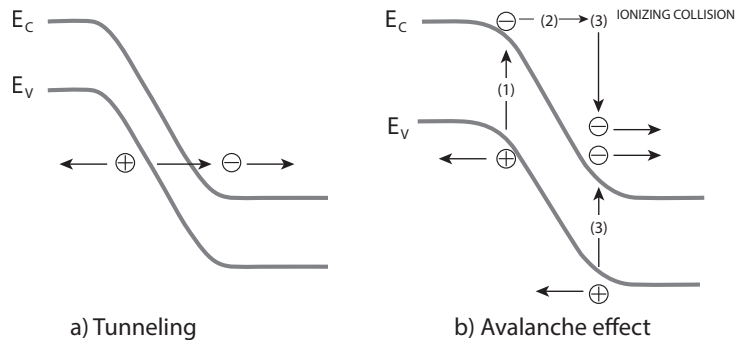

Figure 2.8: Comparison between tunneling and avalanche breakdown.

Figure 2.8 illustrates how a thermally generated electron in the depletion region gains kinetic energy from the built-in electric field. If the field is sufficiently high (but not enough to trigger the tunneling effect), the electron will have enough energy to break the covalent bonds through collision and create an electron-hole pair[4]. This new pair of carriers will also acquire energy from the electric field and continue the process of generating another electron-hole pair every time. This leads to the generation of a cascade of carriers and to an internal gain (i.e the total generated charge in the circuit per photo-carrier pair).

The process is ultimately balanced by the ionization coefficients of the electrons and holes, α_e and α_h. These parameters can be understood as the ionization probability per unit length for each carrier. Their values, in general, are not constant, and depend highly on the electrical field and the temperature of the device[5]. In particular, we expect an increase with the electric field, as more kinetic energy is transferred to the carriers, and a decrease with the temperature, as the collisions with the crystal lattice become more probable.

[4]This process is defined as "ionizing collision" in Figure 2.8 due to the fact that the remaining nuclei after the collision becomes an ionized nucleus.

[5]An empirical formula that shows this dependence can be found in ref [8]

One important consideration in the design of an APD is the need to minimize the avalanche noise, which arises from the random nature of the process. This noise is highly dependent on the ionization coefficients introduced above. In order to characterize the performance of the device we introduce the ionization ratio, k, defined as $k = \alpha_h/\alpha_e$.

The value of k indicates which carrier contributes more to the ionization. If both carriers have similar ionization coefficients, i. e. $k \sim 1$, the avalanche process is unstable, and the noise is maximized because the fluctuation of one carrier represents a large percentual change. On the other hand, when one of the coefficients tends to zero, or both values are contrasting, a fluctuation of one carrier becomes insignificant.

Another way to characterize an avalanche process is through the Multiplication factor, M. It is defined as the ratio between the incident current in the depletion region, I_{n0}, and the final current at the end of the depletion region, $I_{n(W)}$ (Equation 2.4).

$$M = \frac{I_{n(W)}}{I_{n0}} \tag{2.4}$$

The avalanche breakdown voltage, V_{Br}, is the voltage in which the multiplication factor tends to infinity. This condition leads to the following expression [9];

$$V_{Br} = \frac{EW}{2} = \frac{\epsilon E^2}{2qN_B} \tag{2.5}$$

Where E is the electric field in the depletion region, W the length of the depletion region, ϵ the dielectric constant and N_B the ionized background impurity concentration of the light doped side. From 2.5 we can see the proportionality of the breakdown voltage with the depletion region and the electric field.

Separate absorption-multiplication APDs (SAM APDs)

A particular geometrical configuration of a PD worth mentioning is the SAM avalanche photodetector which presents a wide absorption region thanks to the introduction of an intrinsic, or lightly doped, layer that acts as the absorption region, and a thin p-n junction where the multiplication process takes place. Generating and multiplying the photo-carriers in separate regions allow us to have an absorption region with a low-bandgap material and detect long wavelength photons, as infrared radiation, at the same time that we have a high band-gap material in the junction which reduces the dark current and increases the gain.

2.2 Nanowires

The term Nanowire describes a structure with two of its dimensions (the diameter) in the range of 1 to 100 nanometers (10^{-9} m to 10^{-7} m), and the third dimension (the length) typically on the scale of the micrometer (10^{-6} m). The fact that a nanometer corresponds to the length of just a few atoms on a solid, allow us to define Nanowires as quasi-one dimensional structures.

2.2.1 Characteristics

The use of nanowire structures as photodetectors is an emerging research topic; hundreds of papers have been published within the last few years, and it has been shown that one dimensional (or quasi-one dimensional) structures offer several advantages over their bulk counterparts [4]. In this section we are going to describe some of the most relevant ones.

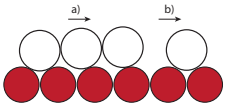

Figure 2.9: Sketch of two materials with different lattice constants. a) more strain is formed until b) dislocations are created [6].

The integration of multiple semiconductors with different physical, electrical and optical characteristics on a single substrate is still a challenge for three and two dimensional structures. This is because a material cannot usually be grown on a substrate with a different lattice constant. This difference leads to strain between the interface, which causes dislocation and defects, as we can see in Figure 2.9. These defects become a high diffusivity path for dopants and non radiative recombination centers, varying the behavior of the device.

In the case of the NWs, this condition is relaxed due to their reduced size. Nanomaterials can be grown on highly lattice-mismatched substrates because their inherent nanoscale geometries enable rapid relief of mismatched strain energy [3]. This fact opens a new horizon on integration of high-performance nano-devices on circuits for electronic and optoelectronic applications.

The optical properties of the NWs are dependent upon the dielectric functions, as in the bulk materials, but additional effects due to their low dimensionality have to be taken into account.

Light polarization dependence of the photoconductivity has been experimentally observed in single NWs of a variety of material systems, as InP [10], p-Si/n-CdS

[6] Strain deformation is thickness dependent, therefore this sketch its only valid for some systems.

[11], and p-i-n Si nano-avalanche photodiodes [12]. Furthermore, enhanced absorption has been observed in closely packed NW arrays; Numeric calculations have shown that Si NW arrays approach total absorption of incident light at small wavelengths [4], which, again, outperforms their bulk counterparts. The surface potential also has a strong impact in suppressing dark currents and enhancing the minority carrier effective recombination lifetime [13], which leads to a significantly increased photoconductivity and an extended diffusion length.

2.2.2 Growth

Numerous techniques exist for producing NWs; still they can be classified in two general groups; the top-down methods and the bottom-up methods. The first ones are based on reducing the size of bulk materials by, mainly, lithographic techniques. These methods have dominated the industry for over the last century, and are still important in the production of electronic components. However, the desired lengths of devices are exponentially decreasing and reaching these scales with a top-down approach becomes more problematic.

Bottom-up methods, on the other hand, mimic nature's way to self assemble atoms in order to form larger structures. It is based on controlled crystallization of materials from vapor or liquid sources, which ends in a highly ordered nanometre-scale structures.

Epitaxy is the general term for the oriented growth of a material on a single crystal surface, with the special characteristic that the system produced will have the same oriented crystal structure as the surface. This technique also allows us to control the length and the composition of the nanostructure, which can even be varied over the length of a nanowire. The diameter can also be controlled by the substrate size, the particle used as a catalyst, or a selectively opened hole in a growth mask.

The first model for explaining one-dimensional crystalline structures was termed the Vapour-Liquid-Solid (VLS) model, in 1964 [15]. From this point, several techniques appeared, mainly distributed in two big groups; Liquid-Phase epitaxy (LPE) and Vapor-Phase epitaxy (VPE). Both of them are based on the same principle introduced in 1964, but using liquid or vapor source, from which the semiconductor material is precipitated forming the nanostructure.

Within the VPE group, one of the most common methods to build III-V semiconductor nanostructures is the Metal-Organic vapor phase epitaxy (MOVPE), which has been used to grow the NWs analyzed in this work. In this case, the semiconductor are not supplied in a gaseous form as pure elements, but they are introduced through precursor molecules that are metallorganic spices [14].

3. EXPERIMENTAL SETUP

3.1 Indium Phosphide nanowire samples

The focus of this thesis is on characterizing single InP NWs with different doping profiles. The NW arrays were grown using VLS through the MOVPE method, introduced in Section 2.2.2, on a p-type InP substrate [1].

After the growth, the NWs were transferred mechanically to a measurement substrate, which will be used to easily contact both ends of the nanowires. The transfer was executed in a clean room using a clean tissue that was first rubbed on the sample, so that it catches the NWs, and then rubbed on the measurement substrate in order to transfer them. This measurement substrate consists of a 3x6mm^2 Silicon chip on which 50 pads have been patterned using UV lithography (25 on the left and 25 on the right) (Figure 3.1a). The pads will be used to contact the tips of the probe station during the measurement. In the space between each two adjacent pads, a total of 24 writefields are defined (Figure 3.1b). Both the pads and the marks that define the writefields are evaporated with gold up to a thickness of 200nm. The last step for the sample consists in a remover bath in Acetone, which is the lift off.

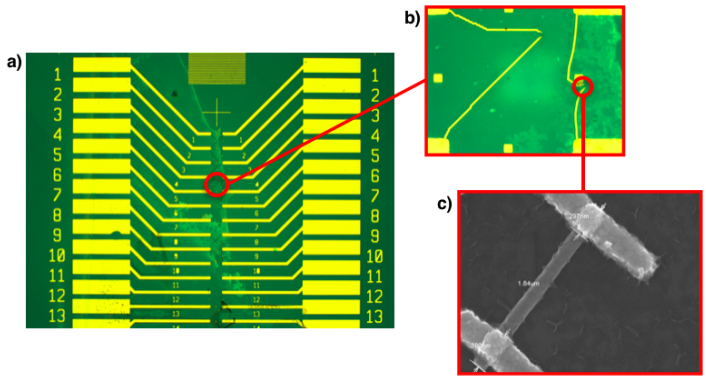

Figure 3.1: a) Optical microscopy image of half of the Si chip used as a measurement substrate. The two columns of gold pads are clearly visible, as the writefields in between. b) Optical microscopy image of the 4th writefield. The contacts from the pads to each NW are visible. c) SEM image of the single NW properly contacted.[2]

[1] For extended technical details check [6]

[2] Both a and b images made by Vishal Jain. Image c made by Mohammad Karimi (Division of Solid State Physics, Lund University)

The contacts that connect the NWs to the pads were first designed with a specific software written in MATLAB and then patterned by Electron Beam Lithography. Finally the metal contact, consisting of a four layers metal junction, was evaporated. The particular arrangement used (based on palladium, zinc and gold) has been specially designed to create an ohmic contact [3] on the p^+ region of the InP.

The samples analyzed had the following size and doping profile (Figure 3.2 and Table 3.1). From now on, they will be referred as Sample A (10421C) and Sample B (10423A). The regions described as p^+ and n^+ correspond to highly doped semiconductors, p- and n-type respectively. n^-, on the other hand, describes a lower level of doping (n-type SC), although the number of free carriers is higher than the intrinsic material.

Figure 3.2: Illustration of the two samples analyzed.

Region	Carrier concentration (cm^{-3}) Sample A	Carrier concentration (cm^{-3}) Sample B
n^+	$> 5 \cdot 10^{18}$	$> 5 \cdot 10^{18}$
i/n^-	$1 - 5 \cdot 10^{15}$	$1 - 5 \cdot 10^{16}$
p^+	$> 5 \cdot 10^{18}$	$> 5 \cdot 10^{18}$

Table 3.1: Doping profiles of the samples[4].

3.2 Probe Station

In order to obtain the I-V curve for each NW we wanted to contact both ends and apply a bias while measuring the resultant current. Due to the size of the samples, we needed a special equipment to perform those measurements.

The equipment used was the so called probe station. Generally, this equipment is used to physically acquire signals of a semiconductor device. The probe station uses manipulators to position precisely its thin needles on the surface of the sample. When the device is stimulated, the signal is acquired by the probe and displayed on an oscilloscope or, in our case, interpreted by a semiconductor characterization system [5].

[3] See section 4.1
[4] This values are estimations based on previous work [21]
[5] Model 4200-SCS Semiconductor Characterization System (www.keithley.com)

In order to perform successful measurements, the device must not experience movements while contacted. To do so, our setup included a vacuum system to keep the sample in place, and the whole equipment was placed on an anti-vibration table (Figure 3.3). We also wanted to avoid any external effect from the humidity of the environment; therefore the measurements were performed under a positive Nitrogen flow. Finally, as we were operating with light-sensitive devices, the sample was placed in a dark chamber, and a microscope was used to visualize the experiment while illuminating the sample when necessary [6].

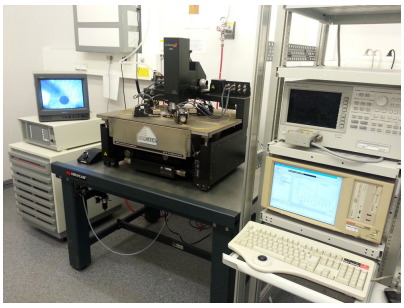

Figure 3.3: Probe Station at Lund University (NanoLund, Solid State Department). From left to right; Temperature controller and microscope screen, Probe Station (on an anti-vibration table), Oscilloscope and Semiconductor Characterization System.

The *I-V* measurements were always first done at dark conditions and then repeated under illumination. Most of the cases a "normal" speed mode was used, because it provides a good combination of speed and low noise. In some cases (especially at low temperatures) the preferred mode was "quiet", which allow us to reach the lowest noise and obtain most accurate measurements. In Figure 3.4 the difference in the “noise level” can be noticed between a measurement performed in normal mode compared to the same one in quiet mode.

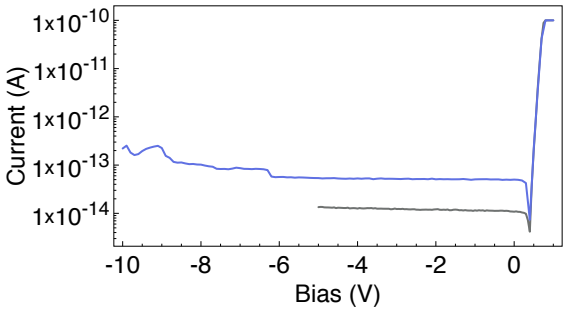

Figure 3.4: Single NW *I-V* curve. Measurements performed at normal mode (blue) and quiet mode (grey). (NW 14r15r, sample A[7])

[6]During all the experiments, the sample was illuminated by all-wavelengths light.

[7]Position of the individual nanowire, the numbers correspond to the pads used to contact it, and the letters to the side; right or left.

4. RESULTS AND DISCUSSION

The final objective of the laboratory work is to determine experimentally the breakdown voltage for two different samples of nanowire-based avalanche photodetectors, as an initial step of determining the dependance of the breakdown voltage with the temperature, and, finally, determine the best doping profile for the desired avalanche photodetector array.

4.1 Contacts

As we introduced before, one of the problems reported in the previous work was the fact that a big percentage of the NWs were not properly contacted [6]. The initial obstacle was that the p-segments on the base of the NWs were too short ($\sim$ 100nm) to be able to contact them properly using EBL. In this study, this problem was overcome by growing NWs with longer p-segments. However p-InP has been reported to show great difficulty in forming ohmic contacts[1]. We therefore fabricated 6 of the NW devices in the sample B such that there are two metal contacts on the p-segment of the NWs (Figure 4.1).

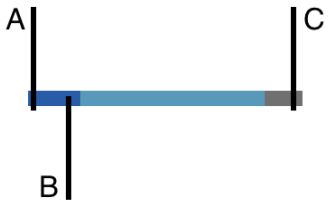

Figure 4.1: Schema of the 3-point-contact connection. The dark blue area (left) represent the p^+-region, the light blue the n^-, and the grey the n^+-region.

To ensure that both A and B contacts were effectively in the p-region we measured the resistance between them applying a small bias. If both were ohmic contacts within the p-region, the resultant resistance must be only due to the resistance of the nanowire.

We calculated the resistance of an InP NW assuming that the SC was degenerate[2] and that we had an ohmic contact. The expression used was $R = \frac{\rho l}{\pi r^2}$, where r represents the radius, l the lenght and ρ the resistivity. ρ can be calculated as

[1]Surface fermi level pinning tends to make contacting more difficult due to band bending [4]
[2]The doping concentration is higher than the corresponding effective density of states.

$\rho = \frac{1}{q\mu_p p}$. In this case the main carriers are holes (p), so the resistivity will depend on the mobility of such carriers; $\mu_p = \frac{\mu_{p_0}}{1+(\frac{N_A}{2\cdot 10^{17}})^{1/2}}$, where μ_{p_0} is the mobility of the holes in the intrinsic material and N_A the number of acceptors [16; 23].

For an InP NW of an approximate radius of 65nm and the length and doping profiles defined before (Figure 3.2), the resistance of the p-region should be $\sim 6.6k\Omega$.

All of the NWs contacted showed a linear dependence of the current to the bias applied, except the 13L14L which was evidently damaged and showed no currents. This dependance corresponds to an ohmic contact, and allow us to determine the experimental value using a linear fit to each curve. The experimental results are summarized in the following table:

1L2L	3L4L	5L6L	9L10L	13L14L	15L16L
50Ω	54Ω	51Ω	63Ω	-	120Ω

Table 4.1: Eperimental values for the resistance between contacts in the p^+ region (Sample B).

The experimental values obtained were several orders of magnitude smaller than the expected value. This could be due to the proximity of the contacts, and the possibility that they were short-circuiting and, therefore, the resistance measured was only due to the probe station tips.

Due to the discrepancy of the experimental values with the expected one, the *I-V* curves were measured for each device, and the results obtained with the edge contacts were compared with the central contact ones. In Figure 4.2, the curves corresponding to the NW that showed a diode-like behavior are plotted. In general we can conclude that the slopes are similar, and the only difference is that the currents through the edge contacts are slightly higher than the central ones.

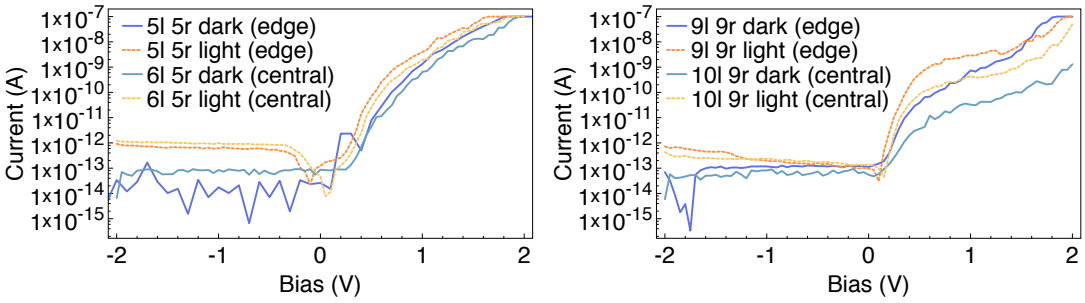

Figure 4.2: *I-V* curves of the 5l-5r/6l-5r NW (left) and 9l-9r/10l-9r NW (right). In both figures the discontinuous yellow curves represent the photocurrents and the solid blue ones, the dark currents.)

Additionally, a Scanning Electron Microscope (SEM) was used to study several contacts of both samples (including the ones studied in this section). It was observed

that the two contacts on the p-segment were indeed short-circuited thus giving the much lower than expected resistance (Figure 4.3).

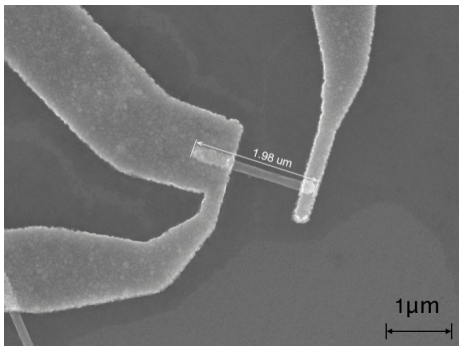

Figure 4.3: SEM imaging of the contact 9l-10l in the p-region (left) and 9r (right) (sample B)[3].

The two possible positions at which a potential barrier may be formed in a NW are the pn junction and the metal-semiconductor interface. In the samples we analyzed, the relevant potential barrier determining the electron transport at reverse bias[4] is formed at the metal interface [18]. Having more data about the nature of this Schottky barrier[5] would help to optimize the contacts and maybe solve the problem we are addressing in this section. Therefore, an experimental analysis of the barrier will be performed (See section 4.2.2.1).

4.2 Individual NWs

The characteristic *I-V* curves are used as a tool to determine the basic parameters of a device and also to compare them to mathematical models. The nanowires studied in this work should present a diode behavior, as the one illustrated in the theoretical background (Figure 2.5). In order to determine their suitability as photodetectors, we applied low biases within the range of -2V to +2V and classified them in three groups based on their ideality factors, the currents reached at forward bias, and the dark currents at reverse bias.

For both types of NWs we could calculate the theoretical electric field, E_{max}, of the i-p^+ junction or the n^--p^+ junction respectively. Also the width of the depletion region, W, and the built-in potential, V_{bi}, can be calculated, just simplifying the problem to a one dimension device and using the expressions 4.1, 4.2, 4.3 [2]. The results for both samples can be found in the Table 4.2.

$$E_{max} = \frac{qn_{p^+}W_p}{\epsilon_o\epsilon_r} \tag{4.1}$$

[3]Made by Mohammed Karimi (Division of Solid State Physics, Lund University)
[4]Voltages higher than $V_{ext} < -3k_BT$
[5]For more details on Schottky barriers in bulk SC and in NW review [1; 2; 18]

$$W = W_{i/n} + W_p = \sqrt{\frac{2\epsilon_o\epsilon_r}{q}\frac{n_{i/n} + n_{p^+}}{n_{i/n} \cdot n_{p^+}}(V_{bi} - V_{ext})} \tag{4.2}$$

$$V_{bi} = \frac{k_B T}{q} ln(\frac{n_{i/n} \cdot n_{p^+}}{{n_i}^2}) \tag{4.3}$$

where n_{p^+}, n_i and n_n are the concentrations of free carriers in the p^+, intrinsic and n^+ regions respectively. W_i, W_n and W_p are the corresponding width of the depletion region in each side of the junction (intrinsic, n-side or p-side). ϵ_0 is the dielectric constant at vacuum and ϵ_r the dielectric constant of the InP [22].

Sample	E_{max} (V/cm)	W (nm)	V_{bi} (V)
A	$1.82 \cdot 10^4$	$1.26 \cdot 10^3$	1.15
B	$5.91 \cdot 10^4$-$1.34 \cdot 10^5$	$4.09 \cdot 10^2$-$1.87 \cdot 10^2$	1.21-1.25

Table 4.2: Theoretical values for both samples at equilibrium.

These calculations have been done at equilibrium conditions, i.e. no external voltage applied. For the case of the Sample B, as the doping of the n-region is a range from 1 to $5 \cdot 10^{16}$ cm^{-3}, the results are also expressed as a range (where the first value corresponds to the lower doping of the n-region, and the second to the higher).

4.2.1 Sample A

In the first group (1) we included the NWs that had an ideality factor lower than 1.5, currents at forward bias higher than 10^{-9}A and low constant dark reverse currents, without fluctuations nor leakage. In the second group (2), the NWs with higher ideality factors were included, which usually correspond to lower forward bias currents (10^{-12}-10^{-10}A). This group also includes the NW that showed high fluctuations, leakage currents at reverse bias and low photocurrents. Finally the third group (3) includes the rest of NW that weren't destroyed and showed a small increment of currents at forward bias. For the following calculations or measurements, only the NW belonging to the first or second group will be considered. In Figure 4.4 we can compare the *I-V* curves for the first and second group.

Of the 38NW contacted on this sample, 7 belonged to the first group ($\sim$ 18%), 6 to the second group ($\sim$ 16%) and 6 to the third group ($\sim$ 16%). These percentages of NWs properly contacted and showing a diode-like behavior is higher than the ones reported previously [6], although 50% of the NWs contacted didn't show any conductance[6]. In this case we considered them either poorly contacted or destroyed during the fabrication/characterization process.

[6]This same percentage of NW destroyed has also been reported on [17]

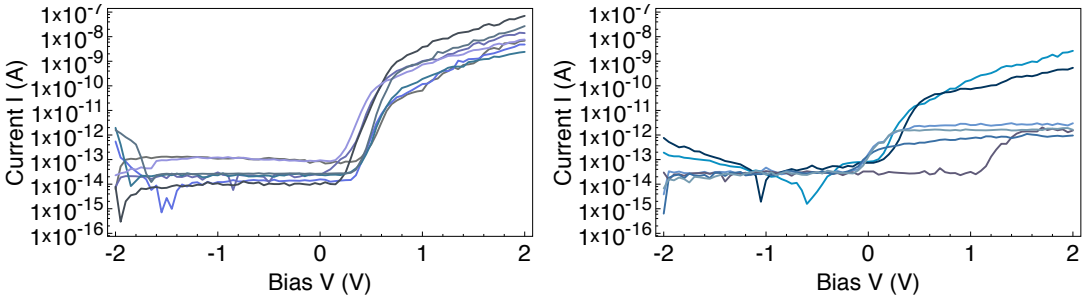

Figure 4.4: I-V curves of the group 1 (left) compared to the I-V curves of the group 2 (right) (sample A). We can notice the lower exponential increase in the second group, as well as the fluctuations and leakage currents (constant increase at reverse bias).

In order to evaluate the ideality factor n of each NW, we rewrite the expression 2.3 as:

$$ln(I) = ln(I_0) + \frac{qV}{nk_BT} \tag{4.4}$$

Which allow us to compare it with the coefficients of an exponential fit to the experimental curves (Figure 4.5). The closer the ideality factor is to 1, the more ideal the measured curve is considered compared to the theoretical one. The experimental values of the ideality factor are displayed in the Appendix A, Table A.1.

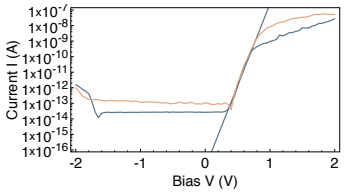

Figure 4.5: I-V dark curve (blue), photocurrents curve (yellow), and exponential regression to determine the ideality factor for the 24r23r NW (Sample A).

The average value obtained $n = 1.2 \pm 0.1$ reflects the quality of the NW analyzed. Although, for a pn-junction at this low voltages, the ideality factor should be closer to 2, due to the presence of recombination processes in the depletion region (see Figure 2.7). In fact, we can consider the ideality factor as a figure of merit that describes the recombination behavior of the device [19]. A device governed purely by diffusion current[7] will have $n = 1$, while a device governed by recombination will have $n = 2$. Therefore, we can say that the currents measured are dominated by diffusion instead of recombination. On the other hand, the ideality factor obtained is in agreement with the presence of the Schottky barrier introduced before. In practical Schottky contacts, the disruption of the crystal lattice at the SC surface

[7]No recombination processes in the depletion region was one of the assumptions made to calculate the ideal diode equation (equation 2.1)

produces a large number of surface energy states that act as a donors or acceptors and, besides of influencing the final barrier height, also affect the recombination processes [2]. For a Schottky junction, there is essentially no recombination in the depletion region, and the ideality factor tends to 1.

4.2.2 Sample B

In this case, in the first group (1) we included the NWs that had an ideality factor lower than 1.5, currents at forward bias higher than 10^{-9}A and low constant dark reverse currents, without fluctuations nor leakage. In the second group (2), the NWs with higher ideality factors were included, which also correspond to lower forward bias currents (10^{-11}-10^{-8}A). This group includes the NW that showed high fluctuations and leakage currents for dark currents at reverse bias. Finally the third group (3) includes the rest of NWs that weren't destroyed and showed a small increment of currents at forward bias.

Of the 32 NWs contacted, 6 belonged to the first group (see Figure 4.6), which represent approximately the 19%, 8 belonged to the second group ($\sim$ 25%) and 10 to the third group ($\sim$ 31%). In this sample, the percentages of contacted NWs are similar to the ones obtained with the analysis of the sample A; consistently higher than the previously reported. The percentage of destroyed/poorly contacted NWs was reduced to 25%.

In Figure 4.6 we can see the *I*-*V* curves for the NW of the group 1 and 2. For this sample the behaviors were not as diverse as for the Sample A, specially considering the currents reached at forward bias and the dark currents at reverse bias.

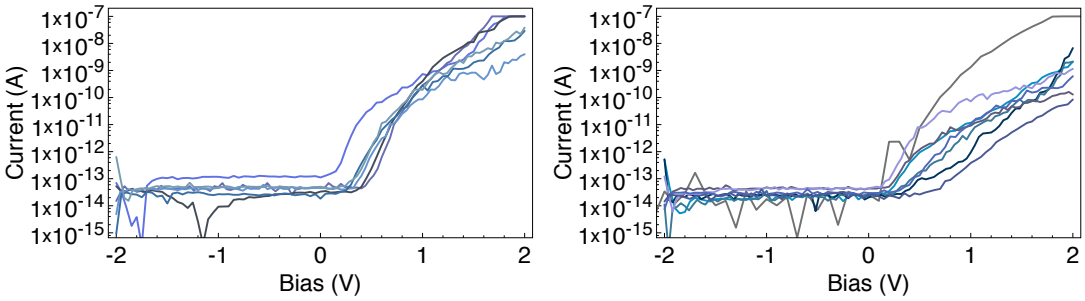

Figure 4.6: *I*-*V* curves of the group 1 (left) compared to the *I*-*V* curves of the group 2 (right) (sample B).

As we did for the first sample, we calculated the experimental values for the ideality factor for the groups 1 and 2, which are summarized in the Appendix A, Table A.2. The average value of $n = 1.53 \pm 0.12$ is higher than in the first sample, so, in this case, the recombination processes are slightly more dominant than in Sample A.

4.2.2.1 Low temperature

For this device, we also measured the I-V curve of the NW belonging to the first and second group at -53^oC (220.15K). The objective of these measurements was to evaluate the potential barrier due to the metal contact in the p^+ region, which can be described through a model based on thermally excited electrons [18] (Expression 4.5, where $\phi(V_{ext})$ is the potential barrier):

$$ln(-I/T^2) \propto -\frac{q\phi(V_{ext})}{k_B T} \tag{4.5}$$

The temperature effects on the potential barrier and the saturation current should also be considered; The lower the temperature, the higher the effective potential barrier (relation 4.3). Therefore, the device will start conducting at higher voltages. The temperature dependence of I_0 relies on its relation with the minority carriers; given that the saturation current is proportional to $e^{(-\frac{E_g}{k_B T})}$ [1] (where E_g is the energy gap and k_B the Boltzmann constant), the lower the temperature, the lower the saturation currents.

The dependence with the temperature could be observed only as a shift in the ideality factor and in the voltage at which the devices start conducting[8] (Figure 4.7). The average value obtained for the ideality factor was $n = 4.27 \pm 0.03$. The shift observed to higher values is in agreement with the one reported in previous research [20]. However, the noise level of our experimental setup made not possible the calculation of the Schottky barrier, which could have been estimated from the Arrhenius plots of temperature dependence of currents at reverse bias [18].

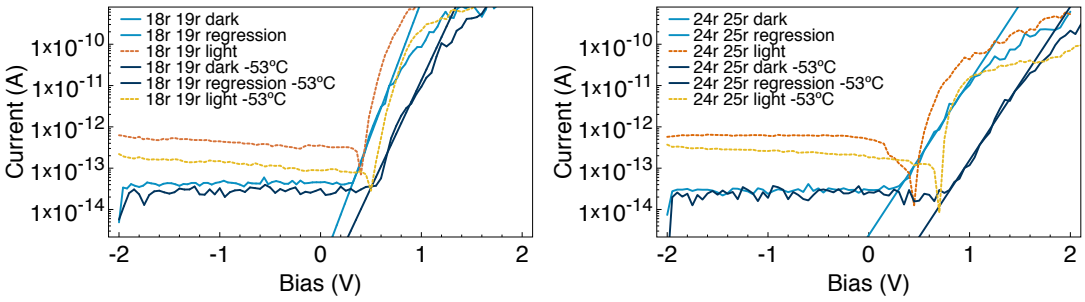

Figure 4.7: I-V curves of two NWs as a comparative between room temperature and -53^oC. Dashed lines represent the I-V curves under light exposure, and solid lines the I-V curves under dark conditions (sample B)

In Figure 4.7 we can see the comparisons of the I-V curve at room temperature and at -53^oC for two of the NWs as an example; the rest of the data are available in Appendix A, Table A.2.

[8]Except for the NW that stop conducting due to external deterioration or during the cooling process (the expanding rate for the measuring substrate is different from the InP, this could lead to unwanted strain and eventually break the structure of the NW).

4.3 Avalanche breakdown

As introduced in the chapter 2, in order to trigger the avalanche process we need to have a rather big electric field in the depletion region, to give the carriers enough energy to ionize atoms in the lattice by direct impact. This electric field should be approximately $2 - 3 \cdot 10^5$ V/cm. Knowing that the field in the junction, E_{max}, depends on the width of the depletion region, W (expression 4.1), and that W depends on the bias applied, V_{ext} (expression 4.2), we can calculate that external bias necessary to trigger the avalanche process. The results for both samples are shown in the following table.

Sample	V_{ext} (V) (reverse bias)
A	$1.4 - 3 \cdot 10^2$
B	$1 - 30$

Table 4.3: Theoretical values for external voltage needed to trigger the avalanche process

To obtain the experimental values for the breakdown voltage, we first measured NWs from group 2 at high reverse bias (starting the measurements from 1V to -5V and increasing the range gradually), in order to obtain a first idea of how each device behaves under these voltages. After that, and knowing an indicative value for the breakdown voltage, we proceed to measure devices form group 1, and calculate also the Multiplication factor in order to quantify the Gain.

4.3.1 Sample A

From the three devices belonging at the second group, only one reached avalanche breakdown at, approximately, -42V (Figure 4.8).

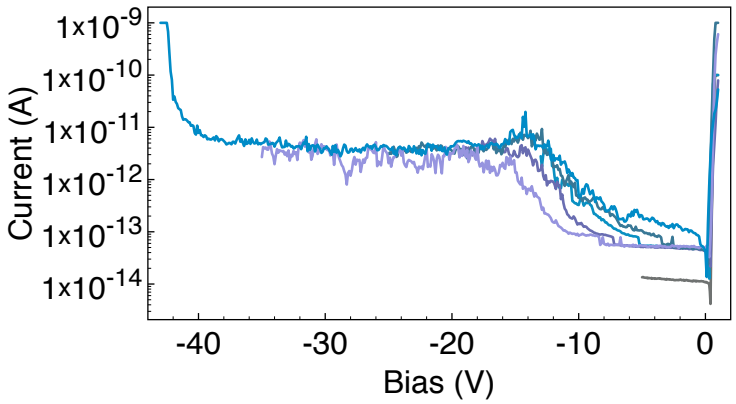

Figure 4.8: Avalanche breakdown for the 14r15r NW (Sample A). Plot of the different dark current measurements until breakdown is reached at approx. -42V.

The high experimental value for the breakdown voltage is consistent with the low value for the built-in electric field, even if it does not agree well with the theoretical value calculated before [9].

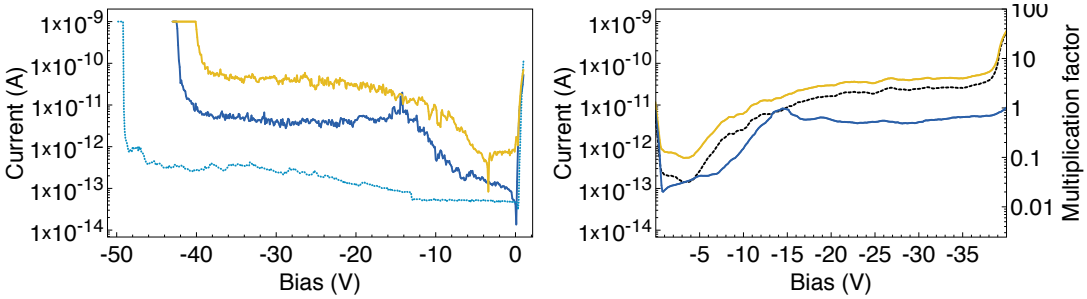

Figure 4.9: Left, avalanche currents, comparison between the first measurement (solid lines, clear color correspond to photocurrent and dark color to dark current measurement. $V_{br} \sim -42V$) and second measurement (discontinuous line, only dark current is plotted. $V_{br} \sim -49V$). Right, Photocurrent (clear line), dark current (dark line), and corresponding multiplication factor (dashed line). Nanowire 14r15r (Sample A).

It can also be seen in Figure 4.8 that the photocurrents are up to ten times larger than the dark currents and increase with the reverse bias. The avalanche gain is quantified by the multiplication factor, defined previously in the photodetectors chapter (equation 2.4). Experimentally, the incident current is obtained from a linear extrapolation of the photocurrent in the bias region from -25 to -35 V, where the curve is nearly flat. The plot obtained (Figure 4.9) shows that this device has a multiplication factor of approximately 30 for sub-breakdown biases, similar to the values obtained for p-i-n Si-based NWs and, moreover, are comparable to multiplication factors for planar devices [5].

Once determined the approximate value for the breakdown voltage, we measured the curves of two NWs belonging to group 1. The results obtained for the breakdown voltage and multiplication factor are in agreement with the ones obtained for this first avalanche measurement (14r15r NW) (Table 4.4 and Figures B.1, B.2 at Appendix B).

	14r15r	l2l11l	12l13l
V_{br} (V)	-42/-49	-45	-49
M	>30	~ 5	>30

Table 4.4: Experimental results for avalanche breakdown voltage and Multiplication factor (sample A).

[9] This discrepancy could be due to different doping concentrations present in the NWs which is difficult to estimate experimentally.

4.3.2 Sample B

For this sample we followed the same procedure as described before. From the two NW measured from the second group, only one showed avalanche currents (Figure 4.10). It is to be noted that, after showing the avalanche currents, the NW stopped conducting. With the SEM we could check that the NW was definitively destroyed (Figure 4.11).

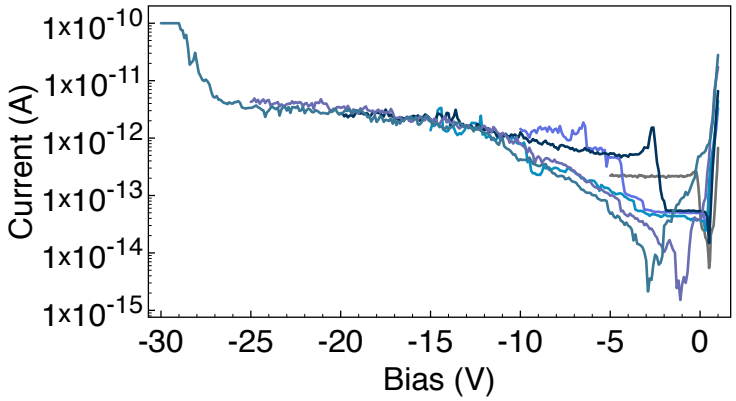

Figure 4.10: Avalanche breakdown for the 9r8r NW (Sample B). Plot of the different dark current measurements until breakdown is reached at approx. -27V.

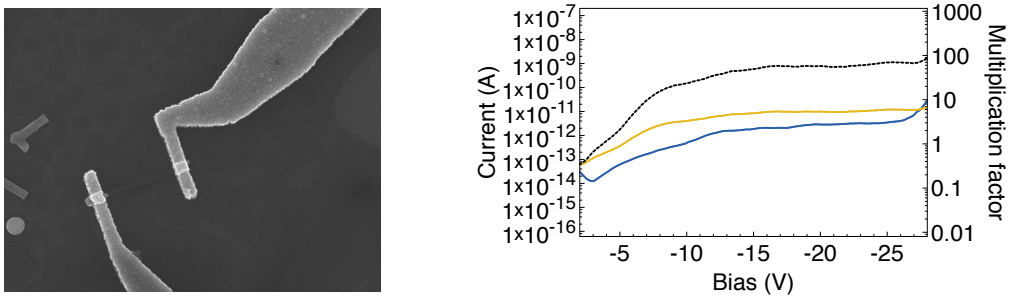

Figure 4.11: Left, SEM imaging of the NW destroyed after the avalanche process. Right, photocurrent (clear solid line), dark current (dark solid line), and the corresponding multiplication factor (dashed line). Nanowire 9r8r (Sample B).

The value obtained for the breakdown voltage (-27V approx.) is in accordance with the values calculated theoretically (Table 4.3). Although, after measuring the *I-V* curve at high reverse bias for other NWs of the same sample, this conclusion seems not that clear.

From the 2 NW measured from group 1, only one showed avalanche breakdown, and at -52V approximately (Figure B.3, AppendixB). Therefore, we must conclude that a deeper study should be addressed in order to complement these data and be able to obtain a more reliable experimental value.

5. OUTLOOK

In this thesis, we had the opportunity to work with two different samples of InP NWs. In general we can conclude that from the 70 NWs contacted, 26 (37% of the total) showed a diode-like behavior, and 16 (23%) showed rectification (conducting only at forward bias). Nevertheless, 28 NWs (40%) did not show any conductance at all. This brings up the first problem addressed in this work, the possible faulty contacting of the NWs.

In previous work, the main problem was that the p-segments were too short to be properly contacted. In this thesis, that problem was overcome by growing NWs with longer p-segments, but the contact was not properly optimized. Therefore we focused on analyzing the Schottky barrier present in the p^+ segment, in order to contribute with our results to the design of a better contact. However, due to the limitations of the experimental setup we could not use our measurements for this purpose. Therefore, we have to conclude that the results obtained do not clarify this problem, and a more complete study should be addressed.

Another important result of this analysis is the value obtained for the ideality factor (1.2 and 1.5). Theoretically, the value expected at these voltages should be 2 or higher, but the presence of a Schottky barrier at the p^+ contact could change this factor closer to 1. Comparing the measurements obtained at lower voltages with the ones realized to measure avalanche processes, we can conclude that the first ones correspond to the Schottky barrier instead of the pn-junction. On the other hand, for higher reverse biases, the *I-V* curves obtained correspond to the pn-junction. Knowing the influence of this barrier to the experimental results force us to assume that, for future research, optimizing the ohmic contact in the p^+-segment of the NW should be a priority.

After comparing the final results of both samples, we can state that the differences expected theoretically were not appreciable experimentally. Both samples, aside from having different doping profiles, presented in average a similar values for ideality factor, dark currents and photocurrents. Even measuring at high biases, we ended up with very similar values for the breakdown voltage in both samples, that makes ourselves ask if the doping profiles described were accurate enough. As in the case of analyzing the contacts, we have to conclude that these results are just a starting point, and more measurements should be conducted in order to have a more reliable

experimental result and a trend on the values obtained.

Finally we should comment on the destruction rate after the measurements. It is important to point out that several NWs were destroyed after applying voltage. That was an expected result in the case of high bias measurements [1], but in our case we have to report that 36% of the NW measured at low temperature (-53^{o}C) didn't conduct current (even if they showed a diode-like behavior at RT). Could this be due to the different expanding rates between the surface and the NWs that lead to their destruction? Or may be just due to external damage? The first SEM images didn't show any evident deterioration. On the other hand, it is known that the sc-metal contact becomes more resistive at low temperatures, could this increase explain our results? This issue is of relevance if we want to continue exploring the characteristics of these devices at different temperatures. Consequently, it should be studied in more detail. On the other hand, unexpectedly, we were able to reproduce avalanche breakdown in two of the devices measured; this fact could open the possibility to measure avalanche in the same NW at different temperatures.

In conclusion, this work can be considered the beginning of a much bigger project. All the results obtained open a new collection of interesting questions to be solved, and set a starting point for further research. Hopefully, the data obtained will work as reference values for improved designs of InAsP NW-based avalanche photodetectors.

[1] Reported previously by [6]

A. APPENDIX: TABLES

Group	NW	n
1	24r23r	0.701
	8l9l	0.723
	12l13l	0.768
	12l11l	0.804
	14l15l	0.882
	16l15l	0.884
	10l11l	0.958
	6l5l	0.961
2	10l9l	1.139
	19r20r	1.639
	14r15r	1.674
	15r16r	1.699
	17r18r	2.286
Average	-	1.163

Table A.1: Table of ideality factors for NW from the groups 1 and 2 (sample A).

Group	NW	n (RT)	n (-53^{o}C)
1	14l15l	0.745	3.494
	16r17r	0.912	1.492
	21r22r	0.985	1.683
	9l9r	1.090	-
	21l20l	1.143	-
	18r19r	1.142	1.907
2	5l5r	1.491	4.320
	5r4r	1.442	-
	9r8r	3.691	6.222
	19r20r	1.517	5.745
	20r21r	1.222	11.562
	24r25r	1.978	2.677
	17l18l	2.459	3.598
Average	-	1.524	4.270

Table A.2: Table of ideality factors, measured at RT and at low temperature, for NW from the groups 1 and 2 (sample B).

B. APPENDIX: FIGURES

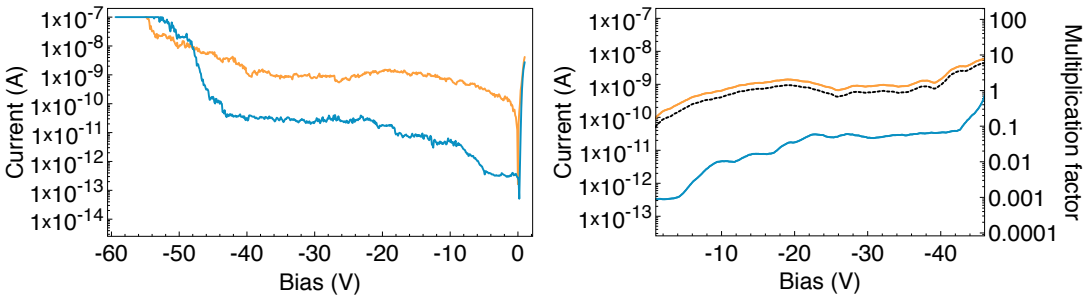

Figure B.1: Nanowire 12l11l (Sample A). Left; I-V curve at high reverse bias (dark current and photocurrent plotted as dark and clear lines respectively). Right; Photocurrent (clear solid line), dark current (dark solid line), and corresponding multiplication factor (dashed line).

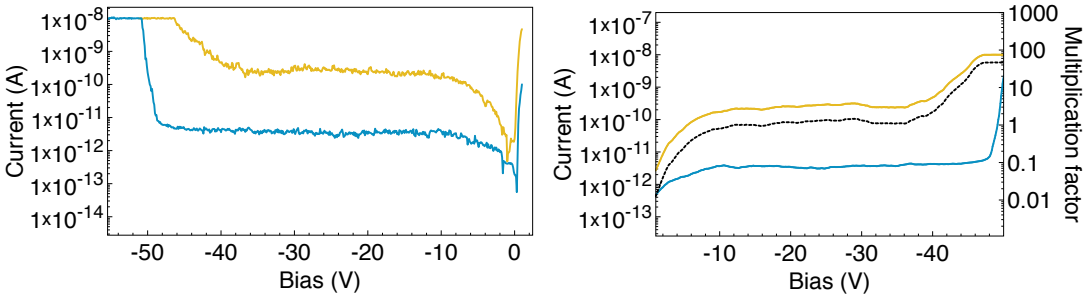

Figure B.2: Nanowire 12l13l (Sample A). Left; I-V curve at high reverse bias (dark current and photocurrent plotted as dark and clear lines respectively). Right; Photocurrent (clear solid line), dark current (dark solid line), and corresponding multiplication factor (dashed line).

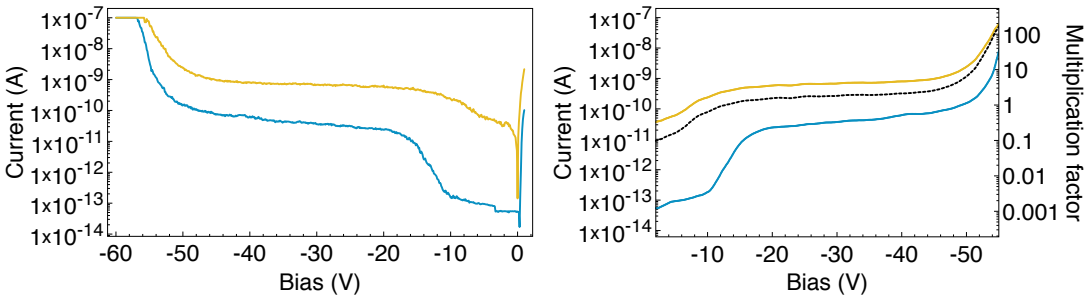

Figure B.3: Nanowire 18r19r (Sample B). Left; I-V curve at high reverse bias (dark current and photocurrent plotted as dark and clear lines respectively). Right; Photocurrent (clear solid line), dark current (dark solid line), and corresponding multiplication factor (dashed line).

REFERENCES

[1] S. M. Sze, K. K. Ng, *Physics of Semiconductor devices*, John Wiley & Sons INC., 2007.

[2] S. M. Sze, M. K.Lee, *Semiconductor Devices*, John Wiley & Sons Singapore Pte. Ltd, 2013.

[3] V. J. Logeeswaran, J. Oh, A. P. Nayak, A. M. Katzenmeyer, K. H. Gilchrist, S. Grego, N. P. Kobayashi, S. Wang, A. A. Talin, N. K. Dhan, and M. S. Islam, "Perspective on Nanowire Photodetectors: Current Status, Future Challenges, and Opportunities", *IEEE J. Sel. Topics Quantum Electron.*, Vol. 17, No. 14, July/August, 2011.

[4] C. Soci, A. Zhang, X. Y. Bao, H. Kim, Y. Lo, and D. Wang, "Nanowire Photodetectors", *J. Nanosci. Nanotechnol.*, Vol. 10, 1-20, 2010.

[5] C. Yang, C. J. Barrelet, F. Capasso, C. M. Lieber, "Single p-type/intrinsic/n-type Silicon Nanowires as Nanoscale Avalanche Photodetectors", *Nano Lett.*, Vol. 6, No. 12, 2929-2934, 2006.

[6] L. Bosco, "Processing and Electrical Characterization of Single Nanowire InP/InAsP APD", Unpublished thesis, Trento: University of Trento, 2014.

[7] D. J. Roulston, *An Introduction to the Physics of Semiconductor Devices*, Oxford University Press Inc., 1999.

[8] F. Zappa, P. Lovati, and A. Lacaita, "Temperature dependence of electron and hole ionization coefficients in InP", presented at the InP and Related Materials conference, Schwabisch-Gmund, 1996.

[9] A.S. Kyuregyan, and S.N. Yurkov, "Room-temperature avalanche breakdown voltages of p-n junctions made of Si, Ge, SiC, GaAs, GaP, and InP", *Sov. Phys. Semicond.*, Vol. 23, No. 10, 1126-1132, 1989.

[10] J. Wang, M. S. Gudiksen, X. Duan, Y. Cui, and C. M. Lieber, "Highly polarized photoluminescence and photodetection from single Indium phosphide nanowires", *Science*, Vol. 293, 1455-1457, 2001.

[11] O. Hayden, R. Agarwal, and C.M. Lieber, "Nanoscale avalanche photodiodes for highly sensitive and spatially resolved photon detection", *Nat. Mater.*, Vol. 5, 352-356, 2006.

[12] C. Yang, C.J. Barrelet, F. Capasso, C.M. Lieber, "Single p-Type/Intrinsic/n-Type Silicon nanowires as nanoscale avalanche photodetectors", *Nano Lett.*, Vol. 6, No. 12, 2929-2934, 2006.

[13] L. Wang, P. Asbeck, "Analysis of Photoelectronic Response in Semiconductor Nanowires", Sixth IEEE Conference on Nanotechnology, Vol. 2, 716-719, 2006.

[14] K. A. Dick, "A review of nanowire growth promoted by alloys and non-alloying elements with emphasis on Au-asisted III-V nanowires", *Progress in crystal growth and characterization of materials*, Vol. 54, 138-173, 2008.

[15] R. S. Wagner, W. C. Ellis, "Vapor-Liquid-Solid Mechanism of Single Crystal Growth", *App. Phys. Lett.*, Vol. 4, No. 5, 1964.

[16] J. D. Wiley, *Semiconductor and Semimetals*, R. K. Willardson and A. C. Beer eds., Academic Press, N.Y., vol. 10, p. 162, 1975.

[17] D.B. Suyatin, C. Thelander, M. T. Björk, I. Maximov and L. Samuelson, "Sulfur passivation for ohmic contact formation to InAs nanowires", *Nanotechnology*, Vol. 18, No. 10, 2007.

[18] D. B. Suyatin, V. Jain, V. A. Nebol'sin, J. Trägårdh, M. E. Messing, J. B. Wagner, O. Persson, R. Timm, A. Mikkelsen, I. Maximov, L. Samuelson, H. Pettersson, "Strong Schottky barrier reduction at Au-catalyst/GaAs-nanowire interfaces by electric dipole formation and Fermi-level unpinning", *Nat. Commun.*, Vol. 5, 2014.

[19] C. J. Novotny, E. T. Yu, and P. K. L. Yu, "InP Nanowire/Polymer Hybrid Photodiode", *Nano Lett.*, Vol. 8, No. 3, p. 775-779, 2008.

[20] V. Jain, A. Nowzari, J. Wallentin, M.T. Borgström, M.E. Messing, D. Asoli, M. Graczyk, B. Witzigmann, F. Capasso, L. Samuelson, H. Pettersson, "Study of photocurrent generation in InP nanowire-based $p^+ - i - n^+$ photodetectors", *Nano Res.*, Vol. 7, No. 4, p. 544-552, 2014.

[21] W. Jesper. E. Martin, W. Reine, S. Lars, B. Magnus, "Electron Trapping in InP Nanowire FETs with Stacking Faults", *Nano Lett.*, Vol. 12, No. 1, p. 151 - 155, 2012.

[22] http://www.ioffe.ru/SVA/NSM/Semicond/InP/basic.html

[23] http://www.ioffe.ru/SVA/NSM/Semicond/InP/electric.html