# Device development for doping evaluation in nanowires using capacitance-voltage measurements

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# 1 Abstract

This thesis aims to show the prospect of capacitance measurements over nanowire arrays as an evaluation method of the p-doping level in weakly p-doped p-n nanowires. The premise of the method is that there will be a high yield of statistical data regarding the doping level of the nanowires. The majority of the work carried out and presented in this thesis is however aimed at the manufacturing of a device suitable for said evaluation, and thus a range of different properties for materials were investigated. Due to early signs of parallel resistance in the device, allowing for an undesirably high back current, the disassociating isolator material as well as radial overgrowth of n-type InP was questioned. The isolating resist *Cyclotene 3044-46* was thoroughly investigated before it was discarded due to its lacking electrical properties. The optional combination of $SiO_2$ and photoresist *S1818* was instead favored, albeit the resulting prolonged processing times. A device was created through various epitaxial, lithographic and etching techniques, creating a device inspired by the design used in nanowire-based solar cells. The design still needs further improvement, in order to eliminate flaws influencing the current through the device. Since the usage of Cyclotene would simplify the design and decrease the manufacturing time, further investigation into the origins of the poor electrical properties is of great interest.

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## 2 Introduction

As technology advanced throughout the 20$^{th}$ century, and into the 21$^{st}$ the importance of semiconductor science became abundantly clear. The ability to scale down transistors allowed for the computer industry to increase the computational power of a chip, and this is what often comes to mind first when talking about semiconductors and their influence on technology. In accordance with Moore's Law, the number of transistors has steadily been increasing, pushing to unlock the potential of semiconductors. In addition it also unlocked the potential of several other fields, e.g. solar cells, light emitting diodes (LED), and a diverse range of sensors. These are devices that are integrated and essential for the growth of modern technology. As research is carried out to improve or develop new technology, the demand for innovation grows. However, that is not to imply that there is a stagnation of semiconductor science, as new findings are being brought to light regulary. As recently as 2014 the Nobel Price in Physics was bestowed upon Isamu Akasaki, Hiroshi Amano and Shuji Nakamura for inventing the blue LED.

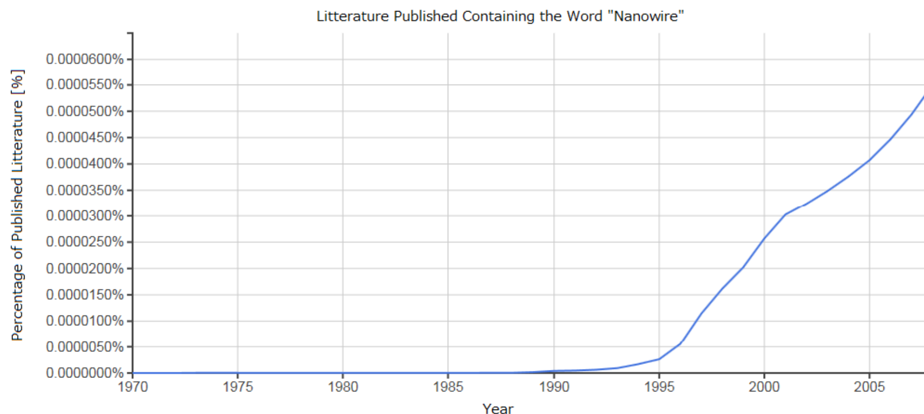



Figure 1: 'ngram' depicting the increase in occurance of the word "nanowire" in literature[9]

A promising field of study is that concerning nanowires. Showing many unique properties, the prospect of nanowires has attracted much attention in recent years. This can be inferred through observing the increase of the word "Nanowire" in literature. As displayed in figure 1 it is evident to the observer that the interest for nanowires is increasing. This attention

is not without cause, and electrical devices such as resonant tunneling diodes (RTDs)[1], single electron transistors (SETs)[2], and LEDs[3] have been demonstrated in NWs. The ability to engineer well-ordered arrays of nanowires[4], as well as to control the axial and radial growth[5] allows for highly optimized designs. If optimized, an InP nanowire array with a wire length of 2 μm is predicted to absorb more than 90% of the light above the InP bandgap[6]. Investigations concerning properties of nanowires have thus proven promising.

In order to achieve desired electrical properties impurities are often introduced into the semiconductor, i.e. doping. While doping is generally done in order to alter the conductivity of the semiconductor[8], it has also been demonstrated to affect growth of nanowires[7]. LEDs can be realized with nanowires by changing doping species during growth, resulting in an n-type doping area, and a p-type doping area[3]. In the presence of a forward bias, this allows for radiative recombination, i.e. injection electroluminescence, at the junction region[8]. As the electrical properties of the semiconductor heavily rely on the introduced dopant, there is a value in monitoring the growth process, thus allowing for the growth parameters corresponding to the desired properties of a nanowire to be determined.

The knowledge concering doping of nanowires is closely related to the strength of the evaluation techniques used. During the development of nanowire fabrication various evaluation techniques have been shown capable of evaluating the doping[7]. However, due to the limitations of the system (the nanowire), and/or the evaluation techniques, all methods are faced with complications, which have to be taken into account during processing. When considering what evaluation technique to use, aspects such as simplicity of the technique and time constraints of the process are often the deciding factor. Optical methods are thus attractive, as they usually require no further processing, and are generally faster than electrical measurements. One such optical technique is to observe the so-called Burstein-Moss shift during photoluminescence (PL). The PL spectra will be blue-shifted as dopant concentration increases. The method has been demonstrated to give accurate results on doping in bulk[10], as well as for nanowires[11]. Although the method carries over from bulk to nanowires, it is limited to evaluation of high doping concentrations and incapable to deliver a qualitative profile of the nanowires. In addition, as the blue-shifting is observed a broadening of the peak is also observed, thus rendering measurements harder to interpret.

Raman spectroscopy is another commonly employed optical method used for doping evaluation of semiconductors, and has also been used

to characterize nanowires[12]. The method is well suited for qualitative measurements, but in order to extract quantitative information a continuous measurement of the nanowire is needed. As this is both time consuming and only provide information on a single nanowire, other methods are preferred for quantitative analysis.

In contrast to the optical methods, electrical techniques and methods utilizing spatial measurements are also available for characterization. Spatial measurement techniques are seldom desired outside of academic environments due to being extremely time consuming. Electrical techniques are however widely used, as they often can deliver information regarding the device under working conditions. The most commonly used method for quantitative characterization of doping in a nanowires is to create a so-called *nanowire field-effect transistor* (NW-FET) device[13]. The FET can be made by using a substrate with an oxide grown on top of it (e.g. Si and $SiO_2$) as the gate and isolating oxide layer, the nanowire is then placed on top of the oxide and contacted on each side, where by the contacts will act as source and drain and the nanowire as the transport channel [38]. By sweeping the source-drain voltage it is possible to determine the conductivity of the nanowire, and therefor the carrier concentration (directly related to the doping) can be determined[7]. This technique is generally only limited by extensive need of processing, resulting in a very time consuming process.

Evaluation of doping using the well-known Hall-effect, while having been proven possible[14], is not commonly used due to it sharing a similar necessity for processing as the NW-FET, and is further constrained by the physical size of the system. It is clear that an evaluation method unlimited by processing time or the physical size of the system would be beneficial to the semiconductor industry. One promising technique is that of CV-measurements on an array of vertically grown nanowires. The promising prospect of the technique was displayed in 1991[3], but has since been generally left uninvestigated. In 2014 attempts to develop a device capable of doping evaluation using said method was carried out[15], producing promising results. This method would demand less processing, and would be capable of delivering high statistical, quantitative characterization of nanowires.

Following previous research[15], attempts at processing a functional device, capable of doping evaluation in nanowires through CV measurements was carried out. The work will be explained during the length of this report.

The report consists of an initial part (3) describing the underlying theory used in order to attempt the doping evaluation of the nanowires. Although the processing and measurements were carried out in parallel these

processes will be split up in a second part presenting the methodology throughout this project (4), followed up by the results (5) obtained through measurements on the devices described in section 4. Lastly ideas for further research on the subject (6), as well as a summary (7) of the project is presented.

# 3 Background

To support the idea of CV-measurements as a possible evaluation method for doping in nanowires, a brief explanation of a p-n junction in a nanowire and its features will first be given. As the properties of the p-n junction are made clear an attempt will be made to evaluate the doping with a parallel plate capacitor approximation, allowing for an uncomplicated method.

## 3.1 Epitaxy of Nanowires

To understand how a p-n junction in a nanowire is realized it is necessary to explain the growth process of a nanowire. When talking about nanowire manufacturing, there are two different approaches that are conducted in order to achieve the desired structure. The first method is the so-called top-down approach, where the structure is etched out from bulk[16]. The other is known as the bottom-up approach, where nanowires are grown using epitaxial methods. Using these methods it has been shown possible to grow nanowires on a substrate[3] as well as in an aerosol[17] enviroment. Throughout this project, nanowires were grown on substrate using the the second approach, and this section will thus be dedicated to summarizing the process flow.

In a bottom-up approach, the nanowires are generally grown from seed particles that are deposited on the substrate before the growth process. Au as a seed particle is one of the most studied form of catalyst for nanowire growth, and the conditions of the seed particles can affect the growth considerably. The growth process exhibits highly similar behaviour between different deposition methods (e.g. electrospray method, Electron Beam Lithography-defined or aerosol gold particles generated by evaporation), but the particles are rather sensitive to nanowire incubation time and annealing[18], greatly effecting nanowire growth.

As the position of the particle will determine the position of the finalized nanowire, both the actual properties of the particle, as well as the deposition location of the particle will have to be taken into consideration. Several techniques to generate and deposit seed particles are available, including aerosol carried particles generated through spark discharge, as well as colloid particles spun on to the target substrate[18]. As metal precursor particles are guided towards the substrate by a gas, and spun colloid particles are deposited in a random fashion on top of the substrate, a control mechanism is vital in order to achieve organized structures. For their ability to guide the deposition with high precision, *Electron Beam Lithog-*

*raphy* (EBL)[20] and *Nano Imprint Lithography* (NIL)[4, 6] are favoured for nanowire growth. NIL comes with the advantage of higher throughput, but with a lower precision than that of EBL. As NIL was the method used in this project it will be described in further detail.

The promising results for the technique known as NIL were demonstrated in 1996[21], as a resolution of 25 nm for imprint lithography was achieved. In imprint lithography a mould with thickness contrast features are pressed into a resist, and a mirrored structure is formed in the resist. During the moulding step the resist is generally heated, as low viscosity promotes the conforming of the resist. Finally, unwanted resist between the finally sought features are removed, this through anisotropic etching (fig. 2). The mould is generally made with slower methods such as EBL defined areas etched by *Reactive Ion Etch* (RIE), which is known to be a time consuming process. Since the mould used to imprint the structures into the resist can be rendered unusable for further processing by resist sticking to it after the moulding, a master is often created, mimicking the finally desired structure. A second mold used for the imprint is then patterned by the master, increasing the life-time of e.g. the EBL defined mould (the master). An anti-sticking coating is also often applied to the mask to further diminish the possibility of resist being torn of the sample as the mould is removed[36]. The method can imprint a large area[21] with high resolution, and is thus as previously stated favoured for high throughput.

When defining the position of the nanowires with NIL, the pattern transferred by the mould will create holes in the resist residing on the substrate. The patterning is then followed by e.g. metal evaporation[4], that will result in the sought after seed particles as the resist is lifted off.

Although the crucial role of each seed particles' position has been stated, the process promoted by the particle is yet to be discussed, and this process is to validate the part the position plays during growth. After seed particle deposition, the method of interest used to grow the nanowires is *Metal Organic Vapor Phase Epitaxy* (MOVPE). This epitaxial method utilizes a carrier gas to transport the constituent elements (in gas phase) to the vapour-solid interface. The gaseous species then dissociate/pyrolyse at the heated growth area, thereby releasing the elements intended for growth. The metalorganic sources are generally stored in bubblers, and at a set pressure the liquid creates an equilibrium vapour pressure, allowing the carrier gas to be saturated with precursor molecules, which are then carried away to the growth chamber, also known as the reactor. The growth process is then governed by three major factors; adsorption, growth and desorption. The elements are adsorbed onto the growth area, were they induce growth.

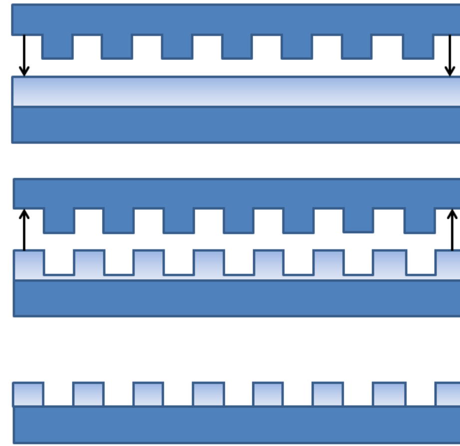


Figure 2: Flow chart of a general NIL process. The mould is first pressed into the thermoplastic. The mould is then removed, and anisotropic etching is used to expose the underlying substrate.

Excess reaction products are then desorbed from the growth area[22].

In the case of a nanowire, the growth is as previously stated locally catalysed by the metal seed particle[23]. As the seed particle saturates it will cause nucleation at the base, forming a crystal layer. The nanowires are as noticed fabricated through a VLS mechanism, and the process needs to be carried out at a high temperature so the seed particle can form a liquid alloy. It has been shown that the continiuous growth at the collector-crystal interface is favourable in comparison to new growth at other interfaces of the collector/seed particle[24], as well as the side facets of the wire. Although not favoured, side growth is a factor that needs to be taken in to consideration when growing nanowires, as it can result in radial overgrowth, rendering the nanowire unusable for the intended purpose. In order to avoid side growth *in situ* etching is performed[5], for InP nanowires (used in this project) HCl is usually used as the etching agent. In the case of InP nanowires the reaction, if simplified, is as follows[15, 35]:

$$In(CH_3)_3 + PH_3 \rightarrow InP + 3CH_4 \quad (1)$$

The small dimensions of the nanowires also allows for different materials to be grown on top of each other to a larger extent then for a bulk system. For example, for a planar structure attempts at growing different materials

on top of each other would cause defects at the junction due to different lattice constants. However, as the junction interface in a nanowire is small the lattice mismatch will not be enough to cause strain or defects[26]. The ability to grow different materials with very well defined interfaces opens up for interesting structures for e.g. photonics, and instinctively we can see that if it holds for different materials the growth process should allow us to grow differently doped regions on top of each other[7], thus enabling structures such as the p-n junction to be created.

### 3.2 Band Structure

As semiconductors in general are poor conductors impurities are often introduced to promote electrical current in the material[8].The source of the poor conductance is that there is a clearly defined bandgap between the valance band and the conductance band. In order for electrons to contribute to a current it is necessary that they are excited to the conduction band. In metals the valence band and the conductance band overlap, allowing for conductance. In semiconductors there is a separation that electrons, given enough excitation energy, can be excited over. Although the bandgap is smaller than that of an insulator, the thermal energy at room temperature is generally not enough to maintain a sufficient electron concentration in the conduction band. During excitation the electron overcomes the energy barrier, moving into the conductance band, leaving a vacancy in the valance band, e.g. a hole. Said holes behave as positively charged particles, and contribute to conductivity.

As previously stated, impurities are usually introduced to promote conductivity. There are two different doping types: the introduction of an energy state close to the conduction band called n-type doping, and an energy state close to the valance band called p-type doping. In order to create an n-type doping profile in the semiconductor impurities with an excess valence electron are introduced. This creates a filled energy state close to the semiconductor's conduction band, and electrons can with conciderably less energy (than the energy needed to be exited from the valance band) be exited to the conduction band, increasing conductivity in the semiconductor. The opposite type of doping is p-type. A p-type doping profile is created by introducing dopants with a shortage of a valence electron, and this will create an energy state close to the edge of the semiconductor's valance band. As the introduced energy states are close in energy to the edge of the valance band (thermal energy allows for excitation), this allows for electrons to be excited from the valance band to the vacant energy states.

As the electrons are excited they become bound, unable to contribute to any current. However, simultaneously they create holes, which as previously mentioned can contribute to conductance. The effect of doping on a material is illustrated in figure 3.

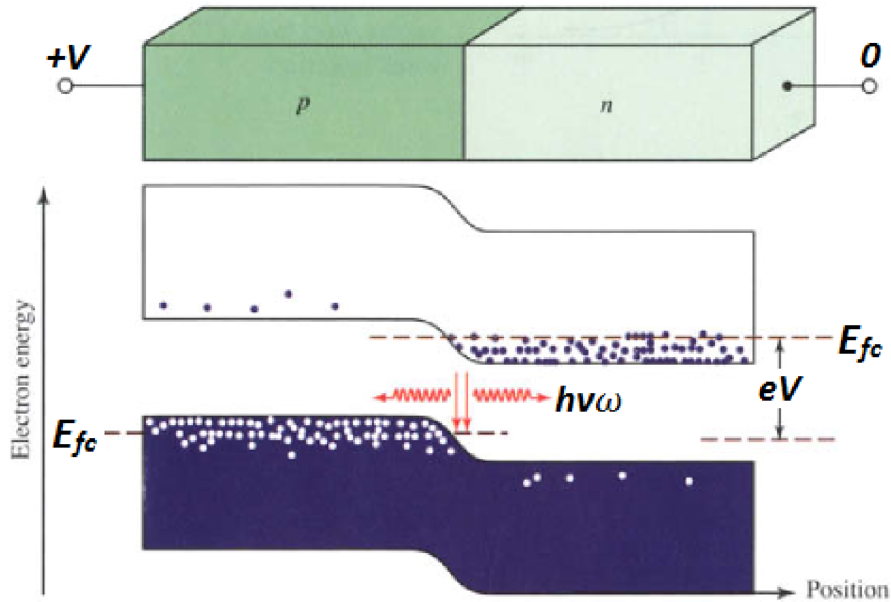



Figure 3: Energy-band diagram of a p-n junction with a forwarded bias, as a result of applied voltage. The blue dots in the conduction band signify electrons, while the white dots signify holes. The figure was adapted from [8].

As can be seen in figure 3, the Fermi level's offset is determined by the doping profile. As the Fermi level guarantees charge neutrality/marks half occupation, n-doping forces the Fermi level up against the conduction band, while p-doping forces the Fermi level down towards the valance band. As two materials are connected the band structure at the interface bends as to maintain a constant Fermi level in the material [28], thus maintaining charge neutrality through the sample. The bending of the bands can be seen in figure 3 (under a bias $V$), where a so called p-n junction has been formed between a p-type and an n-type doped semiconductor.

As the Fermi level of a metal is located in the conduction band, merging a semiconductor interface with a metal may cause the band structure of

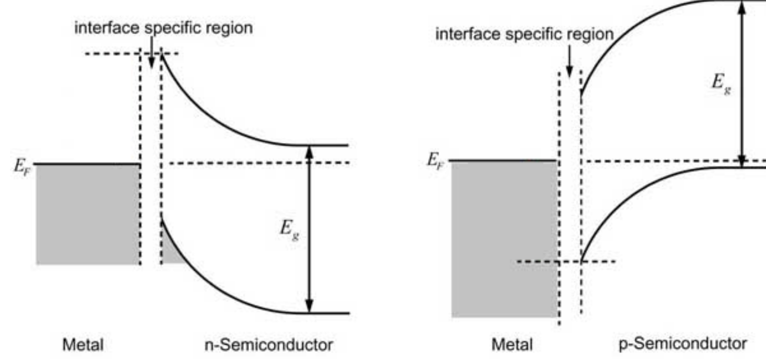



Figure 4: Illustration of the bending of the conduction and valence band as a semiconductor is merged with a metal. The image is an altered version of an image available at [40].

the semiconductor to bend towards higher energy (Fig. 4)[29]. This is especially prominent in semiconductors with a p-type doping profile. This bending will render electrons occupying the lower levels of the conduction band unable to move past the junction. This barrier is called a Schottky barrier and can cause trouble when attempting to make a contact to a semiconductor[25, 30]. The thickness of the barrier $d$ is given by equation 2, were $e$ is the electron charge, $N_D$ is the number of introduced dopants, $V_b$ is the applied bias (in eV), and the permittivity is denoted by $\epsilon_0$ and $\epsilon_b$:

$$V_b = \frac{e^2 N_D d^2}{2\epsilon_0 \epsilon_b} \tag{2}$$

For small $d$ electrons can tunnel through the barrier with a probability $T$ (Eq. 3), where $m$ is the carrier mass, and $\hbar$ is Planck's constant:

$$T \approx exp[-\left(\frac{2mV_b}{\hbar^2}\right)^{1/2} d] \tag{3}$$

This allows for a current to pass through the junction. Thus heavily doped semiconductors can form ohmic contacts with metals. For the purpose of this project InP nanowires were used, a material which has shown difficulties in forming an ohmic contact between metals and p-type InP[25].

### 3.3 The p-n Junction

As a p-type and an n-type material are brought together, carriers (electrons and holes) will start to diffuse to areas with lower concentration; i.e. electrons will diffuse into the p-region, and holes into the n-region. As the electrons diffuse they leave positively charged ions behind, and holes will leave negatively charged ions. Electrons will recombine with holes in the p-region, and holes with electrons in the n-region, as they are abundant. The build-up of charge in the junction area, due to the presence of ions, will eventually block further diffusion over the junction, resulting in an area around the junction nearly depleted of mobile charge carriers[32] known as the *depletion layer*.

The space charge distribution and electrostatic potential $\psi$ of the p-n junction can be described by the Poisson's equation[33]:

$$\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} \equiv -\frac{\mathrm{d}E}{\mathrm{d}x} = -\frac{q}{\varepsilon_s}\left(N_D - N_A + p - n\right) \tag{4}$$

As can be seen the electric field $E$ is determined by the acceptor- $N_A$ and donor-impurity density $N_D$, and the density of free holes $p$ and electrons $n$, with $q$ and $\varepsilon_s$ being the electron charge and the semiconductor's permittivity constant. Local charge neutrality is maintained when:

$$\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} = 0 \tag{5}$$

as such

$$N_D - N_A + p - n = 0 \tag{6}$$

As the junction becomes depleted of mobile charge carriers, $p = n = 0$, and equation 4 becomes reduced to:

$$\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} = \frac{q}{\varepsilon_s}\left(N_A - N_D\right) \tag{7}$$

If the depletion layer is divided into two parts, the space charge distribution (Eq. 7) can also be divided in two parts (Fig. 5): one for the p-side, and one for the n-side.

$$\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} = \frac{qN_A}{\varepsilon_s}, -x_p \leq x < 0 \tag{8}$$

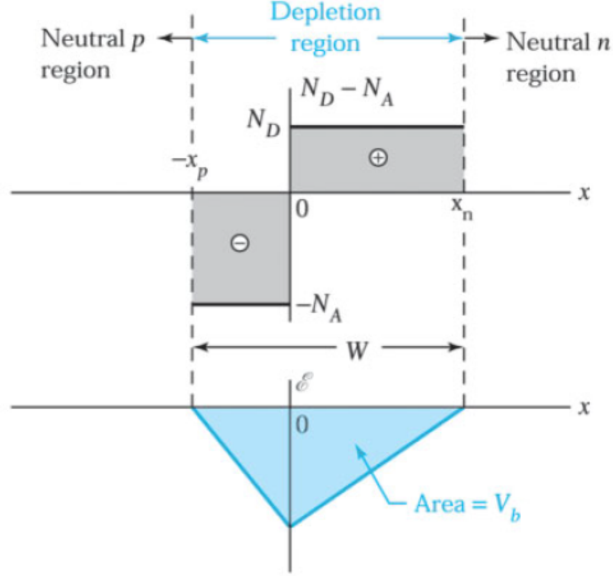



Figure 5: Space charge distribution and electric-field distribution in the depletion region at thermal equilibrium[33].

$$\frac{d^2\psi}{dx^2} = -\frac{qN_D}{\varepsilon_s}, 0 < x \leq x_n \tag{9}$$

The overall space charge neutrality of the semiconductor requires that the total negative space charge per unit area in the p-side equals the total positive charge per unit area in the n-side. Assuming a 1D uniform structure along the e.g. x-axis results in:

$$N_A x_p = N_D x_n \tag{10}$$

The total depletion layer width $W$ (Fig. 5) is given by:

$$W = x_p + x_n \tag{11}$$

The electric field over the depletion layer is obtained by integrating over the electrostatic potential (Eq. 4), and utilizing equations 8 and 9 give:

$$E(x) = -\frac{qN_A}{\varepsilon_s}\left(x + x_p\right), -x_p \leq x < 0 \tag{12}$$

$$E(x) = \frac{qN_D}{\varepsilon_s}\left(x - x_n\right), 0 < x \leq x_n \tag{13}$$

The total electrostatic potential difference between the p-side and the n-side neutral regions at thermal equilibrium is called the *built-in potential* $V_b$, and can be obtained by integrating over the electric field (Eqs. 12 and 13) in the depletion area:

$$V_b = \int E(x)\mathrm{d}x = \frac{1}{2}E(0)W \tag{14}$$

By combining equation 10 through 14, the depletion layer width as a function of built-in potential is obtained:

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)V_b} \tag{15}$$

If a bias $V_a$ is applied over the junction (in the fashion of a positive voltage at the p-side in respect to the n-side), the junction becomes forward-biased, and the electrostatic potential decreases by $V_a$. A change in electrostatic potential naturally effects the width of the depletion region, and as the total electrostatic potential $V_b$ is replaced by $V_b - V_a$, the width of the depletion area becomes:

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_b - V_a)} \tag{16}$$

As the depletion layer separates the neutral p- and n-side, ions at the interfaces causes charge separation, and the p-n junction effectively acts as a capacitor, where the junction depletion layer capacitance per unit area $C_j$ can be defined as[33]:

$$C_j = \frac{\mathrm{d}Q}{\mathrm{d}V} \tag{17}$$

Here $\mathrm{d}Q$ is the incremental change in depletion layer charge per unit area for an incremental change in the applied voltage $\mathrm{d}V$. The amount of change in charge distribution due to an applied voltage can be approximated to be $\mathrm{d}V = W\mathrm{d}Q/\varepsilon_s$, and equation 17 can be rewritten as:

$$C_j = \frac{\varepsilon_s}{W} \tag{18}$$

The attentive reader can now see the connection to the parallel plate capacitor $C = \epsilon A/d$, where $A$ is the area of the parallel capacitor, $d$ is the distance between the plates, and $\epsilon$ is the dielectric constant. The model of a parallel plate capacitor is only true as long as edge effects can be neglected ($R \gg d$, where $R$ is the radius of the plates). In the case of a small $R$ more complex numerical models have to be used to solve for the capacitance[34]. Assuming the model of a parallel plate capacitor $d = W$, and $C_j = C/A$.

By combining equations 16 and 18, the capacitance per unit area as a function of applied voltage can be expressed as:

$$\frac{1}{C_j^2} = \frac{2(V_b - V_a)}{q\varepsilon_s}\frac{N_A + N_D}{N_A N_D} \tag{19}$$

Naturally this only holds when the doping levels are constant in the two doped materials.

## 3.4 Doping Evaluation

As the goal of this project is to develop a method to determine the doping level of weakly p-doped material, further explanation regarding the correlation between capacitance (3.2) and doping levels is necessary. If equation 19 is analysed, a linear relation between $1/C_j^2$ and $V_a$ can be observed. However, it is also evident that the depletion layer capacitance per unit area also has a strong relation to the doping levels in the materials ($N_A + N_D/N_A N_D$). Under the assumption of $N_A \ll N_D$, equation 19 can be rewritten as:

$$\frac{1}{C_j^2} \approx \frac{2(V_b - V_a)}{q\varepsilon_s N_A} \tag{20}$$

From 20 it is evident that only the doping level in the low-doped side can be evaluated. In order to evaluate the doping level, a capacitance-voltage measurement would need to be conducted, where the built in voltage would be determined as an axis cut off ($V_a = 0$), and the doping level could be extracted from the slope of the curve (Eq. 21).

$$\frac{\mathrm{d}}{\mathrm{d}V_a}\left(\frac{1}{C_j^2}\right) = -\frac{2}{q\varepsilon_s N_A} \tag{21}$$

It was previously mentioned that equation 19 only holds for constant doping levels. However, the doping profile of the low-doped side of the junction as a function of position $x$ (Fig. 5) can also be determined[15]. This

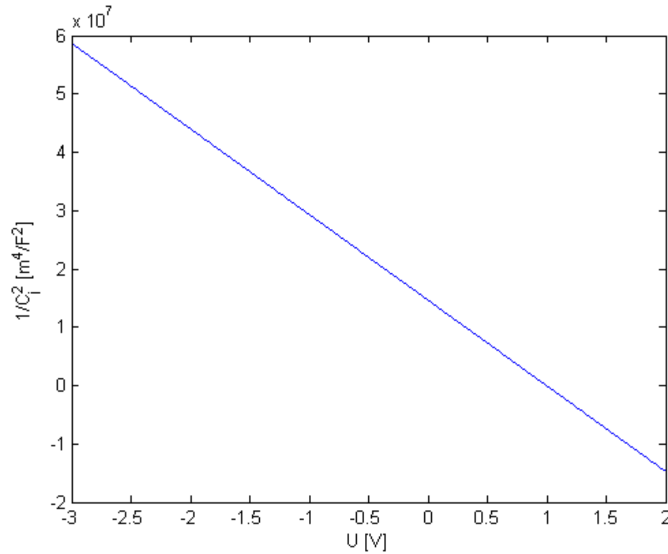



Figure 6: Example figure of $1/C_j^2$ in InP plotted agains $V_a$ using equation 20, with $N_A = 10^{16}$ $[1/cm^3]$, $N_D = 10^{19}$ $[1/cm^3]$ and $V_b = 1$ V. This graph does not take diffusion capacitance into account.

is done by combining equations 18 and 21, which allows for the construction of a doping profile along x.

The theory presented in the sections 3.3 and 3.4 for the capacitance of a p-n junction only holds for the reverse biased case. For the forward case diffusion capacitance becomes much larger than the transition capacitance previously presented. When a forward bias is applied over the p-n junction charge carriers will start to move into the oppositely charged region in order to recombine with the abundance of the opposite charge carrier in that region. As a result the depletion region decreases. The build-up of charge carriers trying to move into another region as well as a decreasing depletion region width results in an increase in capacitance.

For the purpose of this project the reverse bias case will be utilized.

### 3.5 Impedance Translation

The generally used method for capcitance measurements is an impedance measurement. As impedance $P$ consists of a real part $R$ and an imaginary part $-iZ$, models are needed in order to extract the capacitance from the

measurements. The impedance of a capcitor $-ix_D$ can be written as:

$$-ix_D = -\frac{i}{\omega C} \tag{22}$$

Where $C$ is the capacitance of the capacitor and $\omega$ is the angular frequency of the applied bias. The model adopted in order to describe the pn-junction was that of a capacitor in paralell with a resistor, in series with yet another resistor (Fig. 7).

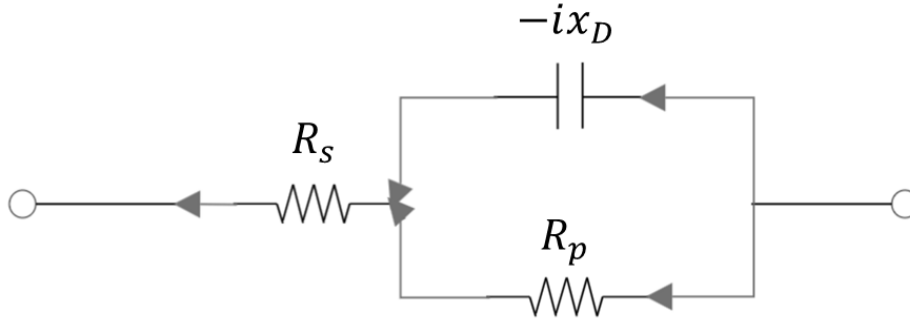



Figure 7: Model used to interpret impendance measurements for the pn-junction. The diode is modeled as a capacitor with a paralell resistor, in series with another resistor.

With the model depicted in figure 7 the total impedance of the component becomes:

$$P = R_s - \frac{ix_D R_p}{R_p - ix_D} = -i\frac{x_D R_p^2}{R_p^2 + x_D^2} + \frac{R_s R_p^2 + x_D^2 R_s + x_D^2 R_p}{R_p^2 + x_D^2} \tag{23}$$

By using the imaginary part $Z = x_D R_p^2 / R_p^2 x_D^2$, where $R_p$, $R_s$ and $x_D$ are resistances/impedances as depicted in figure 7, the resistance of the paralell resistor $R_p$ can be described as:

$$R_p = x_D \sqrt{\frac{-Z}{x_D + Z}} \tag{24}$$

In a similar fashion the real part $R$ can be used to describe $x_D$:

$$x_D = \frac{(R - R_s)^2 + Z^2}{-Z} \tag{25}$$

By estimating the current through the diode at backwards bias, rather than passing through any paralell component, the total resistance $R_{TOT}$ can be estimated as:

$$R_{TOT} = \frac{U_{TOT}}{I_{TOT}} = R_s + R_p \tag{26}$$

This allows $R_p$ to be written as:

$$R_p = \frac{R^2 + R_{TOT}^2 + Z^2 + 2RR_{TOT}}{R_{TOT} - R} \tag{27}$$

By combining equation 24 and 27, $w_D = 1/\omega C$ yields the capacitance $C$ as:

$$C = \frac{-Z}{\omega\Big((R - R_{TOT} + R_p)^2 + Z^2\Big)} \tag{28}$$

As such the capacitance required to solve equation 21 can be extracted from the impedance measurements.

### 3.6 The Ideal Diode Equation

As p-n junctions behave as diodes the measured current over a p-n junction can be used in order to determine if the p-n junction is well defined. In a model diode the current should follow the behaviour as specified in equation 29[39]:

$$i_D = I_s\Big(exp\Big(\frac{v_D}{nV_T}\Big) - 1\Big) \tag{29}$$

Where $i_D$ is the current through the diode, $v_D$ is the bias applied over the diode, $n$ is the ideality factor, and $V_T$ is the thermal bias ($V_T = kT/q$). For a model diode the ideality factor is in the range [1 2]. The equation (Eq. 29) describes the diode well in forward direction, and in the reverse direction it predicts that $i_D \rightarrow -I_S$ for large negative bias. However, usually the measured current is larger than the predicted one. As a low reverse current is desired the rectification ratio $r$ is used in order to give an indication of the quality of the diode. The rectification ratio is defined as:

$$r = \frac{i_D(x)}{|i_D(-x)|} \tag{30}$$

As can be seen in equation 30 the rectification ration determine order of magnitude which the forward current towers the reverse current at a given bias $x$ in forward respectively reverse direction.

As a model diode predicts low currents in the range close to $v_D = 0$, it can be used to determine any parallel resistance included in a diode system. As the total resistance at any given voltage $V$ gives:

$$\frac{1}{R_{TOT}} = \frac{1}{R_D} + \frac{1}{R_P} \tag{31}$$

Where $R_D$ is the resistance of the diode, $R_P$ is the parallel resistance, and $R_{TOT}$ the total resistance. If there is any significant current through the diode system for small biases, and as $R_D$ becomes really large for small biases, the current can be used to approximate any parallel resistance as:

$$R_P \approx \frac{V}{I_{TOT}} \tag{32}$$

# 4 Methodology

## 4.1 Investigation of the Device Material

To be able to continue previous research[15] on the possibility to use a vertical array device of nanowires as a tool for doping evaluatation, processing and measurements were carried out to investigate the poor electrical properties of the previous devices. During measurements on previous devices poorly rectifying devices were found [15], suggesting leakage currents. Previous designs were investigated using a *Scanning Electron Microscope* (SEM), and semi-cracks were found along a small portion (< 10%) of the device edges (Fig. 8). These cracks' effect on the device's performance as a whole was deemed insignificant due to the small number of appearances.

The devices generally displayed a uniform benzocyclobutene (*BCB*) surface with evenly spaced nanowires protruding from the surface by approximately 200 nm. The nanowires are 2 μm long, with a 1 μm long segment of heavily doped ($\sim 10^{19}$ $cm^{-3}$) n-type InP on top of a weakly p-doped ($\sim 10^{16}$ $cm^{-3}$) segment. As the nanowires are protruting the surface by approximately 200 nm it is thought that the metal contact is not circumventing the p-n junction. This due to the fact that the metal contact would need to be in contact with the depletion region centered around the p-n junction (3.3) for the current to be able to circumvent the p-n junction. As the depletion region does not expand as far as 800 nm from the p-n junction (the rough location of the metal contact) it can be assumed that the current is not circumventing the p-n junction as a result of contacting.

In order to localize the error in the design of the device used in order to perform electrical measurements on the nanowires a logical starting point was thought to be the nanowires, as they constitute the most vital part of the device. The nanowires were processed in order to, via single wire contacting, determine their electrical properties. The nanowires in question were broken off from a sample consisting of an array of grown InP nanowires with dimensions as presented previously. In order to be able to measure on the nanowires they had to be moved to a bonding substrate. The substrate was prepared by washing it in acetone during ultrasonic treatment for 2 min, followed by a similar treatment in IPA. This method was used to break the nanowires off from the substrate, and a piece of paper was later used to transfer them to the bonding substrate. Two samples were prepared in parallel in order to yield a larger amount of reliable data in the end.

The preparations for the contacts that were to be defined using EBL, consisted of localizing the nanowire intended for bonding and then con-

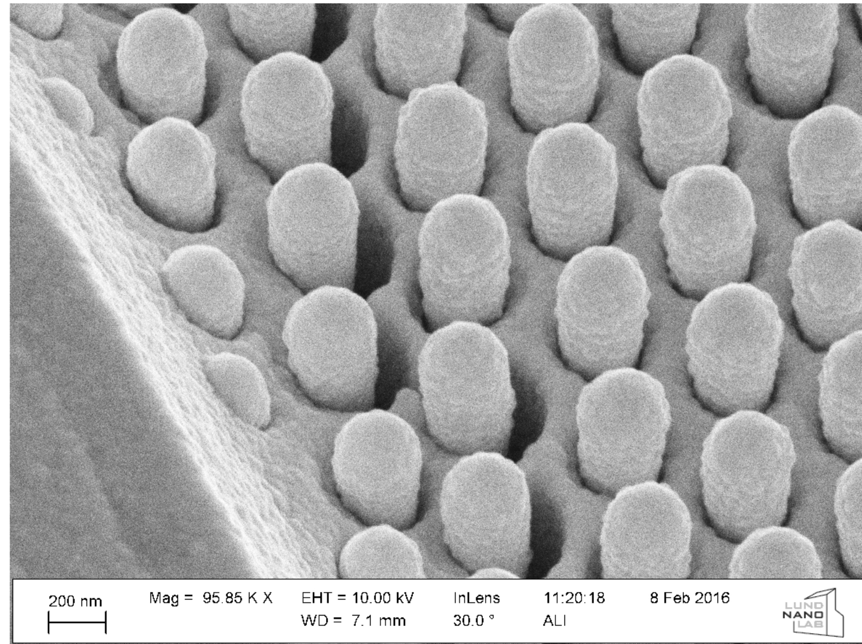
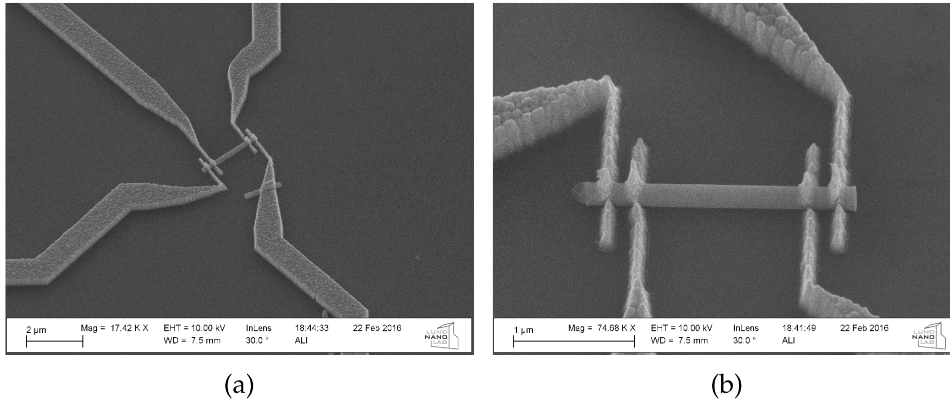



Figure 8: SEM image of formed semi-cracks in BCB along the device edge. The Nanowires protrude from the surface by roughly 200 nm.

structing a contact pattern using software *EBL-Builder* in unison with images taken with a SEM. As it is reasonable to expect the possibility of so-called Schottky-like contacts when contacting to the p-doped part of the wires, a bonding pattern for 4-probe measurements was constructed for one of the samples. The ability to determine if ohmic contacts are possible with the 4-probe setup. Despite the trade-off of a lower yield (4-probe measurements results in half the amount of bondable nanowires) this was thought to be preferable, and thus two different patterns were prepared (one for 2-probe bonding and one for 4-probe bonding). An example of a 4-probe setup can be seen in figure 9a. The resist that was to be patterned *Polymethyl Methacrylate 950K* (PMMA 950K) was spun on to the samples at 5000 rpm for 1 min, followed by baking on a hot plate at 180°C for 5 min. The resist was then treated in an EBL system *Raith 150* to define the desired pattern for the contacts. The pattern was then developed for 1 min in 1:3 *Methyl Isobutylketone:Isopropanol* (MIBK:IPA), followed by 1 min in IPA. As there was a possibility for natural oxide to form on the substrate between development and evaporation of the metal contacts, the samples were treated




(a) (b)

Figure 9: (a): SEM image of a contacted nanowire. The outer contacts are spaced 100 nm from each other. (b): The rougher end determines its doping as p-type. In contrast, the smoother end determines it as previously contacted to the seed particle, thus being n-doped.

in *Buffered Oxide Etch (BOE) 10:1 JT Baker* for 1 min, followed by 1 min in *deionized water* (DIW) before being placed in the evaporator *AVAC*. A layer of Pd/Zn/Pd/Au[25] was evaporated on top of the samples with thicknesses 2.5/20/2.5/225 nm. The samples were then left in acetone over the night in order to lift off the resist and unwanted metal on the surface. The lift off was completed the next day, as the resist was rinsed off in Acetone, followed by IPA.

I-V measurements were carried out on a probestation *Cascade 11000B* to determine the properties of the p-n junctions. The results are presented in 5.1 (Fig. 21 and 23). The contacts were then investigated with a SEM as to determine the polarity, and thus whether any diodic behaviour originated from the nanowire p-n junction or from other sources, e.g. Schottky contacts. The polarity of the wires was determined by comparing the ends of each individual wire, distinguishing the doping type by the general roughness of the ends (Fig. 9b), as the nanowires were broken off from the substrate at the p-doped side. In order to determine to what degree the nanowires influence the full device, measurements were also taken for previously manufactured devices, with an isolating BCB layer[15].

As signs of parallel resistance (3.6) were found in the full devices during measurements (see 5.1, Fig. 22a) an attempt to cure the BCB was carried out. It was reasoned that successful curing could reveal if there were pinholes in the resist. The sample was thus cured for 10 min at 250°C, using a rapid

thermal processing system *RTP 1200*.

It was realized after the first series of measurements that InP had a turn-on voltage at around 1.4 V, although slightly higher than the bandgap it is consistent with other research [27], and in order to get a better estimate of the ideality factor, as well as the rectification, a second series I-V measurements were carried out on the nanowires between -2.5 to 2.5 V.

## 4.2 First Revision of Device Design

As described in 5.1 there were apprehensions concerning parallel resistance in the device. Electrical measurements showed diodic behaviour in the nanowires. Hence radial overgrowth had been ruled out during the single nanowire contacting (5.1. Fig. 23), the properties of the insulating BCB was instead thought to be the cause, and a design for a new device was made (Fig. 10) in order to investigate said BCB. The new design incorporated a thin layer of $SiO_2$ around the nanowires, thus protecting the p-segment and the substrate from current leaking through the resist.

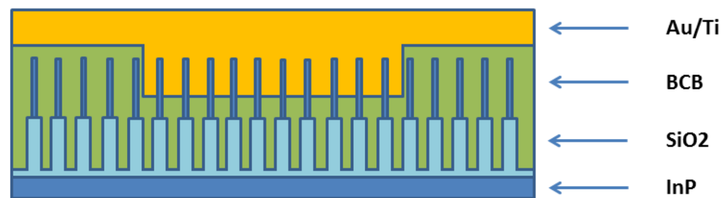



Figure 10: Schematics depicting the design used in order to investigate the properties of the BCB.

Since the exact etch rate of BCB inside the RIE system *Etcher RIE - Trion T2* was unknown, and it was of interest to investigate if a current could be drawn through the BCB, a set of dummy samples were created. This was done by cleaning eight Si substrates in Acetone inside an ultrasonic bath for 1 min, followed by 1 min in IPA. A layer of BCB was then spun onto the substrates. Four substrates were spun at 3000 rpm, resulting in a resist thickness of ∼3 µm. The remaining four substrates were spun at 5000 rpm, resulting in a resist thickness of ∼2.3 µm. The spin-coating was followed by soft baking for 90 s at 120°C, before which the backside of the samples were cleaned of resist using EBR PG. In order to harden the resist the samples were placed in a rapid thermal processing system to bake for

1 h at 250°C, for full recipe see Appendix C. To create dummy samples similar in design to that shown in figure 10, a photolithography step was carried out on the four samples that had been spin-coated at 3000 rpm. The samples were first cleaned in Acetone for 30 s, followed by 30 s in IPA. In order to coat the samples with photoresist S1828, they were spin-coated at 3000 rpm, followed by baking for 90 s at 115°C. After 2 bursts of UV-light exposure in UV-lithography system *Mask aligner MJB4 (soft UV)* the resist was developed for 2 min in MF319, followed by 1 min in DIW. The exposed BCB was then etched in a RIE system, using 10 sscm of $CF_4$, 70 sscm of $O_2$, at a pressure of 250 mTorr, with 150 W of power feeding the plasma. The four samples were etched for different amounts of time, at 30, 60, 90, and 120 s respectively. This allowed for determination of the etch rate. Through the usage of a surface profiler system the etch rate was determined to be ~2 μm/min. The remaing S1828 was removed in Acetone for 1 min, followed by 1 min in IPA. To create the metal contact on top of the samples, two samples, determined to have a BCB layer not fully etched through during RIE, were placed in sputtering system *Sputterer - AJA Orion 5*, where a thin layer (206 Å) of Ti was first sputtered onto the samples, followed by 200 nm of Au.

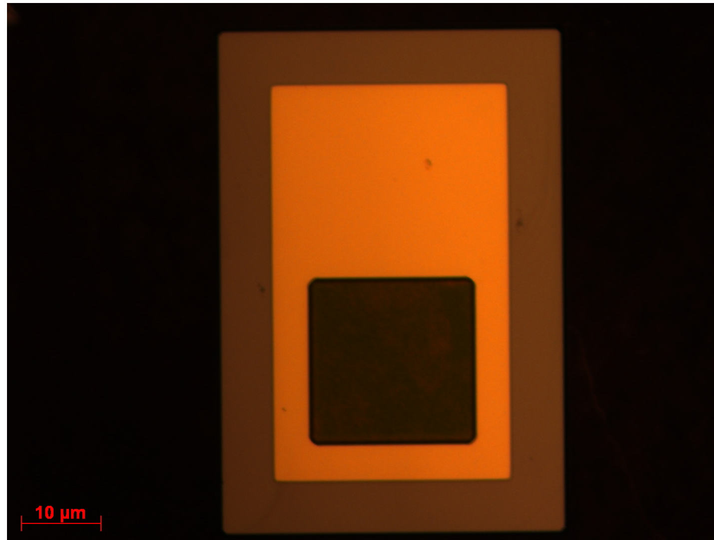
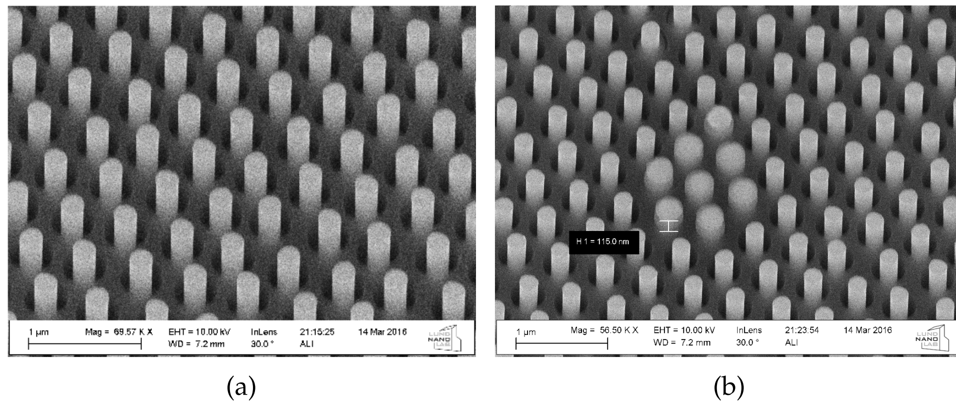



Figure 11: Optical image of the device created through the process described in 4.2. The orange area is the Au contact, the light brown is the isolating BCB layer, and the dark surrounding area consists of exposed nanowires.

The final devices were defined with yet another UV-lithography step, where the samples were first cleaned with Acetone for 1 min, followed by 1 min in IPA, a layer of S1828 was then spin-coated at 3500 rpm, and baked for 90 s at 115°C. The samples were then exposed in a UV-lithography system for 2 intervals of 10 s, followed by development in MF319 for 2 min, and 1 min in DIW. The exposed Au was then etched in $KI/I_2$ for 2 min, followed by 1 min in DIW. As it is likely that there are remains of the Ti layer after the Au etch a second etching was done to remove the Ti where the samples were etched for 10 s in BOE 1:10 JT Baker, followed by 1 min in DIW. The remaining photoresist was removed by 1 min in Acetone and 1 min in IPA. The finished device resembled the real device displayed in figure 11, aside from the nanowires not being present.

As the final objective was not to create dummy samples, but rather a device as depicted in figure 10, processing was carried out on InP substrates with nanowire arrays grown on top. The samples were provided, and had a p-doped substrate with a segment of p-doped nanowire on top, the p-doped segment was then followed by an n-doped segment. The nanowires had a width of ~200 nm, and length of ~2.2 µm, with a ~1.1 nm long p-doped segment and an ~1.1 nm long n-doped segment.




(a) (b)

Figure 12: (a): Exposed nanowires, protruding the S1818 surfaces. (b): Unetched nanowires, $SiO_2$ still covers the top segment of 8 nanowires after 227 s of etching in BOE 1:10 JT Baker.

Two samples with InP nanowires were processed. A table summerizing the processing method for the two samples can be found in Appendix I. The samples were prepared for the deposition of a thin layer of $SiO_2$ by first being cleaned for 1 min in Acetone, followed by 1 min in IPA. A 40-50 nm

$SiO_2$ layer was deposited followed by a 5 nm layer of $Al_2O_3$ (in order to promote adhesion of BCB to the sample) in an ALD system *ALD system - Savannah-100*. With the intent to etch away $SiO_2$ from the top of the covered wires a layer of S1818 was spun on top of the samples. Before spin-coating the samples were cleaned in Acetone for 1 min, followed by 1 min in IPA. The samples were then spun at 3000 rpm, and baked at 115°C for 90 s. To allow the ends of the nanowires to be etched the S1818 needed to be etched back, exposing the tops of the nanowires. This was done using a RIE system, for a total of 2600 s, with a gas flow of 15 sscm $O_2$, and 50 W of power feeding the plasma. The result can be observed in figure 12a (unfortunately one of the samples broke, and was from there only used as a dummy sample). The $SiO_2$ was then etched using BOE 1:10 JT Baker for 227 s, as the etch rate was understood to be 2.7 nm/s from in house experience, it would result in ~600 nm of etching. The sample was then rinsed in DIW for 1 min.

As the thickness of the $SiO_2$ was ~50 nm it was undoubtedly thought to be enough. However, during SEM investigation unetched wires were found (Fig. 12b). In order to remove these a second series of RIE etching was performed, etching an extra 750 s with 15 sscm of $O_2$, and 50 W of power feeding the plasma. The $SiO_2$ was then etched once more with BOE 1:10 JT Baker, this time for 45 s, followed by 1 min in DIW. The S1818 was then stripped with Acetone for 1 min and 1 min of IPA. The resulting structure is displayed in figure 13.

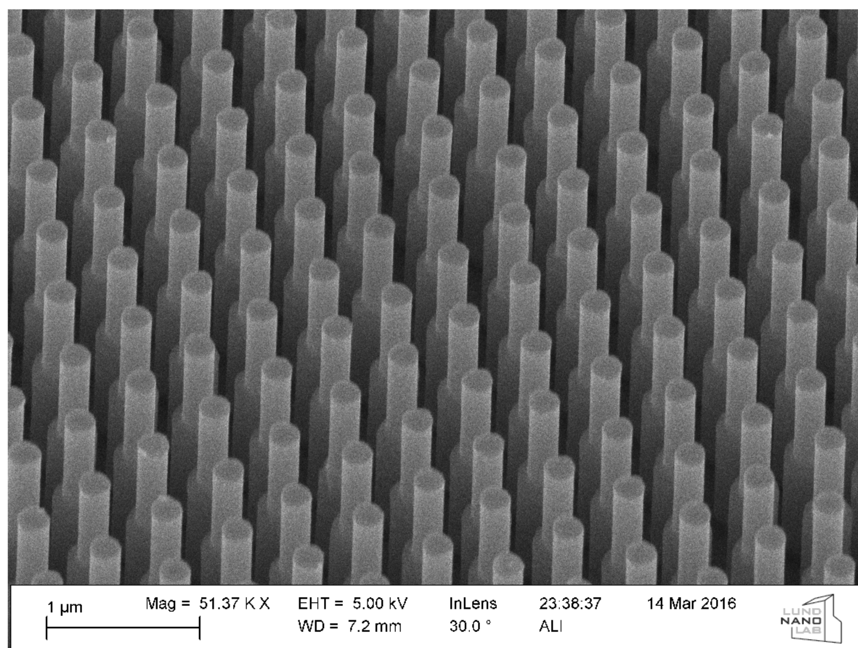
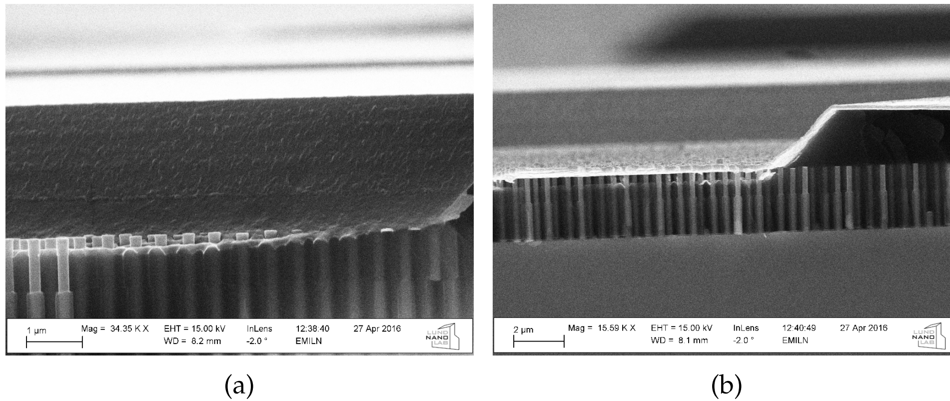



Figure 13: Nanowires after the $SiO_2$ has been etched, and the S1818 has been stripped. ~800 nm of the nanowires are exposed.

In order to define the outline of the devices a layer of BCB was spun onto the sample. The sample was spun at 5000 rpm, resulting in a resist thickness of ~2.35 µm. The spin-coating was followed by soft baking for 90 s at 120°C, before which the backside of the sample was cleaned of resist using EBR PG. To harden the resist the sample was placed in a rapid thermal processing system to bake for 1 h at 250°C—for full recipe see Appendix C. To create the design shown in figure 10, a photolithography step was carried out on the sample. The sample was first cleaned in Acetone for 30 s, followed by 30 s in IPA. In order to coat the sample with photoresist S1828, it was spin-coated at 3000 rpm, followed by baking for 90 s at 115°C. After 2 bursts of UV-light exposure in UV-lithography system *Mask aligner MJB4 (soft UV)* the resist was developed for 2 min in MF319, followed by 1 min in DIW. The exposed BCB was then etched in a RIE system for a total of 85 s, using 10 sscm of $CF_4$, 70 sscm of $O_2$, at a pressure of 250 mTorr, with 150 W of power feeding the plasma. The remaing S1828 was removed in Acetone during 1 min, followed by 1 min in IPA. To create the metal contact on top of the sample it was first etched for 1 min in $H_2SO_4$:$H_2O$ 1:10, followed by

1 min of DIW in order to remove natural oxide. It was then placed in a sputtering system where a thin layer (206 Å) of Ti was first sputtered on to the sample, followed by 2000 Å of Au. The final devices were defined with yet another UV-lithography step, where the sample was first cleaned with Acetone for 1 min, followed by 1 min in IPA. A layer of S1828 was then spin-coated at 3500 rpm, and baked for 90 s at 115°C. The sample was then exposed in a UV-lithography system for 2 intervals of 10 s, followed by development in MF319 for 2 min, and 1 min in DIW. The exposed Au was then etched in $KI/I_2$ for 2 min, followed by 1 min in DIW. As it is unlikely the Ti layer is etched in the process, a second etching was done to remove the Ti. The sample was therefor etched for 10 s in BOE 1:10 JT Baker, followed by 1 min in DIW. The remaining photoresist was removed by 1 min in Acetone and 1 min in IPA. The finished device can be seen in figure 11.

Electrical measurements were then carried out on a probestation *Cascade 11000B*. I-V characteristics were collected for biases between -1.7 V and 1.7 V. The data is presented in 5.2 (Fig. 24). After receiving data that supported the idea of leakage between the devices the sample (Fig. 26) was cleaved to enable for a cross-section inspection through SEM, see figure 14. This was mainly done in order to see if there was a thin metal layer on top of the sample that created a contact between devices (the sample being the fully processed substrate, and the device being a device as depicted in figure 11).




(a) (b)

Figure 14: (a): SEM images of the exposed nanowires outside of a device. The edge of metal layer of the device can be seen in the background (poorly focused). (b): The nanowires inside the device, covered with the contacting metal layer.

## 4.3 Investigating the Isolating Properties of BCB

From the results in 5.2 it can be seen that there was a similar fault (poorly rectifying devices) in the devices as the one observed for the devices presented in 4.1, and the fact that no metal seemed to be present between different devices on the samples (a clear edge of metal is visible in figure 14) the BCB layer was now questioned. As such one of the two previously prepared planar Si substrates which had had a layer of BCB spun on them at 5000 rpm was treated with UV-light in UV-lithography system for two bursts of 10 s. The reason only one of the two samples was flooded was to determine if the UV-treatment could alter the properties of the BCB. The samples were then placed in a sputtering system, depositing 200 Å Ti and 2000 Å Au on top of them. Isolated measuring pads were then defined using the same UV-lithography treatment and metal etch as for the InP nanowire sample presented later in this section. Measurements were then carried out on a probestation in order to see if the BCB was conductive. The results can be found in 5.3.

Measurements on the design presented in 4.2 (Fig. 10) showed a strong reverse current (Fig. 24). Hence in order to see whether the problem with the heavy back-current (3.6) during reverse bias was due to BCB's involvement in the device, a device similar to that in 4.2 but void of BCB inside the metal-nanowire bonding area was manufactured: see figure 15. A new batch of InP nanowires with the same growth parameters as previous samples were provided. See Appedix F for parameters.

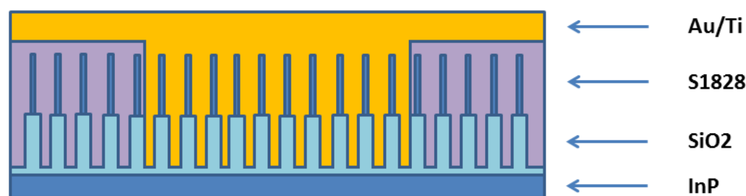
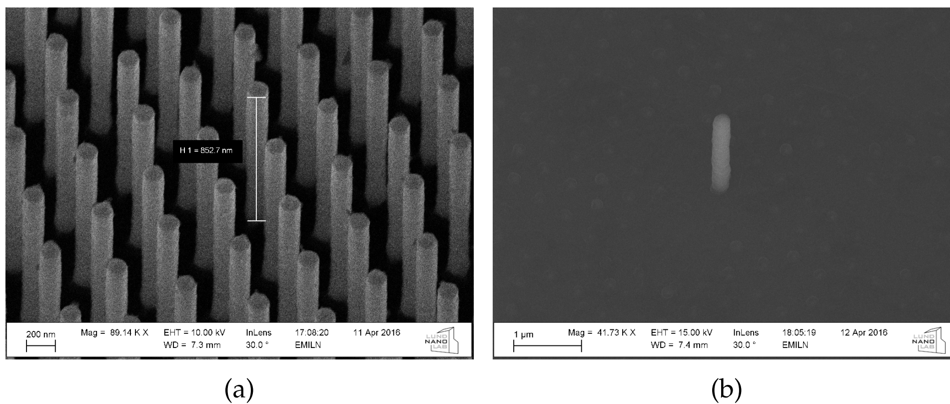



Figure 15: Schematics depicting the design used in order to investigate the properties of the BCB.

The samples were first cleaned in Acetone for 1 min, followed by 1 min in IPA. As the catalyst Au particle was still attached to the grown nanowires, and thought to pose a problem during contacting, the particle was etched off by treating the sample with 10s of $H_2SO_4$:$H_2O$ 1:10 followed by 10s of $KI/I_2$. This treatment was repeated three times. During SEM inspection

of the samples (Fig. 16a) doubts regarding whether the Au particle had fully been removed arose. The substrate was thus etched for three more cycles before the samples were placed in an ALD system. A 40-50 nm layer of $SiO_2$ was deposited, with a 5 nm $Al_2O_3$ on top of it in order to promote adhesion. After the ALD treatment the samples were once more investigated with SEM (Fig. 16b), and it was found that the samples had been stripped of nanowires during the second etching treatment, this to our surprise, as similar etching times had been used previously[15]. After receiving input from other researchers, whom have had the same experience with $KI/I_2$ etching InP, it was decided to maintain more conservative etching times for future processing. The reason for the break off could be due to the intermediate DIW, that is supposed to be a rinsing agent, becoming contaminated and thus resulting in added etching times.




(a) (b)

Figure 16: (a): The nanowires after attempts to remove the catalyst Au particle had been carried out. (b): After second etch the nanowires had been shaved off from the substrate.

During the next attempt to create the device sought after (void of BCB), the InP nanowire sample was prepared in the same way as previously, except the sample was only exposed to the etching process three times, with the etching process being: 10s of $H_2SO_4$:$H_2O$ 1:10 followed by 10s of $KI/I_2$. As the processing method is similar to the one presented in 4.2 it will be summerized in the table below.

| Design III |
| --- |
| Nanowire Au seed particle removed:<br>3x(20 s $H_2SO_4$ 1:10 + 10 s DIW + 20 s KI/$I_2$ + 10 s DIW) |
| Cleaned backside with IPA + rinse in Acetone for 1 min + 1 min IPA |
| ALD: 40-50 nm $SiO_2$ + 5 nm $Al_2O_3$ |
| Rinsed in Acetone for 1 min + 1 min IPA |
| Spin-coat S1818 @ 3000 rpm for 60 s, soft baked for 90 s @ 115°C |
| RIE, 15 sscm $O_2$, 50 W, 2000 s |
| Etch $SiO_2$: 111 s BOE 1:10 JT Baker + 1 min DIW |
| Strip S1818: 1 min Acetone + 1 min IPA |
| Spin-coat S1828 @ 3500 rpm for 60 s, soft baked for 90 s @ 115°C |
| UV-lithography: 2x 10 s exposure |
| Develop: 2 min MF319 + 1 min DIW |
| Hard-baking S1828: 200°C for 40 min + 10 min cooling down |
| Ecth natural oxide: 1 min $H_2SO_4$:$H_2O$ 1:10 + 1 min DIW |
| Sputter 200 Å Ti + 2000 Å Au |
| Rinse in DIW for 1 min |
| Spin-coat S1828 @ 3500 rpm for 60 s, soft baked for 90 s @ 115°C |
| UV-lithography: 2x 10 s exposure |
| Develop: 2 min MF319 + 1 min DIW |
| Au-etch: 2 min KI/$I_2$ + 1 min DIW<br>Residue-etch: 10 s BOE 1:10 JT Baker + 1 min DIW |
| Strip S1828: 1 min Acetone + 1 min IPA |

The sample was contacted with a brass coin using conductive silver glue before measurements were carried out on a probe station. Measurements can be found in 5.3.

As surfaced during measurements (5.2 and 5.3) of the device presented in 4.2 and previous planar Si samples, there were doubts regarding the isolating properties of BCB. BCB is marketed as a good isolator [31], and thus the measurements obtained (5.2 and 5.3) were surprising. As the BCB previously used had been provided by a second party, the quality of the resist was unknown, and thus a new batch of BCB *Cyclotene 3022-46* was used for the processing presented in this section. During processing it was observed that the viscosity of the solution was questionably less. If true, this would suggest that the previous batch had higher viscocity, as a result of manufacturing or due to the solvent evaporating over time (this is also strengthen by the vendor specifications, see Appendix E, as thicker resists results in a thicker layer after spin-coating). The higher viscosity also answer the question regarding longer etching times than expected during

RIE during processing (4.2), as higher viscosity would mean a thicker layer after spin-coating. In order to investigate the isolating properties of BCB two devices were produced.

The new samples were created by first cleaning the Si substrates in Acetone for 2 min during ultrasonic treatment, followed by 1 min in IPA. A layer of BCB was then spun onto the samples at 5000 rpm, creating a layer thickness of roughly 2.3 μm. The backsides of the substrates were then cleaned with EBR PG before the samples were left to soft bake at 120°C for 90 s. As the BCB was going to be the final layer under the top metal contact, with no other treatment to it as it is unaffected by UV-lithography (Sec. 5.3), it needed to be hard baked, and this was done in a RTP system at 250°C for 1 h. Before placing the samples in a sputtering system they were cleaned in Acetone for 1 min, followed by 1 min in IPA. A 200 Å layer of Ti, followed by 2000 Å of Au were then deposited on top of the sample. In order to define measuring pads on top of the sample a layer of S1828 was spun onto the samples at 3500 rpm. The resist was soft baked at 115°C for 90 s before being treated to two bursts of UV-light for 10 s each in a UV-lithography system. The pattern was then developed in MF319 for 2 min followed by rinsing in DIW for 1 min. The unwanted metal was then etched away in $KI/I_2$ for 2 min, rinsing the samples in DIW for 1 min before following up with 10 s in BOE 1:10 JT Baker and another rinsing step in DIW for 1min. Lastly the unwanted S1828 was removed with Acetone for 1 min, followed by 1 min in IPA.

### 4.4 Investigating the adoption of S1818

As the properties of BCB were being questioned, a design void of BCB was instead favoured. As shown during earlier attempts to manufacture the desired device [15] S1818 could be used as an isolating inter-wire medium. A design utilizing S1818 was previously discarded due to the increased manufacturing times, as well as an abundance of cracks showing up in the S1818 film during processing. The cracks were thought to be able to enable the deposited metal contact to create leakage paths, and were thus heavily opposed. In order to avoid cracking a new design was created. Instead of having a uniform S1818 film covering the whole sample, a lithography step would be carried out, creating localized platelets of S1818 in the device areas. A decrease in the are covered by S1818 was thought to decrease the strain introduced to the S1818, thus lowering the probability of cracking. A layer of $SiO_2$ was also used in parallel with the S1818 to ensure separation between wires, as well as no capacitance occurring from side-contacted

wires. Simple schematics of the intended device can be seen in figure 17.

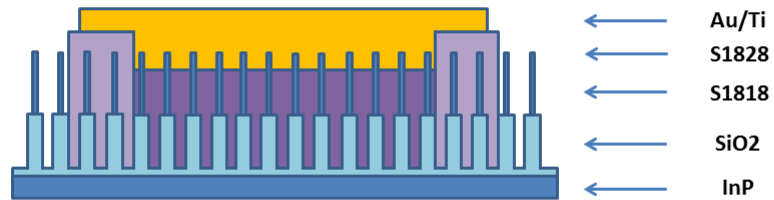


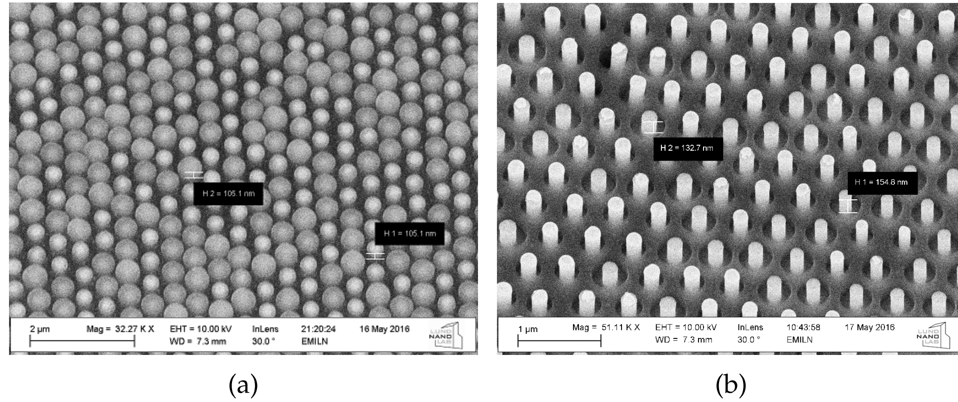

Figure 17: Schematic depicting the design used for the intended device, utilizing S1818 as the isolating medium.

In order to manufacture the device described, 3 samples were prepared. Among the three samples, one (Ax11235a) had nanowires that had had p-segments grown under conditions with a molar fraction of $6.3 \cdot 10^{-7}$ $DEZn$, and the other two (Ax11236d and Ax11236e) had been grown under conditions with a molar fraction of $2.1 \cdot 10^{-7}$. See Appendix F for more details. As the processing method is similar to the one presented in 4.2 it will be summerized in the table below.

| **Design IV** |
| --- |
| Nanowire Au seed particle removed:<br>3x(20 s $H_2SO_4$ 1:10 + 10 s DIW + 20 s KI/$I_2$ + 10 s DIW) |
| Cleaned backside with IPA + rinse in Acetone for 1 min + 1 min IPA |
| ALD: 50-100 nm $SiO_2$ + 5 nm $Al_2O_3$ |
| Spin-coat S1818 @ 3000 rpm for 60 s, soft baked for 90 s @ 115°C |
| RIE, 15 sscm $O_2$, 50 W, 2900-3000 s |
| Etch $SiO_2$: 186 s BOE 1:10 JT Baker + 1 min DIW |
| Strip S1818: 2 min Acetone + 1 min IPA |
| Spin-coat S1818 @ 3000 rpm for 60 s, soft baked for 90 s @ 115°C |
| UV-lithography: 2x 7.5 s exposure (1 min between exposures) |
| Develop: 2 min MF319 + 1 min DIW |
| Hard-baking S1818: 200°C for 40 min + 10 min cooling down |
| RIE, 15 sscm $O_2$, 50 W, 2300-2450 s |
| Spin-coat S1828 @ 3500 rpm for 60 s, soft baked for 90 s @ 115°C |
| UV-lithography: 2x 10 s exposure (1 min between exposures) |
| Develop: 2 min MF319 + 1 min DIW |
| Hard-baking S1828: 200°C for 40 min + 10 min cooling down |
| RIE, 15 sscm $O_2$, 50 W, 100 s |
| Ecth natural oxide: 1 min $H_2SO_4$:$H_2O$ 1:10 + 1 min DIW |
| Sputter 200 Å Ti + 2000 Å Au |
| Spin-coat S1828 @ 3500 rpm for 60 s, soft baked for 90 s @ 115°C |
| UV-lithography: 2x 10 s exposure |
| Develop: 2 min MF319 + 1 min DIW |
| Au-etch: 2 min KI/$I_2$ + 1 min DIW<br>Residue-etch: 10 s BOE 1:10 JT Baker + 1 min DIW |
| Strip S1828: 1 min Acetone + 1 min IPA |

It was found that the deposited $SiO_2$ layer was 50-100 nm thick. The variation in thickness can be seen in figure 18a, where the S1818 has been etched back using an RIE system for 2900 s.

As shown in figure 17 platlets of S1818 needed to be created before applying the S1828 layer (this differs from previous designs). The difference between an S1818 covered area and a non-covered area (outside of platlet) is shown in figure 19.




(a) (b)

Figure 18: (a):Ax11236d after 2900 s of RIE, before $SiO_2$ etch. The $SiO_2$ caps covering the nanowires can be seen protruding the S1818 with ~200 nm. (b): After $SiO_2$ etching using BOE 1:10 JT Baker the caps have been removed.

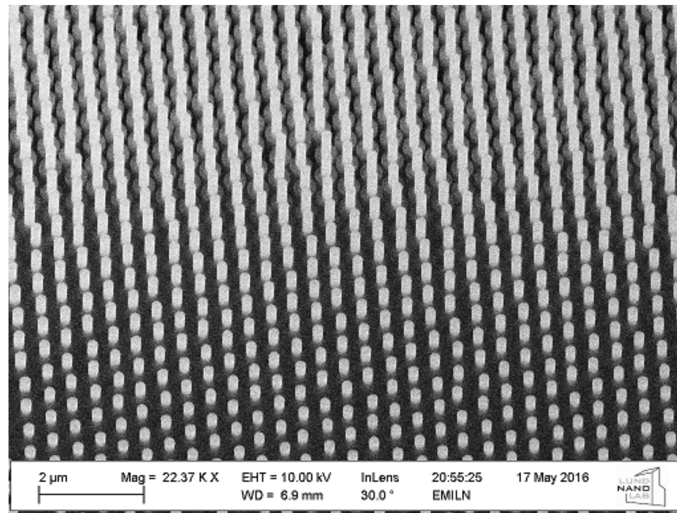



Figure 19: The edge of one of the S1818 platelets on Ax11235a. Outside the S1818 area (top of the image) the covering $SiO_2$ can be seen, but inside the area (bottom of image) only the protruding top segment (~ 300 nm) of the nanowires is visible.

Electrical measurements on the finished devices; IV- as well as CV-measurements were carried out on a probestation. See 5.4 for measurements.

# 5 Results

In this section the data from the previously described experiments (4) will be revealed and analyzed in an attempt to further increase the understanding for the intention of this project.

## 5.1 Previous Device Design

As the purpose of doing single nanowire contacting was to determine if the earlier results[15] were due to e.g. radial overgrowth on the nanowires, I-V measurements were carried out. The sample with two contacts applied to each individual nanowire (intended for 2-probe measurements) had a very bad ratio of measurable nanowires. This was revealed to be due to bad contacts, as the contacts had collapsed (Fig. 20) while they were grown. The reason behind this is thought to have been a too generous amount of metal being deposited to make the contacts. Thus only two measurements could be carried out on the first sample. The breaking of the contacts was thought to be avoidable if the nanowires were partially emerged in resist before the contacts were applied.

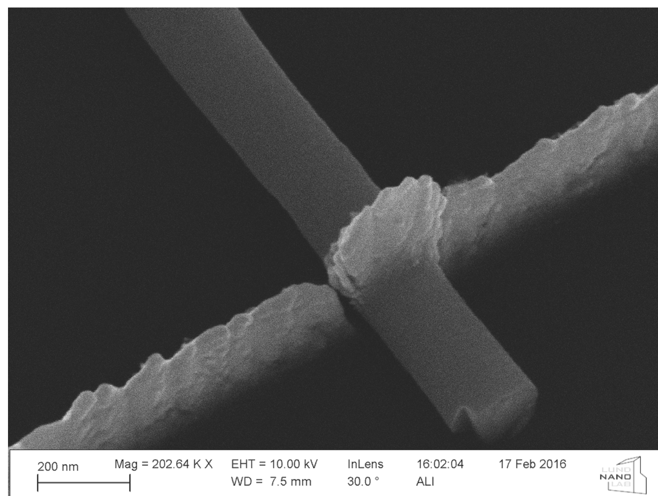
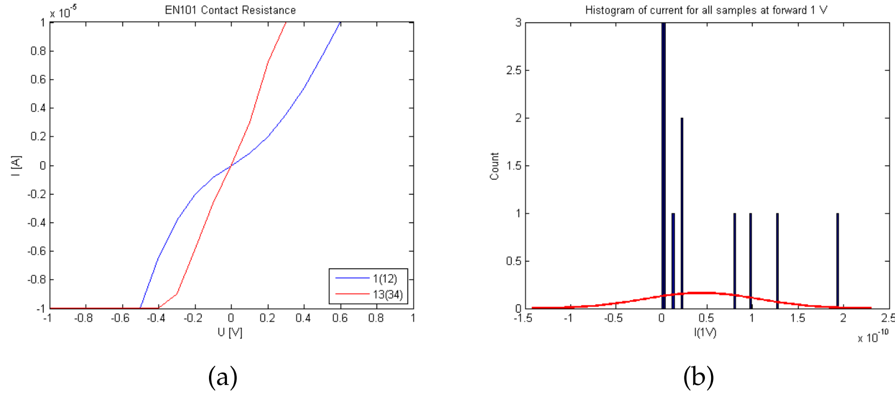



Figure 20: A collapsed contact, a fracture in the contact can be seen at the edge of the nanowire/contact interface. Failure is thought to be due to weight of the contacts, as a result of too generously chosen thickness (~250 nm). The metal contact appears brighter than the underlying nanowire in the image.

As the second sample contained more contacts per each individually contacted nanowire (intended for 4-probe measurements) a higher yield of measurable nanowires were obtained. The measurements (Fig. 23) showed clear diodic behaviour, and concerns regarding the possibility that the nanowires would have been subjected to radial overgrowth during the growth of the n-doped segment could be discarded for the moment. As the contacts were subject to the same type of collapse as the sample with two contacts per nanowire, the existence of a nanowire with four intact contacts were not observed. For two of the nanowires two intact contacts existed on the same doped segment, the I-V measurements are displayed in figure 21a. The resistance was calculated to be 75 kΩ, 31 kΩ respectively. These values strengthen our belief that contacts that satisfy our needs have been formed. Unfortunately, after analysing the polarity of the nanowires it was determined that both of these measurements had been performed on the n-doped segment, generally thought to form good contact. At the time no conclusions about the properties of the more troublesome p-doped segment could be made.

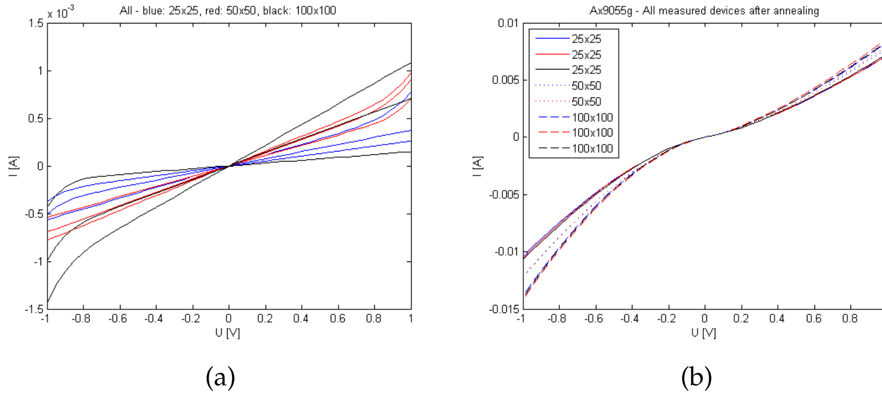



(a) (b)

Figure 21: (a): The measured current over contacts located on the n-doped segment of the nanowires. (b): The current for all 2-probe nanowires at 1 V. The data has been altered to take polarity in to account. The red curve symbolizes the distribution, with an average around $0.5 \cdot 10^{-10}$ A.

The measured current levels over the p-n junctions, displayed in figure 21b, were compared with results obtained through simulations in *COMSOL: Multiphysics 5.0*, as well as an evaluation tool available at *nanoHUB*[19]. The measured values of the current at 1 V were found to be in the range of 1/10 of the simulated values (Appendix A). As the real system can

contain e.g. series resistance, not included during simulations, the obtained measurement reassures us that the nanowires' properties are close to what is intended. Thus concerns regarding radial overgrowth were once again discarded. The nanowires showed a rectification ratio of, at best, 388, and a mean ideality factor (3.6) of ~4.49 (for more data see Appendix B).




(a) (b)

Figure 22: (a): The I-V characteristics for working devices of various sizes, blue are for the smallest (25x25 $\mu m^2$) device size, red is the 50x50 $\mu m^2$ devices, and black is the 100x100 $\mu m^2$ devices. (b): The current through device Ax9055g after attempted curing of the BCB.

The measured values for the bonded single nanowires were then compared to the current of the full device. In order to compare the two systems the single nanowire measurements had to be scaled up with a factor representing the number of nanowires a window of the devices contained. The density of wires can be calculated using equation 33, where $\rho$ is the density, and $l$ is the pitch between wires.

$$\rho = \frac{2}{3}\frac{\sqrt{3}}{l^2} \tag{33}$$

The density was calculated using a pitch of 500 nm, resulting in $2.85 \cdot 10^3$, $1.15 \cdot 10^4$ and $4.6 \cdot 10^4$ nanowires for windows of sizes 25x25 $\mu m^2$, 50x50 $\mu m^2$ and 100x100 $\mu m^2$ respectively. As the average current (fig. 21b) at 1 V for a single nanowire were scaled up and compared to the current observed in the finished devices (fig. 22a), it was discovered that the device current is a factor of $10^3$ higher than the scaled up current. This causes us to believe that there is a leak current present in the device. As the devices display linear behaviour between -0.6 V and 0.6 V (fig. 22a), a parallel resistance

behaviour in conjuncture with the diodic behaviour of the p-n junction was assumed. Hence, measurements of the resistance of two devices, as well as the resistance between them were conducted. The two devices displayed an internal resistance of ~1 kΩ each, and an inter-device resistance of ~400 Ω. As it is expected that the inter-device resistance should be in the range of PΩ if passing through the BCB (Appendix E) or atleast 2 kΩ if passing through the nanowires (series of two ~1 kΩ devices), the measurements act to further strengthen the idea that there is unwanted parallel resistance in the devices.

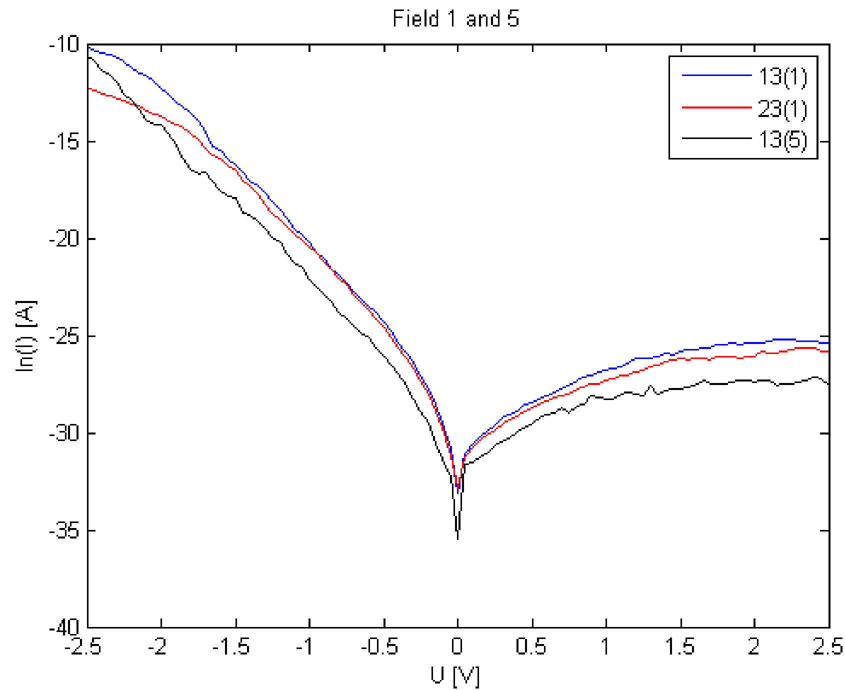



Figure 23: The logarithm of the current through a single nanowire as a voltage is applied.

During the measurements performed under the new parameters described in 4.1 (current measured for biases between -1 V and 1 V) it was found that the attempted curing of the BCB had caused the devices to further behave as a resistor (fig. 22b). As the resist was cured after metal contacts had been applied there is the possibility of a tear between resist and contact. A tear could cause the nanowires to become disconnected

from the metal contact. If there are shunt paths/leakage paths the measured current will behave more like that for a resistor (as the nanowires becomes disconnected the diodic behavior contribute less to the measured signal). However, this would also mean less of a current, and as there is still an observable current the problem is likely that of an alternative origin.

From the measurements carried out on single nanowires for an applied bias ranging between -2.5 to 2.5 V, a reduction of measurable nanowires were observed, and the data collected from the still measurable nanowires is displayed in figure 23. From the data it was deduced that the ideality factor was ~4.92, and the mean rectification (calculated for -2 V and 2 V) was calculated to be $\sim 4.16 \cdot 10^5$ (for more data see Appendix B). The ideality factor lies between 1 and 2 for an model diode, and the fact that the ideality factor is larger than 2 suggests that there are imperfections in the device, e.g. high series resistances from nonohmic contacts. It could also come from recombination at the p-n junction, which is also highly likely as InP is (as previously stated) suited for solar cells. It is worth noting that for the type of devices presented throughout this report the typical ideality factor lies above 2 for reasons just stated.

## 5.2 IV Characteristics of a BCB-based Device

As was discovered during early measurements on old devices[15] a large leakage at low voltage was observed (5.1, Fig. 22a). As the current at low voltages was significantly larger than the model predicted (Appendix A) it was concluded to be signs of parallel resistance in the devices. The source of the parallel resistance was thought to be either deficiency in the nanowires, or the inter-nanowire isolating layer of BCB. The properties of the nanowires were investigated (5.1), and from the data collected (Fig. 23) it was found that the nanowires could not be the source of the parallel resistance.

In order to investigate the properties of the isolating BCB layer a second device design was used (4.2) . Electrical measurements were first carried out on the manufactured device. From the measurements it was deduced that the processing had been successful, due to consistently measured currents and clear diodic behaviour in various devices (Fig. 24a). This also deters the idea of a poorly defined junction, as during processing areas with different degrees of etched back $SiO_2$ were observed, but the measured data is consistent for various devices over the full sample. In accordance to *Ohm's Law* we expect to see the current increase with a factor of 4 as device size increases. However, when the data shown in figure 24b is observed a

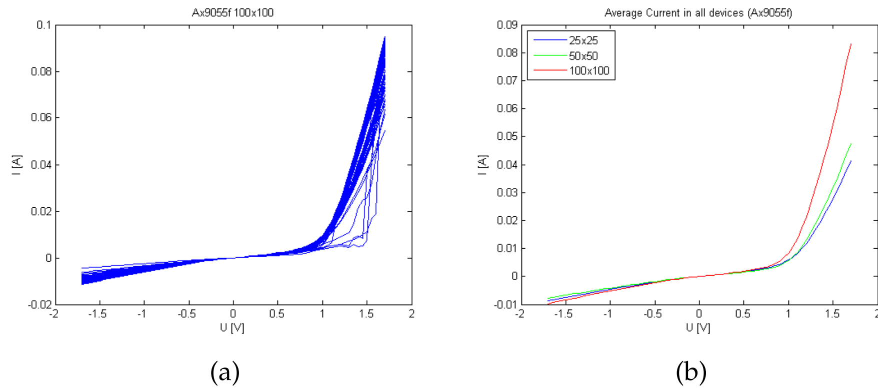



Figure 24: (a): The current measured through devices of the size 100x100 $\mu m^2$. The graph depicts data collected from 80 devices. (b): The average currents measured through different device sizes.

different behaviour is apparent (e.g. the current only scales with a factor of 2 between the 50x50 $\mu m^2$ and the 100x100 $\mu m^2$ devices). This behaviour indicates that the current does not only scale with the increasing number of nanowires connected to a larger device area, but also with some other factor, thus furthering the idea of leakage current.

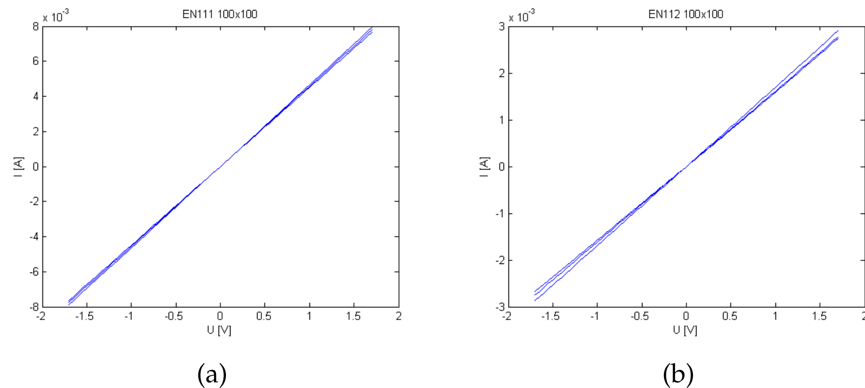
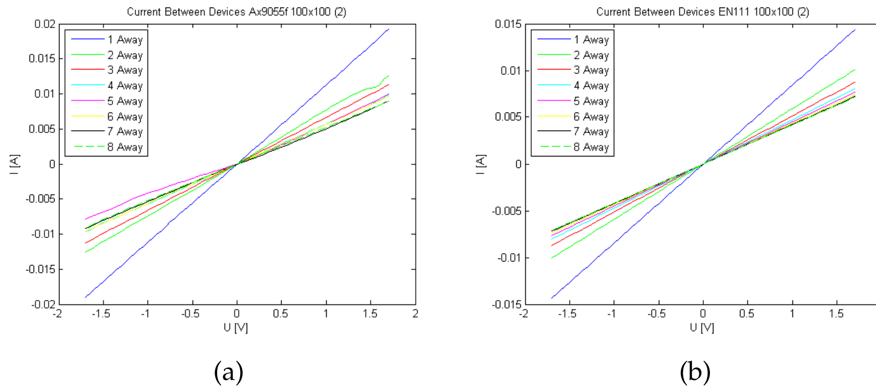



Figure 25: (a): The current measured through Si planar substrate with a layer of BCB spun on it. The BCB had been etched in a RIE system for 30 s ($R$ = 262 $\Omega$). (b): Si planar substrate, etched for 60 s ($R$ = 219 $\Omega$).

As the $SiO_2$ layer is preventing current from directly moving through the BCB from the top contact to the bottom contact, potential leakage current

through the BCB layer can not be measured in the sample. In parallel to the sample two planar samples with BCB spun on top of a Si substrate had been prepared (4.2). This was used to measure possible currents through the BCB layer. Measurements (Fig. 25) acted to strengthen the idea of a current through the BCB layer. The resistance for a 100x100 $\mu m^2$ device calculated from the obtained data was ~270 Ω, ~320 Ω for a 50x50 $\mu m^2$ device, ~310 Ω for a 25x25 $\mu m^2$ device, 262 Ω for EN111 and 219 Ω for EN112 (Appendix D), undermining the isolating properties of BCB (Appendix E).

Since the front contact is connected to the back contact through nanowires for the InP sample it is hard to distinguish any parallel current originating from the BCB layer from that originating from the InP nanowires. As such, measurements were also taken between neighbouring devices to see if the current scales with distance. Results can be observed in figure 26, and it is indicated that there is leakage between devices that can not be correlated with the nanowires' properties as the interdevice resistance is significantly lower than the advertised PΩ[31]. In order to rule out the possibility of the devices being physically in contact, through e.g. a thin metal layer, SEM investigation was carried out, revealing well defined devices, with the sought architecture, as can be seen in figure 5.2.

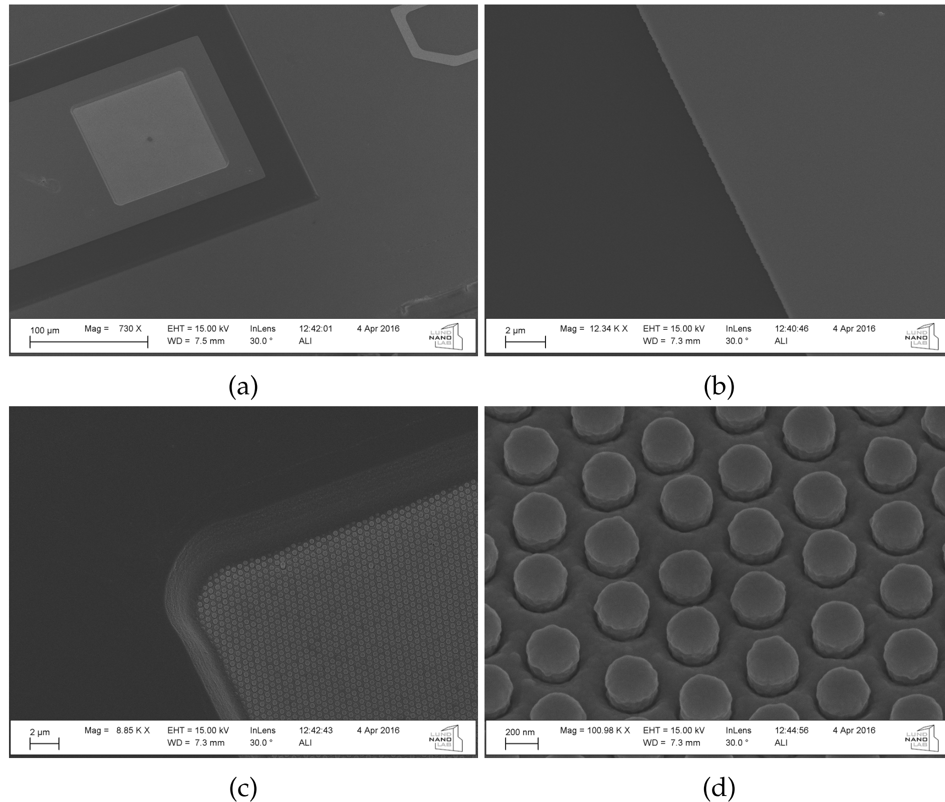



(a) (b)

Figure 26: (a): The current measured between devices on InP sample Ax9055f. (b): The current measured between devices on Si planar sample EN111 (without nanowires).

Suspicions regarding the devices being in contact with one another through the metal contact were thwarted by the well-defined metallic contacts observed (Fig. 27b). From the well-defined contacts, and the consistent interdevice resistance that was observed (Fig. 24a & 25), it was concluded

that further investigation of the isolating material had to be carried out, and it was concluded that a design void of BCB (4.3) could be used in order to determine if BCB was behind the poor electrical properties, or if the issue lied somewhere else.




(a) (b)

(c) (d)

Figure 27: (a): SEM image of a finished device on sample Ax9055f. (b): The interface of the metallic Au contact and the underlying BCB layer, deposited on top of the device. (c): The edge of the contact area of the device. (d): The ends of the nanowires inside the contact area of the device, covered with a metallic Au contact.

## 5.3 Further BCB Investigation

The device described in 4.3 (Fig. 15) showed similar behaviour to that presented for earlier device designs (5.2). Although the device displays a lower reverse current, the same is true for the forward case, see figure 28.

With a rectification ratio of ~8 it behaves on par with the device described in 4.2 (Fig. 10).

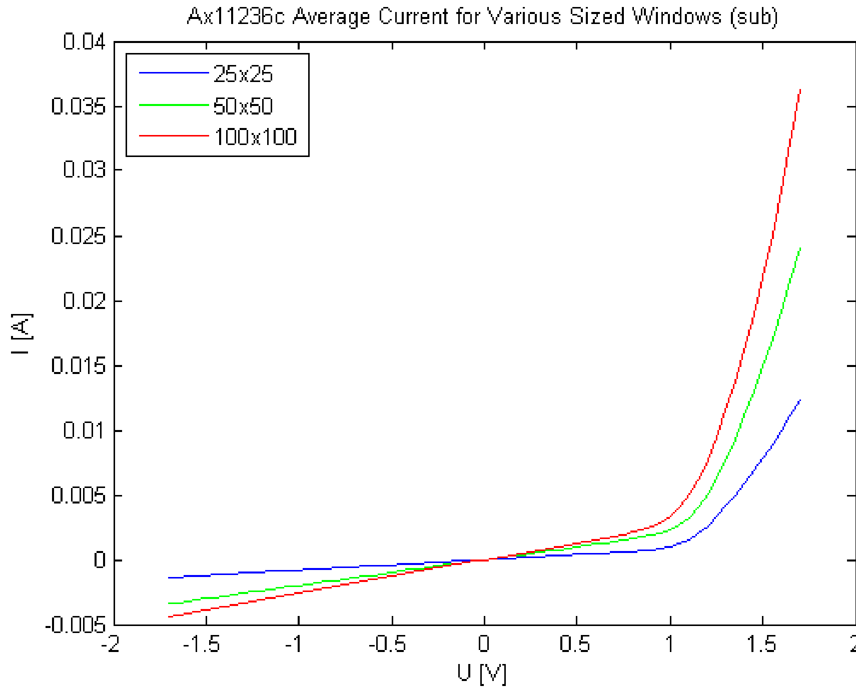


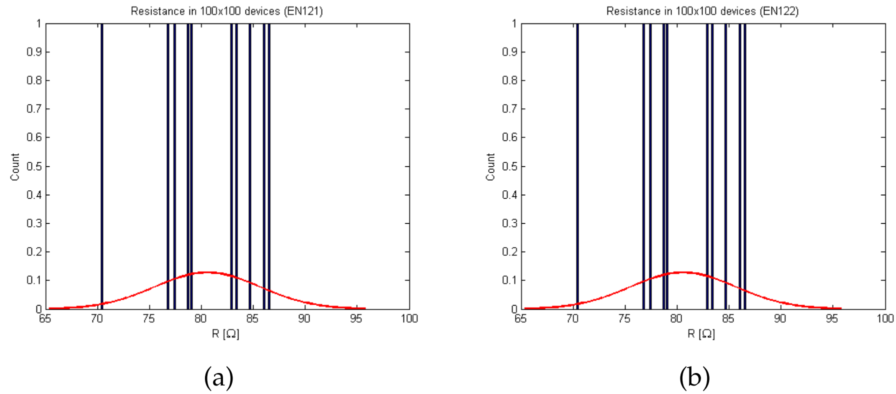

Figure 28: The average current through various devices on the sample described in 4.3 (Fig. 15).

In contrast to these discouraging results, the device shows a significant increase in parallel resistance at weak bias. For previous device design (4.2) a resistance of ~300 Ω for various device sizes was discovered (5.2). However, from the table below it is made clear that the unwanted parallel resistance has increased for the new design, showing promise for a BCB-free device design. The expected scaling of resistance with device size can also be seen, in contrast to that of the previous design presented in 5.2.

| | 25x25 $\mu m^2$ | 50x50 $\mu m^2$ | 100x100 $\mu m^2$ |
|---|---|---|---|
| R/Ω | $1.28 \cdot 10^3$ | 514.51 | 397.00 |

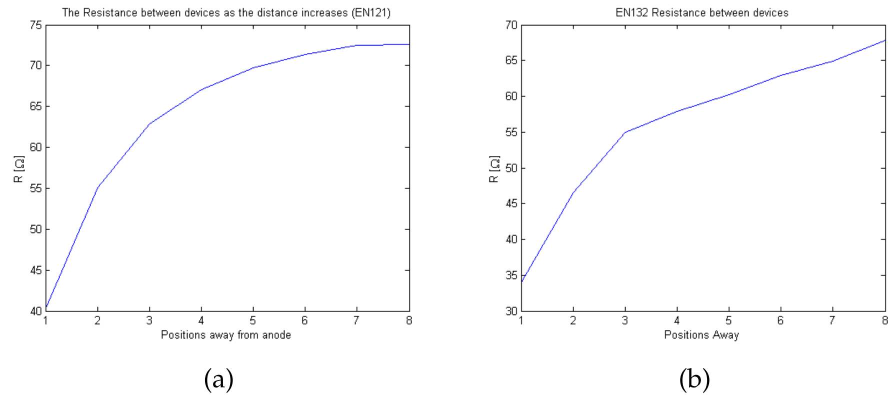
For the first run of processed planar samples (BCB on Si), one of the samples were exposed to UV-light, see 4.3. As is made clear by the data

presented in figure 29, the electrical properties of the device does not seem to differ between the two samples. It was thus concluded that BCB is unaffected by UV-light treatment, as claimed by the manufacturer.




(a) (b)

Figure 29: (a): The resistance in 100x100 devices in the sample treated with UV-light. The red line depicts the distribution of the individual measurements (black lines). (b): The resistance in 100x100 devices in the sample untreated with UV-light. The red line depicts the distribution of the individual measurements (black lines).




(a) (b)

Figure 30: (a): The resistance between devices in the old BCB as the distance increases. (b): The resistance between devices in the new BCB as the distance increases.

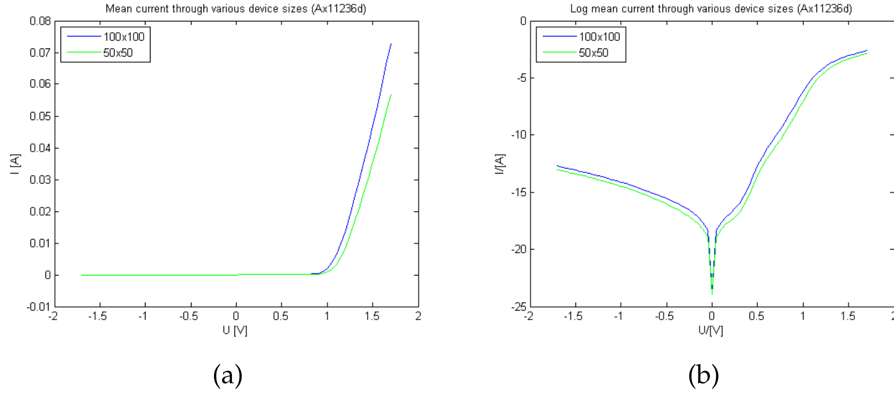
The second evaluation of the BCB was a comparison between an older batch and a newly supplied one, as the older batch may have deteriorated,

changing the properties of the resist. However, as can be seen in figure 30 the properties of the older resist is similar to that of the newer one. The data presented was measured between neighbouring devices in order to determine how the resistance scales with distance. The non-linear behaviour of the graphs displayed in figure 30 could be explained by the increase in the number of intermediate metal contacts, assuming a difference in resistance between the contacts and the BCB-layer.

Comparing the resistance between devices obtained from measurements (Fig. 30) with the vendor specifics[31], and estimating a distance of ~43 µm between contacts, it is evident that the obtained resistance of 35-40 Ω differs greatly from the expected 43 PΩ. This in conjunction with the difficulty of incorporating BCB in the actual device design deterred further use of BCB. If BCB would be considered in the future the contacting process could be questioned, as the in-house experience of BCB is that it is a good isolator. It is there for likely that the contacting method could contribute to the interdevice conductivity.

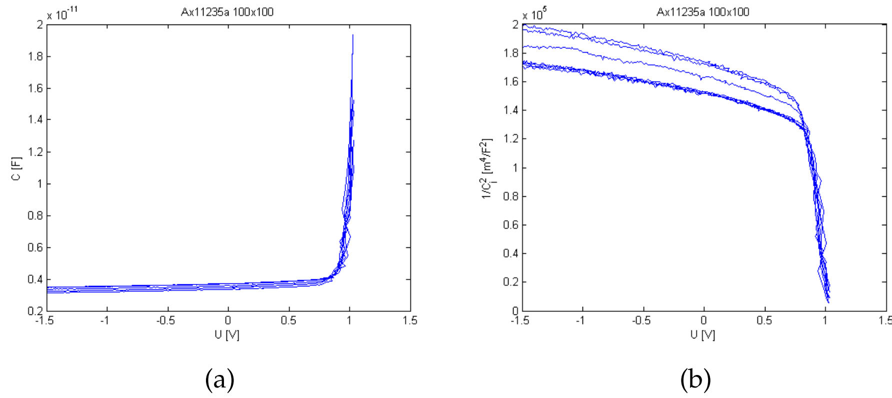
### 5.4 Measurements on a S1818-based device

Measurements on the devices with the design presented in 4.4 (Fig. 17) showed strongly rectifying behaviour ( Fig. 31). Sample Ax11235a and Ax11236e showed rectification (measured between -1.7 V and 1.7 V) in the order of $\sim 10^4$ for Ax11235a, and $\sim 10^6$ for Ax11236d. See Appendix G for full details. The ideality factor for various device sizes on the samples were found to be in the range of [4.28 5.29] for Ax11235a, [2.97 3.00] for Ax11236d, and [3.32 3.63] for Ax11236e (Appendix G).




(a) (b)

Figure 31: (a): The mean (calculated from 16 devices of each size) current through devices on sample Ax11236d under an applied bias. (b): The natural logarithm of the mean current through devices on Ax11236d.




(a) (b)

Figure 32: Measurements performed under an alternating bias of 20 mV, at a frequency of 1 MHz on sample Ax11235a. (a): The measured capacitance. (b) The normalized value of $1/C^2$.

From these samples it was possible to make CV-measurements, and it was quickly found that the devices behave as capacitors (Fig. 32). Since the doping level $N_A$ is calculated from the change in $1/C_j^2$ (Eq. 21), and it was found that the slope (Fig. 32b, extracted from -1 V to 0 V) varied for different frequencies of the applied alternating bias, different doping levels were found for different frequencies (Fig. 33). It was determined that the measuring setup *Probe station - Cascade 11000B* and *Agilent 4294A* were

calibrated for 1 MHz during initial calibration, and that measurements at lower frequencies were vastly inaccurate. For higher frequencies inaccuracy was still a factor, but minute in comparison to the error present for low frequencies. As such, further measurements were carried out at 1 MHz. It can also be seen by extending the linear trend of the reverse bias region in figure 32b that the built-in bias (Eq. 20) is well over any expected value. Although this raised concern it was decided to continue the investigation of the devices.

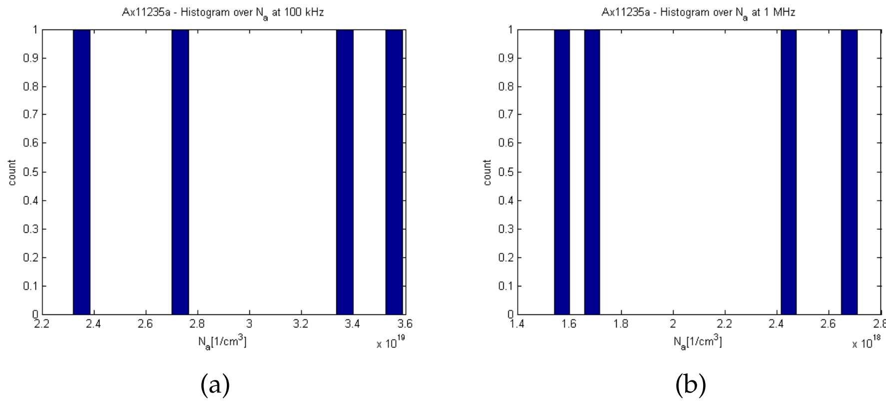



Figure 33: The calculated doping level $N_A$ from measurements at different frequencies. (a): 100 kHz. (b): 1MHz. A visible difference in obtained doping level (a factor ~10) were found, and credited to the equipment used. 1 MHz were later found to be better suited for measurements.

There was also the question regarding the effects of pits around certain wires, mentioned in 4.4, since disconnected wires would make the model used to calculate the capacitance from impedance measurements inaccurate, due to a change in area. Another factor that would have to be taken into account is the overexposure of the final S1828 resting layer, as the exposure could cause the actual contacting area to differ from the intended e.g. 100x100 $\mu m^2$. After inspecting the surface of the contacting area it was determined that the size was on par with the intended one, and slight changes to the model was made in order to make up for the infrequent appearance of disconnected wires (Fig. 34).

After improving the models slightly, the doping levels of the two samples *Ax11235a* and *Ax11236e*, *Ax11236d* will not be presented due to the discovery of large malfabricated areas in the sample, which were found to be in the range of $N_A = [7 \cdot 10^{18}, 9 \cdot 10^{18}]\ cm^{-3}$. A complete presentation of

the doping level data can be found in appendix H.

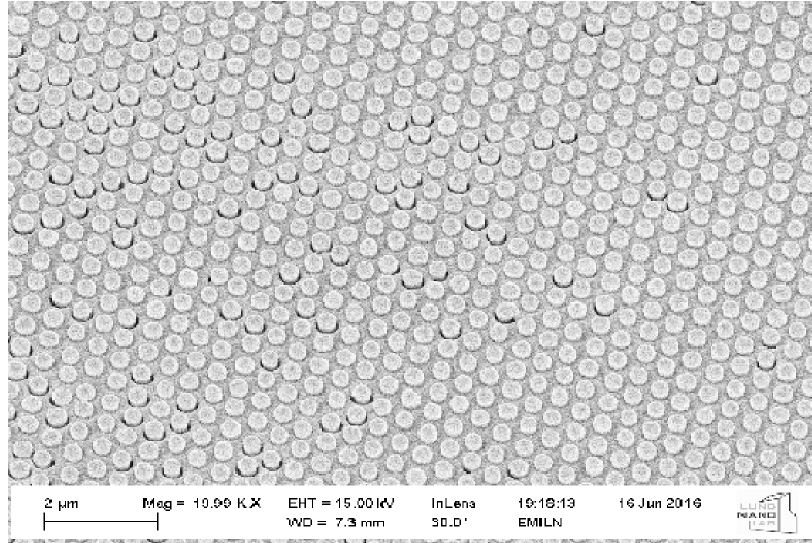
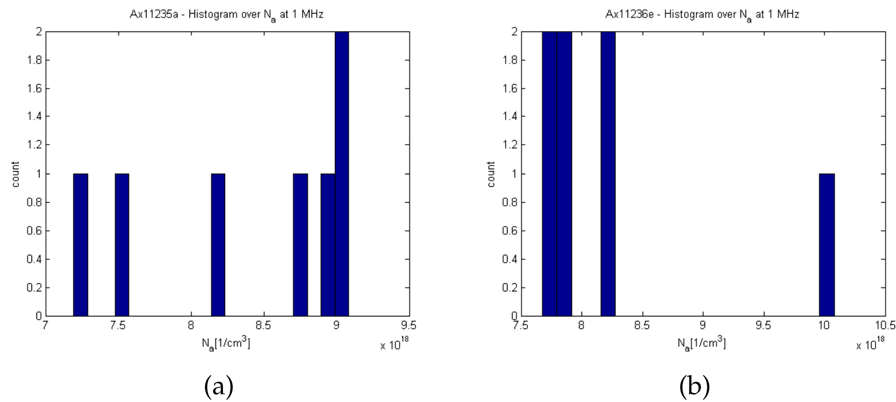



Figure 34: Nanowires thought to be disconnected from the circuit. Disconnected wires appear with dark circles around them.




(a) (b)

Figure 35: (a): $N_A$ for sample Ax11235a. (b): $N_A$ for sample Ax11236e.

From the data (Fig. 35) it is observed that the calculated doping level $N_A$ for the weaker doped Ax11236e is close to $8 \cdot 10^{18} cm^{-3}$ , and for Ax11235a it appears to be in the range $N_A = [7 \cdot 10^{18}, 9 \cdot 10^{18}]\ cm^{-3}$. The doping levels indicated by the measured data (Fig. 35) are a factor of ~100 higher than

the expected value of $\sim 10^{16}\ cm^{-3}$[37] (Appendix F). The difference in DEZn introduced during the growth of the nanowires (Appendix F) also suggests that there should be a larger difference between the two measured series (Fig. 35) than is seen. This causes questions to arise regarding the validity of the method. The validity and the course of action to determine said validity will be discussed in the *Outlook* portion (6) of this report.

# 6 Outlook

As the results presented in 5.4 suggest, the prospect of statistical measurements does not only seem to be a speculative idea, but rather it is supported by results converging towards a mean value, prominent in figure 35b. The high rectification of the devices presented in 4.4 and 5.4 also suggest that previous concerns regarding leakage through the insulating layer (5.3) is greatly deterred, supporting the idea that any current passing through the devices passes through the p-n junction.

However, that is not to say that the design is not open for improvements. As can be seen in figure 35 it is hard to distinguish the difference between the 'highly' doped sample (Fig. 35a) and the low doped sample (Fig. 35b), and as a first course of action further manufacturing of the same type of samples should be prioritized. An increased number of samples would allow for the determination of the possibility of distinction between high- and low-doping, and determine if the questionability that arises from the results presented in figure 35 are sample specific or general for the method.

The high doping level yielded is also worth investigating further. As the p-doping is on par with the expected doping level of the intended much higher n-doping [37], it would be of interest to investigate the accuracy of the measured doping level. The model used for calculating the doping level in the low doped p-doped region is explained in 3.4 and 3.5. Voltage and current compensations were also made in order to improve the calculated values. However, there is still the question regarding the accuracy of the parallel plate approximation, and as previously suggested [15] a numeric analysis [34] of the junction could be necessary in order to obtain the true value of the p-doped side of the nanowires. As any effect of a numerical analysis will be a shift in calculated values it should be prioritized to determine if different doping levels can be distinguished from each other (as discussed earlier), thus first determining if the method is suited for differentiating doping-levels before attempting to produce the true value.

In the event of the finalization of a method that works as intended it would be of great interest to once again look into the properties of BCB. During this diploma work it was concluded that BCB was not suited for the desired application (5.3). However, the properties discovered in BCB are in opposition to other in-house experiences as well as to what is advertised [31]. The device presented in 4.4 has a manufacturing time of 30+ h, in order to cut down on manufacturing time BCB is a suitable candidate for the insulating material. If a functional device utilizing BCB could be realized the manufacturing time could be cut down to ~15-20 h.

# 7 Summary

During the duration of this project four different device designs were used (the BCB-only device, and the devices displayed in: Fig. 10, Fig. 15, and Fig. 17) in order to investigate the prospect of CV-measurements on a p-n junction InP nanowire array as a possible evaluation method for the doping level in the weakly p-doped part of the nanowires. The aim was to create a measuring setup that would yield a high amount of data without the need of unnecessarily time-consuming methods. The basis of the design lies with the nanowire array, consisting of 2 μm long wires, with a diameter of 200 nm. The substrate as well as the bottom part of the nanowires is p-doped and the top segment of the nanowires are n-doped. An insulating layer is then used in order to prevent current from passing between the wires, as well as from the top of the sample to the bottom (without passing through the nanowires). A metallic layer is applied to the top of the sample, acting as the top contact, and the growth-substrate acts as the back contact.

As previous project had had poorly rectifying devices, a sign of unwanted leak current. The properties of an old system were investigated, trying to determine if the problem was in the nanowires or the surrounding material. Through single-wire contacting it was shown that the nanowires had good individual rectification. However, problems arose when measurements were carried out on the old devices (manufactured during the previous project[15]), and it was discovered that the devices were barely rectifying.

An isolating $SiO_2$ layer was thus introduced into the design in an attempt to isolate the wires further. From IV-measurements on the new devices (Fig. 10) it was shown that also this design led to poorly rectifying devices. The fact that the resistance between neighbouring devices were shown to be low, ~300 Ω instead of in the order of PΩ, supported the idea that the BCB layer could be the reason behind the poor performance of the devices.

Thus a design stripped of BCB was used in order to see if good rectification could be achieved for devices void of BCB. A number of planar samples with only a layer of BCB, without nanowires, were also made, these in order to be able to determine if the BCB was conductive. From the planar samples it was quickly realized that the BCB was conductive. Attempts to see if the BCB was affected by UV-light treatment was also carried out, showing no difference between UV-light treated BCB and non-treated BCB. From the real device (the one void of BCB, but with nanowires) a poor rectification was obtained, but this was later explained due to a machine failure during early ALD treatment.

As BCB had been deemed unsuitable for the application, a new device design was drawn out, notably different from the previous device designs. The new design incorporated the idea of a protecting $SiO_2$ layer that had been used previously, but the BCB layer was instead replaced by a S1818 layer. It had during an earlier project been shown that S1818 tends to crack during processing, and that is the main reason experiments with BCB had been carried out, and in order to circumvent this problem the S1818 was patterned in order to create smaller areas covered with the resist. This was done as it was thought that it would reduce any induced stress in the resist, thus preventing the resist from cracking during processing. The design was then finished off with a S1828 resting layer and a metal contact layer. Devices created out of this design was found to have a rectification ration (measured between -1.7 V and 1.7 V) in the order of $10^4$-$10^6$, and it was decided that this was sufficient in order to allow for CV-measurements.

From CV-measurements it was deduced that the doping level of the differently doped samples were somewhere in the range of $\sim 10^{19}\ cm^{-3}$, but accuracy of these measurements were questioned, as the calculated doping level seemed to change with the frequency of the applied bias. This was later determined to be due to inaccuracy of the measuring tool for frequencies under 1 MHz, and the stable measuring frequency was determined to be at 1 MHz. Traces of disassociated wires were also found on some devices, and the calculated values were compensated for this.

The obtained values for the doping levels are questionable as they suggest that the weak p-doping is on par with the high n-doping. It is thus advised that further improvement on the model is done, and that more data on different devices are collected in order to determine if this method is suited for the intended purpose. As this report suggest, there are promising signs that the method could be used, as comparable results of $N_A$ are found over different devices and samples. However, it is still to early to say if the method works for doping evaluation in nanowires.

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# A COMSOL and nanoHUB simulation

Simulated results for I-V measurements over a InP nanowire with a 1 μm long p-doped ($10^{16}$ cm$^{-3}$) segment and a 1 μm long n-doped ($10^{19}$ cm$^{-3}$) segment. The difference in the turn-on voltage in the graphs below compared to the measured data presented in section 5 could be credited to the ideality factor differing from the ideal case of 1. For the simulations used for the graphs below a ideality factor of 1 was used, and for the measured data in section 5 an ideality factor of >2 was found.

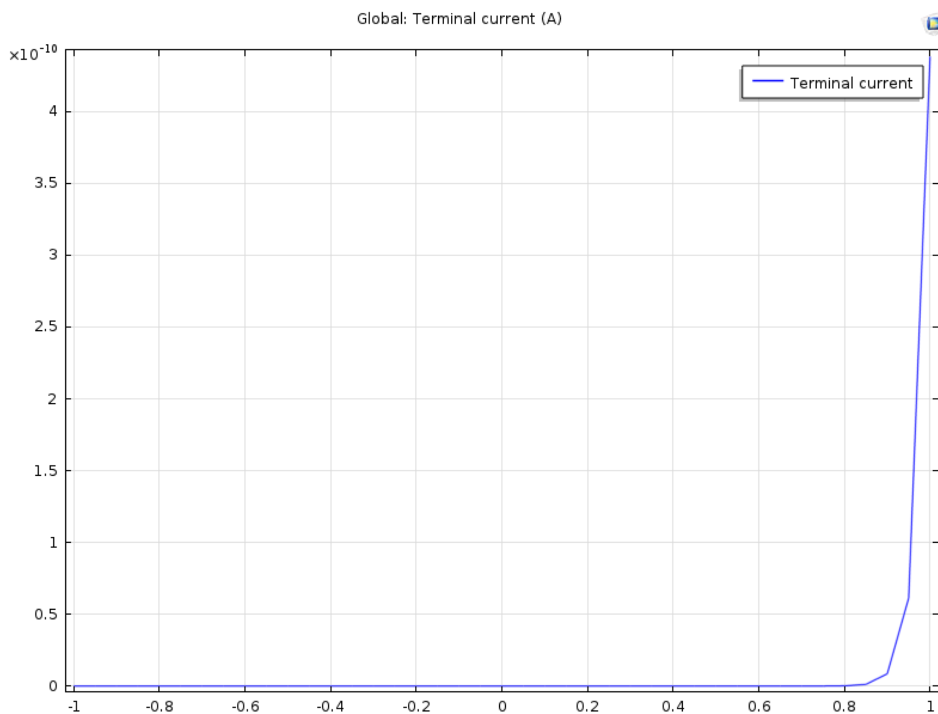



Figure 36: The I-V characteristics of an InP nanowire. Simulation ran through *COMSOL: Multiphysics 5.0*.

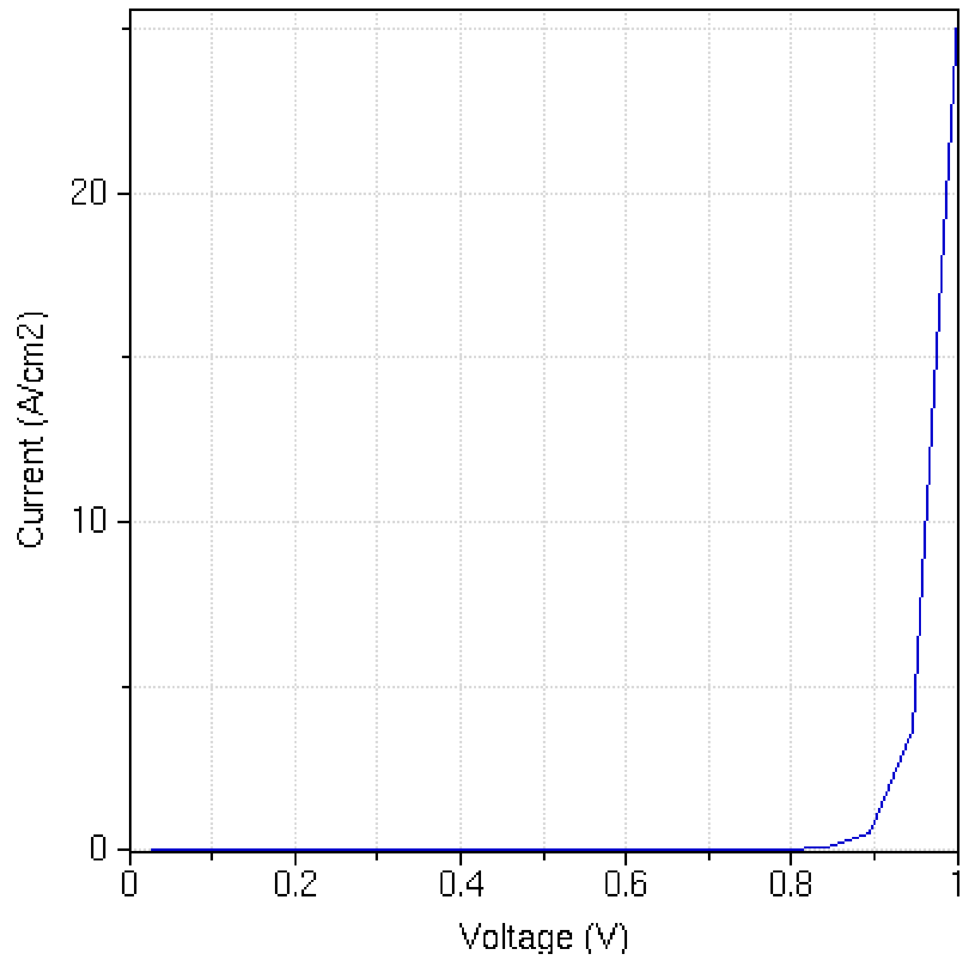



Figure 37

Figure 38: The I-V characteristics of an InP nanowire. Simulation ran through *nanoHUB*[19].

## B Rectification Ratio and Ideality Factor of the Nanowires

Table of rectification ration and ideality factor acquired from nanowires grown on substrate Ax9055a is shown below. The measurement index indicates the location of the field the measured nanowire was located in, and the two probes used. All measurements were made on the substrate with four contacts made to each nanowire (see 4.1), with bias sweeping from -1 V to 1 V.

| **Measurement** | **Rectification Ratio** | **Ideality Factor** |
|---|---|---|
| 1(13) | 27 | 4.2952 |
| 1(23) | 45 | 4.0488 |
| 3(14) | 5 | - |
| 3(23) | 1 | - |
| 3(24) | 7 | 4.8408 |
| 5(13) | 45 | - |
| 9(23) | 6 | 5.7405 |
| 13(13) | 388 | 4.1854 |
| 13(14) | 253 | 4.8080 |
| 15(23) | 0.2 | 12.0778 |
| 17(24) | 3 | 4.8576 |
| 23(13) | 197 | 3.7581 |
| 23(14) | 162 | 3.9200 |

Due to deterioration between measurements, only three measurements were thought to be reliable, they are presented in the table below. The rectification ratio and ideality factor were calculated from an I-V measurement series, were the bias was swept from -2.5 V to 2.5 V.

| **Measurment** | **Rectification Ratio** | **Ideality Factor** |
|---|---|---|
| 1(13) | $4.9258 \cdot 10^3$ | 4.8368 |
| 1(23) | $2.2302 \cdot 10^5$ | 5.0225 |
| 5(13) | $5.3280 \cdot 10^5$ | 4.9112 |

As the measured ideality factor is found to be >2 is could be (as discussed in 5.1) creddited to e.g. nonohmic contacts and/or recombination at the p-n junction.

## C RTP Baking Recipe

| Time/min | Process | Temperature/°C |
|---|---|---|
| 30 | ramp | 25 |
| 2 | vacuum | 25 |
| 15 | ramp | 100 |
| 15 | soak | 100 |
| 15 | ramp | 150 |
| 15 | soak | 150 |
| 60 | ramp | 250 |
| 60 | soak | 250 |
| 60 | cool | 25 |

# D Parallell Resistance Measurements

From measurements taken for sample Ax9055f, EN111 and EN112, resistances for low currents were determined. The mean calculated values are presented in the table below.

| Sample | 25x25 | 50x50 | 100x100 |
|---|---|---|---|
| Ax9055f | 292 Ω | 288 Ω | 262 Ω |
| EN111 | 334 Ω | 365 Ω | 219 Ω |
| EN112 | 610 Ω | 598 Ω | 616 Ω |

The full data over resistance between -0.5 V and 0.5 V for all measured device on Ax9055f are presented in the graphs below.

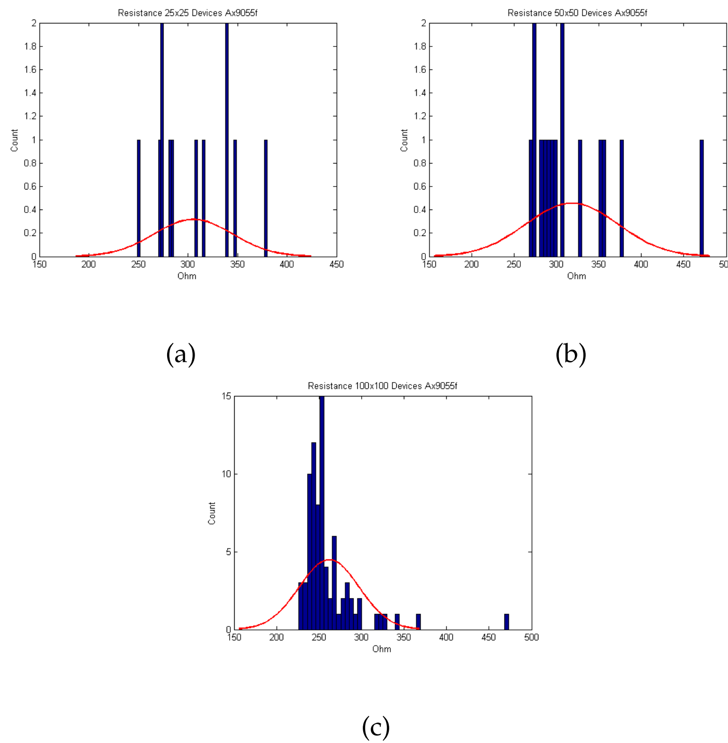



Figure 39: (a): Resistance between -0.5 V to 0.5 for device size 25x25 $\mu m^2$. (b): Resistance for device size 50x50 $\mu m^2$. (c): Resistance for device size 100x100 $\mu m^2$. The blue lines depicts individual measurements, and the red line is the standard distribution of said measurements.

# E Cyclotene 3000 Series Resins

Tables obtained from DOW Chemical Company's datasheet[31].

Table 1. Thermal, Electrical and Mechanical Properties of CYCLOTENE 3000 Series Resins

| Property | Measured Value |
|---|---|
| Dielectric constant | 2.65 at 1-20 GHz |
| Dissipation Factor | 0.0008 |
| Breakdown Voltage | $5.3 \times 10^{6}$ V/cm |
| Leakage Current | $6.8 \times 10^{-10}$ A/cm$^2$ at 1.0 MV/cm$^2$ |
| Volume Resistivity | $1 \times 10^{19}$ Ω-cm |
| Thermal Conductivity | 0.29 W/m°K @24°C |
| CTE | 42 ppm/°C at 25°C |
| Tensile Strength | 87 ± 7 MPa |
| Tensile Modulus | 2.9 ± 0.2 GPa |
| Elongation | 8 ± 2.5 % |
| Poisson's Ratio | 0.34 |
| Residual Stress on Si | 28 ± 2 MPa at 25°C |
| Tg | > 350°C |
| Moisture Absorption | < 0.2% |

Table 3: Thickness after cure (in microns) versus spin speed.

| Spin Speed (RPM) | CYCLOTENE 3022-35 | CYCLOTENE 3022-46 | CYCLOTENE 3022-57 | CYCLOTENE 3022-63 |
|---|---|---|---|---|
| 1000 | 2.26 | 5.46 | 13.8 | 26.2 |
| 1500 | 1.84 | 4.39 | 10.7 | 19.9 |
| 2000 | 1.59 | 3.76 | 9.04 | 16.5 |
| 2500 | 1.43 | 3.35 | 7.97 | 14.4 |
| 3000 | 1.30 | 3.05 | 7.21 | 12.9 |
| 3500 | 1.21 | 2.82 | 6.65 | 11.8 |
| 4000 | 1.13 | 2.63 | 6.20 | 10.9 |
| 4500 | 1.07 | 2.48 | 5.84 | 10.2 |
| 5000 | 1.01 | 2.35 | 5.55 | 9.64 |

## F Nanowire Growth Parameters

Both samples (Ax11235 and Ax11236) were grown at a growth temperature of 440°C, under a $PH_3$ molar fraction of $6.9 \cdot 10^{-3}$ and a TMIn molar fraction of $7.3 \cdot 10^{-5}$. HCl at a molar fraction of $4.6 \cdot 10^{-5}$ was used to suppress radial growth.

The table below descripts the doping conditions of the growth chambers for the different segments.

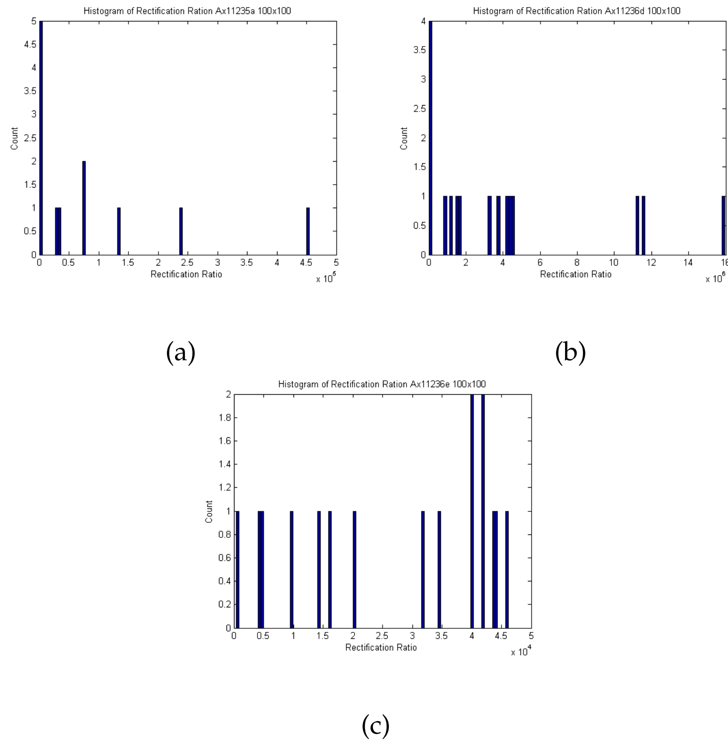
| | **Ax11235** | **Ax11236** |
|---|---|---|
| **p-segment** [μm] | 1 | 1 |
| **DEZn molar frac** | $6.3 \cdot 10^{-7}$ | $2.1 \cdot 10^{-7}$ |
| **n-segment** [μm] | 0.9 | 0.9 |
| **TESn molar frac** | $4.7 \cdot 10^{-5}$ | $4.7 \cdot 10^{-5}$ |

# G Ideality Factor and Rectification - Final Processing Cycle

The table belows shows the ideality factor calculated from the mean IV-values for various device sizes on three different samples.

| | **25x25** | **50x50** | **100x100** |
|---|---|---|---|
| **Ax11235a** | 4.2758 | 4.8911 | 5.2905 |
| **Ax11236d** | | 2.9715 | 2.9984 |
| **Ax11236e** | | 3.3184 | 3.6270 |

The graphs below show the rectification of 100x100 $\mu m^2$ devices on three different samples, the calculation was done for values at -1.7 V and 1.7 V.




(a) (b)

(c)

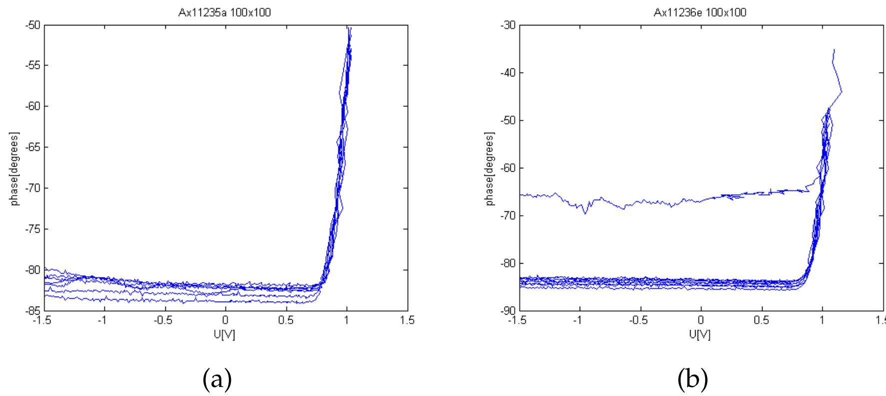
Figure 40: (a): Rectification of devices on Ax11235a. (b): Rectification of devices on Ax11236d. (c): Rectification of devices on Ax11236e.

## H Doping Evaluation of Ax11235a and Ax11236e

The table below depicts the doping level found in the weakly p-doped side of the nanowires. Measurements on 7 different devices are depicted.

| $N_A$ $[10^{18}cm^{-3}]$ | |
|---|---|
| **Ax11235a** | **Ax11236e** |
| 9.0847 | 7.7855 |
| 8.2096 | 7.8439 |
| 7.5508 | 8.2690 |
| 9.0664 | 8.2507 |
| 7.1936 | 10.0080 |
| 8.9696 | 7.6743 |
| 8.7758 | 7.8155 |

As the ideal capacitor has a phase shift of -90°, the phase was checked in order to determine the validity of the measurements. A phase less than $-45°$ is deemed sufficient.




(a) (b)

Figure 41: (a): Phase found in Ax11235a. (b): Phase found in Ax11236e.

# I Processing Summery

The following table describes the processing method used for the design presented in 4.2.

| Design II |
|---|
| Nanowire Au seed particle removed:<br>3x(20 s $H_2SO_4$ 1:10 + 10 s DIW + 20 s KI/$I_2$ + 10 s DIW) |
| Cleaned backside with IPA + rinse in Acetone for 1 min + 1 min IPA |
| ALD: 40-50 nm $SiO_2$ + 5 nm $Al_2O_3$ |
| Rinsed in Acetone for 1 min + 1 min IPA |
| Spin-coat S1818 @ 3000 rpm for 60 s, soft baked for 90 s @ 115°C |
| RIE, 15 sscm $O_2$, 50 W, 2600 s<br>(600 + 500 + 300 + 300 + 300 + 300 + 200 + 300 + 100) |
| Cleaned backside with IPA |
| Etch $SiO_2$: 227 s BOE 1:10 JT Baker + 1 min DIW (non etched $SiO_2$ found) |
| RIE, 15 sscm $O_2$, 50 W, 750 s (300 + 200 + 250) |
| Etch $SiO_2$, 45 s BOE 1:10 JT Baker + 1 min DIW |
| Strip S1818: 1 min Acetone + 1 min IPA |
| Clean backside with IPA + rinse in Acetone for 1 min + 1 min IPA |
| Spin-coat BCB @ 5000 rpm for 60 s, soft baked for 90 s @ 120°C |
| Hard-baking BCB: RTP, 250°C for 1 h (total recepie time: 4 h) |
| Spin-coat S1828 @ 3000 rpm for 60 s, soft baked for 90 s @ 115°C |
| UV-lithography: 2x 10 s exposure |
| Develop: 2 min in MF319 + 1 min DIW |
| RIE, 10 sscm $CF_4$, 70 sscm $O_2$, 150 W, 85 s (20 + 20 +10 + 15 + 10 + 10) |
| Strip S1828: 1 min Acetone + 1 min IPA |
| Clean backside with IPA |
| Ecth natural oxide: 1 min $H_2SO_4$:$H_2O$ 1:10 + 1 min DIW |
| Sputter 206 Å Ti + 2005 Å Au |
| Clean backside with Acetone + rinse in Acetone for 1 min + 1 min IPA |
| Spin-coat S1828 @ 3500 rpm for 60 s, soft baked for 90 s @ 115°C |
| UV-lithography: 2x 10 s exposure |
| Develop: 2 min MF319 + 1 min DIW |
| Au-etch: 2 min KI/$I_2$ + 1 min DIW<br>Residue-etch: 10 s BOE 1:10 JT Baker + 1 min DIW |
| Strip S1828: 1 min Acetone + 1 min IPA |