

MASTER THESIS

Development of Epitaxial Lift-Off to form GaAs nanowire array membranes

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Ny metod för att skapa billiga, effektiva och transparenta solceller

Den teoretiska gränsen för effektivitet i konventionella solceller av kisel är nästan nådd och solceller i material med högre teoretisk effektivitet blir i praktiken alldeles för dyra för att stå till buds för allmänheten. Hur skulle man göra för att fortsätta utvecklingen av effektivare solceller utan att de blir alldeles för dyra?

I en tid av global uppvärmning finns det ett stort behov av att utveckla effektivare och billigare solceller. Ett hett forskningsområde just nu är att tillverka solceller av så kallade nanotrådar, detta är nanometerstora kristaller som har visats vara väldigt lovande för att tillverka solceller med. En av anledningarna till att nanotrådar är så intressanta, är att det krävs väldigt lite material för att tillverka en nanotrådssolcell. Detta gör att solcellerna med nanotrådar kan bli betydligt billigare än konventionella solceller, utan att de för den sakens skull blir mindre effektiva.

Det är svårt att producera en solcell som ensam tar hand om hela solljusspektrat. En ensam solcell är egentligen bara som mest effektiv i en begränsad del av solljusspektrat. En möjlig strategi för att komma runt detta, är att helt enkelt placera två solceller ovanpå varandra som tar hand om var sin del av solljusspektrat. För att detta ska fungera i praktiken krävs det att den övre solcellen är transparent för det ljus som ska generera elektricitet i den undre cellen. Skulle allt ljus fastna i den övre cellen, finns det ju ingen anledning att ha den undre cellen.

Detta ställer stora krav på den övre solcellen, eftersom solceller normalt sett måste produceras på ett substrat som blockerar en stor del av ljuset. För att åtgärda detta behöver själva solcellen avlägsnas från detta substrat. Detta är inte trivialt då solcellen i sig själv är väldigt tunn och ömtålig. En annan potentiell fördel med att substratet inte inkluderas i den slutgiltiga solcellen är att substratet då kan återanvändas för mer solcellsproduktion.

Metoden som avlägsnar solcellen från substratet måste vara väldigt skonsam mot solcellen. En metod som uppfyller detta, är så kallad epitaxiell lift-off. Tanken med denna metod är tillverka ett lager under själva solcellen som ska användas för att lyfta bort den. Detta lager måste självklart vara kompatibelt med den kommande solcellstillverkningen, då tillverkningsprocessen är väldigt känslig.

Epitaxiell lift-off har visat sig vara framgångsrik för tillverkning av konventionella solceller, men har aldrig tidigare används för att tillverka transparenta nanotrådssolceller. Fördelarna med både nanotrådar och epitaxiell lift-off är att båda metoderna kräver väldigt lite material. Om epitaxiell lift-off kan kombineras med nanotrådssolceller, skulle slutresultatet kunna bli en väldigt billig och dessutom transparent solcell.

De första stegen mot denna transparenta nanotrådssolcell har nu tagits genom att utveckla de lager som krävs för att epitaxiell lift-off ska kunna ske för en nanotrådssolcell.

Erik Svensson

Abstract

Epitaxial lift-off (ELO) was developed as a method to create nanowire array membranes, with the intent to pave the way for tandem solar cells. Ultimately this thesis project focused only on growing and characterizing the ELO layers on (111)B oriented GaAs substrates with MOCVD, as this process step is not thoroughly understood in literature.

In this thesis, temperature and V/III ratio dependence for planar GaAs and AlGaAs MOCVD growth on (111)B oriented substrates is shown. Specular GaAs growth is shown V/III <20 and a temperature >800°C on exactly (111)B oriented GaAs substrates. To lower the GaAs growth temperature, 2° miscut substrates were necessary. Specular Al_{0.51}Ga_{0.49}As on exactly (111)B oriented wafers is demonstrated at 13.2 V/III and 800°C.

Although it is not demonstrated in this thesis, the author believes that epitaxial lift-off of nanowire membrane is achievable.

Preface

Thanks to Ingvar, my supervisor at Sol Voltaics, for your enthusiasm and support during this project. Thank you especially for being very patient and giving me the independence required to truly grow during this project.

Thanks to Andreas, Cecilia, Christian, Damir, James, Omid and Yuxuan, the rest of the Cell Engineering Team at Sol Voltaics, for being awesome in general.

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1 Introduction

1.1 How to read this thesis

This a master thesis project in solid state physics, the project aims to solve the following problem: Can the epitaxial lift-off-technique be used on nanowire samples to form GaAs nanowire array membranes? In writing this thesis I have chosen to deviate somewhat from the standard report format in favor of writing the thesis as a problem solving formula on a larger scale. The main reason for writing the thesis this way is to emphasize the engineering process of solving problems. Focus is put on why and how decisions were made, rather than just showing the solution. This thesis has the overall form:



Figure 1.1: Outline of this thesis using the “problem-solving-flow”. It is also stated which section to refer to for each stage of the problem solving.

As this report is focused on the problem solving process, I have included several errors that were made during the project. I have also included several of the problems that were encountered, which are not strictly related to the project. I hope this will make the reading of this thesis more interesting for the aspiring engineer.

1.2 Background and motivation

In a time of climate change the necessity to develop highly efficient low cost solar cells becomes great. One promising candidate for such high efficiency solar cells are nanowire solar cells [1]. Åberg et al in Sol Voltaics [2] has demonstrated a GaAs nanowire array solar cell with 15,3 % efficiency at 1 sun.

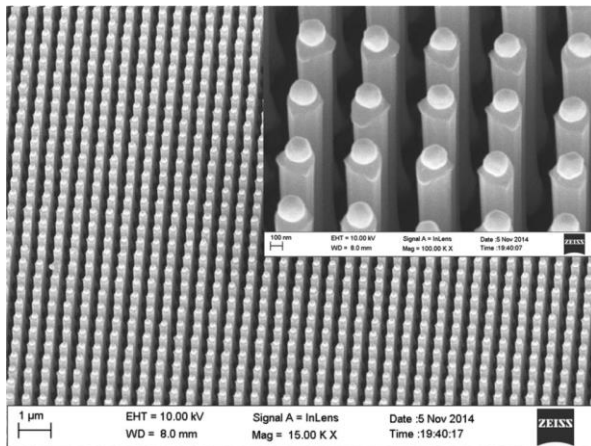


Figure 1.2: Image of the nanowire array, GaAs nanowires with AlGaAs shell. Image from [2].

Nanowire solar cells are attractive since their properties can be finely tuned and less expensive III-V material is required to produce nanowire solar cell as compared to their two-dimensional layered counterparts.

To further the work of Åberg et al, the next step is to remove the nanowires from the substrate they were manufactured on and put the nanowires in an elastic polymer. Not using the bulk substrate in the end product offer several advantages:

1. III-V material such as GaAs is prohibitively expensive, if the substrates are not consumed manufacturing process, production costs can be significantly reduced.
2. Photons captured by the substrate in a nanowire device do not participate in generating electricity. Thus, ideally, the nanowire device without the substrate can be made transparent to all photons not generating electricity. This allows for solar cells created this way to be put in tandem with existing silicon solar cell technology. The GaAs nanowire solar cell would

generate electricity from the high energy photons and the silicon cell underneath generates electricity from the low energy photons. This would make the overall device much more effective.

3. GaAs substrates are rigid, if bulk substrate is removed, the final solar cell can be made flexible which allows for more applications.
4. A solar cell without the substrate would be significantly lighter, making it more attractive for extra-terrestrial applications.

Currently there are no well-established methods for separating nanowires from the growth substrate. One existing technique is to mechanically peel the nanowires from their substrate. This technique engulfs the nanowires in elastic material which is then peeled from the substrate together with the nanowires. This method is very limited by nanowire morphology. If the wires are too short, too thick or are placed too tightly, this technique becomes unreliable, due to the mechanical force required to remove the nanowire containing polymer. Either the nanowires are not entirely peeled from the substrate, or the mechanical force applied damages the nanowires or the polymer itself. The nanowires are also damaged if they do not break cleanly at exactly the interface between substrate and nanowire. The polymer film is damaged if the nanowires are strongly attached to the substrate and the force needed to peel the nanowire-containing film from the substrate becomes so great the film itself starts tearing.

As mentioned above, mechanical peeling puts restrictions on the morphology of the nanowires. Changing the morphology of the nanowires is not easy and requires heavy development. The list of nanowire properties that must be precisely tuned to create nanowires is already fairly extensive [2], it is not desirable that the post-processing, e.g. mechanical peeling, introduces more properties that must be finely tuned.

To circumvent the need to redevelop high efficiency nanowires a different technique can be used. Instead of removing the nanowires from the substrate, the substrate can be removed from the nanowires. Epitaxial lift-off (ELO) would achieve this. The basic principle of epitaxial lift-off is to manufacture a sacrificial layer underneath the device, which can be removed chemically. As the sacrificial layer, which is between the actual device and the substrate, is removed the substrate and the device are separated from each other. Chemical separation in this fashion is attractive since it bypasses all the above mentioned problems with mechanical peeling. Nanowires with any thickness, length and pitch can be removed from the substrate using this technique.

1.3 Process flow of nanowire ELO

As the scope of this thesis is large, it becomes important to fully define the project and set up specifications that need to be met in order to achieve nanowire ELO.

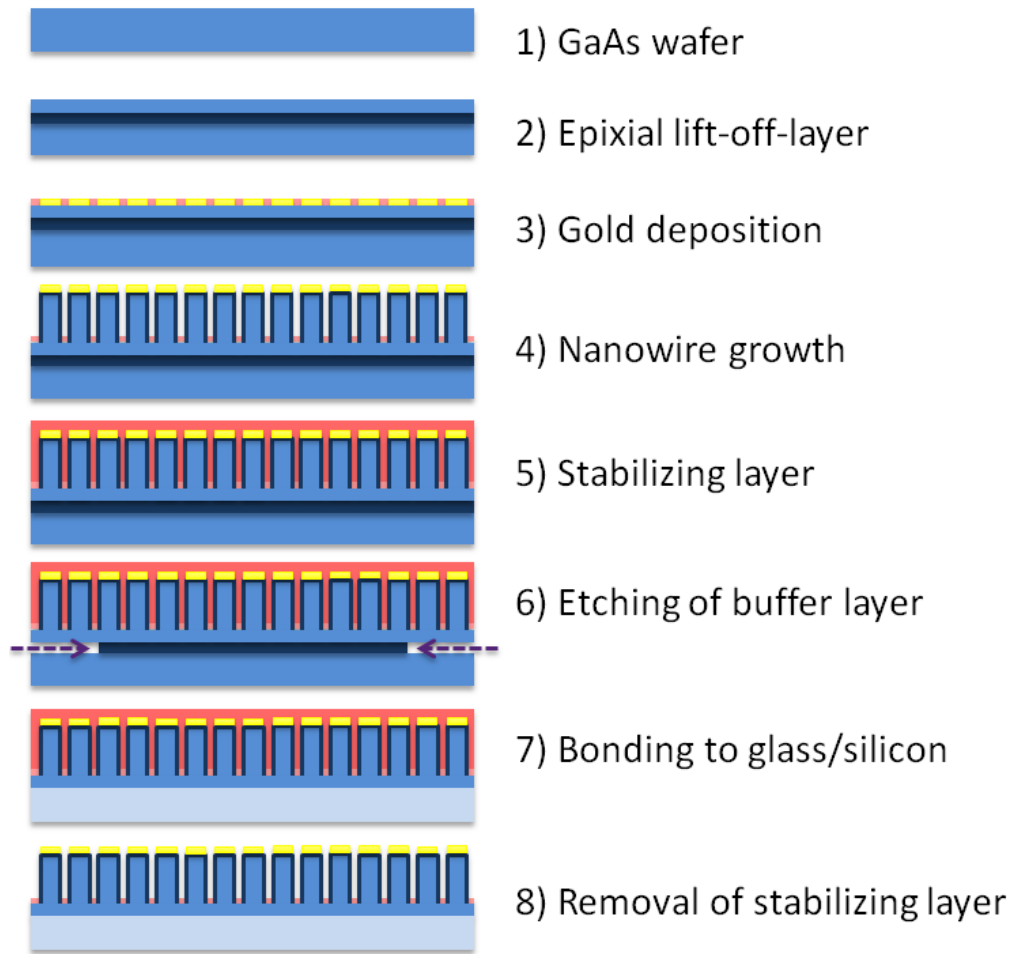


Figure 1.3: Project process flow.

Figure 1.3 outlays the necessary steps for nanowire ELO.

1. Epi ready wafer from manufacturer
2. Growth of epitaxial lift-off layers
3. Patterning with gold nanowire seeds.
4. Growth of nanowires
5. Adding of stabilization layer
6. Etch of sacrificial layer
7. The “device” is bonded to a glass or silicon wafer.
8. The stabilizing layer is removed.

As the goal of this thesis is limited to nanowire ELO, the actual integration of the nanowires into a solar cell is not included in this thesis work.

As will be further discussed in section 3, previous work and literature, most of the steps in the process flow are well-established known techniques. However, growing planar layers on (111)B oriented substrates poses a challenge and is not well covered in literature. As this is the only missing piece of the process flow and has not been done before, growing the epitaxial lift-off-layers will be one of the primary focuses of this thesis.

1.4 Restrictions on the project

It is preferable to develop a growth process that is compatible with current available equipment. The available equipment is an Aixtron 200/4 low pressure horizontal cold wall reactor with maximum temperature capability of 750°C.

The end result must be compatible with previous research from Sol Voltaics, i.e. nanowires that are to be grown must use be gold catalyzed. The gold deposition process must be an imprint process in specific arrays. These restrictions will be discussed more later in the thesis.

2 Understanding MOCVD

As this project is primarily centered on crystal growth development in metal-organic chemical vapour phase deposition (MOCVD), this concept is critical and warrants its own section.

Metal-Organic Chemical Vapor Deposition is a chemical vapor deposition technique normally used to produce thin layers of single-crystalline films. The atoms, which are to be incorporated into the crystal, are supplied into reactor in gaseous precursor form. The precursors are molecules containing the wanted atoms bonded with ligands, which enables vaporization of the precursors. Examples of the precursors are hydrides such as arsine (AsH_3) and organometallics such as trimethylgallium (TMGa), triethylgallium (TEGa) and trimethylaluminium (TMAI). When the precursors enter the reactor they decompose through a series of reactions both in the vapor phase and on the substrate surface. The difference between TMGa and TEGa is that the decomposition energy for TEGa is lower than TMGa since the ligands are more loosely bound to the gallium.

Thermodynamics is the major driving force for MOCVD growth. As the gas enters the heated reactor, it expands, supersaturating the vapor phase creating a difference in chemical potential between the substrate and the vapor. This difference in chemical potential is the driving force for precursor diffusion toward the substrate. The precursors decompose into their main atoms which physisorb to the substrate, becoming so called adatoms. The adatoms are only loosely bound to the surface and may “hop” between available states on the surface, the “hopping” is usually referred to as Brownian motion. They may hop on the surface until they find a state where they are more firmly bound to the crystal lattice or desorb to the vapor phase, the total length of the Brownian motion is called the migration length. Since the desorption rate is low, MOCVD is a mostly a one-way process.

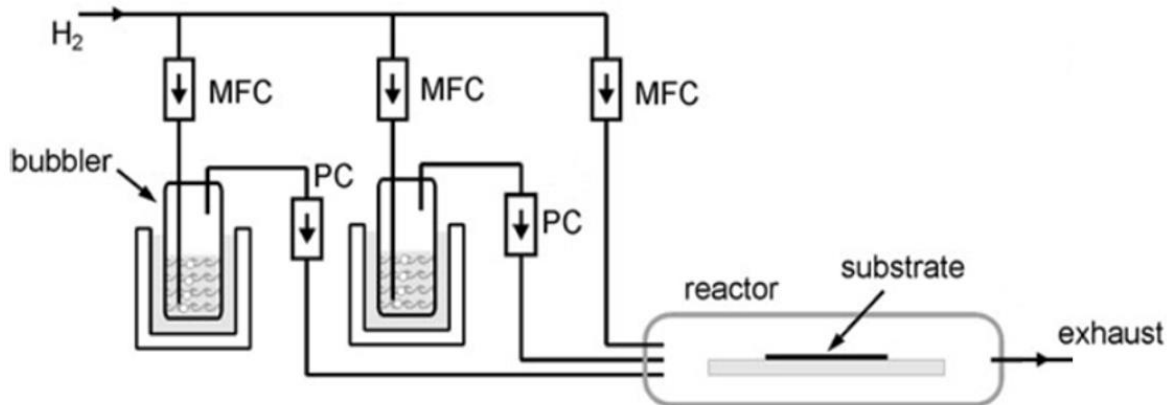


Figure 2.1: Schematic illustration of a MOCVD reactor. Modified image from [27]. The metalorganics are supplied from so called bubblers and the hydrides are supplied from pressurized bottles. Only bubblers are shown in the figure.

MFC: Mass flow controller

PC: Pressure controller

2.1 Atomic incorporation into the crystal lattice

To simplify the explanation of epitaxial crystal growth, a Kossel crystal system is used. This is a very simple model where atoms are represented by cubes. Atomic binding occur at faces of the cubes and each atom in this model thus has six atomic bonds.

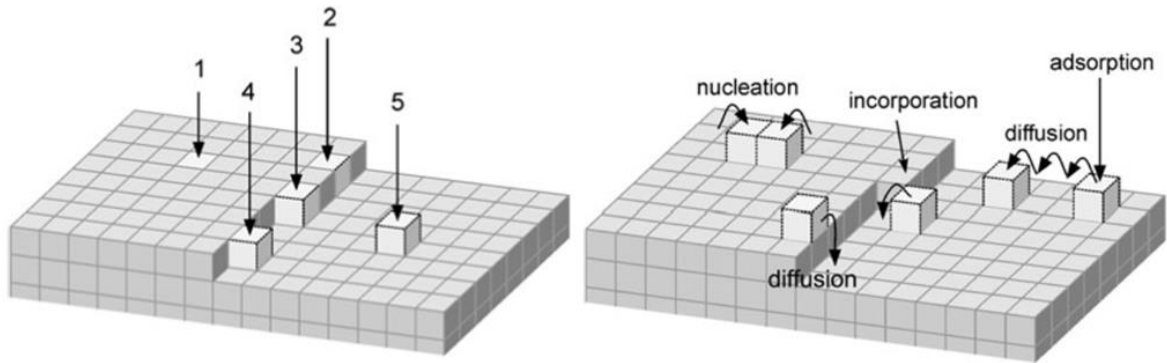


Figure 2.2: Left, different possible sites for an atom in a Kossel crystal. Right, atomic interactions with the substrate during MOCVD growth. Images from [27].

The number of faces the atom binds to will determine the strength of the bond to the surface. The atom #1 in figure 2.2 is very strongly bound to the crystal having only one unsaturated bond and must overcome a high binding energy to move. Atom #2 is embedded in a step edge and has two bonds unsaturated, making it less strongly bound to the crystal than atom #1. Atom #3 is at a position called the kink-site, having three saturated and three unsaturated bonds. When new atoms bind to this site, the number of saturated and unsaturated bonds remains the same and the initial condition is reproduced. As such the surface energy remains the same when atoms bind to the kink sites. The chemical potential of an atom at the kink site is equal to that of the crystal. In order to incorporate new atoms from the vapor at the kink site there must be a higher in chemical potential in the vapor than in the crystal. Atoms #4 and #5 have more unsaturated than saturated and are loosely bound to the substrate, they may readily diffuse on the surface.

During growth impinging atoms adsorb on the substrate becoming adatoms. These adatoms diffuse until they either incorporate into an existing layer at an energetically favorable site or find a bunch of other adatoms and nucleate an entirely new layer.

2.2 Growth modes in epitaxy

There are three growth modes oftentimes referred to in crystal layer growth.

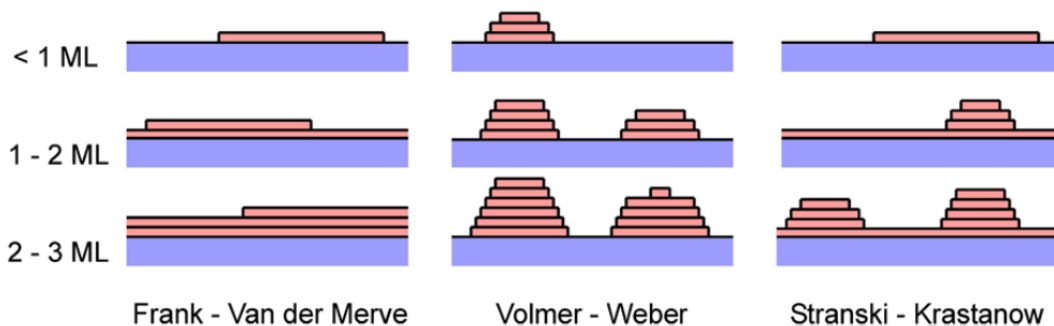


Figure 2.3: Different growth modes in epitaxy, image from [27].

In the Frank – Van der Merve or layer-by-layer growth mode, the adatoms fill up the step edges until it the layer is entirely filled. A new layer is not nucleated before the layer below is completed. In this growth mode the surface energy of the substrate is greater than the surface energy of the film and interface energy between film and substrate. This mode optimally results in one dimensional movement of steps, and is preferable to realize flat, specular surfaces. In contrast, in the Volmer-Weber growth mode, the surface energy of the growing film and the interface energy between film and substrate is greater than the substrate surface energy. Thus the substrate is not sufficiently wetted by the adatoms and many new layers are nucleated the same time. This makes the growth more mosaic in nature. In the last growth mode, the Stranski-Krastanow mode, the growth initially

starts as Frank – Van der Merve, but the interface energy changes during growth changing the growth mode to Volmer – Weber like growth.

2.3 Important parameters in MOCVD

The following section will discuss important parameters of MOCVD growth separately, however these parameters are dependent on each other and changing one of them oftentimes affects another. These parameters all have an impact on the intrinsic material qualities such as minority carrier lifetime, electron mobility and carbon auto-doping. As these intrinsic material qualities of the ELO-layers are not part of the necessary specifications, they will not be extensively discussed in this section.

2.3.1 Temperature

Epitaxy is determined by thermodynamic laws, thus temperature plays a major role. MOCVD oftentimes is divided into two growth modes divided by temperature; the low temperature kinetically limited regime and the high temperature mass-transport limited regime. In the kinetically limited regime, crystal growth rate is limited by reaction kinetics, as all of the precursors used in MOCVD are not fully decomposed due to the low temperature. In the mass-transport limited regime the precursors are almost fully decomposed and the crystal growth rate becomes decoupled from the temperature and instead limited by precursor transport. In addition to the growth mode, temperature also effect diffusion lengths of atoms on the substrate.

2.3.2 V/III ratio

In epitaxial growth of GaAs the V/III ratio expresses the ratio between input group V (AsH_3) and input group III (TMGa and/or TMAI). During GaAs growth an overpressure of AsH_3 , $V/III \gg 1$, is kept to prevent the GaAs substrate from decomposing. Only As is volatile at normal growth temperatures [3].

Given that methyl-groups are oftentimes used as ligands for the precursors in MOCVD, as the precursors decompose, there is carbon in the atmosphere. This carbon, which is pyrolyzed from the precursors, can unintentionally be incorporated into the crystal lattice. V/III effect if this so-called carbon auto-doping is of p-type or n-type. The more AsH_3 the less chance for the carbon impurity atoms to take an As spot in the GaAs crystal [3]. V/III also effects the minority carrier lifetime.

It is important to distinguish between changing the V/III and growth rate parameters. Given that a group V overpressure is usually kept in MOCVD, there is much more group V molecules than group III molecules in the vapor. This means that the group III molecules are the growth rate limiting factor, not the group V molecules. In this thesis, when referring to a change the V/III parameter, the group III flow is kept constant and the group V flow is changed. When referring to a change to the growth rate, the group III flow is changed and the V/III is kept constant. For example a lowered growth rate means that both the group III and the group V flows are lowered.

2.3.3 Miscut

In order to promote the Frank - Van der Merwe growth mode, miscut wafers can be used. Miscut wafers have artificial steps in the crystal, thus the need to revert to nucleate new layers is reduced. Every new layer nucleation is a risk to form crystal defects. Thus miscut provides stability to the growth.

The miscut is created by the substrate manufacturer who saws the wafer ingot at a slight angle creating small atomic steps in the crystal.

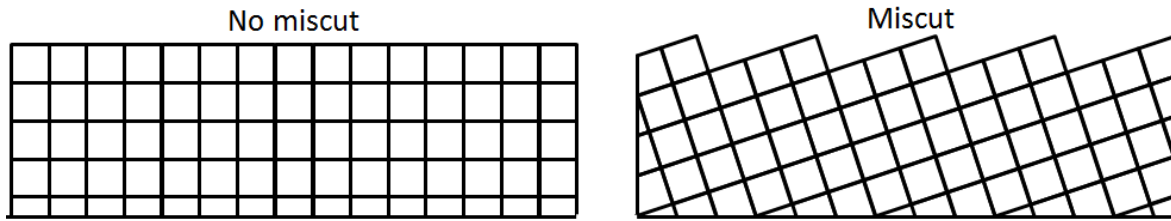


Figure 2.4: Schematic cross-section of miscut and no miscut Kossel crystal. The miscut in this image is grossly exaggerated.

3 Previous work and literature

This section aims to summarize the past work that relates to the project based on the process flow in figure 1.3. The concepts introduced in this section will be tied together in the next section.

3.1 Gallium Arsenide (GaAs) and relevant crystallography

GaAs is a III-V semiconductor compound that has direct band-gap and is suitable for high-efficiency solar cells. GaAs forms a zincblende crystal in bulk from gallium and arsenic, see figure 3.1a. There is extensive literature on growth of GaAs in (100) crystal orientation [3].

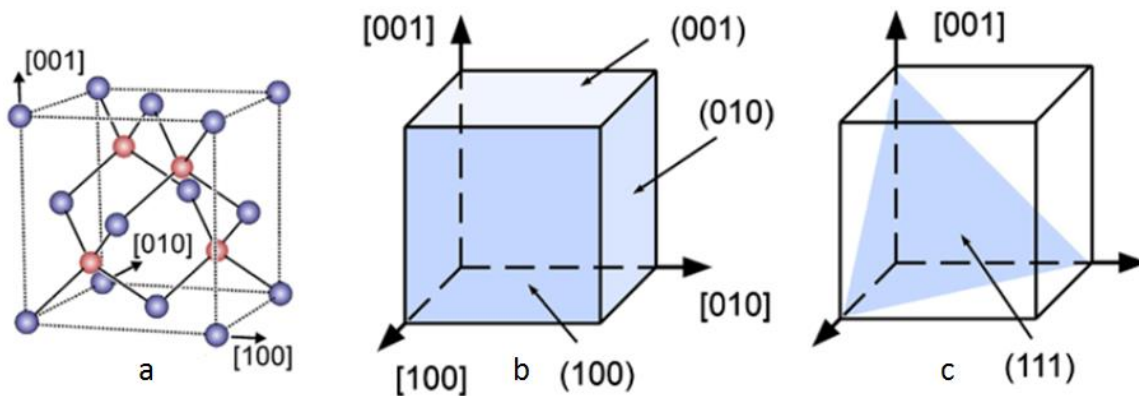


Figure 3.1: Basic crystallography, images from [27]

(a) Zincblende unit cell with atoms. Red and blue dots represent different types of atoms in the lattice.

(b) Unit cell with (100) plane highlighted

(c) Unit cell with (111) plane highlighted.

If a (100) plane is inserted into the atomic unit cell and compared to an inserted (111) plane, figure 3.1, it is clear that they will have a very different surface atomic configurations. Considering the atoms in figure 3.1a, it can immediately be noted that the atomic planes in the [100] direction are of equal distance from each other, whereas the atomic planes in the [111] direction are not. This is

further illustrated in figure 3.2 below.

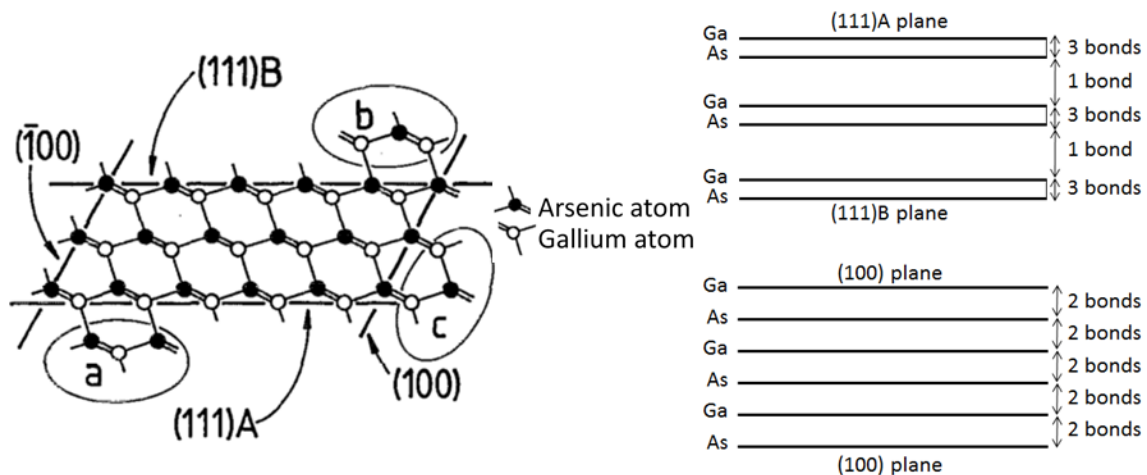


Figure 3.2: Left. GaAs atomic lattice and termination of different crystal orientations, image from [4]. Right. Schematic illustration of how the layers of the planes are ordered and the bonds between for both (111) and (100) planes.

To understand the different surfaces of GaAs, consider the arsenic atom in figure 3.2a on the (111)B plane. It has three bonds towards the bulk of the crystal and only one dangling bond, thus the arsenic atom on (111)B surface is strongly bound to the bulk crystal. In contrast, the surface gallium atom on the (111)B plane only has one bond to the bulk crystal and three dangling bonds, it is only loosely bound to the crystal bulk [4]. The arsenic atoms which have three bonds toward the bulk crystal in the (111)B plane are bound more closely to the crystal bulk, this is shown in figure 3.2 to the right.

Given this contrast in the amount of atomic bonds between arsenic and gallium atoms to the bulk crystal, the (111)B surface will be terminated by arsenic atoms. In addition during crystal growth on the (111)B surface it is much harder to attach the gallium atoms than the arsenic atoms. Therefore growth occurs two monolayers at the same time and the surface remains terminated by arsenic atoms.

Compare this to the atomic binding on the (100) plane, where both the arsenic and gallium atoms have two bonds to the bulk crystal and two dangling bonds. When new atoms are attached to the crystal lattice on the (100) plane, both arsenic and gallium atoms attach with two bonds and the atomic monolayers are of equal distance from each other. There is not a major discrepancy between the binding strength of the atoms on the (100) plane, even though the gallium and arsenic have different binding strength to the crystal lattice.

3.2 Surface reconstructions

As can be noted in figure 3.2 left, the outermost atoms in the crystal have dangling bonds. These dangling bonds will interact and the cause the outermost atoms in the crystal to change their configuration slightly. This phenomenon is called surface reconstruction and is an important consideration during crystal growth.

3.3 Aluminium Gallium Arsenide (AlGaAs)

AlGaAs is a ternary semiconductor compound, where the group III atoms are either aluminium or gallium. Aluminium arsenide (AlAs) is lattice matched to GaAs, i.e. its unit cell size is very close to that of GaAs. This means that AlAs layers or any aluminium concentration in AlGaAs can be epitaxially grown on GaAs without introducing strain in the crystal. Strained layers are harder to grow and it would introduce unnecessary complications in the project to choose a non-lattice matched material. At high concentrations of aluminium (<0.45) in AlGaAs, it has high HF etch selectivity to GaAs [5][6]. Given that AlGaAs can be grown without strain and has good etch selectivity to GaAs, it is a suitable candidate for the sacrificial layer.

3.4 MOCVD growth of GaAs and AlGaAs growth on (111)B

There are few accounts of successful planar wafer (111)B GaAs MOCVD growth in the literature. In their pioneering work Reep and Ghandi [7] made an initial screening of crystal growth on substrates with different orientation. They noted that almost all the growth settings they tried resulted in smooth, specular surfaces in the case of (100) oriented substrates where none of the settings yielded a passing grade for (111)B. It seems that most research has been performed on (100) oriented wafers simply because there has been little need for (111)B planar GaAs growth.

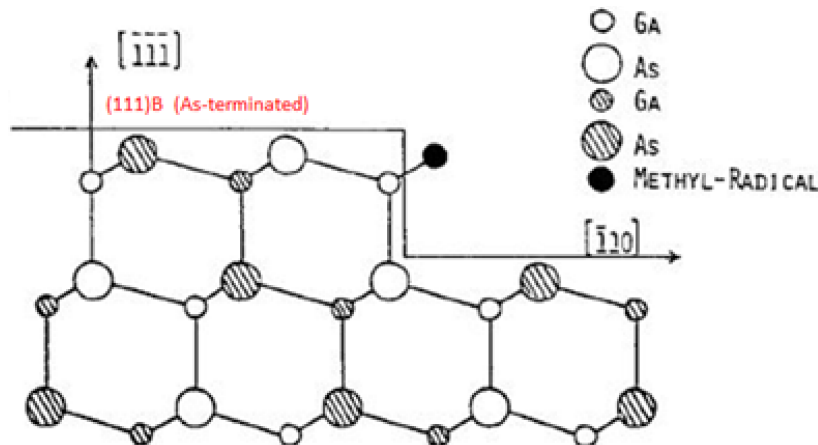


Figure 3.3: (111)B step propagation during growth. Image from [7]

Reep and Ghandi [7] offer the following explanation why growth on (111)B GaAs is more difficult in figure 3.3. The last methyl group of TMGa is not thoroughly pyrolyzed as the gallium atom is integrated in the GaAs lattice. The first two methyl radicals of the TMGa molecule are easily removed whereas the last require much more energy. This remaining methyl-group inhibits the step propagation once a layer is nucleated. Combined with the GaAs crystallography in section 3.1 this may provide some insight as to why (111)B growth is harder. One way to lessen the effect of the remaining radical is to use TEGa as a group III precursor rather than TMGa as the decomposition energy of TEGa is lower than TMGa.

Since Reep and Ghandi did their work in 1983, there has been few attempts to grow planar GaAs on (111)B oriented material in MOCVD. Below are all accounts I have found in literature on (111)B planar MOCVD GaAs growth. They are arbitrarily named high, medium and low temperature growth.

3.4.1 High temperature planar GaAs growth

Kato et al reported in their paper [8] that specular GaAs growth in MOCVD is possible on exactly (111)B oriented substrates at temperatures at 875-900 °C and a V/III of 10-20. They noted that a high density of hillocks appeared at lower temperatures and higher V/III ratios. They also noted that the hillock density can be reduced by using a miscut substrate.

3.4.2 Medium temperature planar GaAs growth

Moise et al [9] tested different growth temperatures between 600 and 750°C and reported to have found a narrow growth window for specular GaAs at 625°C using (111)B miscut 2° toward [100] GaAs substrates. They used triethylgallium (TEGa) as group III precursor rather than TMGa, possibly motivating the usage of TEGa the same way as Reep and Ghandi. They reported $\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$ growth at the same settings; however they note that the AlGaAs growth was not specular.

Fukui and Saito [10] reported specular GaAs growth at 650°C both (111)B GaAs with 2° miscut toward [00-1] and [-1-11]. They note that miscut toward [00-1] yielded better surfaces. When growing AlGaAs at these settings the surfaces became rough. They also report growth of fractional-layered superlattices (FLS), $(\text{AlAs})_{\frac{1}{2}}(\text{GaAs})_{\frac{1}{2}}$ with flow rate modulated epitaxy (FME). Every other layer of

group III atoms are Al. In the FLS growth on (111)B with 2° miscut toward [00-1] they report pits in the growth.

3.4.3 Low temperature planar GaAs growth in MBE

There are multiple accounts of specular molecular beam epitaxy (MBE) growth on exactly (111)B oriented substrates [11][12][13] where the primary interest has been to study the different surface reconstructions on (111)B GaAs, both steady state and during growth. The surface reconstructions are an effect of the dangling bonds from the outermost atoms in the crystal. As is shown by the MBE literature different kinds of surface reconstructions can be achieved by adjusting certain parameters such as temperature and arsenic input, see figure 3.4 below. The surface reconstructions have been shown to have a strong impact on MBE growth quality, for instance Yang et al [14] report optimal temperature for specular GaAs (111)B growth in MBE to be 550-580°C which correlates to a specific surface reconstruction.

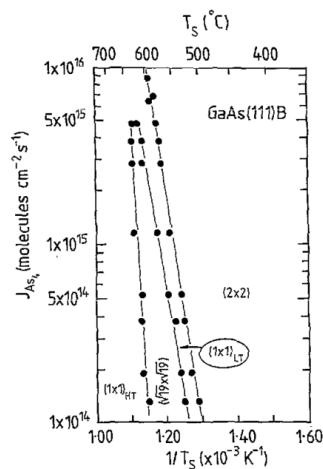


Figure 3.4: The different surface reconstructions of (111)B depending on As flux and temperature. Data from Woolf et al [13].

From MBE growth research the surface reconstruction of (111)B GaAs is well known [13]. Yang et al [12] claims that the $\sqrt{19} \times \sqrt{19}$ is the best starting surface reconstruction for (111)B MBE growth.

3.5 Gold Assisted Nanowire Growth

As nanowire growth is not the main focus of this thesis it will only be discussed very briefly. The gold seeded vapor-liquid-solid (VLS) growth of nanowires is well documented, it was first reported by Wagner and Ellis in 1964. The aspect of gold-catalyzed nanowire growth which is really relevant for this thesis is that the preferred growth direction for nanowires is the (111)B direction [16]. Gold catalyzed nanowires will only grow in the (111)B direction, no matter the orientation of the substrate.

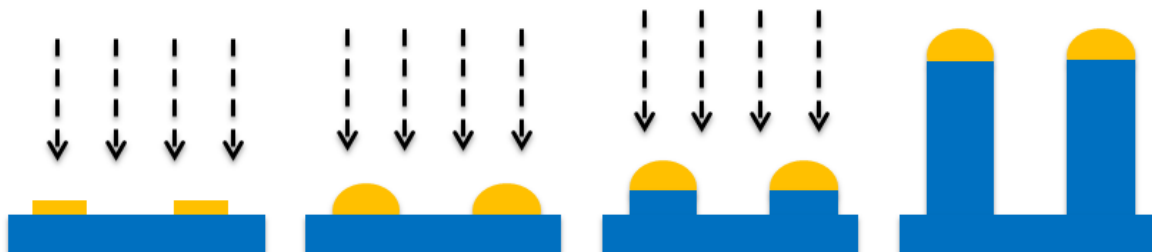


Figure 3.5: Schematic illustration of the Au-assisted VLS nanowire growth.

Gold nanowire seeds are deposited on the substrate outside the MOCVD reactor. In the MOCVD reactor, first the gold discs are alloyed with the group III precursor. Then the nanowires can start to

grow. When nanowires have reached the desired height, growth is ended when precursors are no longer supplied.

There are other ways to manufacture nanowires than through the gold catalyzed VLS scheme. An example of this is selective area growth through a mask. These alternative ways to manufacture nanowires will not be discussed as this project is restricted to the gold catalyzed nanowires in order to be compatible with previous research by Sol Voltaics [2].

3.6 Epitaxial lift-off

The ELO process for planar structures is covered in several papers from different research groups [17][18][19][20][21]. The general strategy these groups have is to grow both the epitaxial lift-off-layer and the solar cell at the same time. After the device has been separated from the substrate, the substrate can be recycled.

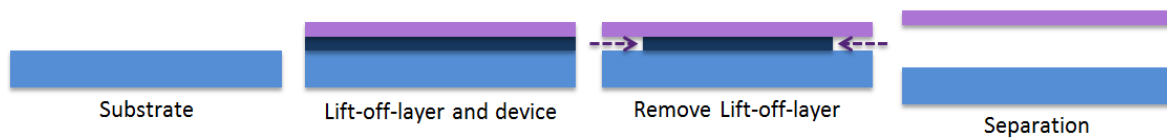


Figure 3.6: Schematic illustration of the ELO process. The lift-off-layer and the device are grown in the same step. The device is then separated from the substrate through selective etching of the lift-off-layer.

As a note of interest the current world record efficiency 30,8 % at 1 sun solar cell for solar cells overall was fabricated by Alta devices [22] using ELO.

Given the restrictions in this project the entire device cannot be epitaxially grown in one single step. The nanowires must be gold catalyzed, thus the substrates need to be imprinted outside the MOCVD reactor before nanowire growth can occur.

3.6.1 Etching the sacrificial layer

The sacrificial layer should ideally be etched isotropically with high selectivity towards the other layers. Epitaxial lift-off using GaAs as substrate and lift-off-layer and AlGaAs as sacrificial layer provides such a system when etched in HF. Other etchants such ammonium hydroxide and citric acid combined with hydrogen peroxide gives only a moderate selectivity between GaAs and AlGaAs [23].

The higher the etch rate of the sacrificial layer is the better, as this minimizes the risk of unintentional etch damage to the final structure. Also higher etch rates are preferable as this saves man-hours. Literature indicates that there are five major ways of accelerating the etch rates:

The primary way to increase etch rate and selectivity between the layers is to increase the aluminium content in the sacrificial layer. Kumar et al [23] did a thorough survey of lateral etch rate of the sacrificial layer versus the aluminium content in the layer.

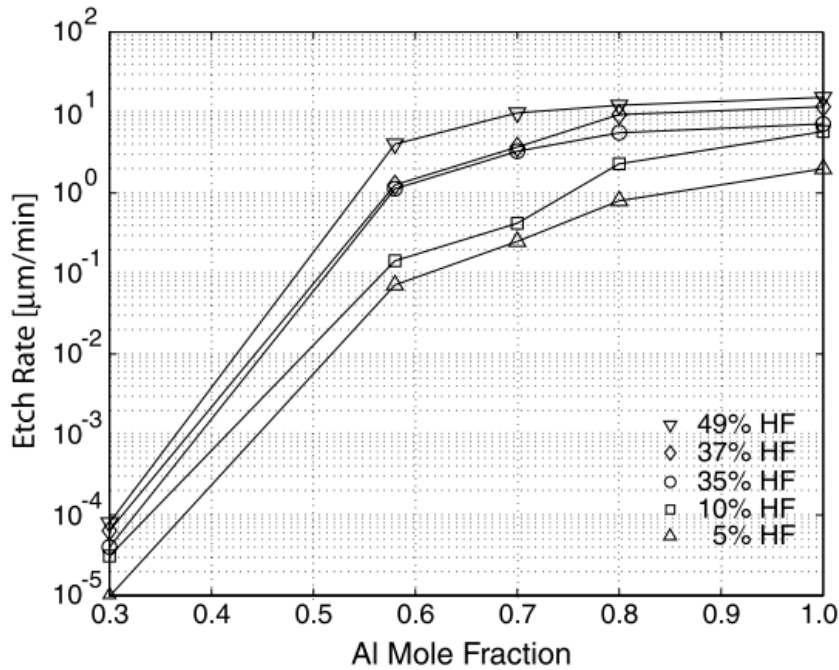


Figure 3.7: Lateral etch rate of the 2,5 μm thick $Al_xGa_{1-x}As$ sacrificial layer vs aluminium mole fraction (x). Note that Al mole fractions beneath 0.3 are very slow to etch and there is no substantial etch rate increase with Al mole fractions above 0.6.

Wu et al [20] tested the etch rate of different thicknesses of the AIAs sacrificial layer (using (100)-GaAs) and demonstrated that the thinner the sacrificial layer is, the higher the etch rate. They also demonstrated that the addition of a hydrophilic substance such as acetone in the HF solution substantially increases the etch rate as the contact angle between etchant and the sample is decreased. This lowers the amount of redeposition on the etched walls. However, HF is extremely poisonous and every step handling HF is a safety risk, thus the scheme of mixing HF with a hydrophilic substance will not be utilized in this work. Further etch rates could be increased by heating the etchants, but as the heating also introduce a safety risk, this was not utilized either.

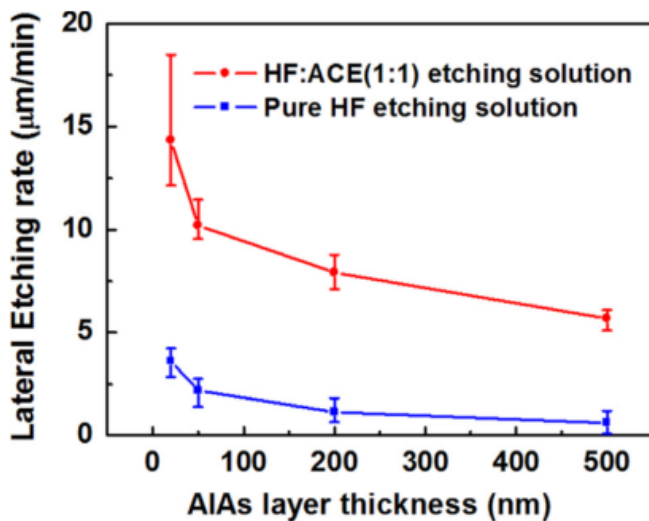


Figure 3.8: AIAs layer thickness vs lateral etch rate, etch rate data with hydrophilic substance is also included Image from [20].

The fifth way to accelerate the etch rate is to peel back the film as it is etching. This strategy was employed by Yablonovitch et al using black wax to induce strain and peel the film.

4 Specifications of the Epitaxial Lift-off-Layers

Given that most of the steps in the process flow, figure 1.3, apart from the epitaxial layer growth, is well established in literature, as this step is solved, the project falls into place. The needed specifications for the ELO-layers are determined by the sequent steps in the process flow.

4.1 Reviewing the process flow



Figure 4.1: Step 3 in the process flow. Imprint of gold seeds.

In step 3 gold nanowire seeds are to be deposited through a sensitive imprint process. As the ultimate goal of this thesis work is to create solar cells a high density of wires is required and this cannot be achieved with aerosol deposition. Thus imprinted Au seeds are necessary.

The imprint process requires the surface to be almost perfectly flat, otherwise the imprint process will be unreliable. There are multiple spin-coating steps in the process that will be uneven unless the surface is flat. If there are any features on the surface, they will interfere with the distribution of the polymer being spun and the resulting layer would be uneven. The actual patterning process requires close contact between the mask with the pattern and the spin-coated substrate. A hilly surface would prevent close contact and may even damage the imprint mask. Ultimately a perfectly flat substrate is preferred, since the imprint process is already complex and fairly sensitive. If there are hillocks on the end product, they cannot be larger than 10 nm in size. Even though there are workarounds to an uneven surface, introducing more uncertainties to a sensitive process is not desirable.



Figure 4.2: Step 4 in the process flow. Growth of the nanowires

In step 4 nanowires are to be grown, this dictates that the substrate must be of (111)B orientation as this is the preferred growth direction of nanowires. It was shown by Hiruma et al [16] that nanowires will grow in the (111)B direction regardless of the original orientation of the substrate. This implies that the topmost ELO layer cannot be polycrystalline as this will create disorder in the nanowire arrays.

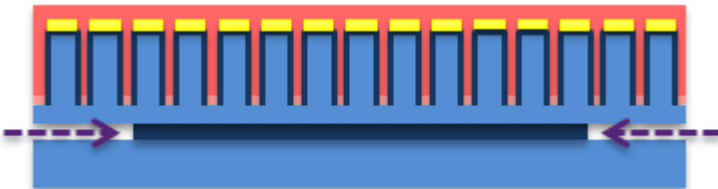


Figure 4.3: Step 6 in the process flow. Etching of the sacrificial ELO-layer.

In step 6 the sacrificial layer will be selectively etched. This means that the sacrificial layer must be etchable and there must be a high etch selectivity between the layers. It is also preferable to have a high lateral etch rate of the sacrificial layer. The lateral etch rate should be $> 1 \mu\text{m}/\text{minute}$, this etch rate is not high enough to etch entire 2" wafers, it would be a good indication that the ELO-strategy is plausible. A high lateral etch rate reduces the needed etch time which both reduces costs and the risk of damaging the end product during the etch step. In addition to etchability, the topmost layer on which the nanowires are to be grown, must remain intact during the etching. Otherwise the etchant might leak through the topmost layer and start etching the shells of the nanowires.

Reviewing section 3.6 on epitaxial lift-off this means that the sacrificial layer should be fairly thin with an aluminium content >0.6 .

4.2 Specification of the ELO-layers

In summary, two distinct layers with (111)B direction and etch selectivity that are perfectly flat must be grown. At least the topmost layer must be GaAs to enable sequent nanowire growth. The sacrificial layer should be AlGaAs with aluminium content >0.6 . If the epitaxial lift-off-layers can be grown according to these specifications, nanowire ELO should be possible by combining steps already shown in literature.

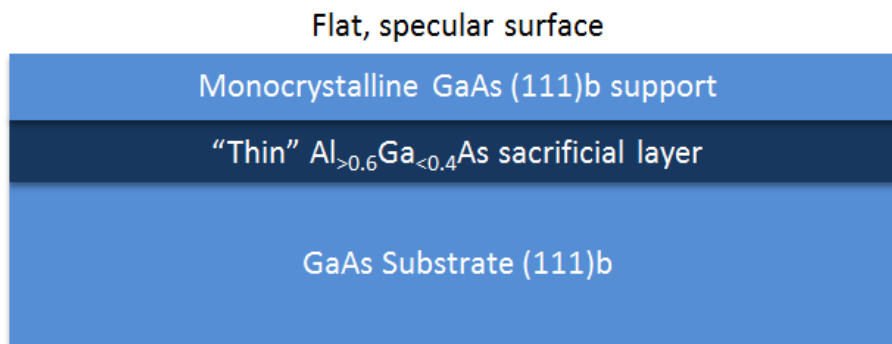


Figure 4.4: Schematic image of the end product for step 2 in the process flow with the requirements to achieve nanowire ELO.

It should be noted that usually in epitaxial development the end product is going to be integrated into an electrical device. Thus, careful consideration of intrinsic material qualities such as conductivity and autodoping is required. These considerations put restraints on how aggressively growth parameters like V/III and temperature can be tuned. Given that the epitaxial layers are ultimately to be removed and not used in the final device, no consideration to these intrinsic crystal properties is needed as long as the nanowires are not affected by the ELO-layers. This will provide some much needed leeway in the development of the ELO-layers.

One final note, it is preferred that the layers which are to be developed can be grown in the current equipment, an Aixtron 200/4 cold wall reactor horizontal flow MOCVD with maximum temperature capability of 750°C.

5 Selection of characterization methods

One of the most important aspects of any development is characterization. Unless there is a firm understanding of the output data, it is very hard to optimize the input data. Therefore, a lot of effort has been put into selecting good characterization methods.

In summary there are three aspects in the ELO-layer development that need characterization. First the topmost GaAs layer surface roughness, this reflects how hilly the growth is and also a smooth surface indicates that the crystal orientation has been kept during the growth. Second the Al mole fraction of the AlGaAs sacrificial layer need to be determined to ensure that the layer is etchable. Third the thicknesses of the grown layers need to be established.

As is already noted, characterization methods that measure intrinsic material qualities such as for instance Hall measurements and lifetime measurements, although interesting, are not made in this thesis. These properties are not of interest to this project.

5.1 Attributes of characterization methods

The following attributes of characterization methods were taken into consideration in the selection of characterization methods:

- **Feedback time:**
Since this thesis project has a strict deadline, one of the most aspects of a characterization is the time it takes to get feedback. In addition, MOCVD tools are expensive and access to them is limited. The quicker the characterization can be made the more runs can be made, since the MOCVD is not slowed down by the characterization feedback loop.
- **Invasiveness:**
Some characterization methods are invasive and destroy the sample being characterized and the III-V material used for the project is expensive. If the characterization is invasive it must provide enough information to motivate the loss of material.
- **Quantifiability:**
When comparing two runs from an experimental split qualitative characterization is enough. However, it is easier to compare numbers and this become more and more relevant when more runs are to be compare to each other.
- **Accuracy**
How precise the measurement is and how specific the data is, there is usually a trade-off between accuracy and the time it takes to get the characterization feedback.

5.2 Specific characterization methods

This section covers summarizes specific characterization methods in relation to the attributes mentioned above. Some characterization methods, although extremely accurate, are prohibitively expensive and time consuming some of the excluded characterization methods will be mentioned toward the end of this section.

5.2.1 Optical inspection (naked eye inspection)

A quick glance at the produced material is oftentimes enough to qualitatively judge the difference between two runs. The needed end result is a flat, specular and mirror-like surface. Given that growth defects such as hillocks and rough surfaces are oftentimes visible by the naked eye, the only needed characterization to determine if a run is bad is a quick optical inspection. However, the optical inspection in itself is not sufficient to determine that a run is good as not all growth defects are visible by the naked eye. inspection

	Optical inspection	
	Surface roughness	Al mole fraction
Feedback time	Instant	N/A
Invasive	No	N/A
Quantifiable	No	N/A
Accuracy	Poor	N/A



Table 5.1: Left, summary table of optical measurements. Right, qualitative optical comparison between two samples. The sample to the left has a very rough surface and is far from the mirror-like surface. The run to the right is mirror-like without hillocks, (the top of the reactor is mirrored in the sample) thus it can be expected to meet the smoothness specification.

5.2.2 Scanning Electron Microscope (SEM)

An SEM is an electron microscope that scans the sample with a focused beam of electrons. The electrons interact with the sample and are then be collected in a detector, producing an image. SEM gives relatively fast and accurate feedback. Even though the surface roughness data from SEM measurements is relatively poor, together with XSEM characterization it gives a good qualitative indication when comparing two runs with each other. One drawback using SEM is that some carbon is deposited on the sample being characterized. However, during development this is not considered to be of consequence.

	Top view SEM		
	Surface roughness	Layer thickness	Al mole fraction
Feedback time	Fast	N/A	N/A
Invasive	No	N/A	N/A
Quantifiable	Feasible	N/A	N/A
Accuracy	Good	N/A	N/A



Table 5.2: Summary table of top view SEM measurements.

5.2.3 XSEM

XSEM refers to cross-section SEM, i.e. the sample is cleaved before put into the SEM. XSEM is the fastest characterization method available to see the AlGaAs layer. There is a slight contrast difference between GaAs and AlGaAs, thus the AlGaAs layer can at least be qualitatively confirmed. In addition the thickness of the grown layers can be measured in XSEM.

	XSEM		
	Surface roughness	Layer thickness	Al mole fraction
Feedback time	Medium	Medium	Medium
Invasive	Yes	Yes	Yes
Quantifiable	Feasible	Yes	No
Accuracy	Good	Good	Poor



Table 5.3: Summary table of XSEM measurements.

5.2.4 Reflectometry

Reflectance measurements can be made by shining light of different wavelength on a sample and the measuring how much light that comes back indicating how much light was scattered by the surface roughness. By normalizing the measured reflectance value to that of ungrown epi-ready GaAs wafers the arbitrary reflectance percentage could be quantified.

Reflectometry has a larger measurement area than SEM and gives a quantifiable measurement of the surface roughness. One drawback with measuring the surface roughness with reflectometry is that data from the reflectometry could be convoluted. Once an epitaxial layer starts to become rough during growth, it will likely become even rougher throughout the rest of the growth. If a thicker layer is grown, the surface roughness is bound to become greater. Thus it is necessary to be careful when interpreting data from the reflectometer as a rough thin layer cannot fairly be compared to a rough thick layer.

The reason to look at many wavelengths at the same time is to bypass the risk of destructive interference.

	Reflectometry		
	Surface roughness	Layer thickness	Al mole fraction
Feedback time	Fast	N/A	N/A
Invasive	No	N/A	N/A
Quantifiable	Yes	N/A	N/A
Accuracy	Good	N/A	N/A

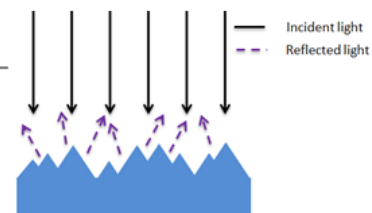


Table 5.4: Left, summary table of reflectance measurements. Right, schematic image of how reflectance measurements work.

5.2.5 Stain etch

After growth the samples are cleaved and the AlGaAs is selectively etched in HF. This gives some information to the Al mole fraction as AlGaAs layers with higher Al molar fraction will etch faster.

Most importantly the “etching characterization” answers the question: does the material etch fast enough. As the sacrificial layer thickness also impacts etch rates, care must be taken not have the etch data convoluted.

Stain etch (with XSEM)			
	Surface roughness	Layer thickness	Al mole fraction
Feedback time	N/A	Slow	Slow
Invasive	N/A	Yes	Yes
Quantifiable	N/A	Yes	Yes
Accuracy	N/A	High	Medium




Table 5.5: Summary table of stain etch and XSEM characterization.

Dynamic Secondary Ion Mass Spectrometry (SIMS)

SIMS is used to analyze atomic composition of a solid material. The surface of the substrate that is to be characterized is sputtered with a focused ion beam. The ion beam contains the primary ions. The secondary ions are ejected from the substrate due to sputtering. The ejected ions from the substrate are the secondary ions, which are measured and quantified with a mass spectrometer as they are ejected from the substrate. Substrate composition vs depth profiles are obtained as the ion beam etches deeper and deeper into the sample.

SIMS is an accurate but invasive. Preferably every sample should be characterized with SIMS, but it is expensive and slow.

SIMS			
	Surface roughness	Layer thickness	Al mole fraction
Feedback time	N/A	Slow	Slow
Invasive	N/A	Yes	Yes
Quantifiable	N/A	Yes	Yes
Accuracy	N/A	High	High

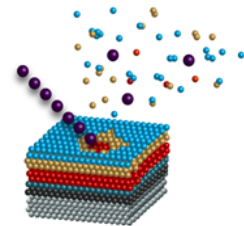


Table 5.6: Left, summary table of SIMS characterization. Right schematic image of SIMS from [28]

5.2.6 Weighing samples

In order to determine thickness of the grown epitaxial layer, the sample can be weighed before and after growth on a scale with 0.0001g resolution. This mass divided by sample size and density gives a fairly accurate approximation of the grown thickness.

Weighing			
	Surface roughness	Layer thickness	Al mole fraction
Feedback time	N/A	Fast	N/A
Invasive	N/A	No	N/A
Quantifiable	N/A	Yes	N/A
Accuracy	N/A	Decent	N/A



Table 5.7: Summary table of characterization by sample weight.

5.2.7 Interactions and synergistic effects between the characterization methods

As is already mentioned, some characterization methods provide data that is convoluted with other properties of the material. For example, the reflectance measurement is convoluted with the thickness of growth. In such cases before any conclusions of the growth quality can be made a more holistic approach is required, looking at both the weight measurements and the reflectance measurements.

5.2.8 Characterization methods not used in this project

The following characterization methods were not used, mostly due to time constraints.

Atomic force microscope (AFM) probes the surface of the sample with an atomically thin cantilever. As the cantilever is in contact with the sample, it moves up and down with the sample topography allowing for atomic resolution topography scans.

A photoluminescence (PL) setup illuminates the sample with a laser, so called photoexcitation. As the electron relaxes back to the valence band a photon is emitted with information about the band-gap of the sample. PL is a very fast characterization method that could provide insight the aluminium molar fraction in the AlGaAs layer as it measures bandgap in the material. There are several issues with using PL measurements though.

1. If aluminium molar fraction is higher than 0,4 the band gap becomes indirect and it is no longer possible to measure aluminium molar fraction accurately
2. The only PL setup that was available was a room temperature PL setup. To get a strong enough signal, the material need to be at least slightly doped to increase the recombination in the structure.
3. The material to be measured should preferably be contained in a quantum well

Both point 2 and 3 above would require epitaxial development which would be more expensive and time consuming than to just characterize with SIMS. In addition, the results from PL on samples with higher aluminium molar fraction than 0.4 would have had to be extrapolated from runs with lower molar fractions.

6 Results, MOCVD development of ELO layers

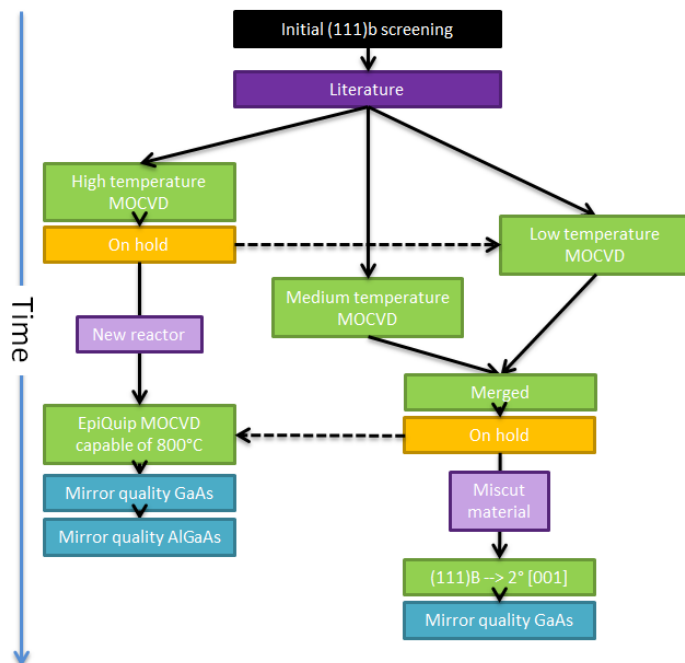


Figure 6.1: Overview of the epitaxial work flow over time. Some of the development was put on hold while waiting for miscut material or new reactor.

Figure 6.1 intended to help the understanding of the work flow. Since there were three different strategies employed to achieve the ELO structures, it is necessary to understand the work flow over time. Initial screening of (111)B growth based on known (100) growth conditions

The first test that was made, was to include a (111)B oriented wafer in a run designed for (100) oriented wafers. This, to check if the reported literature on (111)B growth is accurate.

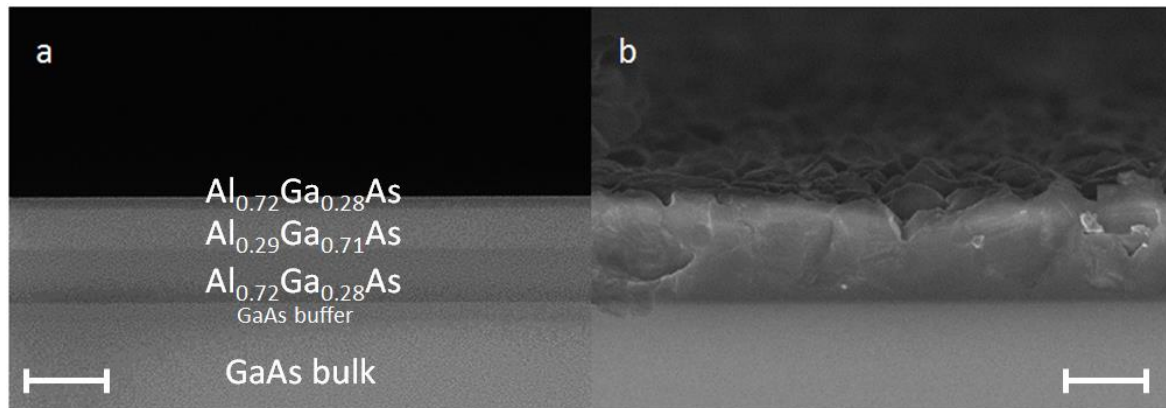


Figure 6.2: XSEM of standard (100) test run. Scale bar is 1 μm .

(a) (100)-GaAs with the different layers in the PL structure, this is how it the growth should look
 (b) (111)B-GaAs. The growth is polycrystalline and rough.

Second a simpler structure was tested. A GaAs/ $\text{Al}_{0.92}\text{Ga}_{0.08}\text{As}$ /GaAs structure.

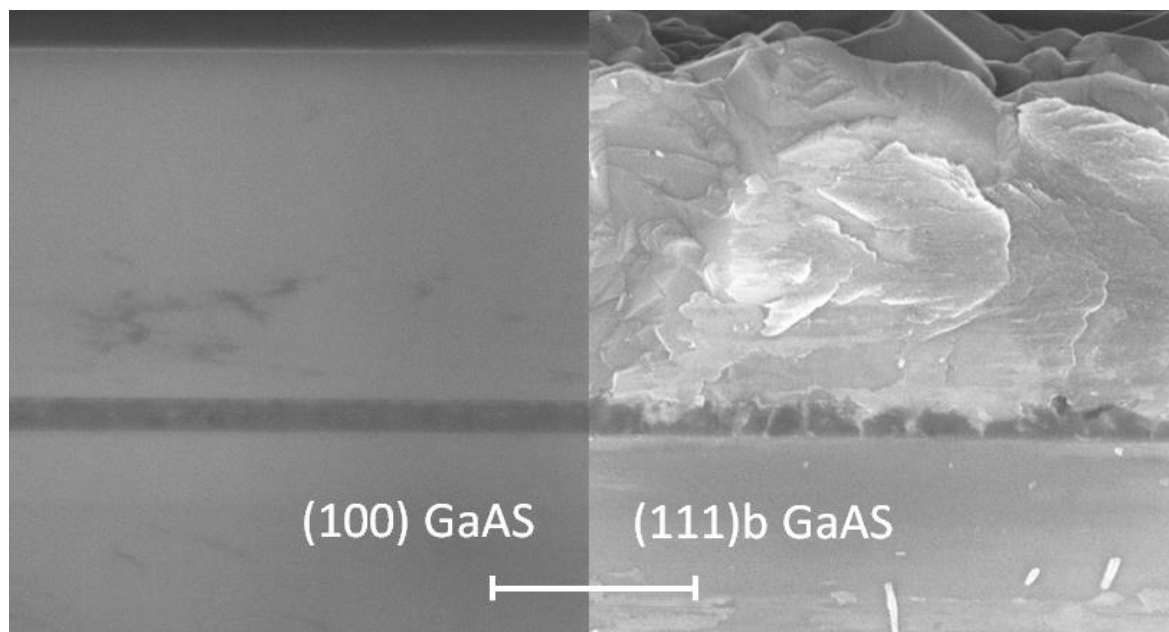


Figure 6.3: XSEM of the second test. Left, growth on (100) oriented substrate. Right same growth on (111)B oriented substrate. Scale bar is 1 μm

From figure 6.2 and figure 6.3 it is clear that the “standard” (100) growth settings is not applicable to (111)B. Development will be required to realize the ELO layers on (111)B material. These two tests is in accordance with what literature suggest. In both tests, it seems that the growth failed as soon aluminium was introduced. Therefore, the first step will be to successfully grow GaAs on GaAs.

6.1 Possible approaches and their limitations.

Section 3.4 contains a summary of all previous work relating to MOCVD growth on (111)B oriented GaAs that was found. From this literature, three possible approaches to achieve the ELO layers were discerned. None of these approaches could be reproduced as they were reported in literature due to these initial limitations.

1. Only access to Aixtron MOCVD tool which is limited to 750°C
2. Only access to substrates which are exactly (111)B oriented, no miscut material available.

Since none of the approaches could be reproduced all approaches were kept as alternatives, to mitigate the risk of choosing a failing approach.

6.1.1 High temperature MOCVD

The high temperature approach based on Kato's work [8], is the approach that lies closest to the initial tests made in figure 6.2 and figure 6.3. In addition Kato's work is the most detailed and is actually focused on growth development on (111)B oriented wafers. The problem with reproducing their research is they reported that at least 850°C is needed for specular growth at exactly (111)B oriented wafers.

6.1.2 Low temperature MOCVD

The low temperature approach is based on MBE work is a high risk approach. It is difficult to relate MBE growth settings to MOCVD. A MBE uses pure element sources and "evaporates" them toward the substrate in vacuum. MOCVD uses metal-organic precursor which are transported toward the substrate in H₂ ambient. Still, there are plenty of reports in MBE where GaAs have been grown successfully on exactly (111)B oriented substrates [12][14] [24]. Also, there is a firm understanding of what happens on the surface during MBE growth.

6.1.3 Mid temperature MOCVD

Moise et al [9] reported (111)B GaAs and AlGaAs growth at 625°C using TEGa as precursor. However, they used 2° miscut material to achieve specular growths, which was not available. Also for the AlGaAs growth they reported crystal defects already on Al_{0.15}Ga_{0.85}As. As discussed in the section 3.6, at least Al_{0.6}Ga_{0.4}As is required to achieve the desired ELO-structure.

6.2 High temperature, initial test based on results from Kato et al

Based on the initial test in figure 6.3, two growth splits were made to approach the growth settings reported by Kato et al. These splits were made growing only GaAs on GaAs. First a temperature split was made to determine the effect of increasing the temperature from 710°C to 750°C, the maximum allowed temperature for the Aixtron reactor.

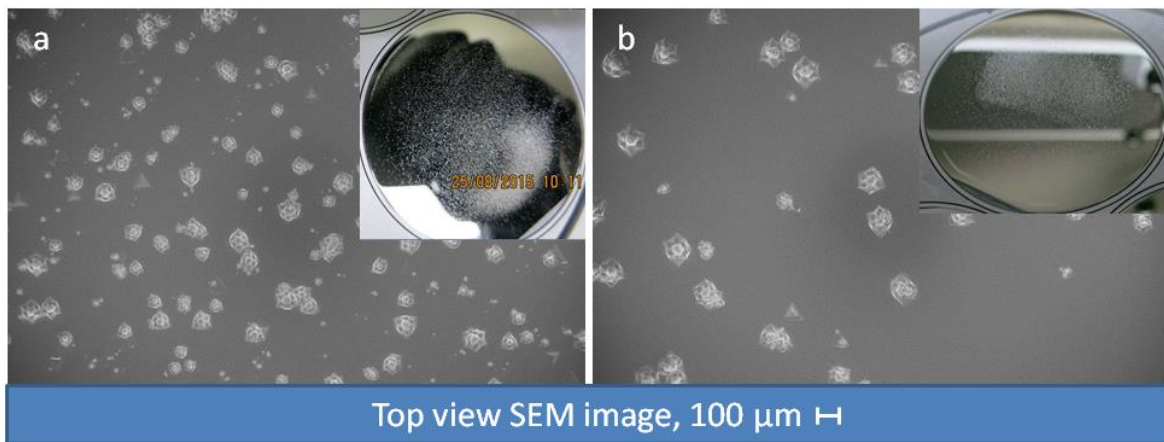


Figure 6.4: Initial GaAs growth, temperature split. SEM image together with photograph of wafer.

(a) 710°C, 50 V/III.

(b) 750°C, 50 V/III

There is an indication of improvement when the temperature is increased by 40°C as the amount of hillocks on the wafer is reduced. Second a V/III ratio split was made.

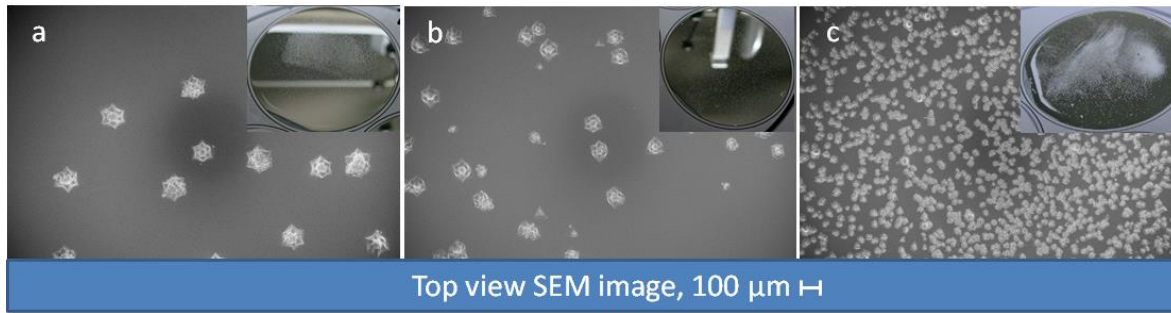


Figure 6.5: Initial GaAs growth, V/III split. 100X SEM image together with photograph of wafer
 (a) 750°C, 50 V/III
 (b) 750°C, 23 V/III
 (c) 750°C, 11 V/III

The growths in the above splits were adapted from (100) growth recipes to yield approximately 2 μm thick planar GaAs. The growths on (111)B oriented GaAs did not seem to yield this thickness, also the thickness is bound to be convoluted by the growth of hillocks. Given that only GaAs is grown on GaAs it is difficult to determine if any planar growth has occurred at all. XSEM and stain etching is unviable since these rely on the layers being of different material. However, the GaAs layer grown in these splits is undoped, whereas the substrate used is doped. Therefore, the growth and the growth thickness can be confirmed by using SIMS profiles looking at the Zn dopant profile.

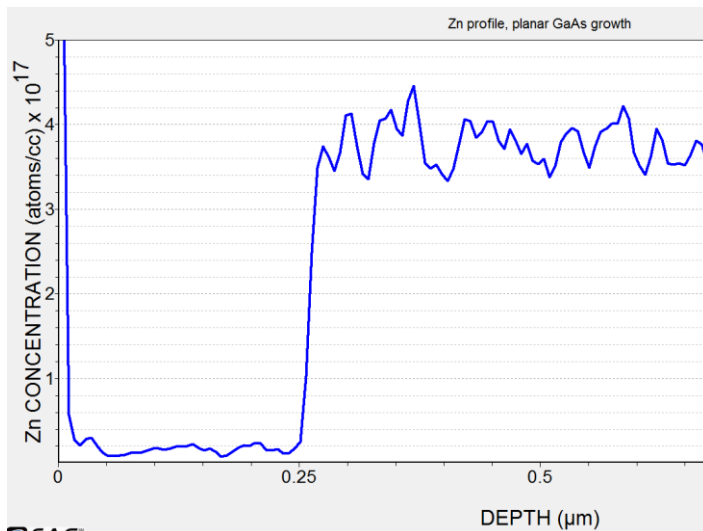


Figure 6.6: SIMS profile of the growth in figure 6.5b, the best growth pursuing the high temperature approach. SIMS “drills” the substrate from the surface of the wafer, so the leftmost value is the grown layer.

The SIMS profile show that only approximately 250 nm GaAs was grown on the (111)B GaAs, when the same growth supposedly should yield approximately 2 μm on (100) oriented substrates. The slow growth rate could possibly be explained by the theory posed by Reep and Ghandi, figure 3.3, that the hillocks consume some of the material, or that the Ga-atoms have difficulties sticking to the surface. The last theory was explained in detail together with figure 3.2.

The results of these two splits are summarized in Table 6.1.

Temperature (°C)	V/III	Defect count	Area covered with defects (%)
710	50	356	13
750	50	113	12
750	23	23	6
750	11	229	24

Table 6.1: Summary of the initial temperature and V/III split. Three spots on the wafer were randomly selected where defects were characterized by count and area coverage.

The scheme to select three random spots on each wafer is not fully reliable. There was a high variance between the counts in the independent images, which is attributed in the photographs in growth split in figure 6.4 and figure 6.5. The hillocks not randomly distributed on the wafers. Still it gives some indication of the growth quality.

The results from the two splits in figure 6.4 and figure 6.5 are not in agreement with claims from Kato et al. A lower V/III should decrease hillock formations just as an increase in temperature should. Additionally, the hillocks are not evenly distributed on some of the wafers. The wafers seen in figure 6.4 and figure 6.5 have the same specification from the manufacturer and the wafers were treated identically prior to growth. The only difference is that the wafers were from different wafer ingots. To test if the ingot had an impact, one more run was made.

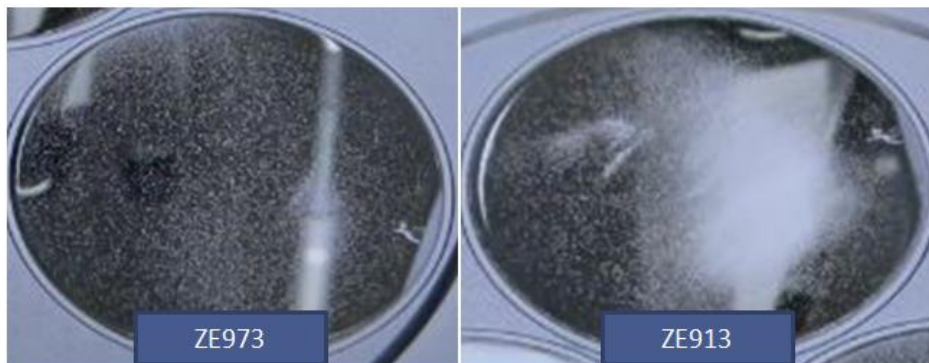


Figure 6.7: Comparison of growth quality between wafers from two different ingots. These wafers were in the same growth run and were handled identically prior to growth.

From figure 6.7 it is clear that the wafers from the ingot named ZE913 are defect, as the hillocks are unevenly distributed. The wafer manufacturer had delivered sub-par wafers, compromising the growth split. The bad batch of wafers was discarded. From this point onward, only wafers from ingots that had been tested were used in the growth splits.

Even though the results from growth splits in figure 6.4 and figure 6.5 were compromised by the ingot, it is clear that the growth quality would not meet the specifications. There are far too many hillocks on the wafers, even in the best growth run. Given that AlGaAs growth is even more difficult than the GaAs growth, there is not enough leverage to find a good growth setting. The temperature is already at its maximum for the Aixtrix 200/4 system and V/III is close to its minimum. Minimum V/III is limited by arsenic desorption and GaAs decomposition due to high temperatures [25]. As was reported by Kato et al higher reactor temperature is key to achieving good material. The high temperature approach cannot continue unless a reactor that allows for higher temperatures is found.

6.3 Low temperature approach

Next the low temperature approach based on MBE work was tested. This project was set up to examine if surface reconstruction ideas from MBE can be transferred to MOCVD. In the early development of growing GaAs/AlGaAs on (111)B, MBE was also struggling with hillock formations at

higher temperatures. Instead of raising the temperature to prevent hillocks, the temperature was lowered, keeping close watch on the surface reconstructions [4]. Perhaps a similar strategy can be employed in the MOCVD development. This approach was appealing since it hopefully does not require miscut material.

6.3.1 The importance of growth characterization and tracking tool condition

Based on the surface reconstructions shown by Woolf in figure 3.4 an aggressive V/III split was set up to see if some difference in the surface reconstructions could be observed by changing the V/III at 570°C. The initial screening experiment was meant to find the extreme V/III ratios, rather than the optimized, to quickly discern if this approach at all is viable. Originally the split was intended to be at 10, 75 and 155 V/III, but given fairly specular results of the 155 V/III, see figure 6.8b, the intended 75 V/III replaced 255 V/III as the extreme ends of the range were of interest.

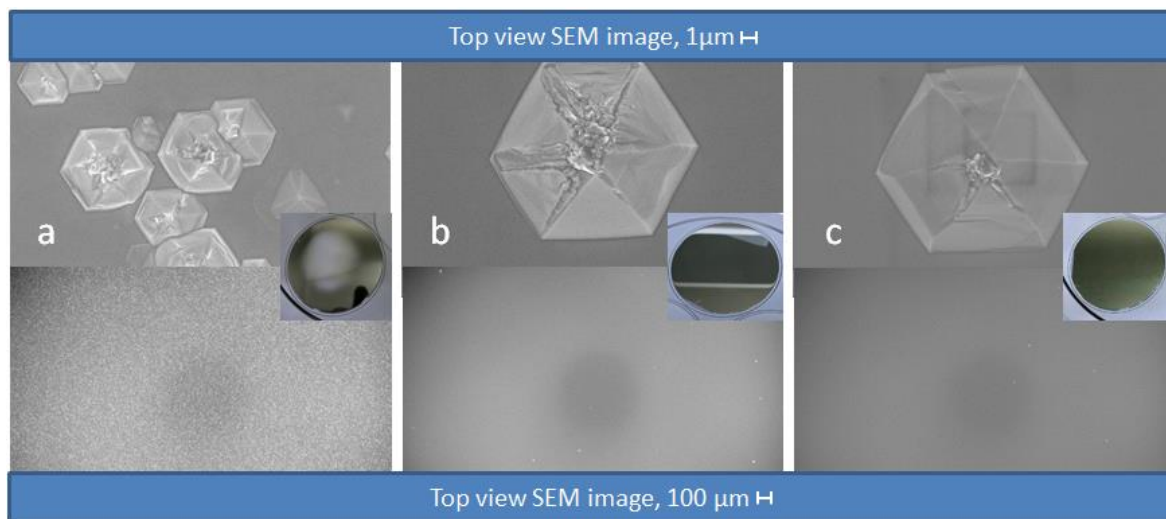


Figure 6.8: Initial V/III Screening at 570°C and 3.2e-5 mol/min TMGa.

- (a) 25V/III
- (b) 155 V/III
- (c) 230 V/III

At first optical inspection, it seems that the increased V/III suppressed the hillock formations and the growths become specular at extremely high V/III. This result is confusing. If the same surface reconstructions are achievable as MBE show in figure 3.4, a higher arsenic flow should result in 2×2 surface reconstructions, which according to Ruixia et al [14] should be worse than the $\sqrt{19} \times \sqrt{19}$ surface reconstructions for growth. Additionally these results are not in agreement with Kato's and Dzurko et al [26] results that a lower V/III should prevent hillock formations in (111)B growth. Thus the troubleshooting began.

The first step in the troubleshooting is to compare the test structure that is run first every MOCVD session and then compared to a baseline of these test structures. The test structure from this session

is compared to the baseline in figure 6.9 using XSEM and PL measurements.

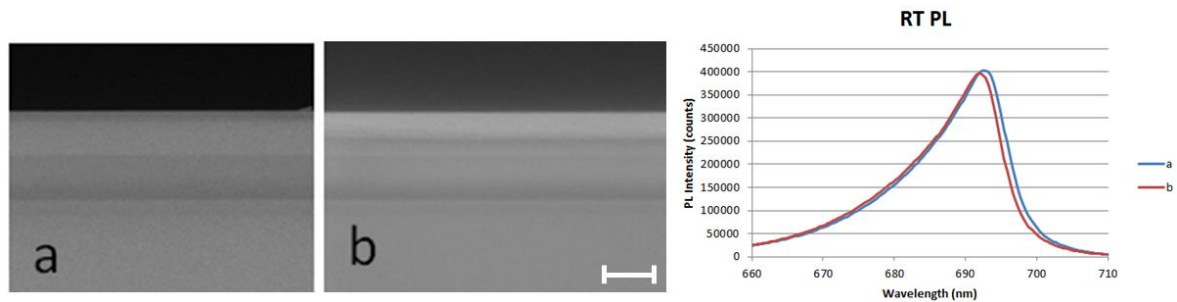


Figure 6.9: Comparison of test structures over two growth sessions. Same growth recipe was used. Scale bar is 1 μm . The test structure was also inspected with PL measurements.

(a) Old baseline test structure

(b) Test structure from same session as figure 6.8.

It should be noted that the contrast difference in figure 6.9b is likely a cleave artifact. From the test structure, there is no reason to believe that there is something wrong with MOCVD equipment.

To further test the issue, it was necessary to determine if anything had been grown at all on the “specular” runs. Given the confusing results of the figure 6.8 split, weighing as a characterization method was introduced. A rerun of the growth in figure 6.8b was made. There was no increase in weight at all. Apart from the few and far and between hillocks, there had been no growth at all.

Ultimately another test structure was grown during the same growth session it clearly showed that TMGa had depleted. It wasn't caught in the first test structure run since the TMGa source depleted in the middle of the growth session, most likely during the figure 6.8a growth. As this error led to an extensive troubleshooting, a lot of time was lost.

This is a good example of why growths in a split always should be randomized. A randomized split decouples the results in the split from gradual reactor state deterioration. Also this instance shows why the usage of in-line gas monitors, such as Epison that monitors the actual amount of material that enter the growth chamber, is a good practice in MOCVD development. Lastly this example highlights the importance of good characterization, had the wafers been properly characterized (weighed) from the start and a lot of time and effort could have been saved.

Even though most of the runs in the session was without TMGa, the failed run in figure 6.8a, which was supposed to be the best run, is still enough to motivate a change of approach.

6.4 Mid temperature GaAs growth development

This development is based on Moise et al [9] who found specular GaAs growth at 620°C using miscut wafers at a surprisingly high V/III of 54. They also used TEGa as precursor instead of TMGa.

To quantify surface roughness, reflectance of the wafers was measured using a F10-RT reflectometer from Filmetrics. As is already noted, the reflectance data from rough layers are likely convoluted by layer thickness, thus care is needed when comparing surface roughness of layers with different thicknesses.

The data on y axis in reflectance measurements can be treated as arbitrary units and is not normalized towards the reflectance of ungrown virgin GaAs wafers. Using the best approximation of Moise's growth settings [9] available with Aixtron 200/4, a V/III growth split was made.

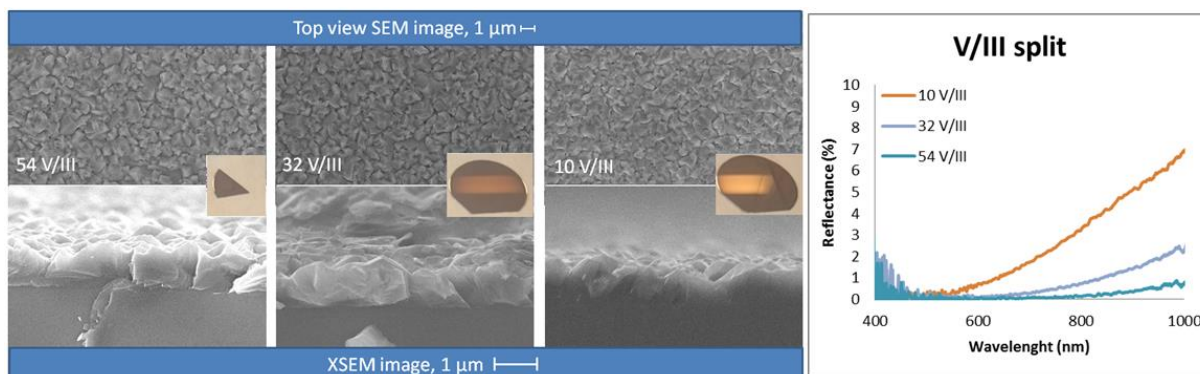


Figure 6.10: V/III split with TEGa as precursor at 620°C

There was a significant improvement in reflectance and layer morphology, lowering V/III ratios to 10 V/III. The thickness of growth was measured by weight to 0.79, 1.00 and 0.95 μm for 54, 32 and 10 V/III respectively. Based on the 10 V/III, a precursor split between TMGa and TEGa was made.

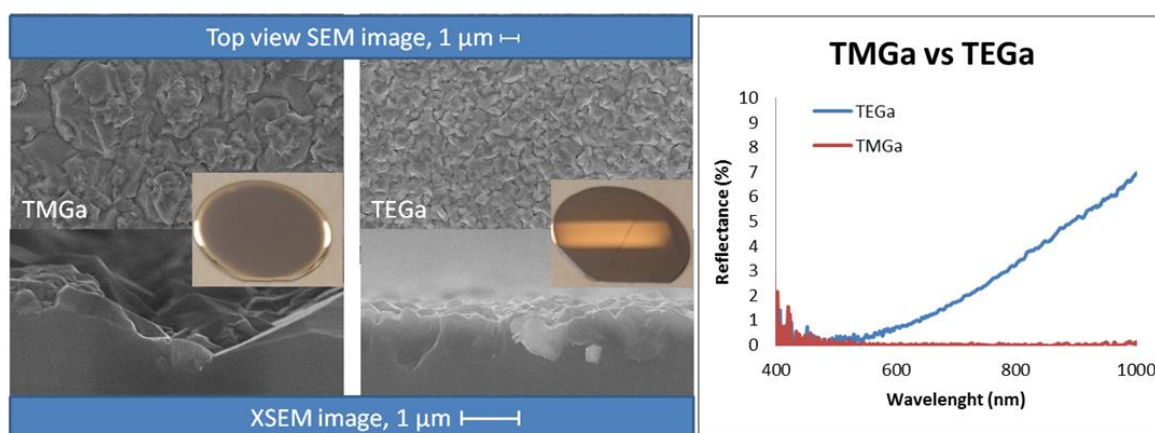


Figure 6.11: Growths at 620°C, 15 SLPM and 10 V/III

The TMGa growth was entirely unreflective apart from the edge defects. Thus TMGa was dismissed as precursor for these experiments. The believed reason why TEGa is a better gallium precursor is it has a lower pyrolysis temperature than TMGa. It is easier to decompose TEGa to gallium atoms as it enters the heated reactor, which is very relevant at lower temperatures. Using TEGa as a precursor might prevent the issue with the methyl radical preventing growth noted by Reep and Ghandi, see figure 3.3.

Continuing on the best V/III setting, a temperature split was made with lower temperatures.

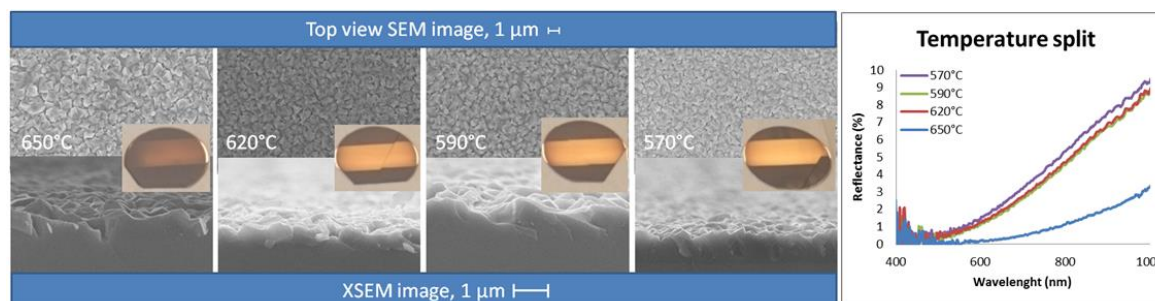


Figure 6.12: Temperature split at 10 V/III and 15 SLPM using TEGa as group III precursor

The growth was smoothest and the reflectance highest at 570°C. The thickness of growth was measured by weight to 1.04, 0.70, 0.64 and 0.81 μm for 650, 620, 590 and 570°C respectively. Even though the layer grown at 570°C was thicker, the reflectance was still higher, indicating that growth at 570°C is smoother. The growth at 570°C also looks morphologically better in top view SEM and XSEM.

Since total reactor flow and group III partial pressure can potentially change growth quality, a split was made with these parameters as well. The variable for reactor flow is standard liter per minute (SLPM). The group III partial pressure is called growth rate (GR) in figure 6.13 as growth rate is expected to linearly related to group III partial pressure.

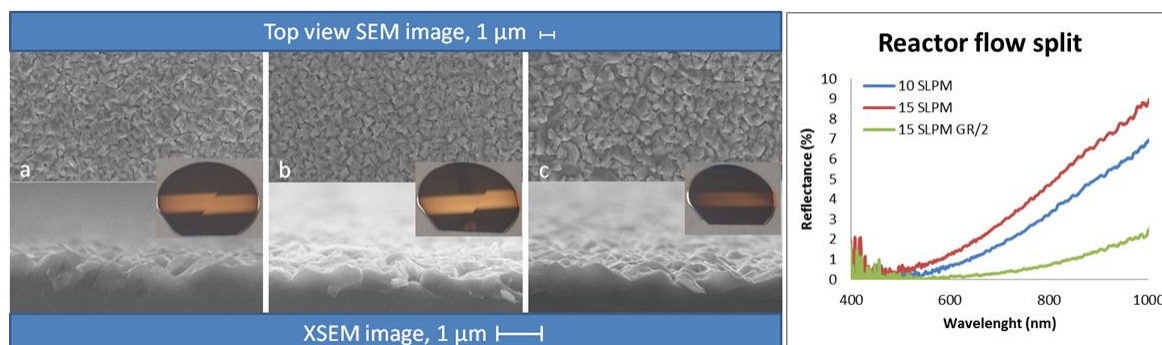


Figure 6.13: Growth rate and reactor flow split at 10 V/III and 620°C

(a) 10 slpm reactor flow, ~0.95 μm growth thickness

(b) 15 slpm reactor flow, ~0.70 μm growth thickness

(c) 15 slpm reactor flow, half source flows, double growth time, ~0.66 μm growth thickness

There was no significant growth improvement when the reactor was changed. Even though the 15 SLPM run is more reflective, it is significantly thinner than the 10 SLPM run. As is already noted, the reflectance data is convoluted by growth thickness. However, the unknown improvement or detriment of the lowering the reactor flow is not sufficient to motivate further investigation.

There was a significant detrimental effect of lowering the growth rate and increasing the growth time. The difference in reflectance between b and c is large while there is no significant difference in layer thickness. This gives a clear indication that the higher growth rate is better. However, the growth rate could not be increased any further as it was already maxed out. The growth rate is limited by size of the TEGa mass flow controller.

Given the results from these growth splits, the only parameter that is expected to still have some leverage for the growth quality is the V/III. Specifically it should be lowered further.

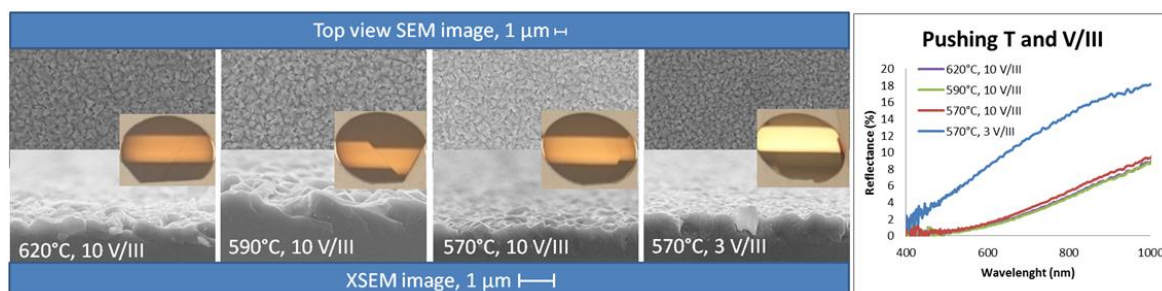


Figure 6.14: Continuation of temperature and V/III split. Results from earlier temperature splits are included in this image to provide a better overview of the effects of these growth parameters.

3 V/III shows a significant increase in reflectance and the growth is thicker than that of its 10 V/III counterpart, 0.86 μm vs 0.81 μm. The best possible setting in the Aixtron reactor is thus 570°C and 3 V/III, here is optimum V/III and temperature. However, this growth setting is still very rough and not even close to specular, the growth is polycrystalline and not at all suited for nanowire growth. The only way to continue this approach is to wait for miscut material. The medium temperature development was aborted until the ordered miscut material arrived from the manufacturer.

When the miscut material finally arrived, a repeat of the best setting was made. The reflectance was measured for both the miscut material and the non-miscut material and then compared to the reflectance of an epi ready GaAs wafer.

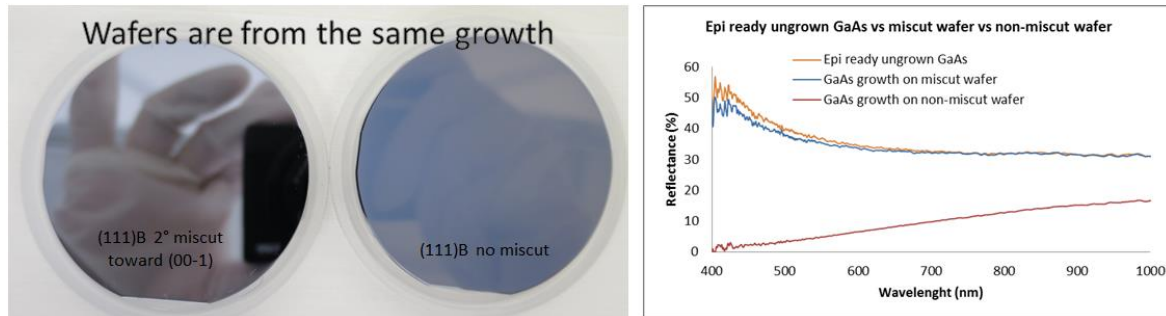


Figure 6.15: Rerun of best growth, same growth settings as figure 6.14d used. Both miscut and non-miscut material was included in this run.

Left, photograph comparing the growth on miscut and non-miscut wafers.

Right, reflectance measurement of the two grown wafers compared to reflectance measurements of epi-ready ungrown GaAs. The growth on the 2° miscut wafer is very close to the ungrown and epi-ready GaAs.

With the miscut substrate, a specular GaAs growth that meets the smoothness specification was finally achieved. The surface is specular. As is shown in figure 6.15, the (111)B GaAs wafer with 2° miscut toward [00-1] improves the quality of growth significantly compared to the growth on the wafer which is exactly (111)B oriented. The reflectance of the miscut wafer after growth material is almost identical to that of the epi-ready ungrown GaAs wafer. The thickness of the growth was 0.88 μm on the exactly (111)B oriented material and 0.77 μm on the miscut material. As the miscut material arrived very late in the development the high temperature approach had already yielded results and no AlGaAs growth was tested.

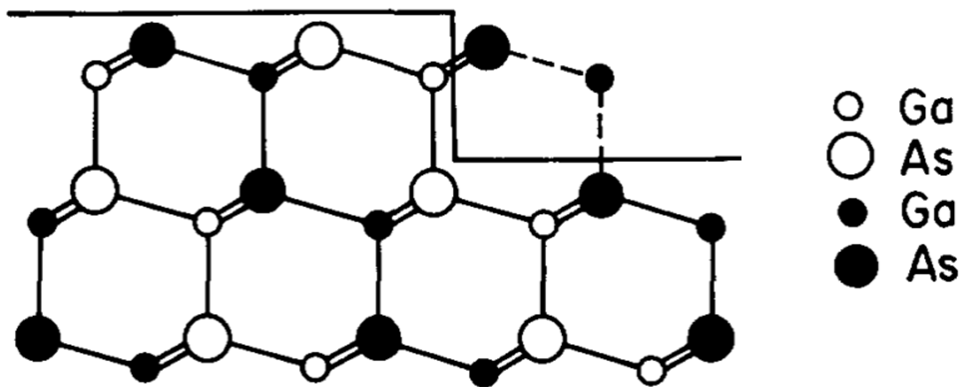


Figure 6.16: Schematic illustration of (111)B with miscut toward [00-1]. Image from [10].

The reason why the miscut improved the growth quality is that artificial steps are introduced which reduces the need to nucleate new layers. The lattice constant of GaAs is 5.65 \AA , which means that the distance between the biplanes, (one plane with gallium atoms and one plane with arsenic atoms) in $\langle 111 \rangle$ direction is 3.26 \AA . If the steps are evenly distributed in the 2° miscut wafer, one artificial step is introduced every 93 \AA on the wafer.

6.5 Continued high temperature GaAs growth development

While waiting for the miscut material for mid temperature growth development, a reactor with higher temperature capability than the Aixtron 200/4 was located. The Epiquip is an older reactor, but it can reach 800°C. Given the new temperature budget, the high temperature development could continue. The best high temperature recipe from Aixtron was translated to and compared to Epiquip

reactor.

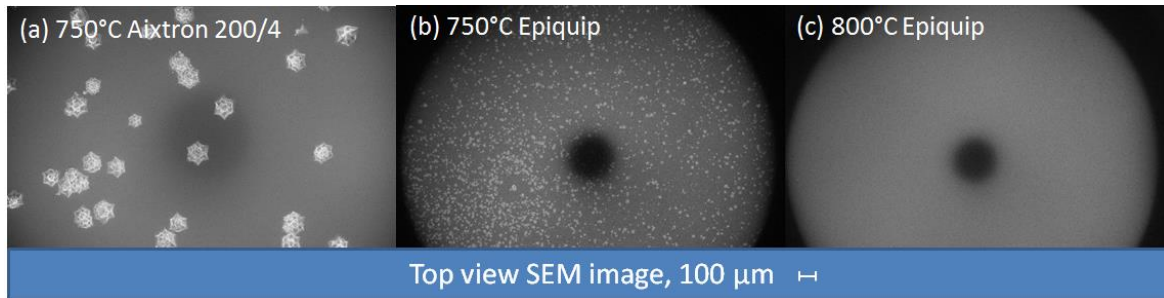


Figure 6.17: Initial growth screening in Epiquip reactor, temperature split.

- (a) Best growth in Aixtron, 20 V/III at 750°C
- (b) Aixtron settings in Epiquip reactor, 20 V/III at 750°C
- (c) Aixtron settings in Epiquip reactor, 20 V/III at 800°C

The growth quality between Aixtron and Epiquip at 750°C is not identical. First, it should also be noted that the TMGa partial pressure is three times higher in Epiquip. Also there might be discrepancies between thermocouples in Epiquip and Aixtron. The run at 800°C in Epiquip is specular. To determine the available growth window a V/III split was made using the 20 V/III at 800°C in Epiquip as a middle point.

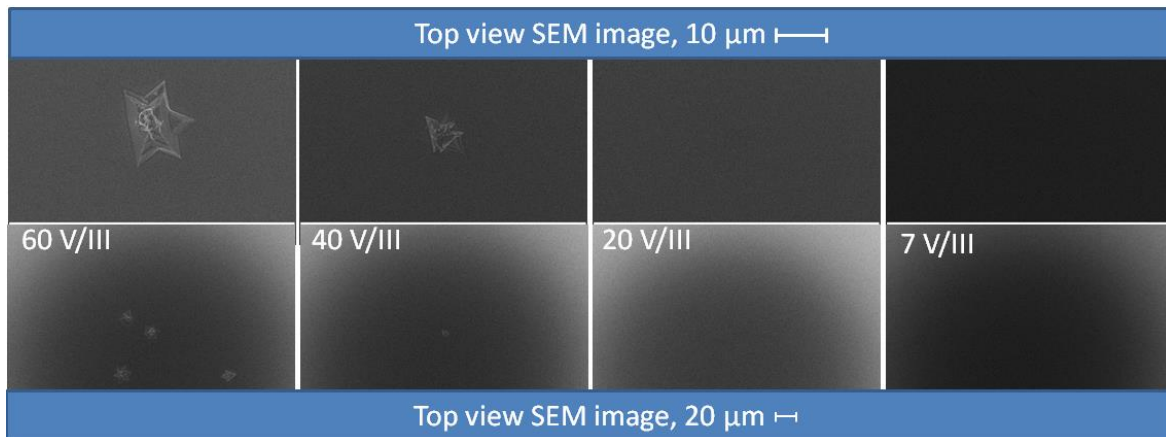


Figure 6.18: GaAs growth V/III split at 800°C. No hillocks were found in the samples with 7 and 20 V/III

No hillocks were observed at V/III:s lower than 20. At 40 V/III small hillocks were observed, even more and larger hillocks were found on the growth at 60 V/III. The trend is similar to the trend observed by Kato et al, but specular growth conditions were found at 800°C rather than the 875°C reported by Kato. Kato et al suspect that this V/III dependence is related to the migration lengths of the group III species as excessive amounts of AsH₃ should prevent gallium migration on the surface [8]. If the migration length of the gallium atom is too low, the misplaced adsorbed gallium atom may act as nucleation site for the hillocks. This argument would also support why there are fewer hillocks observed at higher temperatures, gallium migration length is dependent on temperature.

The chosen standard growth for GaAs was 20 V/III and 800°C. At temperatures as high as 800°C GaAs readily decomposes, unless kept in an environment already saturated with arsenic [25]. Even though both 7 and 20 V/III yielded in specular surfaces, 20 V/III was chosen as standard since it is more stable at higher temperatures with the higher AsH₃ flow.

6.6 High temperature AlGaAs growth development

As the GaAs growth condition is found, the next step is to start the AlGaAs development.

6.6.1 Comparison between TMAI and TMGa precursors

Comparing the formulas of TMGa, Ga(CH₃)₃, and TMAI, (Al(CH₃)₃)₂, it should be noted that TMAI is a dimer in its gaseous form. For every TMAI molecule, there are two Al atoms delivered to the reactor.

Further Al is notorious for being reactive and and 'sticky' inside the reactor. Aluminium has a high probability of sticking to positions that are not the optimal position in the crystal lattice, creating crystal defects and hillocks.

6.6.2 Strategy for finding the AlGaAs growth window

During the initial AlGaAs sacrificial layer development, focus was put on achieving high aluminium content. Ultimately, if the ELO literature is to be trusted, the preferable layer design would be to have a high aluminium molar fraction in ~10-20 nm thick sacrificial layers. However, thin layers are more stable to grow than thick layers, e.g. growing one atomic layer is less likely to fail than growing an infinitely thick layer. With this in mind, even if an unstable growth condition is found, the end growth might still look good. A failed run provides more information toward the growth window than a successful one, given that there is at least one successful run in the split. Thus by growing thicker layers than the optimum for the end result, the process of finding the AlGaAs growth window can be accelerated. The chosen thickness of the AlGaAs sacrificial layers was 50-100 nm, the reason for varying the thickness is to extract more data during the etch tests.

The strategy for pinpointing the AlGaAs growth window was to start with a small amount of TMAI/III and then gradually increase this amount until the growth goes bad. When the growth goes bad, other parameters are changed to improve quality of growth. The parameters which are likely to have an impact on the growth quality are V/III, temperature and miscut. There is no access to miscut material and the temperature is already at its maximum for the Epiquep. Growth rate is not expected to have any impact on growth quality, given the initial growth rate screening during the GaAs growth window screening. As such the only parameter that remains to tune is the input V/III ratio.

For AlGaAs layers the growth strategy was to replace input TMGa with TMAI and to keep the group III input partial pressure of these gases constant. The relationship between input TMAI and total input group III (TMAI/III) was used as an input metric. When TMGa is replaced with TMAI, more group III atoms are introduced into the reactor, since TMAI is a dimer. As will be shown, it would have been preferable to keep the amount of group III atoms constant rather than input partial pressures. This was an oversight during this thesis project.

6.6.3 Initial AlGaAs sacrificial layer growth

The first split that was made increasing TMAI/III until the growth quality became poor. To improve growth quality, V/III was lowered.

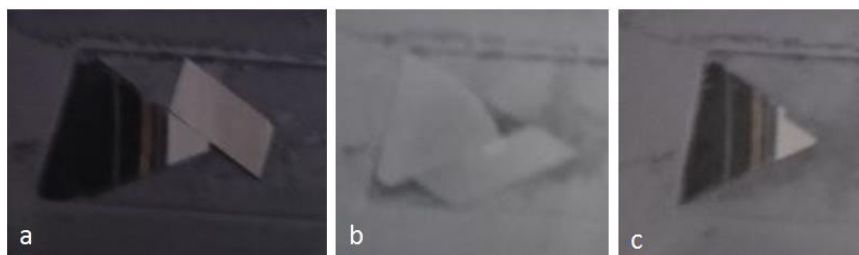


Figure 6.19: Initial indications of higher TMAI/III being sensitive to V/III.

(a) 16 % TMAI/III, 21 V/III

(b) 24 % TMAI/III, 21 V/III

(c) 24 % TMAI/III, 10 V/III

The optical inspection of the initial AlGaAs split, figure 6.19, reveals that the growth quality is very sensitive to V/III, even more sensitive than GaAs growths. The increased sensitivity is attributed to the difference between TMAI and TMGa as precursors. When V/III is too high during AlGaAs growth, surface becomes uneven and polycrystalline. This trend was assumed to continue at higher TMAI/III. In upcoming growths, V/III was lowered with increasing TMAI/III.

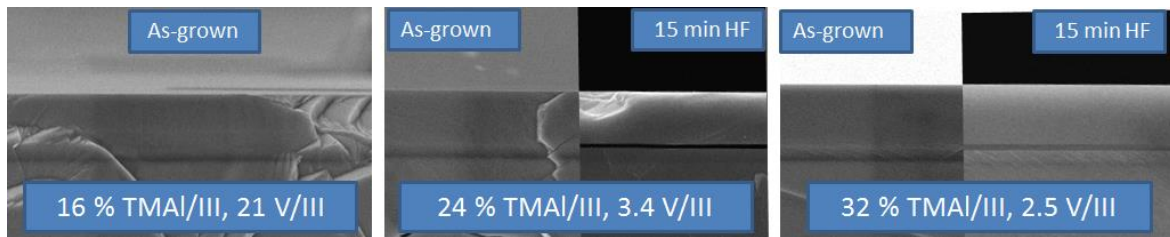


Figure 6.20: AlGaAs growths with specular surface, the two runs with higher Al content was also characterized by HF stain etch for 15 minutes.

The AlGaAs layers in this split had the same growth time of 30 seconds. 30 seconds was to guarantee that the AlGaAs layers would be visible in SEM and to amplify any growth instability. Note in the HF stained layers that the thicknesses of the AlGaAs layers are different. The 24 % TMAI/III is ~67nm where the 32% is ~93nm, this is likely the reason why the 24 % TMAI/III run etched faster than the 32 % TMAI/III run. The GaAs caps were grown thick to provide support for etch tests and to test if the AlGaAs sacrificial layer growth would have any impact on the continued GaAs growth.

The etch rates from these growths were much lower than needed, much less than a micron was etched in the 24 % TMAI/III and the etching is barely noticeable in the 32 % TMAI/III which is thicker. Using the ELO etch rate discussion from section 3.6.1, this indicates that incorporated aluminium content is lower than 60%. Kumar et al [23] showed that AlGaAs layers as thick as 2,5 μ m should have an etch rate at approximately 1 μ m/minute, see figure 3.7. Without knowing the exact Al content yet in these layers, we know that we need to increase Al-content further to have manageable etch rates.

The second way accelerate the etch rate is to make the layers thinner, instead of growing the layers 50-100 nm thick, they could be grown 10-20 nm thick. The scheme to grow the layer thinner was not employed in the upcoming splits for three reasons. First, it is preferable to have similar structures be able to make comparisons between the growth runs. Second, according to the data from Kumar in figure 3.7 etch rates of approximately 10 μ m/min, which is sufficient for the initial tests, are achievable given that the aluminium content is high. Third and most importantly, a successful thicker AlGaAs growth can be considered much more stable than a successful thinner growth. It is preferable to find out that the growth condition is unstable early in the development.

6.6.4 Aluminium content maximization

The next Epiquip session was focused on maximizing Al content in AlGaAs layer. A firm understanding of AlGaAs growth principles is needed to optimize the growth. The goal of this session was to find the growth window that relates V/III to TMAI/III.

It should be noted that between the two growth sessions in the Epiquip reactor, the AsH₃ bottle source and its MFC had been changed. Therefore, all the recipes needed to be adjusted slightly. Using an approximation of the best growth from previous session the following V/III split was made with 35 % TMAI/III.



Figure 6.21: V/III split at 35 % TMAI/III

1.8 V/III is too low and group III droplets are observed. The reason for the droplet formation is that there are not enough group V atoms during growth to match the amount of group III atoms. In analogy with the GaAs growth development, 26.6 V/III is too high and the migration lengths of the

group III atoms become too low. Thus some of the misplaced group III atoms have misnucleated and the material becomes polycrystalline. Next a V/III was set up for 50 TMAI/III.



Figure 6.22: V/III split at 50 % TMAI/III. Note that no “perfect” material grown at 50 % TMAI/III, approximately 1 triangular defect was found / $40 \mu\text{m}^2$

The same argument is proposed for the split made in figure 6.21 as figure 6.22. The difference is that the gallium droplets are formed already at 4.7 V/III, where the 5.3 V/III in 35 % TMAI/III yielded good material quality. Also the 13.3 V/III started to show signs of the triangular hole defects, similar in shape to the growths where the V/III is too high. This indicating that this growth is very close to the upper V/III limit. The conclusion from these two splits is that the specular growth window becomes narrower as more aluminium is introduced in the reactor.

Finally, an attempt at pushing the aluminium-content in the AlGaAs layer was made, using best results from growth splits in figure 6.21 and figure 6.22 and extrapolating for 70 % TMAI/III.

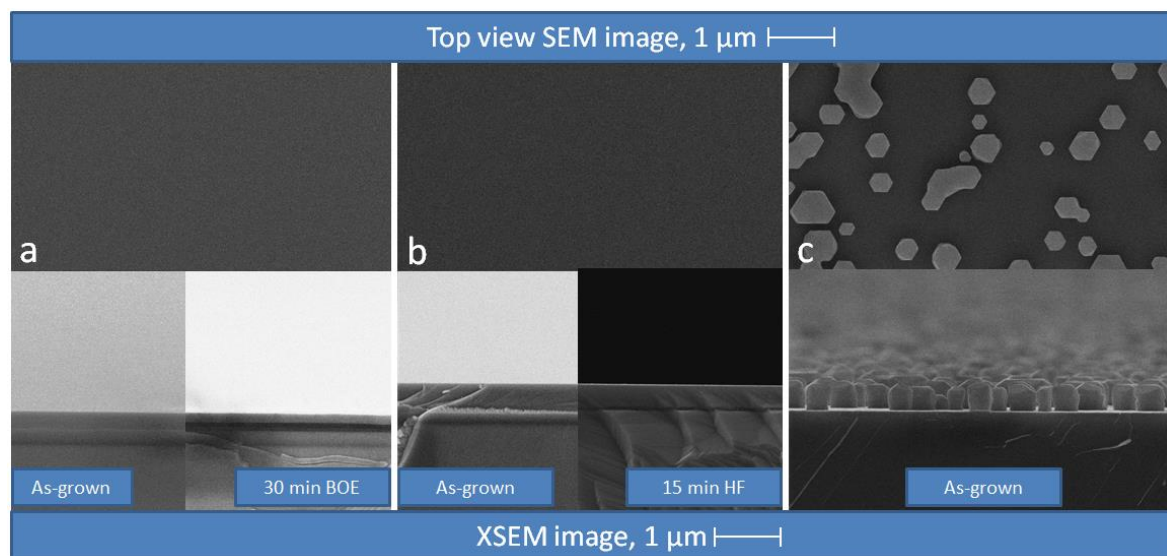


Figure 6.23: TMAI/III split at best found growth settings. When possible the layers were etched either with buffered oxide etch (BOE) or HF to enhance the contrast between the layers in XSEM.

- (a) 35 % TMAI/III, 13.2 V/III
- (b) 50 % TMAI/III, 13.3 V/III
- (c) 70 % TMAI/III, 10.7 V/III

No good growth condition was found at higher Al/III than 50 %. At 70 % TMAI/III group III droplets are observed at 10,7 V/III which was expected to be the upper limit given the results in the growth split from figure 6.22.

The run at 70 % TMAI/III further strengthens the conclusion that the V/III growth window becomes narrower with higher TMAI/III. The growth window is the widest at 0 TMAI/III (growing GaAs) and the narrowest at high TMAI/III. A schematic growth window with the relationship between TMAI/III and V/III is drawn in figure 6.24 below.

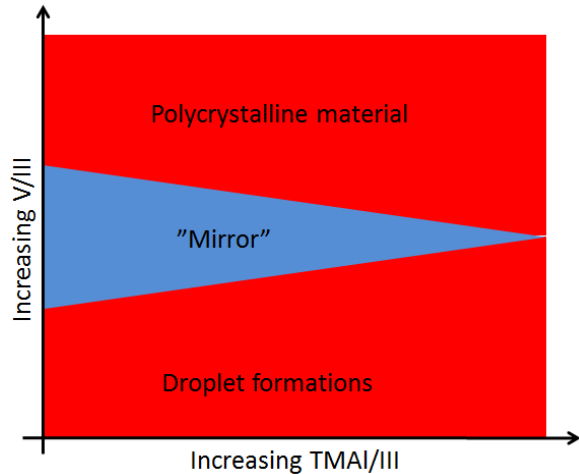


Figure 6.24: Schematic image of AlGaAs growth on (111)B material summarizing the runs in figure 6.19- figure 6.23. The higher the TMAI/III is, the narrower the growth window becomes. At too high TMAI/III the bad growth area with droplet formation starts to overlap with the polycrystalline material area.

6.6.5 Understanding Al-incorporation in (111)B growths

To find the exact amount of aluminium that was incorporated, three samples of varying TMAI/III were characterized by SIMS. The selected samples were 24 %, 35 % and 50 % TMAI/III.

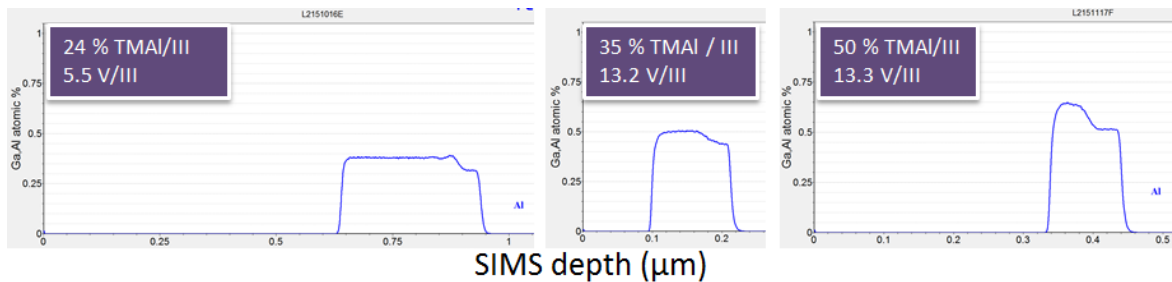


Figure 6.25: SIMS data from three different TMAI/III settings. The graphs show the aluminium content vs the depth of the SIMS. A depth of 0 μm corresponds to the surface of the sample. Note that there is an initial plateau on the AlGaAs layers, during the initial AlGaAs growth, the aluminium incorporation is lower.

Initial AlGaAs plateau speculations

The reason behind initial hump during the first 50-60 nm growth of is unknown. The input precursors were kept constant throughout the growth AlGaAs growth. I have not found any literature with the same behavior and unless this is an epitaxial hardware failure, I can only propose the following speculations:

1. As aluminium is first introduced in the reactor, the reactor and its inner walls contains no aluminium. The reactor walls has a higher affinity for aluminium than the substrate and will consume TMAI until they are saturated, thus the true Al concentration in the atmosphere reactor is initially lower. However, if this was the case there should be a gradual increase in the aluminium concentration, not a plateau.
2. The surface properties of the substrate change during initial AlGaAs growth, allowing for more aluminium incorporation. Maybe there is a transition from one surface reconstruction to another. This explanation could explain the binary growth behavior, with two aluminium concentration plateaus.

For the remainder of this thesis, the aluminium concentration after the initial plateau is considered the correct value and all calculations are based on this value.

Data from the SIMS measurements are summarized in table 6.2 below.

Input TMAI/III (%)	True input Al/III (%)	Measured Al concentraion (%)	V/III	True V/III	Input III (mol/min)	True III (mol/min)	Actual growth rate (nm/s)	Normalized growth rate (nm/s)**
0*	0	0	20.3	20.3	2.04E-05	2.04E-05	1.18	1.18
24	39	38	5.5	4.4	2.94E-05	3.65E-05	2.50	1.40
35	52	51	13.2	9.8	2.04E-05	2.75E-05	1.87	1.38
50	67	65	13.3	8.9	2.02E-05	3.02E-05	2.36	1.59

*0 % TMAI/III data point from the GaAs cap

**Growth rates were normalized towards the molar flows of the GaAs growth

Table 6.2: Table summarizing data from growth recipes and SIMS measurements. In the “true” data points it has been compensated for the dimer nature of TMAI and the amount of group III atoms are actually counted.

When determining layer thickness for growth rates, layer thickness data from SIMS data was used, rather than from SEM measurements. $Al_{0.51}Ga_{0.49}As$

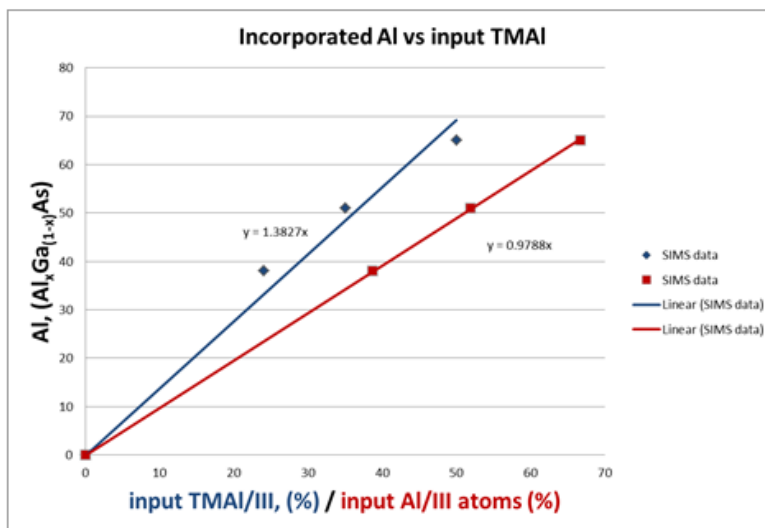


Figure 6.26: Incorporated Al vs input TMAI/III and true Al/III.

When it is taken into consideration that TMAI has two group III atoms the data can be fitted linearly, see figure 6.26. There is almost a 1:1 correlation between input Al/III and the measured Al concentration in the AlGaAs layer. This data also correspond very well to what Stringfellow claim about TMAI incorporation in (100) oriented GaAs [3].

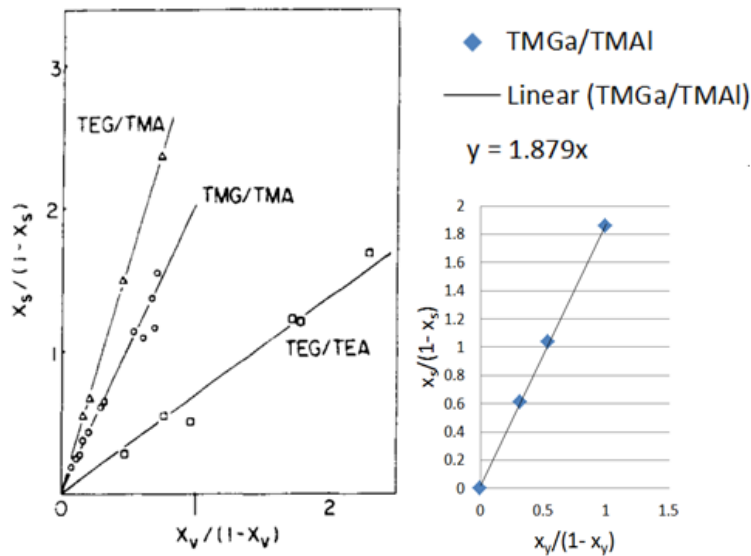


Figure 6.27: Left, TMAI incorporation data from Stringfellow [3]. Right, SIMS data from growths plotted the same way as Stringfellow.

In figure 6.27 the distribution coefficient of TMAI is plotted, both from Stringfellow [3] and from the acquired SIMS data. In Stringfellow's data this coefficient is 2, i.e. gallium atoms are as likely to incorporate as the aluminium atoms. The distribution coefficient of 1.88 indicates that the gallium atoms are slightly more likely to be incorporated in the Epiquip reactor. This is shown more clearly in figure 6.26, where input aluminium atoms are plotted vs incorporated aluminium. Which type of group III atom that is incorporated seem to be independent on all other parameters than the input ratio between the two precursors. Given this trend, looking at input aluminium/III in atoms would have been a more intuitive approach than input TMAI/III.

The shape of the schematic growth window with TMAI/III vs V/III in figure 6.24 would change slightly when looking at the input of group III atoms rather than molecules. The border toward the droplet formation would be flatter and the border toward the polycrystalline material would become steeper.

6.6.6 AlGaAs layer growth stability

Thicker AlGaAs layers were grown to test the stability of the best growth conditions.

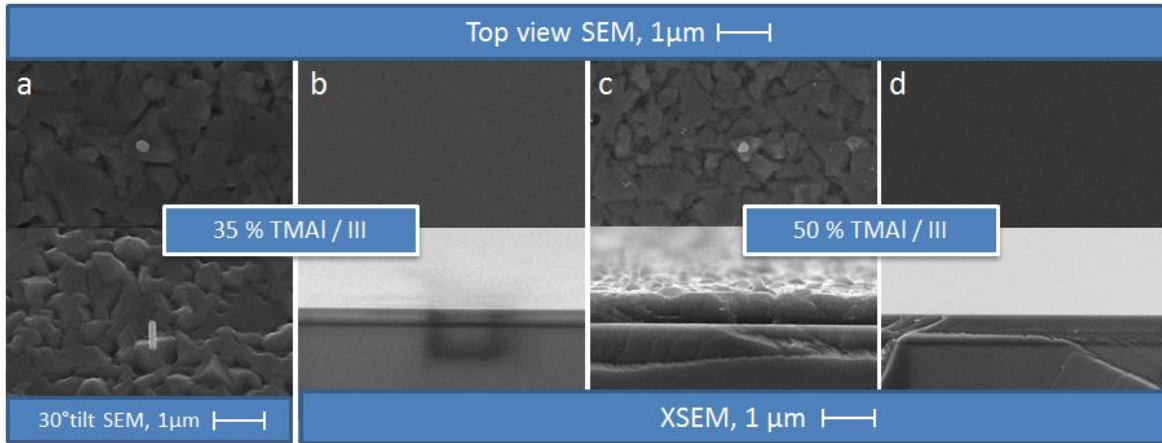


Figure 6.28: Growth time split, using same settings as Figure 6.23.

- (a) Nominally ~450nm AlGaAs growth and ~200nm nm GaAs growth
- (b) 112 nm AlGaAs growth, 100 nm GaAs growth
- (c) Nominally ~550 nm AlGaAs growth, ~100 nm GaAs growth
- (d) 106 nm AlGaAs growth, 335 nm GaAs growth

The failing growth is independent of GaAs cap growth time. In the growth split in figure 6.20 thick layers of GaAs were grown on top of the AlGaAs layer.

It is unclear why the growth fails when thicker sacrificial layers are grown. One theory is that the growth window that is found is only the layer nucleation setting. After the sacrificial layer has been nucleated and growth has started, growth settings need to be changed to keep growth stable. In figure 6.28a and figure 6.28c, there are even nanowires grown. Sometime during growth, group III droplets has formed and nucleated into nanowires. If that is the case V/III need to be increased as the growth is started to prevent the group III droplet formation, just as was shown in figure 6.21 and figure 6.22.

6.7 Nanowire growth on ELO material

One of the specifications of the ELO growths is that nanowire growth should not be impacted by the layers. Ultimately the gold seeds need to be imprinted, but the imprint process is time consuming and demands a lot of resources. In contrast gold aerosol deposition is quick and fairly cheap. Nanowire growth catalyzed by aerosols will yield the required test data much quicker than imprinting would. Thus, the rapid gold aerosol deposition was used. One small piece of every grown ALGaAs sample was tested and no impact on nanowire growth was discovered.

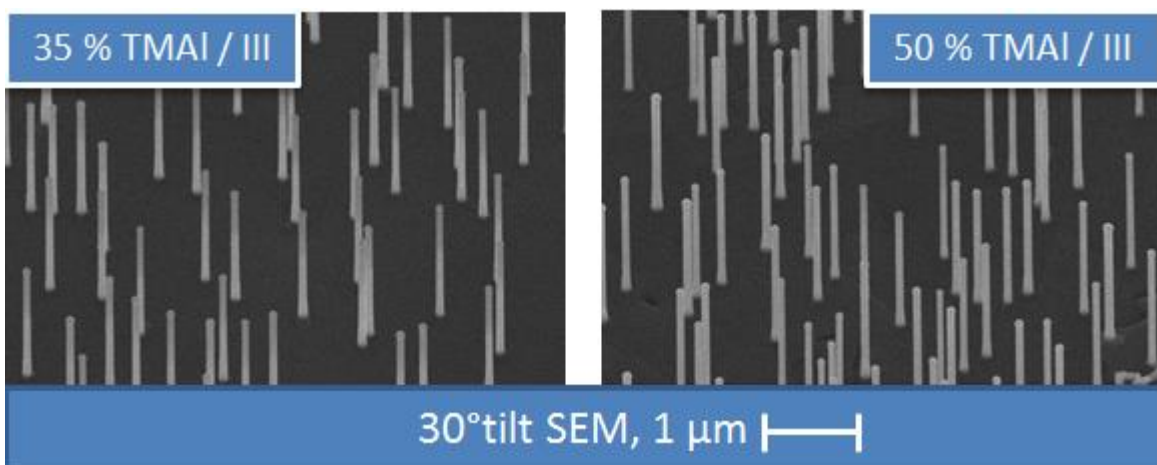


Figure 6.29: Nanowire growth on ELO material. In the 50 TMAI/III, the previously noted defects are visible. Nanowire morphology does not seem to be affected by these defects.

Catalyzed by the gold aerosols, nanowires were successfully grown on ELO material. No adjustments had to be made to nanowire growth recipes to allow nanowire growth on ELO material. As the aerosol catalyzed nanowire growth was unimpeded by the ELO layers, the initial conclusion is that the nanowire growth specification is met. To truly test if the material meets this specification, the nanowire growth need to be performed on imprinted material.

6.8 Etching the AlGaAs release layers

As the ELO layers were grown with focus on understanding the AlGaAs growth rather than maximizing their etchability, ultimately the most etchable structure was not grown.

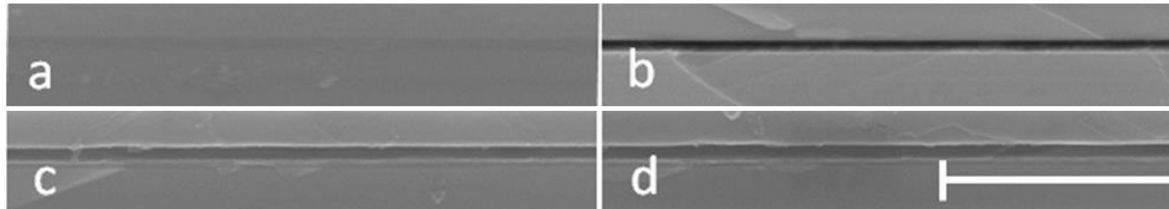


Figure 6.30: XSEM of 1 hour 48% HF stain etch on different ELO materials. Scale bar is 1 μm

(a) 50 nm $\text{Al}_{0.38}\text{Ga}_{0.62}\text{As}$

(b) 48 nm $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$

(c) 94 nm $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$

(d) 93 nm $\text{Al}_{0.62}\text{Ga}_{0.48}\text{As}$

To obtain good etch rates it is required that the layers are very thin and have very high Al-content. This is shown in figure 6.30. Even though the lateral etch rates ultimately were too low to get quantifiable data, $\gg 1 \mu\text{m}$ was etched in 1 hour 48 % HF, the results were good enough to acquire qualitative data.

Refer to figure 6.30 for the following reasoning: Comparing a with b, layers that have similar thickness but different aluminum content, it is shown that $\text{Al}_{0.38}\text{Ga}_{0.62}\text{As}$ etch significantly slower than $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$. Comparing b with c, samples with similar aluminum content but different layer thickness, it is shown that 94 nm layers etch significantly slower than the 48 nm layers. Finally comparing b with d, samples with different thicknesses and different aluminum content in the layers, it is shown that the thinner layer with lower aluminum content etched faster. This would indicate that lateral etch rate perpendicular to $\langle 111 \rangle$ have a heavier dependence on layer thickness than aluminum content.

The etch rates are not in agreement with what was claimed by Kumar et al in figure 3.7. The d layer in figure 6.30 had an aluminum concentration >0.6 and etched $\ll 1 \mu\text{m}$ in 60 minutes. Given this aluminum concentration, the etch rate should be approximately $1 \mu\text{m}/\text{min}$ according to Kumar.

One possible explanation for the slower etch rate is that the atoms in (111) planes are tightly packed whereas the atoms in (100) planes are not. Given that the etch occur perpendicular to the planes, the (111) planes may be more stable to etching than the (100) planes, see figure 6.31 below.

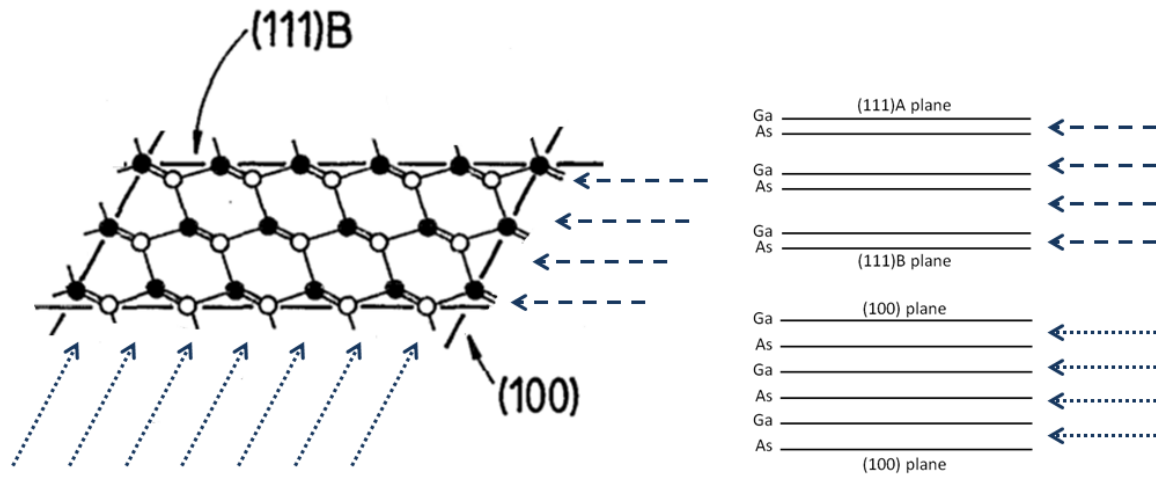


Figure 6.31: Comparison between perpendicular etching of the (100) planes and the (111) planes. Dashed lines represent etch direction of the (111) planes and dotted lines represent etching of the (100) planes.

The planes perpendicular to $\langle 100 \rangle$ have rotational symmetry, where the planes perpendicular to $\langle 111 \rangle$ have not this rotational symmetry. The different arrangement of the atoms in the planes may explain the difference in etch rates between the AlGaAs layer grown in this thesis, and the tests performed by Kumar [23].

6.9 Summary of the results

Specification	Achieved	Shown in
Flat, specular surface	Yes	Figure 6.23
Monocrystalline GaAs (111)B supporting layer	Yes, $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$, Almost, $\text{Al}_{0.65}\text{Ga}_{0.35}\text{As}$	Figure 6.23
$\text{Al}_{>0.60}\text{Ga}_{<0.40}\text{As}$ sacrificial layer	Yes, with some surface defects	Figure 6.23
Etchable sacrificial layers	No	Figure 6.30
Nanowire growth on ELO-layers	Yes	Figure 6.29

Table 6.3: Summary of the specifications and if they were met.

No layers were grown that fully met the specifications. Initially $\text{Al}_{>0.6}\text{Ga}_{<0.4}\text{As}$ sacrificial layer was believed to be sufficient, but even higher aluminum concentrations seem to be necessary to etch layers thicker than 90 nm with etch rates $>1 \mu\text{m}/\text{min}$ when etching is perpendicular to $\langle 111 \rangle$. Possibly the layers could be grown thinner in order to accelerate the etch rates. The initial AlGaAs plateau of the 50 % TMAI/III growth setting yielded $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$. If this was grown 10 nm thick, the etch rate might be accelerated sufficiently to be etchable with lateral etch rates $>1 \mu\text{m}/\text{min}$.

Moise et al's [9] (111)B GaAs growth was reproduced, but was achieved at 570°C instead of 625°C using 2° miscut wafers. Kato et al's [8] work was extended upon, the aluminum content in the AlGaAs was significantly increased. Kato demonstrated specular $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ at 875°C , where specular $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$ was demonstrated in this thesis at 800°C . For every ELO-structure grown, including $\text{Al}_{0.65}\text{Ga}_{0.35}\text{As}$, the growth quality sufficient to support nanowires. But at the $\text{Al}_{0.65}\text{Ga}_{0.35}\text{As}$ triangular hole defects were observed on the GaAs cap, given that the GaAs cap was grown with specular settings, these hole defects are attributed to poor AlGaAs growth quality. Even though these holes did not have an impact on the nanowire growth, it could be detrimental as the cap is needed to

protect the nanowires during the etch step. Ultimately the $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$ was the best layer grown with specular surface.

There are three ways to further improve the ELO-layers, using the same reactor as in this thesis. First, with some fine-tuning of the V/III for the 50 % TMAI/III AlGaAs growth, the triangular growth defects could likely be prevented. Second, it is plausible that if thinner layers were grown higher input aluminum/III would also have yielded specular surfaces. Third, all AlGaAs growths in this thesis were run on exactly (111)B oriented substrates. Given the improvement shown with the miscut wafers during the mid-temperature GaAs development, it is plausible that the miscut wafers would provide the same headroom for growth quality at higher temperature as well.

Nanowires were successfully grown on the ELO-layers. No additional degradation in growth quality, such as an increase in misnucleation or kinking, during growth was observed for the nanowire growth due to the ELO layers.

Even though the specifications were not fully met it is believed that ELO of nanowire membranes are possible using the same growth equipment as in this thesis. Ultimately there were only two growth sessions using the Epique reactor in this thesis, if there had been time for a third session, I believe that the specifications for the ELO-layers could have been fully met using the strategies mentioned above.

7 Summary

This thesis work is aimed at demonstrating ELO on samples containing gold-catalyzed nanowires. The purpose of this thesis is to continue the work of Åberg et al [2] and demonstrate that the nanowires used in Åberg's work can be removed from the substrate used during nanowire growth. This means that the nanowires must be of GaAs and gold-catalyzed. The needed process flow to demonstrate this is shown in figure 1.3. Ultimately the project was boiled down to developing ELO-layers compatible with gold-catalyzed GaAs nanowire growth, as that the rest of the steps are well understood in literature and will fall nicely into place if the ELO-layers are well designed. Thus if the ELO-layers are compatible with the nanowire growth and the sacrificial layer is selectively etchable, this project can be considered successful.

The chosen design of the ELO layers is an AlGaAs sacrificial layer with a GaAs capping. AlGaAs is the chosen material for the sacrificial layer, because it is lattice matched to GaAs and has excellent etch selectivity to GaAs and lateral etch rates $>1 \mu\text{m}$ at $\text{Al}_{>0.6}\text{Ga}_{<0.4}\text{As}$ [23]. GaAs is the chosen capping layer material to make the layers compatible with GaAs nanowire growth.

That the nanowires must be gold-catalyzed imposes an important restriction on the project, which makes it more challenging than the ELO covered in literature. The substrates need be oriented in the (111)B direction, as this is the growth direction of the nanowires [16]. Growth of GaAs and AlGaAs on (100) oriented substrates is well understood [3], but there is very little literature detailing GaAs and AlGaAs growth on (111)B oriented substrates.

The epitaxial growth of the ELO-layers on (111)B oriented substrates in this thesis is mainly based on two papers in literature. First, Moise et al [9] found GaAs and $\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$ growth settings at 625°C , V/III at 54 and using 2° miscut wafers. Moise's work on GaAs was reproduced in an Aixtron 200/4 reactor at 570°C using 2° miscut wafers. Second, Kato et al [8] did an excellent survey of high-temperature GaAs and AlGaAs growth. They demonstrated specular GaAs growth at $875\text{-}900^\circ\text{C}$ and V/III ratios of 10-20. They note that hillocks will start to form at lower temperatures and higher V/III ratios, the hillock density can be reduced by usage of miscut material. Ultimately they demonstrate an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ growth. Kato's work at higher temperatures was extended upon, $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$ was grown on exactly (111)B oriented GaAs at 800°C . Growth conditions that are very close to specular

and are likely to yield specular surfaces with further V/III tweaking were found for $\text{Al}_{0.65}\text{Ga}_{0.35}\text{As}$ sacrificial layers.

Two interesting features of AlGaAs growth on (111)B was observed, first there was initial plateau with lower aluminum content as the AlGaAs growth was initiated. Second the AlGaAs growth at higher input aluminum was not stable for growths thicker than 400 nm. There were formations of group III droplets during the growth, indicating that the growth settings of the AlGaAs sacrificial need to be changed during growth to grow thick layers.

To accelerate the feedback loops aerosol deposition was used instead of imprint to deposit the gold nanowire seeds. Although not part of the process flow, the nanowires grown from aerosols will provide sufficient information of the nanowire growth on ELO-layers to make an educated decision. The nanowire growth was unimpeded by the ELO-layers, even on the $\text{Al}_{0.65}\text{Ga}_{0.35}\text{As}$ layers where small holes were observed in the surface. No additional kinking or misnucleation in the nanowire growth was observed.

Ultimately the lateral etch rate of the layers was too slow. All the grown sacrificial layers had a lateral etch $\ll 1 \mu\text{m}/\text{min}$ in 48 % HF. Kumar et al had indicated that $\text{Al}_{>0.6}\text{Ga}_{<0.4}\text{As}$ should be sufficient to have etch rates $>1 \mu\text{m}$ in 48 % HF [23]. This discrepancy in etch rates is attributed to different etch directions. Kumar etched perpendicular to $\langle 100 \rangle$ where the layers in this thesis were etched perpendicular to $\langle 111 \rangle$. It was shown that a 48nm thick layer of $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$ had a higher lateral etch rate than a 93 nm thick layer of $\text{Al}_{0.62}\text{Ga}_{0.48}\text{As}$. This indicates that lateral etching perpendicular to $\langle 111 \rangle$ is more thickness sensitive than lateral etching perpendicular to $\langle 100 \rangle$.

Even though the specifications were not fully met it is believed that ELO of nanowire membranes are possible using the same growth equipment as in this thesis.

8 Further work and outline

8.1 Demonstrating ELO with nanowires

With the work of this thesis as a starting point, I believe it would be fairly straight-forward to actually demonstrate ELO on samples with nanowires.

It is necessary to manufacture etchable ELO-layers on (111)B oriented substrates. The layers grown during this work could be improved in two ways.

- The aluminum content in the sacrificial layer can be further increased. The following schemes are proposed to increase the aluminum content:
 - Use reactor that allows for higher temperatures. Given the significant growth quality increase observed when going from 750°C to 800°C, a further increase in temperature is believed to provide additional head-room for aluminum incorporation.
 - Use miscut wafers for growth of the AlGaAs layers. Miscut wafers were not used during the AlGaAs development in this thesis. Given the growth quality increase that was observed in the mid temperature growth, miscut material is believed to provide additional head-room for the high temperature growths as well.
It should be noted that macrosteps have been shown when AlGaAs has been grown on miscut material [8].
- The sacrificial AlGaAs layer can be grown thinner. As was observed in figure 3.8 and figure 6.30, thinner layers are etched faster both for (100) and (111)B. Use the best growth setting which was found in this thesis and grow thinner sacrificial layers. The initial AlGaAs plateau of the 50 % TMAI/III growth setting yielded $\text{Al}_{0.51}\text{Ga}_{0.49}\text{As}$. If this was grown 10 nm thick, the etch rate might be accelerated sufficient to have lateral etch rate $> 1 \mu\text{m}$. Additionally if the

sacrificial layer is grown thinner, the small triangular defects which were observed with this growth setting might disappear since the growth of thinner layers is more stable.

The actual etchant can be improved. Usage of a hydrophilic agent during the etching, such as acetone, will decrease the contact angle between etchant and substrate. This prevents re-deposition as the sample is being etched. This will also increase the etch rate.

Another way to improve the etching-behavior is to use a stabilization layer with a slight strain, such as black wax, that will continuously peel back the device layer as the sacrificial layer etches.

8.2 Fully understanding the AlGaAs growth

It would be of interest to fully understand why there is a plateau during the initial AlGaAs growth. If this is fully understood, it might ultimately be leveraged to increase the aluminum content in the sacrificial layer further.

Additionally, it would be of interest to understand why the AlGaAs growth is not stable for thick layers as was shown in section 6.6.6. This is not as crucial to achieve the necessary ELO structure, given that the sacrificial layer should ultimately be very thin. However, since it is not fully understood it would be interesting to do some additional tests. My best guess is that the growth condition that is found is only the nucleation conditions and it is necessary to raise the V/III after a certain amount of growth to stabilize it.

8.3 Understanding the effect of miscut material

Moise et al [9] found growth conditions at 625°C whereas the optimum low temperature growth setting found for the Aixtron 200/4 was at 570°C. It would be of interest to examine exactly how much the 2° miscut extend the growth window on (111)B.

9 References

- [1] J. Wallentin, N. Anttu, D. Asoli, M. Huffman, I. Aberg, M. H. Magnusson, G. Siefer, P. Fuss-Kailuweit, F. Dimroth, B. Witzigmann, H. Q. Xu, L. Samuelson, K. Deppert, and M. T. Borgstrom, "InP Nanowire Array Solar Cells Achieving 13.8% Efficiency by Exceeding the Ray Optics Limit," *Science* (80-.), vol. 339, no. 6123, pp. 1057–1060, 2013.
- [2] I. Åberg, G. Vescovi, D. Asoli, U. Naseem, J. P. Gilboy, C. Sundvall, A. Dahlgren, K. E. Svensson, N. Anttu, M. T. Björk, L. Samuelson, and S. V. Ab, "A GaAs Nanowire Array Solar Cell with 15.3 % Efficiency at 1 Sun," *IEEE J. Photovoltaics*, vol. 6, no. 1, pp. 3–5, 2015.
- [3] G. B. Stringfellow, "08 - Specific Materials," *Organomet. Vap. Ep.*, pp. 391–484, 1999.
- [4] D. A. Woolf, Z. Sobiesierski, D. I. Westwood, and R. H. Williams, "The molecular beam epitaxial growth of GaAs/GaAs(111)B: doping and growth temperature studies," 1992.
- [5] E. Yablonovitch, T. Gmitter, J. P. Harbison, and R. Bhat, "Extreme selectivity in the lift-off of epitaxial GaAs films," *Applied Physics Letters*, vol. 51, no. 26, pp. 2222–2224, 1987.
- [6] Baca and Ashby, "Fabrication of GaAs Devices," 2005.
- [7] D. H. Reep and S. K. Ghandhi, "Morphology of organometallic CVD grown GaAs epitaxial layers," *J. Cryst. Growth*, vol. 61, no. 3, pp. 449–457, 1983.
- [8] K. Kato, Y. Hasumi, A. Kozen, and J. Temmyo, "AlGaAs epitaxial growth on (111)B substrates by metalorganic vapor-phase epitaxy," *J. Appl. Phys.*, vol. 65, no. 5, pp. 1947–1951, 1989.
- [9] T. S. Moise, L. J. Guido, J. C. Beggy, T. J. Cunningham, S. Seshadri, and R. C. Barker, "Optical Properties of Strained Layer (111)B Al_{0.15}Ga_{0.85}As-In_{0.04}Ga_{0.96}As Quantum Well Heterostructures," *J. Electron. Mater.*, vol. 21, no. 1, 1992.
- [10] T. Fukui and H. Saito, "Step-flow growth and fractional-layer superlattices on (111) B GaAs vicinal surfaces," vol. 107, pp. 231–236, 1991.
- [11] H. H. Farrell, J. Lu, B. D. Schultz, a. B. Denison, and C. J. Palmstrøm, "GaAs(111)B($\sqrt{19}\times\sqrt{19}$)R23.4° surface reconstruction," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 19, no. 4, p. 1597, 2001.
- [12] K. Yang and L. J. Schowaltep, "Surface reconstruction substrates phase diagram and growth on GaAs (111) B by molecular beam epitaxy," no. 111, pp. 1851–1853, 1992.
- [13] D. a Woolf, D. I. Westwood, and R. H. Williams, "The homoepitaxial growth of GaAs(111)A and (111)B by molecular beam epitaxy: an investigation of the temperature-dependent surface reconstructions and bulk electrical conductivity transitions," *Semicond. Sci. Technol.*, vol. 8, no. 6, pp. 1075–1081, 1999.
- [14] Y. Ruixia, W. Yibin, N. Chenliang, and Y. Fan, "Surface reconstructions and reflection high-energy electron diffraction intensity oscillations during homoepitaxial growth on nonmisoriented GaAs(111)B by MBE," *J. Semicond.*, vol. 31, no. 11, p. 113001, 2010.
- [15] R. S. Wagner and W. C. Ellis, "Vapor-Liquid-Solid Mechanism of Single Crystal Growth," *Appl. Phys. Lett.*, vol. 4, no. 5, p. 89, 1964.
- [16] K. Hiruma, M. Yazawa, T. Katsuyama, K. Ogawa, K. Haraguchi, M. Koguchi, and H. Kakibayashi, "Growth and optical properties of nanometer-scale GaAs and InAs whiskers," *J. Appl. Phys.*, vol. 77, no. 2, pp. 447–462, 1995.
- [17] G. J. Bauhuis, P. Mulder, E. J. Haverkamp, J. C. C. M. Huijben, and J. J. Schermer, "26.1% thin-film GaAs solar cell using epitaxial lift-off," *Sol. Energy Mater. Sol. Cells*, vol. 93, no. 9, pp. 1488–1491, 2009.
- [18] B. M. Kayes, H. Nie, R. Twist, S. G. Spruytte, F. Reinhardt, I. C. Kizilyalli, and G. S. Higashi, "27.6% Conversion efficiency, a new record for single-junction solar cells under 1 sun illumination," *Conf. Rec. IEEE Photovolt. Spec. Conf.*, pp. 04–08, 2011.
- [19] J. J. Schermer, G. J. Bauhuis, P. Mulder, E. J. Haverkamp, J. van Deelen, a. T. J. van Niftrik, and P. K. Larsen, "Photon confinement in high-efficiency, thin-film III-V solar cells obtained by epitaxial lift-off," *Thin Solid Films*, vol. 511–512, pp. 645–653, 2006.
- [20] F. L. Wu, S. L. Ou, R. H. Horng, and Y. C. Kao, "Improvement in separation rate of epitaxial lift-off by hydrophilic solvent for GaAs solar cell applications," *Sol. Energy Mater. Sol. Cells*, vol.

- 122, pp. 233–240, 2014.
- [21] E. Yablonovitch, “Ultra-Efficient Epitaxial Lift-off Solar Cells Exploiting Optical Confinement in the Wave Limit Ultra-Efficient Epitaxial Lift-off Solar Cells Exploiting Optical Confinement in the Wave Limit,” *Sol. Cells*, no. November, 1999.
 - [22] B. M. Kayes, L. Zhang, R. Twist, I. Ding, and G. S. Higashi, “Flexible Thin-Film Tandem Solar Cells With > 30 % Efficiency,” *IEEE J. Photovoltaics*, vol. 4, no. 2, pp. 729–733, 2014.
 - [23] P. Kumar, S. Kanakaraju, and D. L. Devoe, “Sacrificial etching of Al_xGa_{1-x}As for III-V MEMS surface micromachining,” *Appl. Phys. A Mater. Sci. Process.*, vol. 88, pp. 711–714, 2007.
 - [24] D. a. Woolf, D. I. Westwood, and R. H. Williams, “Surface reconstructions of GaAs(111)A and (111)B: A static surface phase study by reflection high-energy electron diffraction,” *Appl. Phys. Lett.*, vol. 62, no. 12, pp. 1370–1372, 1993.
 - [25] J. R. Arthur, “Vapor pressures and phase equilibria in the Ga-As system,” *Solid State Commun.*, vol. 5, no. 7, p. i, 1967.
 - [26] K. M. Dzurko, S. G. Hummell, E. P. Menu, and P. D. Dapkus, “MOCVD growth of AlGaAs/GaAs structures on nonplanar {111} substrates: Evidence for lateral gas phase diffusion,” *J. Electron. Mater.*, vol. 19, no. 12, pp. 1367–1372, 1990.
 - [27] U. Pohl, *Epitaxy of Semiconductors: Introduction to Physical Principles*. 2013.
 - [28] [Http://www.nanolabtechnologies.com/d-sims-service](http://www.nanolabtechnologies.com/d-sims-service), “nanolabtechnologies.” .