Master's Thesis

Modeling and Implementation of A 6-Bit, 50MHz Pipelined ADC in CMOS

By

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Abstract

The pipelined ADC is a popular Nyquist-rate data converter due to its attractive feature of maintaining high accuracy at high conversion rate with low complexity and power consumption. The rapid growth of its application such as mobile system, digital video and high speed data acquisition is driving the pipelined ADC design towards higher speed, higher precision with lower supply voltage and power consumption. This thesis project aims at modeling and implementation of a pipelined ADC with high speed and low power consumption.

Acknowledgements

First of all, I would like to thank Almighty ALLAH for giving me the strength to complete this work. My supervisor Mr. Xiaodong Liu needs a big appreciation here because he helped me at every stage of my work. Whenever I found myself stuck in a problem he helped me and gave me some very useful suggestion which proved very helpful to me. Without his constant support and guidance this work wouldn't be completed. I would like to thank my examiner Dr. Pietro Andreani for providing me the opportunity to do a Master's Thesis in Mixed Signal group. I also want to thank Mr. Waqas Ahmed for giving me time whenever I needed his help and helped me in understanding problems I went through.

A big thanks to all my friends in Sweden for their support and love.

At the end I would like to thank my parents who supported me throughout my life and prayed for me especially my mother who called me every day just to ask how's my thesis is going.

Qazi Omar Farooq

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Table of Contents

CHAPTER 1

1 Introduction

1.1 Motivation

With the rapid increase in demand of portable handheld communication devices, high-quality video systems and high-quality data acquisition systems in which both speed and accuracy are critical, there is a need of an ADC which is high speed, highly accurate, consumes less power, occupy small area and works on lower supply voltage. Low power consumption is critical because for battery-powered portable devices there is a need to increase battery life. So, it is important that the ADC used in those applications are high speed and consumes less power. Low voltage is also a critical factor for such applications. Instead of having a separate power supply for powering up digital and analog blocks on the chip, a single voltage supply can be used which reduces the overall cost and effort. So, there is also a need of ADC which operates at low supply voltage. A high speed ADC provides a high dynamic performance i.e. SNDR, SFDR at very high sampling rates. ADCs with sampling rate or clock frequency above 10MHz are considered high speed [2].

Designing high speed ADC with low power consumption has always been challenging. With an increase in sampling rate there is also a significant increase in power consumption due to fast settling requirement of an Op-amp. Its always being a challenge for the designers to design an ADC which is high speed (clock frequency $\geq$ 10MHz) and consumes as much less power as possible. Idea in the proposed work is also to achieve as less power consumption as possible and still doing fine conversion at high sampling rate achieving a high dynamic range. Flash ADC achieves a high sampling rate but then there is a significant increase in power consumption as resolution of the converter has been increased. Flash ADC is explained more in section 1.3.1. In the past efforts have been made to design a pipeline ADC at a sampling rate of 5 Msample/sec (MS/s) but it consumed large power ranging typically above 100mW [33]. There are some design limitations that limits the overall speed of the converter and limits the clock frequency below 10MHz. The SHA and MDAC circuits needs to be accurate to give a good dynamic performance. SHA circuit must sample and hold at the correct time intervals and the output of the MDAC circuit

must settle fast. If the SHA and MDAC circuits are not accurate due to longer settling time, it will result in an increase in distortion and degrade the overall SNDR, SFDR, INL/DNL performance of the ADC. As the main building block in SHA and MDAC circuit is an operational amplifier, the long settling time of an op-amp is the reason of degraded performance that will limit the speed of the converter below 10MHz. The Op-amp must settle to within ±1/2 LSB, where 1 LSB = 15.62mV for a 6-bit ADC. The longer the settling time the lower the sampling rate. Overall speed and accuracy of ADC is determined by the settling time and accuracy of operational amplifier output. Another important circuit that determines the overall speed of the converter is the comparator. Comparator should be fast enough to work fine at a high sampling rate and output correct digital bits at correct timing. The idea is to look at the components that are limiting the overall speed of the converter below 10MHz. Components sensitive in determining speed and accuracy are operational amplifier, clock, comparators (Sub ADC), Sub DAC. These components are tested separately at a clock frequency of 50MHz.

In order to accomplish a low power consumption a front-end SHA is used which results in a significant power reduction compared to other pipelined ADCs which has a dedicated power hungry SHA in each stage except the final stage which is a 2-bit flash ADC.

In this thesis a 6-bit pipelined ADC has been designed which operates at a clock frequency of 50MHz and dissipates only 31.62mW of power. Implementation is completed in 130nm CMOS process at a supply voltage of 1.2V.

1.2 Analog to Digital Converter

As the real world is analog, an analog to digital converter (ADC) is needed for further processing of the signal in digital domain using a digital signal processor (DSP). The only way to interact the digital system with the analog system is by converting the analog signal into digital using an ADC. Why the processing must be done in digital domain? Because the digital circuits are less susceptible to noise, consume less power. After the necessary operations performed on the signal in the DSP block the signal is reproduced into analog by digital to analog converter so the signal is ready again for the analog world.

An ADC samples and quantizes the analog signal and output the digital code which is basically the representation of an analog signal in digital form.

1.3 Comparison of Different ADCs

Different ADC architectures can be used depending on the required accuracy, speed and power consumption [2]. There is always a tradeoff in the design of an ADC. According to table 1.1 it can be seen for example in case of flash ADC speed is high which is good but then the accuracy is low and it takes more area. So there is a tradeoff in speed, accuracy and area. Also it consumes more power.

Table 1. 1: Comparison of different ADCs [2]

Architecture	Latency	Speed	Accuracy	Area
Flash	No	High	Low	High
SAR	No	Low-Medium	Medium-High	Low
Folding + Interpolating	No	Medium-High	Medium	High
Delta-Sigma	Yes	Low	High	Medium
Pipeline	Yes	Medium-High	Medium-High	Medium

1.3.1 Flash ADC

It is called a flash ADC because all the comparators work in parallel. Flash ADC is one of the fastest ADC among all the ADC architectures. The whole conversion can take place in just one clock period. So for high speed conversion while the resolution is low flash ADC is used. The problem with a flash ADC is that it is not suitable for high resolution because as the resolution increases the number of comparators increases therefore the power consumption increases. The number of comparators used in a flash ADC depends on the number of bits needed at the output.

$$\text{Number of Comparators} = 2^n - 1 \qquad (1.1)$$

Where n is the number of bits.

So there is a tradeoff between speed and power. Flash ADC converts an analog input into digital output by comparing the analog input with a fixed

reference voltage created by the resistive ladder. The output of a flash ADC is thermometer code. A thermometer to binary decoder forms the required binary representation of the analog input. Figure 1.1 shows the block diagram of a flash ADC.

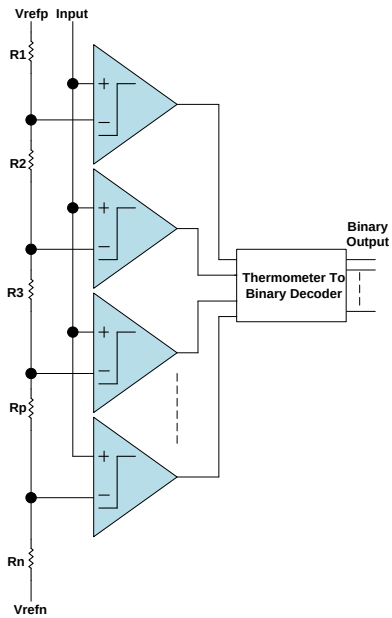

Figure 1.1 Flash ADC

1.3.2 Successive Approximation Register (SAR) ADC

SAR ADC operation is based on a binary search algorithm [3].

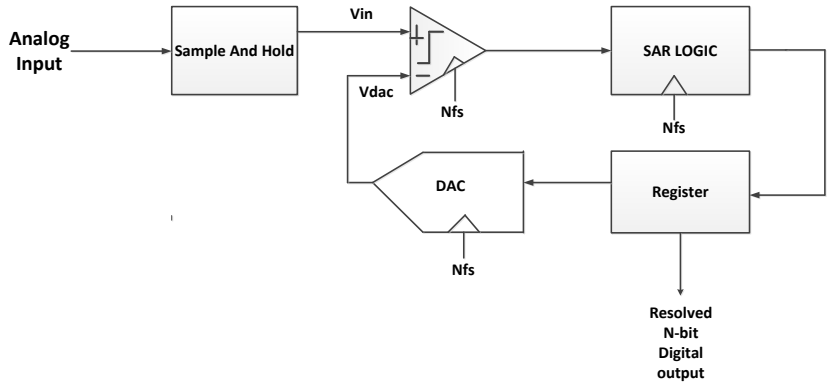

Figure 1.2 SAR ADC

Figure 1.2 shows the block diagram of SAR ADC. It is a medium to high resolution ADC. SAR ADCs are used for sampling rate of up to 5Mbps with resolutions from 8 to 18 bits [8]. An analog input is first processed by the sample and hold circuit. The held input signal is then compared with the output of a DAC using a comparator. The binary search algorithm is then implemented by first setting the register to midscale. As full scale is from 0 - $V_{REF}$where $V_{REF}$is the ADC reference voltage. Therefore, after this the DAC output will become$\frac{V_{REF}}{2}$. Now this voltage from the DAC is then compared with the held input signal. If analog input is greater than the voltage from the DAC, the comparator output's logic high and the MSB of the Register is set to 1. On the other hand, if the analog input is less than the DAC voltage well in that case the comparator output's zero and MSB of the register is set to zero. Now the operation continues until the final LSB is available.
The SAR logic basically moves to the next down bit, make it high, and another comparison is performed. At the end N-bit digital output is available in the register.

1.3.3 Delta Sigma ADC

A delta-sigma ADC is an oversampling ADC [3].

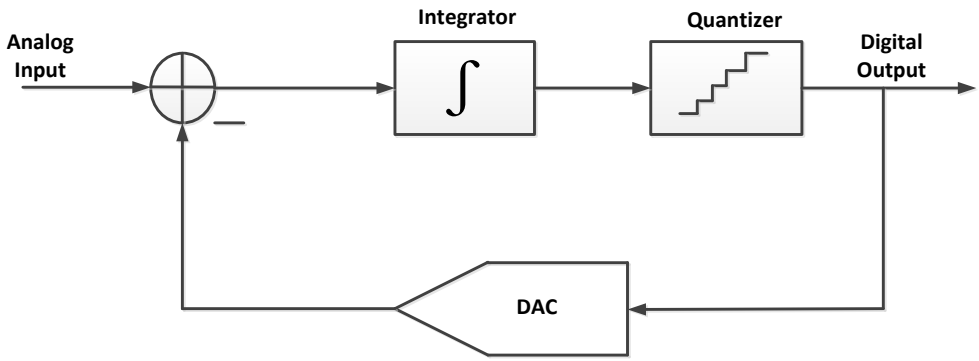

Figure 1.3 Delta Sigma ADC

Figure 1.3 shows the block diagram of a delta-sigma ADC. A delta-sigma ADC is good choice for low speed and highly accurate analog to digital conversion. Delta-sigma ADC spectrally separates the quantization noise from the signal which is added by the quantizer. A technique called noise shaping is used here by using a feedback DAC and integrator [3]. In a delta-sigma ADC the output from the DAC is subtracted from the analog input using a differentiator while the difference is applied to the integrator. The integrator output is quantized using an n-bit ADC.

1.4 Pipelined ADC

Pipelined ADC is a Nyquist –rate analog to digital converter [3]. It is a good choice among other analog to digital converter architectures for sampling rate from few mega samples per second to higher sampling rates. Resolution for such converters ranges from 8 to 16 bits. Pipelined ADC is one of the most efficient ADC used in today's consumer electronics. Pipelined ADCs are used in a variety of applications such as: mobile systems, CCD imaging, ultrasonic medical imaging, digital receivers, base stations, digital video (e.g. HDTV), Xdsl, cable modems, and fast Ethernet [1]. In a pipelined ADC different stages are cascaded and the number of stages to be cascaded depends on the number of bits needed at the output.
The accuracy requirement for a pipeline ADC decreases from first stage to the last stage. The first stage must be more accurate than the later stages. The best thing about a pipeline ADC is that it can provide high throughput rates and occupy small die area. It has a high throughput because of the

concurrent operation of the stages i.e. At any given time, the first stage operates on the most recent sample while all other stages operate on residues from previous samples. To tolerant the non-idealities such as comparator offset, some redundancy is introduced in each stage. That's why 1.5-bit stage is extensively used. A digital correction algorithm later eliminates the redundancy.

1.5 Pipelined ADC Design and Requirements

System design and transistor level design has been done using Cadence Spectre circuit simulator because it provides fast, high precision simulations for mixed-signal circuits and waveforms have been viewed using waveform viewer. System design has been completed using Verilog-A and transistor level design has been done and tested using Cadence Virtuoso Schematic Editing. Further post processing for FFT and INL/DNL has been done on MATLAB. All the figures are drawn in Microsoft Visio and the simulation results are plotted in MATLAB by exporting waveform data. In order to define the performance of an ADC, performance parameters play a very vital role and it is really important to ensure that the ADC is working well by measuring its static and dynamic parameters. Static parameters are ADCs INL/DNL and they should be within ±0.5LSB for an ADC to be linear and having no missing codes. Dynamic parameters tell how well the ADC will behave for real sinusoidal signals at a particular input frequency by measuring distortion contributions below the input signal. It is important to ensure that the highest distortion below the input signal is low enough for the conversion to be implemented linearly. So, high SFDR and SNDR is desired for an ADC to perform well. For a 6-bit performance SNDR should be close to 38dB and SFDR should be above 40dB.

1.6 Specifications

Table 1.2: Pipeline ADC Specifications

Specification	Value	Units
V_{inp}	350 to 850	mV
V_{inn}	850 to 350	mV
Differential Input	-500 to 500	mV
V_{refp}	662.5	mV
V_{refn}	537.5	mV
Resolution	6	bits
Sample Rate	50	MHz
Power Supply	1.2	V
V_{cm} (Op-amp)	600	mV
Power Consumption	31.62	mW
Current Consumption	26.33	mA
f_{in}	0.317, 13.01	MHz

1.7 Design Methodology

The idea is to break down the design into small blocks, test them independently, make sure that they are working well and then put them together to build the complete ADC. Most critical is the operational amplifier used in SHA and MDAC, because most errors in a pipelined ADC are due to slow settling and finite gain of an Op-amp. First a non-overlapping clock generator circuit has been designed and tested to generate four non-overlapping clocks for the ADC. Next is to design an Op-amp and testing it using Cadence Spectre simulator to make sure that the designed Op-amp is fast enough to be plugged into the ADC and all the specifications has been met. After Op-amp, comparator has been designed and tested for 50MHz clock. Next is to design MDAC, SHA and sub-ADC blocks. After designing all the blocks individually, 1.5-bit stage has been built by putting all the individual blocks together to make sure it is working fine for 1.5-bits stage. After successful testing of 1.5-bit stage next step is to design and build a shift register, digital correction logic and the last stage. A 6-bit pipelined converter has been built by cascading four 1.5-bit stages followed by a last stage, shift register, digital correction logic blocks and an SHA at the front end. Next step is to test the 6-bit ADC by adding a

6-bit DAC after the ADC. Two different type of tests has been performed to measure the performance of the converter. First a linearity test has been performed by applying a ramp input and static performance is measured by exporting output data samples to MATLAB and measuring INL/DNL. In the second test ADC has been tested for real signals by applying a sinusoidal input and FFT spectrum has been plotted to measure SNDR, SFDR of the converter.

1.8 Related Work

Xi.Long designed a 9 stage 10-bit, 40MHz pipelined ADC in AMIS C5N process. The design of this 6-bit 50MHz pipelined ADC is based on his work [31]. Idea is to implement the design in 130nm CMOS process at 1.2V power supply. 6-bit resolution was the minimum requirement for this work which is accomplished at 50MHz clock frequency.
For the past few decades a lot of work have been done in the field of ADCs due to an increasing demand of communication electronics [2] [7] [21] [23] [31] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46]. High speed ADCs required for applications like portable handheld devices, high-quality video systems and high-quality data acquisition systems with a sampling rate above 5Msample/sec have consumed a large amount of power typically above 100mW [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46]. In the work done by Xi.Long the idea was to sample at high clock rate. Although the design was simulated and tested both for 5 stages which is a 6-bit pipelined ADC and 9 stages which is a 10-bit pipelined ADC, it is concluded that the design did not work well for the sampling frequency above 40MHz and its performance starts degrading for sampling rate greater than 40MHz because the designed Op-amp is not fast enough to settle to its final value in the required time frame which is making the sub ADC in the subsequent stages to take wrong decisions giving error bits at the output. Those error bits will introduce high harmonic distortion and spurs that will degrade the overall SNDR, SFDR of the converter where as in the proposed work designed ADC is giving optimal results for a 6-bit performance at 50MHz sampling frequency which is higher than the maximum sampling rate achieved in Xi.Long work. Also the designed ADC which is implemented in a totally different process consumes much less power as it operates at 1.2V (600mV common mode) power supply as compared to a 5V (2.5V common mode) power supply used in his work. Of course Xi.Long design achieves a resolution of both 6-bit and 10-bit and the

proposed work is limited to a 6-bit performance but that's in the future work of this design to extend the number of resolved bits to at least 10-bit at 50MHz sampling rate with low power dissipation.

1.9 Thesis Organization

The remaining chapters in this thesis are designed as follows.

Chapter 2 discusses the modeling of pipelined ADC. Different blocks used in a 1.5-bit stage have been discussed in detail.

Chapter 3 discusses the implementation of the pipelined ADC.

Chapter 4 discusses the simulation results.

Chapter 5 and 6 discuss the conclusions and future work.

CHAPTER 2

2 Modeling of Pipelined ADC

In this chapter blocks used in building this pipelined ADC are discussed. As mentioned in last chapter, since each stage is 1.5 bit except the last stage. Each 1.5-bit stage consists of an SHA, a sub ADC, sub DAC, MDAC and the last stage is a 2-bit flash ADC. The final digital output is generated by the digital correction logic.

2.1 Architecture

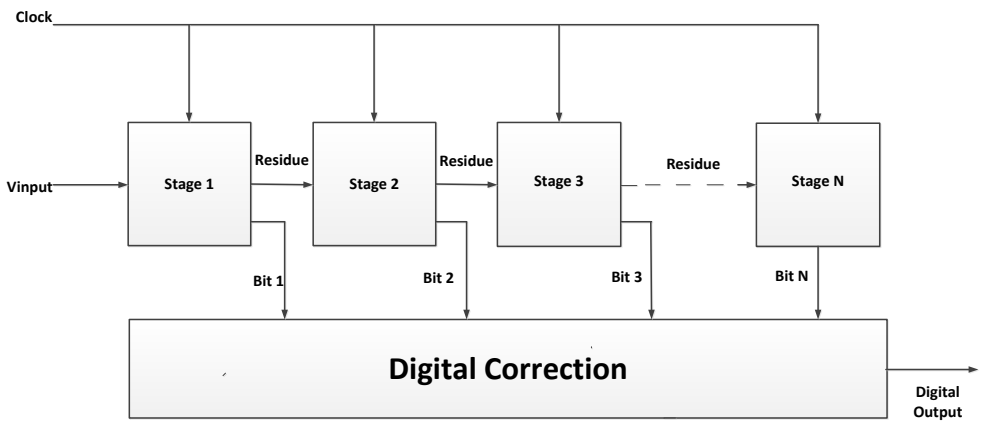

Figure 2.1 Pipeline ADC architecture

Figure 2.1 shows the architecture of an n-bit pipelined ADC with different stages cascaded to obtain the final digital output. Each stage is of 1.5-bit except that the final stage is a 2-bit flash ADC. The digital output from each stage is stored in a shift register until the final digital output is available from the last stage. The stored data in the shift register is then processed by digital correction logic.

2.2 1.5-bit Pipeline stage

Figure 2.2 shows the 1.5-bit pipeline stage. Each 1.5-bit stage has a sample and hold amplifier (SHA), a low resolution analog to digital converter (sub-ADC), a low resolution digital to analog converter (sub-DAC), a subtractor and an amplifier. The sub-DAC, subtractor and the amplifier are implemented in a single switched capacitor circuit called MDAC.
The input held by the SHA is converted into a low resolution digital output by the ADC. This digital output is stored into the shift register. The low resolution digital output is then converted back into analog by the sub DAC where it gets subtracted from the held input. The residue is amplified by 2 and sent off to the next stage for further digitization.

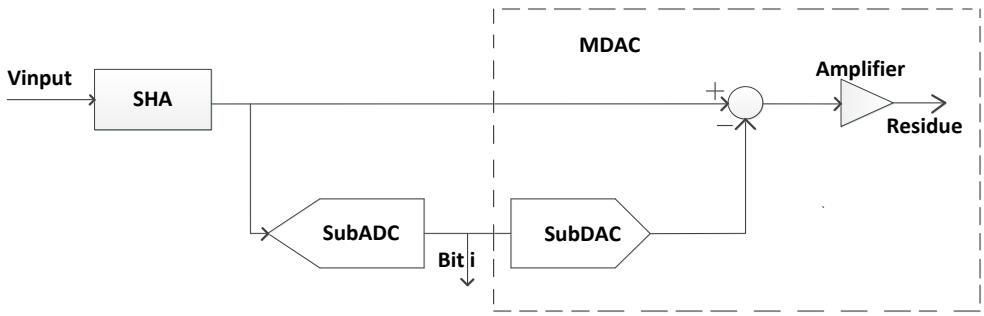

Figure 2.2 1.5-bit Pipeline Stage

2.2.1 Sample And Hold Amplifier

SHA plays an important role typically in all ADC's, switched capacitor filters. In a pipelined ADC an SHA must be used at the front end in order to improve its dynamic and static performance especially for a high frequency input signal. Also it helps in achieving high speed and better accuracy with a low power consumption. It is needed in a pipelined ADC because the input signal must be held until other operations like the analog to digital conversion and the digital to analog conversion are completed. So it plays a crucial role. There are errors in a SHA like clock feed–through, charge injection, sampling clock jitter. Various techniques have been implemented to get rid of these errors [28]. While designing an SHA different parameters must be studied [1].
An SHA acquires an analog input signal and hold it for some period of time. SHA used in this thesis is a fully differential conventional flip around

front end sample and hold [29]. It consists of an operational amplifier, a switch and a capacitor for sampling and holding.
Figure 2.3 shows the schematic of the fully differential SHA used in the pipelined converter. A fully differential structure is used as it will cancel the common mode noise and reduce the sampling offset error.

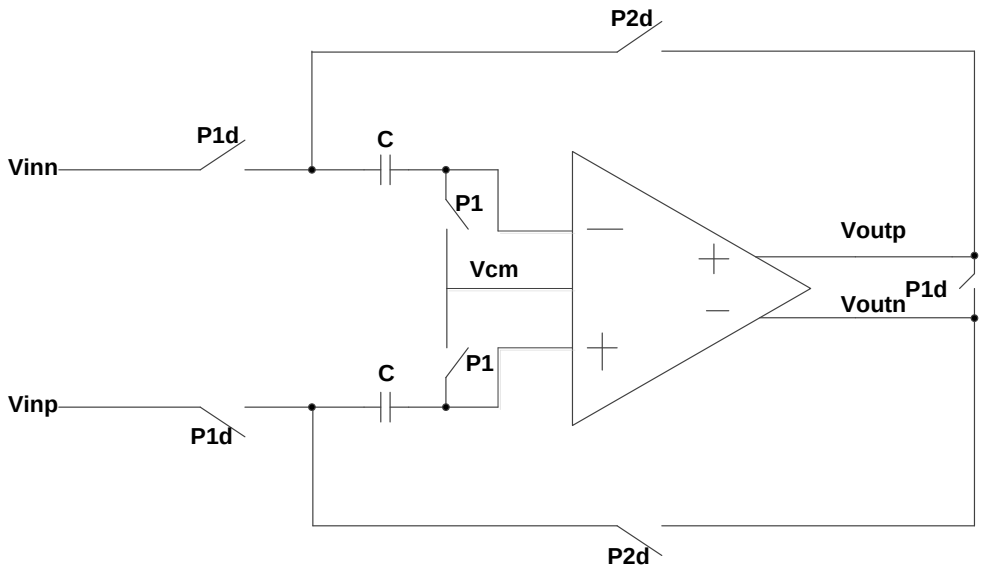

Figure 2.3 SHA schematic

This SHA is working on two non-overlapping clock phases P1d and P2d while P1 is the early falling edge of P1d used for bottom plate sampling. Figure 2.4 shows the clock waveforms.

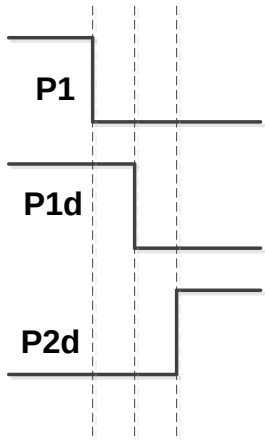

Figure 2.4 Clock Waveforms

During the sample phase input is acquired on the input capacitor and during the hold phase the same capacitor is flipped to the output. Operational amplifier outputs are at common mode level (600mV) during the sampling phase. At the input the operational amplifier will serve as a high impedance output buffer which won't let the charge stored on the capacitor during the sampling phase due to the high input impedance of an amplifier. During the hold phase (amplification phase) when P2d goes high, operational amplifier is connected in a closed loop configuration, due to the conservation of charge the charge stored on the capacitor during the sampling phase will now appear at the output during the hold phase. So the operational amplifier role came into play during the hold phase. It must have a high bandwidth, a high phase margin, good swing, high slew rate so the output must be settled to the sampled input voltage i.e. within half of the clock cycle. There is a noise generated in a SHA given by the capacitors in the sampling and amplification phase called $\frac{KT}{C}$ noise. This noise degrades the SNR of the converter. Capacitor value should be properly sized so that it won't degrade the SNR that much.

2.2.2 Sub ADC

Each pipeline stage has a flash sub ADC block for the coarse quantization of analog input to produce the digital output. Two comparators do the job of quantizing the analog input signal.

The differential input voltage to the sub ADC is (-500mV to 500mV) differentially. There should be two thresholds defined at $\frac{-V_{ref}}{4}$ and $\frac{+V_{ref}}{4}$. Comparators compares the analog input to the thresholds. The maximum number of possible binary combinations we can get from two comparators is 4.

Table 2.1: Binary Representation

D_1	D_0
0	0
0	1
1	0
1	1

Since for a 1.5-bit ADC, the maximum regions of operations are three (00,01,10), so the 11 combination must be discarded. The digital output from the sub ADC is 00, 01 or 10 depending on where the input falls. 1.5-bit/stage architecture is the most popular choice in pipelined ADC because it helps in minimizing the nonlinearity by adding redundancy in sub ADC block. In a sub ADC block the extra 0.5 bit is a redundant bit which is corrected in digital correction logic. It is only utilized for the offset relaxation in an ADC. A comparator offset as large as $\pm\frac{V_{ref}}{4}$ can be tolerated in this case.

Three regions of operations are defined as 00,01or 10 with two thresholds at $\pm\frac{V_{ref}}{4}$. So if $V_{in} < \frac{-V_{ref}}{4}$, the digital output is 00, if $\frac{-V_{ref}}{4} < V_{in} < \frac{V_{ref}}{4}$ the digital output is 01 and if $V_{in} > \frac{+V_{ref}}{4}$ the digital output is 10. Say the comparator offset is 120mV and the range of 01 region is -125mV to 125mV, so offset falls in this range. There is no need of any offset cancellation technique in a 1.5-bit/stage architecture.

Figure 2.5 shows the schematic of a 1.5-bit flash ADC used in a pipelined stage. Comparators used are fully differential whose functionality was described in detailed in chapter 3. It uses an XOR gate in order to get rid of 11, as we need only three combinations (00, 01, 10). The digital output (D1, D0) is fed to the shift register where it is stored. It is also fed to the sub DAC for further processing.

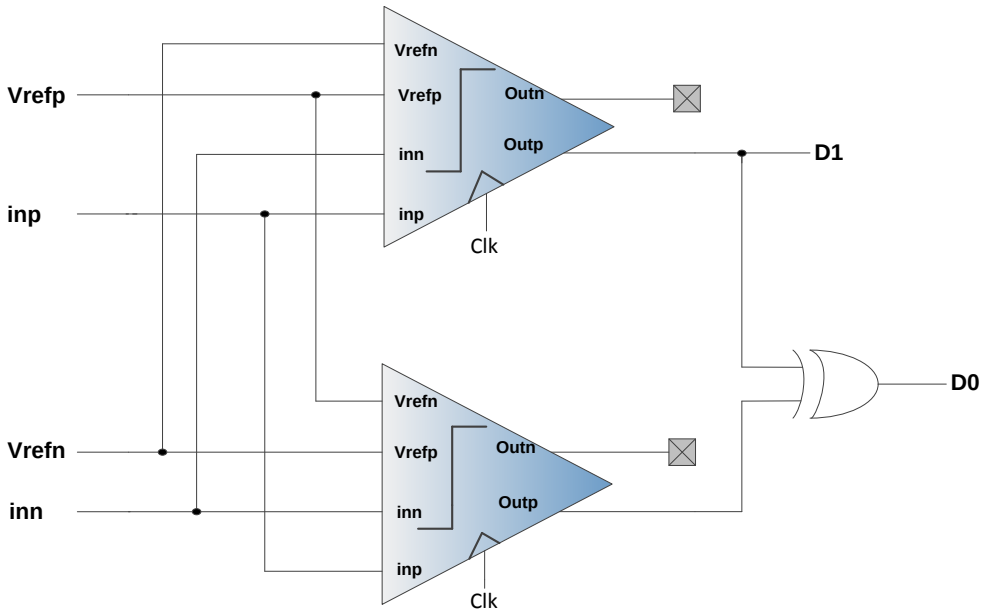

Figure 2.5 1.5-bit Sub ADC Schematic

2.2.3 MDAC

MDAC performs the sampling, amplification by 2 and subtract operation. MDAC used in this thesis is a flip around fully differential switched capacitor MDAC. Analog outputs from the sub DAC are ($\frac{-V_{ref}}{2}$, 0, $\frac{+V_{ref}}{2}$). The sub DAC output is then subtracted from the input signal. In this design the sub DAC output is multiplied by 2 before the subtraction with the input signal. So the analog output of the sub DAC is ($-V_{ref}$, 0,$+V_{ref}$).

There are certain errors in the MDAC block like gain error due to capacitor mismatch, DC gain and bandwidth of operational amplifier. This will result in integral nonlinearity and differential nonlinearity (INL/DNL) errors. Various techniques have been implemented to reduce this mismatch induced gain errors [30]. The flip around fully differential switched capacitor MDAC used in this thesis is shown in figure 2.6. The operational amplifier used in MDAC must have wide bandwidth and must be settled fast in order to improve the overall performance of the converter.

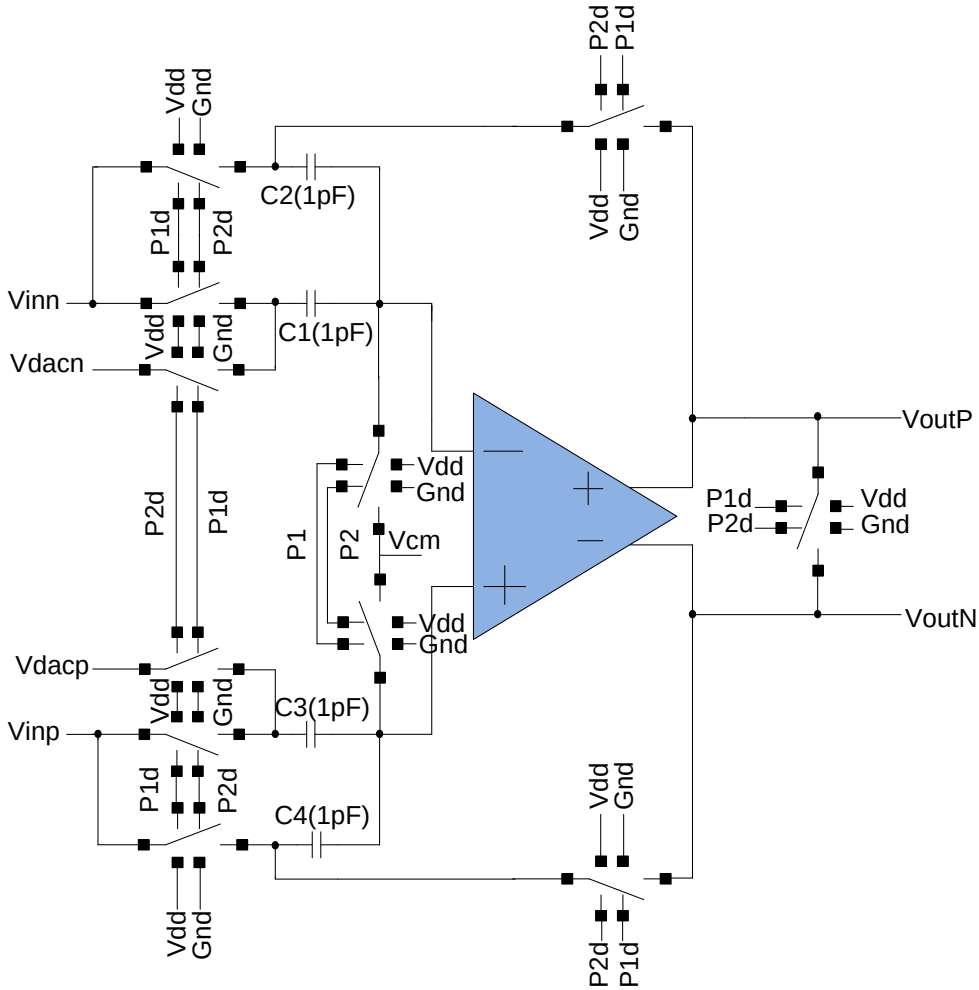

Figure 2.6 1.5-bit MDAC Schematic

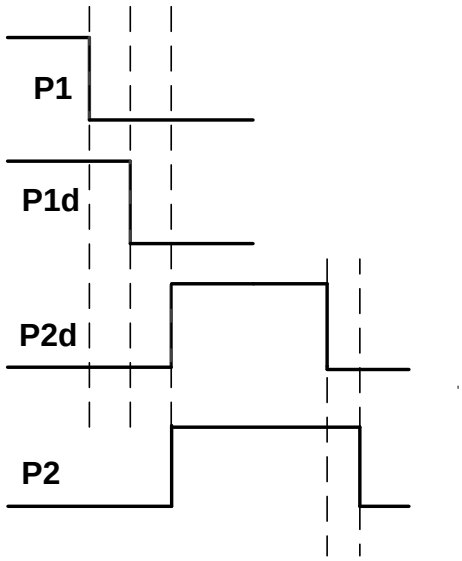

Figure 2.7 Non-Overlapping Clocks

Figure 2.7 shows the two non-overlapping clocks. P1d and P2d are the non-overlapping clocks for sampling and amplification. P1 and P2 are used for bottom plate sampling.

In figure 2.6 during the sampling phase (P1d) analog inputs are acquired by all four capacitors (C1, C2, C3, C4). Charge stored on the capacitors is CV. Here only single end is considered. The calculations are the same for the other end as it is fully differential. If the analog input to the MDAC block is between $\frac{-V_{ref}}{4}$ and $\frac{V_{ref}}{4}$ and the sub ADC output is 01, so the charge stored on the capacitors is

$$Q_{C1} = C_1 V_{inn} \quad (2.1)$$

$$Q_{C2} = C_2 V_{inn} \quad (2.2)$$

During the amplification phase (P2d), C2 is connected to the output of the operational amplifier, while C1 is connected to the DAC output (V_{dacn}). So the charge on C1 changes. Now the charge stored on C1 and C2 is transferred to the output during this phase according to the conservation of charge.

$$C_1 V_{inn} + C_2 V_{inn} = C_2 V_{outp} \quad (2.3)$$

$$V_{outp} = \left(1 + \frac{C_1}{C_2}\right) V_{inn} \quad (2.4)$$

If, $C_1 = C_2$, then

$$V_{outp} = 2V_{inn} \quad (2.5)$$

If the stage analog input to the MDAC block is below $\frac{-V_{ref}}{4}$ and the sub ADC output is 00, then

During the sampling phase (P1d)

$$Q_{C1} = C_1 V_{inn} \quad (2.6)$$

$$Q_{C2} = C_2 V_{inn} \quad (2.7)$$

During the amplification phase (P2d)

$$C_1 V_{inn} + C_2 V_{inn} = C_1(-V_{dacn}) + C_2 V_{outp} \quad (2.8)$$

$$V_{outp} = (1 + \frac{C_1}{C_2})V_{inn} + \frac{C_1}{C_2} V_{dacn} \quad (2.9)$$

If, $C_1 = C_2$, then

$$V_{outp} = 2V_{inn} + V_{dacn} \quad (2.10)$$

$$V_{outp} = 2(V_{inn} + \frac{V_{dacn}}{2}) \quad (2.11)$$

If the stage analog input to the MDAC block is above $\frac{V_{ref}}{4}$ and the sub ADC output is 10, then

During the sampling phase (P1d)

$$Q_{C1} = C_1 V_{inn} \quad (2.12)$$

$$Q_{C2} = C_2 V_{inn} \quad (2.13)$$

During the amplification phase (P2d)

$$C_1 V_{inn} + C_2 V_{inn} = C_1(V_{dacn}) + C_2 V_{outp} \quad (2.14)$$

$$V_{outp} = (1 + \frac{C_1}{C_2})V_{inn} - \frac{C_1}{C_2} V_{dacn} \quad (2.15)$$

If, $C_1 = C_2$, then

$$V_{outp} = 2V_{inn} - V_{dacn} \quad (2.16)$$

$$V_{outp} = 2(V_{inn} - \frac{V_{dacn}}{2}) \quad (2.17)$$

Equations (2.5), (2.11) and (2.17) represents the residues which are generated at the output of a pipeline stage and are fed into the next stage for further quantization providing 1.5-bits/stage until it reaches the last stage formed of a 2-bit flash ADC. Figure 2.8 explains the residue transfer curve at the output of a 1.5-bit MDAC.

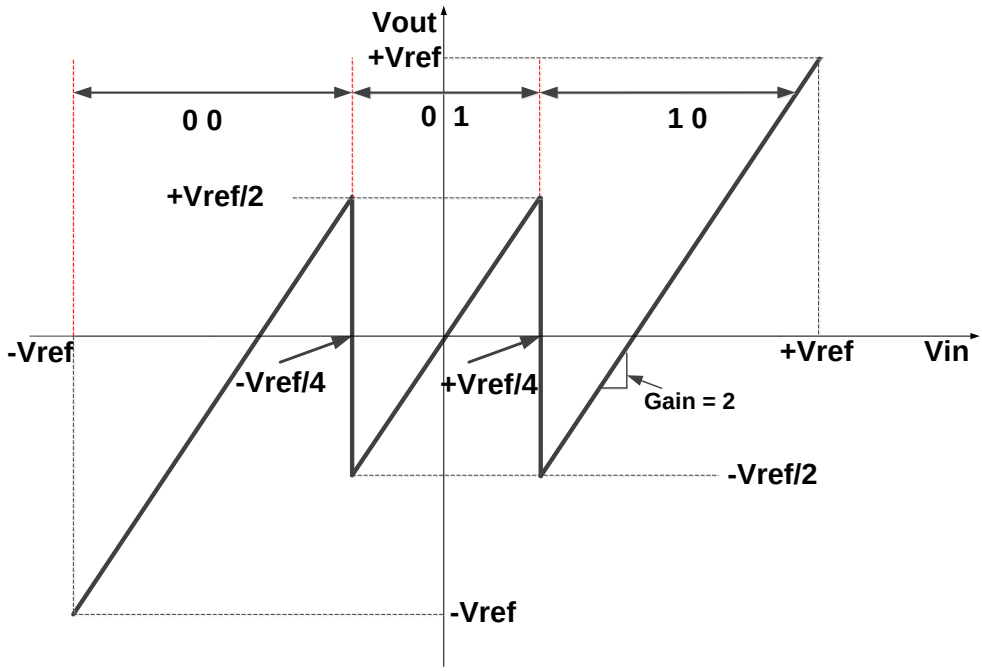

Figure 2.8 Transfer Curve of 1.5-bit MDAC

According to figure 2.8, $\frac{V_{ref}}{2}$ is added to the input when the output of sub ADC is 00 and $\frac{V_{ref}}{2}$ is subtracted from the input when the sub ADC output is 10. In the 01 region which is the uncertain region the output is just the amplification by 2 of the input.

2.2.4 Last Stage

The last stage in a pipelined ADC is simply a 2-bit flash ADC. With three comparators the 2-bit flash ADC has thresholds defined at ($\frac{-V_{ref}}{2}$, 0 , $\frac{V_{ref}}{2}$). It will give a full two-bit digital signal (00,01,10,11). The digital output of the last stage doesn't need to be corrected by the digital correction logic. The digital output of the last stage represents the last 2 LSB bits of the converter. Figure 2.9 explains the transfer curve of the 2-bit flash ADC and figure 2.10 describes the 2-bit flash ADC schematic used in this thesis.

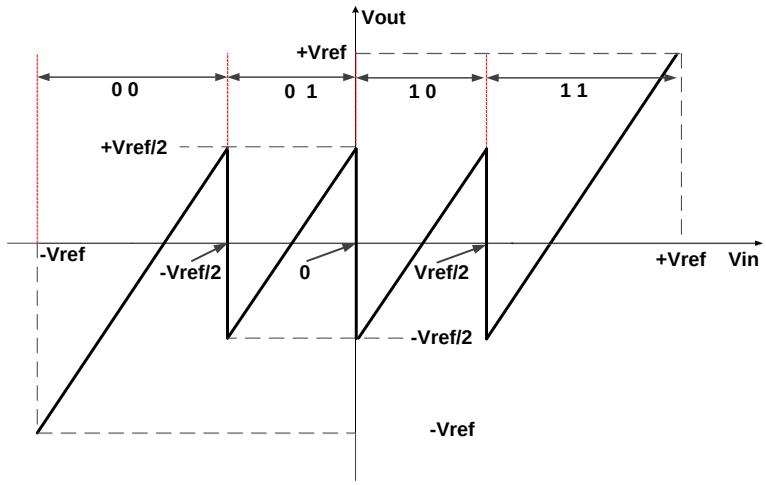

Figure 2.9 Flash ADC transfer curve with defined threshold levels

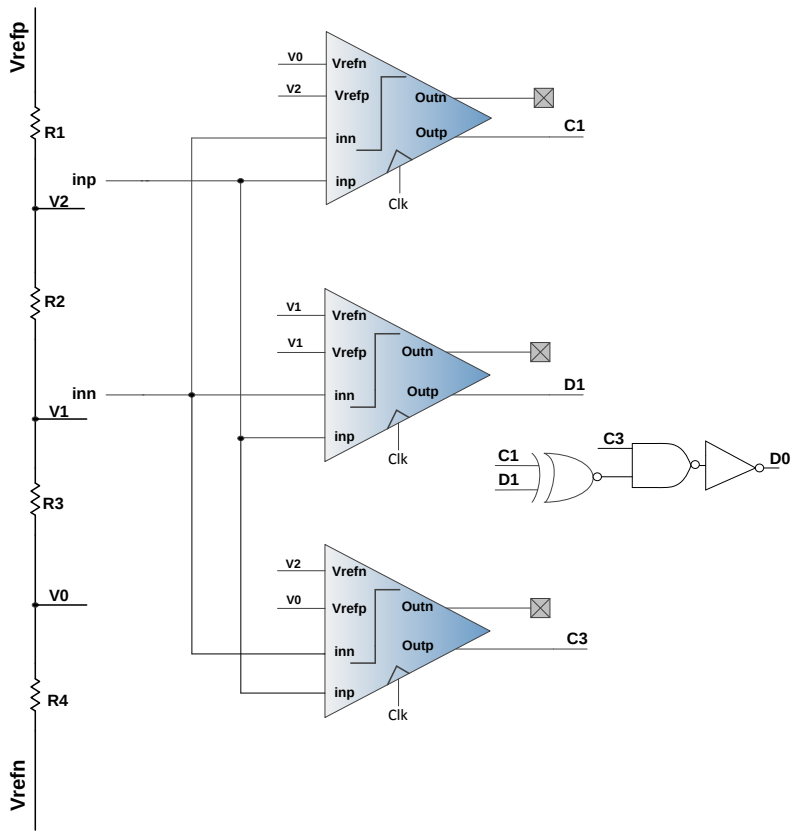

Figure 2.10 2-bit Flash ADC schematic

2.2.5 Shift Register

Shift register is a sequential logic circuit used for storing digital information. A shift register plays a very important role in the working of a pipelined ADC. Since each pipeline stage is 1.5-bit. The intermediate bits resolved during each stage are stored in a shift register until the last stage resolves the final 2-bits. A shift register produces a delay of the digital data. Since in a pipelined ADC first the digital data is available for the first stage and with many clock cycles delay it is available for the last stage. As a result of adding a delay using shift register the digital bits coming out of the last stage can be matched to those available for the first stage. So by doing this the digital data is synchronized and is available at the same time for all the stages so it would be ready to feed into the digital correction block. The delay is 'n' clock phases, where 'n' is the number of shift register stages, so the delay is determined by the shift register stages. Figure 2.11 describes the shift register schematic for a 6-bit pipelined ADC with 5 stages. It carries D-flip flops together with a transparent latch connected in a chain, the output of the transparent latch is connected to the input of the flip flop. Each of the flip flops and the transparent latch is 2-bit. It takes 2-bit digital input and gives a 2-bit digital output. Outputs from the stages are available at P1.

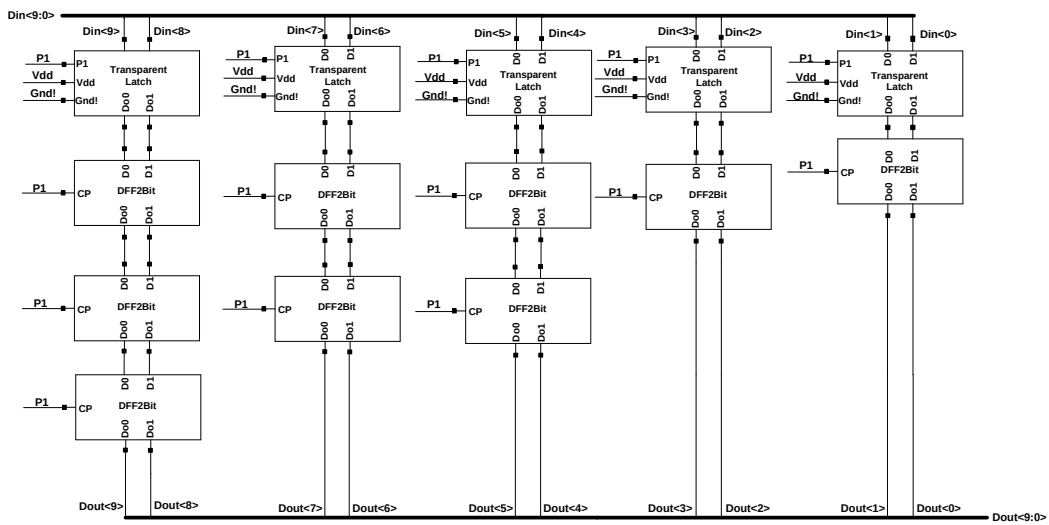

Figure 2.11 Shift Register

2.2.6 Digital Correction

As in the sub ADC digital redundancy was added for comparator offset relaxation as a result of which the residue would be within the desired range ($\pm V_{ref}$) for the next stage. Besides this the digital output from the sub ADC must be corrected before getting the final digital output of the system and this error would be corrected by digital correction logic. The digital outputs of the intermediate stages are stored in a shift register until the final stage has its output available. The stored digital data is then added using full adders in a digital correction block to produce the final output. Digital correction doesn't apply to the last stage which is a 2-bit flash ADC since there is no stage after this to correct the error. So by using digital correction, if the thresholds in the sub ADC deviates from there designed values, the final digital output would remain the same. How this correction will take place can be explained from figure 2.12. The concept is adapted from [3].

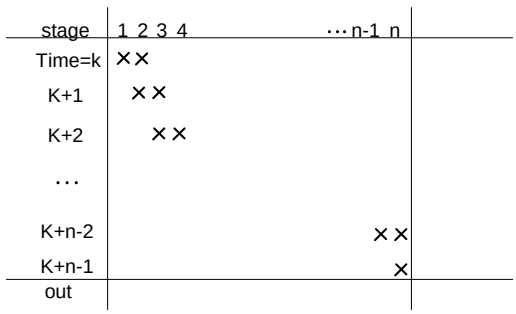

Figure 2.12 Digital combination of the bits for 1.5-bit/stage [3]

The (k+n-1)th stage output is added to (k+n-2)th stage output and the carry will propagate in the direction of MSB. Figure 2.13 shows the schematic of a digital correction block.

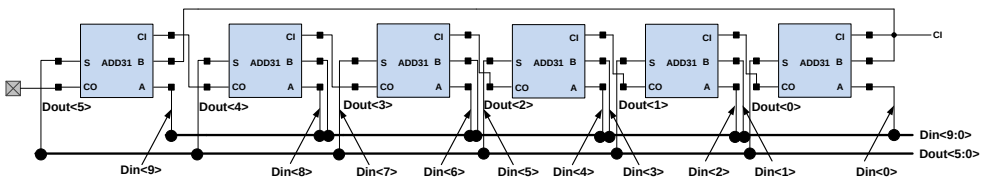

Figure 2.13 Full Adder

CHAPTER 3

3 Implementation of Pipelined ADC

3.1 Bottom Plate Sampling

A simple sample and hold arrangement is formed by a switch and a capacitor. During the sampling phase, clock is high, switch is on and the input signal is sampled on to the capacitor. The charge stored on the capacitor is

$$Q = C_s V_{in} \qquad (3.1)$$

During the hold phase the switch is off, and the capacitor holds the input signal stored on it during the sampling phase. Figure 3.1 shows the circuit of a simple sample and hold arrangement.

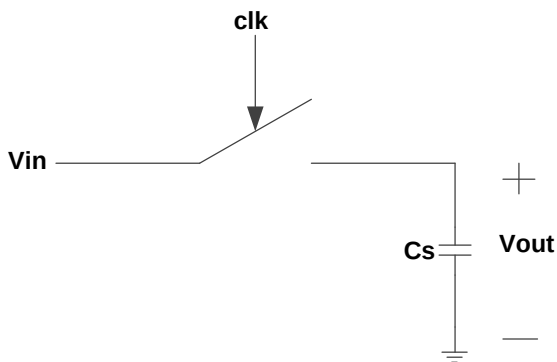

Figure 3.1 Sample and Hold Circuit

Practically, a MOS transistor is used to implement the switch. Either a PMOS or NMOS can be used or if greater voltage swings are needed in a sampling circuit then CMOS switch can be used like a transmission gate.
When a MOS transistor operates as a switch, it is operating in the triode region, so a conducing channel exists between its source and drain terminal. In a triode region the MOS on resistance is

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})} \quad (3.2)$$

Now while choosing the value of the on resistance it must be ensured that the value of the RC network time constant must be smaller than the time allowed to charge the sampling capacitor [3]. In a real switch using a MOS, when the switch goes off there might be errors due to charge injection and clock feed-through. Clock feed-through is usually due to the coupling of the gate voltage (clock) on the output voltage via parasitic capacitance C_{gs}orC_{gd}. It doesn't affect the performance of the circuit as it is signal independent and can be eliminated using differential configuration which will cancel the common mode error signals. Charge injection is another error that arises in a sample and hold circuit when the switch goes off. One way to get rid of this error is by using a dummy transistor in series with a switch [1]. When the switch is on there is some channel charge. When the switch is turned off there should be drainage of the channel charge. Some fraction of the channel charge gets dumped on the hold capacitor. This charge injection problem results in distortion. What is required is to make the channel charge independent of the input and some fraction of the channel charge is dumped on to the hold capacitor.

To eliminate the charge injection problem, a technique called bottom plate sampling can be used. Figure 3.2 shows the bottom plate sampling configuration. In a bottom plate sampling the bottom plate of the sampling capacitor is connected to another switch with an early falling edge. When both the clocks (clk1, clk2) are high the input is sampled onto the sampling capacitor. Now first when clk2 goes low M2 off, some of the fraction of the channel charge got dumped on to the capacitor but the potential at both the ends is same (ground) so the charge injection is signal independent. The bottom plate of the capacitor is floating. When M1 is turned off all the charge will go to the input. Now the charge on the capacitor is comprised of input, a fraction of channel charge from M2 and noise.

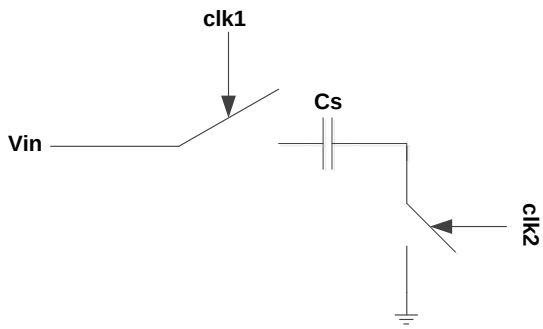

Figure 3.2 Bottom Plate Sampling

3.2 Two Stage Fully Differential Operational Amplifier

In this thesis a fully differential two stage amplifier has been used in MDAC and SHA circuits. There are different operational amplifier topologies i.e. telescopic, folded cascode and two stage etc. [4]. The two stage topology is chosen as it provides a good voltage gain, output swing, common-mode range and can be compensated with a single capacitor.
In designing a fully differential amplifier the most critical part is the common mode feedback circuit which will be explained later in this chapter. Fully differential amplifier is a good choice as it will cancel the common mode noise which helps in improving the signal to noise ratio (SNR) and gives high output swing [4]. Fig 3.3 shows a symbol for a fully differential amplifier with differential inputs (Vin_n, Vin_p) and differential outputs ($Vout_p$, $Vout_n$).

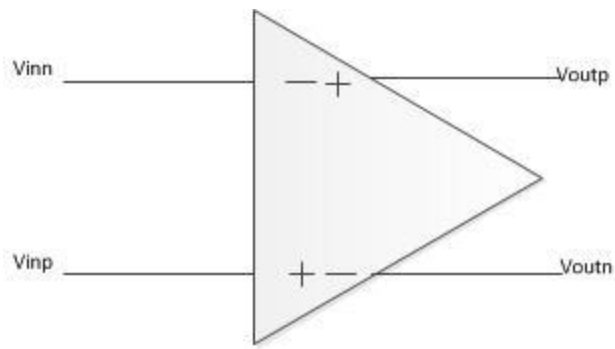

Figure 3.3 Fully Differential op-amp

3.2.1 Overview

It is called two stage amplifier because it has two stages wherein the first stage is a differential input stage providing high gain and the second stage is a common source stage with an active load providing high swing and an output stage usually added for driving heavy loads off-chip as shown in figure 3.4[5]. It has a moderate gain, large output swing and also consumes less power.

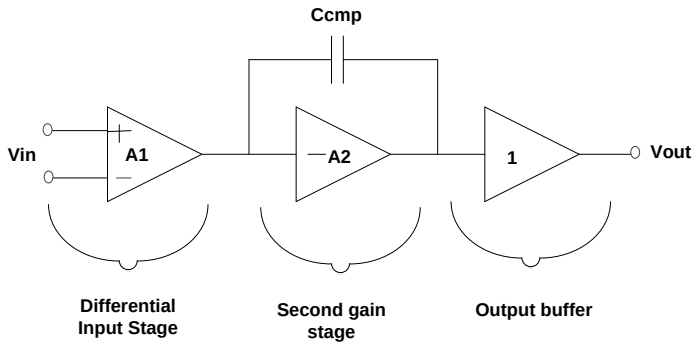

Figure 3.4 A block diagram of a two stage operational amplifier [8]

3.2.2 Architecture

Figure 3.5 shows the architecture of two stage fully differential op-amp used in this thesis. The first stage is a differential amplifier with PMOS differential pair (M1, M2) which drives an n-channel active load (M3, M4). PMOS transistors are chosen because they have lower 1/f noise than NMOS. The first stage is followed by a second gain stage which is an n-channel common source amplifier (M7, M9) with PMOS current source load (M6, M8). NMOS transistors because of their high trans-conductance give a high bandwidth. Minimum gate length is used for both input devices (M1, M2) and output gain devices (M7, M9). These devices should all have high gm and low input capacitance so minimum gate length is absolutely critical to speed up the amplifier. M5 is the p-channel tail current source for the input stage. The current in M8 and M6 is mirrored by the current source M10. M1a and M2a are for common mode latch up [9]. They help in setting the common mode level initially. M1a and M2a are biased in such a way that most of the time they are off. They are only needed if transistors M1 or M2 are off and CMFB circuit saturates, M1a and M2a will conduct current and help in recovering the CMFB circuit.

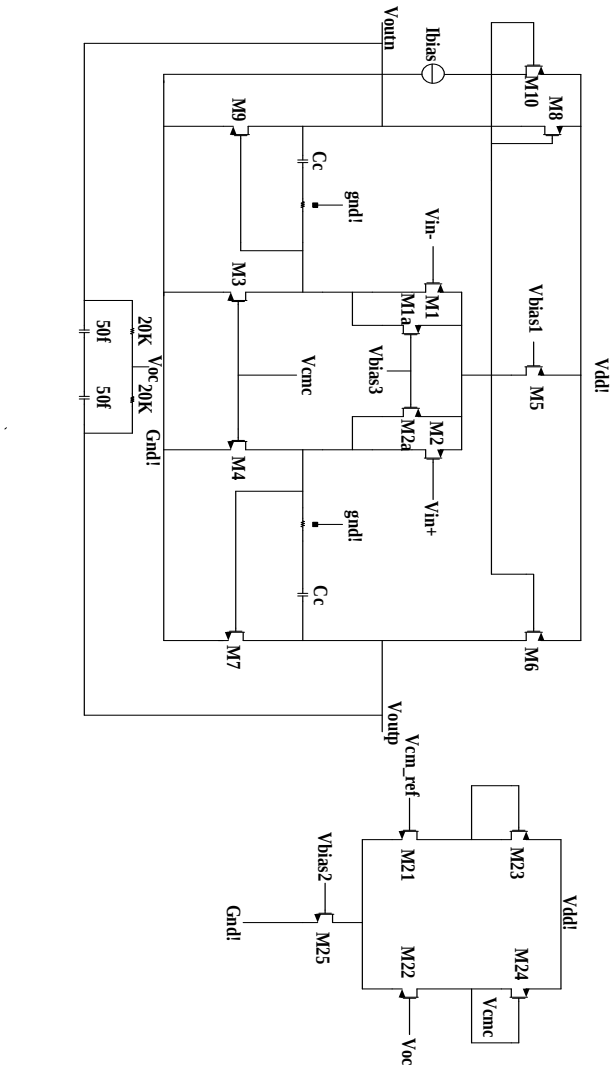

Figure 3.5 Two stage fully differential operational amplifier with common mode feedback circuit [4]

Miller compensation is used to stabilize the amplifier. So the op-amp is stable in a negative feedback configuration [5]. The miller capacitor introduces a pole in the system. So it basically moves the dominant pole down in frequency and the second pole high in frequency, a technique called pole splitting [4]. The feed forward path introduces a zero and this zero is not desired here as it will make the system unstable. So to get rid of this right half plane zero this feed forward path must be killed. This is done by introducing a nulling resistor in series with the compensation capacitor [4]. In this design resistor is implemented by a poly resistor since a poly resistor has a less parasitic capacitance.

CMFB circuit is required in all fully differential amplifiers. Vcmc is the common mode control input. Vcmc will bias M3, M4 in such a way so it can maintain the differential output at a common level which is 600mV in this thesis [4]. It is needed to stabilize the differential output voltage at a common level.

CMFB circuits are of two types 1) Switched Capacitor CMFB circuit [10] 2) Continuous time CMFB circuit [11].

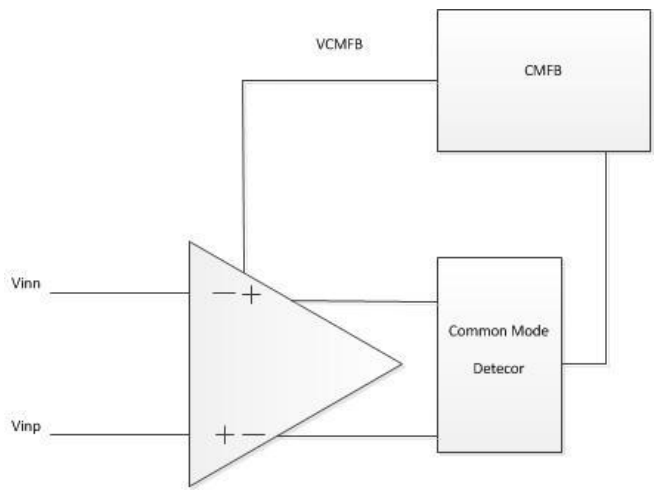

Figure 3.6 CMFB

Figure 3.6 shows a general block diagram of a fully differential amplifier with a CMFB. A CMFB circuit has a common mode signal detector and a sense amplifier. Figure 3.7 explains the common mode detector. Common mode signal detector is a parallel combination of two 20K resistors and 50fF capacitors. The capacitors are added to achieve better stability. The value of the resistors used in a common mode detector must be large enough compared to the differential amplifier output resistance so that it won't affect the open loop gain of the differential amplifier.

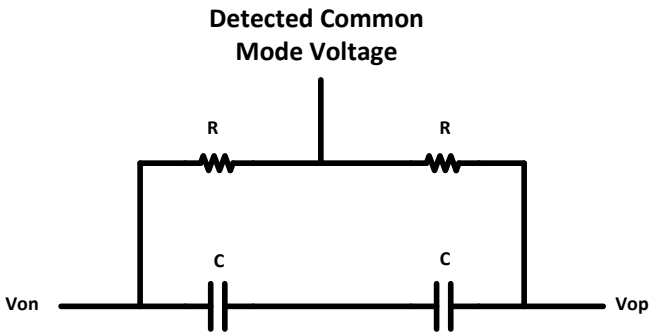

Figure 3.7 Common mode Detector

Common mode output voltage is the average of the differential outputs.

$$V_{cm} = \frac{(V_{op} + V_{on})}{2} \qquad (3.3)$$

The CMFB sense amplifier used in this operational amplifier is shown in figure 3.8[4].

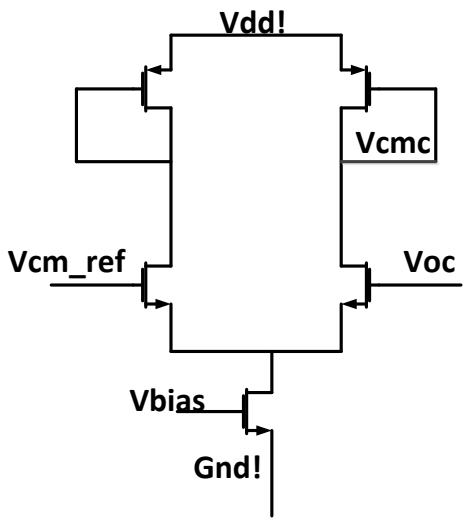

Figure 3.8 Common Mode Sense Amplifier

V_{oc} is the detected common mode output voltage and Vcm_ref is the desired common mode voltage. Common mode detected voltage, is compared with the desired voltage, Vcm_ref. The difference is amplified and the voltage Vcmc controls the gates of the current sources M3 and M4 which changes

the current in the output stage and it continues until Voc is equal to Vcm_ref [4].

3.2.3 Design of a two stage fully differential operational amplifier

3.2.3.1 Specifications

In this pipelined ADC table 3.1 shows the specifications which should be met in order to get this amplifier working in a pipelined system.

Table 3.1: Operational Amplifier Specifications

Parameter	Specification
Open Loop DC gain (dB)	$A > 2^N$ **[2]** **For, N = 6** $A > 36.12$
Phase margin(°)	**≥55**
GBW(MHz)	**200**
Slew Rate$\left(V/\mu S\right)$	**250**
$V_{dd}(V)$	**1.2**
$C_L(pF)$	**2**
$C_1(pF)$,$C_2(pF)$	**1**
$C_c(pF)$	**2**
Poly Resistance(Ω)	**154.71**
Common Mode Voltage (mV)	**600**

3.2.3.2 Aspect ratios

Table 3.2 shows the transistor dimensions.

Table 3.2: Transistor Dimensions

Transistor	$\left(\frac{W}{L}\right)$	$W(\mu m)$	$L(\mu m)$
$M_{1,2}$	1153.84	150	0.130
$M_{1a,2a}$	10	5	.5
$M_{3,4}$	32.21	32	1
M_5	257.75	257.7	1
$M_{6,8}$	615.2	615.2	1
$M_{7,9}$	384.61	50	0.130
M_{25}	64	32	.5
$M_{23,24}$	33	16.5	.5
$M_{21,22}$	40	16	.4

3.3 Comparator

In each pipeline stage there is a sub-ADC block for coarse quantization providing digital output for each stage. Also the last stage which is a 2-bit flash ADC use comparators. Each of these sub-ADC blocks uses two fully differential comparators. In this chapter, a comparator operation and its design is discussed. As it is desired to achieve a high speed and low power and the comparator design should be such that it consumes less power and do conversion at high speed.

3.3.1 Overview

A comparator is an operational amplifier in an open loop configuration. It is an important block in all of the ADCs. It is also used in other applications like in data transmission, switching power regulation [6]. A comparator compares two voltages, either two analog signals or an analog signal with a fixed reference and gives a digital signal in output based on the comparison. Figure 3.9 shows the schematic symbol of a voltage comparator. According to the comparator operation if $V_{in} > V_{ref}$ then $V_{out} = VDD$, if $V_{in} < V_{ref}$ then $V_{out} = 0$.

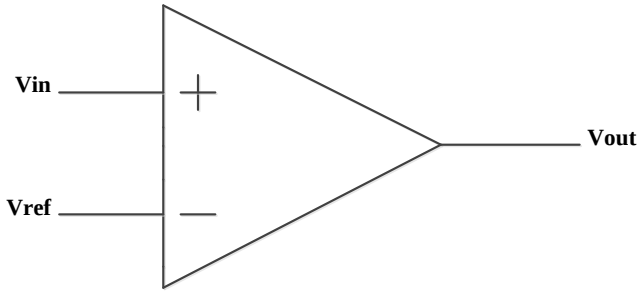

Figure 3.9 Basic Comparator Symbol

Comparator design for an ADC is very critical since speed and resolution is determined by how fast a comparator is working. Comparator can be of different types like static latched comparator, dynamic latched comparator [13]. Dynamic comparator doesn't have a pre-amplifier while static comparator does have a pre-amplifier circuit.

3.3.2 Comparator Characteristics

3.3.2.1 Propagation Delay

Propagation delay is the time difference between the input signal crossing the reference and output changing its code. In an ideal case, the propagation delay is zero but real comparators always have some delay. It determines the speed of the comparator that how fast the comparator will respond for a step input. It is tested by looking at how much does it take for the output to reach 50 % of a transition, when the input signal has crossed the reference level. Figure 3.10 shows how the propagation delay works in comparator.
Where tp is the propagation delay. Propagation delay can be reduced by increasing the overdrive voltage of the differential pair in a pre-amplifier block. So if the power is increased propagation delay comes down.

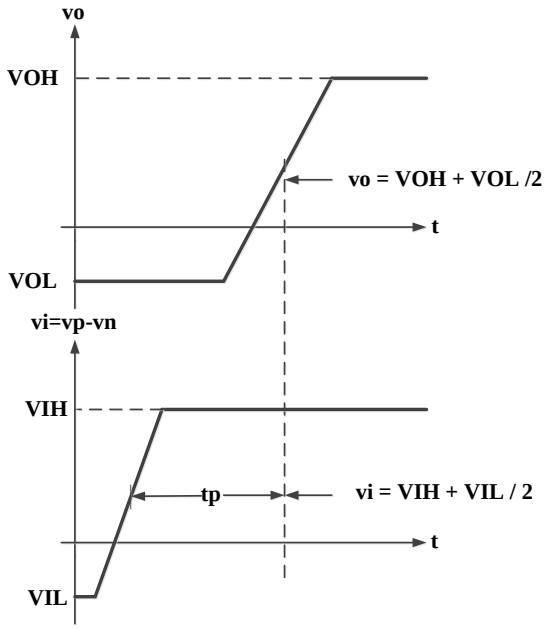

Figure 3.10 Propagation Delay Time [14]

3.3.2.2 Kickback Noise

During the regeneration phase of the comparator there are large voltage variations in the internal nodes due to switching which are coupled to the input and effects the behavior of the input voltage. This is called kickback noise. It can be reduced but not totally eliminated. Various techniques have been used for the reduction of kickback noise [15]. A pre-amplifier before the latching phase helps in reducing the kickback noise.

3.3.2.3 Hysteresis

When the comparator is placed in a noisy environment hysteresis is added. Without hysteresis the comparator response will toggle continuously between states due to noise when the input signal is near the threshold voltage. It will help the comparator response to stay away from such toggling [14].

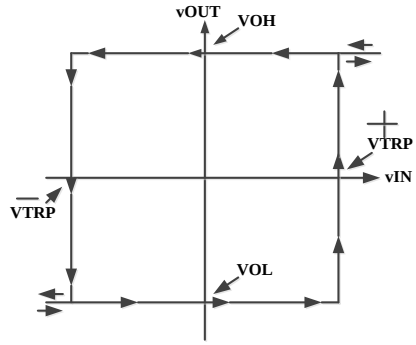

Figure 3.11 Comparator transfer curve with hysteresis [14]

Figure 3.11 shows the comparator transfer curve with hysteresis. Output is not changing its code until the input reaches the trip points both in the positive and the negative sides.

3.3.2.4 Offset

Offset is also a source of error in a comparator. It might be because of the mismatches in the input differential pair or if the comparator is not designed properly. There are techniques to eliminate the offset voltage [16].

3.3.2.5 Meta-stability

Meta-stability is the problem that has been encountered by the comparator when it takes more time to make a decision to switch to a valid output level in the time available for switching. It occurs when the input signal is not large enough, so at the end of the regeneration phase the output doesn't know the correct logic [3].

3.3.3 Comparator Design

3.3.3.1 Overview

The comparator used in this thesis is a static latched comparator [17] [18]. Static latch because of less kickback noise then a dynamic latch comparator but the power consumption is more as there is a pre-amplifier circuit. Figure 3.12 shows the block diagram of a comparator. It consists of three stages. A pre-amplifier circuit followed by a regenerative latch circuit, SR

latch and an output buffer. It has a differential input for the signal and a differential input for the reference voltages.

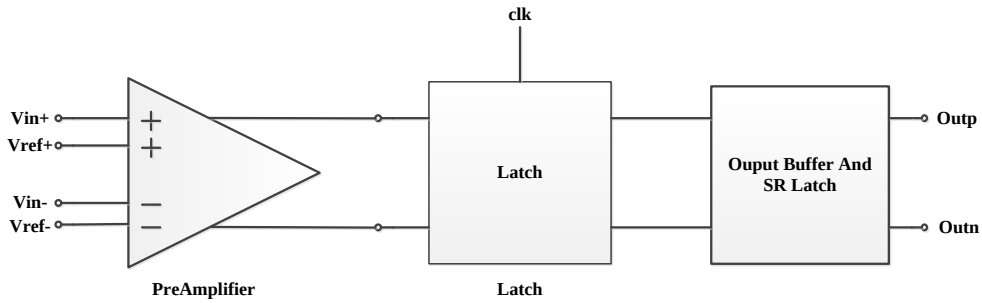

Figure 3.12 Comparator Block Diagram

3.3.3.2 Pre-Amplifier Circuit

A pre-amplifier is a differential amplifier circuit with a tail current source and active loads. Used with a latch in order to reduce the kickback noise. A preamplifier amplifies the input difference and the output currents are mirrored into the latch stage using current mirror. It helps in amplifying the difference between the input and the reference so it can be large enough to be detected by the latch stage within a very short time [19]. The preamplifier schematic is shown in the figure 3.13 as proposed in [20].
Figure 3.13 shows the schematic of a fully differential pre-amplifier circuit. NMOS M1, M2, M3, M4 are the input differential pair with PMOS M7, M8 diode connected active loads while NMOS M5 and M6 are the tail current source for the input differential pair.

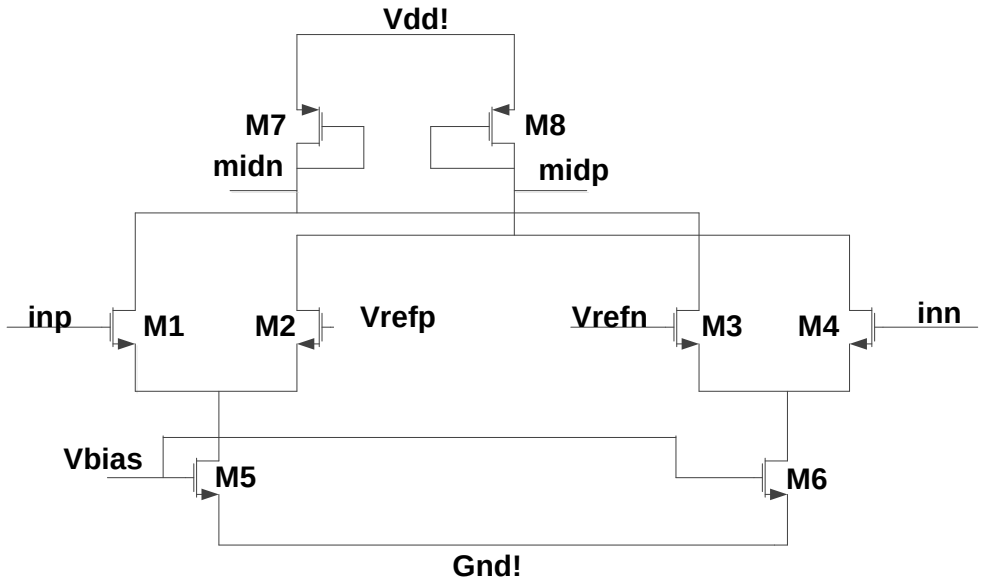

Figure 3.13 Fully Differential Pre-Amplifier

Table 3.3: Pre-Amplifier Aspect Ratios

Transistor	W(µm)	L(µm)
M1	4	2
M2	4	2
M3	4	2
M4	4	2
M5	4	1
M6	4	1
M7	2	0.240
M8	2	0.240

3.3.3.3 Latch Circuit

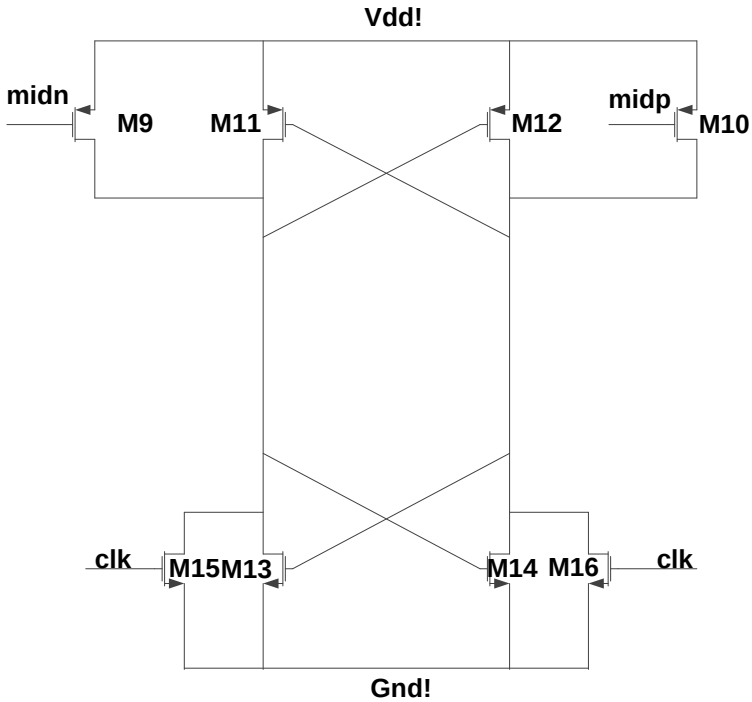

Figure 3.14 Regenerative latch

A latch stage consists of two back to back inverters. It consists of a cross coupled pair of PMOS and NMOS transistors. Controlled by a clock, a latch stage is the decision stage of the comparator. It works on two phases.
A reset phase and a regeneration phase. During the reset phase preamplifier current is mirrored to the output nodes. During the regeneration phase, due to positive feedback the small output voltage found in the beginning of this phase has been regenerated into full scale digital levels. Figure 3.14 shows latch schematic [20]. Latch is implemented using four transistors M11, M12, M13, M14 acting as inverter and connected in a back to back configuration. M9 and M10 is the current mirror from the pre-amplifier stage. M15 and M16 is the clock. Two positive feedbacks are used using the transistor pair M11, M13, M12, and M14 as it will increase the conversion speed.

Table 3.4: Regenerative Latch Aspect Ratios

Transistor	W(μm)	L(μm)
M11	8	0.120
M12	8	0.120
M13	4	0.120
M14	4	0.120
M15	36	0.120
M16	36	0.120
M9	1	0.5
M10	1	0.5

3.3.3.4 Positive Feedback

A positive feedback plays a very useful role in improving the performance of a comparator. It will actually push the two outputs away from each other, where one will go to the supply voltage and the other towards ground depending upon which one is greater.

3.3.3.5 Comparator Schematic

Pre-amplifier and regenerative latch schematics are shown in figure 3.13 and figure 3.14. Based on these circuits the schematic of the complete comparator used in this thesis is shown in figure 3.15 [21] [22] [23] [24] [25] [26]. The pre-amplifier output is connected to the input of the regenerative latch circuit. The latch output is connected to the output buffer formed by a series combination of two inverters whose output is then connected to SR latch. During the reset phase, clock is high. NMOS transistors M15, M16 controlled by a clock signal push the outputs to ground. The voltage at the output node is zero during this phase. The differential input is amplified by the NMOS differential pair and the differential current is mirrored by the diode connected PMOS load formed by M7, M8. Now the next phase is the regeneration phase. It is initialized when the clock goes low. A voltage difference is created due to different current flowing through transistors M9 and M10. This voltage difference is amplified to full scale by the positive feedback. An imbalance situation is created at the output node. Voltage at one node is greater than the other node. NMOS M15, M16 are open now. So the voltage difference created during the reset phase is regenerated during this phase using two positive

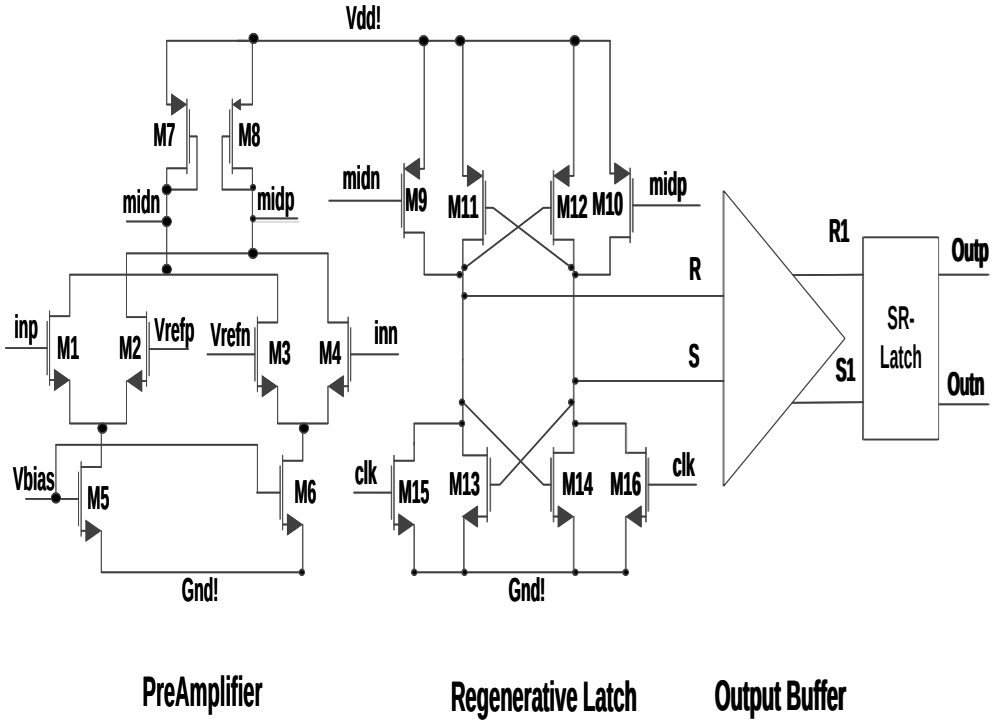

Figure 3.15 Comparator Schematic

feedbacks. Two back to back inverters formed by transistor pair M11, M13 and M12, M14 will generate the voltage difference created at the output node into a full scale digital level. Suppose the gate voltage of M14 is greater than that of M13. More current will flow through M14 than M13. It will push M14 to lower level and M13 to higher level. Same is the case at the top. The gate voltage of M12 is more than M11. So M11 will give the supply voltage at the node and M12 is open so the voltage at the drain of M12 is zero. So basically the positive feedback is pushing one voltage to the supply and the other one to the ground. That's how the latch stage is working.

3.3.3.6 Output Buffer

Output buffer is used at the output of the latch stage to reduce the gap between the output voltage and the full scale. It will help in restoring the output of the latch circuit into full logic level. Figure 3.16 shows the block diagram of output buffer consisting of inverters.

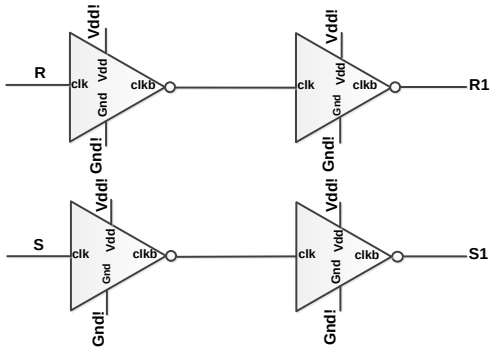

Figure 3.16 Output Buffer

3.3.3.7 SR latch

SR-latch has been added at the output to keep the data stable. If the analog input is stable the digital output should also be stable and that's what is achieved using an SR-latch. It will help in sustaining the previous output. The output will not be reset each time the clock transitions if an SR-latch has been connected. Figure 3.17 shows the schematic of a conventional SR-latch used in this thesis [27].

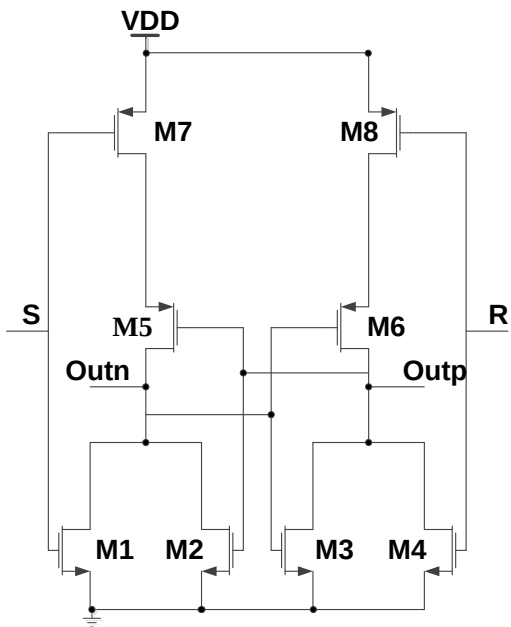

Figure 3.17 SR-Latch

According to figure 3.17, SR latch has two inputs S(set) and R(reset) and gives two complementary outputs, outn and outp. If the set input is high and reset input is low, transistors M1, M2 will be on resulting in an output voltage of zero volts at node outn. Whereas, the voltage at node outp is equal to the supply as both M3, M4 are off. If the reset input is high and set input is low, the situation will be reversed. In that case M1, M2 turned off and M3, M4 turned on, giving the supply voltage at node outn and zero voltage at node outp.

3.4 Two phase Non-Overlapping Clock

In a pipelined ADC, operation of all the stages depends on a two phase non-overlapping clock signals. Two non-overlapping clocks P1d and P2d are out of phase by 180° and there is also some delay between the clock transitions. During P1d all the odd stages will sample the analog input signal and during P2d a valid residue is passed to the subsequent stage. For even number of stages, the working will be on opposite clock phases. After some initial delay, on every clock cycle there is a valid bit from each stage. Since the clock is skewed between alternate stages, each stage must settle within $\frac{1}{2}$ of the clock period. So, for the pipelined ADC where the sampling frequency is 50MHz, each stage must settle within 10ns. Additional two clocks P1 and P2 are needed to ensure bottom plate sampling in a switched capacitor circuit used in each stage for reducing charge injection. Schematic of two phase non-overlapping clock is shown in figure 3.18. The design was adopted from [31].
Figure 3.18 shows the schematic of a two phase non-overlapping clock. Various inverters and NAND gates are used to get the required clock phases. Inverters add delay to the clock signal. At the output four clock signals P1, P1d, P2, and P2d can be seen ready to get feed in to the ADC.

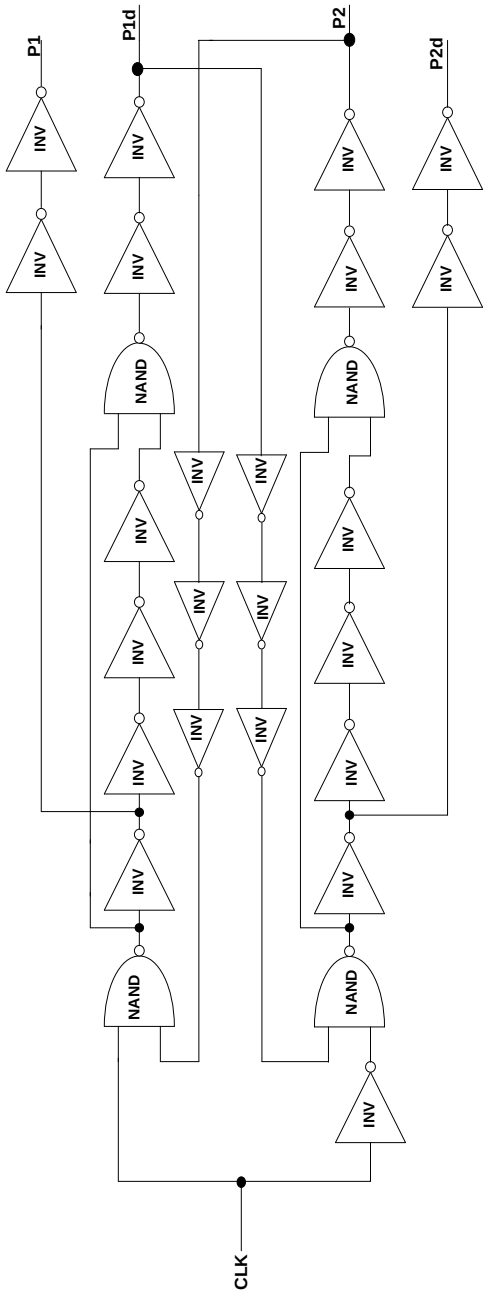

Figure 3.18 Two Phase Non-Overlapping Clock

CHAPTER 4

4 Simulation Results

This chapter discusses the Verilog-A modeling and the schematic testing of the pipeline ADC. System design of different blocks used in a pipeline ADC is simulated and then 1.5-bit stages are cascaded to build the overall converter. How different blocks behave and the behavior of the overall converter using Verilog-A and transistor level modeling has been described in this chapter. After that different tests are performed on the system. First a linearity test is performed. After linearity test a single tone test is done. The output data is then exported to MATLAB to see the SNDR, SFDR and INL/DNL.

4.1 Two Phase Non-Overlapping clock

The two phase non-overlapping clock is designed to run at 50MHz. The schematic of a non-overlapping clock is described in chapter 3. Now a test bench is created to test the clock. So the main clock with a sampling frequency of 50MHz is connected to the clock generator. A Vpulse source from analogLib has been used to generate the square wave clock pulse with an amplitude of 1.2 V. Simulation results are shown in figure 4.1 after running a 40 ns transient simulation.

Figure 4.1 shows the simulation results of the two phase non-overlapping clock generator. According to the figure 4.1, the t_{nov}, which is the non-overlap period between P1d and P2d is 0.36ns and the lagging period t_{lag} between P1d and P1 is 0.21ns. So, each stage should get settled within 9.43 ns.

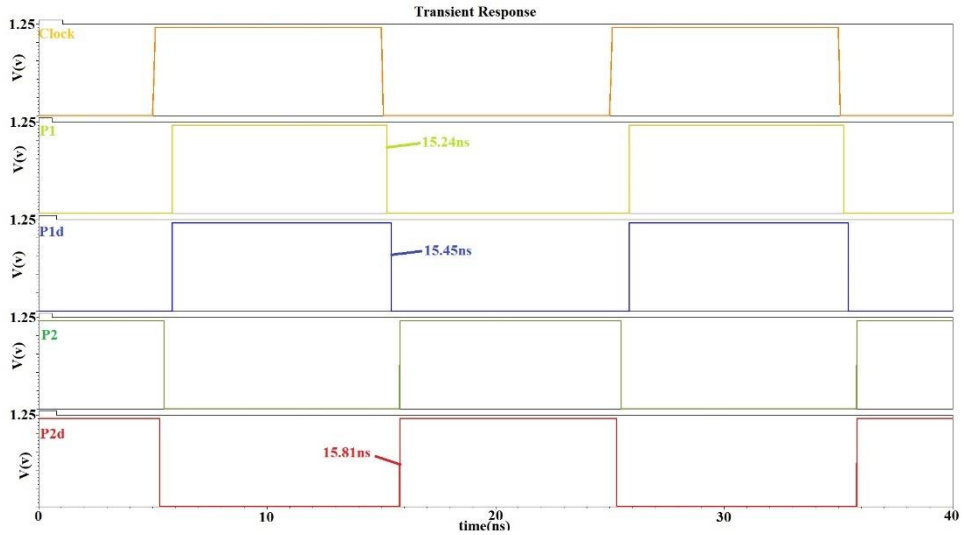

Figure 4.1 Simulation Results of Clock

4.2 Operational Amplifier

An operational amplifier is one of the most important blocks in the design of a pipelined ADC. Details about the operational amplifier design have been explained in chapter-03. In this chapter testing of the operational amplifier is done using Cadence Spectre Simulation toolbox at a supply of 1.2 V. Simulation results like GBW, DC gain, phase margin, CMFB stability has been discussed. Simulation results shows that the operational amplifier is fit to be plugged into the pipelined converter to get the system work though there are other blocks too but the operational amplifier is the most important block in a pipelined converter. Figure 4.2 shows the test bench setup of a fully differential operational amplifier with a load capacitance of 2pF. It has been tested using different analysis in analog design environment.

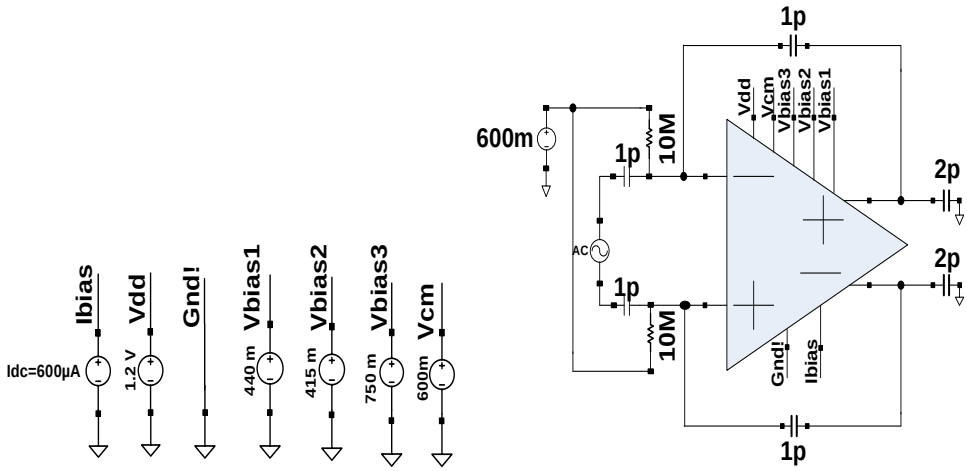

Figure 4.2 Operational Amplifier Test Bench

4.2.1 AC Simulations

AC analysis has been performed to check the open loop DC gain and the Phase margin for a given operational amplifier. The DC bias to the input stage of the op-amp is provided through a 10M ohm resistor.

Figure 4.3 shows the frequency response after simulating the test bench setup shown in figure 4.2. Two plots are plotted. First is the gain plot which shows the operational amplifier open loop DC gain and the unity gain frequency (GBW) and the second one is phase plot which shows the open loop phase margin. Current flowing into the input differential pair is 1.58mA and the current flowing into each output stage is 7.42mA. 600µA is the current from the current source (Ibias) whereas the current flowing into the sense amplifier is 394.79µA. So, the total current consumption is 17.41mA. For a 1.2V supply, the total power consumption of this op-amp is 20.8mW.

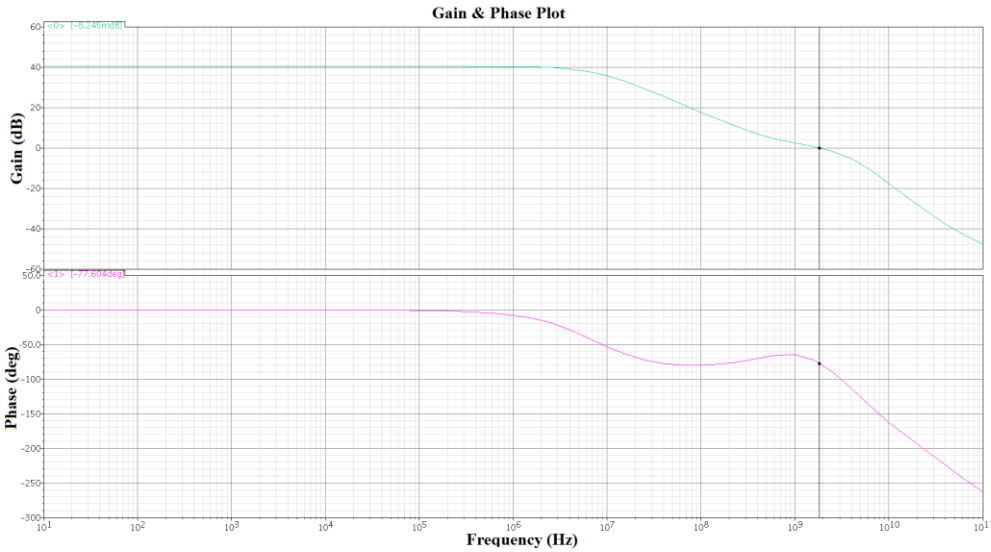

Figure 4.3 AC Gain and Phase Response

The AC simulation response is shown in figure 4.3. Unity gain frequency is where the DC gain drops to 0dB and phase margin is the phase shift at unity gain frequency. Phase margin is calculated from equation 4.1.

$$Phase\ Margin = 180° - 77.60° \qquad (4.1)$$

The above AC analysis shows that the designed operational amplifier has a DC gain of 41dB, a unity gain frequency of 1.81GHz and a phase margin of 102° which meets the Op-amp specifications in table 3.1. Op-amp gain error will alter the jump in the residue curve whenever the sub ADC transition say from 00 to 01. This will result in missing codes at the output of overall pipelined ADC whenever the sub ADC changes state while performing ramp simulation. Missing codes will degrade the overall performance of the converter by introducing nonlinearity and harmonic distortion. To perform linear conversion missing codes are not desired and needs to be eliminated by achieving a good DC gain. A high phase margin is good for an Op-amp to be stable and not go into instability for subsequent pipeline stages and hence avoid overshoot and ringing. A high GBW will ensure that the Op-amp will settle fast, so that overall performance of the ADC is not degraded due to non-linearity caused by

slow settling. For an Op-amp to be sufficiently settled within a given time frame it must have enough bandwidth.

4.2.2 Stability Simulation

Next test is to check the stability of common mode feedback circuit. A cmdm probe and iprobe from the analogLib is used to check the stability of common mode feedback circuit. After performing the stability test it was found that the common mode feedback circuit is stable with a phase margin of 54° which is reasonable. Figure 4.4 shows common mode feedback circuit phase margin after doing stability analysis.

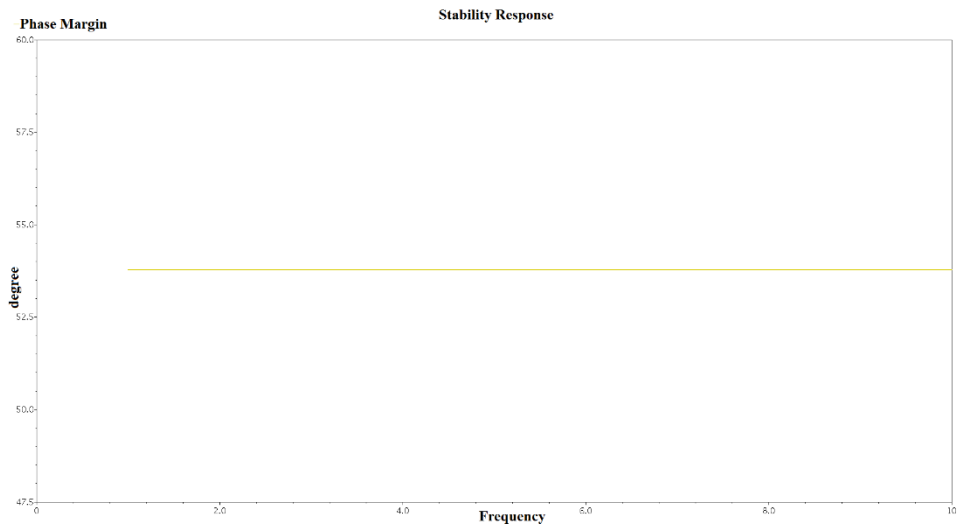

Figure 4.4 Common Mode Feedback Circuit Phase Margin

4.3 Comparator

Next is to test the comparator used in a sub ADC block. The working of the differential comparator has been explained in chapter 3. Figure 4.5 shows the test bench setup of differential comparator with an input ramped from -500mV to 500mV. Vinp is ramped from 350mV to 850mV and Vinn is ramped from 850mV to 350mV. Vrefp and Vrefn sets the threshold at 125mV by setting Vrefp to 662.5mV and Vrefn to 537.5mV.

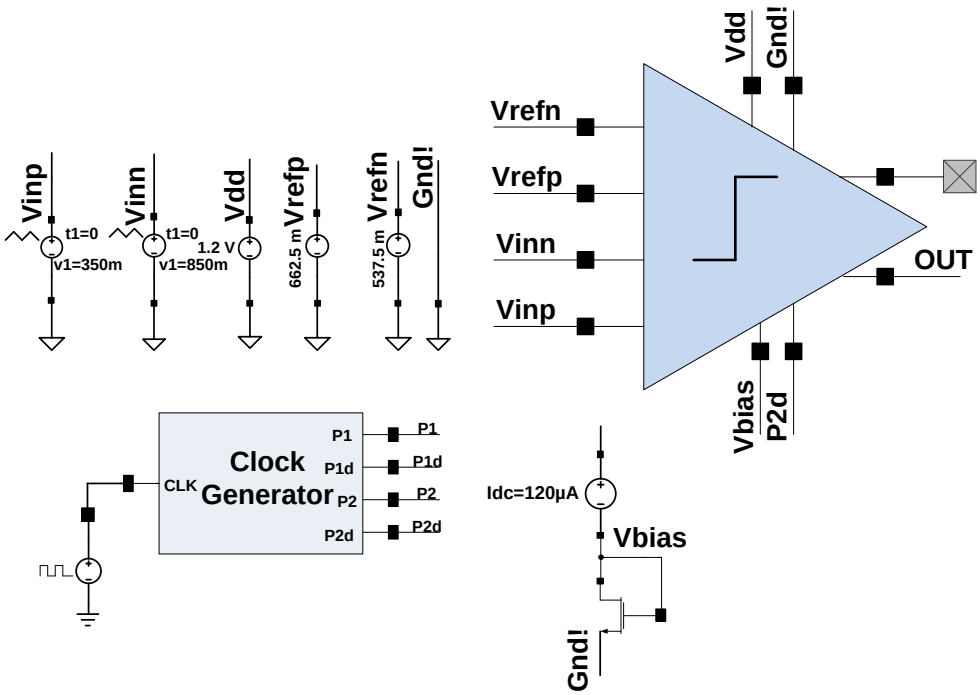

Figure 4.5 Comparator Test bench

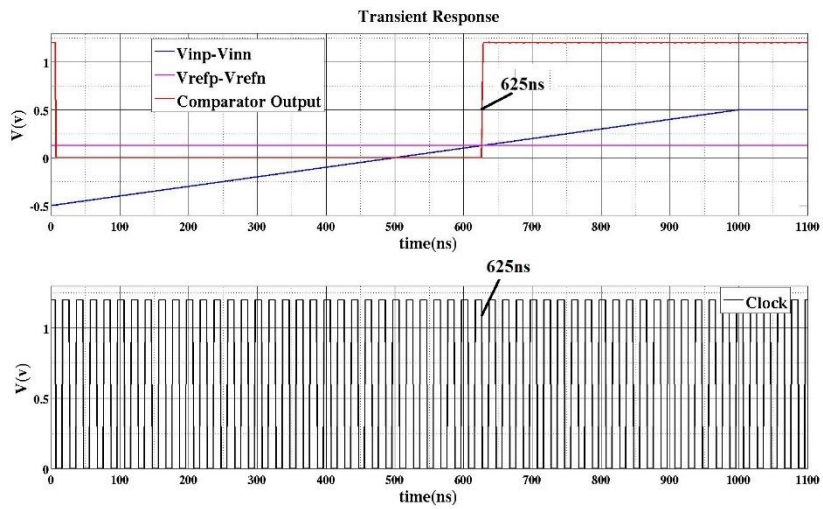

Figure 4.6 Simulation Result of differential Comparator

Figure 4.6 shows the simulation results for a differential comparator. As soon as the input crosses the reference voltage, comparator output changes its state from 0 to 1 on the falling edge of the clock. Comparator output

transition from 0 to 1 at the same time instant of falling edge of the clock. Simulation done at 50MHz shows that the comparator works well at 50MHz.

4.4 SHA

SHA block is tested in Cadence Spectre simulator at a clock frequency of 50MHz. The input voltage is a ramp signal where Vinp is ramped from 350mV to 850mV and Vinn is ramped from 850mV to 350mV. Figure 4.7 shows the schematic of the SHA used in this thesis whereas the test bench is shown in figure 4.8 with a load capacitor of 2pF. According to simulation results in figure 4.9, SHA is working well at 50MHz clock.

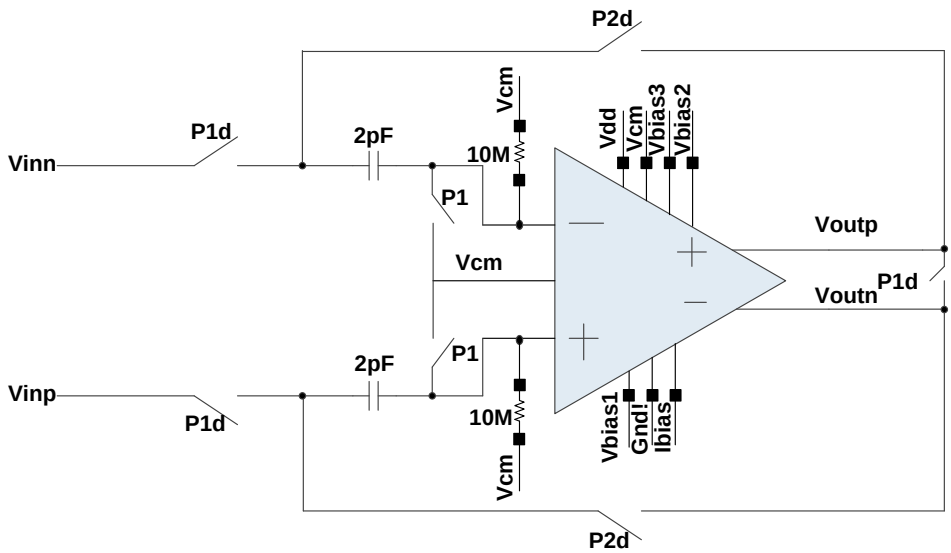

Figure 4.7 SHA Schematic

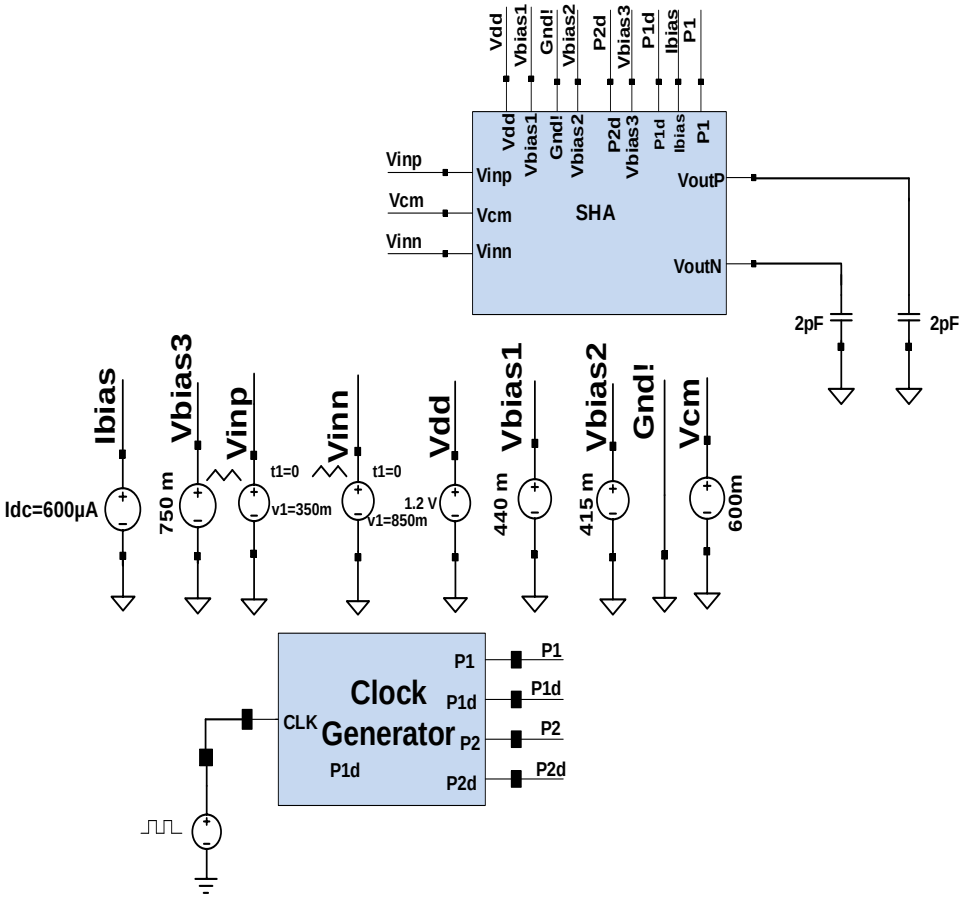

Figure 4.8 SHA Test bench

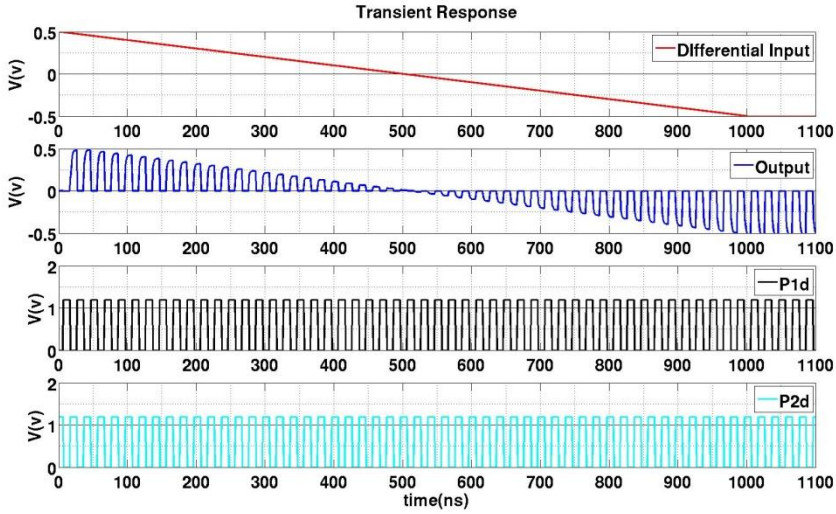

Figure 4.9 Simulation Results of SHA

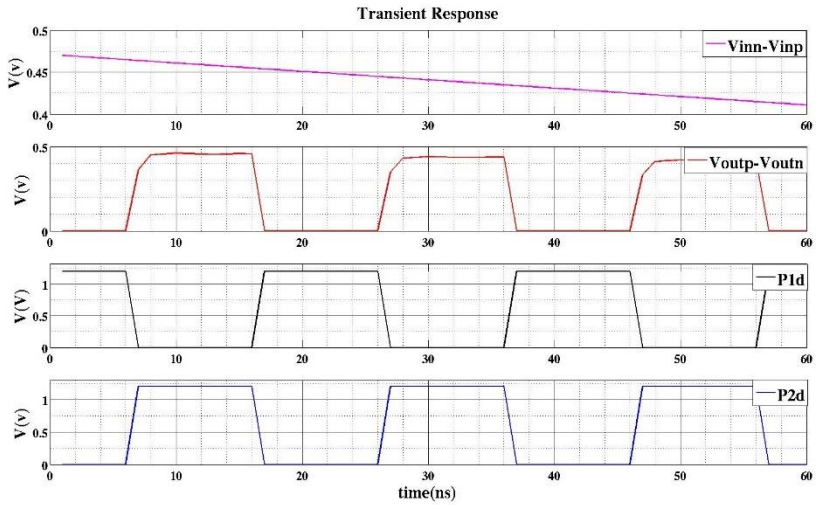

Figure 4.10 Simulation Results of SHA for few clock cycles

Figure 4.10 shows SHA results after zooming in the transient response in figure 4.9 for few clock cycles. SHA is accurately sampling and holding at correct time intervals. During P1d input is sampled correctly. During P2d it is correctly holding the value of previous input.

4.5 Sub ADC

Each pipeline stage has a 1.5-bit sub ADC block consisting of two comparators. Figure 4.11 shows the test bench schematic of the sub ADC block. Two thresholds at 125mV and -125mV are set by the reference voltage by setting Vrefp to 662.5mV and Vrefn to 536.5mV. Vinp is ramped from 350mV to 850mV and Vinn is ramped from 850mV to 350mV (-500mV to 500mV) differential. Figure 4.12 shows the simulation results of a sub ADC block. The sub ADC works well at 50MHz clock frequency.

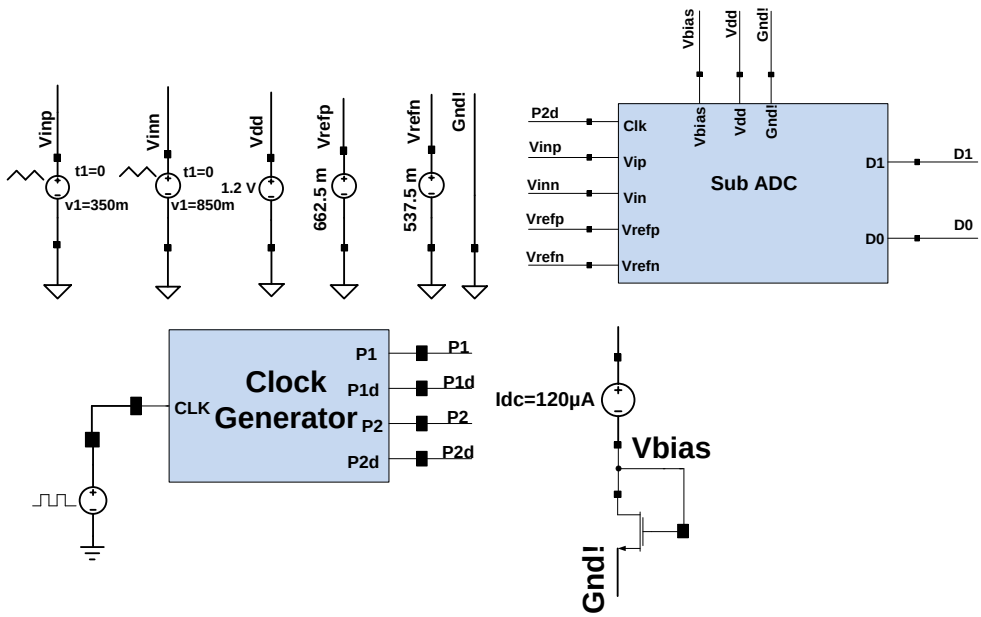

Figure 4.11 Sub ADC test bench

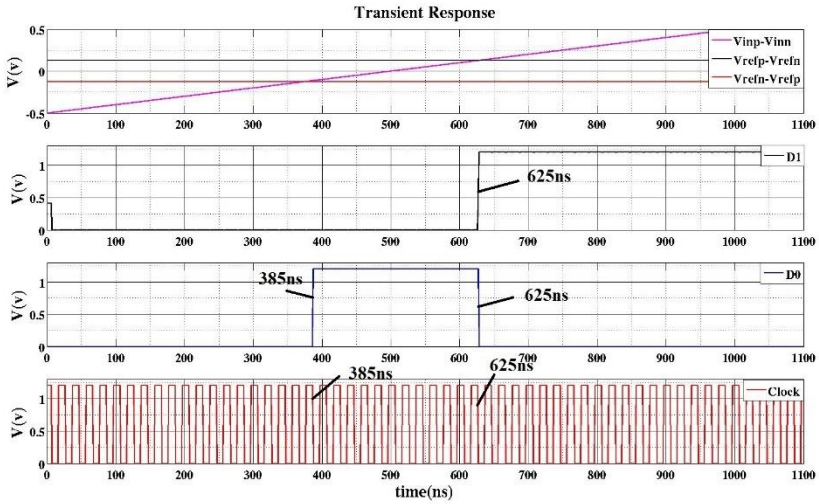

Figure 4.12 Simulation Result of Sub ADC

Input crosses the lower threshold (-125mV) at 385ns. Comparator output D0 transition from 0 to 1 at the falling edge of clock. Comparator output D1 transition from 0 to 1 when the input crosses the upper threshold (125mV) at 625ns and D0 transition from 1 to 0 at falling edge of the clock. A 1.5-bit sub ADC must produce three different bit combination (00, 01, 10) which can be seen in figure 4.12.
In figure 4.12 D1 is the comparator output for upper threshold (125mV) and D0 is the comparator output for lower threshold (-125mV).

4.6 Sub DAC

In this section sub DAC is tested. Figure 4.13 shows the test bench schematic of a sub DAC block. Two square wave inputs at a clock frequency of 50MHz are applied. Figure 4.14 shows the simulation results of the sub DAC. The designed sub DAC works well at 50MHz.

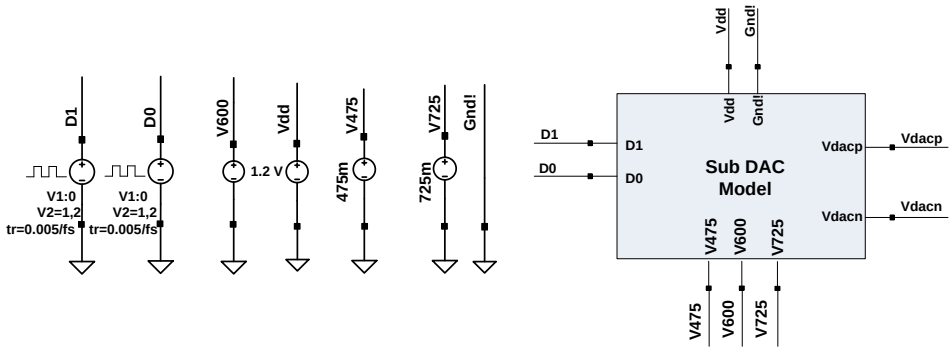

Figure 4.13 Sub DAC model Test bench

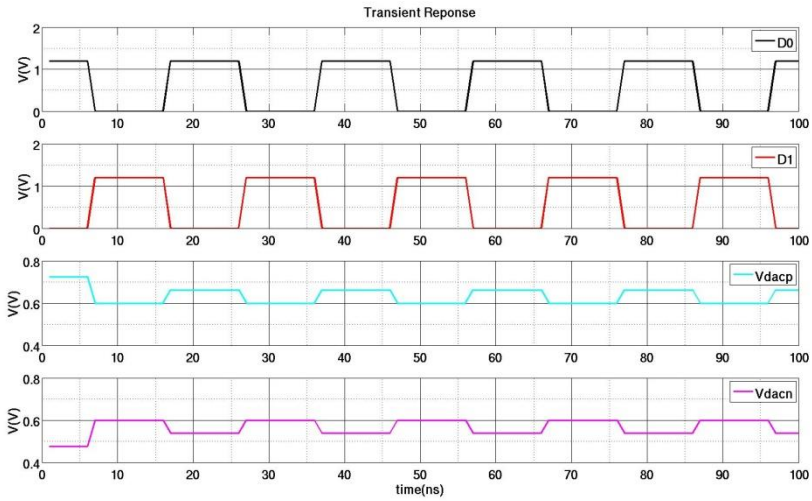

Figure 4.14 Sub DAC model Transient Response

4.7 1.5-bit stage

4.7.1 System Modeling

Figure 4.16 shows the test bench schematic of a 1.5-bit stage pipeline ADC system model which is tested at 50MHz. The differential input is from -500mV to 500mV with inp ramped from 350mV to 850mV and inn ramped from 850mV to 350mV. The 1.5-bit stage is simulated successfully at 50 MHz and the corresponding residue plot is shown in figure 4.15 which is

what expected from a 1.5-bit stage according to the transfer curve of 1.5-bit MDAC as shown in Figure 2.8. As the sub ADC transitions from 00 -> 01 ->10, the transfer curve changes states.

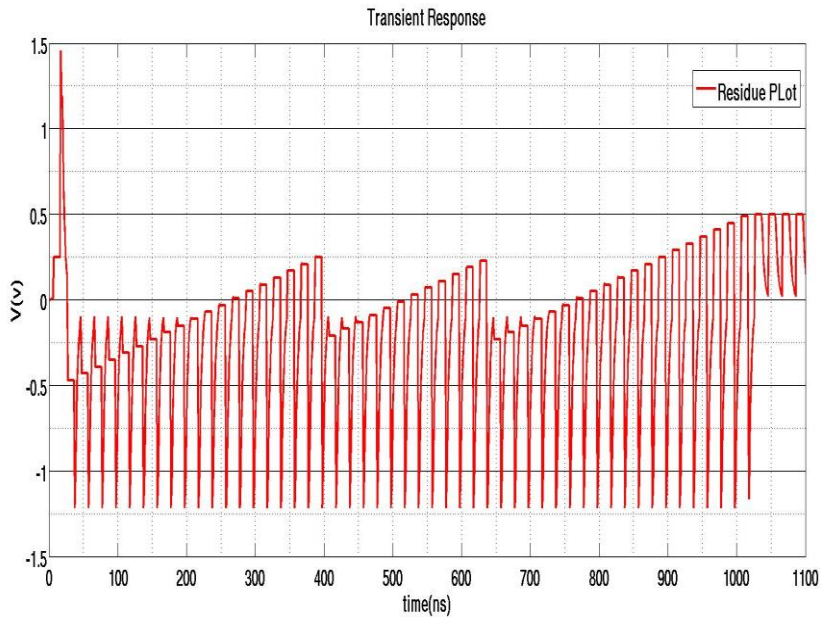

Figure 4.15 Residue Plot from a 1.5-bit stage System Model

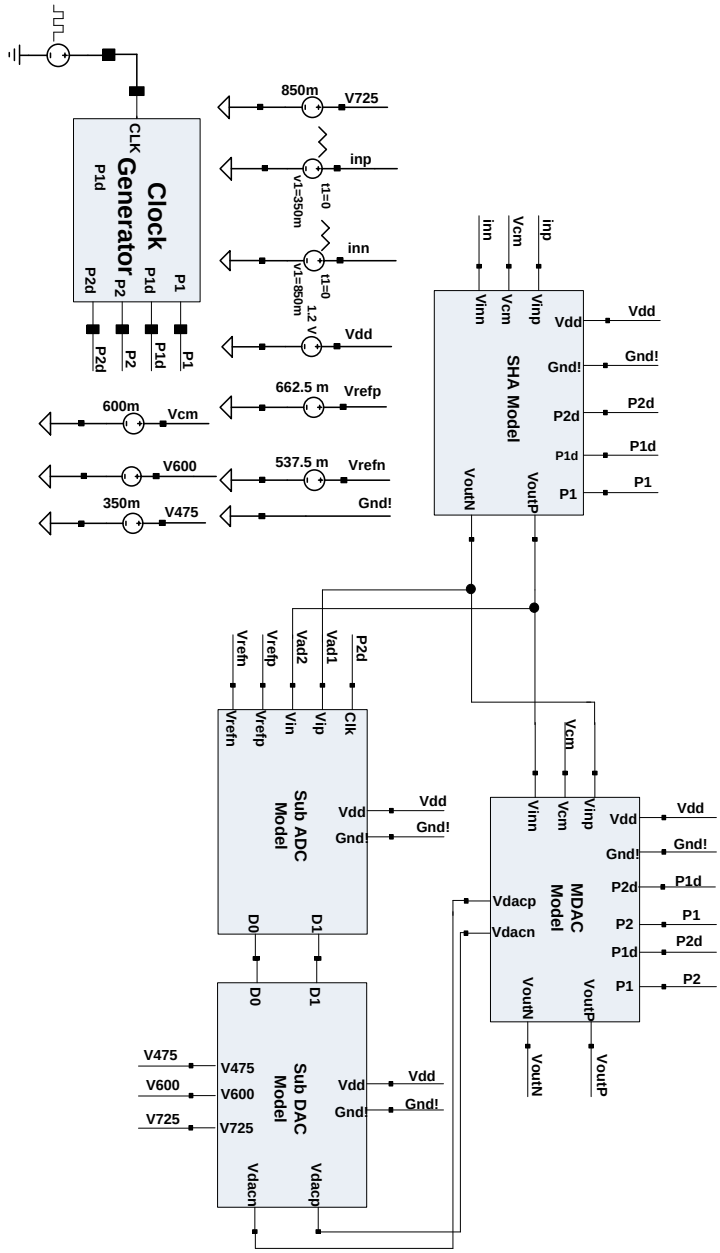

Figure 4.16 1.5-bit stage System Model

4.7.2 Transistor Level Simulation

Figure 4.19 shows the test bench schematic of a 1.5-bit stage pipelined ADC which is tested at 50MHz. The differential input is ramped from -500mV to 500mV with Vinp ramped from 350mV to 850mV and Vinn ramped from 850mV to 350mV. The 1.5-bit stage is simulated successfully and the corresponding residue plot is shown in figure 4.17.

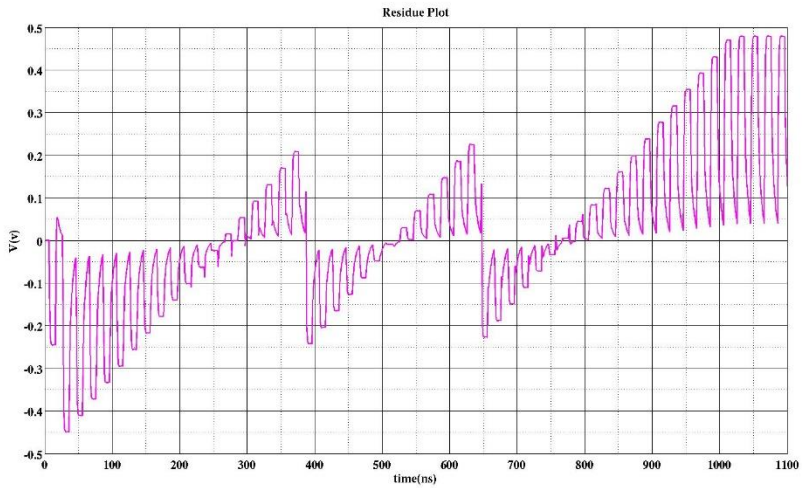

Figure 4.17 Residue Plot

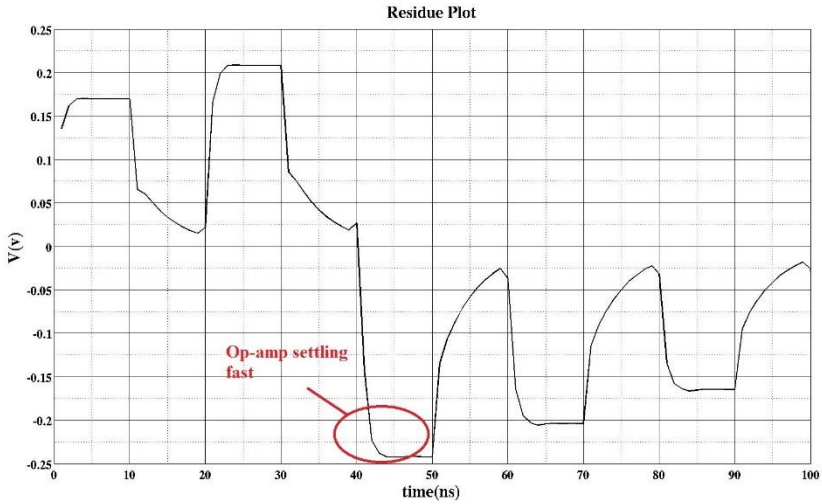

Figure 4.18 Residue Plot at first sub ADC transition

Figure 4.18 shows the residue plot after zooming in Figure 4.15 near the first sub ADC transition (00 -> 01). It is clear that the Op-amp is fast enough at a clock frequency of 50MHz. Output is settled completely at the point circled in red. Once the settling requirements are fulfilled at 50MHz clock, a 6-bit pipelined ADC is assembled and tested in next section.

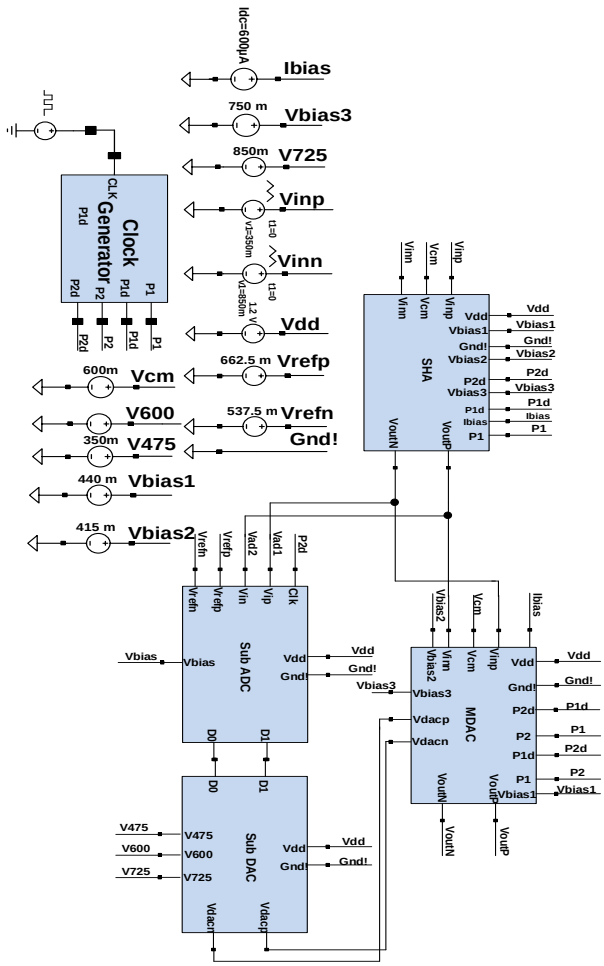

Figure 4.19 1.5-bit stage Test bench

4.8 Five Stage Pipelined ADC test

4.8.1 System Modeling

Now the performance of the pipelined ADC when five stages are cascaded is analyzed to obtain a 6-bit converter. The first four stages are 1.5-bit stages whose schematic is described in figure 4.16 and the last stage is 2-bit flash ADC. The four stages, shift register, digital correction logic and the DAC are connected together to form the pipelined ADC under test. Figure 4.20 show the schematic of a five stage pipelined ADC.

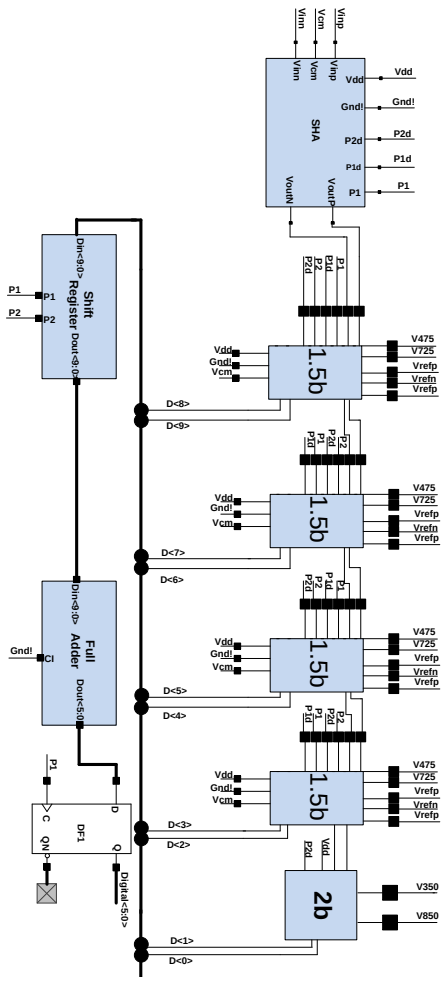

Figure 4.20 Five Stage Model Schematic

4.8.1.1 ADC Linearity test

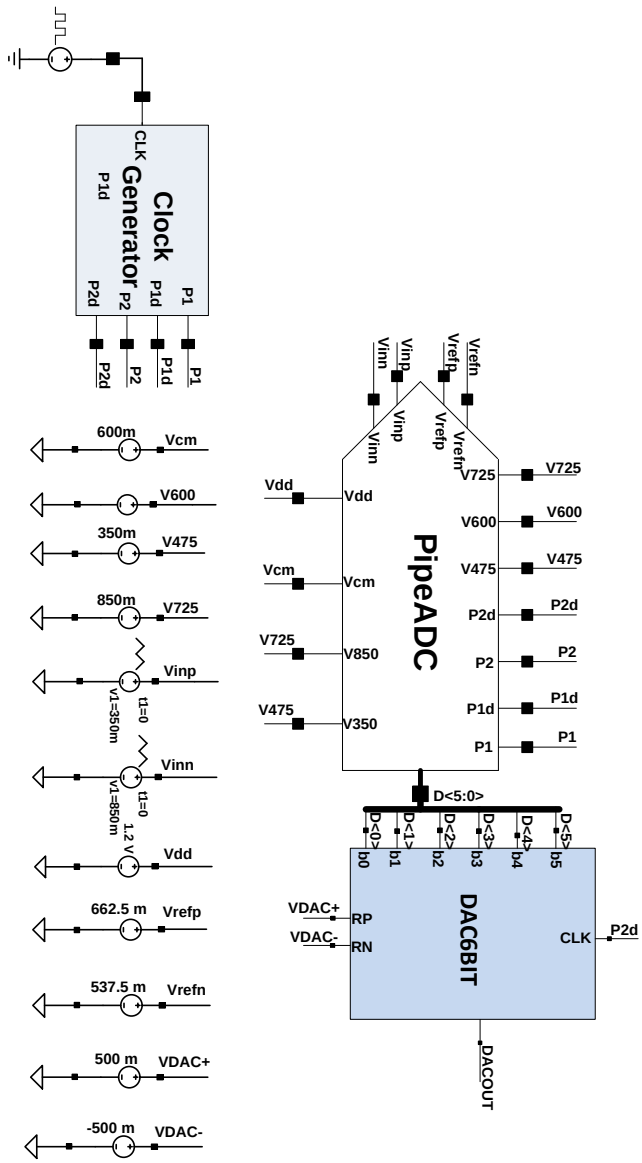

Figure 4.21 Five stage Model Test bench

Figure 4.21 shows the test bench setup for a five stage pipelined ADC linearity test. The input ramp settings for the positive ramp are from 350mV-850mV and for the negative ramp from 850mV-350mV. So, a differential input from -500mV-500mV was applied. A transient simulation was run for 13us at a clock frequency of 50MHz. ADC output is followed by a 6-bit DAC in order to generate a stair case output to see if the converter is giving the correct output codes.

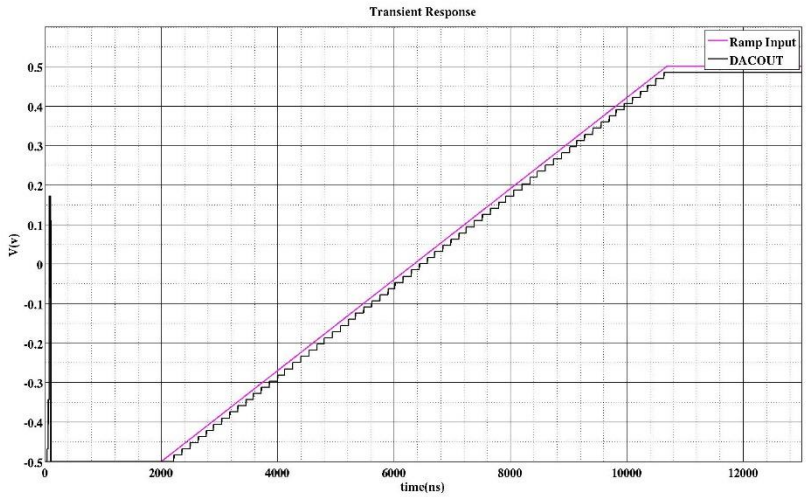

Figure 4.22 Five stage ADC model Ramp test

Figure 4.22 shows the linearity test results. For a 6-bit converter, 64 different output codes are obtained with a step size of 1 LSB. Where 1 LSB is 15.62 mV for a 6-bit ADC. The output tracks the input of the ADC very well. As everything is ideal, so there is no missing code or glitch in the output.

4.8.1.2 ADC Single-tone test

Figure 4.23 shows the test bench setup for a single-tone test with a transient stop time of 48us. Simulations were performed at two different input frequencies, 317.38KHz and 13.01MHz using Cadence Spectre transient analyses. Figure 4.24 shows the simulation result for an input frequency of 317.38KHz at a clock rate of 50MHz. A sine wave can be seen at the output.

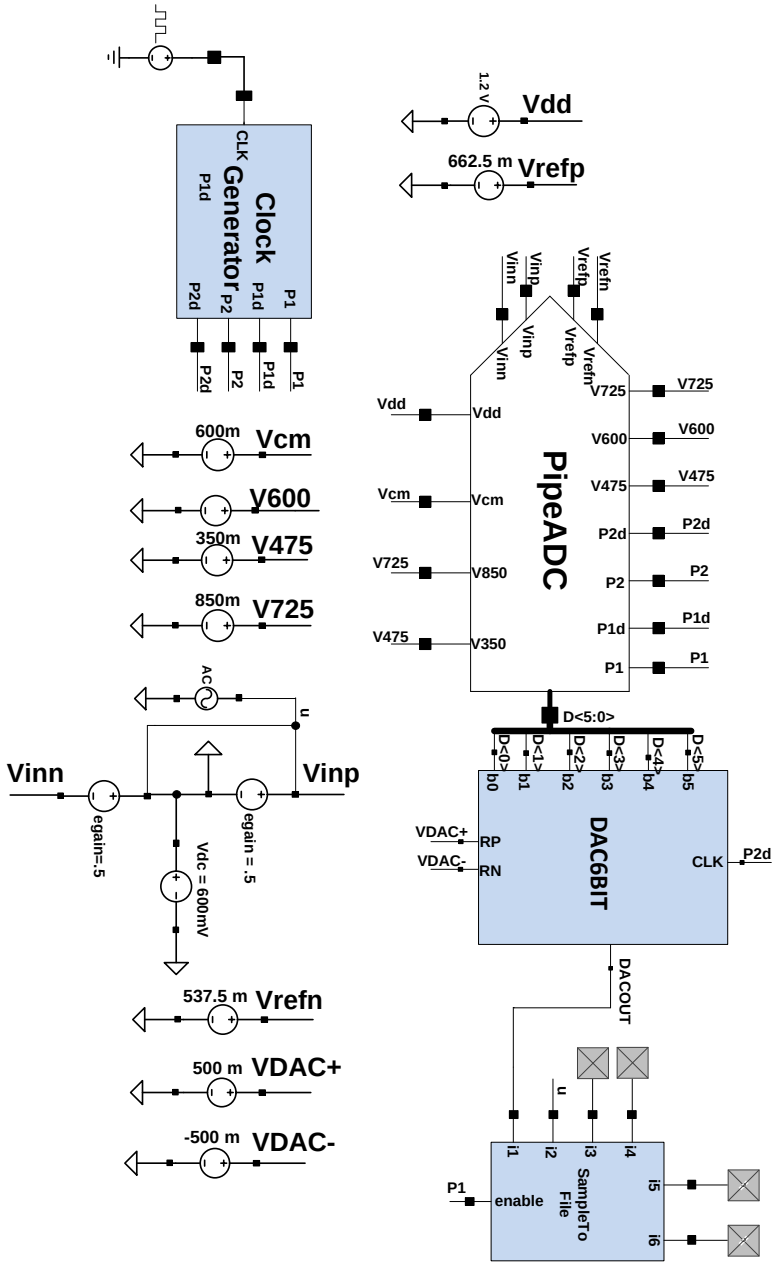

Figure 4.23 Test bench setup for a system model single-tone test

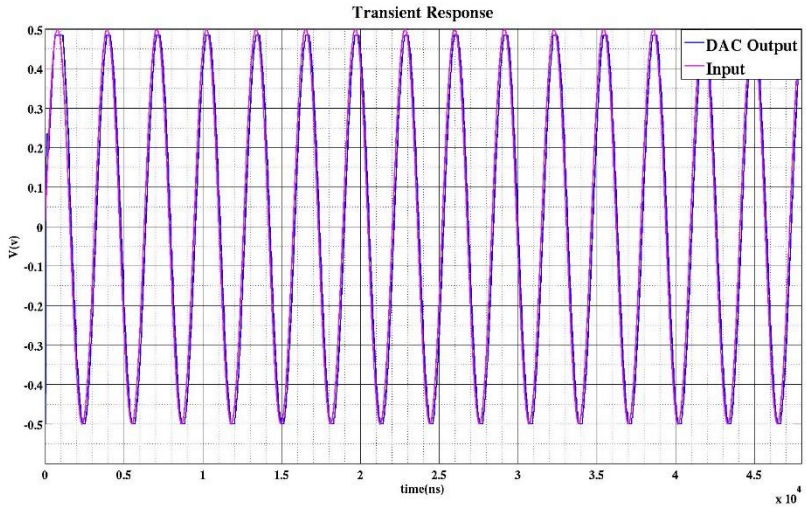

Figure 4.24 Single-tone test simulation result for input frequency of 317.38KHz

The output data is then exported to MATLAB using SampleToFile block to check the SNDR and SFDR. SNDR is the ratio of fundamental signal power to the total noise and harmonic distortion at ADC output spectrum excluding dc when a sinusoid is applied as an input to the ADC. Better SNDR ensures a good overall dynamic performance of an ADC. SFDR is the ratio of the full-scale fundamental signal to the strongest spurious signal in the spectrum from dc to fs/2. SFDR is an important performance parameter because it tells how well the fundamental signal is distinguished from the largest harmonic (spur) irrespective of where the harmonic falls in the spectrum. 2048 data points are collected at the output for plotting FFT spectrum. Figure 4.25 shows the ADC output FFT spectrum from dc to fs/2 after applying a differential sinusoid input of 317.38KHz. Theoretically, according to equation 4.2 for a 6-bit ADC SNDR is 37.88dB.

$$SNDR = 6.02n + 1.76dB \qquad (4.2)$$

Where n is the resolution of converter.
Simulation results shows that the proposed ADC achieves an SNDR of 37.4dB for a full scale sine input which is very close to the theoretical value of 37.88dB and an SFDR of 52.26dB which is promising for a 6-bit performance. Figure 4.26 shows the FFT spectrum for 13.01MHz input. Proposed ADC system model achieved an SNDR of 37dB and an SFDR of 51.31dB. Measured SNDR and SFDR shows the system modeling is

working well for both low and high input frequencies at a sampling rate of 50Msample/sec.

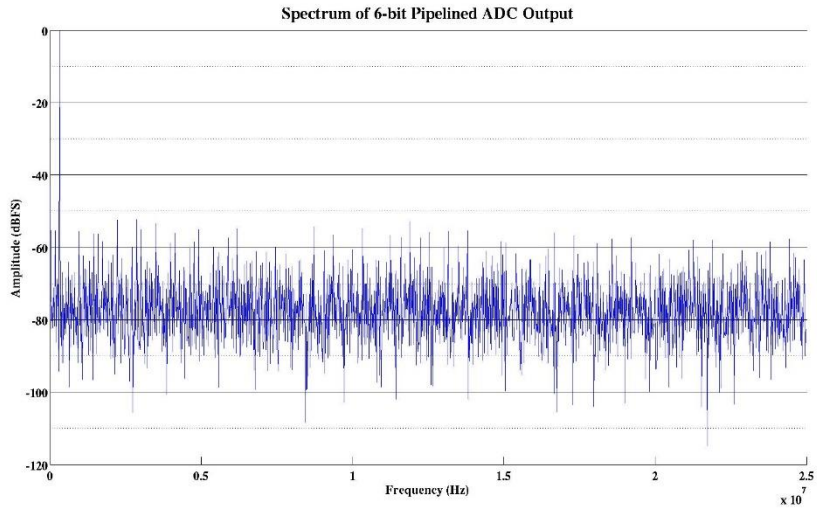

Figure 4.25 FFT Plot for input frequency of 317.38KHz

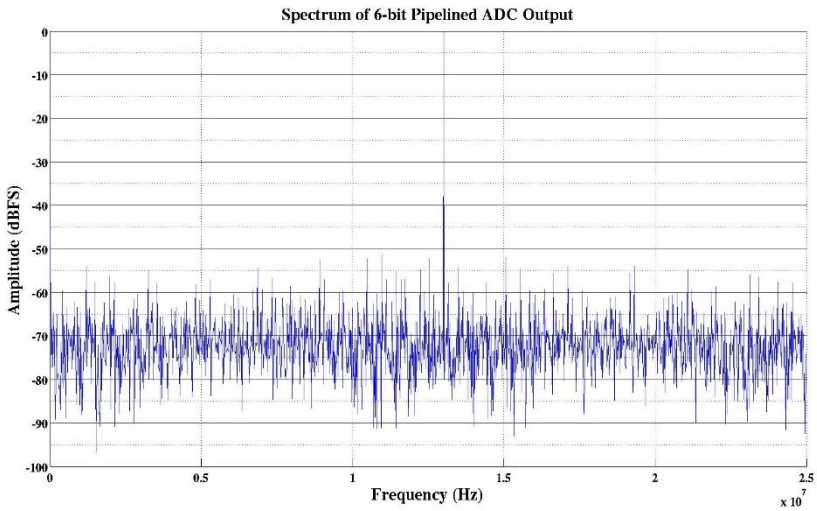

Figure 4.26 FFT Plot for input frequency of 13.01MHz

4.8.2 Transistor Level Simulation

Five stages are cascaded together with a shift register and digital correction logic to obtain a 6-bit converter to test the functionality of the pipelined ADC at a clock of 50MHz. Figure 4.27 shows the schematic arrangement for a 6-bit pipelined ADC. Two tests have been performed using Cadence Spectre transient analyses to test the working function of pipelined converter. In the first test, input is ramped from -500mV to 500mV and the digital output is converted into analog using a 6-bit DAC. The output digital codes are then compared with an analog input to test the linearity of the converter. The second test is the single tone test to simulate the dynamic performance of the pipelined converter like SNDR and SFDR.

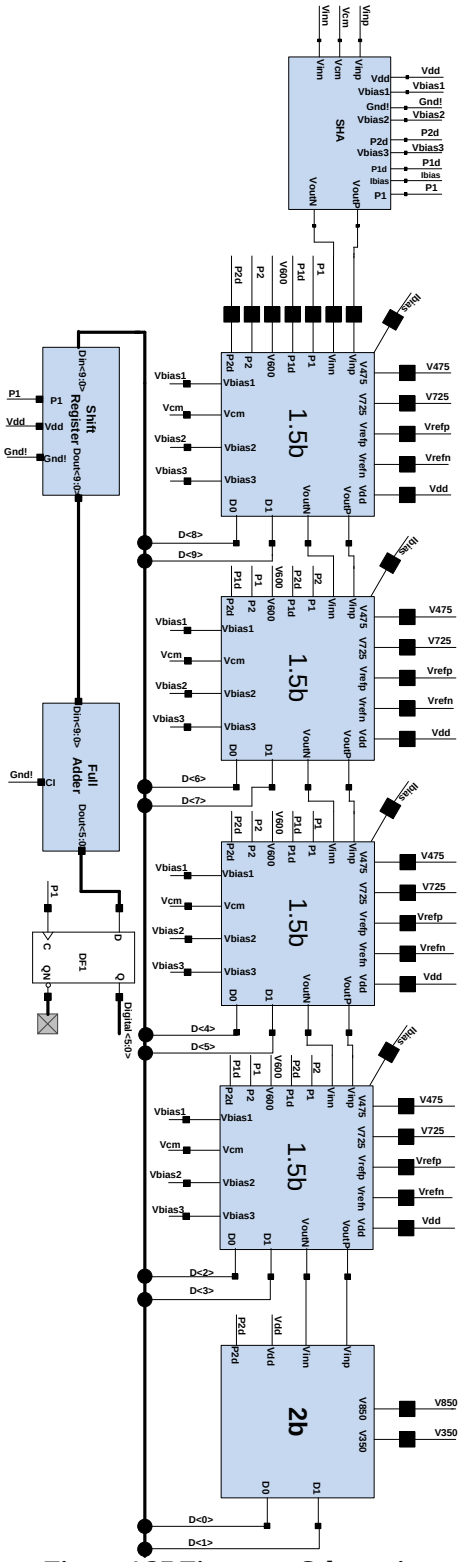

Figure 4.27 Five stage Schematic

4.8.2.1 ADC Linearity test

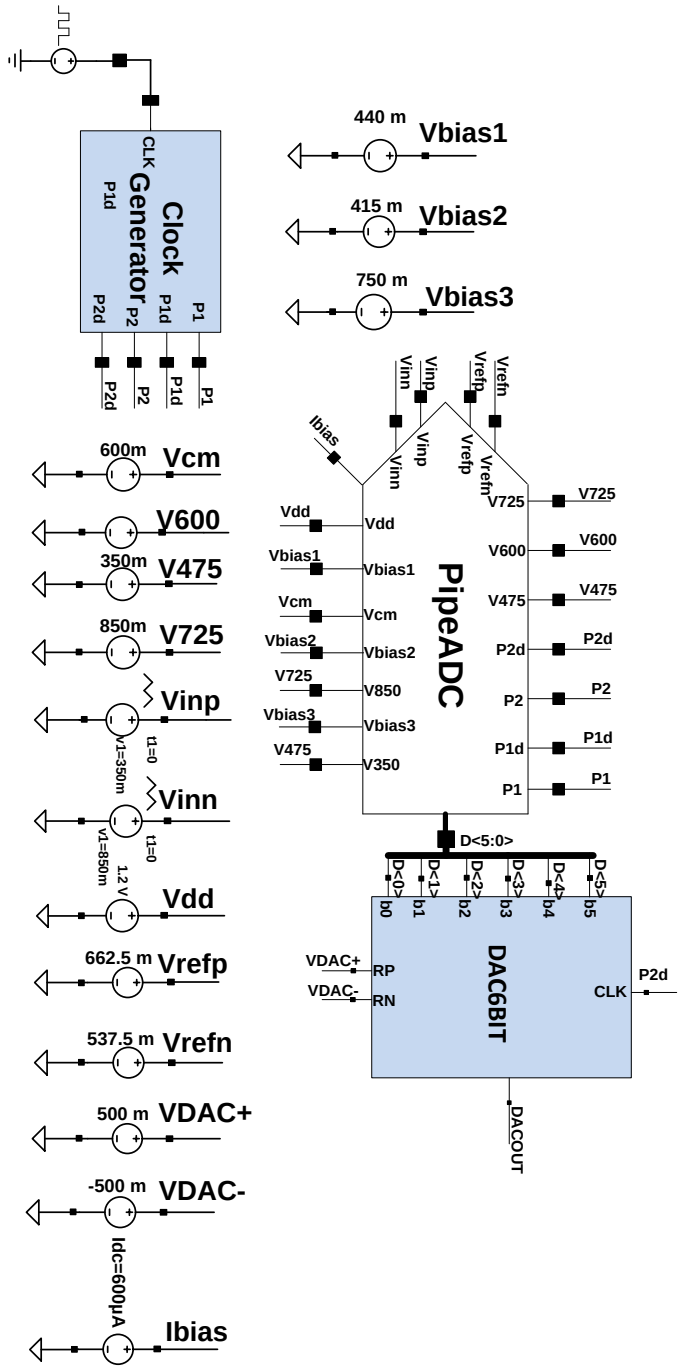

Figure 4.28 Test bench for a five stage pipelined ADC Linearity Test

Figure 4.28 shows the test bench setup for testing the linearity of the designed ADC. For the linearity test, input is ramped from -500mV to 500mV. Transient simulation has been performed with a stop time of 13us. As seen from figure 4.29 the output is staircase with 64 different output codes for 6-bit resolution. The step size in the staircase output is uniform with a step height of 1LSB, where 1LSB = 15.62mV. Conversion is linear with no missing code or glitch in the output transfer curve. The output tracks the input which is a straight line with very little deviation.

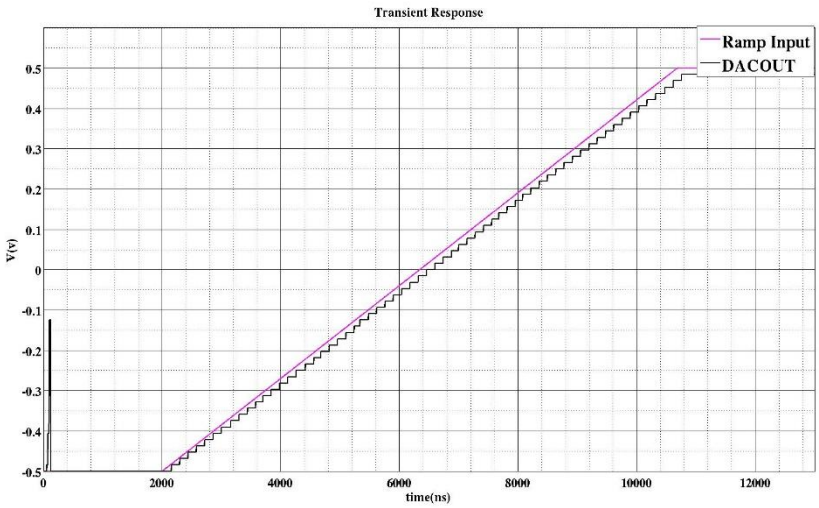

Figure 4.29 Five stage ADC Ramp test

4.8.2.2 ADC Single-tone test

A single-tone test has been performed in order to check the SNDR and SFDR of the converter. Two tests have been performed for two different input frequencies. First a sine wave input with $f_{sig} = \frac{13}{2048} * 50\text{MHz}$ has been applied at ADC input where 13 is a prime number (bin number), 2048 is number of samples collected at the output, 50MHz is the clock frequency. Second input frequency is a sine wave input with $f_{sig} = \frac{533}{2048} * 50\text{MHz}$. Figure 4.30 shows the test bench setup for the single-tone test. Two voltage controlled voltage sources are used to generate the differential input for the pipeline converter from a single vsin source. The output data is saved in a file for further processing in MATLAB. The SampleToFile block is used to save the output data samples.

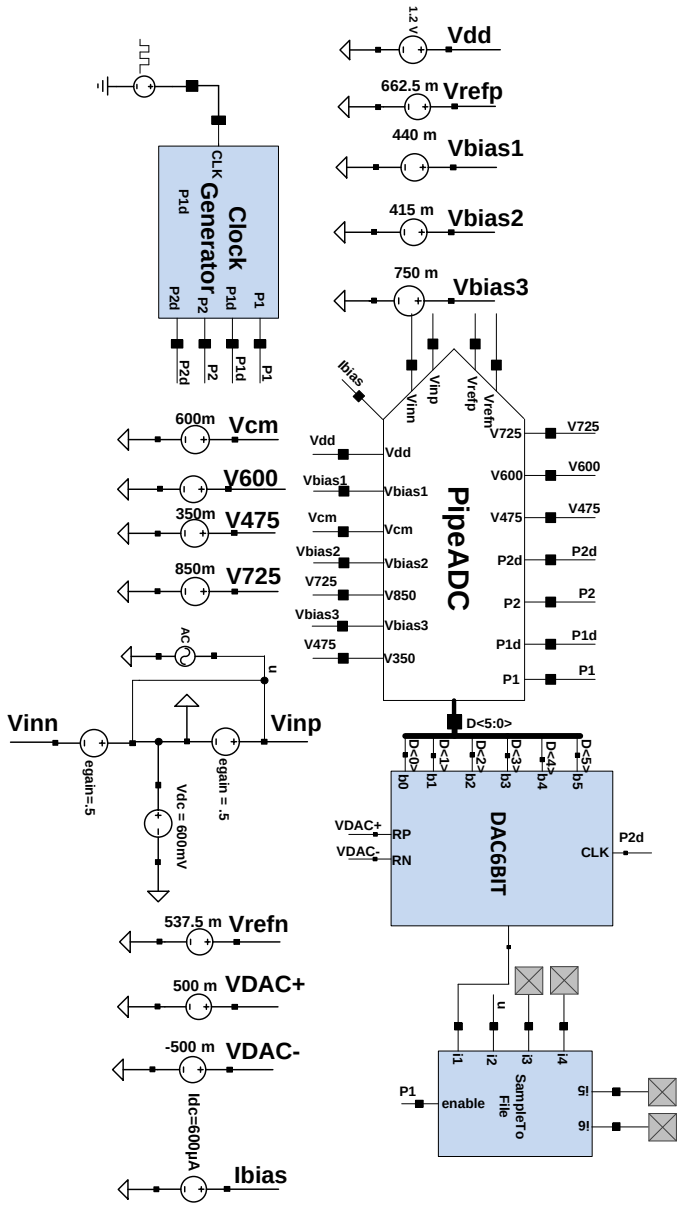

Figure 4.30 Test bench setup for a single-tone test

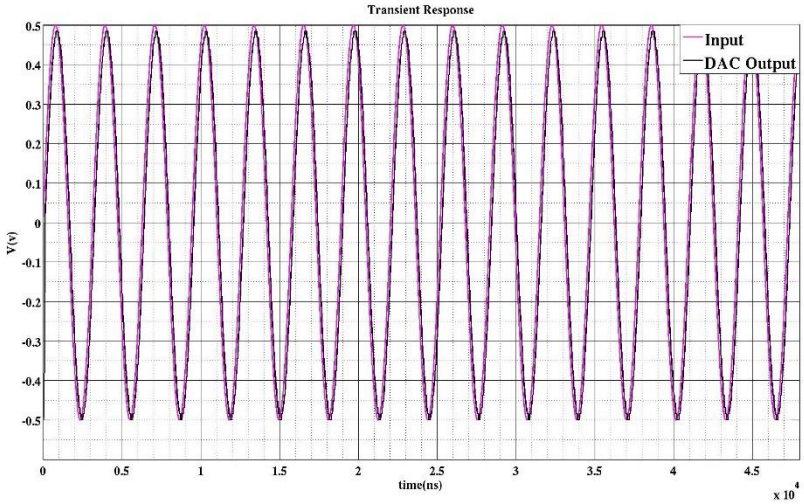

Figure 4.31 Single-tone test Transient response for input frequency of 318.38KHz

Figure 4.31 shows the ADC output after performing a single-tone test for an input frequency of 317.38KHz. A sine wave can be seen at ADC output. The output data is exported to MATLAB to measure the ADC SNDR and SFDR. Output spectrum is plotted by taking 2048-point FFT with an input frequency of 317.38KHz and 13.01MHz at 50Msample/sec sampling rate. SNDR and SFDR is calculated using two functions in MATLAB (adcfft and adcperf). Figure 4.32 shows the ADC output FFT spectrum for sine input at 317.38KHz. Simulation results shows that the proposed ADC achieves an SNDR of 37.1dB which is very close to an ideal SNDR of 37.40dB whereas the achieved SFDR is 47.47dB which is promising for a 6-bit ADC performance. Figure 4.33 shows the FFT spectrum for 13.01MHz input. Achieved SNDR and SFDR is 36.83dB and 46.73dB. The proposed ADC works well for both high and low input frequencies at a sampling rate of 50Msample/sec.

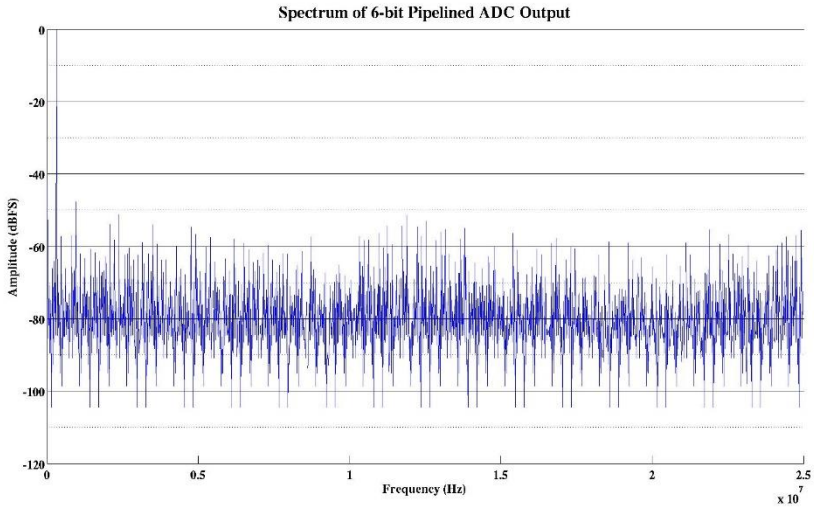

Figure 4.32 FFT Plot for input frequency of 317.38KHz

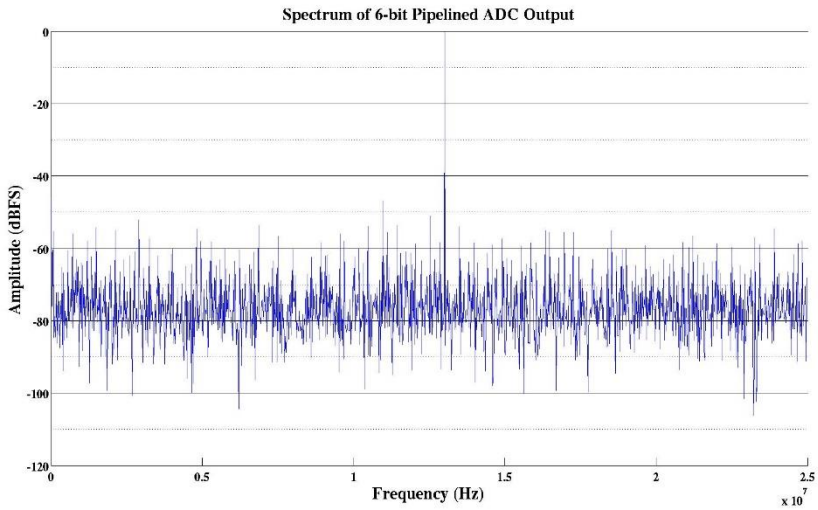

Figure 4.33 FFT Plot for input frequency of 13.01MHz

4.9 INL and DNL

INL/DNL determines the static nonlinearity of the designed ADC. Static nonlinearities tell if there is any missing code in overall ADC output. Missing code is if certain digital output codes are missing and never appear

at the ADC output. For an ADC to be linear having no missing codes INL/DNL must be within ±0.5LSB. INL is the deviation of the output transfer curve from ideal straight line whereas DNL is a measure of deviation of actual step height from ideal step value of 1LSB. INL and DNL is measured using code density testing [32]. A text file is generated from output transfer curve in Figure 4.26 and data is exported to MATLAB for calculating and plotting INL/DNL. Figure 4.34 and Figure 4.35 shows the DNL and INL plots for the designed ADC. Measured DNL is +0.15LSB and -0.27LSB. Measured INL is +0.31LSB and -0.28LSB, which is promising for a 6-bit performance.

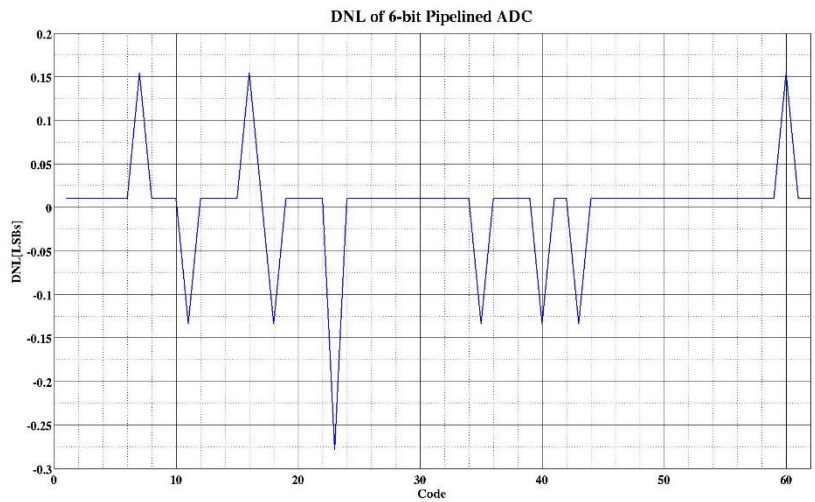

Figure 4.34 DNL Plot

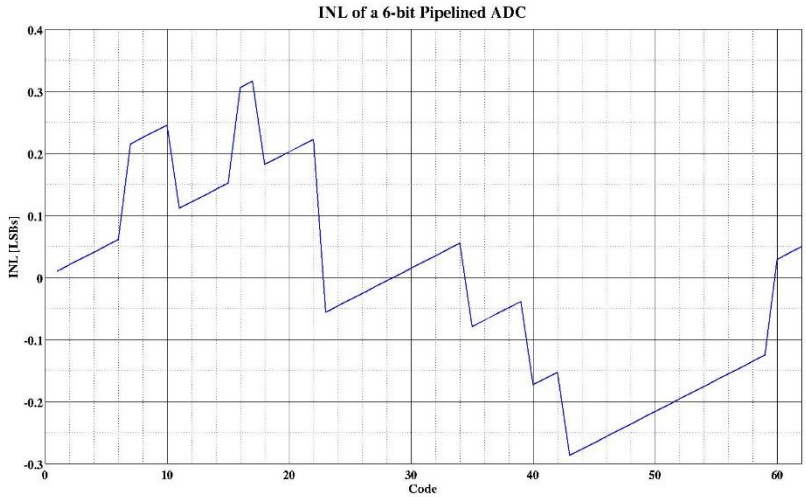

Figure 4.35 INL Plot

CHAPTER 5

5 Conclusions

The objective of this Master thesis is to design a 6-bit 5 stage high speed pipelined ADC which will operate on 1.2 V power supply. The input to the converter is -500mV to 500mV (600mV Common mode voltage) fully differential input. All the requirements of the project have been fulfilled. The converter is running well at 50MHz and consumes only 31.62mW. Designed pipelined ADC shows good linearity as it achieves an SNDR of 37.1dB, SFDR of 47.47dB and INL/DNL $\leq$ 0.5LSB. Measured SNDR is close to the theoretical SNDR of 37.88dB for a 6-bit performance and achieved SFDR is above 40dB which shows a good dynamic performance for a 6-bit ADC. Measured INL/DNL is within ±0.5 LSB with no missing codes in overall pipelined ADC output.

CHAPTER 6

6 Future works

Future work involves extending the number of stages to make it a high resolution converter. Implementation of the pipelined converter using Op-amp sharing and removal of the input sample and hold stage or through digital calibration in digital domain. Further work also involves layout of the whole design so it can be fabricated on a chip.

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List of Figures

List of Tables

List of Acronyms

ADC	Analog to Digital Converter
SHA	Sample and Hold Amplifier
DSP	Digital Signal Processing
DAC	Digital to Analog Converter
MSB	Most significant bit
LSB	Least significant bit
HDTV	High definition television
MDAC	Multiplying DAC
GBW	Gain bandwidth product
SNDR	Signal-to-noise and distortion ratio
CMFB	Common mode feedback
Op-amp	Operational amplifier
INL	Integral nonlinearity
DNL	Differential nonlinearity
SFDR	Spurious-free dynamic range