

# Low Cost Embedded Accurate 6 GHz RF Frequency Counter

LINUS HELLMAN

MASTER'S THESIS

DEPARTMENT OF ELECTRICAL AND INFORMATION TECHNOLOGY

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# Low Cost Embedded Accurate 6 GHz RF Frequency Counter

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# Abstract

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Speed, portability and quality. These are all attributes that manufacturers are striving to achieve. The demand for speed is making wireless frequencies increase with a steady pace. The demand for portability is filling the world with high speed wireless devices that are expecting their data fast and without errors. The demand for quality is met by making efficient ways of testing products before reaching the market to ensure faulty devices never reaches the consumer.

A common way of testing product is to build a fixture containing means of connecting to the different interfaces of the device and running tests on them to assure proper functionality. Since wireless products are becoming more and more popular, carrier wave frequencies and wireless output power are things in need of testing.

The scope of this thesis has been to, with easily accessible, commercial components, implement a prototype design of a low cost, accurate frequency counter capable of measuring frequencies of signals up to 6 GHz. The project includes the construction of a 4 layer printed circuit board to implement a prescaler to bring the high frequencies down to more manageable frequencies. The prescaler includes the means of attenuating strong signals and amplifying weak signals in order to ensure the capability of covering as many use cases as possible from measuring a wireless signal received from an antenna to measuring a high power signal ready to be transmitted. The divided signal is then processed by a microcontroller and the input frequency is calculated. The prototype can be supplied via a USB connection. All the specification requirements were met and this thesis provides a stable base to further develop a low cost, embedded, accurate 6 GHz RF frequency counter.



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## Acknowledgements

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I would like to thank Mats Iderup, my company supervisor and founder of Mikrodust AB, for giving me the opportunity to make my thesis work at their company. Other Mikrodust AB employees that has played a major part in this project is Martin Johansson, Rebecka Erntell and Henrik Segerbäck. Thanks for helping me when I got stuck and providing me with valuable input as the work progressed. Outside Mikrodust I would like to give thanks to my academic supervisor Markus Törmänen who was always not more than an email away and always helpful. And when the time came to evaluate my prototype at LTH, Markus arranged so that I got all equipment that I needed. In addition to these people I would like to thank my girlfriend, friends and family for always supporting me in bad times and good.

-Linus Hellman



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## Popular Science Summary

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If it can be built, you can build it. That has been a motto of mine for quite some time now. And it was this kind of thought that sprung the project leading to this thesis work at Mikrodust AB. Mikrodust has specialized in building test fixtures. Test fixtures are specially made fixtures for a specific product. The fixture connects to the product through its different interfaces and runs a series of tests on the product. This is done to assure that the product functions as it is supposed to and that nothing has gone wrong in the manufacturing of the product. These tests are done to assure that a faulty product does not reach the customer but also to get statistics about what the bottlenecks of the product design are. What is most likely to fail and what can be done to prevent it?

The rising popularity of wireless products causes the need for cost efficient, accurate and small radio test equipment that can be integrated into a test fixture. One example of test equipment commonly used to verify the radio signals frequency is the frequency counter. This is used to check if the transmitted signal frequency is within the specified limits for the protocol used. Mikrodust have previously used a commercial frequency counter to measure the output frequency of the carrier waves for different products. The goal of this thesis work was to investigate the possibility for Mikrodust to implement their own frequency counter. This to save money and to rid them from dependence of another company to make their test fixtures. The frequency counter should be able to accurately measure frequencies to up to 6 GHz. 6 GHz was a limit chosen by Mikrodust in order to include the most common frequencies used in wireless communication and still have a buffer for future protocols. Mikrodust wanted the counter to be implemented on a microcontroller that is frequently used by the company. However to be able to sample such a high frequency signal in a microcontroller the signal must first be divided down to a lower frequency. This is done in order for the slower components in the microcontroller to be able to detect the signal. The primary task in this thesis work was to find a suitable frequency divider.

After having compared a variety of solutions taking noise, power consumption and cost into consideration a suitable candidate were chosen to be used in the prototype design. When the divider was chosen began the work of implementing a design to making the circuit run. A printed circuit board was designed including features such as a programmable front-end, capable of attenuating and amplifying signals to the ideal level for the divider. The design also features a power supply



solution which allows the board to be supplied via a common USB port. The front end and divider are controlled by the microcontroller, which can set the division to anything from 32 to 1048575. The output of the prescaler circuit is a square wave with the divided frequency, which can easily be detected by the microcontroller. The microcontroller interrupts every N'th period (where N can be chosen to any positive integer) of the signal and counts the number of clock cycles between these instances. In this way an average period time of the signal can be found and with that the frequency. When the divided frequency is known the microcontroller simply multiplies with the division ratio and now the undivided frequency is known. When a working prototype was done the evaluation began. The results were good, the prototype succeed to meet all specifications. And will provide a solid base to further develop to reach the goal, a low cost, embedded, accurate, 6 GHz RF frequency counter.

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# Introduction

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Times are changing. The rapid evolution calls for more flexibility, portability and speed. Every piece of technology is expected be portable and wireless. In the same phase as personal technology is developing the phenomena known as the internet of things (IOT) have been getting a lot of attention for the last couple of years. This as well calls for small maintenance-free and wireless nodes. The rapid growth of wireless articles leads to a bigger demand for speed and bandwidth. The wireless protocol frequencies are steadily increasing in order to please this demand.

In a close future there will be a lot of wireless consumer products in manufacturing where a high volume should be thoroughly tested before being released to the quality expecting consumers. As a result, testing equipment for wireless applications are needed. A simple solution that should be able to test the necessities for a working product and the result should be acquired fast and with high precision. The testing equipment should be able to handle a wide range of frequencies for maximum flexibility. Portability and energy consumption are two other important factors in order to create a small and energy efficient testing environment for a wide variety of products. An example for such a test utility is a frequency counter. This tool gives the ability to easily check and tune carrier frequencies.



## 1.1 Project description

Mikrodust AB have for the last years made a name for themselves on the test fixture market. Through good communication with suppliers and a fast phased and thought through system they are constructing test fixtures for a variety of products. For the time being, Mikrodust are using commercial frequency counters in some of their test fixtures. This has proven to work very efficiently but is at the same time quite costly.

The task at hand is to evaluate the possibility to design a frequency counter for their own use. A small, cost efficient design that works with their current protocols. The design should be able to replace the currently used product which has a bandwidth in the range of 1-6000 MHz. This is one of the guidelines present in this project.

To successfully handle these frequencies a prescaler is needed. The scope of this project also includes evaluating suitable components and implementing a proposition for a prescaler. The prescaler system should be completed with an RF front-end and built into a suitable enclosure with shielding characteristics. The chosen implementation should be designed using the PCB design software Altium.

Frequency counting algorithms should be researched and the ones considered suitable should be used to implement a frequency counter on an EFM32 microcontroller using the prescaled signal as an input.

The resulting design should be tested with account to power consumption and accuracy.

As a summary, the scope of this master thesis consists in the following:

- Design a RF front-end rated for frequencies up to 6 GHz.
- Find a suitable prescaler taking accuracy, cost and prize into consideration.
- Design a PCB that holds the chosen RF front-end and prescaler using Altium.
- Evaluate and implement different frequency counting algorithms on an EFM32 microcontroller.

## 1.2 Report structure

The report was written in the following manner.

1. Introduction - Introduction to the project.
2. Method and theory - Covers the Method of the project and theory.
3. Project overview - Design considerations and research.
4. Prototype design - Presentation of final design.
5. Evaluation - Evaluation of implemented prototype.
6. Discussion - Discussion of evaluation and finished project.
7. Conclusion - Reflections on the project and considerations for future work.



## Method and theory

---

This chapter discusses the projects method and theory on the subject of frequency counting.

### 2.1 Method

This master thesis was conducted in the following manner. First an evaluation of available prescalers was made. When the prescaler was set, hardware blocks could be defined and implemented around this in order to make the prescaler run. The hardware blocks were as follows:

- RF front-end.
- Power supply.
- Divided output

The complete evaluation and construction of these blocks are further discussed in chapter 3.

The other part of the project was the controller side part, including the algorithm implemented in order to accurately count and present the results. Discussion and considerations from the controller side aspects can also be found in chapter 3.

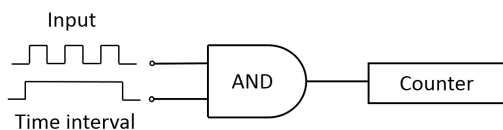
## 2.2 Frequency counting

The definition of frequency is "Rate of occurrence during a specific time". The "occurrence" in the electrical case is the repetition of a period of a signal. This can be written as.

$$f = n/t \quad (2.1)$$

Where  $f$  is the frequency and  $n$  is the amount of periods that occurred during the interval  $t$ .

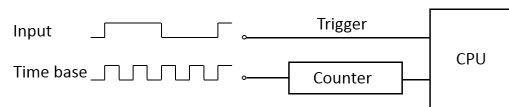
If one were to extract this data from an actual electrical signal the most intuitive way of doing this would be to simply define the interval as one second and have a counter increment every time a voltage pattern is repeated. By taking this idea and realizing it the result could look something like in figure 2.1.



**Figure 2.1:** Illustration of conventional frequency counter.

This technique was commonly used a couple of decades ago and is commonly referred to as conventional frequency counting. If a time interval of one second is used the frequency of the signal is equal to the counters value after the time interval stops being active. The downside of this technique is that the accuracy will be 1 Hz since this is the representation of the least significant bit (LSB) in the counter. A way to increase the accuracy would be to increase the time interval used. Though this would increase the accuracy of the counter the time for one single acquire would increase proportionally. Another downside to conventional counting is that the number of value numbers of the calculated frequency is directly proportional to the frequency of the signal of which one is measuring. An easy refinement of conventional counting that rids the method from the value number problem is called reciprocal counting.

Reciprocal counting counts, instead of the input pulses over a time interval, the number of time base pulses during a number of periods of the input signal. The reciprocal counter will therefore always get the same number of value numbers due to the division made to ultimately find the input signal's frequency.



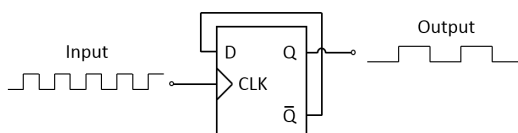
**Figure 2.2:** Illustration of reciprocal frequency counter.

Upon study of figure 2.2 which depicts a very basic illustration of a reciprocal frequency counter it's quite clear that this method needs some more processing power. The controller unit uses the input signal to trigger a new check of the counter. Based on the period time of the time base the control unit can calculate the period time of the input frequency. Using the reciprocal method of counting makes the accuracy depend on the time base clock instead of the input frequency. For reciprocal counting the insecurity is one time base pulse instead of one input pulse. For frequencies close to the time base clock's frequency, this might not be much of a difference but it will be consistent regardless of the input frequency. In the same way as in the conventional method averaging can be used to increase the accuracy. This is easily done by adding up time base periods over several trigs.

At some point in frequency logic counters won't be able to accurately detect pulses any more. This would prevent the time base clock from rising too high which demonstrates that there is a limit to how high frequencies that can be measured. For applications that require very high accuracy interpolation can be used. Basically, interpolation is used to calculate the time between an input trigger and the closest time base pulse. By doing this the accuracy is increased substantially because the accuracy is not longer controlled by the length of the time base period. This method can be done both digitally or analog. The analog way is done by charging a reactive component with a specific current during the time of interest. Then to measure this time accurately the reactive component is discharged with a fraction of the current. The time for the discharge is measured, and the measured value is proportional to the actual time with the same ratio as between the charging and the discharging current. A digital interpolator can be implemented using two time base clocks. One main clock and one accurately scaled down from this clock. The main clock is allowed to run freely but the slower clock is reset when a trigger is made on a new measurement. Because this clock is a scaled version of the main clock, the two clocks will at some point coincide. When the two clocks coincide the number of periods of the scaled clock run since the reset can be used to accurately calculate the time of interest. For more counting theory, see [2].

## 2.3 Prescaling

When dealing with frequencies in the RF spectrum special measures has to be taken. First of, traces on printed circuit boards that will carry RF signals has to be specially designed, further discussion of this can be found in section 2.4. Another issue with RF signals is that the majority of standard components aren't fast enough to keep up with such high frequencies. There could be many reasons for why one would want to lower a frequency to a more manageable one. To lower a frequency a prescaler (also referred to a frequency divider) is used. The basic functionality of a prescaler is to divide the frequency of the incoming frequency  $N$  times where  $N$  can be a fixed integer or for more advanced prescalers a programmable value. A primitive realization of a prescaler can be seen in figure 2.3. In the figure a common latch has been used to present the functionality of the circuit. The input signal is used to clock the latch which is connected with a feedback from the inverted output to the input. This causes the latch to toggle the output every other pulse and a divide-by-2 prescaler is implemented.

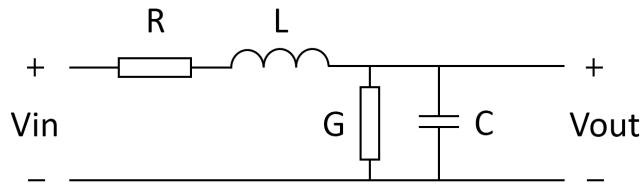


**Figure 2.3:** Illustration of a frequency divider.

To implement variations of the common flip flop divider to reach frequencies of several gigahertz finer silicon technology has to be used. This is done to lower the parasitics of the transistors of the digital blocks such as the latches. For applications such as these, bipolar transistors are often used, atleast for the ones controlled by high frequency signals, this is done because the bipolar transistors has substantially lower capacitance between the base and emitter than the gate source capacitance on a cmos transistor. This technique is used in publication [1] which describes the implementation of a prescaler rated for 6 GHz.

## 2.4 Characteristic impedance

When designing a printed circuit board (PCB) that will include board traces used to carry signals within the RF spectrum, special considerations have to be taken. Every PCB trace has what is commonly referred to as characteristic impedance. This is easiest described by illustrating a section of a transmission line to realise the components of a common PCB trace or any transmission line for that matter. A infinitesimal length of a transmission line can be described by four components distributed as seen in figure 2.4.



**Figure 2.4:** Illustration of a transmission line.

Where the  $R$  can be described as the series resistance due to the non-ideal conductive characteristics of the trace material.  $L$  represents the current and magnetic energy in the line segment.  $G$  represents non ideal insulator properties of the isolation material between the copper layers of the PCB. And where  $C$  represents the electric energy stored in the transmission line. From this assumption the formula of characteristic impedance can be described as equation 2.2, see [15] for full derivation.

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (2.2)$$

Characteristic impedance can be described as the impedance seen for a signal on every point along the transmission line. There is a possibility for the PCB designer to alter the characteristic impedance by changing the layout of the trace. By changing the material of the insulator the permittivity can be altered and thus making the impedance change. This can also be controlled by changing the thickness and width of the copper trace.

The reason that the characteristic impedance of a trace is important is that when a signal hits a discontinuity in the medium in which it propagates, part of the signal is reflected off of the discontinuity leading to a wave with less power that continues along the transmission line. The ratio of the voltage of the wave that continues forward and the voltage of the wave that is reflected is called the reflection coefficient and can be written as in equation 2.3.

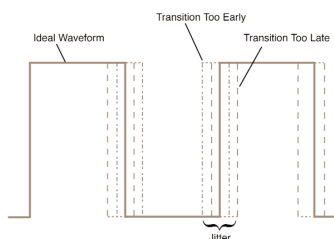
$$\Gamma_L = \frac{V_L^-}{V_L^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (2.3)$$



Where  $V_L^-$  is the voltage of the reflected wave,  $V_L^+$  is the incident voltage and  $Z_L$  is the impedance of the second propagation medium. If one examines equation 2.3 the ideal reflection coefficient for keeping the entirety of the signal power continuing to propagate into the new medium is to have the impedance of the second medium equal to the characteristic impedance of the primary medium. As mentioned before the characteristic impedance of a PCB trace can be altered but can also be calculated using various simulation techniques, making it possible to design for a wanted characteristic impedance before the circuit board is manufactured.

## 2.5 Phase noise

Phase noise is easiest described by examining a signal with a specific frequency in the time domain. If the signal is not ideal it will fail to always keep the same time period. In a random matter the time period will change ever so slightly causing pulses arriving earlier alternately later than for the ideal signal. This phenomenon is called jitter. An illustration of this can be seen in figure 2.5.



**Figure 2.5:** Time base view of a signal with jitter [16].

These deviations from the ideal behaviour of a repetitive signal shows up in a different way in when looking at the signal in the frequency domain. The slight changes in frequency adds power in the frequency in close proximity to the ideal signal frequency. When examining a jittery signal in the frequency domain the noise jitter will add a skirt to the signal peak. This appearance in the frequency domain is used to measure the phase noise. To describe phase noise one looks at the relative signal power at different frequency offsets from the ideal frequency. For an example the phase noise added to a signal by a prescaler could be -60 dBc/Hz @ 1 kHz, which would mean that the power drops 60 dB relative to the signal peak at an offset of 1 kHz from the ideal frequency. To add more information about the phase noise the relative power for several offsets can be used. To calculate the rms jitter from the phase noise information the formula in equation 2.4 can be used.

$$RMS J_{PER}|_{f_1 to f_2} = \frac{1}{2\pi f_c} \sqrt{2 \int_{f_1}^{f_2} 10^{\frac{L(f)}{10}} df} \quad (2.4)$$

Where  $f_1$  and  $f_2$  is the offset frequencies for which the information is measured between. Note that jitter behaves like white noise and can be averaged away.

## 2.6 Oscillator types

Oscillators are used in almost every electronic project. Use cases differ from just driving a microcontroller, where the frequency determines the processing speed of the controller, to producing a very accurate time base for example a GPS system. It is quite obvious that different designs are in need of different amounts of accuracy of their oscillators.

When talking about the accuracy of an oscillator one talks about the stability of the oscillator. The stability of an oscillator is referring to the oscillators ability to maintain its frequency over a period of time. The stability of an oscillator depends on a few factors. First there is the statical error of the oscillator, the inability for an oscillator to deliver the frequency it is designed for. The second error is the temperature dependence of the oscillator, the change of the frequency when the oscillator experiences a change in temperature. The last error commonly mentioned when discussing oscillators is the ageing of an oscillator. The inability of the oscillator to maintain its frequency over time.

Stability is usually measured in parts per million (ppm), which refers to the possible deviation of the frequency measured in the oscillators ideal frequency divided by a million. Say for example that a 1 MHz crystal has a stability of  $\pm 50$  ppm, this would mean that this crystals frequency could change by  $50 * \frac{1e6}{1e6} = 50$  Hz during normal use. For very stable oscillators parts per billion (ppb) might be used.

Different types of oscillators have different levels of immunity to these types of stability errors. Three of the most common oscillators are:

**Crystal oscillators** - Low cost oscillators with bad stability characteristics. These oscillators are susceptible to changes both from temperature and from ageing.

**Temperature controlled oscillators (TCXO)** - A TCXO is an oscillator more stable than a common crystal. A bit more costly but comes with built in circuitry that corrects its temperature dependence.

**Oven controlled oscillators (OCXO)** - An OCXO is the most stable of the three and by far the most expensive. An OCXO eliminates almost all temperature dependence by heating the oscillator with a built in oven, and in this way keeps the oscillator at a constant temperature.



## Project overview

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### 3.1 Specification

The specifications for this thesis were set by Mikrodust AB. The specifications were set so that the frequency counter could without excessive work replace the current solution for counting frequency. The goals were set high to test the limits of what can be produced in this short time frame using low cost components. The specifications can be described by three categories seen below.

**Frequency rating** - The resulting frequency counter shall be able to accurately detect and calculate frequencies up to 6 GHz.

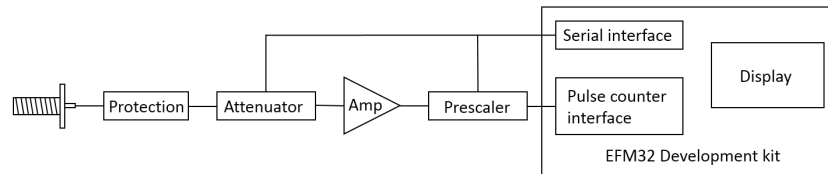
**Accuracy** - The calculated frequency shall not differ more from the input than  $\pm 500$  Hz over the whole bandwidth.

**Power consumption** - The resulting frequency counter should not draw currents exceeding 500 mA at 5 V. This is the power a high power USB device is allowed to draw.

**Cost** - The cost of the finished frequency counter should be profitably lower than the price of the current frequency counter that is about 5000 SEK.

## 3.2 Hardware design

The outline of the hardware in this project was roughly shaped as early as in the specification of this project. The thesis specification described that a prescaler would be used and that the counting and calculation should be handled by a Silicon labs EFM32 micro processor. Starting with this a few more building blocks needed to be introduced before the frequency counter would work. An overview of the system hardware can be seen in figure 3.1.



**Figure 3.1:** Illustration of the proposed system design.

If the signal path is followed starting by the leftmost component, an SMA connector used to input the signal of interest is shown. Next is a protection circuit to avoid damaging the attenuators with electrostatic discharges (ESD) voltages. Next is the adjustable attenuator, and the RF-amplifier. These three components (Protection, Attenuator and Amplifier) will from here on be referred to as the RF front-end. After the RF front-end the prescaler is located. This part of the hardware system will be enclosed in a RF tight box to avoid leakage of the RF signals. The prescaled signal then goes into the microcontroller. The microcontroller is located on a development board that features a display that will be used to display the result. The microcontroller will also be used to control the attenuator and the prescaler using serial communication.

### 3.2.1 Microcontroller

The microcontroller used in this thesis work was the Silicon labs EFM32 Giant Gecko. The usage of this specific microcontroller was set in the thesis specification by Mikrodust AB since this is a microcontroller series that has been used by the company before. The Giant Gecko is just one of many in a large family of low power, 32-bit microcontrollers in the EFM32 series. The Giant Gecko is one of the more powerful controllers in this family and shouldn't have any problems completing the task at hand. A summary of the Giant Geckos specifications can be found in table 3.1.

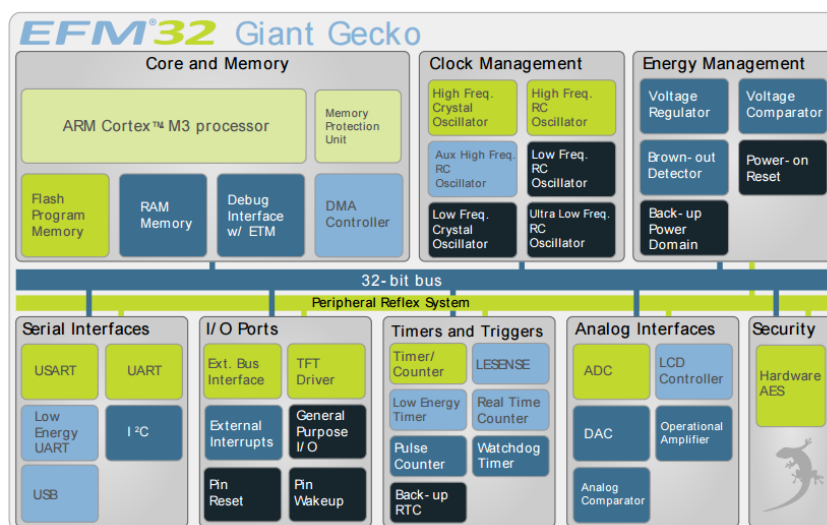
Processor	ARM Cortex-M3
Clock speed	48 MHz
RAM	128 kB
Flash memory	1024 kB
Timers (16-bits)	4

**Table 3.1:** Specifications for the Silicon labs EFM32 Giant Gecko microcontroller [4].

All work with the Giant Gecko was conducted on an evaluation board made by Silicon labs called the Giant gecko starter kit EFM32GG-STK3700. This features multiple power supply possibilities, a debug interface, several pin headers to easily reach the many general purpose input output (GPIO) ports. The evaluation board also features an lcd segment display capable of displaying both characters and numbers. The specification of the evaluation board can be found in table 3.2.

Supply voltage	1,98 - 3,8 V
Deep Sleep current	1.1 $\mu$ A @ 3 V
Current consumption	219 $\mu$ A/MHz @ 3 V
General purpose I/O pins	86
LCD display	8 x 34 segments

**Table 3.2:** Specifications for the Silicon labs EFM32 Giant Gecko evaluation board reference [4].



**Figure 3.2:** Overview of the hardware blocks of the EFM32 Giant Gecko [3].

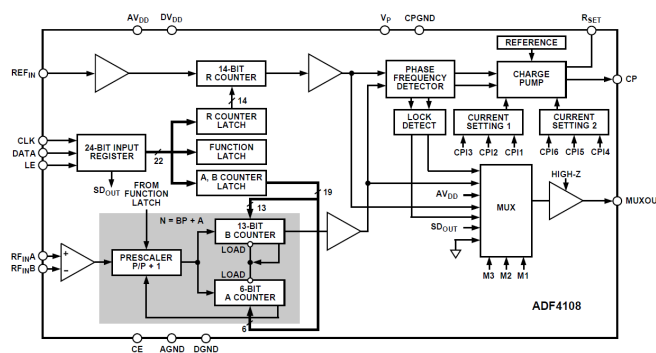
A rough image of the features and specifications of the microcontroller setup can be found in the tables 3.1, 3.2 and in figure 3.2. A short summary of the important features that was used in the design and implementation of the frequency counter will follow. The first interface that is mentioned is the pulse counter interface. The Giant Gecko features four separate pulse counters that are able to operate asynchronously. One of which has a sixteen bits register and three that all have eight bit registers. The pulse counter interface is basically a counter that have the feature to be incremented by an external signal connected to one of the GPIO pins. With the right configuration this interface is able to generate interrupts after a specific number of pulses has been encountered. The pulses must be seen as a logic high so the output from the prescaler must be modified to fulfil the needs of the pulse counters external clock signal. The external clock signal of the pulse counter is rated as high as the Giant gecko's core clock is rated, up to 48 MHz. Which doubles the bandwidth compared to using a regular GPIO pin to detect a pulse, which needs two samples to detect a change in voltage. This makes the pulse counter interface highly valuable for this project, the specific way of usage is discussed further in section 3.7. Another important feature is the timers. These are used to count the time base oscillator. One timer feature that should be specifically mentioned is the cascade capability. This feature allows the 16 bit timers to overflow into another timer thus making these two 16 bit timers work as a 32 bit timer. The last mention about the EFM32 hardware is the lcd segment display, excellent for debugging and showing the frequency output or the attenuation of the RF front-end.

### 3.3 Prescaler

The prescaler was the first priority in the project and great proportions of the design depended on what prescaler was chosen. The first proportion of the thesis work was to research what was currently available on the market that could fulfil the specifications of the frequency counter project. Using the search engines at the main distributor and manufacturers websites a handful of alternatives were presented. The main reason why the majority of prescalers couldn't be used was that their bandwidth was too narrow. A great proportion of the prescalers that can handle frequencies above 3 GHz had a lower frequency limit higher than tolerable for the project. The lowest radio frequency of interest to Mikrodust AB was specified as 433 MHz. This is a common frequency used for short range wireless devices. After some time of searching four alternatives were discovered. These will now be presented in greater detail.

#### 3.3.1 ADF4108 PLL Frequency Synthesizer

This phase locked loop (PLL) frequency synthesizer features a programmable dual-modulus prescaler with a maximum division of 64 or 65. This combined with two programmable counters of 13 bits and 6 bits which yields a total maximum frequency division of 16447 times. The synthesizer features a multiplexer making it possible to output just the divided signal which would be the use case in this project. The input bandwidth of this circuit is rated in the span of 1 - 8 GHz which may seem a little high judging by the lowest frequency of interest at 433 MHz, but the data sheet clearly states that the chip will be able to handle lower frequencies if a certain slew rates are achieved. The previous rating is not ideal for this project but it was still considered for the final design. The circuit could be supplied with a voltage of 3,2 to 3,6 V and draws a maximum current of 17 mA. The input circuitry is rated for signals with a power between -5 dBm and +5 dBm. The phase noise of the ADF4108 drops to -81 dBc/Hz at an offset of 1 kHz.

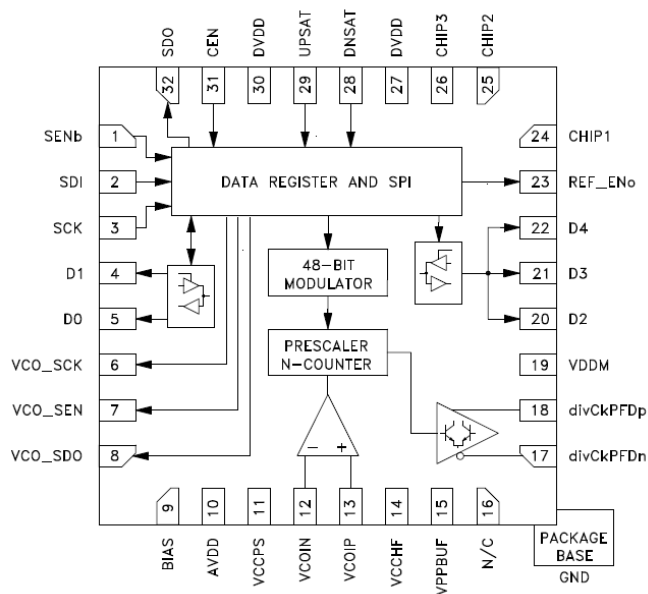


**Figure 3.3:** Block schematic of the ADF4108 PLL frequency synthesizer [5]



### 3.3.2 HMC983LP5E DC - 7 GHz FRACTIONAL-N DIVIDER AND FREQUENCY SWEEPER

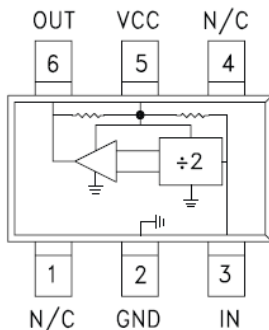
The HMC983LP5E is a frequency synthesiser and is a product of Hittite Microwave Corporation that was bought by Analog Devices in 2014. The HMC983LP5E has besides a 20 bit programmable frequency divider also an integrated frequency sweeper that could be an excellent tool for testing. The frequency division is set by a register of 20 bits and can operate in both integer mode and in fractional mode using a integrated 48 bit delta sigma modulator. The 20 bit control register gives a division capacity of 32-1048575 for integer division and 36-1048571 for fractional division. The capability of such high division gives a great deal of flexibility both for later tuning of the prescaler and for testing the output result for different division sizes. The HMC983LP5E features by far the best noise statistics of the four alternatives. For an input of 6 GHz the phase noise drops to about -140 dBc/Hz at 1 kHz offset in integer division mode. The phase noise characteristics in fractional division mode is a bit higher than in integer mode but it still manages to drop the noise to about -130 dBc/Hz at the 1 kHz offset for a 6 GHz input signal. The circuit needs both a +5 V and a +3 V power supply which complicates usage slightly. The current consumption for normal use in integer mode is about 104 mA. The input stage is rated for signals with a power of between -15 dBm and 0 dBm but achieves the best spectral performance with an input with a power of -10 dBm.



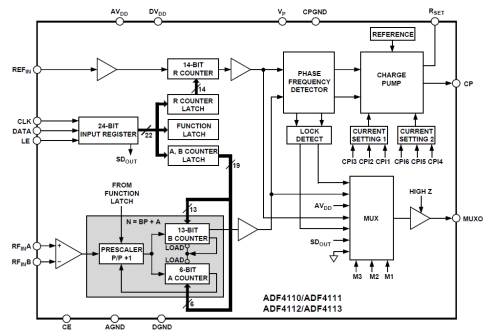
**Figure 3.4:** Block schematic of the HMC983LP5E DC - 7 GHz FRACTIONAL-N DIVIDER AND FREQUENCY SWEEPER [6].

### 3.3.3 HMC432 DIVIDE-BY-2 + ADF4112 RF PLL Frequency Synthesizer

Before RF circuitry broke the boundary of 3 GHz this was the standard bandwidth of most RF circuitry. This alternative takes use of the wide variety of circuits capable of handling 3 GHz by using a fixed divide by 2 circuit from Analog Devices called HMC432. This divider is powered by a 3 V supply and draws a maximum current of 56 mA. It has a wide input range between -12 dBm and +12 dBm up to 7 GHz but can reach all the way up to 8 GHz if the signal power is between -4 dBm and +10 dBm. The minimum input frequency for a sine wave is 200 MHz that is well in reach for the specifications. The phase noise of the circuit drops to -140 dBc/Hz at 1 kHz offset. After this circuit the maximum frequency is limited to 3 GHz which opens up more possibilities, one of which is the Analog Devices ADF4112 RF PLL Frequency Synthesizer. This frequency synthesizer bares a resemblance of the ADF4108 discussed in section 3.3.1 but has a bandwidth of 3 GHz instead of 8 GHz. The lower frequency limit of this circuit is 200 MHz which makes it 400 MHz for the whole solution with the frequency division by two on the first circuit. The ADF4112 have very similar specifications as the ADF4108, it can be supplied with anything from 2,7 V up to 5,6 V. The input power rating lies between -10 dBm and 0 dBm and the HMC432 delivers a output power with a typical value of -3 dBm. The circuit has a maximum current consumption of 7,5 mA when driven by a voltage of 3 V. The phase noise with a carrier of 1750 MHz drops to -70 dBc/Hz at an offset of 1 kHz. Note that the phase noises of these two circuits will accumulate.



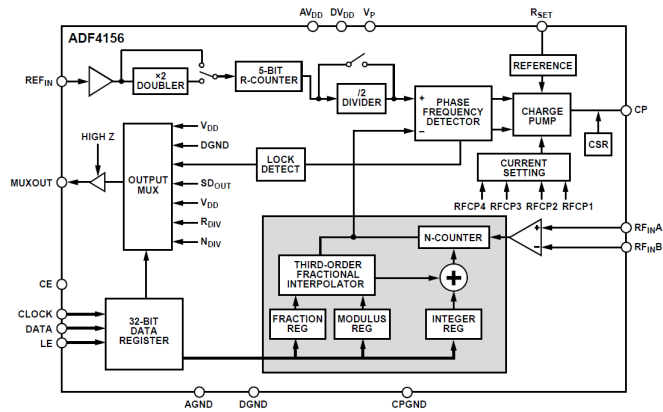
**Figure 3.5:** Block schematic of the HMC432 [7].



**Figure 3.6:** Block schematic of the ADF4112 [8].

### 3.3.4 ADF4156 6.2 GHz Fractional-N Frequency Synthesizer

The ADF4156 is as many of the other alternatives a frequency synthesizer. The circuit is manufactured by Analog Devices and features an input bandwidth from 500 MHz to 6200 MHz but can reach lower frequencies if the signal meets certain requirements. The input stage is rated for signal of a maximum voltage level of the analog supply voltage which can be set to a minimum of 2,7 V and maximum 3,3 V over 50  $\Omega$ . This corresponds to 23,4 dBm maximum input signal for a supply voltage of 3,3 V. The circuit draws a maximum of 32 mA during operation. The phase noise characteristics on the output for an input signal of 6 GHz drops to -85 dBc/Hz at an offset of 1 kHz, the phase noise curve shows a couple of spurious noise peaks that reaches upwards -60 dBc/Hz.



**Figure 3.7:** Block schematic of the ADF4156 6,2 GHz Fractional-N Frequency Synthesizer [9].

### 3.3.5 Prescaler decision and discussion

When the prescaler candidates had been settled on the work on deciding which of these would be used in the first prototype design of the frequency counter began. It would have been preferable to run tests on all of these but time and cost prevented the project to include a prototype PCB that fitted all of these circuits. To compare the specifications of all the candidates information of importance have been collected and displayed in table 3.3.

Alternative	1	2	3	4
Circuit	ADF4108	HMC983LP5E	HMC432+ADF4112	ADF4156
Bandwidth	1000-8000 MHz	0-7000 MHz	200-6000 MHz	500 - 6200 MHz
Input ratings	-5/+5dBm	-15/0dBm	-12/+12dBm	-10/0dBm
Phase noise	-81 dBc/Hz @ 1 kHz	-140 dBc/Hz @ 1 kHz	-70 dBc/Hz @ 1 kHz	-85 dBc/Hz @ 1 kHz

**Table 3.3:** Collected interesting specifications of the prescalers of interest.

When comparing the prescalers there is one immediate concern. The bandwidths of alternative 1 and 4 are not guaranteed to handle the lowest frequency of interest in this project, they are not certain to not, but they are not certain to do either. Alternative 2 and 3 are rated to handle all frequencies of interest. Alternative 3 has a higher input tolerance, but since an RF front-end will be used to regulate the input power this feature isn't of that much value. The price of alternative 2 and 3 doesn't differ substantial but the noise figure and complexity makes alternative 2 the strongest candidate of the two circuits. The prescaler considered most suited for this project and the prescaler chosen for further investigation was alternative 2, HMC983LP5E DC - 7 GHz FRACTIONAL-N DIVIDER AND FREQUENCY SWEEPER.

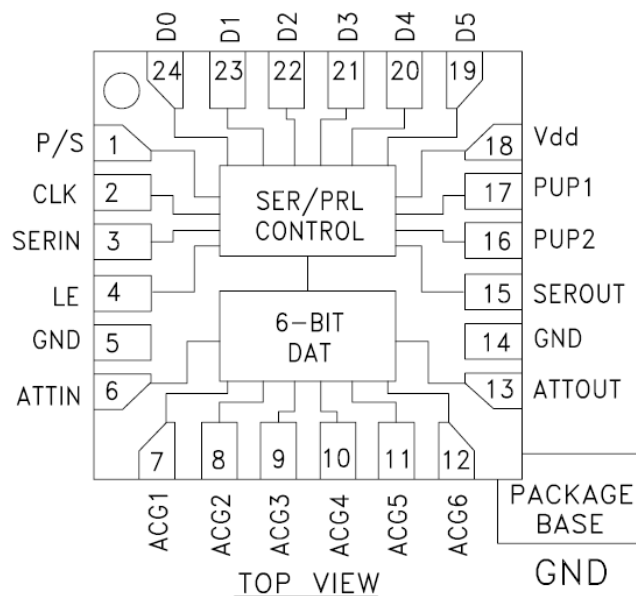
### 3.4 RF front-end

The RF front-end main purpose is to increase the range of the input signal power and at the same time maintain the ideal input power of the prescaler. By connecting an attenuator with controllable attenuation in series with an amplifier the power level at the amplifier output can be accurately controlled. Depending on the input power level the power level at the prescaler can be set to achieve the ideal operation of the prescaler. A controllable front-end is viable in order to assure the ability to test a large variety of signals. Amplification is needed for measuring wireless signals that will occur if for example an assembled product is tested and test points on the antenna or on the transmitter cant be directly connected. Then it is necessary to mount an external antenna and measure the signal from the outside. Attenuation is needed when a conductive measurement is done and the device is operating with maximum output power. This can cause the signal power level to be very high and then attenuation is needed to not damage the input stage of the prescaler. To build a properly working front-end for this frequency counter an attenuator working for the whole frequency bandwidth needs to be found. The attenuator also needs to be simple to program and needs to have a high enough max attenuation to be able to bring large signals down to the optimal input signal power for the prescaler. The second part needed is a fixed gain amplifier. This too with a frequency rating that covers the whole bandwidth and which can handle a the power levels outputted by the attenuator. Neither of these components were seen as the most vital parts of this thesis work and thus the first components that were found suitable and fulfilled all specifications were chosen. But not without regard to power consumption and cost. The components chosen are presented below.

#### 3.4.1 Attenuator

There are a lot of attenuators on the market that would fit this projects specifications since attenuators haven't got the high switching speed demands and other features that gets complicated when the frequency rises there is many attenuators on the market that reaches well over 6 GHz. For this project a programmable attenuator with a high maximum attenuation with a step size of about 1 dB to

accurately be able to set the power level at the prescaler input. The attenuator will also have to have a reasonable price and cannot draw excessive power. The best candidate found for the attenuator was an Analog/Hittite product called HMC624ALP4E and is a 6 bit, 0,5 dB LSB, DC to 6 GHz digital attenuator. Supply voltages from +3 V to +5 V are valid which corresponds well to the prescaler's ratings which means that this circuit won't need any additional voltage regulators to run. The HMC624ALP4E has a maximum attenuation of 31,5 dB. The attenuation level is easily set by either a parallel interface where 6 GPIO pins are a direct representation of the 6 bit attenuation control register. The circuit also features a serial interface that is easily switched to by changing the voltage on the parallel / serial (P/S) pin. The serial interface is TTL/CMOS compatible and is rated up to an input level of the supply voltage +1 V which makes it directly compatible with the EFM32 development kit board which runs on +3,3 V. The serial interface is controlled by a clock signal, a data signal and a latch enable (LE) signal. The implemented driver to run this along with the timing diagram is further discussed in section 3.7. The power consumption when driven on a supply voltage of +3 V is typically 2,4 mA. The input stage is rated for signals with a maximum power of +28 dBm and since this is the first component in the RF path this will set the maximum RF input power level of the frequency counter. Note that the lowest possible attenuation when of the signal passing the attenuator is not 0 dB it is the insertion loss of the attenuator, which for this circuit is typically 2,3 dB for 6 GHz. To increase the span two HMC624ALP4E were put in series, this increased the minimum attenuation due to more insertion loss but the gain in maximum attenuation were of more importance.



**Figure 3.8:** Block schematic of the HMC624ALP4E attenuator [10]

### 3.4.2 Amplifier

The amplifier sought was a fixed gain amplifier that were specified for the whole bandwidth of the project without significant changes in amplification. The ideal amplification would be around half the maximum attenuation which would lead to an equal span of amplification and attenuation. The best amplifier found for the job was the Analog Devices ADL5545, RF/IF Gain Block. This amplifier features a very wide band of operation from 30 MHz to 6 GHz which covers the project bandwidth of 500 MHz to 6 GHz. The maximum gain of the amplifier is present at the frequency of just 140 MHz where it is around 24,8 dB. Then as frequency increases the gain drops gradually. At 3,5 GHz it has dropped to around 20 dB and at 5,8 GHz the gain is about 16 dB. With this behaviour the attenuation may have to be tuned depending on the frequency that is measured. This is not regarded a problem since the frequency that is intended to be measured is generally known in a test case. An example could be that a carrier wave for a radio transmitter should be measured, if the measured frequency is not inside a specific interval then the device under test (DUT) will be marked as faulty. The point of this example is that the specific frequency interval for which the DUT passes the test is known and can be used to tune the front-end for the best performance. The circuit is supplied with a single +5 V supply and draws a maximum of 70 mA in operation. The ADL5545 is enclosed in to a SOT-89 package which is a common package for RF amplifiers. This is a benefit if there is a problem with the amplifier and another alternative is to be tested.

### 3.4.3 Protection

The scope of this project consisted in implementing a proof of concept of a RF frequency counter and report the problems that had to be overcome in this process. Since this prototype will mainly be used in a lab environment to confirm the functionality of the circuit and measure what accuracy that could be archived with this configuration protective circuitry was not prioritised. If this configuration should be proven capable to be used in a test fixture in the near future, Mikrodust AB had the request to design the printed circuit board (PCB) with pads to be used to fit electro static discharge (ESD) protection. The RF input first reaches an attenuator, the HMC624ALP4E has an ESD sensitivity graded class 1A which classify it up withstand voltage spikes up to 250-500 V. Since the signal passing this protective circuit will measure up to 6 GHz in frequency a very low series capacitance is needed to not alter the signal characteristics. A candidate for this application is the LITTELFUSE PGB1010402KR. A small transient voltage suppression (TVS) diode with a capacitance of only 0,04 pF. This diode will improve the RF input ESD ratings to upwards 8 kV from contact discharge and will service fine in the prototype design.

### 3.5 Power supply

The components chosen for implementing the design so far requires +3 V and +5 V supply voltage to function properly, this is not a complicated task to implement but there were one thing to watch out for. The +3 V supply is easily implemented using a low noise low drop out voltage regulator (LDO), more on this below. For the +5 V supply on the other hand there is a problem. When the frequency counter is mounted in a test fixture and used out in a factory. The power supply will come from a universal serial bus (USB) interface.

The USB standard is implemented in such a way that when a device is connected to a host the host registers the device as either a low power or a high power device. A host delivers a maximum of 100 mA of current to a low power device. If the device upon connection tells the host that it's a high power device the current limit is increased to 500 mA. The whole prescaler chip will draw about 200 mA worth of current so it will have to register as a high power device to work, this can be done by the microcontroller. Although the specification on the voltage level outputted by the host is for a high power device between 4,75 V and 5,25 V. This is right on the lower edge of what the amplifier is rated for and another concerning part is that the voltage level can change sporadically between these voltage levels. From an RF point of view this is not ideal and measures have to be taken to avoid these voltages to directly supply the delicate RF components. The statistics of USB was gotten from [11].

After consulting a local distributor of Texas Instruments about the problem the advice given was to first use a boost converter to raise the voltage level of the incoming +5 V USB supply to about +5,3 V. After this is done the +5,3 V should be downwards regulated by a low noise LDO to always maintain a constant voltage level with low noise. The component used to achieve this was also recommended by the local distributor for Texas Instrument and were as follows. The LDO choosen for the +3 V regulation was the Texas Intrument LP5907. This circuit features a fixed output voltage and can operate with an input voltage from +2,2 V to +5,5 V which can supply a maximum of 250 mA which is sufficient for the +3V supply. Specifications for the LP5907 was collected from [12]. The boost converter chosen was the TPS6107 also a Texas Instrument product. This circuit has the ability to be tuned externally by a resistor bridge to output the voltage needed. The output can be set to a maximum of +5,5 V and can deliver a maximum of 150 mA worth of current. This is enough to drive the TPS731 LDO to bring the voltage back to +5 V. This circuit can also output 150 mA of current wich will be sufficient to drive the RF amplifier and the +5 V supplies on the prescaler. Specifications of the circuits collected from [13] and [14].

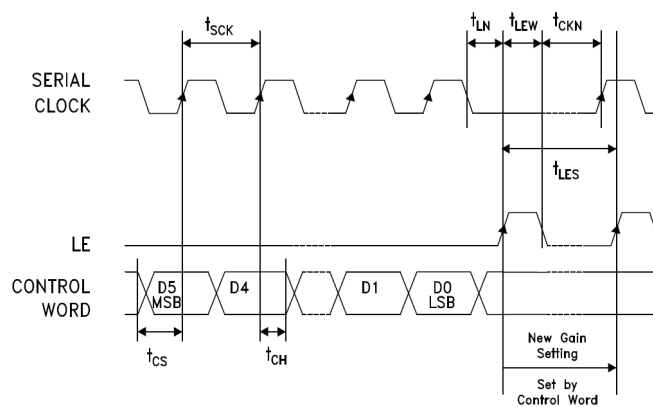
## 3.6 PCB design

## 3.7 Software design

This section consist in two subsections which discusses the two major components on which the code implements. The first section will discuss the communication with the attenuators and the prescaler. The second part discusses the theory of the implementation of the frequency counter.

### 3.7.1 Communication

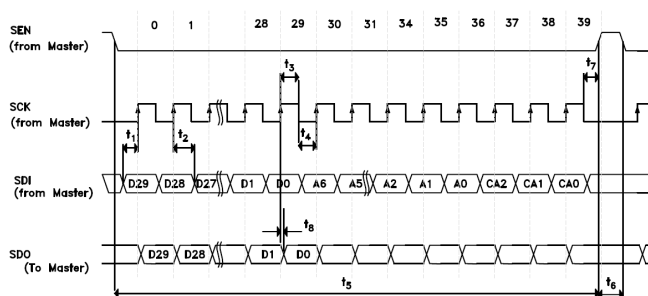
Both the attenuators and the prescaler uses a variant of a standard serial communication protocol. The attenuators uses a clock signal, a data signal and a latch enable (LE) signal. The prescaler uses a similar approach but instead of a LE signal a send enable (SEN) signal is used. The LE and the SEN signals are used to "activate" the components serial interfaces.



**Figure 3.9:** Serial interface timing diagram for the HMC624ALP4E attenuator [10]

As seen in figure 3.9 the LE signal is pulsed half a clock period after the 6 bit control word is fully transmitted. The attenuator registers all data transmitted to it but doesn't set the attenuation register until the LE signal is activated. A similar function is present in the prescaler circuit. As seen in figure 3.10 the SEN signal has to be activated (active low) in order for the prescaler to register the incoming serial data.





**Figure 3.10:** Serial interface timing diagram for the HMC983LP5E prescaler [6]

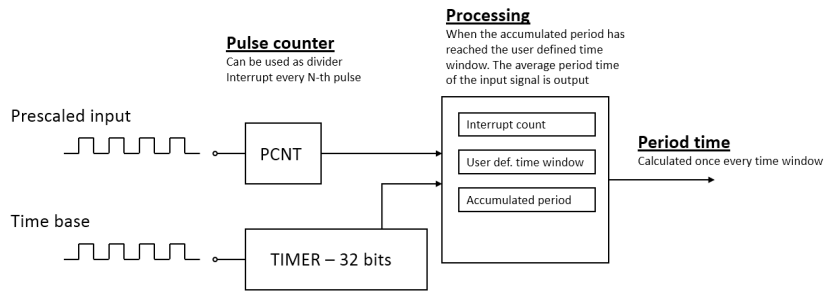
The way that these serial interfaces are implemented with a signal used to activate the receiver on the circuit makes it possible to connect all clock signals and data signals in parallel and thus saving four inputs through the filtered DSUB connector used to connect the signals through the RF enclosure. To implement the serial interface on the microcontroller a simple bit banging sequence were written using the GPIO pins. No level shifter were used to transform the +3,3 V logic levels from the EFM32 to the attenuators' and prescaler's +3 V voltage levels because both the attenuators and the prescaler are rated to handle those voltages on their serial interface pins.

### 3.7.2 Frequency counter

A few different tactics were used when implementing the frequency counter. To get familiar with the platform a conventional counter was implemented. After testing this however and after examining the theories of frequency counting it became quite obvious that reciprocal counting was the method to choose. The division of the high frequency signal would later have to be multiplied with the divisor to find the frequency of the original signal as intended. This means that if there should be an error in the calculated divided frequency this error will increase proportionally. This means that the accuracy of the counter is somewhat controlled by the size of the division in the prescaler. If the maximum input frequency of the pulse counter interface is used the division would have to be  $\frac{6e9}{48e6} = 125$  giving the lowest acceptable accuracy to 4 Hz in order to reach the goal of a having a total error of less than 500 Hz over the whole bandwidth.

The implementation of the frequency counter takes use of the EFM32 pulse counter interface first discussed in section 3.2.1. This interface has the ability to use an external clock signal to clock a counter and has a maximum input frequency equal to the maximum clock frequency of the microcontroller which in the case of the Giant Gecko is 48 MHz. The counter of the pulse counter interface has a programmable top value. This in cooperation with an overflow interrupt is used as a software divider in order to be able to tune for the optimal functionality. The software divider came to be important in order for the microcontoller to have time to properly execute the correct overflow interrupt routine. The final

implementation of the frequency counter can be seen as a block schematic in figure 3.11.



**Figure 3.11:** Illustration of the functionality of the reciprocal frequency counter algorithm.

The signal of interest is input into the PCNT (pulse counter) which outputs overflow interrupts upon reaching a specific amount of pulses. These interrupts triggers the processing block which in cooperation with the timer keeps track of how long the measurement should go on. When the accumulated time since the first interrupt reaches the specified time window the measurement is terminated and the average period time is calculated. This configuration has a lot of tunable parameters which makes it possible to examine the impact of different changes made on different parameters.

When the prototype implementation was fully done it was discovered that the RF filtered connection connecting the prescaler output to the microcontroller through the casing distorts signals exceeding 3 MHz. This will be the maximum output of the prescaler in the prototype design but there is ways to improve this in following designs.

A major part in achieving the accuracy needed of the frequency counter is an exact time base. The first implementation was made using the crystal oscillator which was already mounted on the development board. This was a 48 MHz crystal with a stability of  $\pm 50$  ppm. When running the design using this time base the counter implementation was close to managing to output a frequency within the specification but sometimes outputted an error exceeding the limitations. When examining the theoretical worst case error of the  $\pm 50$  ppm clock for a 3 MHz input signal the error will be closer to 30 kHz for 6 GHz. To achieve a worst case within the specifications the stability of the oscillator would have to be around 80 ppb. Although since  $\pm 50$  ppm were close to completing the task and since a 40 MHz,  $\pm 2,5$  ppm TCXO that was available from a previous project at Mikrodist, the TCXO was patched onto the evaluation kit. The stability of the TCXO can be seen in figure 3.12, note that the oscillator had been both resoldered more than twice. The theoretical worst case with this oscillator was calculated to be about 18 kHz at 6 GHz but in practice the measurements were far better. After some testing and tuning the design seemed to fulfil the specifications now with a reciprocal counting algorithm, a software divider at 200 and a time window at 4 s. The 40 MHz  $\pm 2,5$  ppm TCXO was chosen to be included in the final prototype design. See the final results in chapter 5.

Frequency Stability	Vs. Temperature ( - 30 ~ + 85 °C )	$\pm 0.5 / \pm 2.0$ ppm
	Vs. Load ( Load varies $\pm 10$ % )	$\pm 0.2$ ppm Max.
	Vs. Supply Voltage ( Vcc = Typical $\pm 0.1$ V )	$\pm 0.2$ ppm Max.
Frequency Tolerance	at 25 °C after 2 Reflows with Typical Applied to Auto Frequency Control Pin	$\pm 2.5$ ppm Max.

**Figure 3.12:** Table of the stability of the used TCXO [17].

## Prototype design

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This chapter will present the finished prototype design and all of its features. The different sections through out this chapter are containing the different sections of the PCB design along with what was considered valuable input about that section. Since the implementation and design of the prototype has been one of the biggest parts in this thesis work it was seen appropriate to dedicate a chapter to present the final design.

## 4.1 Schematic

When all components were chosen began the time consuming work of symbolising each and every component that would be included in the printed circuit board (PCB) design. The program used for the design was Altium which is a modern and well used design tool for PCBs. A component symbol contains useful information about the component such as power ratings and component values. The symbol also contains all pins/pads that will be connected to the PCB. This is used in the trace routing part of the design to check that all traces connects to the correct net.

The entity of the schematic is displayed in figure 4.1 were all sections of the prescaler PCB are separately displayed. Note that the figure have been rotated to better fit the page. The Input connector is displayed on the top left of the figure followed by the two attenuators and after that (top right) the amplifier is presented. Along the RF path one can spot the serial capacitors used to AC couple the signal to avoid DC levels harming the input stage of the sensitive RF components. Note that in order to be able to AC couple the U.FL connectors between the components in the front-end two capacitors are used. After the amplifier the signal enters the prescaler circuit. The input to the prescaler is differential but in this design the single ended signal coming from the amplifier is AC coupled and then connected into the non inverting differential input of the prescaler. The idea of using a balun in order to differentiate the signal to increase the signal swing was quickly discarded since there were no suitable baluns available with such a large bandwidth as this project demands. The inverting differential input is AC coupled and tied to ground to avoid a floating input. In the lower middle section of the schematic the output circuitry can be seen. This will be further discussed in section 4.7.

The power supply section in the schematic can be seen in the left middle section and contains in. The common mode choke coil on the power input to decouple noise from the power supply. The +3 V regulation circuit and the +5 V regulation circuit. In the lower right corner the pin headers to connect the digital input/output signals to the microcontroller.

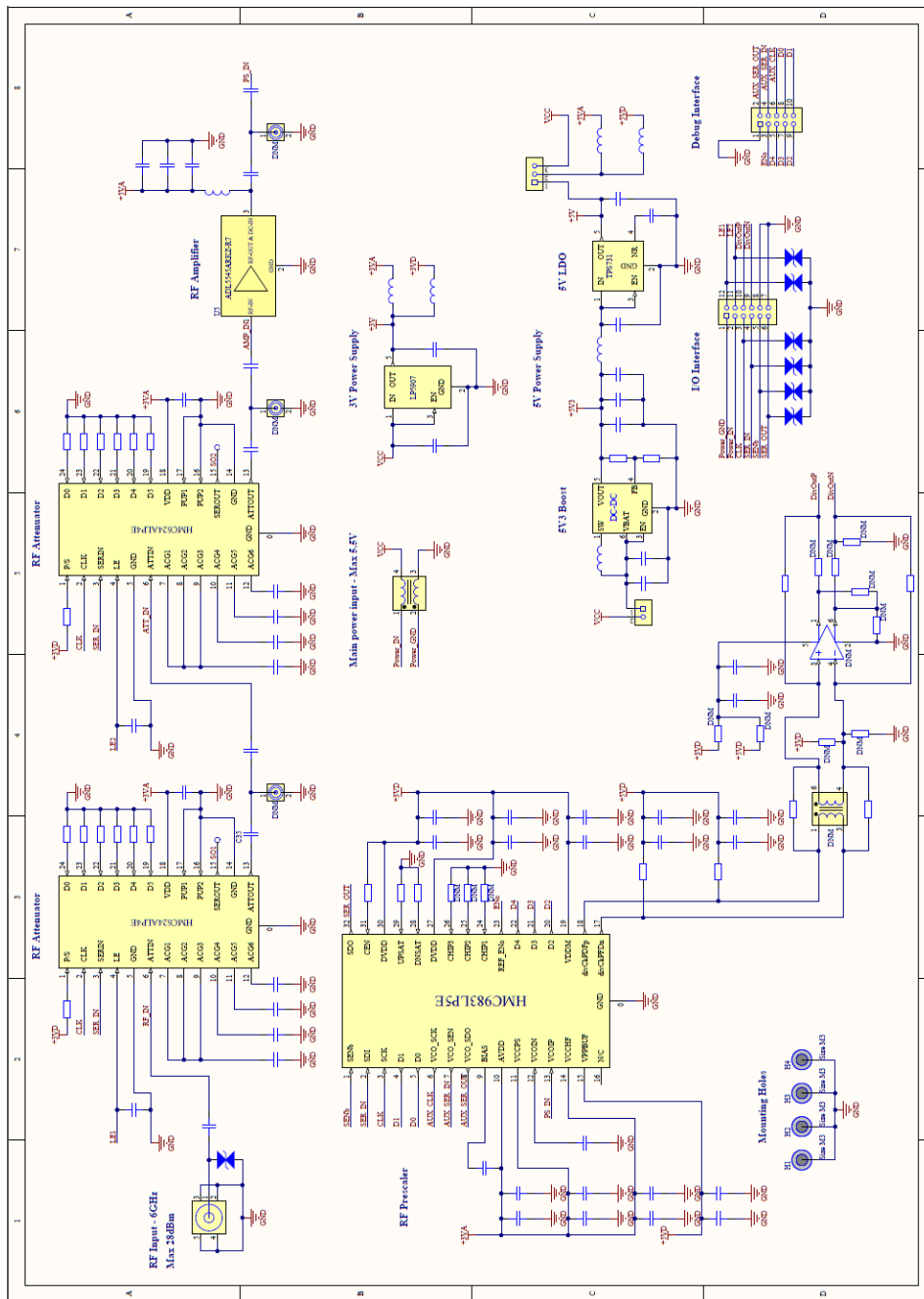
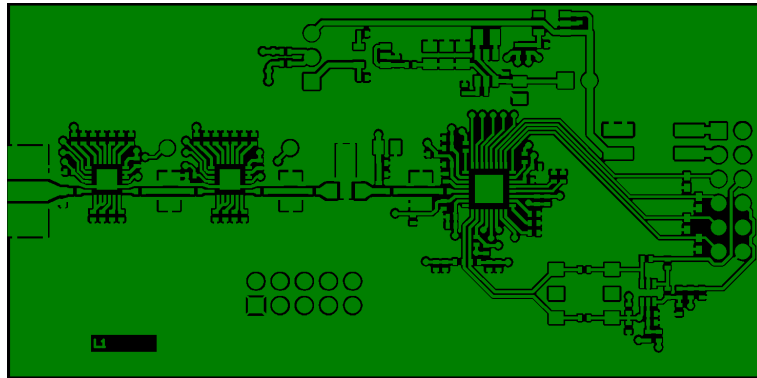


Figure 4.1: Schematic design of the prescaler PCB.

## 4.2 Layout

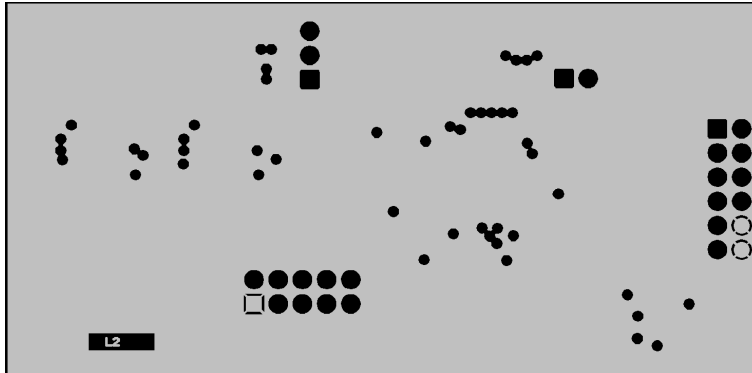
In this section the layout is presented. The following figures displays the all the layers on the 4 layer PCB that was designed. Figure 4.2 represents the top layer. Figure 4.3 displays the second layer which is used as as the ground layer. Figure 4.4 represents the supply layer. Finally the bottom layer can be seen in figure 4.5.

In order to decrees complexity for the mounting of the components, all components were placed on the top side of the PCB to keep them compressed and to avoid a board flip for the mounting company. When examining the top layer layout in picture 4.2 one can clearly see the RF trace beginning by the SMA connector footprint at the far left and then continuing through the two attenuators and through the amplifier to end in the prescaler. This track is kept straight in order to avoid changes in the characteristic impedance. The digital signals that controls the attenuators and the prescaler are routed to avoid the RF trace in the best manner possible. Test points have been placed on the digital outputs of the attenuator for debugging purpose. To be able to easily measure the RF signal along the front-end pads for U.FL connectors was added along the RF trace. In areas where no routing is present ground pours have been added for better RF behaviour. A constant potential surrounding the RF trace is ideal to not interfere with the signal. Sharp lines on the RF trace was avoided by using a tear drop design approach, which essentially just smooths sharp edges to avoid sudden changes in characteristic impedance. The characteristic impedance tuning can be seen on the unique width and distance to the ground plane of the RF trace. The footprint for the pin header for the digital input/output can be seen in the right end of the layout.



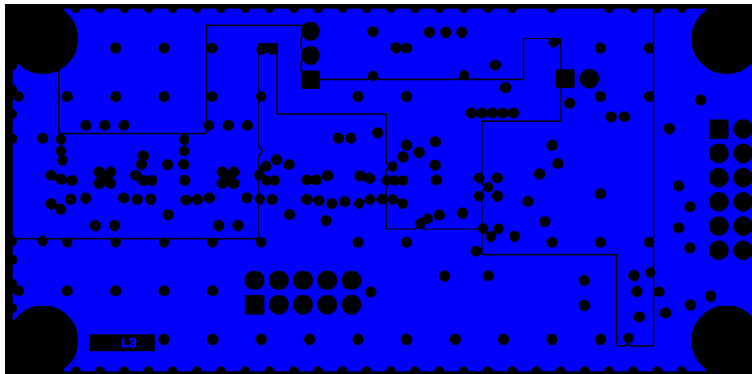
**Figure 4.2:** Layout of top layer of the prescaler PCB.

Layer two of the PCB was can be seen in figure 4.3 and is used as a ground plane. This design choice is made to surround the RF trace with a constant potential to avoid interference. Another advantage with a ground plane is that there is always a fast ways to terminate decoupling capacitances to maximise their efficiency.



**Figure 4.3:** Layout of second layer of the prescaler PCB.

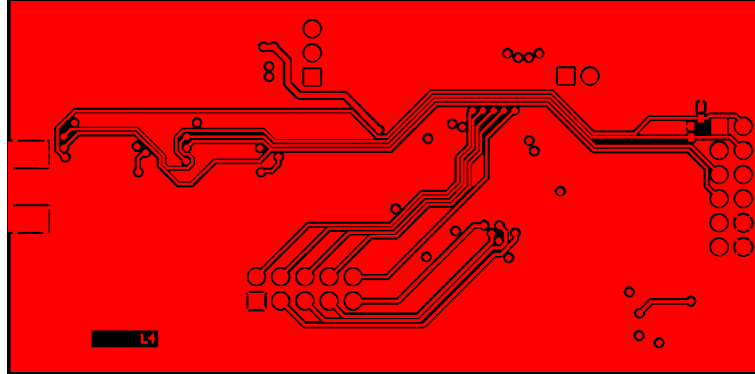
The third layer is seen in figure 4.4 and is used as the supply layer. Here the different supply voltages are routed. Pours are used to maximize the width of the areas for minimal series resistance on the supply rails.



**Figure 4.4:** Layout of third layer of the prescaler PCB.



The last layer presented is the bottom layer and can be seen in figure 4.5. This layer is used for routing some traces that wouldn't fit on the top layer, along with the prescaler debug interface and the power supply to the amplifier.



**Figure 4.5:** Layout of bottom layer of the prescaler PCB.

### 4.3 PCB overview

The resulting PCB after manufacturing and population can be seen in figure 4.7. The PCB was manufactured in panels by two, were the PCBs were held in place in the panel by small strips making it easy to snap the PCB free from the panel after it was populated by components. The company manufacturing the PCB was Würth Electronic AB. The company populating the PCB was Note Lund AB. The isolating material used in the PCBs were a special kind of FR4 suggested by Würth for it's RF features.

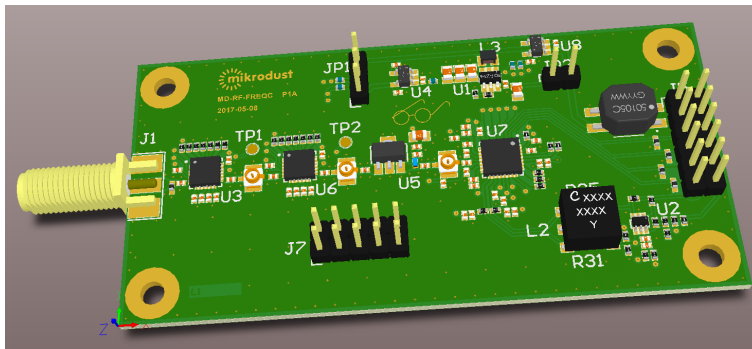


Figure 4.6: 3D view of the PCB design.

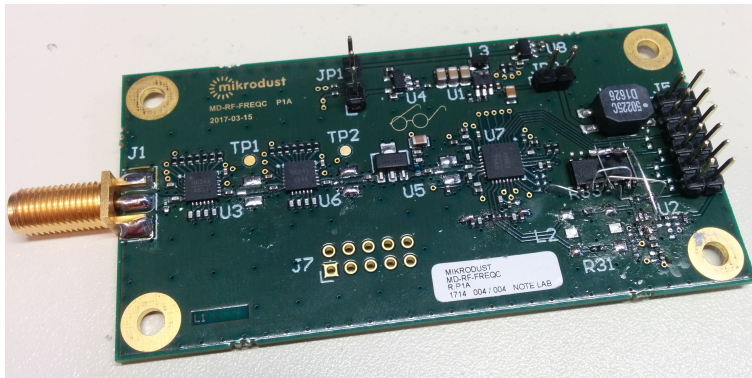
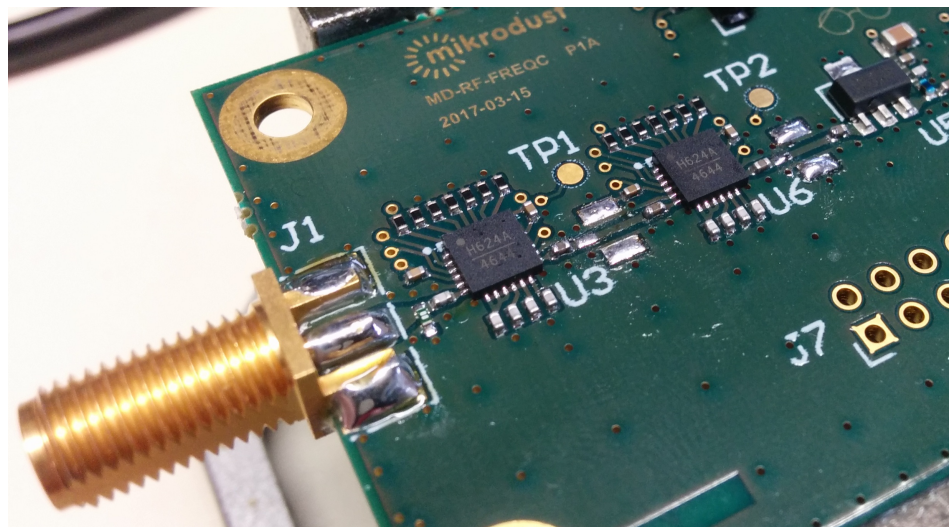


Figure 4.7: Picture of mounted PCB.

## 4.4 RF front-end

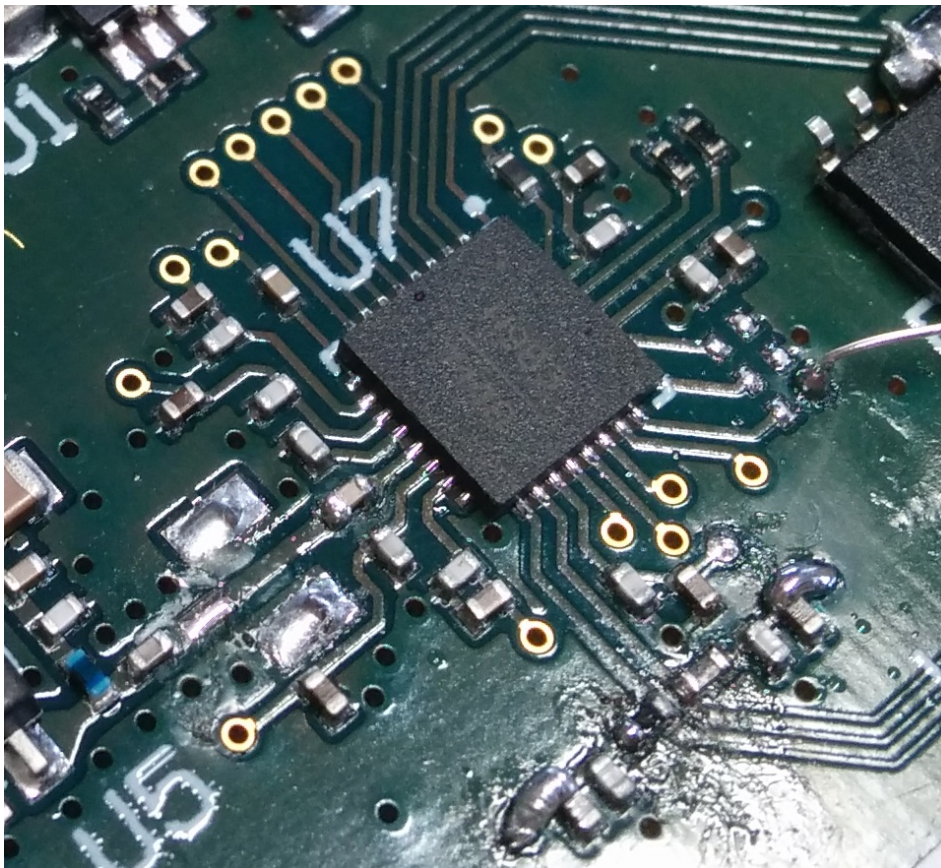
The finished front-end can be seen in figure 4.8. Two attenuators in series were used to increase the input power swing. The resistors over the attenuators are present to tie the parallel input pins to ground to avoid floating inputs, even though the parallel interface is not used in this design it is a good idea to prevent possible unstable behaviour. The amplifier is supplied through the output pin on the far right. The biasing network can be seen in figure 4.8 in the upper right corner, the parallel decoupling capacitors and the blue inductor preventing the RF signal to turn up the supply trace. Also note the via stitching along the RF path to ensure a well defined ground potential along the high frequency signal trace.



**Figure 4.8:** Overview of the RF front-end.

## 4.5 RF prescaler

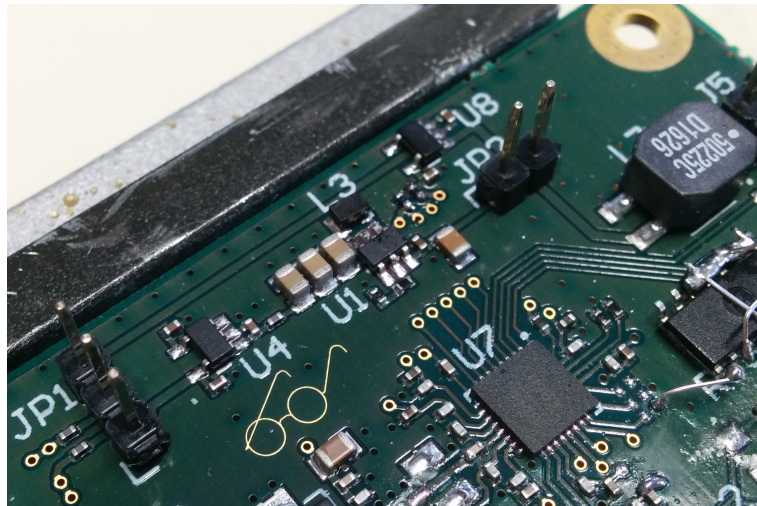
The prescaler section of the PCB can be seen in figure 4.9. The RF signal entering on the lower left side on the non-inverting differential input pin. The grounded inverting input pin is the one above. The chip is powered by both +3 V and +5 V which is collected from layer 3 through vias. All RF components are thoroughly decoupled. The output can be seen in the lower right section with two pull-up resistors in parallel with the trace. More discussion on the the prescaler output in section 4.7.



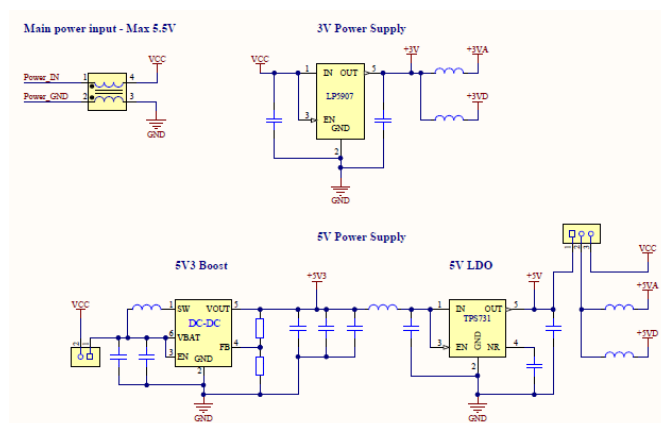
**Figure 4.9:** Overview of the RF prescaler.

## 4.6 Power supply

The power supply section of the PCB can be seen in figure 4.10. Upon closer study all components mentioned in section 3.5 can be seen in the figure. The common mode choke is visible at the far right, the +3 V LDO is visible in the top (component U8). The +5 V solution can be seen in the center of figure, U1 is the boost converter and U4 is the LDO to bring the voltage down to +5 V. The jumpers (JP1 and JP2) are used to disconnect the +5 V solution and drive the PCB directly from the supply voltage when using a stable external power supply and not USB power. The jumper configuration can be seen in the schematic section in figure 4.11.



**Figure 4.10:** Overview of the power supply.



**Figure 4.11:** Schematic of the power supply.

### 4.7 Prescaler output

The biggest issue encountered during the implementation of the hardware was by far to handle the output signal of the prescaler. The signal output from the prescaler is a differential signal which when using the recommended pull-up resistors has a signal swing from about +4,5 V to +5 V. As seen in the figure 4.12 many theories of how to best take care of this signal and converting it into a +3 V digital signal were implemented in the prototype design. The implementations included AC coupling of the signal either with a transformer or with two capacitors and then using a comparator as a level shifter to +3 V or the comparator would be supplied with +5 V and directly fed with the output signal, and then voltage divided to +3 V. The problem encountered after manufacturing and population when the testing began was that the width of the pulses outputted by the prescaler were too short to be for the comparator's slew rate. The pulse width of the output signal can be controlled via the serial interface, but the maximum width is represented by 61 signal periods of the input signal. For 6 GHz this would correspond to a pulse width of only 10,2 ns which was much too low for the comparator to manage. And even if a comparator was found which could follow the fast slew rate of the pulse, the microcontroller's pulse counter interface would not be able to detect the pulse.

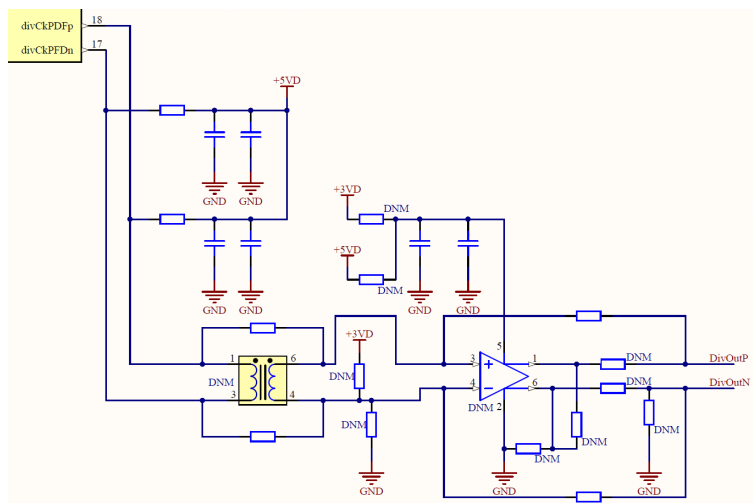
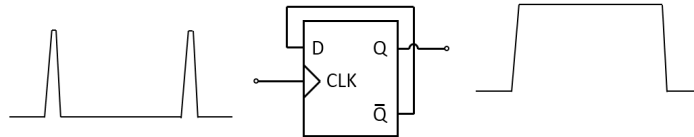


Figure 4.12: Schematic view of the prescaler output.

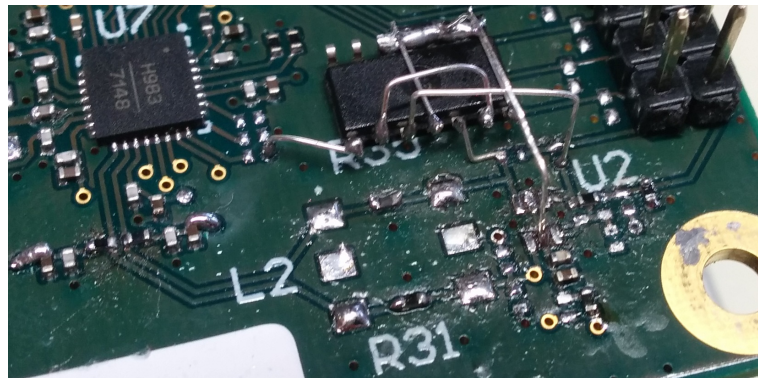


The solution for this problem on this prototype was to increase the resistor value on the pull-up resistors to the point at which the swing could be used as a clock signal to a high speed latch as mentioned in section 2.3. The latch would function as illustrated in figure 4.13 where the latch functions not only as a divide-by-2 frequency divider but also as a way to widen the pulses.



**Figure 4.13:** Output latch functionality illustration.

The latch was supplied with +5 V in order to handle the peak voltage of the pulse, this means that the output had to be voltage divided before being sent to the microcontroller. A potential problem with this solution is that the pulse voltage would be lowered too much to be able to be used as a clock for the latch for too high input frequencies. Due to the increased pull-up resistors the slew rate of the output was lowered. The latch solution was patched in to the prescaler output and verified up to 6 GHz. The patched design can be seen in figure 4.14. For the prototype design this would work, but for future revisions this would have to be fixed.



**Figure 4.14:** Overview of the prescaler output.

## Evaluation

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This chapter contains the results of the various measurements conducted when the prototype design were considered functional. The chapter has been divided into three sections and which are in the correct order. The frequency counter section, where measurements of frequency are conducted over the whole bandwidth of the project. After that comes the prescaler output section where the output of the prescaler is further examined. And last the power supply section where the power supply solution is evaluated.

### 5.1 Frequency counter

The prototype were input with frequencies covering the whole bandwidth of the project in steps of 500 MHz. The measurement was done three times with different input powers to which the front-end was tuned in order to keep the prescaler fed with the ideal input power through out the measurement. Each measurement were repeated 10 times and the mean was calculated. Included in the following tables is also the minimum and maximum deviation from the mean along with the variance of the data. For the input power of 0 dBm the results are seen in figure 5.2, for the input power of +10 dBm the result is displayed in figure 5.3 and for the result of the measrement made with an input power of -10 dBm the result is presented in figure 5.1.



Input frequency	Mean	Min error	Max error	Error variation
500 MHz	500000012,7 Hz	-87,7 Hz	45,3 Hz	133 Hz
1000 MHz	1000000022 Hz	-35,2 Hz	29,8 Hz	65 Hz
1500 MHz	1500000044 Hz	-17,5 Hz	14,5 Hz	32 Hz
2000 MHz	2000000040 Hz	-33,8 Hz	35,2 Hz	69 Hz
2500 MHz	2500000039 Hz	-13,8 Hz	9,2 Hz	23 Hz
3000 MHz	3000000065 Hz	-17,1 Hz	20,9 Hz	38 Hz
3500 MHz	3500000081 Hz	-51,9 Hz	49,1 Hz	101 Hz
4000 MHz	4000000044 Hz	-53,6 Hz	46,4 Hz	100 Hz
4500 MHz	4500000064 Hz	-45,6 Hz	58,4 Hz	104 Hz
5000 MHz	5000000076 Hz	-64,0 Hz	78,0 Hz	142 Hz
5500 MHz	5500000096 Hz	-89,2 Hz	47,8 Hz	137 Hz
6000 MHz	6000000061 Hz	-57,9 Hz	57,1 Hz	115 Hz

**Table 5.1:** Frequency counting results for -10 dBm input signal, 20 dB attenuation.

Input frequency	Mean	Min error	Max error	Error variation
500 MHz	500000005,2 Hz	-46,2 Hz	40,8 Hz	87 Hz
1000 MHz	1000000020 Hz	-31,7 Hz	26,3 Hz	58 Hz
1500 MHz	1500000012 Hz	-63,0 Hz	27,0 Hz	90 Hz
2000 MHz	2000000017 Hz	-35,8 Hz	33,2 Hz	69 Hz
2500 MHz	2500000007 Hz	-20,7 Hz	18,3 Hz	39 Hz
3000 MHz	2730000023 Hz	-25,2 Hz	43,8 Hz	69 Hz
3500 MHz	3500000034 Hz	-49,3 Hz	52,7 Hz	102 Hz
4000 MHz	4000000015 Hz	-50,3 Hz	45,7 Hz	96 Hz
4500 MHz	4500000036 Hz	-46,3 Hz	57,7 Hz	104 Hz
5000 MHz	5000000029 Hz	-34,8 Hz	73,2 Hz	108 Hz
5500 MHz	5500000003 Hz	-33,3 Hz	34,7 Hz	68 Hz
6000 MHz	6000000030 Hz	-68,0 Hz	48,0 Hz	116 Hz

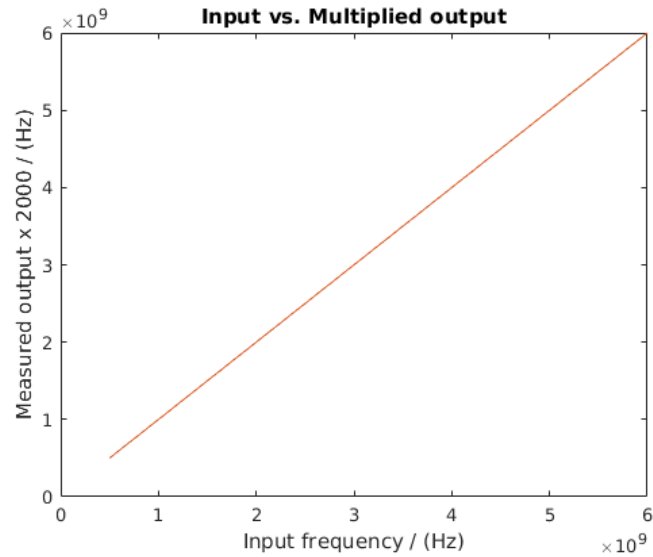
**Table 5.2:** Frequency counting results for 0 dBm input signal, 30 dB attenuation.

Input frequency	Mean	Min error	Max error	Error variation
500 MHz	499999998,5 Hz	-73,5	50,5	124 Hz
1000 MHz	1000000019 Hz	-46,4 Hz	45,6 Hz	92 Hz
1500 MHz	1500000012 Hz	-31,2 Hz	30,8 Hz	62 Hz
2000 MHz	2000000017 Hz	-14,2 Hz	20,8 Hz	35 Hz
2500 MHz	2500000007 Hz	-21,4 Hz	33,6 Hz	55 Hz
3000 MHz	2730000023 Hz	-44,2 Hz	24,8 Hz	69 Hz
3500 MHz	3500000034 Hz	-16,6 Hz	41,4 Hz	58 Hz
4000 MHz	4000000015 Hz	-42,1 Hz	91,9 Hz	134 Hz
4500 MHz	4500000036 Hz	-91,0 Hz	61,0 Hz	152 Hz
5000 MHz	5000000029 Hz	-40,4 Hz	25,6 Hz	66 Hz
5500 MHz	5500000003 Hz	-81,2 Hz	90,8 Hz	172 Hz
6000 MHz	6000000030 Hz	-56,3 Hz	18,7 Hz	75 Hz

**Table 5.3:** Frequency counting results for 10 dBm input signal, 40 dB attenuation

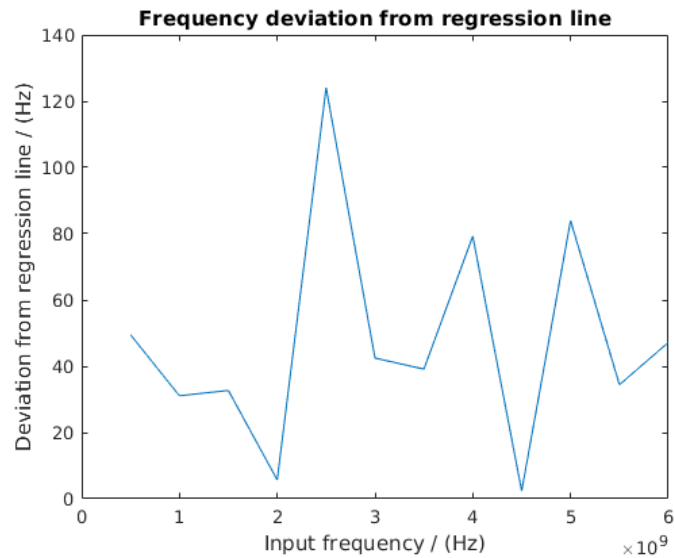
## 5.2 Prescaler output

The measurements of the prescaler output signal was conducted by feeding a frequency counter with the digital signal instead of feeding it into the microcontroller. The measurement was made with a span of the input power from -30 dBm to +20 dBm without any difference on the output. Note that the output of the frequency counter was limited to 0,1 Hz accuracy. Figure 5.1 displays the measured output multiplied by the divisor to display the linearity over the whole bandwidth.



**Figure 5.1:** Chart showing the measured output of the prescaler multiplied by the divisor for different input frequencies.

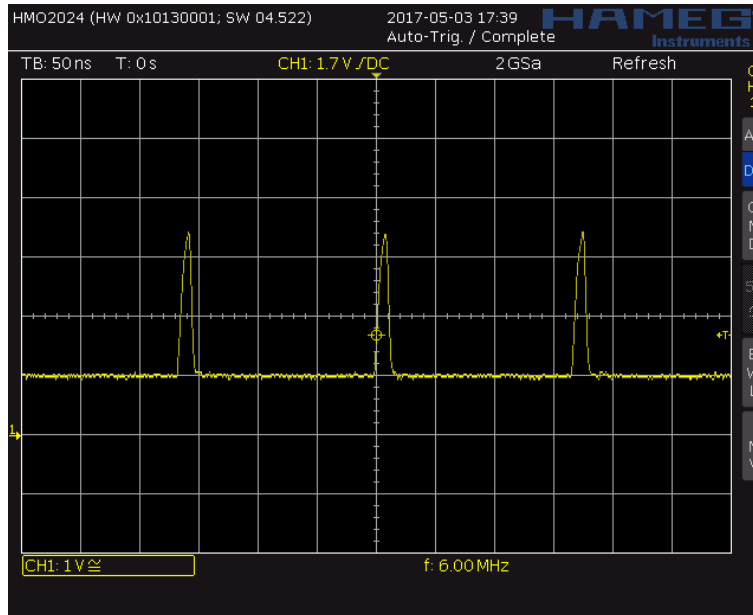
Figure 5.2 presents the deviation of each point to a linear regression line made from the measured data points.



**Figure 5.2:** Frequency deviation from regression line of prescaler output.

Figure 5.3 presents the signal output from the prescaler feeding the latch at

an input signal with a frequency of 6 GHz.



**Figure 5.3:** prescaler output measured before the latch for a input of 6 GHz.

### 5.3 Power supply

The power supply solution for achieving a stable +5 V supply was tested for the voltage span which a USB can output (4,75 V to 5,25 V). The result is presented in table 5.4.

Input voltage	Output voltage	Supply current
4,75 V	5,009 V	203 mA
4,8 V	5,009 V	202 mA
4,9 V	5,009 V	199 mA
5,0 V	5,009 V	197 mA
5,1 V	5,009 V	194 mA
5,2 V	5,009 V	193 mA
5,25 V	5,009 V	192 mA

**Table 5.4:** Supply measurement of the +5 V power solution.



In this chapter the results of the evaluations are discussed. To maintain the previous structure the chapter is divided into sections representing the sections in the evaluation chapter.

## 6.1 Frequency counter

When examining the results of the frequency counter the first thing noted is that for all cases of the measurement the maximum deviation from the average is well within the specified  $\pm 500$  Hz. The averaged error can easily be tuned to perfectly land on the correct frequency by altering the code but the swing of the output is not as easily improved. When comparing to the currently used product the resolution for a bandwidth of 1400 MHz to 6000 MHz is  $\pm 800$  Hz, which means that the prototype is a huge improvement to the previously used design. The results also shows that the current caption time of 4 seconds can be shortened and still be within the frames of the specifications. There are slight changes between the different input power levels but nothing worth noting. One thing that is quite interesting is that the largest variances are not measured at the highest frequencies, an explanation of this could be that there is higher insertion losses in the front-end for these frequencies causing the signal power transmitted to the prescaler to be less than nominal. Measurements were made on the front-end to verify the s-parameters of the design. These were discluded from the report since the results were deemed faulty. According to some of the measurements the prescaler the power level reaching the prescaler would not be sufficient for the prescaler to function properly for frequencies higher than 4 GHz. Although, judging by the results in the previous chapter the prescaler functions fine over the whole bandwidth and for a wide variety of input powers. Judging by some measurements done on the front-end the input signal would be 10 dB lower than for what the prescaler would stop working. The prescaler worked with a fixed attenuation over the whole bandwidth, this proves the functionality of the front-end. This is why these measurements were left out of the report. Possible sources of these faulty measurements are reasoned to be caused by bad connections in the U.FL connectors. Another possibility is that the error is introduced in the small cable used to connect the U.FL connector to the SMA connector reachable from outside the enclosure.

## 6.2 Prescaler output

When examining the linearity of the prescaler output in figure 5.1 the result is very pleasing. And upon closer inspection of the error along the bandwidth in figure 5.2 the result is well within the specifications. The result may very well be better than this if a more accurate counter would be used, but this measurement proves that this design is capable of fulfilling the specifications. These measurements were repeated without any difference on the output for a wide variate of input powers. Although the results from the frequency counter measurements have slight changes for different input powers. This is explained by referring to the accuracy of the frequency counter used which was 0.1 Hz. Since the divisor is 2000 and these changes noticed in the frequency counter output is smaller than 200 ( $2000 * 0,1$ ) the changes would first be noted in a hundredth of a hertz resolution. That is why the small changes are not detected on the prescaler output. The worry about the narrow peaks discussed in section 4.7 was proven to be able to trigger the latch even at high frequencies. The input signal to the latch was probed to verify the behaviour, the result can be seen in figure 5.3. The peaks measure a bit more than 10 ns in width but the peak is just approximately 3,5 V which according to the data sheet of the latch is just enough to count as a logic high. This solution would not be adequate in a finished product but for a prototype design made for verification it does the job fine. This would have to be changed in the second revision of the design though.

## 6.3 Power supply

The measurements conducted on the power supply solution were a success. The solution suggested by Texas Instruments will be sufficient for driving the design over a USB connection. The voltage is constant on a stable 5,09 V through the whole potential swing of a USB supply. The current is well within the 500 mA limit of the USB standard and will be able to run the microcontroller to control the design as well.

## Conclusion

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The scope of this project was to present a possible design of a frequency counter and evaluate and verify its functionality. To conclude this thesis report it is time to revisit the specifications of the project stated in section 3.1.

**Frequency rating** - The prototype design implemented reaches frequencies up to 6 GHz and down to about 70 MHz, well within the specified requirements.

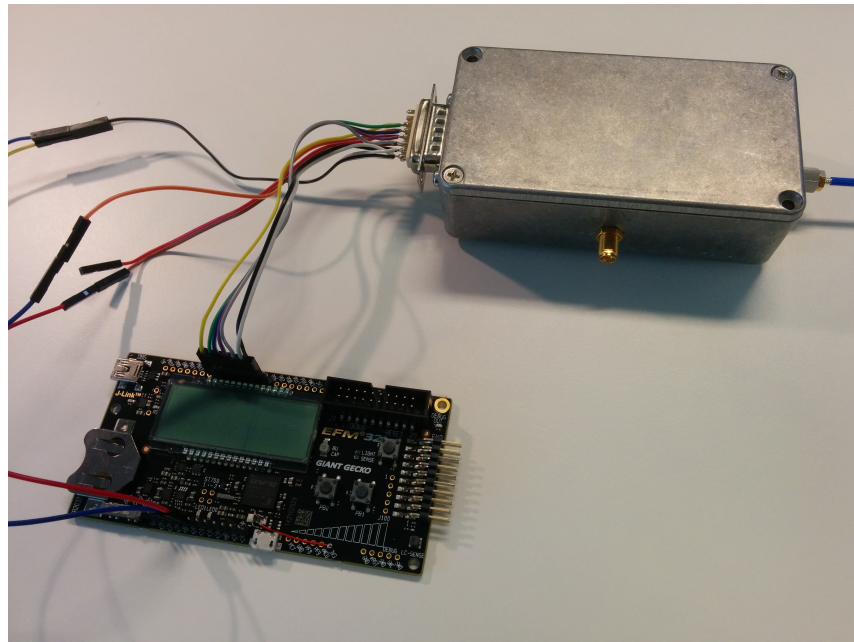
**Accuracy** - During the evaluation stage of the thesis work the worst variance of the frequency was 172 Hz. If the static error of the oscillator is tuned away in the algorithm this variance can be centred over the real frequency giving an accuracy of about half the variance.

**Power consumption** - The maximum current draw with the power solution included is 203 mA at 4,75 V making it possible to run this design off of a USB supply. The low power consumption makes it possible to include the microcontroller and creating a one chip solution.

**Cost** - The cost to populate a board is about 600 SEK. Combine this with the board cost and the RF tight aluminium enclosure and the price per counter will be about 1000 SEK. In comparison to the product used today it is about a fifth of the price. It is also worthy to note that the price will drop substantially for larger orders.

This design has still unfinished work that has to be done before it is ready to enter a test fixture, but this thesis work has supplied a solid ground which can be further improved. The prescaler design works and will be sufficient to prescale signals to be accurately measured. But small issues surrounding it will have to be examined before the design is truly ready. A discussion on the work to come can be read in section 7.1.





**Figure 7.1:** Picture of the finished prototype.

## 7.1 Future work

Future work in need of conducting before this product can be called done would primarily be examine a way to properly design the prescaler output to avoid the small margins of the signal driving the latch. A new latch would have to be found and included in the next revision of the board. Other items in need of change on the board would be to include the microcontroller on the board to avoid sending the divided output through the filtered connector on the enclosure. If this is avoided the division will not have to be quite as large and the accuracy of the counter may be able to be increased further. The oscillator of the design has to be further evaluated. The  $\pm 2,5$  ppm TCXO oscillator used in the prototype design worked, but no measurements of ageing or temperature dependence were conducted. When the new hardware is implemented the product would get a USB interface will be added and a protocol called Standard Commands for Programmable Instruments (SCPI) will be implemented. This is used by a vast majority of testing equipment in the modern day and is used to simply be able to communicate digitally with the devices.

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