# Automotive Test Advances

## Implications on ASIC production tests for Fingerprint Cards AB - new requirements and yield consequences

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Implications on ASIC production tests for Fingerprint Cards AB - new requirements and yield consequences

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May 29, 2017

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Printed in Sweden
Tryckeriet i E-huset, Lund

# Abstract

The purpose of the thesis was to study the safety and reliability requirements in the automotive industry from a production test perspective. A survey of the requirements in the automotive standard AEC-Q100 was conducted and the implications of compliance with the requirements were analyzed. In addition to this, production data was reanalyzed considering the requirements found in the survey. From this, conclusions regarding the necessity of new tests, new design requirements and potential yield reduction were drawn.

**Keywords:** Automotive electronics, production test, AEC-Q100, reliable electronics, dynamic testing, manufacturing of integrated circuits, Fingerprint Cards AB

# Acknowledgments

During spring of 2017 this report was written in partial fulfillment of the requirements for the degree of Master of Science in Engineering, Electrical Engineering at Fingerprint Cards AB in Gothenburg. This thesis would not have been possible if it were not for a number of dedicated persons.

Firstly, I would like to thank Johan Hammersberg and the entire production test team at the ASIC department at Fingerprint Cards. They have given me valuable insights and lessons in the importance of making electronics testable.

I would also like to thank my adviser at LTH, Markus Törmänen for supervising this thesis and for his teaching efforts during the earlier stages of my education.

Finally, I would like to express my sincere gratitude to my family and friends for always being supportive throughout my education.

# Popular Science Summary

Almost every new mobile phone entering the market have a built in fingerprint sensor which can be used for unlocking the phone. When the finger is placed on the fingerprint sensor a 'picture' of fingerprint is taken and if it sufficiently similar to a stored template the phone is unlocked. This simple authentication concept can be applied to almost an infinite number of use cases. Possible applications are replacing PIN codes on credit cards, unlocking doors and integrating fingerprint sensors into automobiles. There are many features in the car which can be improved by adding a biometric authentication system. Imagine for instance a car which automatically configures your seat and rear view mirrors to your personal settings and starts playing your favorite playlist when you unlock it. In addition to this your insurance company is notified that you are driving the car and the insurance rate is adjusted according to your driving experience, age and record of previous accidents. As you drive along and pass a high way road toll the payment is authorized by placing your finger on the sensor rather than queuing and paying with a credit card. Similarly, parking fees are accepted by placing the finger on the sensor.

However, introducing new electronic components in the automotive industry is a long and cumbersome procedure since there are stringent safety and reliability requirements. All electronic designs has to be thoroughly tested before they are qualified for use in the automotive industry. For general purpose, non safety critical components the electronic circuit undergoes electrical and environmental testing and if all the tests are passed the design is said to be qualified for use in automotive applications. However, if the electronic component is to be used in a safety critical application, the entire development process has to be reviewed by an external auditor to make sure that sufficient considerations to possible consequences of a system failure has been taken. Also, safety critical systems are sometimes required to have built in self testing and diagnostics.

Due to the complex manufacturing process of modern electronics some of the produced devices will contain defects which may cause the device to fail. Such devices must be detected in order to avoid delivering faulty products to the customer. It is preferable if the faulty units are found early in the enrichment process in order to save cost by discarding the faulty devices before they are put into a package. Testing is essential in manufacturing of automotive grade electronics due to the long product lifetime. However, testing is also an increasing part of

the manufacturing cost in modern electronics. Even though testing a circuit only cost a couple of cents a second and the test time is a fraction of a second in high volume production the total cost can be high. It can therefore be tempting to remove tests in order to save cost but that could lead to an increased number of test escapes, i.e. faulty devices that pass all production tests. On the other hand, adding new tests should be carefully considered. Adding a new test is a waste of money if it can not be proven that it increases the test coverage.

It is very likely that biometric authentication systems will be integrated in various automotive applications in the coming years. A part of the success will depend on the semiconductor manufacturers ability to provide reliable, safe and secure products.

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# Acronyms

**AMS** Analogue and Mixed Signal. 13

**ASIC** Application Specific Integrated Circuit. 30, 42

**ASIL** Automotive Safety Integrity Level. 16, 17, 34, 35

**ATE** Automatic Test Equipment. 9, 10

**ATPG** Automatic Test Pattern Generation. 10, 12, 13, 29, 35

**DFT** Design for Test. 3, 11, 35

**DPPM** Defective Part Per Million. 7, 8

**FMEA** Failure Mode and Effect Analysis. 41

**HTOL** High Temperature Operating Life. 20, 34

**$I_{DDQ}$** Quiescent Drain Current. 12, 23, 29

**MCM** Multi Chip Module. 33

**PAT** Part Average Testing. 24, 25, 30

**PGD** Probability of Good Die. 7, 8, 15, 30, 31, 37–39

**SBYA** Statistical Bin and Yield Analysis. 25, 31, 32

**SEOOC** System Element Out Of Context. 18, 34

**$V_{DD,min}$** Minimum Drain Supply Voltage. 13, 30

Chapter 1

# Introduction

The automotive industry is a new potential target market for Fingerprint Cards AB. Due to the strict safety and reliability requirements in the automotive industry electronic components have to undergo stringent tests in order to be qualified for use in automotive applications. Prior to an introduction in the automotive industry Fingerprint Cards AB need to investigate which requirements are applicable to a semiconductor supplier. This thesis work mainly focuses on the production test requirements in the automotive industry but qualification test requirements are also covered.

## 1.1 Aims and challenges

The goals of this thesis project were the following

1. Perform a survey of the standards governing requirements in the automotive industry
2. Map applicable test requirements in the automotive standards to Fingerprints Cards AB
3. Discuss the consequences of complying to different automotive standards

A challenge with this thesis was that the are many different standards in the automotive industry targeting different parts of the vehicle and different operating conditions as well as different levels of the system. Which standards that can be relevant to Fingerprint Cards in case of an introduction in the automotive industry had to be determined. Furthermore, the standard are formulated very generally and the implication on Fingerprints Cards AB of each statement in the relevant standards had to be thoroughly analyzed.

## 1.2 Related work

The need of reliable and well tested automotive electronics is obvious when thinking about automotive safety. Much research effort have been put into this field during the past 20 years. There are two well known conferences where advances

in tests of integrated circuits are discussed, namely IEEE International Test Conference and European Test Symposium. Many of the papers published by these conferences concern testing and testability of automotive electronics, showing the importance of new approaches to testing as more and more electronics are integrated into the automobiles.

The need of frameworks when working with automotive safety and reliability has resulted in several international standards, among them ISO 26262 and AEC-Q100.

## 1.3 Thesis outline

The thesis report is outlined as follows: In chapter 2 a thorough background in semiconductor manufacturing, failure mechanisms and testing is given. In addition to this two automotive standards that might be relevant to consider in a launch in the automotive industry are briefly presented. In chapter 3 the consequences of complying with the identified automotive requirements are discussed. In chapter 4 various methods for quality improvements used in the automotive industry are analyzed even if they are not required by the standards studied in the thesis. In the final chapter conclusions are drawn and further work is discussed.

# Chapter 2
# Background

## 2.1 Consumer and automotive electronics

During the past twenty years the electronic systems in automotive applications have become more and more advanced. As the number of electronic components in vehicles has increased concerns regarding the safety and reliability of these components have been risen. Due to the potentially dire consequences during a safety critical electronic system failure the reliability requirements are much more strict for automotive electronics than consumer electronics. A target in the automotive industry is 'zero defects' in all electronics. Many other industries such as medical, aeronautical and space applications also have these kind of reliability goals but in general these industries are not exposed to the same price pressure as the automotive industry and reliability issues can be solved with redundant systems. In order to avoid the expenses related to redundancy, automotive grade semiconductor manufacturers has opted to use various defect detection techniques such as Design for Test (DFT). In DFT extra effort is put into the design phase in order to ensure that the entire circuit is testable for defects. This could include adding extra logic in order to facilitate testing. This increases the overhead of the design but can make more blocks of the design observable and controllable. Such design schemes can increase the number of detected defects and thereby increase the quality of the shipped product. This is important because of the longer life time of the longer assumed life time of automotive electronics which is about 15 years. This can be compare to the assumed life time of consumer electronics which is about three years [14, 28].

## 2.2 Manufacturing of integrated circuits

The manufacturing of integrated circuits is a complex multi-step process. In all silicon based technologies the first production step in the process is to purify silica to to electronic grade silicon. This is done by first oxidizing the silica at high temperature and thereafter expose it to hydrochloric acid in order to remove impurities. The electronic grade silicon is thereafter formed into a disk called a wafer on which the electronic circuits are manufactured on.

In the manufacturing of the electric circuitry on the wafer two distinct phases

can be identified, namely Front End Of Line (FEOL) and Back End Of Line (BEOL). In the FEOL process the passive and active components of the circuit are formed on the wafer and in BEOL the components are connected together by metallic interconnects.

#### Front End Of Line

The FEOL process can be broken down to three different steps which are used to create the features on the wafer. In the first FEOL step, oxidation, a thin layer of silicon dioxide is grown on the wafer. The oxide layer servers as dielectric in the gates of the CMOS transistors. After the oxide layer is formed impurities, dopants, are implanted into the silicon. The dopants are used to give the silicon the desired electrical properties. In modern CMOS processes a method called ion implantation is used. Ions are accelerated through a strong electric field and directed to the wafer.

In order to create features on the wafer, a process called photo-lithography is utilized. A chemical called photo-resist is applied on the wafer and ultraviolet light is used to illuminate the wafer through a glass mask. This results in some of the photo-resist being unexposed to the UV-light. When the photo-resist is illuminated the either the exposed or unexposed photo-resist will undeveloped depending on the kind of photo-resist. The undeveloped photo-resist is thereafter removed. This process enables the next step, the etching. During the etching the pattern of the developed photo-resist is applied to the wafer. The etching is either done by applying different chemicals to the wafer or by plasma etching.

The oxide growth, ion implantation and photo-lithography steps are repeated in order to create different features on the wafer. After some iterations the gates, sources and drains of the transistors have been formed. [26]

#### Back End Of Line

After FEOL, the components on the wafer are connected together by interconnects in the BEOL process. The interconnects are usually made by aluminum or an aluminum alloy. Usually there are several metal layers which simplify the layout. The different metal layers are electrically connected by tungsten vias. When these processes are done each chip on the wafer is tested, "probed", in order to check for manufacturing defects. The wafer is finally diced and the chips that have passed the wafer test are packaged. [3]

### 2.2.1 Process stability

The manufacturing process of integrated circuits is incredible sensitive to contamination of impurities and mismatches during fabrication. It is sufficient to have a contamination of one part per million in the silicon in order to make the electrical properties change in a way that can make the chip fail. Many steps in the manufacturing process are not precise, for instance, during the ion implantation the ion concentration have a Gaussian spatial profile i.e. the dopant concentration

will not be exactly the same in the region where the ions are implanted. One can distinguish between four different variations in integrated circuit design [4]

1. Lot-to-lot
2. Wafer-to-wafer, within lot
3. Within wafer
4. Within die

Because of the process variations, the feature size - widths and lengths of the circuit elements, dopant concentrations etc will not be exactly the design value. This can be a problem specially in analogue circuits, where some transistor geometries have to be matched to each other, for instance in current mirrors. Some techniques exist to counter the process variation on the die. One of these is to draw the circuit elements that need to be matched in a common centroid technique. In this technique the circuit elements are split into an number of smaller elements which are placed in a two-dimensional pattern such that the effect of process variation across the die is limited. This design technique however, does not counter the process variations within the wafer or wafer-to-wafer variations. Therefore, the design has to be robust enough to be able to withstand different variations that can occur during production [3].

### 2.2.2 Corner lot analysis

In order to verify the robustness to process variations of an integrated circuit a "corner lot" is often ordered from the fabrication plant. The manufacturing process parameters are manually skewed in order to simulate the different variations that can occur in the fabrication process. In case the design is not functional in certain corners of the process then yield during manufacturing could be low and redesign of the circuit for increased robustness should be considered. In some cases it is desirable to set the production test limits from results of the corner lot, but due to the large variations in process parameters the acceptable ranges can become large. An alternative way of determining the test limits is called adaptive testing which is described later [25].

## 2.3 Defects in integrated circuits

In a complex integrated circuit there are many possible failure modes. Different failure mechanisms govern the failure rate during different parts of the life cycle of the integrated circuit. This is illustrated in figure 2.1. In the early life of the integrated circuit any latent manufacturing defect might cause the device to fail, but the risk of such failures are reduced after the 'infant phase'. After this initial phase, the failure rate is constant during the operational lifetime of the product until the product enters the wear out phase. This phase is characterized by an increase in the failure rate [24].

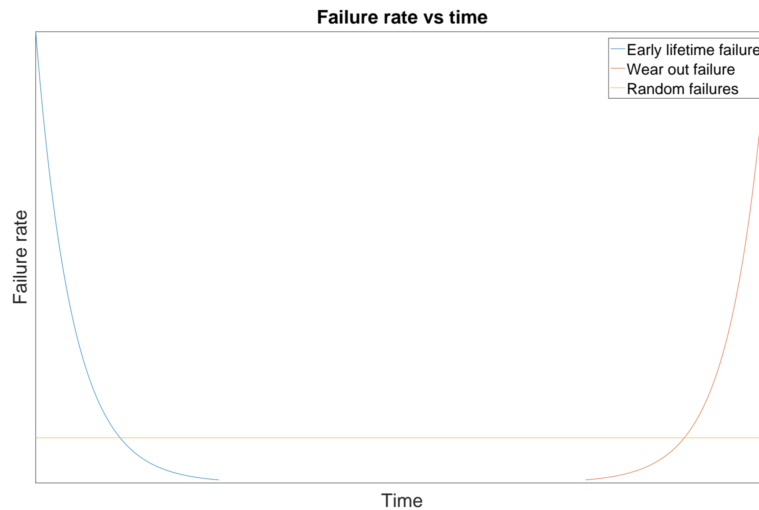


**Figure 2.1:** Failure rates during a life time of an integrated circuit.

### 2.3.1 Manufacturing related defects

Some of the defects occur during manufacturing of the circuits and some are related to wear of the component. Since feature sizes become smaller and smaller the designs become more and more sensitive to contamination of impurities. In addition to this, since numerous masks are used to create features on the wafer, mask matching is critical. If two masks are mismatched die features could be misplaced. This can also cause the circuit to fail [3].

### 2.3.2 Design-related failures

Due to the nature of CMOS manufacturing techniques it is impossible not to create unwanted PN junctions on the die. For instance, the source and drain of a NMOS transistor will form junctions with the p-doped substrate. If a NMOS transistor is in the proximity of a PMOS transistor in a n-well a pnpn junction is formed. In principle this junction constitutes two parasitic bipolar transistors that will act as a thyristor. During normal operation all the PN junctions are reversely biased but under certain external influence the two transistors might become active. If the pnpn junction starts to conduct it will not stop until the circuit is powered off, a condition that is often refered to as latch up. This can be catastrophic in a safety related applications. In addition to this, the circuit might incinerate due to the high current that flow through the parasitic bipolar transistors [3, 15].

### 2.3.3 Wear-related failures

Some of the defects in a semiconductor devices occurs when the device enters the wear out phase. An example of such a defect is electromigration. In metallic interconnects the flow of electrons can move the atoms in the interconnect, causing

areas with high resistance which may cause the circuit to fail. A way of decreasing the risk of electromigration is to make interconnects wider and thereby decreasing the current densities in the interconnects. Usually the process design rules are defined such that the risk of electromigration is low.

Another wear related failure is oxide failures related to hot carriers or dielectric breakdown. Due to the strong electric fields in the MOS transistor holes can obtain sufficient energy to be injected into the gate oxide. If the number of trapped holes in the oxide become too large an electrical path between the gate and the substrate is formed. This might change the transistor characteristics in a destructive way. The wear out related failures are closely related to the manufacturing process of the wafer [15].

### 2.3.4 Failure related metrics

A commonly used metric for calculating the number of defects in a design is the Defective Part Per Million (DPPM) which is shown in equation 2.1. The expression is derived by analyzing the test coverage and Probability of Good Die. If the Probability of Good Die is $PGD$ and the test coverage is $TC$ then the fraction of shipped bad units is $(1 - PGD) \cdot (1 - TC)$. Normalizing this expression with respect to the number of million good units the expression in equation 2.1 is obtained. In principle it is a metric of how many test escapes there are per million units.

$$DPPM = 10^6 \cdot \frac{(1 - PGD) \cdot (1 - TC)}{PGD} \tag{2.1}$$

This expression is evaluated for a some different values of $PGD$ and $TC$ in figure 2.2

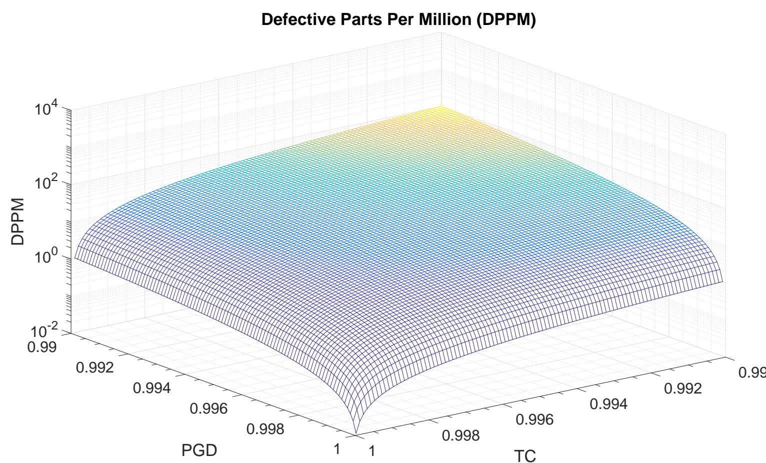


**Figure 2.2:** DPPM as a function of test coverage and probability of good die.

As seen in equation 2.1 and figure 2.2 either the PGD or the test coverage must approach 100% in order to achieve a low DPPM

The expression for DPPM can be used to evaluate difference in number of test escapes, either between two wafers or different areas of a single wafer. This is done by dividing the expression for DPPM, as seen in equation 2.2

$$I = \frac{10^6 \cdot \frac{(1-PGD_1)\cdot(1-TC)}{PGD_1}}{10^6 \cdot \frac{(1-PGD_2)\cdot(1-TC)}{PGD_2}} = \frac{\frac{(1-PGD_1)}{PGD_1}}{\frac{(1-PGD_2)}{PGD_2}} \tag{2.2}$$

$I$ is a metric for how many time more or less test escapes there are in different regions.

### Failure distributions

Assuming that all dies fail at a constant rate $\lambda$ the probability of failure of a deployed circuit can be described by a Poisson process. The time between the events in such a Poisson process can be described by the exponential distribution which has the following probability density function

$$f(\lambda, t) = \lambda \cdot \exp\left[-\lambda \cdot t\right], \text{ when } t, \lambda > 0. \tag{2.3}$$

Integrating this expression with respect to time yield the cumulative distribution function

$$F(\lambda, t) = 1 - \exp\left[-\lambda \cdot t\right] \tag{2.4}$$

This CDF describes the fraction of circuits with a failure rate $\lambda$ that have failed in a certain time $t$. $\lambda$ is a experimentally determined rate which is given by equation 2.5

$$\lambda = \frac{\chi^2_{(CL, 2\cdot r+2)}}{2 \cdot T} \tag{2.5}$$

where $\chi^2_{(CL,2\cdot r+2)}$ is the Chi-squared distribution with a confidence level of $CL$ and $r$ failures during the test. $T$ is the test time. The unit of $\lambda$ is $\mathrm{h}^{-1}$ but sometimes the unit FIT is used instead, 1 FIT $= 10^{-9}$ $\mathrm{h}^{-1}$ or equivalently one failure per one billion operational hours [33].

## 2.4 Test of mixed signal integrated circuits

A mixed signal circuit is a circuit that contains both digital and analogue blocks. The testing procedure of analogue and digital blocks has substantial differences. In digital testing a test pattern is applied and the output of the digital circuit is observed. If the output is not exactly the same as the expected value the circuit has produced a logic error, either from design flaw or from manufacturing defects. In either case the circuit has to be discarded. An analogue circuit on the other hand, produces an analogue signal which is continuous. Variations in different

parameters may or may not cause catastrophic failures. In general there is not a single correct output from an analogue block [30].

### 2.4.1 Automatic Test Equipment

In order to test mixed signal integrated circuits a device called Automatic Test Equipment (ATE) is used. The ATE consist of general purpose analogue- and digital circuitry to test the mixed signal integrated circuits. Some of the capabilities of an ATE are generating and monitoring digital patterns in order to test digital logic and generating precise DC and AC signals for parametric measurements. The ATE consist of a mainframe and a probehead. The main frame contains all the electronics for generating and measuring signals while the probehead contains the interface to the device under test. It is often desirable to test several chips in parallel due to the decreased test time and therefore cost. The number of devices that can be tested simultaneously is limited by the number of needles in the probe head. Testing with a state of the art ATE cost between one to six cents a second.

The integrated circuit is tested many times during the manufacturing process. Testing is typically performed on wafer level, intermediate packaging, and final assembly. The purpose of this to screen out defect units early in the value chain, i.e. save the cost of packaging a defect part. Since some defects only present themselves after the wafer is diced and packaged the device has to be thoroughly tested after each step in the value chain [30].

### 2.4.2 Verification, qualification and production test

In the design flow of semiconductor products an initial design has to verified to conform the the design specifications. The prototype is put under extensive testing under different conditions, such as temperature and supply voltage variations in order to verify that the circuit works and intended and that the design is robust. The verification testing is very expensive due to the number of tests and it is not desirable to perform the extensive testing on every chip in production due to the high cost. Instead, a fraction of the verification test set is chosen for production testing. The production test set must be chosen such that the electrical functionality is guaranteed while minimizing the test cost [30].

Depending on which application the integrated circuit will be used in the end customer may want the integrated circuit to qualify for an industry standard. Different standards are used in consumer electronic, medical, military and automotive applications. A standard can specify operating and storage temperatures, maximum mechanical stress and electrostatic discharge requirements. In addition to this, the qualification standards usually require the semiconductor manufacturer to stress test the design in order to verify that the risk of latch up is low and that the circuit is insensitive to electromigration. An example of a qualification standard used for integrated circuits in the automotive industry is AEC-Q100 [10].

### 2.4.3 Common production test

In this section some common production test of integrated circuits are described. The test set should be optimized for a large test coverage while minimizing the test time. Even though a large test set can provide a good coverage there is a limit where added test do not improve the quality of the shipped product [35].

#### Continuity testing

Before any functional test are executed the connectivity of the pads and presence of ESD-protection should be tested. This is done by a continuity test. The power supply pads of the integrated circuits are connected to ground and a small current is first pushed then pulled through the input/output pads of the integrated circuit. The voltage at the input/output pad is measured. If the ESD protection is functional then forward bias voltage of the ESD-protection diode should be measured. If 0 V is measured then there is a short circuit to ground and the ESD protection is inoperative. If there is no electrical connection, i.e. the line is open the ATE will notice it. Next, the same measurement is repeated on the power supply pads but the measurements are referenced to ground or other power supply pads. The purpose of the measurements is to verify the functionality of the ESD-protection and to ensure that there are no shorts between the power rails. [30]

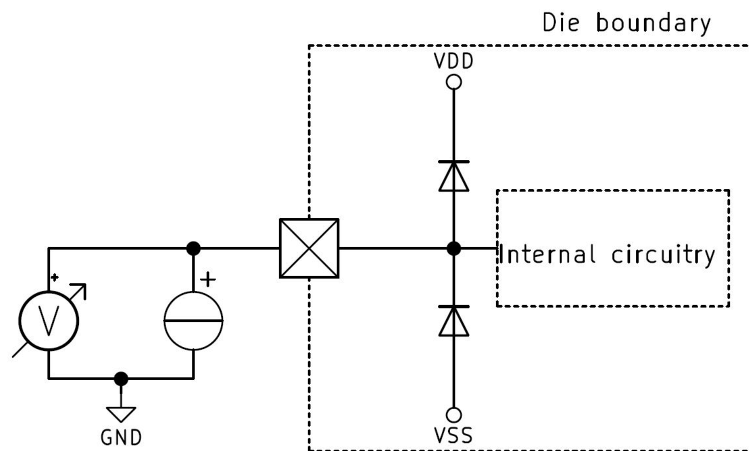


**Figure 2.3:** Test setup for continuity testing of I/O pad

#### Test of digital logic

The digital parts of an integrated circuit can be tested by applying a test pattern and monitoring the output. If any bit in the output differs from the expected value the circuit contains a logic error and the chip is considered faulty. For an n-input circuit there are $2^n$ possible input patterns. Since it would be impractical to

apply all possible patterns a fraction of the possible input patterns are selected for the production test using a Automatic Test Pattern Generation (ATPG) algorithm. The test pattern from the ATPG can provide a high test coverage in a reasonable amount of input patterns [32].

As a part of the DFT scheme all flip flops are built as scan flip flops. This increases the effectiveness of the ATPG algorithm and reduces the test time. A scan flip flop has two modes of operation 'scan' and 'normal'. In scan mode the flip flops operate as a shift register and the circuit can be put in a certain state. Scan mode is then disabled and the circuit operates as normal for a clock cycle. Finally, the circuit is put in scan mode again and the result is scanned out of the scan flip flops. Scan chains increase the controllability of the circuit but if the scan chain is very long then the test time can become unnecessary long. The scan chain can then be split into several shorter chains but that requires more pads for the scan input and output. The principle is shown in figure 2.4. The signal 'Test_Enable' is used to control the multiplexers to either use the state produced by the combinational logic or a state that has been scanned in.

An advantage with scan testing is that any sequential circuit can be treated as a combinational circuit. The ATPG algorithms can have problems analyzing large sequential circuits, especially if they are cyclic [5].

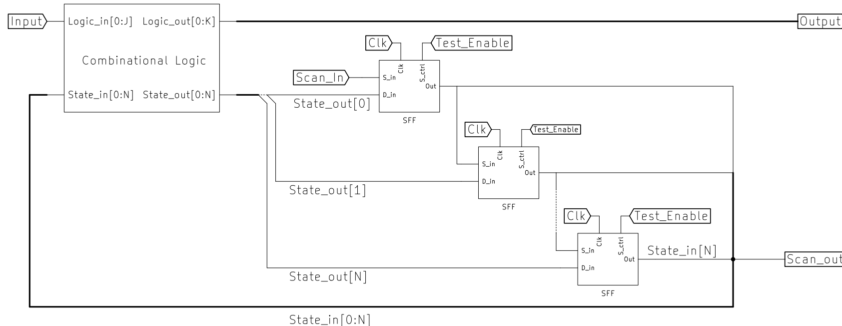


**Figure 2.4:** Principle of scan testing

In some cases, especially when the combinational part of the logic becomes large it can be hard to generate test patterns that check the functionality of every single node in the circuit. In such cases it can be necessary to add additional observation nodes in the logic so that the logic values in the combinational circuit can be scanned out with the scan chain [16]. This is illustrated in figure 2.5.

In order to make a model for the faults that can occur in the digital logic *fault-models* are used. The fault model is a description of how the fault affect the circuit. Two commonly used fault models are described below.

The stuck-at fault model is used to model logic errors produced by the circuit. A stuck-at fault is modeled by logically tying a node potential to the same potential as $V_{DD}$ or $V_{SS}$. When the node is put in the opposite logic state the fault is excited and if it is propagated to the output it can be observed. This is illustrated in figure 2.6. The function of the circuit is $Z = AB + C + D$. In order to check

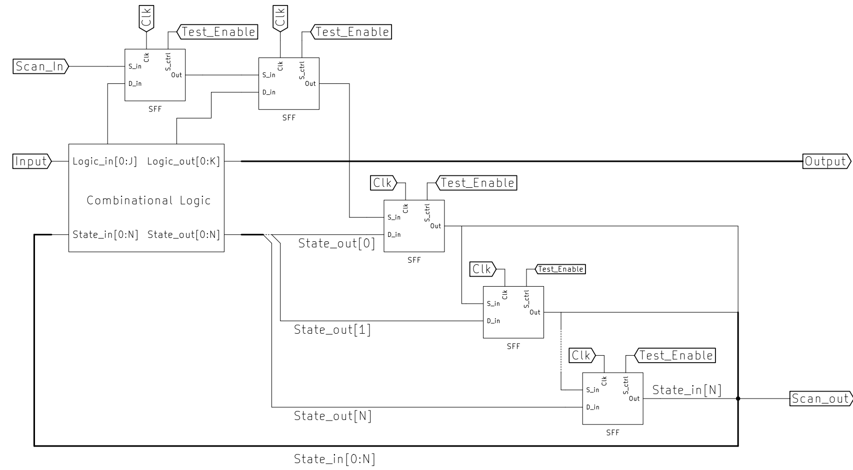


**Figure 2.5:** Scan test with increased observability

the output of the AND-gate for a stuck-at-zero fault the inputs to the AND-gate must be '1'. This will excite the fault. In order to propagate the fault to the output the inputs to the first OR-gate must be '0'. Because of the stuck-at-zero fault the output $Z$ will be '0' rather than the fault-free value '1'. Because of this, the fault is detected and the circuit can be discarded.

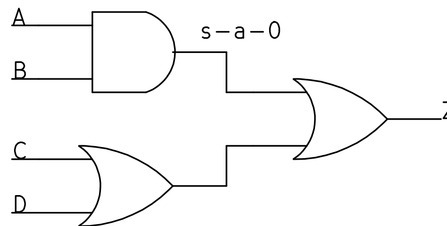


**Figure 2.6:** Test for a stuck at fault

Another commonly used fault-model is the transition delay fault model. It is fairly similar to the stuck-at fault-model but instead of regarding faulty nodes as stuck-at '0' or stuck-at '1' the faulty nodes are considered to be 'slow-to-rise' or 'slow-to-fall'. A potential defect is excited by a logic transition. If the correct

logic value has not been detected at the next sequential stage in a given amount of time the node is considered to be defect [7].

#### Quiescent drain current testing

Another common test to scan for defects is the Quiescent Drain Current ($I_{DDQ}$) test. The purpose of the $I_{DDQ}$ test is to find defects that cause abnormal quiescent current consumption. By measuring the quiescent current of the circuit the test verifies that there are no paths, bridging resistances, between nodes. Ideally, CMOS transistors do not conduct any current in the quiescent state except a very small leakage current. This is exploited in $I_{DDQ}$ testing since any bridging resistance will cause the leakage current to increase. $I_{DDQ}$ testing is a complement to the ATPG-testing since it may catch faults that the ATPG will not. For instance, bridging resistance can cause noise as well as timing issues. This fault model is sometimes refered to as the pseudo stuck-at fault model. A circuit containing such fault can pass all functional test during the fabrication but fail early in the field.

A problem with $I_{DDQ}$ testing is that there has to be a potential difference between two adjacent nodes in order to excite any bridging resistance defect between the two nodes. In order to extend the test coverage the $I_{DDQ}$ test should be repeated several times with different stimuli [2,22,29].

### 2.4.4 Weak chips and early life time failure

Some chips that pass the tests still contain defects that might cause the chip to fail early in its life cycle. Such chips are said to be weak. In order to screen for weak chips a Minimum Drain Supply Voltage ($V_{DD,min}$) test can be performed. In principle the test is similar to an ATPG test but the test is performed at a reduced supply voltage. The voltage is decremented until the circuit can not produce a correct logic value. This supply voltage is referred to as $V_{DD,min}$ By comparing the value of $V_{DD,min}$ of the circuits some assumptions can be made. For instance, $V_{DD,min}$ is increased if the circuit contains near metal or gate shorts. These kind of defects are not certain to be found in a functional test since the chip might be producing the correct logic value but the digital logic is weakly driven [6].

### 2.4.5 Functional test of analogue and mixed signal blocks

Testing of Analogue and Mixed Signal (AMS) blocks differs substantially from purely digital blocks. Since the output of the AMS block is continuous rather than discrete there is not an unique output signal that can tell whether the chip is faulty or not. Instead the test output is compared to a test criteria in order to determine the if the circuit is faulty. The test criteria is can be determined by measurements on the corner lot or by adaptive methods. Examples of AMS tests are current consumption in different power modes, pin leakage tests and output level tests [30].

### Input and output level tests

In order to verify the functionality of the input- and output buffers of the die input and output level tests are usually included in the production test set. The input buffers are tested by determining the minimum voltage that the chip registers a '1' as well as maximum voltage that the chip registers as a '0'.

The output buffers are tested in a similar way, but in addition to testing the logic voltage limits there is an additional requirement on the output buffer: it has to be able to supply a sufficient current while maintaining the logic state. The test setup for the output level test is shown in figure 2.7 [30].

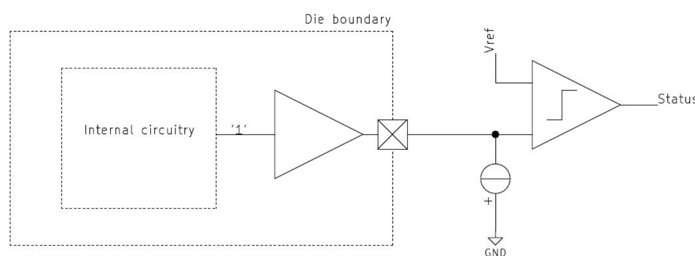


**Figure 2.7:** Test setup for output level test

## 2.4.6 Adaptive testing

In some cases it can be beneficial not to have static limits during parametric tests but rather adapt the test limits to the results from the wafer. The is due to the fact that process parameters can vary in deep sub-micron process. If a static limit is calculated from several lots the test limits will be wider than if the limits were calculated for a single lot. A problem with a wide guard band is that chips called outliers might pass the test even if their test result differ very much from their neighbors on the wafer. This is illustrated in figure 2.8. Such deviations can imply that the chip contains defects which should be investigated further [27,31]. A scheme for adaptive testing is described in section 2.5.2.

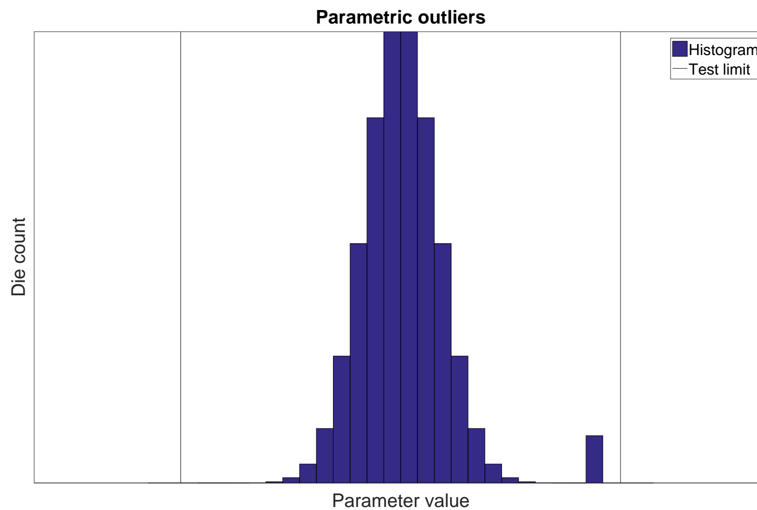


**Figure 2.8:** Outliers that are within test limits

### 2.4.7 Spatial algorithms for outlier detection

Usually, defects on a wafer tend to cluster and even if a die passes all functional tests it might have latent faults which will not appear until the device is deployed in the field. In order to avoid this, integrated circuit manufacturers sometimes opt to discard all dies that has a given number of faulty neighbors, even if the die pass all functional tests. If there are a high number of detected faults in a region, it is likely that there are also a high number of latent faults. Since such schemes impact the yield in a negative way they are usually deployed in applications that require extreme levels of reliability [35].

A tool called wafer maps are used to illustrate how defect chips are located on the wafer. A typical wafer map is shown in figure 2.9. The wafer map is colored such that the dies that fail the same tests have the same color.

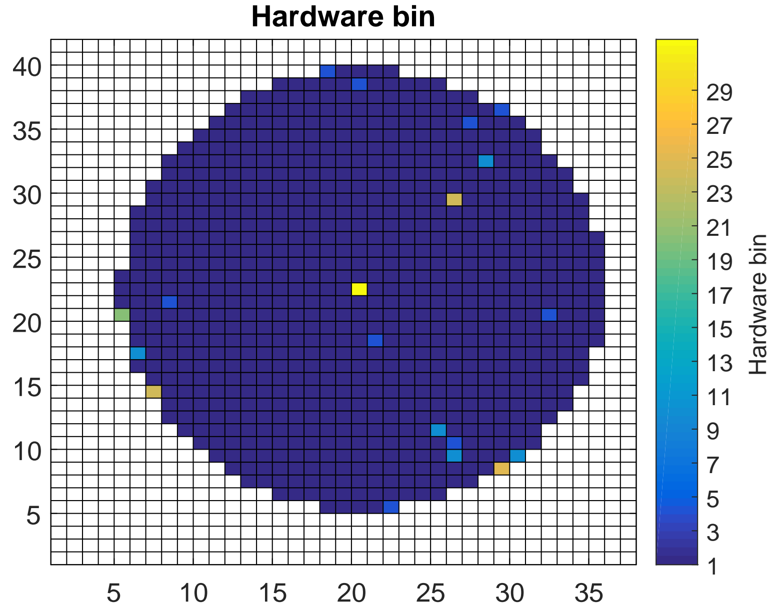


**Figure 2.9:** Typical wafermap showing which dies fail tests.

Another spatial scheme which are used to decrease the risk of delivering faulty dies is to exclude all dies on the wafer edge. It has been shown that dies on the wafer edge are more exposed to mechanical stress and uneven etching. This can cause the PGD to drop on the edge of the wafer [34].

### 2.4.8 Accelerated lifetime testing

In order to predict the reliability of electronic components accelerated lifetime tests is usually performed at the some stage in the development process of the semiconductor product. By exposing the circuit to thermal and electrical stress failure mechanisms can be accelerated. A commonly used model for the effect of increased temperature is the Arrenhius model. The model was derived in 1889 as a way to describe how the rate of chemical reactions increase with temperature. The model is now used to describe of the lifetime of integrated circuit are impacted by temperature increases [23]. The model assumes that the rate of a mechanism can be described by

$$\mathcal{R} = \gamma \cdot \exp\left[\frac{-E_a}{k_b \cdot T}\right]$$

Given a temperature increase the quotient of the two rates gives the expression for the acceleration factor

$$AF_T\,(T) = \frac{\mathcal{R}(T)}{\mathcal{R}(T_0)} = \exp\left[\frac{E_a}{K_b} \cdot \left(\frac{1}{T_0} - \frac{1}{T}\right)\right] \tag{2.6}$$

where $AF_T$ is the thermal acceleration factor, $E_a$ is the activation energy which is empirically determined to be in the range of 0.35 eV to 0.8 eV, $K_b$ is Boltzmann's constant, $T_0$ is the operating temperature and $T$ is the stress temperature.

In addition to the thermal acceleration increasing the supply voltage accelerates failure mechanisms in a similar way. The expression for the voltage acceleration is given by

$$AF_V(V) = \exp\left[\beta \cdot (V - V_0)\right] \tag{2.7}$$

where $AF_V$ is the voltage acceleration factor, $\beta$ is the acceleration parameter which is failure mechanism dependent, $V$ is the stress voltage and $V_0$ is the assumed operating voltage.

when the the acceleration factors are combined the total acceleration factor becomes

$$AF_{Tot} = AF_T \cdot AF_V \tag{2.8}$$

in order to determine how long the devices under test should be tested the following expression can be derived under the assumption that the failure rate $\lambda$ is constant which is given by equation 2.5

$$T_{test} = \frac{\chi^2_{(CL, 2\cdot r+2)}}{2 \cdot \lambda} \tag{2.9}$$

where $T_{test}$ is the required test time to achieve a confidence level of $CL$ that the device will have a failure rate of $\lambda$, which relates to a certain reliability. A commonly used confidence interval is 60%. The parameter $r$ is the tolerated failures during the testing. If $r$ is increased then the test time is also increased. The test time can be reduced by putting the component under stress i.e increasing the temperature or supply voltage during the test. Since the assumption that the failures are exponentially distributed the number of devices tested can also be increased in order to reduce the test time further. The expression for the reduced test time is given by

$$T_{test,reduced} = \frac{T_{test}}{AF_{Tot} \cdot N} \tag{2.10}$$

where $N$ is the number of devices under tests [21, 33].

## 2.5 Automotive standards

### 2.5.1 ISO 26262

ISO 26262 is an international standard which defines functional safety requirements for the automotive industry. The standard covers the entire life cycle of the automotive systems that provide safety related functions. Each safety related system is assigned an Automotive Safety Integrity Level (ASIL) classification. Depending on which ASIL classification a safety system has different requirements apply. For instance, different ASIL levels have different requirements on failure

rates due to random hardware errors. This section mostly describes the hardware requirements of ISO 26262 but the standards defines many more requirements regarding the development process. For instance quality management, change control and record management.

### Safety and non-safety related hardware

In the workflow of ISO 26262 a hazard analysis has to be performed during the concept phase in product development. Any potentially hazardous event has to be classified into a severity class from "S0 - No injuries" to "S3 - Life-threatening injuries, fatal injuries", a probability of exposure-class from "E0 - Incredible" to "E4 - High probability" and a controllabillity class from "C0 - Controllable in general" to "C3 - Difficult to control or uncontrollable". Depending on the classification of the hazardous event an ASIL level is determined. If the hazard is non safety related then no ASIL classification is necessary and the classification is QM.

### Hardware requirements in safety related systems

For safety related hazards a corresponding safety goal has to be determined. A safety goal is a top-level system requirements that is supposed to reduce the risk of a hazard. The risk of violating a safety goal due to hardware failure must be evaluated. This is done by estimating failure rates due to random errors. The target values are cited in table 2.1

| Safety Level | Random hardware failure rate |
|---|---|
| ASIL D | $< 10^{-8}\ h^{-1}$ |
| ASIL C | $< 10^{-7}\ h^{-1}$ |
| ASIL B | $< 10^{-7}\ h^{-1}$ |
| ASIL A | $< 10^{-6}\ h^{-1}$ |
| QM | N/A |

**Table 2.1:** Failure rates requirements due to random hardware failures in ISO 26262

In order to ensure that the failure rates in table 2.1 are ensured a quantitative analysis must be performed considering, among other things, the architecture of the item, diagnostic coverage by safety mechanisms and the estimated failure rate of each hardware part. The failure rate must be established using a recognized industry source or statistics from field returns.

For the two higher ASIL levels C and D dedicated measures must be taken in order to ensure the accuracy of the estimated random hardware failure rate. ISO 26262 suggest the following examples of procedures that can ensure the accuracy.

(a) Electrical or thermal rating

(b) Sample testings

(c) Burn in

### ISO 26262 architectural metrics

ISO 26262 defines four different kinds of faults:

**Single Point Fault (SPF)** Fault in a hardware part which has not safety mechanism. The fault leads to a violation of a safety goal.

**Residual Fault (RF)** A part of a hardware fault which leads to a violation of a safety goal. The part of the fault is not covered by a safety mechanism.

**Multiple Point Fault (MPF)** Several independent fault that in a combination lead to a perceived, detected or latent failure

**Safe Fault (SF)** Fault that do not increase the probability of violating a safety goal

ISO 26262 defines two metrics that describes the robustness of the system, either from good diagnostic coverage from safety mechanism or from a good design.

$$SPFM = 1 - \frac{\sum_n (\lambda_{SPF} + \lambda_{RF})}{\sum_n \lambda} \tag{2.11}$$

$$LTFM = 1 - \frac{\sum_n \lambda_{MPF,Latent}}{\sum_n (\lambda - \lambda_{SPF} - \lambda_{RF})} \tag{2.12}$$

where $\lambda_i$ is the associated failure rate of fault type $i$ and $n$ is the number of safety related hardware elements. The target values for the architectural metrics are shown in table 2.2 [11].

| | **ASIL B** | **ASIL C** | **ASIL D** |
|---|---|---|---|
| **Single point faults metric** | $> 90\%$ | $> 97\%$ | $> 99\%$ |
| **Latent faults metric** | $> 60\%$ | $> 80\%$ | $> 90\%$ |

**Table 2.2:** Architectural metrics requirements in ISO 26262

### System Element out of Context (SEooC)

As mentioned in the previous section the safety goals are a top-level requirement. However, the automotive industry is a multi-tier structure where suppliers in the lower stages do not know the architecture and safety goals of the final product. This is referred to as System Element Out Of Context (SEOOC). The developer of the SEOOC has to make assumptions regarding the use of the SEooC and create safety requirements from this. When the SEOOC is deployed in the final item these assumptions has to be verified [1, 17].

### 2.5.2 AEC-Q100

'AEC-Q100 - Stress test qualification for integrated circuits' defines qualification tests for integrated circuits in automotive applications. AEC-Q100 has eight different test groups containing various tests. The integrated circuit is temperature graded between 0 to 4 depending on the temperature requirements of the integrated circuit. The test groups are shown in table 2.3. The tests in test group A and B depends on the temperature grading. The purpose of AEC-Q100 is to provide a framework for qualification of automotive electronics. There are no no third party that certifies a product claiming to be compliant to AEC-Q100. Instead the supplier submits the test results of the tests and the customer determines whether the results are in compliance with the standard. All test are not applicable to all semiconductor devices so certain tests can be omitted if it is justified - and approved by the customer.

| Test group | Qualification |
|---|---|
| A | Accelerated environment stress test |
| B | Accelerated lifetime simulation test |
| C | Package assembly integrity tests |
| D | Die fabrication reliably tests |
| E | Electrical verification tests |
| F | Defect screening tests |
| G | Cavity package integrity tests |

**Table 2.3:** Qualification tests in AEC Q100

In the coming sections the tests in AEC-Q100 are described briefly. The test methods, sample sizes and fail criteria are found in [10].

#### Accelerated environment stress test

The qualification tests in Test group A is shown in table 2.4. Semiconductor manufacturers delivering integrated circuits to the consumer electronic industry are usually performing similar tests. However, the current sample sizes are usually smaller then the samples required by AEC-Q100.

**Preconditioning**
Preconditioning is a stress test that simulates the thermal and moisture stress of the device being soldered.
**Temperature humidity bias or Bias HAST**
Accelerated temperature and humidity stress.
**Unbiased HAST**
This test ensures that the device is moisture resistant.

*Continued on next page*

Table 2.4 – *Continued from previous page*

**Temperature cycling**
Tests the interconnects resistance to thermal expansion and contraction.
**Power temperature cycling**
Only required for devices with a power rating of 1 W or more
**High temperature storage life**
Thermal stress when the device is unbiased.

**Table 2.4:** Accelerated environment stress test

### Accelerated environment simulation tests

Test group B in AEC-Q100 contain tests that test the reliability of the integrated circuit. The tests are shown in table 2.5. In order to reduce the test time all tests are carried out in elevated temperature.

**High temperature operating life (HTOL)**
Demonstrates the reliability of the product by accelerating failure mechanisms. The circuit can be put under both thermal and electrical stress in order to increase the acceleration factor.
**Early life failure rate**
Similarly to the High Temperature Operating Life (HTOL) this test demonstrates reliability but the focus is to prove that the devices survive past their infant phase. The test method is the same as the HTOL test. However, the sample size is larger and the test time is shorter.
**NVM endurance**
Tests that non volatile memory retains its content even under environmental stress.

**Table 2.5:** Accelerated lifetime simulation test

### Package assembly integrity tests

Test group C contains test which demonstrates the integrity of the package that the die is placed in. The test are shown in table 2.6.

**Wire bond shear**
Verifies the integrity of the bond wires and the attachment to the die.
**Wire bond pull**
Verifies that the bond wires are sufficiently well attached to the substrate of the package and that the bond wires are strong enough.
**Solderability**
The purpose of this test is to verify that the package terminations are solderable.
**Physical dimensions**
Verifies that the size of the package do not deviate to much form lot to lot.
**Solder ball shear**
This test is only applicable to Ball Grid Array (BGA) packages.
**Lead integrity**
Only required for through-hole devices

**Table 2.6:** Package assembly integrity tests

### Die fabrication reliability tests

The qualification tests in test group D verifies that the manufacturing process is resistance to wear out failure mechanisms. The tests are shown in table 2.7. AEC-Q100 do not specify the test methods for the qualification test but the standard demand that the supplier shall be able to produce test results if required by the customer.

**Electromigration**
Verifies the integrety of the metallic interconnect. A potential qualification test is JEDEC JESD87 [20]
**Time dependent dielectric breakdown**
In order to ensure that the reliability of the insulator in gates and capacitors a dielectric breakdown test should be performed on the device. An example of a test method is JEDEC JESD35a [19]
**Hot carrier injection**
A problem in MOS technologies is that charge carriers, holes or electrons can get trapped in the gate oxide of the transistors. This can change the electrical characteristics in a negative way. Reliability testing for such failures can be carried out according to the test method JEDEC JESD28 [18]
**Negative Bias Temperature instability**
This is a wear out mechanisms that mainly affects the PMOS transistors in the device. It manifests itself by an increase in threshold voltage. The physics behind the failure mechanism is yet not completely understood. An example of a test method is JEDEC JESD90

*Continued on next page*

Table 2.7 – *Continued from previous page*

**Stress migration**
Around vias there can be stress induced in the metallic interconnect. This stress can induce voids in the interconnect. A test method for these defects is JEDEC JESD87 [20]

**Table 2.7:** Die fabrication reliability tests

### Electrical verification tests

A part of the qualification test concerns the electronic performance of the device, both from a qualification and production perspective. The qualification tests are shown in table 2.9. In addition to the qualification tests the electrical verification tests contains requirement on how thoroughly all devices should be tested in production. The production test requirements are the same as the requirement for the pre- and post stress function program as seen in 2.8.

| Test | Acceptance criteria |
|---|---|
| Analogue circuit blocks | 100% specification coverage |
| Digital circuit blocks* | 98% stuck-at test coverage |
| Transition delay faults in digital blocks** | 80% test coverage |
| Pseudo stuck-at IDDQ faults in digital blocks** | 70% test coverage |

**Table 2.8:** Test program requirements in AEC Q100

Since $I_{DDQ}$ testing can be done in various ways AEC-Q100 provides guidelines on how the $I_{DDQ}$ testing should be carried out. A certain test pattern is applied to the circuit and when the circuit has reached it quiescent state the current from the positive digital power supplies are measured. In order to excite any defects in the circuit the operating voltage should be the maximum rated voltage. AEC-Q100 also defines a method of setting the test limits for the $I_{DDQ}$ test. [7]

**Pre- and post stress function parameter**
Test program to be executed before and after stress. The test program should fulfill the specifications in table 2.8

*Continued on next page*

*If IDDQ testing is used the required test coverage is 97%
**Desirable in order to increase test coverage

Table 2.9 – *Continued from previous page*

**Electrostatic Discharge - Human Body Model and Charged Device Model**
This qualification tests measures the device capability to withstand a short but large current discharge.
**Latch-up**
The circuit must be able to withstand certain input conditions without triggering latch-up.
**Electrical distributions**
Limits for drift of key parameters should be determined. This should be done in collaboration with the customer.
**Fault grading**
In order to be able to determine to develop a adequate test program the design has to be fault graded. Which fault models to use and which fault coverage are required is described in AEC-Q100-007
**Characterization**
When a new design is developed it should be characterized in order to determine data sheet limits. Guideline for this process is given by AEC-Q003
**Electromagnetic Compatibility**
Ensures that the device does not radiate nor is sensitive to radiation
**Short circuit characterization**
Only applicable to smart power devices. Dialogue between supplier and customer
**Soft error rate**
Only applicable to devices with more than 1Mbit of SRAM or DRAM
**Lead free**
For lead free devices additional testing of the solder is required.

**Table 2.9:** Electrical verification test

### Defect screening tests

In order to increase the reliability AEC-Q100 suggest outlier screening by a method called Part Average Testing (PAT). Basically, PAT is a method to remove all dies which parametric values deviate more than six standard deviations from the sample mean. PAT can be either static or dynamic. In static PAT data from several lots are collected and analyzed in order to establish test limits, where data from a single wafer is used in Dynamic PAT. In order to minimize the effect of dies which have off-the-chart parametric values PAT testing utilizes robust mean and standard deviation. The formula for the PAT limits is given by equation 2.13.

$$PAT = Q_2 \pm 6 \cdot \frac{Q_3 - Q_1}{1.35} \tag{2.13}$$

where $Q_1$, $Q_2$ and $Q_3$ is the first, second and third quartile of the ranked data. AEC-Q100 suggest but do not demand the following tests for PAT. [7,8]

- Pin leakage test

- Standby power supply current test
- IDDQ test
- Over-voltage stress test
- Low level input current test , high level input current test , low level voltage test, high level output voltage test
- Propagation delay test
- Extended operating tests

### Statistical bin and yield analysis

AEC-Q100 also defines a method of working with abnormal yield drops and if many dies fail specific tests called Statistical Bin and Yield Analysis (SBYA). By collecting yield and fail bin data from six lots mean values and standard deviations can be calculated, if they fit a normal distribution. If the yield drops or if the failure rate in a specific bin increases more than three standard deviations from the mean value then the wafer, wafer lot or assembly lot should be reviewed. If the yield decrease or fail bin increase is more than four standard deviations then the wafer, wafer lot or assembly lot should be quarantined. A record of all quarantined wafers must be kept as well as documentation of root cause analysis of the yield drops and corrective actions [9]

$$SYL_1 = \bar{Y} - 3 \cdot Y_\sigma \tag{2.14}$$

$$SYL_2 = \bar{Y} - 4 \cdot Y_\sigma \tag{2.15}$$

$$SBL_1 = \bar{X} + 3 \cdot X_\sigma \tag{2.16}$$

$$SBL_2 = \bar{X} + 4 \cdot X_\sigma \tag{2.17}$$

where $\bar{Y}$ is the mean yield, $Y_\sigma$ is the standard deviation of the yield, $\bar{X}$ is the mean fraction of dies in each failure bin and $X_\sigma$ is the standard deviation of the fraction of dies in each failure bin.

### Cavity package integrity tests

If the dies is placed in a cavity package then the integrity of the package must be verified by exposing the package to various mechanical stresses. The qualification tests are shown in figure 2.10. The qualification test in this group are very dependent on the kind of package the die is placed in and the supplier must analyze which qualification tests are applicable.

| |
|---|
| **Mechanical shock** |
| Verifies functionality after short pulses of high acceleration. |
| **Variable frequency vibration** |
| In order to qualify for use in automotive applications the device must be able to withstand the vibrations in the car. |
| **Constant acceleration** |
| Another mechanical stress test that is used in AEC-Q100 is constant acceleration. It verifies the mechanical endurance of the device. |
| **Gross/Fine leak** |
| This qualification test is only applicable for ceramic packaging |
| **Package drop** |
| Applicable for Micro Electro-Mechanical Systems (MEMS) cavity devices |
| **Lid torque** |
| This qualification test is only applicable for ceramic packaging |
| **Die Shear** |
| Tests how well the die is attached to the substrate in the cavity. |
| **Internal Water Vapor** |
| This qualification test is only applicable for ceramic packaging |

**Table 2.10:** Cavity package integrity test

#### Multi-Chip-Modules

In some applications, a module consists of several dies, where each die has an unique function, for instance a sensor die and a die containing the digital logic or memory. The supplier may not want the end user to have access to all signals some pads are not routed to the user interface. This can cause issues testing the final module. AEC has recognized and is currently working on a new standard where qualification tests for Multi-Chip-Modules are presented.

From the project updates it is known that the dies should be fully tested in accordance to the electrical functional tests in AEC-Q100 and thereafter qualify the module to the environmental tests and package integrity tests. It is of course also desirable to perform some functional tests on the module to assure that the dies have not been damaged in the packaging process. [13]

### 2.5.3 Automotive industry quality management

In addition to the standards mentioned above, the automotive industry has special addendum to the quality management standard ISO 9001, called ISO/TS 16949. This standard establishes procedures to continuously improve the product, guidelines for document control etc. This standard focuses more on the organization of the company and is out of scope of this thesis, but might be relevant to Fingerprint Cards AB in the future [12].

Chapter 3

# Consequences of compliance with automotive standards

In this chapter the implications of compliance with the automotive standard AEC-Q100 is discussed. In addition to this the reliability requirements of AEC-Q100 and ISO 26262 are compared.

## 3.1 AEC-Q100 requirements

All specified analogue parameters of the investigated sensor are not tested in production. This is because they are considered to be 'guaranteed by design'. In order to comply with the demands of AEC-Q100 and recommendations of AEC-003 several parametric test have to be added, or the specification of the product has to be changed. Whether tests are added or untested parameters are removed from the product specification or a combination of the two is made an alignment process have to be initiated.

Also, the stuck-at test coverage of the digital blocks do not reach the levels defined in AEC-Q100. In principle this is a design issue since the ATPG tool will not be able to generate test pattern that ensure the functionality of unobservable nodes, they may be tested by the test pattern but the ATPG tool will not be able to determine whether the node contains a fault or not. This could be solved by adding observation flip-flops and thus increasing the length of the scan chains as indicated in figure 2.5. However, this would require redesign of the sensor and re-synthesizes of the digital blocks. Even though the report from the ATPG-tool specifies a lower test coverage than the limit in AEC-Q100 some gates might be indirectly tested by other functional tests. The test coverage of the functional tests should be investigated further.

Currently, only one current measurement is done in the $I_{DDQ}$-testing. Since AEC-Q100 demands a higher coverage with at least 70% pseudo stuck-at test coverage the $I_{DDQ}$ test must be modified. Also, AEC-Q100 requires the $I_{DDQ}$ test to be performed at the highest operating supply voltage, at the present moment it is only performed on the nominal voltage. Since the pseudo-stuck-at fault coverage requirement is substantially lower than the normal stuck-at fault coverage requirement there should not be any problems generating new test patterns which

meet the requirements in AEC-Q100. However, considerations to the increase in test time should be made.

### 3.1.1 Introduction of new tests

There are no schemes in the current test patterns to test the circuit for transition delay which is recommended by AEC-Q100. Since the current operating frequency of the Application Specific Integrated Circuit (ASIC) is fairly low, the sensitivity to transition delay faults are also low. However, if more computing capacity is added to the ASIC, and hence the frequency of certain parts of the ASIC are increased, then transition delay testing could be utilized. It could also be advantageous to introduce $V_{DD,min}$ testing in order to find weak chips.

### 3.1.2 Dynamic part average testing

The impact of adding Dynamic PAT in accordance with equation 2.13 was analyzed using wafer production data. By calculating the robust mean and robust sigma the Dynamic PAT limits could be obtained. The result of the Dynamic PAT is shown in figure 3.1, 3.2, 3.3, and 3.4. One should note that the dynamic limit in figure 3.3 is higher than the static limit. This demonstrates the necessity to still have static limits in order to have adequate test limits.

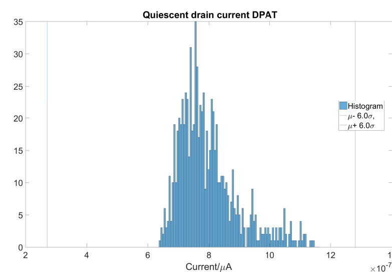


**Figure 3.1:** Dynamic part average testing of quiescent drain current.

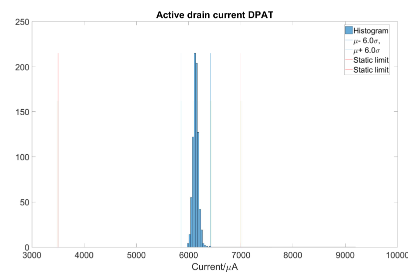


**Figure 3.2:** Dynamic part average testing of active drain current.

In table 3.1 the impact of Dynamic PAT is shown. The data is a mean value of wafer in a single lot. As seen in the table the yield drop is small. It shows that the process is stable. However, there are only a few parametric measurements done in the test program of the investigated sensor. If more parametric measurements were made the impact of Dynamic PAT could be higher. One should also observe that the PGD is extremely high of the dies that pass the Dynamic PAT.

The most efficient way to do the Dynamic PAT screening seems to be on the wafer level since it will be easy to sort out the dies that have failed the screening. Performing PAT after the wafer is diced would pose some issues in sorting the dies since it is not known if an individual die passes the screening until all the dies from the wafer have been measured.

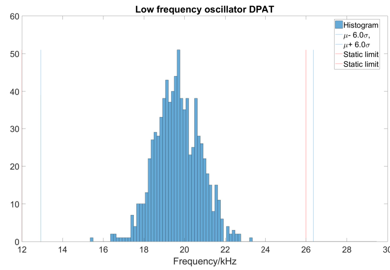


Figure 3.3: Dynamic part average testing of low frequency oscillator.

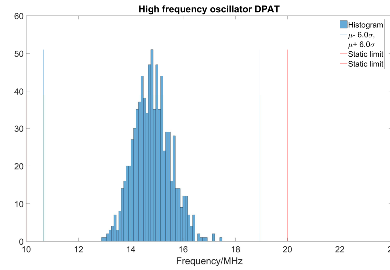


Figure 3.4: Dynamic part average testing of high frequency oscillator.

| Screen | $\sigma$ | DPAT PGD (%) | Overall yield (%) | Yield drop (%) |
|---|---|---|---|---|
| *IDDQ* | 6 | 99.350 | 97.450 | 0.030 |
| *IDD* | 6 | 99.523 | 97.465 | 0.015 |
| *FOSCLO* | 6 | 98.986 | 97.480 | 0.000 |
| *FOSCHI* | 6 | 98.986 | 97.480 | 0.000 |
| — | — | — | — | — |
| *Total* | 6 | 99.523 | 97.435 | 0.045 |

**Table 3.1:** DPAT metrics

### 3.1.3 Statistical yield analysis

The addition of SBYA is preferable since it is a tool to ensure process stability and quality. The principle figure is shown in figure 3.5. Hwbin 1 is the bin of good dies. The other hardware bins represent different failures.

The mean value and standard deviation of dies in each bin have been calculated. As seen in the figure the procedure is fairly simple and any wafers that would contain excessive yield loss or have a high failure rate in specific bins would be detected. Since such a system must be constantly online in foundry it has to be developed in cooperation with the foundry. It is not unlikely that the foundry offers such solutions.

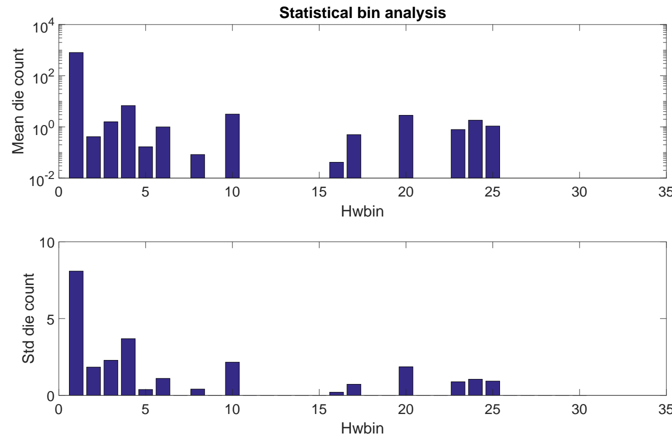


**Figure 3.5:** Statistical bin analysis.

The SBYA limits have been calculated in table 3.2 and 3.3. In the fraction of good dies on a wafer are below SYL1 or if the fraction of dies in a failbin are above the SBL1 limit the wafer should be put under engineering review. Similarly, if the limits SYL2 or SBL2 are exceeded the the wafer should be quarantined.

| Hwbin | SYL1 (%) | SYL2 (%) |
|---|---|---|
| 1 | 94.62 | 93.65 |

**Table 3.2:** Statistical yield limits

| Hwbin | SBL1 (%) | SBL2 (%) |
|---|---|---|
| 2 | 0.72 | 0.94 |
| 3 | 1.02 | 1.29 |
| 4 | 2.16 | 2.60 |
| 5 | 0.16 | 0.20 |
| 6 | 0.52 | 0.65 |
| 8 | 0.16 | 0.21 |
| 10 | 1.16 | 1.42 |
| 16 | 0.08 | 0.10 |
| 17 | 0.32 | 0.41 |
| 20 | 1.01 | 1.24 |
| 23 | 0.42 | 0.52 |
| 24 | 0.60 | 0.73 |
| 25 | 0.47 | 0.58 |

**Table 3.3:** Statistical bin limits

### 3.1.4 Qualification of the product

Depending on where in the value chain Fingerprint Cards enters the automotive industry the qualification for AEC-Q100 will look differently. Since the package and module constitutes a part of the environmental protection of the die any environmental stress test can not be carried out before the the die is inserted into a module. Fingerprint Cards AB could opt to sell wafers to a package manufacturer which in turn sell packages to a module manufacturer. If such a business model is used then there have to be a collaboration between the three to ensure suitability for automotive use and to make sure that the requirements in the automotive standards are fulfilled. On the other hand, if Fingerprint Cards AB chooses to develop a module of their own then the whole responsibility of the qualification will lay on Fingerprint Cards AB.

It is impractical to route all signals to the module contact. A problem with this is that the testability of the circuit drops if for instance signals to enable scan test mode are not accessible in the final module. Therefore, it is necessary to ensure that the electrical functionality of the die completely tested before the dies are packaged and after that do functional testing of the module. This would require an analysis of the test coverage of the functional test can be launched after the die is packaged.

If the business model where wafers are sold is chosen the wafers have to be tested in accordance with the production test requirements in AEC-Q100 to a package manufacturer. In addition to the wafer, test software should be supplied to ensure that no part of the wafer have been damaged when it was diced and packaged. Some certification that the wafer fabrication process has been tested for die fabrication reliability in accordance with the test in tests in test group D in AEC-Q100 should also be provided.

Since Fingerprint Cards most likely would outsource the production of the modules in the same way that wafer production of wafers is outsourced today that procedure would not differ to much if the other business model is chosen. However, more this business model would require more effort maintaining all designs and customizing the module to customer specific requirements.

AEC is currently working on a new standard for qualification of a Multi Chip Module (MCM). It is likely that some parts of this standard will affecting Fingerprint Cards AB automotive expansion in some way. Especially if the aim of automotive introduction is be higher up in the value chain.

## 3.2 ISO 26262

Since ISO 26262 is mostly applicable on safety related hardware a use case analysis of the fingerprint sensor in the automotive industry has to be made. If the fingerprint sensor will only be used for configuring seat, tune in radio etc an ISO 26262 is most likely not necessary since it would not be required by automotive manufacturers. However, if there is a demand for integrating the fingerprint sensor in a safety related system an ISO 26262 certification is necessary.

If there is a customer demand for an ISO 26262 certified product this would have a substantial impact on Fingerprint Cards. Since ISO 26262 regards the de-

velopment phase of both hardware and software the entire development phase has to be remade with the approach suggested by ISO 26262. Since the exact use case in a safety related system is unknown the SEOOC has to be utilized.

Fingerprint Cards could opt to use the strategy to first qualify their intended automotive product for AEC-Q100 and introduce fingerprint sensors in the automotive industry. This will give Fingerprint Cards a opportunity to prove their use case and if there is a customer demand for integration in the safety related systems then the organization could be certified according to ISO 26262.

## 3.3 Reliability differences between ISO 26262 and AEC-Q100

The challenges of delivering a reliable product that must last for at least 15 years will be challenging since the current life time of a fingerprint sensor is approximately the same as the life time of a mobile phone, i.e. two years. The two standards discussed in this thesis, AEC-Q100 and ISO 26262 have different approaches regarding the reliability of the products. AEC-Q100 makes the supplier demonstrate the reliability by a HTOL test. ISO 26262 on the other hand, requires different failure rates depending on the ASIL level of the system. Using equations 2.5 and 2.9, 2.7, 2.6 the two methods can be compared.

Assuming that $3 \cdot 77$ units are HTOL tested at a temperature of 125°C for 1000 hours. The supply voltage is 110% of its nominal value and the assumed operating temperature is 50°C. The thermal activation energy and voltage acceleration factor is assumed to be 0.7 eV and 0.5 $\mathrm{V}^{-1}$ respectively. Further assuming that a confidence interval of 60% is desirable and no device failures are tolerated the failure rate then becomes

$$AF_T = \exp\left[\frac{0.7\ \mathrm{eV}}{8.61 \cdot 10^{-5}\ \mathrm{eV/K}} \cdot \left(\frac{1}{(50+273)\ \mathrm{K}} - \frac{1}{(125+273)\ \mathrm{K}}\right)\right] = 114.4 \tag{3.1}$$

$$AF_V = \exp\left[0.5\mathrm{V}^{-1} \cdot (1.98\ \mathrm{V} - 1.8\ \mathrm{V})\right] = 1.1 \tag{3.2}$$

$$AF_{Tot} = 114.4 \cdot 1.1 = 125.1 \tag{3.3}$$

$$\lambda = \frac{\chi^2_{(60\%,2\cdot 0+2)}}{2 \cdot 1000\ \mathrm{h} \cdot 3 \cdot 77\ \mathrm{units} \cdot 125.1} = 2.20 \cdot 10^{-8}\ \mathrm{h}^{-1} = 22.0\ \mathrm{FIT} \tag{3.4}$$

Comparing this with the failure rate limits in table 2.1 one can see that the failure rate is well below the limit for ASIL C. However, if the fingerprint sensor will be used in a safety critical application then it is reasonable to assume that it will be a system that consists of many parts each having a certain failure rate. Since these failure rates each will contribute to the overall failure rate of the system the product supplied by Fingerprint Cards much have a substantially lower failure rate than the requirement in ISO 26262. However, from a reliability point

of view, the calculated failure rate should be sufficient for integrating the sensor in systems with the lower ASIL classifications. However, it has to be determined on a case-by-case basis.

## 3.4 New design requirements

The requirements in the automotive industry puts high demand on the design to be testable. Even if DFT is used it might be hard to make the entire design controllable and observable as illustrated in figure 2.4. This becomes especially obvious of the output of the digital block is connected directly to an analogue blocks. Since AEC-Q100 require 98% test coverage of digital *and* digital portions of mixed signal blocks testability of these blocks have to be guaranteed. This might require observation flip flops to be added whose only purpose is to observe output values from combinational blocks. This is illustrated in figure 2.5.

This will of course add design overhead and thus die area. Currently, the interface between the digital and analogue domain is tested by functional tests. A problem with this is that it is hard to quantify the test coverage. If scan testing is used instead the ATPG tool can be used to quantify the coverage. This should be considered in new generations of fingerprint sensors.

### 3.4.1 Characterization and datasheet requirements

Fingerprint Cards AB should establish a procedure where the characterization of any new device is closely related to the determination of data sheets limits of the device. The data sheet should contain minimum, typical and maximum values for all relevant continuous parameters. Which parameter which are relevant must be discussed by the supplier and customer. It should also be assured that the parameter do not drift to much when operating at its temperature extremes.

### 3.4.2 Robustness requirements

In addition to the previously mentioned testability requirements AEC-Q100 presents new robustness requirements which are not present in the consumer electronic industry. The robustness requirements relate to mechanical stress, vibration, electromagnetic compatibility and Non Volatile Memory Endurance. It may be so that the current design and fabrication process fulfill the requirements but it may be so that the production of automotive grade fingerprint sensors have to be put at specific fabrications plants which have specific processes for automotive applications.

Chapter 4

# Quality improvements

In this chapter a few measures to increase the quality of the product are discussed. The requirements are not found in any standard studied in this thesis but semiconductor suppliers to the automotive industry sometimes use them since they reduce the number of test escapes and increase the overall quality of the product.

## 4.1 Bad neighborhood screening

In order to decrease the number of dies shipped with latent defects a neighbor screening algorithm was implemented. The effect on PGD if all dies with a given number of bad neighbors were discarded was analyzed. The result is shown in figures 4.1, 4.2 and tables 4.1, 4.2.

As seen in figure 4.1 the PGD decreases significantly for dies with three or more bad neighbors. At the same time the risk of test escapes increases drastically, which is shown in table 4.2. Since the fraction of dies that have more than two bad neighbors is very small, the dies with more than two bad neighbors could be scrapped with any major economic impact. This is illustrated in table 4.1

| Neighbor limit | PGD (%) | Yield (%) | Yield drop (%) |
|---|---|---|---|
| 0 | 97.852 | 83.484 | 13.996 |
| 1 | 97.643 | 96.079 | 1.401 |
| 2 | 97.613 | 97.309 | 0.171 |
| 3 | 97.572 | 97.445 | 0.035 |
| 4 | 97.548 | 97.475 | 0.005 |
| 5 | 97.529 | 97.480 | 0.000 |

**Table 4.1:** Neighbor screen - yield analysis

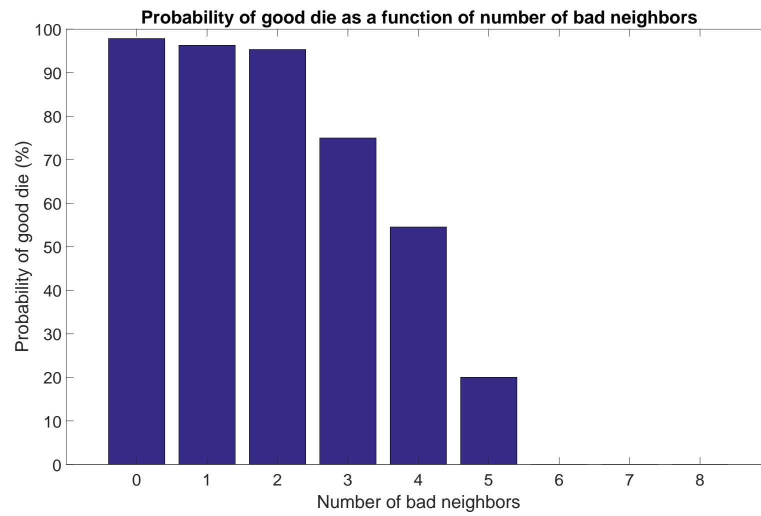


**Figure 4.1:** Probability of good die as a function of defect neighbors.

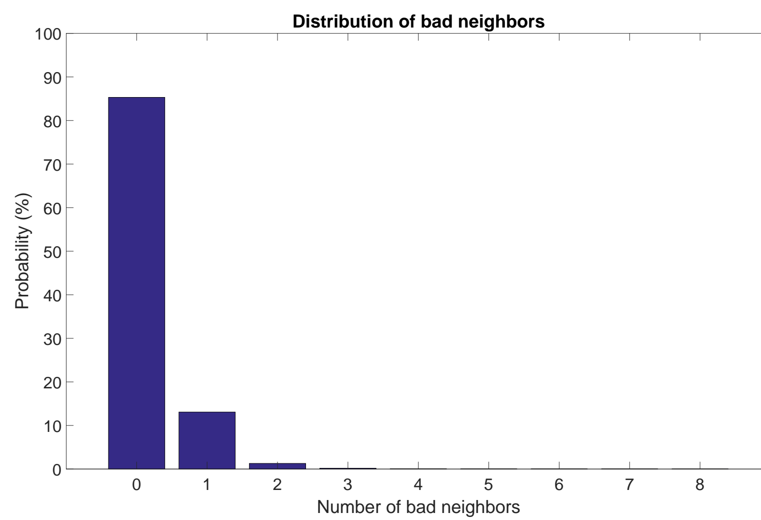


**Figure 4.2:** Distribution of bad neighbors.

| Limit (N) | PGD ∣ X <= N (%) | PGD ∣ X > N (%) | DPPM impact |
|---|---|---|---|
| 0 | 97.852 | 95.316 | 2.239 |
| 1 | 97.643 | 87.461 | 5.939 |
| 2 | 97.613 | 54.839 | 33.678 |
| 3 | 97.572 | 26.923 | 109.083 |
| 4 | 97.548 | 6.667 | 557.045 |

**Table 4.2:** Neighbor screen - test escape analysis

## 4.2 Removal of dies on the wafer edge

As seen in figure 4.3 the PGD is higher in the interior of wafer than on the wafer edge. There is a substantial difference, 98.2% of the dies in the interior pass the production tests and only 93.5% of the dies on the wafer edge pass the tests. Using equation 2.2 the risk of a test escape 2.6 times more likely for dies on the wafer edge compared to dies in the interior. However, removing all the dies on the wafer edge will contribute to a significant revenue loss. Assuming that each die is sold for $2 and there are 100 dies on the wafer edge removing the dies on the edge will add up to a revenue loss of $200 *for each wafer!* This revenue loss will most likely not be acceptable unless it is a direct requirement from a customer which then will motivate a higher component price.

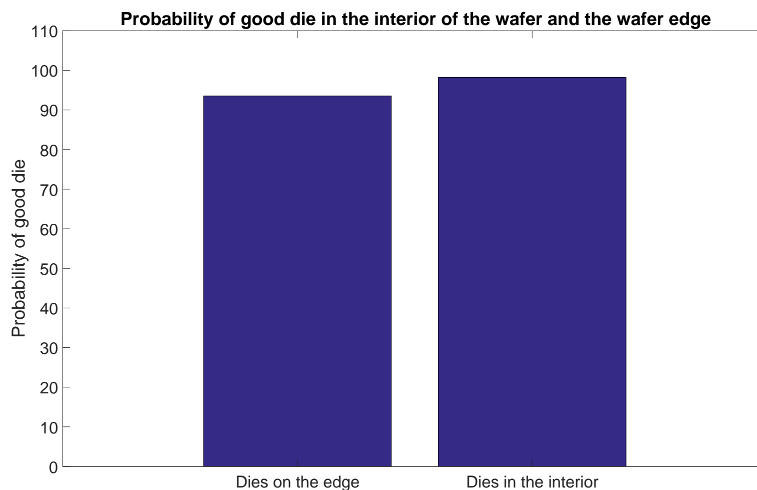


**Figure 4.3:** PGD on the wafer edge.

## 4.3 High temperature production testing and burn in

As discussed earlier exposure to high temperatures accelerates failure mechanisms and can cause weak chips to fail. It has also been discussed that the early

life failure rate is substantially higher than the failure rate in the operational phase. Two actions that could decrease the risk of early failures in the field and increase the quality of the product are high temperature production testing and burn in tests.

No such production test are not required by any of the standards covered by this thesis report. Burn-in testing is suggested by ISO 26262 for the most safety critical systems in the vehicle. However, there may be customer requirements which make such test necessary. One could also argue that if a new product is launched for automotive applications then burn in testing could be used for a limited time until it is verified that the process is stable. On the other hand, one could also argue that since the design is proven in the consumer electronic industry with no known early lifetime failure issues then the design is good enough to omit high temperature- and burn in testing.

## 4.4 Customer specific requirements

The quality improving schemes discussed in this chapter are not required by any standard studied in this thesis work. However, there is a possibility that some automotive customers would like to have some of the discussed quality improvement schemes in the production test set, e.g. burn in testing. Since development of test programs is costly and time consuming there might a problem if every automotive customer want to have a unique test program. Also, administering all the test programs to different customers will be a nuisance.

It is therefore important to chose a production test set that is large enough and demonstrates high reliability without adding excessive test cost. In order to be able to target a large segment in the automotive industry, a survey of the customer specific requirements must be made.

# Chapter 5
# Discussion

In this chapter a pending launch in the automotive industry is discussed.

## 5.1 The automotive business case

As seen in the previous chapters there are several requirements in the automotive industry that Fingerprints Cards AB has to adapt to if an introduction in the automotive industry is desirable. Adapting to such requirements will most likely lead to revenue losses due to an increase in scrapped dies, but in return the product quality will probably be higher. However, adapting to the automotive requirements for the consumer electronic business line will lead to unjustifiable cost increases.

A more sensible approach would be to launch an automotive version of an existing product, providing that the design is sufficiently testable. This product would be qualified according to AEC-Q100 and more thoroughly tested in production than the consumer electronic version. Since a existing product will be used and it has not been developed in accordance to ISO 26262 and ISO/TS 169494 it must not be integrated into safety critical systems.

If the automotive launch of the existing product is successful, Fingerprint Cards AB could opt to certify the organization in accordance to ISO/TS 16949 and ISO 26262 in order to qualify the product for use in safety critical applications. This would most likely have a major impact on operations since almost every department in the company would be affected by such certifications. This would include starting doing Failure Mode and Effect Analysis (FMEA) in the development process of the products as well as implementing automotive quality management systems.

The extensive certification work has to be put in relation to the size of the potential market. The statistics of the amount of cars produced each year differ a bit depending on the source but it can be assumed that 70 million cars are produced each year. Even if the launch is well accepted by the market and the technology penetration of 50% is achieved within five years and Fingerprint Cards AB secures a large market share the yearly volumes in the automotive industry will equal a months volume of the consumer electronic business line. If the launch is to be economically successful the margin must be high enough to cover qualifi-

cation cost for both AEC-Q100 and customer specific requirements as well as the yield reduction due to quality improving measures.

The positive aspects of an expansion to the automotive industry are obvious. Fingerprint Cards AB has a possibility to be first to market which provides an opportunity to secure a large market share. Also, if Fingerprint Cards AB succeeds in being first to market it will be possible to sell products at a better margin. In the long run it is also possible that several fingerprint sensors are integrated in each vehicle. This would of course strengthen the incentives to enter the automotive market.

## 5.2 Further work

This thesis work was intended as a pilot study in the automotive requirements. Some 'action points' have been identified for compliance with the automotive requirements. The action points are shown below

- Implement Part Average Testing in production
- Implement Statistical Bin and Yield Analysis in production
- Develop AEC-Q100 grade test software alternatively do a fault coverage analysis of functional tests in order to meet test coverage requirements.
- Do relevant AEC-Q100 qualification tests with the approved software
- Look into customer specific requirements such as removal of dies with bad neighbors, dies on wafer edge etc. Implement these requirements in production test software
- Create a task group to investigate observability of the ASIC and add observation flip flops in critical nodes. This will increase the fault coverage of the scan testing.

The consequences of implementing these actions have been discussed in the thesis report but a substantial amount of work remain in the implementation of these schemes in production.

If the introduction is successful then a product for safety critical applications could be developed. This would require certification according to ISO/TS 16949 and ISO 26262.

# References

[1] Tim Kelly Alejandra Ruiz, Alberto Melzi. *Systematic application of ISO 26262 on a SEooC: Support by applying a systematic reuse approach*. Design, Automation & Test in Europe Conference & Exhibition. IEEE, 2015.

[2] Dale Grosch* Anne Gattiker, Phil Nigh* and Wojciech Maly. *Current Signatures for Production Testing*. Digest of Papers 1996 IEEE International Workshop on IDDQ Testing. IEEE, 1996.

[3] R.J. Baker. *CMOS: Circuit Design, Layout, and Simulation*. IEEE Press Series on Microelectronic Systems. Wiley, 2011.

[4] Duane Boning and James Chung. *Statistical Metrology: Tools for Understanding Variation*. Future Fab International, 1996.

[5] Agrawal & Bushnell. *Design for testability - Theory and Practice. Sequential ATPG*. Integrated Circuit Engineering Corporation, 2001.

[6] Phil Nigh Chao-Wen Tseng Ray Chen and Edward J. McCluskey. *MINVDD Testing for Weak CMOS ICs*. VLSI Test Symposium. IEEE, 2001.

[7] Automotive Electronics Council. *Fault Simulation and Fault Grading*. AEC, 2007.

[8] Automotive Electronics Council. *Guidelines for part average testing*. AEC, 2011.

[9] Automotive Electronics Council. *Guidelines for statistical yield analysis*. AEC, 2012.

[10] Automotive Electronics Council. *AEC Q100 Rev - H: Failure Mechanism Based Stress Test Qualification For Integrated Circuits*. AEC, 2014.

[11] Organización Internacional de Normalización. *ISO 26262: Road Vehicles : Functional Safety*. ISO, 2011.

[12] Organización Internacional de Normalización. *Quality management systems — Particular requirements for the application of ISO 9001 for automotive production and relevant service part organizations*. ISO, 2016.

[13] Bautista et al. *AEC Workshop Session - Known good die/MultiChipModule*. Automotive Electronics Council, 2015.

[14] Robert BOSCH GmbH. *Design Requirements for Automotive Reliability*. Robert BOSCH GmbH, 2006.

[15] P.R. Gray. *Analysis and Design of Analog Integrated Circuits*. Analysis and Design of Analog Integrated Circuits. John Wiley & Sons, 2009.

[16] M. Hayashi. Semiconductor apparatus and method of disposing observation flip-flop, October 18 2011. US Patent 8,042,014.

[17] Eckhardt Holz. *Practical Issues in Safety Critical Component Reuse in the Automotive Industry*. KPIT, 2013.

[18] JEDEC. *JEDEC Standard - Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress*. JEDEC, 2001.

[19] JEDEC. *JEDEC Standard - Procedure for the Wafer-Level Testing of Thin Dielectrics*. JEDEC, 2001.

[20] JEDEC. *JEDEC Standard - Standard Test Structures for Reliability Assesment of AlCu Metallizations with Barrier Materials*. JEDEC, 2001.

[21] JEDEC. *Failure Mechanism and Models for Semiconductor Devices*. JEDEC, 2016.

[22] Sandip Kundu. *IDDQ Defect Detection in Deep Submicron CMOS ICs*. Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian. IEEE, 1998.

[23] Ramon Leon. *Unit 18: Accelerated Test Models*. Stat 567. University of Tennessee, Knoxville, 2004.

[24] United States. Department of Defense. *Military Handbook: Electronic reliability design handbook*. U.S. Department of Defense, 1988.

[25] Seokjin Kim ; Martin Peckerar. *High-speed ADC dynamic performance validation: The impact of skew-corner lot testing*. Autotestcon. IEEE, 2008.

[26] L. Peters, J. Griffin, Integrated Circuit Engineering Corporation, and R.D. Skinner. *Cost Effective IC Manufacturing*. Integrated Circuit Engineering Corporation, 1995.

[27] Erik Jan Marinissen; Adit Singh; Dan Glotter; Marco Esposito; John M. Carulli Jr. Amit Nahar; Kenneth M. Butler; Davide Appello; Chris Portelli. *Adapting to Adaptive Testing*. Design, Automation & Test in Europe Conference & Exhibition. IEEE, 2010.

[28] Rajesh Raina. *Achieving Zero-Defects for Automotive Applications*. IEEE, 2008.

[29] Rochit Rajsuman. *Iddq Testing for CMOS VLSI*. Proceedings of the IEEE. IEEE, 2002.

[30] G.W. Roberts, F. Taenzler, and M. Burns. *An Introduction to Mixed-Signal IC Test and Measurement*. The Oxford series in electrical and computer engineering. Oxford University Press, 2011.

[31] R. Madge; B. Benware; R. Turakhia; R. Daasch; C. Schuermyer; J. Ruffler. *In search of the optimum test set - Adaptive test methods for maximum defect coverage and lowest test cost*. Test Conference, 2004. Proceedings. ITC 2004. International. IEEE, 2004.

[32] L. Scheffer, L. Lavagno, and G. Martin. *EDA for IC System Design, Verification, and Testing*. Electronic Design Automation for Integrated Circuits Hdbk. CRC Press, 2016.

[33] Alpha & Omega Semiconductor. *Power semiconductor Reliability handbook*. Alpha & Omega Semiconductor, 2010.

[34] Oguz Yava Ernst Richter Christian Kluthe Markus Sickmoeller. *Wafer-edge yield engineering in leading-edge DRAM manufacturing*. Fabtech, 2009.

[35] Adit Singh. *Statistical adaptive test methods targeting "zero defect IC quality and reliability*. International Test Conference. IEEE, 2015.

Printed by Tryckeriet i E-huset, Lund 2017

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