Lund University

Master Thesis

Simulation and TLM studies of vertical nanowire devices

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A thesis submitted in fulfilment of the requirements for the degree of Master of Science in the

Nanoelectronics Group
Department of Electrical and Information Technology
Faculty of Science, Lund University

May 2017

LUND UNIVERSITY

Abstract

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by Albin Linder

Vertical nanowire field effect transistors (NWFETs) have in this diploma work been studied in order to examine possible benefits of introducing a highly doped shell around the nanowire channel. It could be concluded that this new device geometry significantly enhances DC performance metrics. It does however also introduce an additional potential drop which may be large enough to reduce device stability. Having the newly introduced shell at the bottom of the nanowire is seen to be best operated in a bottom ground configuration. Transmission line method (TLM) measurements were also conducted on nanowire resistors where molybdenum was observed to potentially be a more suitable contact metal to InAs and InGaAs NWs compared to tungsten.

Acknowledgements

Before I present my thesis that I've been working on this last year, I would like to express my gratitude to the people who have been helping me out throughout this project. First and foremost, I would like to thank my main supervisor Lars-Erik Wernersson for his expertise and continuous support. Discussing the project with you was always really motivating and you constantly gave me new points of view when tackling all of the problems I came across. I would then like to thank Dan Hessman, my senior supervisor, for accepting my project and teaching me the fundamentals of solid state physics. Your calm and pedagogical way of teaching made me think that this field in physics is really exciting. The third person I would like to thank is my practical coach Olli-Pekka Kilpi, whom I have spent the most time with during this work, both in the clean room and in front of the computer. It has been inspiring to work with you and you've taught me that it is better to focus on things you've accomplished rather than all the problems you encounter, which I think is a wonderful philosophy that is applicable in every day life.

I would also like to thank all the other phenomenal people at the Nanoelectronics group for being so welcoming and friendly. By simply attending the weekly meetings, you made me feel like a member of the group and like I was involved in all your research. I was also lucky enough to share the same office as the other Masters students in the group, namely Andreas, Christian, Daniel, Edvin, George and Lun. Together, you guys really made the office a pleasant and fun work environment to be in, and I would therefore like to thank you all!

On a more personal note, I would like to thank my girlfriend, all my friends and my family for always sticking up with me. And still after all these years, you still try to convince me that I'm smart, and for that I'm truly grateful. Thank you!

/ *Albin Linder*, May 2017

Contents

Abbreviations

DC	Direct Current
EOT	Equivalent Oxide Thickness
FET	Field-Effect Transistor
FP	Field Plate
GAA	Gate-All-Around
HEMT	High Electron Mobility Transistor
HSQ	Hydrogen Silsesquieoxane
InAs	Indium Arsenide
InGaAs	Indium Gallium Arsenide
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOVPE	Metal Organic Vapour Phase Epitaxy
NW	Nanowire
NWFET	Nanowire Field-Effect Transistor
RGB	Red-Green-Blue
RIE	Reactive Ion Etch
SCE	Short Channel Effect
SEM	Scanning Electron Microscopy
Si	Silicon
SiO_2	Silicon Dioxide
TMAH	Tetramethylammonium Hydroxide
TLM	Transmission Line Method
UVL	Ultra Violet Lithography
VLS	Vapour-Liquid-Solid

Chapter 1

Introduction

Semiconductor technology has throughout many decades been researched and great advancements have continuously been made in terms of device material, cost reduction, efficiency etc. As for *metal oxide semiconductor field effect transistors* (MOSFETs), the industry has for a long time been focusing on downscaling conventional *silicon* (Si) based devices according to Moore's law [1], which states that the number of transistors on a chip increases exponentially. This approach has worked very well and the processing costs for densely packed Si MOSFETs have continuously been reduced whilst at the same time the performance of the devices has been improved. However, it is well known that infinite downscaling of Si based MOSFETs is not plausible and that the industry already seems to be pushing the physical limits of these devices. In order to further downscale MOSFETs and improve the performance of them, scientists have been developing MOSFETs with new materials, inherently superior to Si in various aspects, as well as derived completely new device geometries in order to enhance performance in numerous ways e.g. by obtaining better electrostatic gate control using a *gate-all-around* (GAA) design. The industry currently also utilizes *high-κ* (high dielectic constant) materials and multigate structures to extend Moore's law.

In this introductory chapter, a brief background to what MOSFETs are and how they work will be given. The motivation behind the project will also be stated together with a description of the thesis layout.

1.1 MOSFETs

MOSFETs consist of several parts; a semiconducting body (constituting the *channel*) connected to two conducting leads (called *source* and *drain* respectively). The channel is then covered by an insulating oxide to which a third lead, called the *gate*, is put. Biasing the gate alters the electrostatic potential inside the channel which further enables (or disables) an electric current flowing from source to drain through the channel.

In order to understand how this works, knowledge in solid state physics is required. Here some fundamentals will briefly be given, but for a more thorough explanation of the subject, please see [2], [3], and [4].

In a crystalline solid, so called *energy bands* are formed when isolated atoms are brought together. Degenerate electron states of the atoms constituting the solid will then split into continuous energy bands. The last filled energy band is known as the valence band, and the first non-filled band is the conduction band. The energy difference between the top of the valence band and the bottom of the conduction band is called the *band gap*, see Fig. 1.1 (a). There are no states for the electrons to occupy inside the band gap.

The *Fermi level* is defined as the energy where the probability for an electron to occupy a state is exactly one half [2]. For an intrinsic (undoped) semiconductor, the Fermi level, $E_{\mathrm{F},i}$, lies inside the band gap. However, by introducing *donor* impurities to the lattice, the Fermi level is elevated to a higher energy, $E_{\mathrm{F},n}$, and the solid gets *negatively*-doped (n-doped). Analogously, the Fermi level is lowered to $E_{\mathrm{F},p}$ if the solid is doped with *acceptor* impurities, also depicted in Fig. 1.1 (a).

A current, I_{ds}, through the channel in a MOSFET can be attained by applying a voltage, V_{ds}, between the drain and source. The channel then resembles a resistor. But the amplitude of I_{ds} can further be regulated using the present *metal-oxide-semiconductor-capacitor* (MOS-capacitor) in the device by biasing the gate. This may raise or lower the potential barrier in the gated channel depending on the sign of the applied voltage. The potential barrier originates from differences in *work-functions* between the gate metal and the semiconductor channel [2], where the bands in the channel bend. How the current is amplified by the channel is schematically depicted in Fig. 1.1 (b), where a certain voltage has to be applied to the gate in order to turn the transistor on.

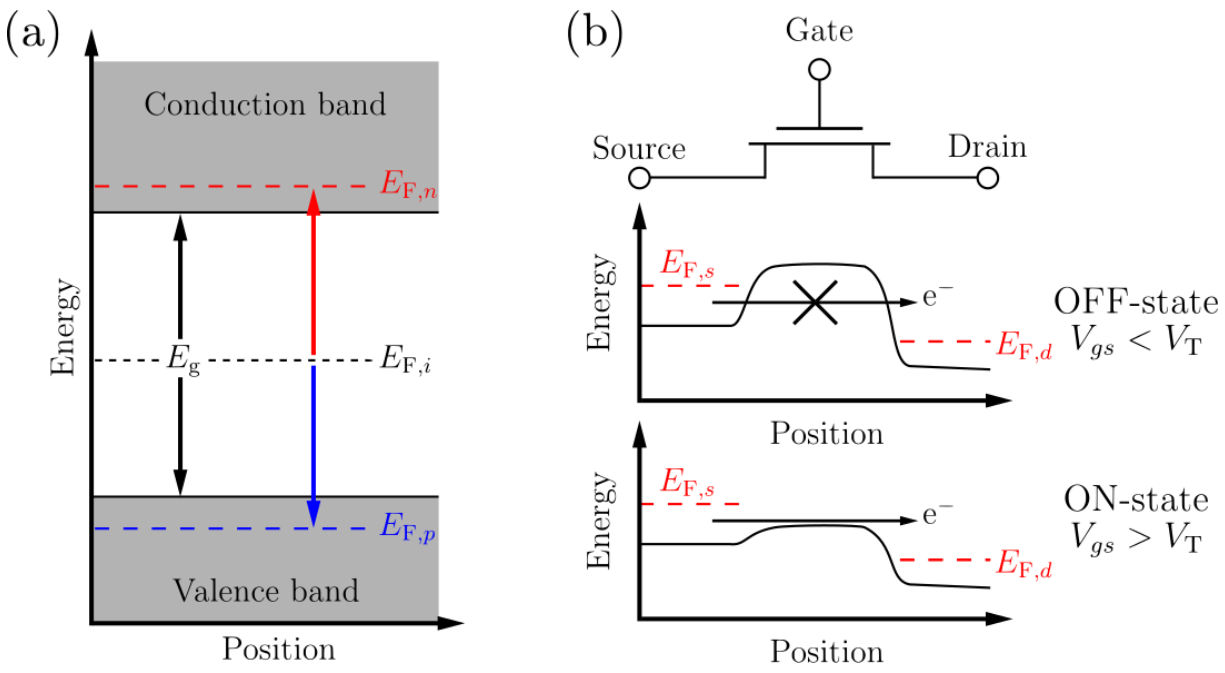

FIGURE 1.1: The conductance- and valence band of a solid is shown in (a) separated by the band gap energy E_g. The Fermi level of the solid can be seen to shift depending on the impurity doping, where $E_{F,i}$ is the intrinsic (undoped) Fermi level. Having the material n-doped raises the Fermi level as seen by $E_{F,n}$ while p-doping it will lower the Fermi level shown by $E_{F,p}$. The conduction band along the channel of a MOSFET is shown in (b) where a drain-source voltage is applied which separates the Fermi levels in the source ($E_{F,s}$) to the drain ($E_{F,d}$). The gate-source voltage, V_{gs} has to exceed a certain threshold voltage, V_T, in order to lower the potential barrier for an electron in the conduction band to go from source to drain. Applying V_T to the gate thus turns the MOSFET on.

1.2 Motivation behind the project

III-V materials are very versatile as different compounds can be combined in various desirable compositions changing their intrinsic properties. By combining indium (group III) with arsenic (group V), the semiconducting compound *indium arsenide* (InAs) can be formed. An attractive feat of InAs is that it has superb electron mobility μ_n of around 33000 cm^2/Vs, compared to Si which has $\mu_n \approx 1500$ cm^2/Vs [5]. As μ_n is a measure of how strongly an electron is influenced by an applied electric field, the parameter becomes important for carrier transport [2]. A high mobility further implies a long *mean free path*, which is crucial for *ballistic* transistors where no scattering occurs in the channel.

However, III-V materials are unfortunately rare compared to Si and therefore also expensive in comparison. On top of that, compared to Si, III-V technology is less matured and

the III-V wafers are small and brittle [6]. Consequently, it is impractical to manufacture pure III-V devices and a demand to co-integrate III-Vs on Si-substrates has arisen.

Evidently, as III-V materials are expensive, it is preferable to use as little resources as possible when processing III-V devices in order to keep costs at a minimum. For that reason, bottom up processed vertical *nanowires* (NWs) using the *vapour-liquid-solid* (VLS) method, is a convenient choice in device geometry as the low dimensions of the structures do not require excessive material consumption. Another advantage of the vertical NW geometry is that they can be grown on lattice mismatched substrates because the induced strain can easily be relaxed by lateral expansion [7]. This is a major selling point as the lattice mismatch between III-V and Si otherwise makes co-integration challenging. Being able to stack NWFETs vertically is also advantageous as it decouples the gate length from the device footprint which enables dense packing on a small area whilst maintaining relatively long gates lengths [8].

Because of *short channel effects* (SCEs), the overall performance for future, ultrascaled FETs will be dominated by the contact resistances [9]. It is therefore crucial to optimize the source and drain regions to minimize their contact series resistance. This problem serves as the main reason for the second part of this diploma work.

1.3 The report

This project has been devoted to optimize vertical III-V *nanowire field effect transistors* (NWFETs) by two seemingly different approaches. Firstly, a simulation software was used in order to freely probe various parameters of the device and examine their caused effects. Secondly, an experimental study has been conducted to optimize for the contact metals in vertical InAs and InGaAs NW resistors.

Like the project itself, the report is also divided into two parts to make it more concise and readable. The necessary theory of the whole project will be given in the theory chapter but the two parts will later have their own separate chapters of how they were conducted, as well as their own results and discussion chapters. In the final chapter entitled “conclusions and outlook”, there will be a short summary of the project and remaining research in device optimization in terms of simulations and extrinsic resistances will be highlighted.

The first part, in which vertical InAs NWFETs were simulated, aimed to give insight into how the potential and electric field inside the channel is affected by a new transistor geometry. Changes in the output and transfer characteristics of the device were also inspected.

In the second part of the project, *transmission line method* (TLM) measurements were conducted on vertical NW resistors. Four samples were processed; two with InAs NWs, and two with $In_{0.2}Ga_{0.8}As$ NWs. *Molybdenum* (Mo) and *tungsten* (W) were compared as contact metals to determine which one is best suited for the respective semiconductor material.

Chapter 2

Theory

Simulation tools have supported the advancements of nanoscale transistors immensely. By simulating a device in a realistic fashion, knowledge about the intrinsic and extrinsic properties of it can be extracted without extensive and/or expensive experimental work. Simulations also have the ability to depict the band structure at any given point in a device. It is also possible to plot how it is affected by various parameters such as electrical fields and local doping concentration variations. There are of course numerous other advantageous benefits for complementing and comparing experimental research with simulations. In this project, a device simulation program called Atlas, developed by Silvaco, was used. All of the equations in this chapter regarding the used simulation models were taken from the Atlas users manual [10].

It is important to be able to extract the specific contact resistivity in vertical NWFETs. The reason for this is because the performance of NWFETs are thought to ultimately be limited by extrinsic resistances when these small devices get further downscaled. Although it is a difficult task to measure the specific contact resistivity in NWFETs, it is possible to do it by using the principles from conventional planar TLM. A description behind the basics of TLM and how it can be applied to vertical NWs will be given in this chapter.

2.1 Simulations

2.1.1 Atlas physics

By linking together a set of fundamental equations governing the electrostatic potential and the carrier statistics within a simulation domain, Pinto et al were able to develop a simulation program called PISCES-II in 1984 [11]. The same set of equations is used in Atlas and is originally derived from Maxwell's laws. These equations consists of Poisson's equation, the continuity equations and the equations for carrier transport. Poisson's equation describes how the electrostatic potential varies with local charge densities, while the continuity and transport equations expresses how the carriers are influenced by transport-, generation- and recombination processes.

2.1.2 Poisson's equation

As previously mentioned, Poisson's equation relates the electrostatic potential ψ to the space charge density ρ, which is the algebraic sum of the charge carrier density and the ionized impurity concentrations. The equation is given by

$$\mathrm{div}(\varepsilon \nabla \psi) = -\rho \tag{2.1}$$

where ε is the local dielectric permittivity. The divergence operator and the gradient operator ∇ in the above expression is, for an arbitrary vector $\vec{F}$, defined as

$$\mathrm{div}(\vec{F}) = \nabla \cdot \vec{F} = \left(\frac{\partial}{\partial x}, \frac{\partial}{\partial y}, \frac{\partial}{\partial z}\right) \cdot \vec{F} = \frac{\partial \vec{F}}{\partial x} + \frac{\partial \vec{F}}{\partial y} + \frac{\partial \vec{F}}{\partial z} \tag{2.2}$$

The electric field is further given as the gradient of the potential:

$$\vec{E} = -\nabla \psi \tag{2.3}$$

2.1.3 Continuity equations

The time evolution of electron and hole concentrations, n and p respectively, are given by the continuity equations below. For electrons the expression is [2]

$$\frac{\partial n}{\partial t} = \frac{1}{q}\text{div}(\vec{J_n}) + G_n - R_n \tag{2.4}$$

where t is time, q is the elementary electron charge, $\vec{J_n}$ is the electron current density, G_n is the generation rate of conduction band electrons and R_n is the recombination rate of them. For holes, due to the opposite sign of charge, the corresponding equation becomes

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\text{div}(\vec{J_p}) + G_p - R_p \tag{2.5}$$

where $\vec{J_p}$, G_p and R_p are the hole current density, hole generation rate and hole recombination rate respectively.

2.1.4 Drift-Diffusion transport model

Equation (2.1), (2.4) and (2.5) are fundamental in device simulations. But in order to describe the ingoing parameters in these equations, such as $\vec{J}_{n/p}$, $G_{n/p}$ and $R_{n/p}$, additional equations are needed. In this project, the *drift-diffusion* model was used as the charge carrier transport model.

An electric field will exert a force upon the free carriers in a semiconductor as they are electrically charged. Electrons will experience a force in the opposite direction of the field as they are negatively charged, and holes will be subjected to a force along the field due to their positive charge. The current generated in this way is called the *drift current*. Furthermore, if the impurity doping in the semiconductor varies spatially, there will be a spatial variation in the free carrier concentration as well. The carrier concentration gradient will also generate a current, called *diffusion current*, in the semiconductor as carriers tend to move from regions of high concentration to regions of low concentration [2].

2.1.5 Mobility models

When a charge carrier is accelerated in an electric field $\mathscr{E}$, it gains an additional component to its velocity called the *drift velocity* v_{d}. The mobility is the proportionality factor between the drift velocity and the electric field given as $\mu = -v_{\mathrm{d}}/\mathscr{E}$. As mentioned in the introduction, the μ is an important parameter in semiconductor physics as it describes how the motion of a charge carrier is influenced by an electric field. The mobility is further defined as the product of the elementary charge q and the mean free time τ_c between collisions divided by the effective mass m_n, i.e.,

$$\mu_n \equiv q\tau_c/m_n. \tag{2.6}$$

Although this relation seems simple at first glance, τ_c and m_n are themselves dependent on other variables making mobility calculations more complex. The mean free time is for instance dependent on the temperature of the solid as well as the impurity doping of it [2]. However, in this diploma work the only variable for mobility modelling that will be considered is the parallel electric field E [12]. The model `fldmob` used to calculate the mobility is given by

$$\mu_n(E) = \mu_{n0}\left[\frac{1}{1+\left(\frac{\mu_{n0}E}{v_{\mathrm{sat}}}\right)^{\beta}}\right]^{1/\beta} \tag{2.7}$$

where μ_{n0} is a fixed low field electron mobility, v_{sat} is here considered to be a fixed saturation velocity and β is a fitting parameter.

Furthermore, the carrier concentration in the simulations were determined by the Fermi-Dirac function which calculates the probability $f(\epsilon)$ of an electron occupying a state of energy ϵ as

$$f(\epsilon) = \frac{1}{1+\exp\left(\frac{\epsilon - E_F}{kT_L}\right)} \tag{2.8}$$

where E_F is the Fermi level, T_L is the lattice temperature and k is the Boltzmann constant [10]. If the Fermi level lies in the middle of the bandgap $\epsilon - E_F << kT_L$, a simplification of the above expression can be used known as Maxwell-Boltzmann distribution. This is however not possible if the semiconductor is heavily doped since the Fermi level then either

gets raised above or close to the conduction band edge if negatively doped, or lowered to the valance band if positively doped. In these instances, Eq. (2.8) has to be used.

2.2 MOSFET DC performance metrics

Besides MOSFETs, there are plenty of other types of transistors, each with advantages and disadvantages. Therefore, in order to compare them to each other, various benchmarking parameters have to be established. By benchmarking new nanoelectronic devices to their Si counterparts, nanotechnology research has been accelerating and it is thus important to continue comparing devices through benchmarking [15]. In order to benchmark different transistors, various performance metrics first have to be extracted.

In this project, *direct-current* (DC) performance metrics will be deduced from *current-voltage*-characteristics (IV-characteristics). Considering a common source configuration, the drain current, I_d, is dependent on the applied gate-source voltage, V_{gs}, as well as the drain-source voltage, V_{ds}. This dependency can be displayed in two different IV-characteristics; the *output characteristics* where V_{gs} is kept constant and I_d depends on V_{ds}, and *transfer characteristics* where V_{ds} instead is kept constant sweeping over V_{gs}. How some of the important metrics can be extracted from these curves will be described in this section.

2.2.1 Mutual transconductance

An important metric for MOSFETs is the mutual transconductance, g_{m}, which is defined as the partial derivative of I_d with respect to V_{gs} for a fixed V_{ds} as

$$g_{\mathrm{m}} \equiv \frac{\partial I_d}{\partial V_{gs}}. \tag{2.9}$$

This is essentially the slope of the transfer characteristics curve, showing how much I_d is amplified by increasing V_{gs}. It is favourable to have a steep slope which gives a high g_{m}. For digital applications, high g_{m} enables a lower supply voltage, V_{dd}, for maintaining a certain drive current, which makes the device more energy efficient. Plotting g_{m} against

V_{gs} shows that there will be a peak value of g_{m} usually denoted $g_{\mathrm{m,max}}$, as shown in Fig. 2.1 (a).

2.2.2 Threshold voltage

On a linear scale, a certain V_{gs} has to be applied to the gate before an increase in I_d can be observed, which marks the transition of switching the device on. In conventional MOSFETs, this *threshold voltage*, V_{T}, is where strong inversion occurs opening up the channel for minority charge carriers [2]. However, for the NWFETs considered in this work, the channel current is constituted of majority carriers and this definition of V_{T} therefore no longer applies as no inversion of carriers takes place. Instead, V_{T} is here extracted from a linear extrapolation of the current as a function of V_{gs} giving $I_d = 0$. The anchor point for the extrapolation is set where V_{gs} gives $g_{\mathrm{m,max}}$, as seen in Fig. 2.1 (a).

2.2.3 Sub-threshold swing

Another performance metric deducible from transfer characteristics curves is the *sub-threshold swing*, S. For V_{gs} smaller than V_{T}, I_d increases exponentially with V_{gs} and will therefore show a linear slope if plotted on a logarithmic scale, see Fig. 2.1 (b). This slope is called the *sub-threshold slope* and its reciprocal value gives S. The sub-threshold swing is a measure of how sharply a transistor turns off by V_{gs}, and is given by the gate voltage needed to induce a drain current difference of one magnitude. This metric is particularly important in digital logic and memory applications in low-voltage and low-power devices [2]. Also notable is that S, is modelled as a thermionic injection over a potential barrier which, in an ideal case, gives a value of 60 mV/decade at room temperature [17].

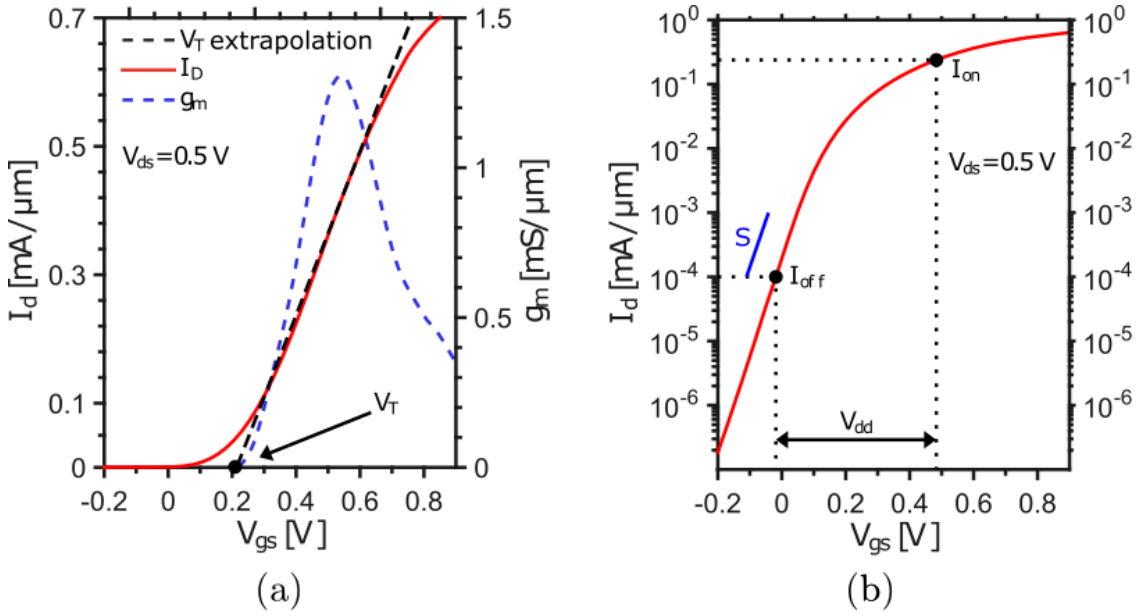

FIGURE 2.1: Transfer characteristics curves with (a) linear y-axis and (b) logarithmic y-axis. The transconductance is also plotted in (a) where the extrapolation of V_{T} is anchored at $g_{\mathrm{m,max}}$. In (b) the sub-threshold regime is shown where S is measured. Also shown is the *on-current*, I_{on}, which is the current obtained by applying V_{dd} from the gate voltage giving the *off-current*, I_{off}, of 100 nA/μm.

2.3 Standard TLM

TLM is a technique used to calculate the specific contact resistance ρ_{c} between a semiconductor and an ohmic contact. The technique is a convenient way to characterize the contact quality and the standard set-up is schematically shown in Fig. 2.2. A semiconductor material is fabricated on an insulator and two metal contacts are defined on top of the semiconductor. This structure forms a series of resistors where the total resistance R_{tot} is the sum of the resistance in the two contacts R_{c} and the resistance in the semiconductor R_{s}

$$R_{\mathrm{tot}} = 2R_{\mathrm{c}} + R_{\mathrm{s}} \tag{2.10}$$

The technique was first demonstrated for planar ohmic contacts by Shockley in 1964 [18] and it relates the total resistance R_{tot} between two contact to the distance L between them. The method also enables characterization of other material parameters such as the transfer length L_{T} and the semiconductor resistivity ρ_{s}. The transfer length is a measure of how deep the electrons travel underneath the contact before being swept up into it. It

is given as the distance where $1 - e^{-1} \approx 0.63\%$ of the total semiconductor current goes into the contacts [17]. By multiplying L_T with the width of the semiconductor (and hence also the contact) W_s, the effective contact area is given as $A_c = L_T W_s$. In Fig.2.2, a schematic of the explained structure is shown.

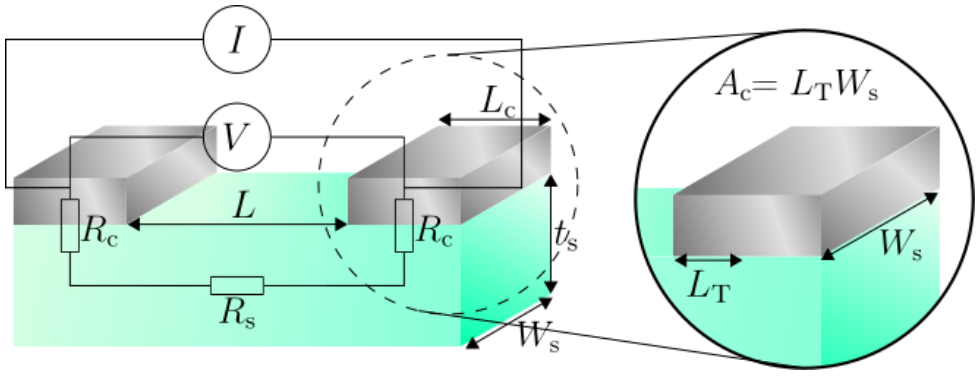

FIGURE 2.2: Schematic view of a semiconductor resistor with two contacts. A current goes through the circuit and the voltage over the semiconductor is measured to extract the resistance.

For a planar structure, such as in Fig. 2.2, the resistance of the semiconductor is given by [19]

$$R_s = \frac{\rho_s L}{W_s t_s} \tag{2.11}$$

where t_s is the thickness of the semiconductor. If ρ_s is assumed to be constant and the semiconductor cross-section $W_s t_s$ the same, it is easy to see that the resistance is linearly dependent on L. Therefore, by differentiating the above expression, the following is obtained

$$\frac{\partial R_{tot}}{\partial L} = \frac{\rho_s}{W_s t_s} \tag{2.12}$$

The contact resistance R_c is independent on L and can be calculated by the following expression [20]

$$R_c = \frac{\rho_s L_T}{W_s t_s} \coth\left(\frac{L_c}{L_T}\right) \tag{2.13}$$

where L_c is the contact length. As the function $\coth(x)$ converges to 1 for large x, the contact resistance where $L_c >> L_T$ can be simplified to

$$\lim_{L_c \to \infty} R_c = \frac{\rho_s L_T}{W_s t_s} \tag{2.14}$$

The specific contact resistivity ρ_c is defined as the contact resistance over the contacted area for a infinitesimal thin interface, i.e., $\rho_c = R_c A_c$. This implies that if the contact length is long enough ($L_c >> L_T$), Eq. (2.14) is valid and ρ_c can be calculated as

$$\rho_c = \frac{\rho_s L_T^2}{t_s}. \tag{2.15}$$

If R_{tot} is plotted as a function of L, ρ_s can be extracted from the slope of the linear fit as shown in Fig. 2.3. By extrapolating the fit to $L = 0$, the contact resistance can be determined as the second term in Eq. (2.10) vanishes.

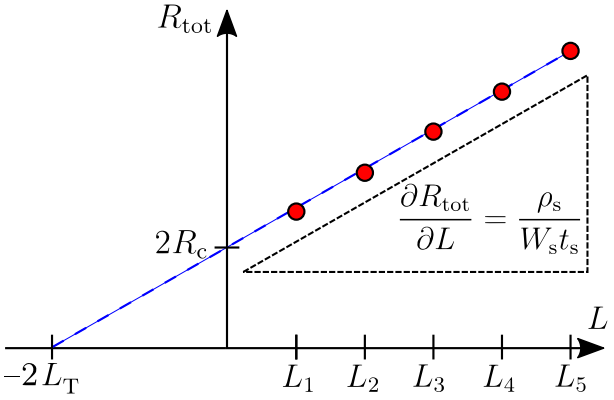

FIGURE 2.3: Depiction of a typical TLM plot. The measured resistance, shown as red dots are plotted against the contact separation. With a linear fit it is possible to extrapolate down to both $L = 0$ and $R_{tot} = 0$, which gives R_c and L_T respectively. From the slope of the fit, ρ_s can be extracted.

2.4 TLM in a cylindrical geometry

TLM is still an applicable technique for deducing the specific contact resistivity in nanowires. The underlying principles are the same but because of their cylindrical geometry, small corrections have to be made to the equations. A simple schematic of how TLM can be applied to vertical nanowire arrays is shown in Fig. 2.4. In accordance to regular TLM, the total resistance of this configuration increases with the spacer thickness as the current has to travel a longer distance. Systematically changing the thickness of the spacer thus enables a TLM plot to be produced.

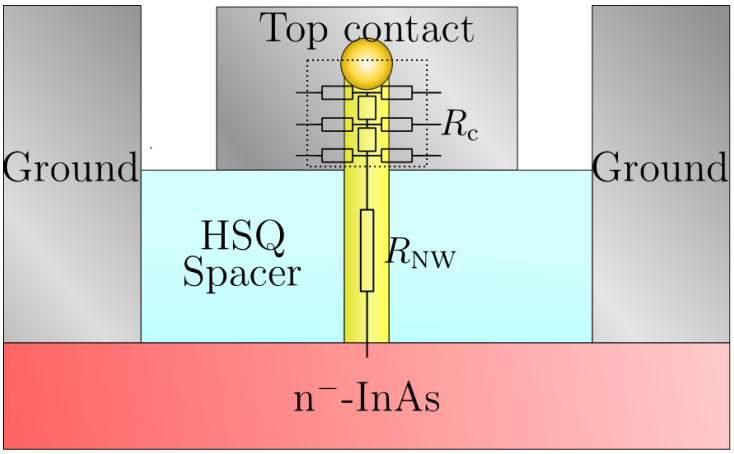

FIGURE 2.4: A semiconductor nanowire is grown on top of a heavily doped buffer layer with negligible resistance. The top part of the nanowire is covered with a metal contact which is separated to the buffer layer by an insulating spacer. The buffer layer is however contacted and grounded outside the spacer. By biasing the top contact, electrons flows through the ground contacts, up through the nanowire, and are swept up by the top contact.

Neglecting the resistance from the highly doped buffer layer, the total resistance of the circuit is the sum of the nanowire resistance R_{NW} and the contact resistance

$$R_{\mathrm{tot}} = R_{\mathrm{NW}} + R_{\mathrm{c}}. \tag{2.16}$$

Notice that the above expression only has one contact-term compared to Eq. (2.10) where two contacts have to accounted for. This is due to the large contact area and assumes negligible resistance from the heavily doped buffer layer. The resistance of the nanowire R_{NW} is given by

$$R_{\mathrm{NW}} = \frac{\rho_{\mathrm{s}} L_{\mathrm{HSQ}}}{\pi r^2} \tag{2.17}$$

where L_{HSQ} is the thickness of the HSQ spacer and r is the radius of the nanowire. In Eq. (2.17) a linear dependence of L_{HSQ} is again obtained analogously to conventional TLM. The contact resistance is later given by

$$R_{\mathrm{c}} = \frac{\rho_{\mathrm{s}} L_{\mathrm{T}}}{\pi r^2} \coth\left(\frac{L_{\mathrm{NW}} - L_{\mathrm{HSQ}}}{L_{\mathrm{T}}}\right) \tag{2.18}$$

as $L_{\mathrm{NW}} - L_{\mathrm{HSQ}}$ gives the contact length. The specific contact resistivity ρ_{c} is ultimately given by [21]

$$\rho_{\mathrm{c}} = \frac{2 L_{\mathrm{T}}^2 \rho_{\mathrm{s}}}{r}. \tag{2.19}$$

Chapter 3

Simulations

Creating realistic models of devices on a nanometre scale easily become quite complex. In order to prevent this, it was in this project decided that an approach where the simplest physical models as possible were to be used. If this can be achieved, the computational time may be reduced, while at the same time, still maintaining a fair representation of an realistic device. How the simulation environment was defined in this project will be described in this chapter together with the used physical models and material parameter settings.

3.1 Method of simulating the transistors

The software used to simulate the vertical NWFETs was "Atlas" developed by Silvaco. To run simulations in Atlas, the structure of the device first has to be defined in a finite element grid. To simulate a NWFET, cylindrical coordinates were used where the structure is rotated around $x = 0$. The mesh-points were later defined, which serves as the nodes where the partial derivative equations for boundary value conditions are to be solved. The mesh therefore serves as a skeleton for the device simulations. A higher density of mesh-points will render more accurate solutions to the equations, but will also require longer computational times. In order to effectively balance this, regions where relevant simulation parameters were thought to show large local variations were given a finer mesh while a coarse mesh was kept in regions of low variations. Balancing the mesh-point density of the structure was carried out empirically. As one of the goals for

the project was to collect information about how the implementation of a shell around the NWFET alters its properties, the simulated structure was continuously changed.

After the mesh was defined, regions defining contact electrodes, insulators and semiconductor materials could be added together with their respective, user definable, properties such as doping concentration, work function and relative dielectric permittivity. In the simulations three electrodes (source, drain, gate) were defined where a voltage could be applied. The source and drain were given ohmic contacts and the gate was set by a work function to mimic a tungsten gate. For the semiconductor material InAs was chosen and its properties were pre-set by the software (see [10] for specifications). The semiconductor NW had a doping concentration emulating an unintentionally doped realistic channel, which was linearly increased to higher levels near the source and drain. The insulator material was user defined for the possibility of changing its dielectric permittivity.

Before device simulation, the physical models had to be specified. Depending on the structure, dimensions, materials, and other parameters used in the device, certain models are more important than others and some may not even be applicable under the specific circumstances. The chosen models are what ultimately defines the physics in the simulation and are therefore of great importance for producing a representation of a realistic device.

For the simulations to not turn out too complex, the physical models were restricted to the Fermi-Dirac carrier statistical model, with drift-diffusion transport and electric field-dependent mobility model mentioned in the theory chapter. As the impurity doping in the InAs channel was set to be high, it could be assumed to be degenerate. This further implies that the Maxwell-Boltzmann approximation for calculating the Fermi level is invalid as it only can account for non-degenerate cases [3]. For this reason, the Fermi-Dirac carrier statistical model is used.

Output and transfer characteristic simulations of the designed devices were later run. The device metrics were then calculated from the generated IV-curves. These metrics, together with the IV-curves were compared to experimental data from a comparable device.

3.2 Device dimensions and parameter settings

The simulation part was dynamically carried out by constantly changing the NWFET structure from a very crude and simple transistor into a more complex one. The final device constituted of a 650 nm long wire with a diameter of 28 nm, see Fig. 3.1. The height of the defined shell was 290 nm from the bottom and it was vertically separated from the gate by 10 nm. The gate was 150 nm long over the channel and stretched down over the shell for another 100 nm. The insulator was 7 nm thick from gate to channel/shell. The highly doped parts of the NW at the top and bottom were 100 nm long, with a 20 nm long linear doping transition.

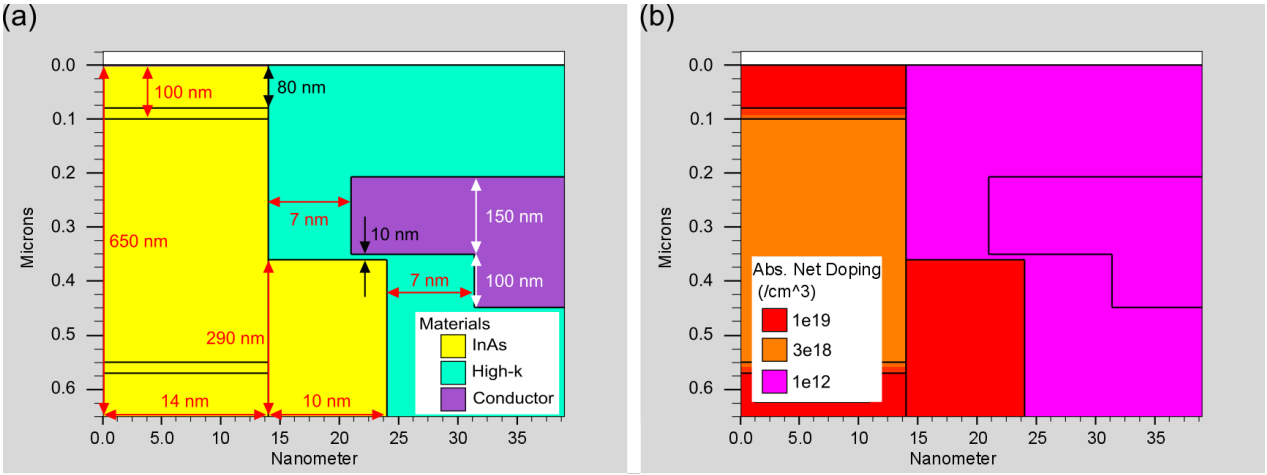

FIGURE 3.1: The final NWFET structure is shown in (a) and the differently doped regions of the NW are illustrated in (b).

For the simulations, the material parameters were pre-defined by Atlas. The defined gate oxide was made to resemble *hafnium dioxide* (HfO_2) which has a dielectric constant between 16-22 [22], [23]. In the simulations, the dielectric constant was therefore arbitrarily set to 19, which together with the insulator thickness corresponds to an *equivalent oxide thickness* (EOT) of 1.44 nm.

The electron mobility μ_{n0} in Eq. (2.7) was set to 2000 cm^2/Vs [24], and the saturation velocity v_{sat} was set to $8{\cdot}10^7$ cm/s [25] to emulate InAs NWFETs. For the fitting parameter β in Eq. (2.7), the Atlas default value of 2 was used.

The NW channel had a doping concentration set to $3 \cdot 10^{18}$ cm^{-3} to resemble the unintentionally doped InAs NWs in [26]. The doping was increased to 10^{19} cm^{-3} near the source and drain for better contacts. The doping in the shell was set to 10^{19} cm^{-3}.

Chapter 4

Simulations: Results and Discussion

When simulating the vertical III-V NWFETs, several structures were defined and compared against each other. By analysing the band structure and electric field along the channel, it could be concluded that the different structures affect the device in various ways. The stability of the devices together with the extracted DC performance metrics show that there seems to be a preferable biasing configuration. The simulated devices were also compared to a real device.

4.1 Symmetric gate

In the simplest transistor model, the gate was symmetrically defined and had a length of 150 nm as seen in Fig. 4.1 (a). The band structure and electric field of the device were all evaluated along a cut-line parallel to the y-axis at $x = 10$ nm, also shown in the figure. A shell structure was then introduced around the bottom of the wire making the NWFET asymmetric, Fig. 4.1 (b). This new geometry was examined along the same cut-line as the previous one in order to investigate the shell impact on the device.

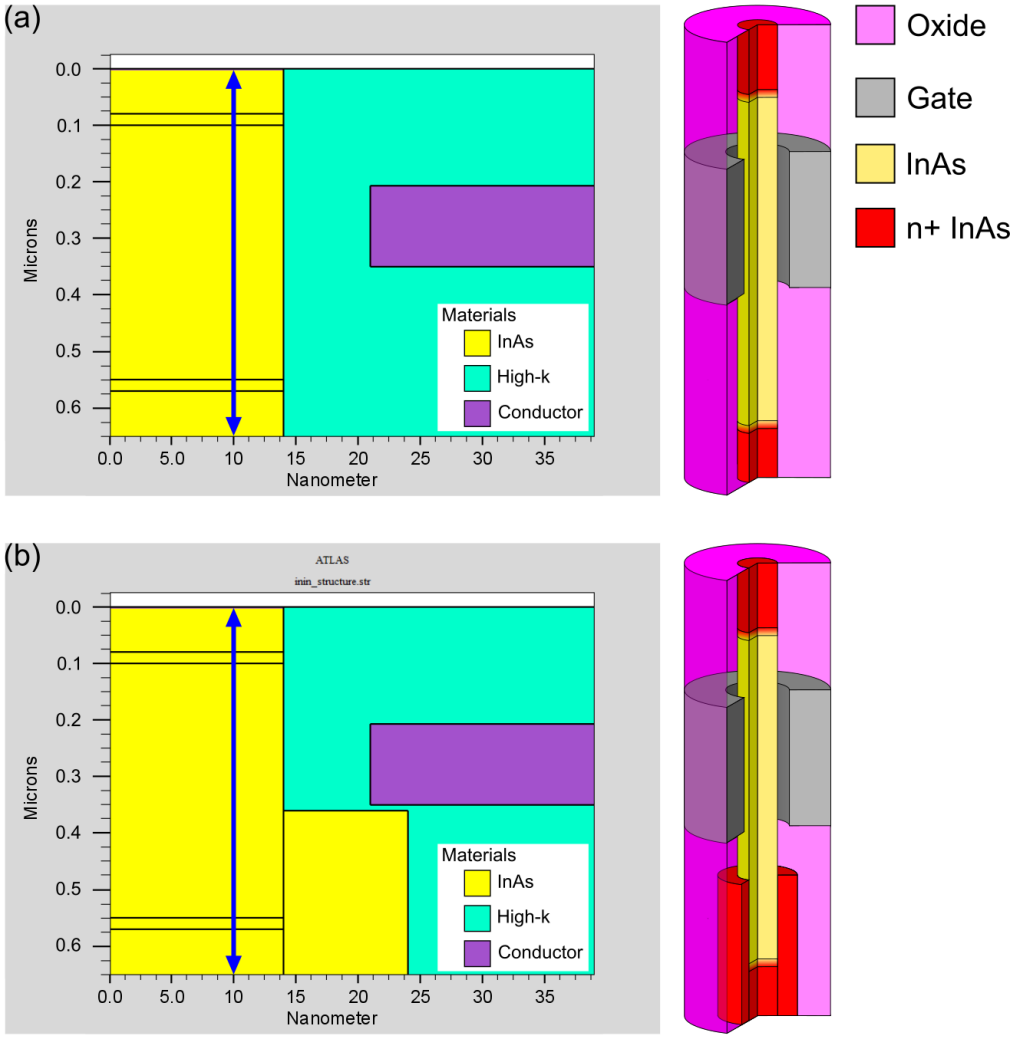

FIGURE 4.1: The left hand side of (a) and (b) shows the transistor structure as seen from Atlas. Notice that the axis of symmetry is along $x = 0$ and that the x- and y-axes are not the same scale. To better visualize the geometry, a schematic is shown to the right. In (b) a shell is implemented not present in (a). The NW colour differences in the schematics depicts doping changing regions. The blue arrows in the left figures indicate the cut-line where the transistor was evaluated.

The band structure of the NW along the cut-line shown in Fig. 4.1 are plotted in Fig. 4.2, where no bias is applied. As expected, the bands near the source and drain contacts bend due to doping concentration differences forcing the Fermi level to shift in order to preserve charge neutrality [2]. Also seen in the plot is that the work function of the gate metal pulls up the bands in the gated part of the channel as thermal equilibrium over the MOS-capacitor is reached. This shows that the work function of the metal is larger than the work function of the semiconductor channel. The high doping of the shell can be seen to effectively lower the bands in the part of the wire covered by the shell.

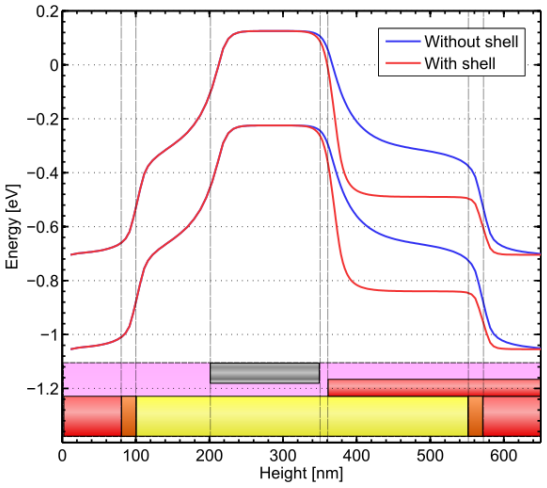

FIGURE 4.2: Band structure comparison with and without a shell. A schematic of the NWFET is shown lying at the bottom of the graph in order to better see what part of the architecture is causing the bands to bend.

A drain bias of $V_{ds} = 0.8$ V and a gate bias of $V_{gs} = 0$ V is applied to the transistors, keeping the source grounded. As the NWFET is asymmetric, the device is evaluated in both a top grounded configuration where the bias is applied to the bottom contact, and in a bottom grounded configuration where the bias is applied at the top of the device. The obtained band structure along the previous cut-line is given in Fig. 4.3.

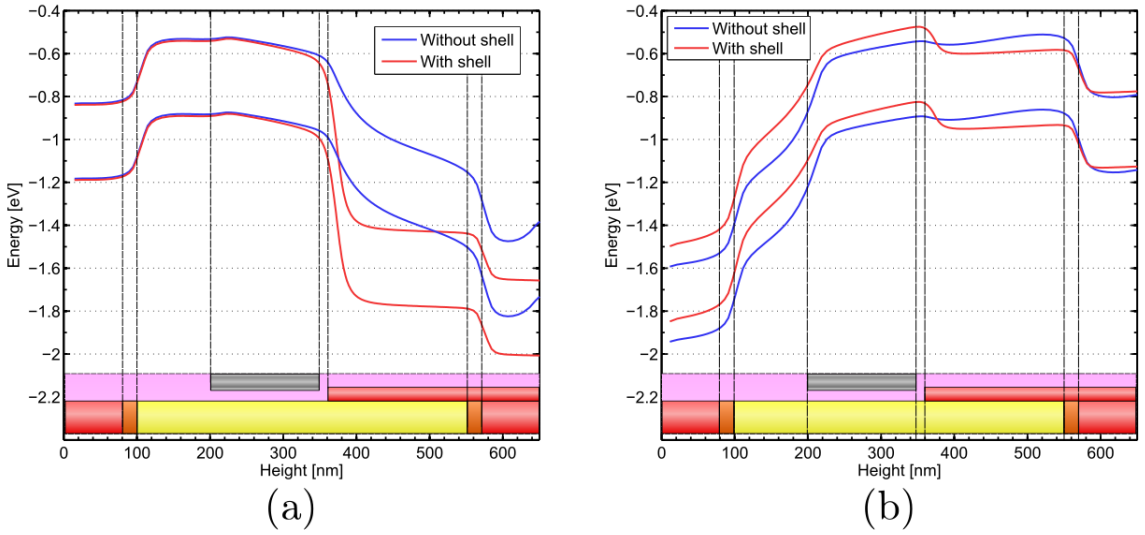

FIGURE 4.3: Band structure for a certain bias in (a) top ground configuration and (b) bottom ground configuration, with and without a heavily doped shell. The top part of the NW is to the left (x=0 nm) and the bottom part to the right (x=650 nm).

The shell can again be seen to lower the bands in both configurations. However, the lowering of the bands under the shell is much more prominent when top grounded, where the gap between the conduction- and valence bands is greatly reduced around the top of the shell. As the gap occurs to be suspiciously small, it is reasonable to believe that this configuration easily gets afflicted by device breakdown in form of either band-to-band tunnelling- or impact ionization events. The shell thus seems to have a negative effect on the device for the top grounded configuration which may result in stability unreliability. This is however not observed in the bottom ground configuration which therefore seems to be much more suited to operate with a shell.

By instead plotting the electric field under the same biasing conditions, Fig. 4.4 is created. As expected, the interface between differently doped regions in the device give rise to peaks in the electric field. Evidently, the presence of a shell also makes a huge impact on the magnitude and profile of the electric field. Starting with the top grounded configuration, the first striking difference comparing the device with or without a shell is that there is a large peak in the electric field generated at the top of the shell, about twice the intensity of the peak generated by the edge of the gate seen without the shell. The electric field can also be seen to stay high parallel along the shell structure in both configurations. Contrary to the top grounded case, the bottom grounded configuration shows a peak reduction at both edges of the gate. Despite the electric field being high along the shell in this configuration as well, the maximum measured electric field is still reduced which may suggest that the shell prevents device breakdown for higher voltages.

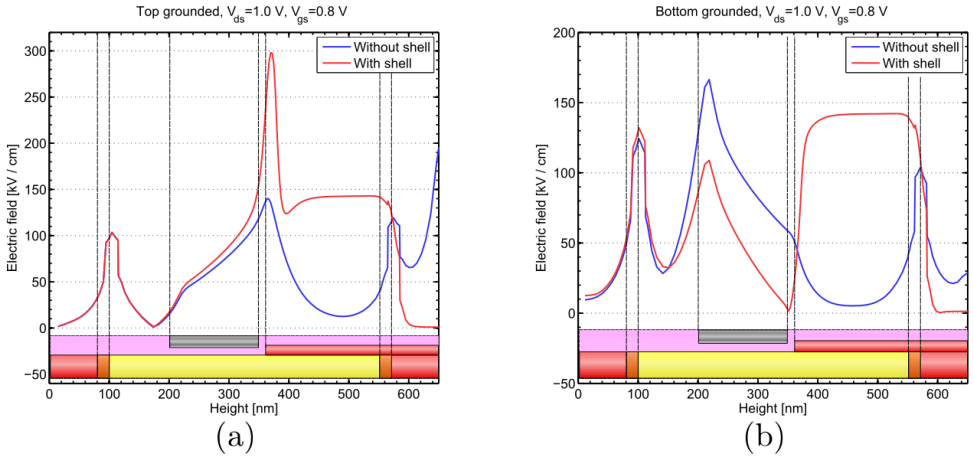

FIGURE 4.4: Band structure for a certain bias in (a) top ground configuration and (b) bottom ground configuration, with and without a heavily doped shell. The top part of the NW is to the left (x=0 nm) and the bottom part to the right (x=650 nm) as shown by the schematics at the bottom.

4.2 Asymmetric gate

When processing real vertical NWFETs with a similar shell as simulated here, it is common to have the gate reach down over the shell to some extent. The reason for this is to generate a *field plate* (FP) behaviour which could improve the transistor in several aspects, e.g., increasing breakdown voltage and add device stability [13]. FPs have been researched for *high-electron-mobility-transistors* (HEMTs) where they can be seen to induce an additional electric field peak in the channel, effectively dividing the voltage drop between the FP edge and the gate edge [14]. Therefore, in an attempt to simulate this for vertical NWFETs an asymmetric gate was also defined and analysed in an identical way as the previously studied symmetric gate case, see Fig 4.5.

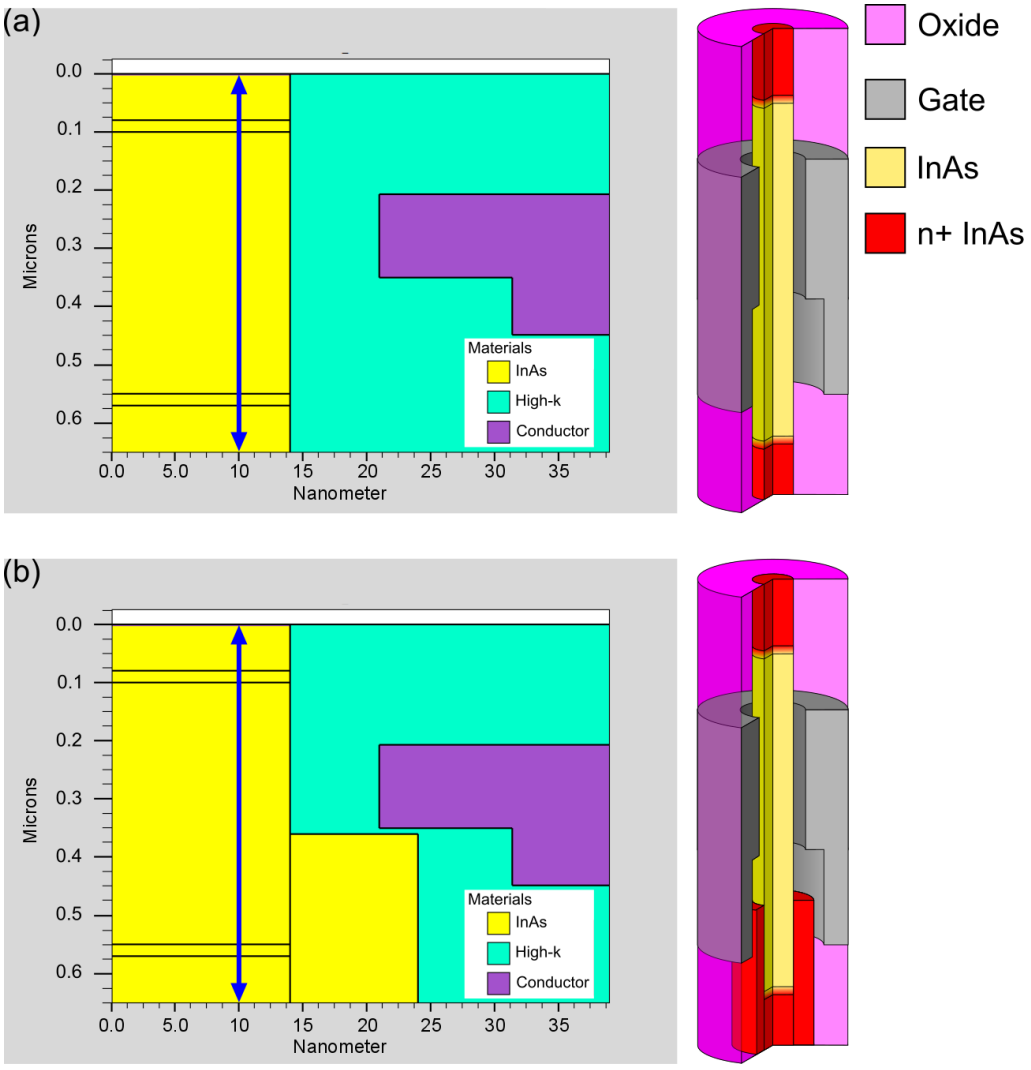

FIGURE 4.5: The asymmetric gate is applied to the device in, (a) without a shell, and (b) with a shell. Schematics to the right show a more comprehensive image of the NWFETs. The blue arrow indicates the measured cut-line.

The band structure in the channel with this new gate geometry is shown in Fig. 4.6, where the band structure using a symmetric gate also can be seen for comparison. The top grounded configuration clearly shows how the gate extension pulls up the bands and increases the lateral distance from conduction to valence band. As the shell is located at the bottom of the NWFET, its electrostatic properties seem to be very sensitive in this configuration. In the bottom grounded configuration the band structure shift is much more subtle and almost not noticeable.

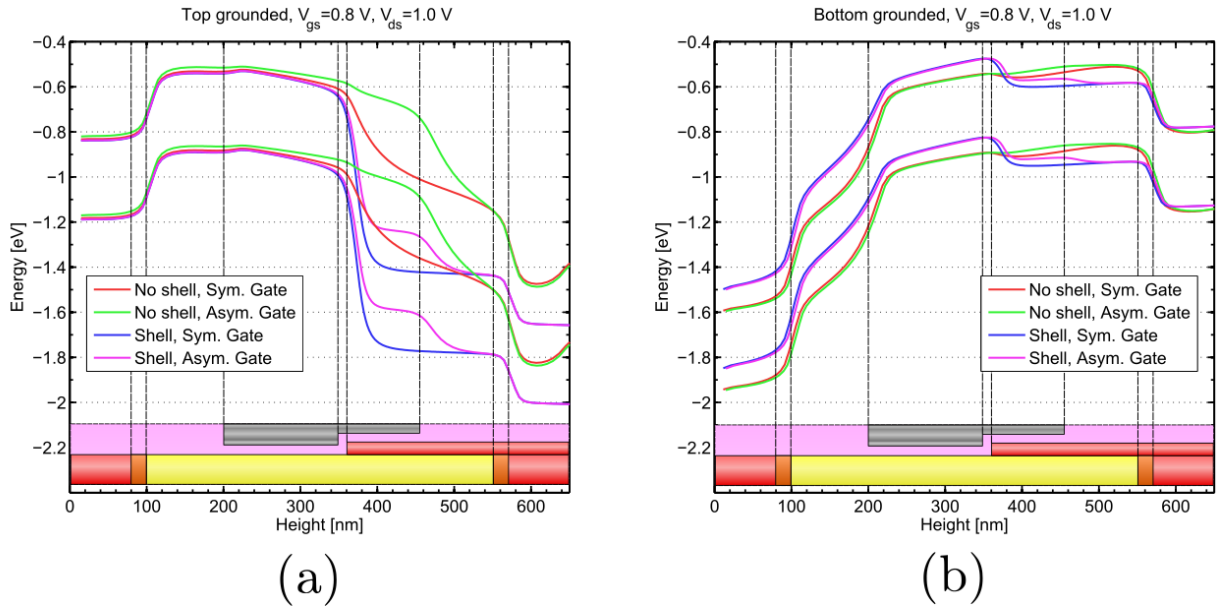

FIGURE 4.6: Band structure in the a top ground configuration (a), and a bottom ground configuration (b).

Looking at Fig. 4.7, the asymmetric gate extension seems to reduce the electric field peak slightly for the top grounded configuration. This, in accordance to the lateral broadening of the narrow band gap, is expected if the asymmetric gate extension would serve as a FP. This effect is however rather small and it is therefore possible that the extension of the gate does not affect the channel sufficiently to be regarded as a FP, as the heavily doped shell might screen the potential drop in the channel. In the bottom grounded configuration on the other hand, the difference in electric field redistribution is less pronounced and the maximum field does not seem to change visibly. The shell apparently influences the electrostatics in the device to a higher extent compared to the new gate geometry.

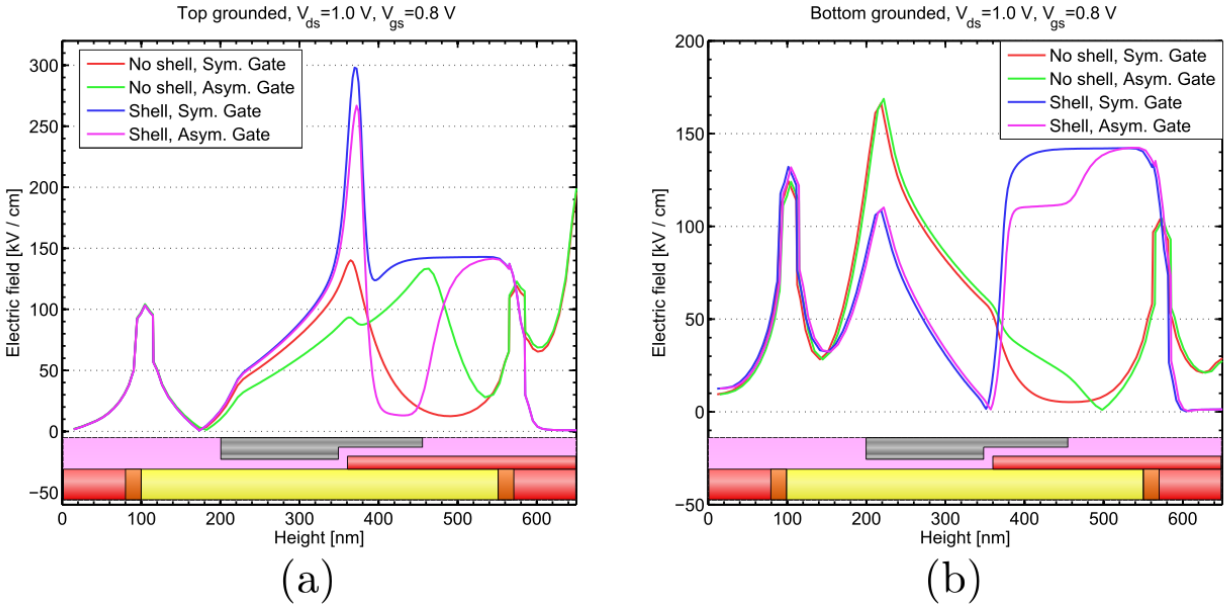

FIGURE 4.7: Electric field inside channel in a bottom ground configuration comparing the four different structures grounding the top (a), and the bottom (b).

4.3 Comparison to experimental data

Vertical InAs/$In_{0.7}Ga_{0.3}As$ NWFETs are currently being developed by the Nanoelectronics group at Lund Technical University. The NWs in these devices are processed to have an InAs core channel which transitions to highly doped $In_{0.7}Ga_{0.3}As$ near the top contact. These NWs are overgrown with highly doped InGaAs creating a shell around them. Furthermore, W is used as the gate metal in these devices. This makes the NWFETs similar to the ones simulated in this work. Output- and transfer characteristics from these experimental devices were therefore compared to the simulated ones. In order to acquire the same slope in the output characteristics, a contact resistivity of 1.0 $\Omega\mu m^2$ was added to the source and drain in the simulations (this value is comparable to the measured TLM data presented in chapter 6). Fig. 4.8 and 4.9 show IV-characteristics comparing the experimental and simulated data. A comparison between top and bottom ground for the simulations can also be seen in these figures.

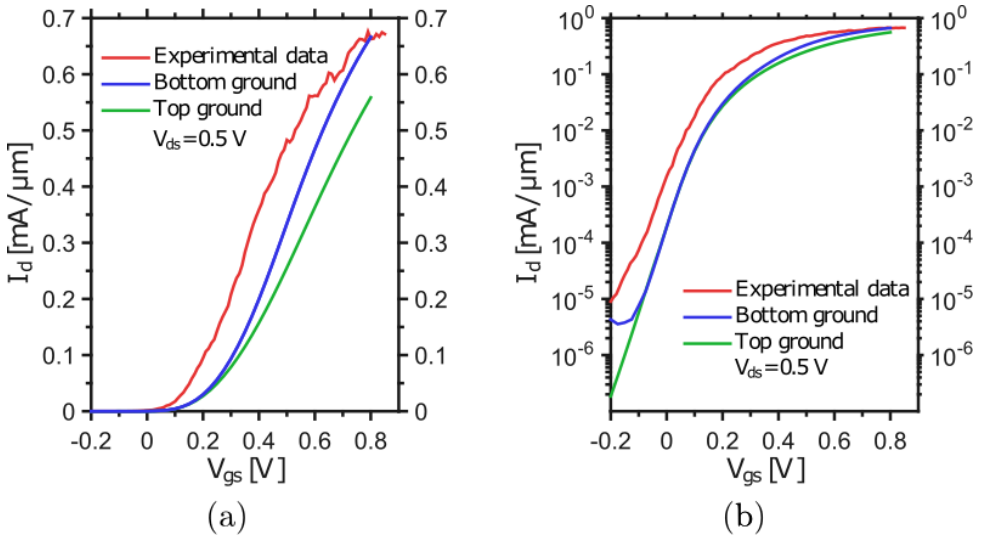

FIGURE 4.8: Transfer characteristics comparing real devices with simulations plotted on a linear scale to show the on-state (a) and a logarithmic scale to see how the devices behave in the off-state (b). The experimental device was measured with the bottom contact grounded.

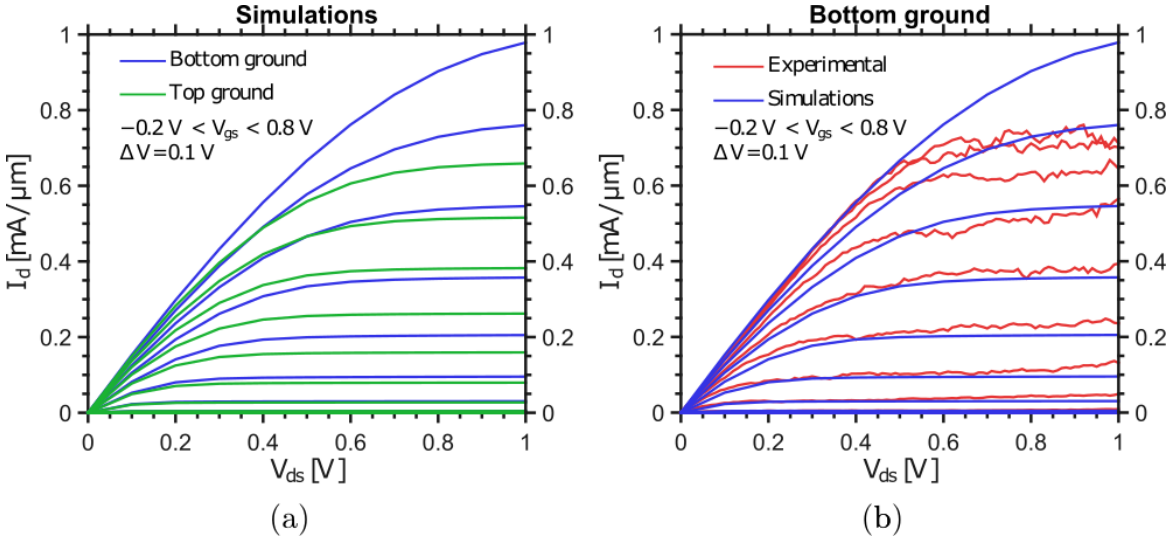

FIGURE 4.9: The output characteristics simulated with a top/bottom ground configuration are compared in (a). Simulated and experimental output characteristics are compared in (b) for a bottom ground configuration.

As seen in both Fig. 4.8 and 4.9, the simulated curves are remarkably similar in shape to the real data despite the relatively simple models used. The V_{T} can however be seen to differ and is higher in the simulations. This can be seen in both the output and transfer curves as the device "turns on" earlier at lower V_{gs}. The reason for this V_{T}-shift is probably due to differences in the gate metal work function between the simulated NWFETs and the experimental ones. A lower V_{T} for the real transistor indicates that the gate work

function was lower compared to its simulated counterpart. Another possible explanation is differences in channel doping. Performance metrics of the devices are calculated from these IV-curves and are presented in Table 4.1.

TABLE 4.1: Calculated performance metrics from simulations with different geometries and configurations. Metrics from the experimental device are also given.

Top ground				
Geometry	$g_{m,max}$ [mS/μm]	I_{on} [μA/μm] I_{off}=100 nA/μm	V_T [V]	S_{min} [mV/dec]
Without shell, Sym. gate	0.916	222	0.231	64.0
Without shell, Asym. gate	0.804	197	0.227	63.6
With shell, Sym. gate	1.09	232	0.261	65.6
With shell, Asym. gate	1.08	230	0.262	65.4
Bottom ground				
Geometry	$g_{m,max}$ [mS/μm]	I_{on} [μA/μm] I_{off}=100 nA/μm	V_T [V]	S_{min} [mV/dec]
Without shell, Sym. gate	0.813	197	0.230	63.9
Without shell, Asym. gate	0.811	179	0.252	64.1
With shell, Sym. gate	1.40	304	0.257	63.3
With shell, Asym. gate	1.39	300	0.258	63.2
Experimental data				
Configuration	$g_{m,max}$ [mS/μm]	I_{on} [μA/μm] I_{off}=100 nA/μm	V_T [V]	S_{min} [mV/dec]
Bottom ground	1.40	330	0.150	85

Judging by the performance metrics, it can be concluded that introducing a shell around the bottom of the NWs enhances overall performance independent on the configuration. It is also clear that it is preferable to have the bottom grounded when a shell is present in the device as higher current are observed. This implies that the top contact has a higher resistance compared to the bottom contact. This can be explained by the larger contact area at the bottom created by the added shell. Another reason for the improved bottom contact is due to the heavy doping in the shell which lowers the metal-semiconductor barrier height for a n-doped semiconductor [3]. Having an asymmetric gate does however not seem to affect the performance considerably although Fig. 4.6 and 4.7, suggest improved device stability.

For more realistic simulations, the gate dialectic has to be further modified where the extrinsic capacitances of it has to be taken into consideration. Having a high-κ insulator is important for good gate control of the channel but it also generates more extrinsic capacitances which slows down the switching speed of the device. This trade-off was not considered in this project. Also impact ionization- and band-to-band tunnelling events have to be taken into account in more realistic simulations. In this project it can be assumed that impact ionization and band-to-band tunnelling occurs in the channel although it is not explicitly modelled.

Chapter 5

TLM: Device Fabrication and Measurements

In this project, the specific contact resistivity from different metals were compared for InAs and $In_{0.2}Ga_{0.8}$ NWs. To calculate the contact resistivities, the transmission line method was used. In order to apply this technique, the samples had to be processed in a certain way. Before the devices were finalized, the *hydrogen silsesquieoxane* (HSQ) spacer between the buffer layer and the top metal contact was measured. This chapter explains how all these steps were carried out.

5.1 TLM processing

InAs and $In_{0.2}Ga_{0.8}As$ nanowire samples grown by *metal organic vapour phase epitaxy* (MOVPE) had been prepared for TLM processing. The NWs were grown from Au seed particles using the VLS-method, where the resulting radii of the wires were defined by the seed particle sizes which were changed systematically [19]. The samples were grown on *p*-type Si wafers covered by an 300 nm heavily doped InAs epitaxial layer film [27]. The InAs film served as a buffer layer for the NW growth [28].

After receiving the samples, the quality of the NWs were inspected by *scanning electron microscopy* (SEM). The dimensions of the NWs, i.e., the thickness and length, were also measured with SEM. A HSQ film was then spin coated on the samples covering the wires.

By using *electron beam lithography* (EBL), the HSQ was patterned to form planar HSQ spacers. The thickness of these could be varied by changing the EBL dose [29]. In order to be able to contact the NWs, the thickness of the spacers had to be less than the height of the NWs. After EBL treatment, the samples were developed in concentrated *tetramethylammonium hydroxide* (TMAH) and rinsed with water before baking the HSQ [19].

The samples were later wet etched in hydrochloric acid (HCl) to remove native oxides prior to top contact metal deposition. The top contact was sputtered on and different metals were used for the two processed batches. In the first batch, 60 nm W and 150 nm Au was deposited, and in the second batch 50 nm Mo was sputtered with an additional 140 nm Au.

After that, the samples were spin-coated with photoresist and the contacts were defined by *ultra violet lithography* (UVL). Subsequently, the excess Au was wet etched with a potassium iodide (KI) solution, and for Mo etching, hydrogen peroxide (H_2O_2) was used. W was dry etched by *reactive ion etch* (RIE). The samples were then finalized by removing the photoresist with acetone and isopropyl alcohol.

5.2 Determining HSQ thickness of TLM samples

It is vital in TLM experiments to measure the contact separation to a sufficiently high resolution to be able to deduce the contact resistance. In this diploma work, the HSQ thickness (essentially the contact separation) was determined by analysing the RGB-values from optical microscope pictures of the HSQ pads in MATLAB. The thickness of the spacers aligned in a test row (without NWs), were measured by a profilometer. The thickness was then calibrated to the corresponding RGB-values from the optical microscope pictures. By doing this, a colourbar was created which enabled deduction of spacer thickness judged by the colour of them from the taken microscope pictures, see Fig. 5.1 and Fig. 5.2 below. For this method to work it is crucial that the exact same lighting conditions are used when taking all microscope pictures.

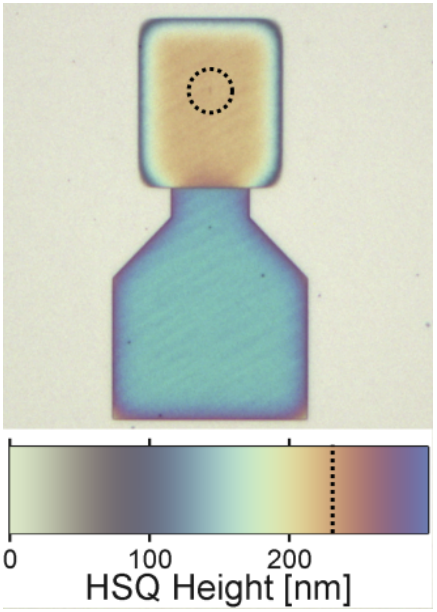

FIGURE 5.1: Reference RGB colorbar calibrated with profilometer. The HSQ thickness from the optical images can be extracted as the colour of the HSQ spacer corresponds to a certain thickness.

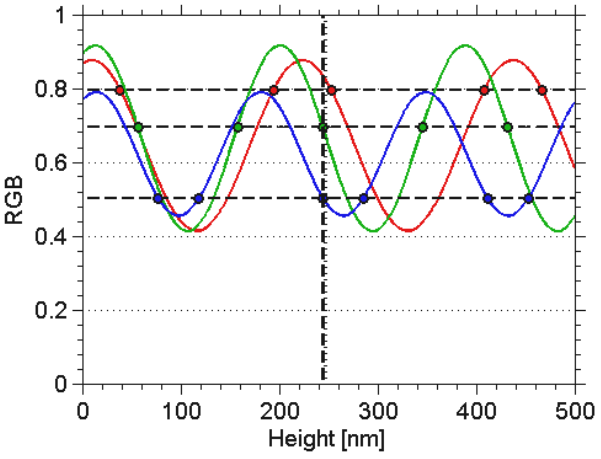

FIGURE 5.2: MATLAB script generated by providing the RGB values for a certain HSQ pad. The code automatically gives the best fit for the given input values. In this case the best fit corresponds to a thickness of 247 nm.

Because the NWs were longer than the HSQ spacers, the thickness of the spacers were not measured directly by profilometer in fear of damaging the wires. However, in order to verify the accuracy of the used method, some of the rows containing wires were sacrificially also measured with profilometer.

5.3 DC characterisation

The finished samples were measured with a "Cascade 11000B" probe station. The top contact was swept from -0.1 V up to 0.1 V with a step size of 10 mV, while the bottom contact was kept grounded.

The total resistance of the resistors was calculated by Ohm's law. TLM graphs were then produced by plotting this resistance against the deduced HSQ thickness. The desired material parameters could then be calculated in MATLAB by applying the least square fit method to the TLM equations found in the theory chapter.

Chapter 6

TLM: Results and Discussion

By applying the TLM technique on vertical NW resistors, it was possible to calculate the specific contact resistivity between the semiconductor NW and the contact metal. Because the NWs made of $In_{0.2}Ga_{0.8}$ had a non-cylindrical shape, the already established TLM equations could not be applied. In order to still be able to deduce the desired parameters from these samples, slight modifications had to be made to the TLM equations. The reasoning and assumptions behind these changes will be given in this chapter. Some of the encountered problems behind the TLM studies and the errors are also discussed at the end.

6.1 NW quality

A first degree inspection of the quality of the NWs were performed by observing the samples with SEM. For both the InAs and InGaAs samples, the consistency of identical NWs per array could be seen to increase with seed particle radius. The longest NWs, i.e., the ones grown from the smallest seed particles, fluctuated more in both length and radius compared to the shorter NWs. Furthermore, it was also more common for longer NWs to bend to an non-functional degree (see Fig.6.9 in section "TLM obstacles"). Because of this observation, it is reasonable to assume that the TLM measurements from rows with shorter NWs provide more trustworthy data. The SEM images in Fig. 6.1 show the shape of the NW resistors.

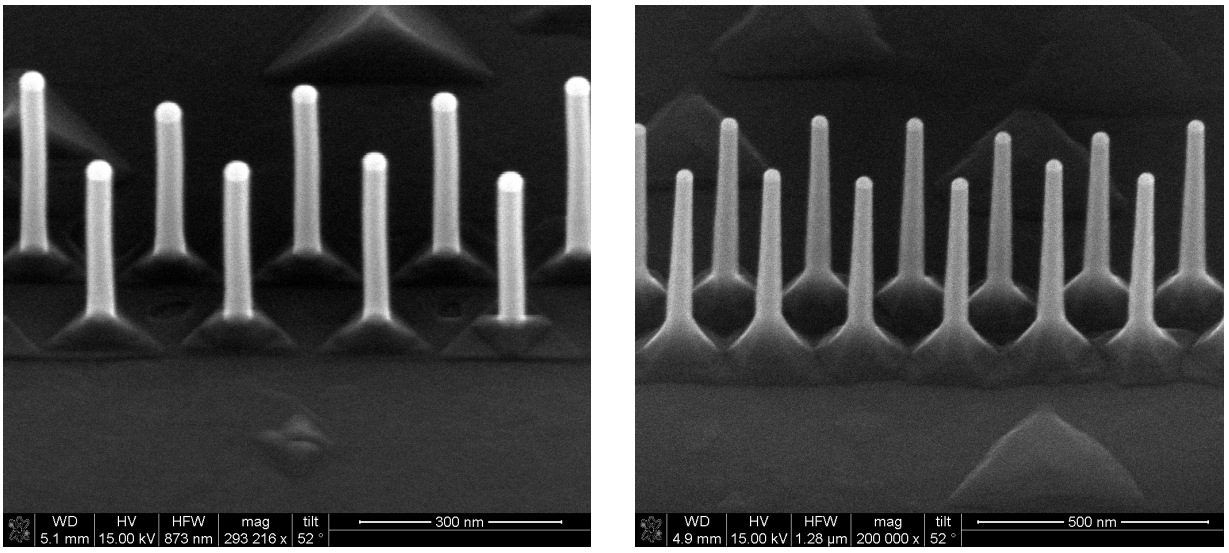

FIGURE 6.1: SEM images showing the InAs NWs in (a) and $In_{0.2}Ga_{0.8}As$ NWs in (b). The InAs NWs can justifiably be assumed to be completely cylindrical but the radii of the InGaAs NWs are evidently height dependent as the wires seem to have a more cone-like shape.

6.2 InAs

In both InAs samples, three radii of the NW were systematically changed over nine rows. Although the NW growth itself was not conducted in this diploma work, both samples were grown at the same time and therefore the NW quality and dimensions ought to have been the same. However, when inspecting the thickness of the wires with SEM, the sample later contacted with W, seemed to have slightly larger diameters. The rows with the thinnest wires in both samples were discarded due to insufficient NW quality (see Fig.6.9 in section "TLM obstacles"). The radii of the remaining functional wires were estimated to be 20 and 22 nm for the W sample, and 19 and 20 nm for the Mo sample.

By applying the least square fit method to Eq. (2.16) through (2.19), a fit to the measured data was created to form TLM plots of all measured rows from where L_T, ρ_s and ρ_c could be determined. The two contact metals were then compared, see Fig. 6.2, where the data fit also is included. The fitted curves for the thicker wires clearly show excellent agreement with the data. The fit of the Mo-contacted sample especially gives a good fit where the upswing to the right arises from L_c getting smaller than L_T, see Eq. (2.13), as $\lim_{x\to 0} \coth(x) \to \infty$. It can be seen that the TLM fit improves with NW radius. This is quite expected as the consistency of the wires was seen to be more even for the thicker

wires. The material parameters are calculated and presented in Table. 6.1 below. In Fig. 6.3, the best rows for each sample is compared.

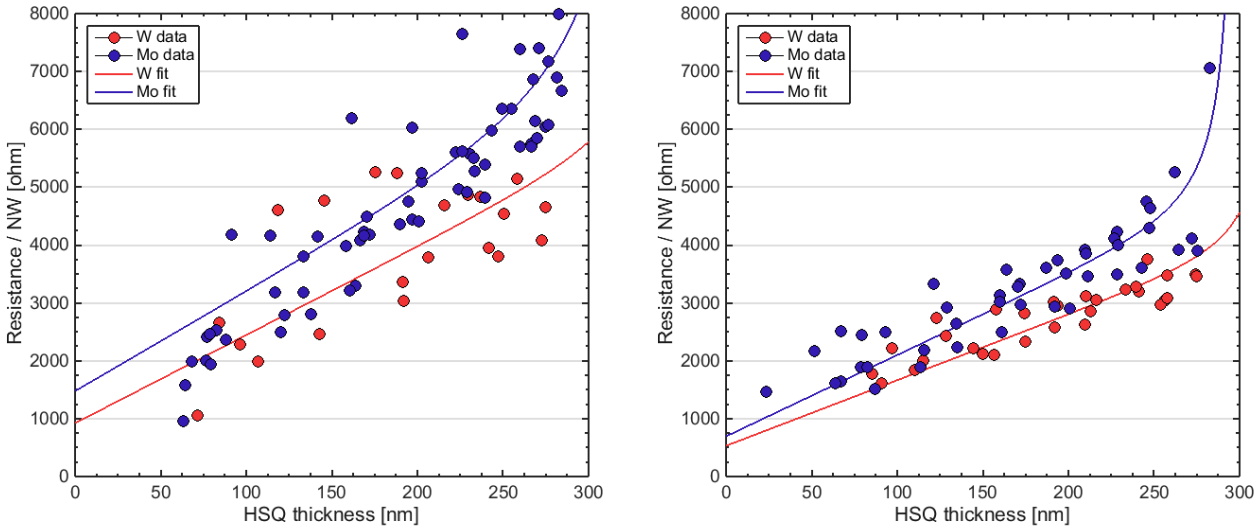

FIGURE 6.2: The left figure corresponds to TLM measurements performed on thinner NWs in both samples, and the right figure shows TLM plots of the thicker wires.

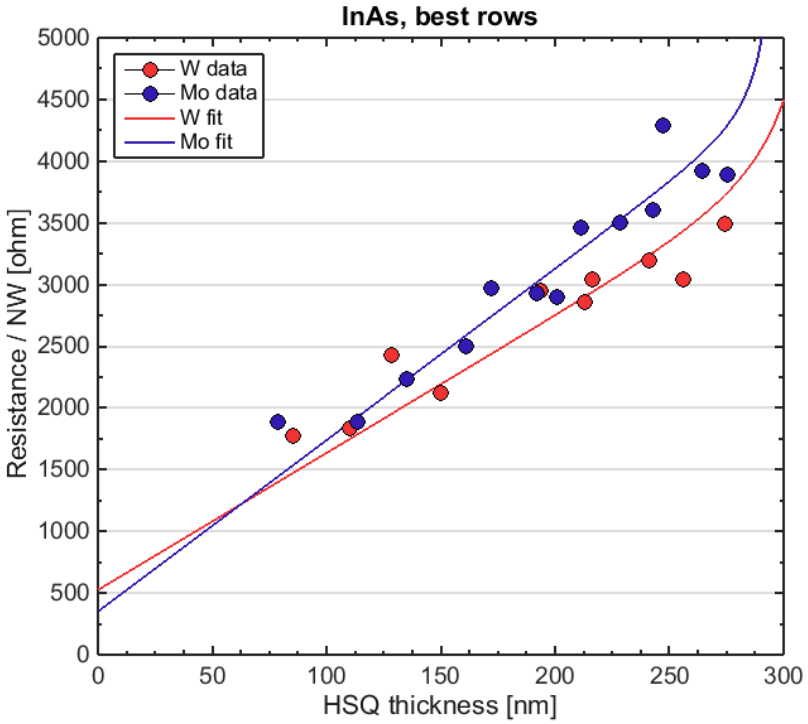

FIGURE 6.3: Plot comparing the best rows for both W and Mo contacted InAs samples.

TABLE 6.1: Calculated parameters from the InAs NW TLM measurements. The errors in the measurements are thought to be large and are instead of being estimated by a number, discussed at the end of this chapter.

InAs (W)			
Radius [nm]	$\boldsymbol{\rho_s}$ [$\Omega \cdot \mu$m]	$\boldsymbol{\rho_c}$ [$\Omega \cdot \mu$m^2]	$\boldsymbol{L_T}$ [nm]
∼20	18.1	7.33	62.9
∼22	16.9	3.39	46.7
∼22 (Best row)	16.6	3.33	46.7
InAs (Mo)			
Radius [nm]	$\boldsymbol{\rho_s}$ [$\Omega \cdot \mu$m]	$\boldsymbol{\rho_c}$ [$\Omega \cdot \mu$m^2]	$\boldsymbol{L_T}$ [nm]
∼19	20	10.3	70
∼20	17.7	4.31	49.4
∼20 (Best row)	17.5	1.11	25.2

As seen in Table 6.1, the best measured data was extracted from one of the rows contacted by Mo, where the specific contact resistivity was deduced to 1.11 $\Omega \cdot \mu$m^2 corresponding to a transfer length of 25.2 nm. However, due to the larger data spread for this sample, these values are also seen to be quite reduced when all rows with the same radii were included in the fit, in contrast to W which seemed to be much more consistent. Comparing the radii dependence in both samples, the calculated parameters seem to improve with increasing radius. Therefore, comparing the samples where the radius is estimated to be 20 nm further suggests that Mo is a better contact metal than W for InAs NWs.

The resistivity in the wires should be the same in both samples as they were grown on the same occasion. It should presumably also be independent on the thickness of the wires. But the retrieved data suggests that ρ_s decreases with increased radius. One possible explanation to this might be that the surface energy states in the thinner wires constitute a larger amount of the total energy states in the wire relative to the core where the majority of the carrier transport is assumed to take place. As the surface states greatly enhances the carrier recombination rate [2], it is expected that the resistivity also increases near the surface and thus is more prominent for wires of smaller radii. This would explain why the resistivity seemingly goes down with the NW radius.

6.3 InGaAs

The heterojunction present at the bottom of the $In_{0.2}Ga_{0.8}As$ NWs to the InAs buffer layer induces a potential barrier. This further implies that a current sent through the two materials will favour one direction over the other, i.e., the IV-characteristics show a diode-like shape where a positive bias at the top contact generates a higher current compared to if it was negatively biased. This is an unattractive feature as calculating the resistance in the TLM NW resistors depends on using Ohm's law, which requires an ohmic linear behaviour. However, by keeping the voltage sweep low, ranging from -0.1 V to 0.1 V, a linear behaviour can be approximated. In Fig. 6.4, the IV-characteristics from an InGaAs sample is plotted where the lines showing the largest currents, and largest current differences, correspond to the arrays with thinnest HSQ spacers.

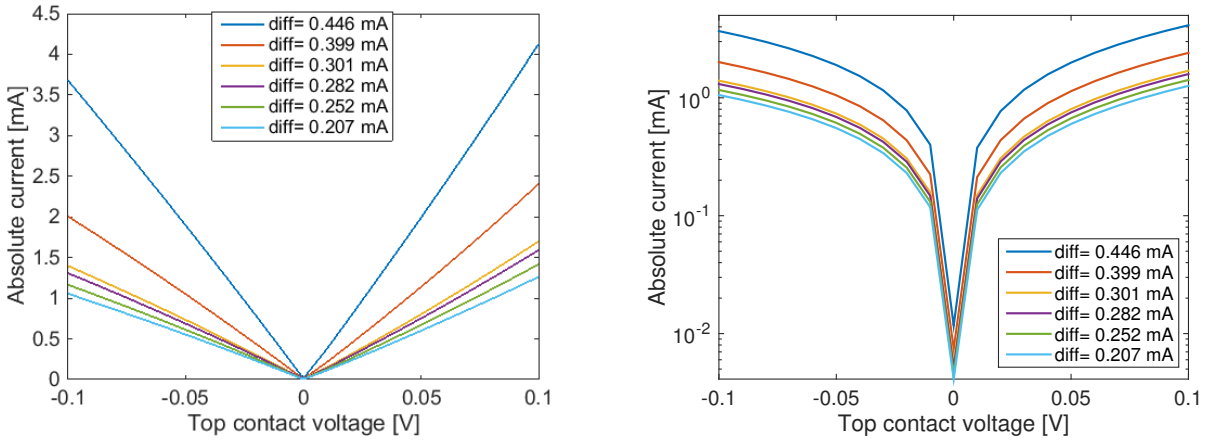

FIGURE 6.4: Plot showing how linear an InGaAs NW resistor row was. The data is taken from a row of large seed particle sizes and is plotted on a linear scale to the left and a logarithmic scale to the right. The difference in absolute current is given in the legends.

The shape of the $In_{0.2}Ga_{0.8}As$ NWs (Fig. 6.1) further pose concern about how to use the TLM equations, Eq. (2.16) through Eq. (2.19), as they are designed for NWs of cylindrical geometry. In an attempt to solve this problem, the equations are slightly modified to regard the asymmetric shape of the wires. In this new approach, the NWs were approximated to have three distinct parts; the NW "foot", the NW "channel", and the contacted top part. All these parts each have a linearly height dependent cross-section and are depicted in Fig.6.5.

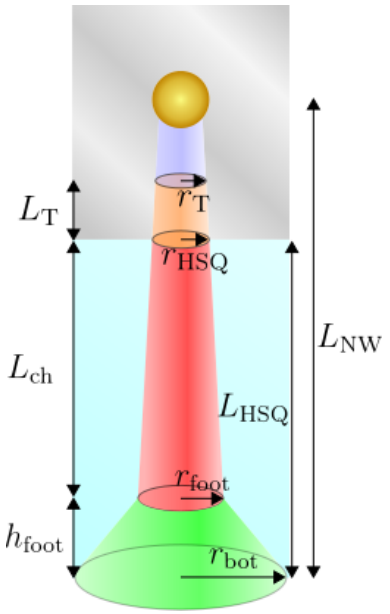

FIGURE 6.5: Schematic of an asymmetric InGaAs NW. The lower green part is the foot of the wire, the red middle part is called the channel and the orange part shows the approximated effective contact area one transfer length from the HSQ.

The sum of the resistances for the three parts is then assumed to constitute the total resistance measured with the probe station, namely

$$R_{tot} = R_{foot} + R_{ch} + R_c \tag{6.1}$$

where R_{foot} is the resistance in the foot and R_{ch} is the resistance in the NW between the top of the foot and the top of the HSQ spacer. As the resistance of a conductor with varying linear cross-section has the general form of $R = \rho/\pi ab$, where a is the radius at one end of the conductor and b is the radius at the other end, the above expression can together with the cylindrical TLM equations (2.16)-(2.19) be modified to

$$R_{tot} = \frac{\rho_S h_{bot}}{\pi r_{bot} r_{foot}} + \frac{\rho_S L_{ch}}{\pi r_{foot} r_{HSQ}} + \frac{\rho_S L_T}{\pi r_{HSQ} r_T} \coth\left(\frac{L_{NW} - L_{HSQ}}{L_T}\right) \tag{6.2}$$

and

$$\rho_c = \frac{2L_T^2 \rho_s}{\left(\frac{r_{HSQ}+r_T}{2}\right)} \tag{6.3}$$

where h_{foot} is the height of the foot and L_{ch} is the length of the channel, r_{bot}, r_{foot}, and r_{HSQ} are the radii at the bottom of the NW, the top of the foot and the top of the HSQ respectively and r_T is the radius one transfer length into the contacted region

from the HSQ spacer. It is noteworthy that the above expression only works if $h_{\text{foot}} < L_{\text{HSQ}}$. Therefore data where $h_{\text{foot}} \geq L_{\text{HSQ}}$ had to be disregarded in the TLM plots. The denominator in Eq. (6.3) resembles the radius for the contact and because it varies with height, it was approximated as the mean between r_{HSQ} and r_{T}.

The only unknown parameters in Eq. (6.2) are L_{T} and ρ_{s} as the other ones are either directly or indirectly measurable. This further enables deduction of L_{T} and ρ_{s} using a least square fit model to the TLM data. This is shown in Fig. 6.6 where the grey line is fitted to the raw data points also shown in grey.

One of the visible consequences of this effect is that the fit cuts the y-axis at a negative value. In conventional TLM, this would imply a negative contact resistance, which of course is unrealistic. To avoid this, the foot of the wire is regarded as a contact as it is assumed to be constant for $L_{\text{HSQ}} > h_{\text{foot}}$. By calculating the resistance in the foot and subtracting it from the total resistance, an adjusted TLM plot can be produced where the fit intersects the y-axis at a positive value, as seen in Fig. 6.6. The height of the foot also has to be subtracted from the HSQ thickness in these plots. Using the revised TLM equations, ρ_{s}, ρ_{c} and L_{T} were calculated from the samples and are tabulated in Table 6.2.

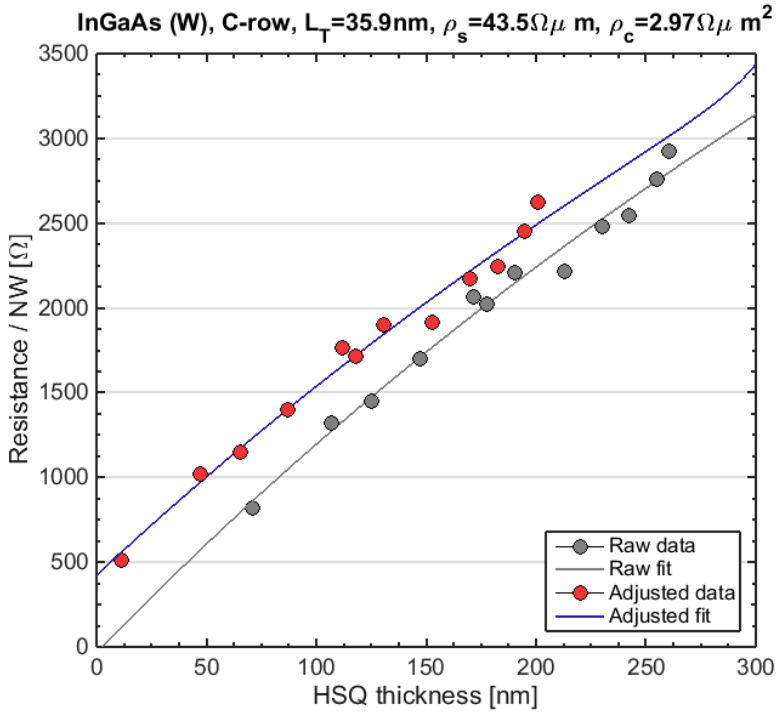

FIGURE 6.6: InGaAs TLM plot contacted with W. The gray dots show raw data and their fit intersects the y-axis at a negative value. The red dots show how the data were adjusted enabling the fit to intersect at a positive value.

However, the R_{ch} term in Eq. (6.1) is not linearly dependent on L_{ch}, as opposed to R_{NW} being linearly dependent on L_{HSQ} in Eq. (2.16). Furthermore, R_c is also non-linear because of the changing radius. This non-linearity is clearly visible in Fig. 6.6 as the fit first seems to bend downwards and then upwards.

Fitting data from all the rows in both samples renders the TLM plots shown in Fig. 6.7. The data is widely scattered and it is obvious that this imposed a bigger problem for the Mo sample. The inconsistencies are believed to originate from processing errors in both samples when etching the contact metals. However, if individual rows for the two samples are considered, better fits can be achieved, see Fig. 6.8.

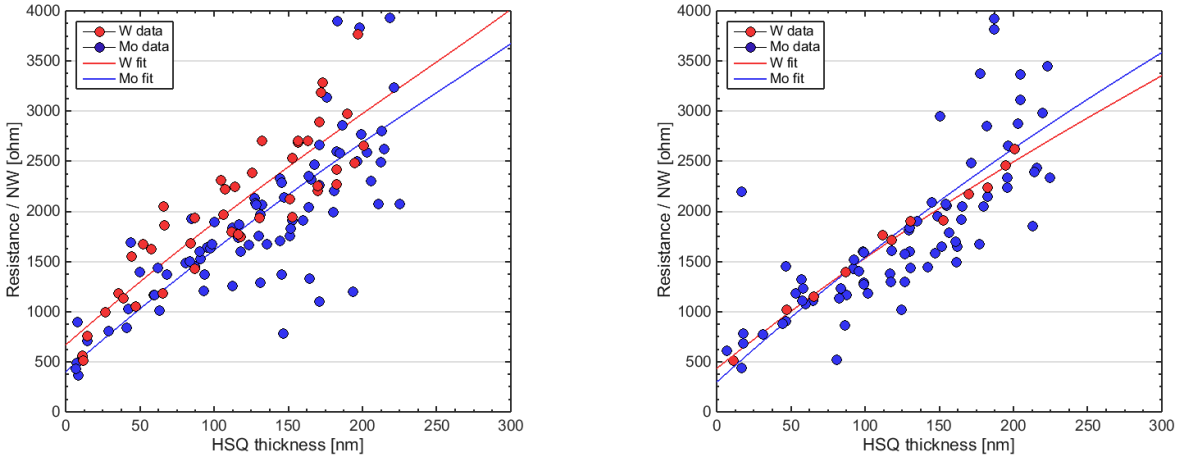

FIGURE 6.7: TLM plots of the InGaAs NW resistor samples. The left figure shows the TLM measurements of thinner NWs compared to the right figure. These TLM plots show adjusted data and fits.

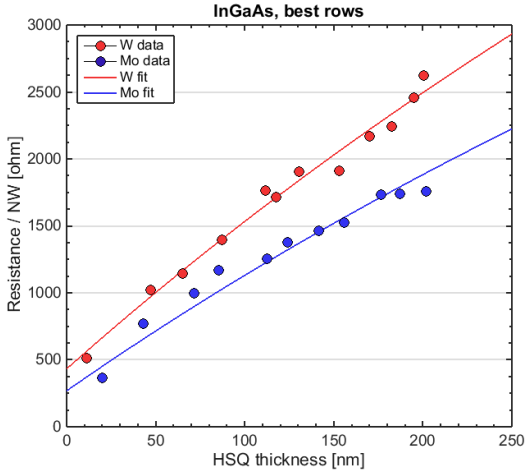

FIGURE 6.8: TLM plots comparing the contact metals for the InGaAs NW resistors.

TABLE 6.2: Calculated parameters from the InGaAs TLM samples. The errors in the measurements are thought to be large and will instead of being estimated by a number be discussed at the end of the chapter.

InGaAs (W)			
Seed size [nm]	$\boldsymbol{\rho_s}$ [$\Omega \cdot \mu$m]	$\boldsymbol{\rho_c}$ [$\Omega \cdot \mu$m^2]	$\boldsymbol{L_T}$ [nm]
∼18	34.7	25.4	105
∼21	41.6	10.4	67.5
∼21 (Best row)	43.5	2.97	35.9
InGaAs (Mo)			
Seed size [nm]	$\boldsymbol{\rho_s}$ [$\Omega \cdot \mu$m]	$\boldsymbol{\rho_c}$ [$\Omega \cdot \mu$m^2]	$\boldsymbol{L_T}$ [nm]
∼19	33.7	15.5	85.0
∼22	46.2	7.15	53.0
∼22 (Best row)	33.2	1.59	29.7

Judging by the calculated values in Table 6.2, Mo seems to be a better contact metal for InGaAs NWs compared to W. This is predicted as the contact resistivity of Mo contacts on n^+-InGaAs have been reported to be as low as 0.69 $\Omega \cdot \mu$m^2 for planar devices [30], and 1.3 $\Omega \cdot \mu$m^2 in III-V fins [31]. The specific contact resistivity measured for Mo in this study is really close to these low values.

The conducted TLM studies imply that the InAs NW resistors roughly have a factor two lower resistivity than $In_{0.2}Ga_{0.8}As$, which is quite expected due to higher electron mobility in InAs. The specific contact resistivity between the two semiconductor materials also seem to be better for InAs when fitting data, although the gap might be smaller if the best measured rows are compared to each other. For the best rows, using Mo as a contact metal provided specific contact resistivities below 2 $\Omega \cdot \mu$m^2 for both InAs and $In_{0.2}Ga_{0.8}As$.

6.4 TLM obstacles

In the TLM measurements, several obstacles arose, especially for the InGaAs samples but also for InAs. These problems are to be mentioned in this section starting with the SEM figure below (Fig. 6.9) illustrating one complication of growing NWs with too small seed particles. This problem was more severe for InAs. Adding to this, as there were

hundreds of NW arrays on each individual sample, all arrays were not inspected by SEM and therefore it is reasonable to believe that a fair amount of the used data had some defects which was not taken into account when analysing it.

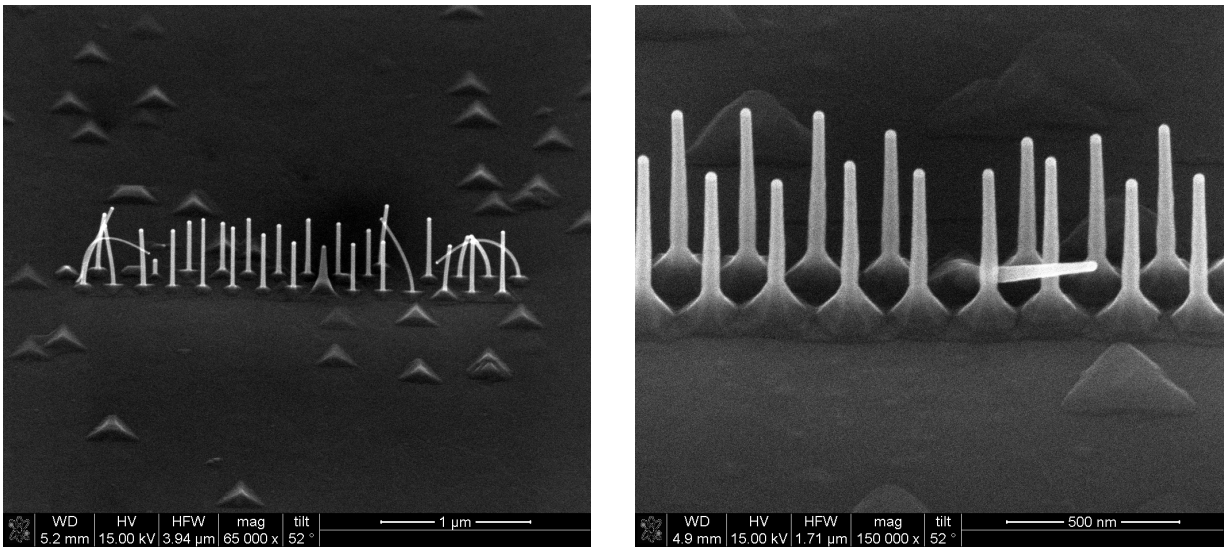

FIGURE 6.9: SEM images depicting observed problems with longer NWs. In (a) an array of InAs NWs are shown where the seed particle size was at its smallest. The image shows large inconsistencies between the wires and the outermost wires grow too long and bend to a non-functional degree. The InGaAs NWs was seen to be more consistent but in some arrays, as the one shown in (b), fallen NWs could be observed. This also happened when the seed particle size was small.

When processing the Mo contact samples, the etchant (HF) was thought to have etched through the InAs buffer layer. This suspicion was verified by inspecting the samples with SEM where 300 nm trenches could be observed corresponding to the thickness of the InAs layer. The consequences of this is however hard to estimate as the TLM characteristics still could be recognised with comparable, if not better, results compared to the W contact samples. It could although explain why there seems to be more spread in the measured resistance in these samples.

As already mentioned, the heterojunction in the InGaAs samples causes concern whether the resistance of the NWs can be calculated by Ohm's law and if Ohm's law is a valid approximation in this specific case. But beside this, more approximations were assumed when modifying the TLM equations for the non-cylindric form of the wires. The most obvious assumption is the radius of the wires having a perfectly linear height dependence, which is a simplification. Another assumption is that the material properties stays the

same throughout the wire with e.g. the same resistivity independent on radius and distance from the highly doped InAs layer. The transfer length is also assumed to stay constant in the InGaAs TLM model, although it might be highly unlikely because of the varying radius which further changes the contact area.

6.5 Errors

For all possible errors in the conducted TLM measurements, inaccuracies in determining the device dimension are thought to give the highest uncertainties to the calculated parameters. As the thickness of the HSQ spacers in the samples were determined from optical microscope pictures calibrated to profilometer data in MATLAB, the HSQ thickness errors originates from two independent sources. The profilometer has a resolution of 20 nm and the largest observed deviation when converting RGB values to HSQ thickness was also 20 nm, resulting in a $\pm$30 nm uncertainty for the spacer thickness. Because the TLM equations are sensitive to changes in spacer thickness, large errors in ρ_c are observed when fitting data having the HSQ thickness $\pm$30 nm. Due to the complex relation between the involved equations the affect of these errors on the contact resistivity depends on the evaluated row. The spread due to the thickness uncertainty was seen to range from 0.2-6 $\Omega \cdot \mu m^2$ for the InAs sample contacted with Mo and 0.8-7 $\Omega \cdot \mu m^2$ for the W-contacted NWs. The InGaAs samples had showed a spread from 0.6-11 $\Omega \cdot \mu m^2$ with Mo-contacts and 1-10 $\Omega \cdot \mu m^2$ when having W as contact metal.

There are other errors in the measurements as well. The diameter and height of the NWs were deduced from SEM-images where the error is thought to be around $\pm$3 nm. This difference does not have as big impact on the contact resistivity as the inaccuracy of the HSQ spacer thickness. Because of the large errors in the conducted TLM study, the precision of the numerical parameter values is not sufficient to conclude that Mo really is better than W as a contact metal for InAs and InGaAs. The data does however hint that this might be the case and that the metals at least show comparable results.

Chapter 7

Conclusions and Outlook

In this work it has been concluded that implementing a shell around the bottom of a vertical NWFET enhances its DC performance in terms of g_{m}, I_{on} and V_{T}. The shell does however create a substantial potential drop at its edge which could degrade stability and cause earlier device breakdown. This effect can to some extent be observed to weaken by prolonging the gate over the shell as the narrow gap between conduction and valence band becomes slightly larger. The new device geometry is concluded to operate better and more stable if the bottom contact is grounded. When top grounded, the device becomes more sensitive to geometry changes. Although, the simulated NWFETs in this project were made with restricted physical models and limited geometrical details, the resulting performance metrics and IV-curves were still found to be in good agreement with results from real devices. Continuing these studies with more realistic models concerning carrier transport, mobility, breakdown events and heterojunctions, could therefore greatly support optimization in these devices.

The TLM studies showcases Mo as a potentially better contact metal for both InAs and InGaAs NWs compared to W. Plotting the TLM data from several rows in order to calculate the material parameters shows that there was a huge data spread for the samples. This spread was observed to degrade the TLM-fit and it presumably originates from possible processing errors when etching the metal contacts. But if individual rows instead were evaluated, the fit was seen to become greatly improved. Mo could then be seen to have excellent specific contact resistivity below 2 $\Omega\mu\mathrm{m}^2$ for both InAs and $\mathrm{In}_{0.2}\mathrm{Ga}_{0.8}\mathrm{As}$. There are however large uncertainties in the measurements due to the

errors mainly originating from determining the HSQ spacer thickness. Because of this, it is hard to confidently confirm that Mo is a better suited contact metal compared to W for InAs/InGaAs NWs, although the data hints towards that conclusion.

Therefore these values may better be viewed more as a probable possibility, rather than a confirmation, that Mo is a better contact metal compared to W for InAs/InGaAs NWs.

In this thesis, a complimentary TLM-model applicable for non-cylindrical NW resistors was also presented. This model can be used as a valuable first degree approximation when calculating L_{T}, ρ_{c} and ρ_{s} for the InGaAs samples. A varying cross-section in TLM studies are however still problematic and further revision may therefore be required improve this model. As extrinsic contact resistances are predicted to ultimately cap performances of ultra scaled NW devices, it is undoubtedly important to continue researching how to minimize it for further device optimization.

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