Optimization of through-silicon via structures in a fingerprint sensor package

Fingerprint Cards AB

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ABSTRACT

The through-silicon via (TSV) is a type of vertical electrical connection that can pass through a silicon wafer or die. By using TSVs, compared to using wire bonding as interconnections in a capacitive fingerprint sensor, the capacitive strength between the sensor die and the finger can be increased. However, since TSV structures are both more complex as structures and have a more complex manufacturing process compared to wire bonding, reliability can be an issue. This thesis studies a TSV structure that failed qualification in where the aim was to find the root cause of the failure and to find how the material parameters affect the reliability of the TSV. A set of changes in process steps and materials used have been evaluated both by cross-section analysis and thermomechanical finite element analysis (FEA) simulations. The root cause of the failure could not fully be determined, but the cross-section analysis and FEA simulations showed that the usage of low coefficient of thermal expansion (CTE) polymers and high modulus trench fill could reduce the delamination ratio in the TSV.

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ABBREVIATIONS

CMOS	Complementary Metal-Oxide Semiconductor
CTE	Coefficient of Thermal Expansion
DOE	Design of Experiments
E	Young's Modulus
EMC	Epoxy Mold Compound (=Overmold)
FEA	Finite Element Analysis
FT	Final Test
FPC	Fingerprint Cards
HTSL	High-Temperature Storage Life
JEDEC	Joint Electron Device Engineering Council
LGA	Land Grid Array
OEM	Original Equipment Manufacturer
OSAT	Outsourced Semiconductor Assembly and Test
PSV	Passivation
POR	Plan of Record
RDL	Redistribution Layer
SAT	Scanning Acoustic Tomography
SEM	Scanning Electron Microscopy
SiP	System in Package
SM	Solder Mask
TC	Temperature Cycling
T_g	Glass-transition Temperature
TSV	Through-Silicon Via
uHAST	Unbiased Highly Accelerated Temperature and Humidity Stress Test

1 INTRODUCTION

Identification by fingerprint recognition has been done for over a hundred years. Previously done with ink and paper, it provided a primitive but working method of identification by comparing the patterns of our unique fingerprints [1]. Nowadays fingerprint recognition can be realized with semiconductor technology in general and silicon CMOS (complementary metal–oxide–semiconductor) technology in particular. Recently, sensors like these have become available and are today often integrated in consumer electronics such as computers and smartphones. For smartphone applications, capacitive fingerprint sensors are the most common type of fingerprint sensor due to its high image quality, low price, low power consumption and small size [2].

For smartphone users, certain design features of the smartphone are the most important, some of them include the display screen and button design [3]. The integration of a fingerprint sensor in a smartphone is usually done under a physical home button on the front side. To improve the design of the smartphone display, the fingerprint sensor could be placed underneath the cover glass of the phone which enables removal of the physical button on the front side. However, for a capacitive fingerprint sensor, the thicker the material covering the sensor die, the weaker the capacitance is between the finger and the sensor die.

Since the fingerprint sensor needs input from the finger, the sensor die must be packaged to protect it during usage. Also, the sensor die needs to have electrical connections from its bond pads. Using wire bonding which is a conventional type of interconnection will add height to the package. This will reduce the capacitance between the finger and the sensor die which will decrease the image quality. Using wire bonding will not be a problem unless the fingerprint sensor is to be integrated under glass. Instead of wire bonding, through-silicon vias (TSV) can be used as interconnections. Compared to wire bonding, TSV is a more complex type of interconnection where the connections are going through the sensor die. This will reduce the height above the sensor die enabling easier integration of the sensor under glass [4].

In this thesis, a TSV structure in a fingerprint sensor package from the company Fingerprint Cards AB (FPC) which failed qualification is studied. The aims of the thesis are to find the root cause of why the TSV failed qualifications, to evaluate how the material parameters of the TSV affect the reliability and to find a TSV structure that can pass new qualification tests. To improve the TSV structure, several changes of manufacturing processes and/or materials used will be performed, also known as design of experiments (DOE). Packages with the new TSV structures will be assembled and a new set of qualification tests will be performed on them. Thermomechanical finite element analysis (FEA) simulations on the TSVs for the DOEs are going to be performed to see if the results of the new qualification tests could be predicted. Also, simulations on how the material parameters affect the reliability of the TSV will be performed. Since the total time of manufacturing and qualification test is almost two months while each simulation takes a minute, if the results of the simulations match with the manufactured TSVs, this could reduce the time and money spent on development. The aim of the DOE study is to find a TSV structure that can be qualified, which can also help to understand why the first TSV structure failed qualifications. If any of the DOEs pass the requalification, this will enable the sensor die to be placed under glass which can improve the design of smartphones.

2 BACKGROUND

2.1 THE CAPACITIVE FINGERPRINT SENSOR

This study is conducted on a capacitive fingerprint sensor (Figure 1). Capacitance is the ability of a body to hold electrical charge. A capacitive fingerprint sensor generates the fingerprint image with the help of a matrix containing thousands of small capacitor plates where each of them acts as one plate of a parallel-plate capacitor, while the dermal layer of the finger, which is electrically conductive, acts as the other plate [2].

The capacitance of a parallel-plate capacitor can be expressed as:

$$C = \frac{\varepsilon A}{d} \qquad (1)$$

where C is the capacitance, ε is the permittivity of the material between the plates, A is the area of the plates and d is the distance between the two plates [5]. Using Equation 1, it can be seen that the capacitance is higher the shorter the distance between the plates and for materials with high permittivity.

In an ideal capacitor, the capacitance has the relation

$$C = \frac{Q}{V} \qquad (2)$$

where Q is the amount of charge on the plates and V is the potential difference between the conductors [5]. Combining equation 1 and 2 it can be realized that if the potential difference is the same between the finger and the capacitor plates, more charge will be accumulated on the plates with high capacitance.

The sensor studied in this thesis consists of a 176 x 64 matrix of capacitor plates where each of the plates acts as a pixel in the final image. By applying voltage to the capacitor plates, charges will build up on these plates. Depending on if the plate is beneath a fingerprint ridge or valley, the capacitance will differ. Plates with high capacitance are beneath the ridge of a fingerprint since the distance between the plate and the fingerprint is less compared to if the plate would be beneath the fingerprint valley. By reading

out the charges that are built up on the capacitor plates, the sensor measures the capacitance pattern across the matrix of pixels. The measured values are digitized by the sensor and sent to the microprocessor in the phone in which an algorithm is validating the image captured of the fingerprint.

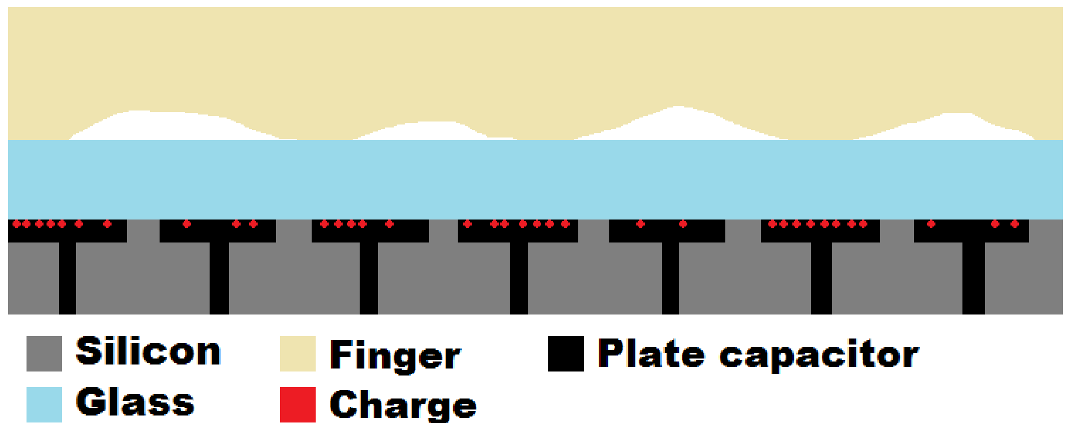

Figure 1: Schematics of capacitive fingerprint sensing. More charge is accumulated for the plates underneath a fingerprint ridge.

The sensor consists of a sensor chip which reads out the fingerprint image and a companion chip which supplies the sensor chip with voltage. These chips consist of CMOS technology at the 180 nm node and are manufactured on 8-inch wafers (Figure 2) at a foundry. These wafers are shipped to an OSAT (outsourced semiconductor assembly and test) in where TSVs are processed on the wafers. The wafers are then diced and sent to another OSAT where the dies are packaged in land grid array (LGA) packages (Figure 2). The LGA differs from other types of packages since the contacts consist of flat pads. The packaged sensors are then sent to a module house where the packages are assembled into a module (Figure 2). At the module house, the packages are attached to a flexible substrate with passive components and connectors to the phone. An adhesive layer and an ink layer is then applied on top of the packages on which a glass piece is then attached. The modules are then sold to an OEM (original equipment manufacturer) where they are assembled into the end product, in this case a smartphone.

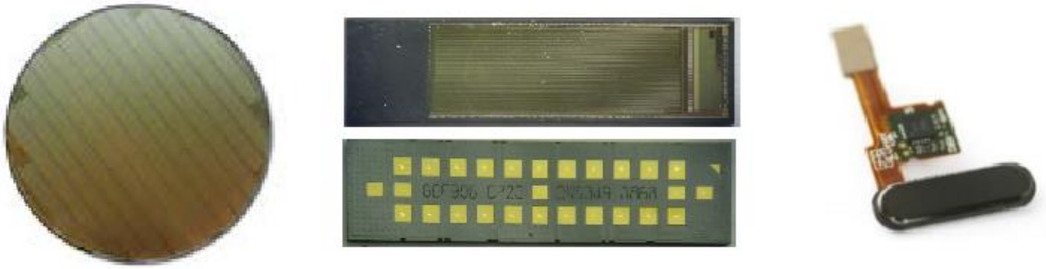

Figure 2: Left image showing an 8-inch wafer with sensor dies. Middle image showing the top and bottom part of a sensor package in the form of an LGA consisting of a sensor die, companion chip and capacitors. Right image showing a sensor module consisting of a sensor package with glass on top, mounted on a flexible printed circuit board with additional passives and connections. [6]

2.2 THE FINGERPRINT SENSOR PACKAGE

Since the sensor die consists of a thin piece of silicon with sensitive transistors, the sensor die must be packaged to protect it during usage. For example, the sensor die needs to be protected from mechanical pressure and static discharge from the fingers. There also need to be electrical connections from the sensor die to the companion chip and to the phone. Designing a package for a fingerprint sensor can provide a challenge since the packaging needs to be robust for everyday usage while fulfilling the requirements from the OEMs whom want small packages for better integration into the smartphone. The package design must also allow the sensor to last longer than the product it is assembled into [2].

To prove that the sensor package is durable enough, the sensor manufacturer can qualify the sensor package through several qualification tests. These tests include high temperature storage life (HTSL) where the package is stored at elevated temperatures, preconditioning where processing conditions of the sensor is simulated, unbiased highly accelerated temperature and humidity stress test (uHAST) where the package is stored at elevated temperatures and humidity and temperature cycling (TC) where the package is cycled through alternating high and low temperatures. Some of these tests take a long time to perform. For example, TC with 700 cycles (TC 700) takes two weeks.

When designing a fingerprint sensor package, other aspects than the functionality should be considered, the final sensor also needs to be visually appealing for the consumer. Currently, the trend for fingerprint sensors in smartphones is to place the sensor under glass for better design integration [7]. This will add a challenge since the piece of glass must be thick enough to withstand the mechanical pressure from the finger. For a capacitive sensor, the greater the distance is between the finger and the sensor die, the lower the signal strength will get and each pixel will receive more signal from other parts of the finger that is not directly above the pixel.

Currently, the most common type of fingerprint sensor package at FPC is an overmolded (EMC) wire bond package due to its simplicity and low cost. Thin metal wires connect the bond pads of the sensor to a substrate which is then molded, protecting the sensor die and the bond wires (Figure 3 b). If the wire bonded sensor is under glass, the total distance between the finger and the sensor die will mainly be the mold height and glass height. For a capacitive sensor, the distance between the finger and sensor die should be as small as possible which makes the wire bonding solution for a sensor under glass challenging to achieve. Instead of using wire bonding where the wires are protruding from the sensor die, TSV interconnections (Figure 3 a) are used in the sensor package studied in this thesis. In this solution, the sensor die is etched from the backside and the electrical connections go through the die. The total distance between the finger and the sensor die will then mainly consist of the glass height.

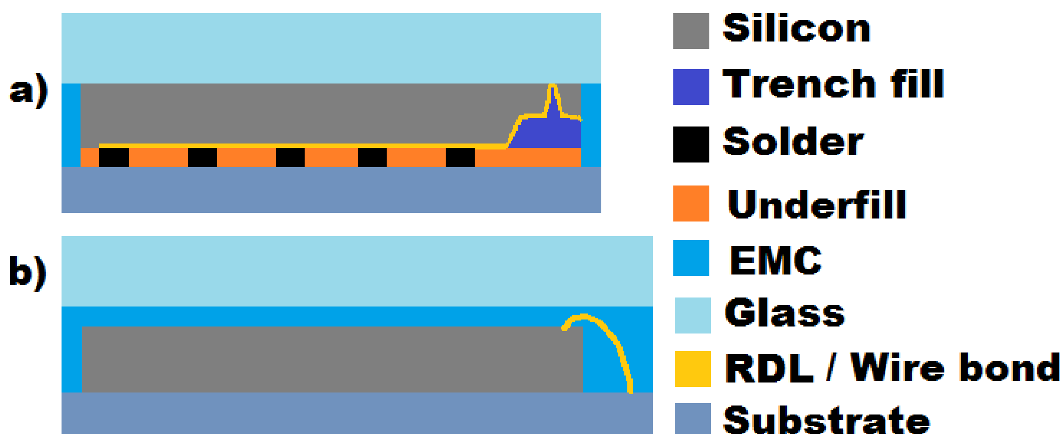

Figure 3: Stack-up comparison between two types of fingerprint sensor packages under glass. a) Showing a TSV solution where the connections from the sensor die go through the die. b) Showing an overmolded wire bond solution where wires are used as interconnections. Note that the distance between the sensor die and the top of the glass is shorter in the TSV solution.

2.3 THROUGH-SILICON VIA (TSV)

The TSV was first invented in 1958, when William Shockley filed a patent that described how can be used to connect two wafers together, but it is only recently that TSVs are available for mass production. Using TSVs as interconnections, it enables reduced interconnection length since the connections go through the silicon die. Compared to wire bonding, using TSVs as interconnections enables higher speed communications, lower power consumption and the possibility to use a higher number of interconnections [4]. As mentioned before, another benefit of using TSV interconnections in a fingerprint sensor package is that the distance between the sensor die and the finger can be reduced.

Compared to wire bonding, TSV is a complex type of interconnection with many process steps (see chapter 2.4). The total time of manufacturing takes two weeks and because of the long process time and numerous process steps it is also a more expensive method than wire bonding. Due to the structures being more complex, the risk of failure during the qualification tests also increases [4].

The sensor in this study has nineteen I/O, which translates to nineteen bond pads and nineteen TSVs (Figure 4). These signals are for example power supplies, ground connections, signals used for testing the sensor and signals for image transfer of the fingerprint.

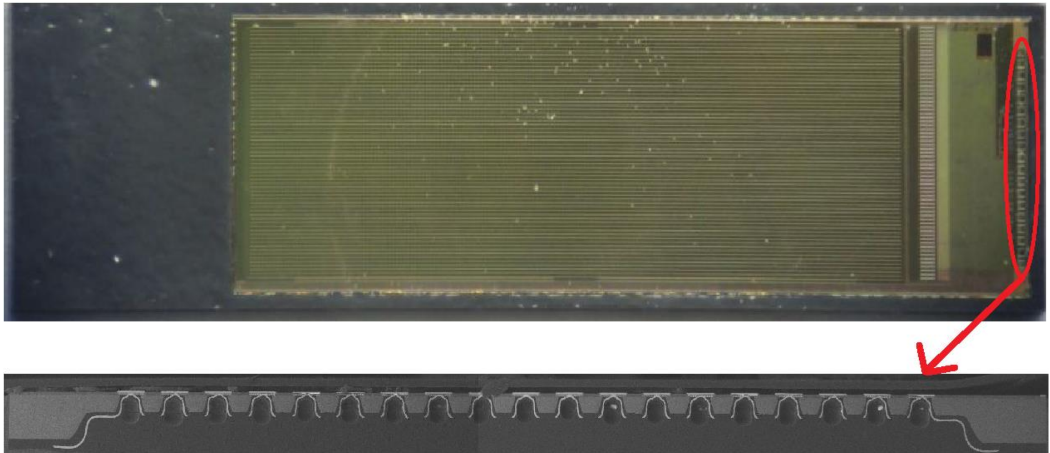

Figure 4: The location of the bond pads and TSVs on the sensor package with a scanning electron microscope (SEM) cross-section image of the whole row of TSVs.

The type of TSV used in the sensor is a polymer filled via last TSV (Figure 5). Via last means that the TSV is processed after the integrated circuit fabrication. Other types of TSVs include copper filled TSV and via first TSV where the TSVs are processed before the integrated circuit fabrication [4]. The polymer filled TSV has different parts which consist of different materials with different properties. From the bond pad, which consists mostly of aluminum, the redistribution layer (RDL) connects the sensor die with the substrate in the package. The RDL consists of four layers of metal; titanium, copper, nickel and gold where the thickest layer is copper. Titanium is an adhesive for the RDL on the passivation (PSV) layer, the copper layer is conductive and nickel acts as a diffusion barrier for the final gold layer which protects the RDL from oxidation [8].

Between the silicon die and the RDL is a dielectric polymer layer, also called passivation layer. On the other side of the RDL is another dielectric polymer layer called the solder mask (SM). This layer will act as a mask to protect the RDL metallization layer. The TSV is also filled with a polymer, the trench fill, which increases the mechanical stability of the TSV [9].

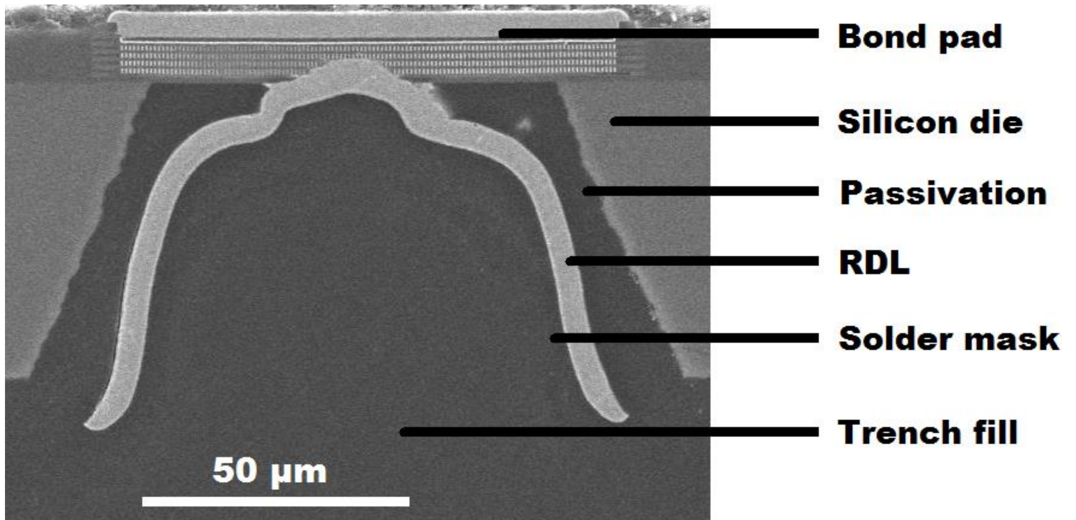

Figure 5: SEM cross-section image of a polymer filled TSV.

2.4 TSV MANUFACTURING PROCESS

The packaging process of the fingerprint sensor is a long process with many steps. For this process, two OSATs are involved, OSAT A which manufactures the TSVs and OSAT B which assembles the LGA packages. Here, the manufacturing process with the most important process steps for the plan of record (POR) build is presented (Figure 6). Refer to Table 1 at p.22 for materials used and Table 2 at p.23 for their respective properties.

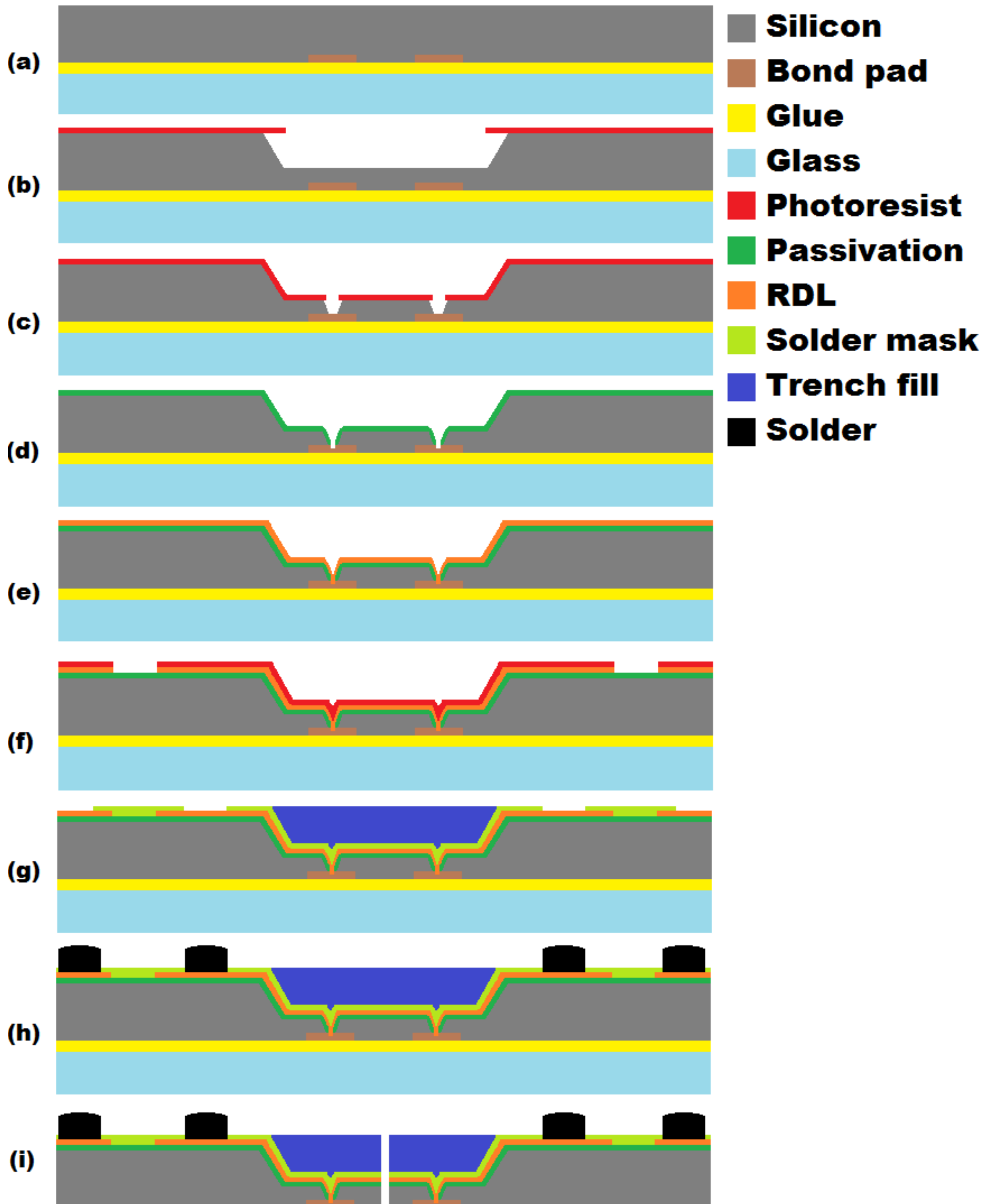

Figure 6: Schematics of the TSV process showing side view of the end points of two dies on the wafer. a) Bonding of glass wafer and backgrinding b) Trench etch c) Via etch d) Passivation deposition with laser removal at bond pad locations e) RDL plating f) RDL etch g) Solder mask deposition and trench filling h) Stencil printing and reflow i) Debonding of glass wafer and dicing

At OSAT A, the packaging process starts with incoming 8-inch Si wafers which contain sensor dies manufactured at a foundry. The Si wafers are glued on glass carrier wafers with the active side facing the glass wafer. These glass carrier wafers protect the Si wafers from breaking and protect the active side from contamination during the TSV process [4]. The Si wafers are then grinded on the backside with a diamond wheel to decrease its thickness and then later lapped to make the surface more uniform. This process induces stress in the silicon that could propagate through the whole wafer. To release the induced stress from the grinding, the wafers are plasma etched (Figure 6 a) [4].

After the plasma etching, a negative photoresist is spin coated on the wafers. The photoresist is baked and then light is exposed everywhere on the wafers except at the trench locations. Since the photoresist is negative, the unexposed regions will be removed when developed [10]. The wafers are then plasma dry etched which creates an anisotropic etch profile (Figure 6 b) [10]. After the trenches are etched, the remaining photoresist is removed and the wafers are once again coated with photoresist. Since the surface of the wafers are uneven because of the trenches, instead of spin coating, the wafers are spray coated to create an even surface. The photoresist is baked and then the via locations are exposed by light. Since the photoresist is positive, the exposed regions will be removed when developed [10]. The vias are plasma dry etched which once again creates an anisotropic etch profile (Figure 6 c). The remaining photoresist is then removed.

Next, a thin passivation layer is sprayed on the wafers. The passivation layer is then baked to remove its moisture. The bond pads will then be covered by a passivation layer, and to expose them, a laser is used (Figure 6 d). To form the RDL, a thin layer of titanium is sputtered on the wafers. Sputtering is a process where a solid material is bombarded by energetic particles. Particles from that material are ejected and deposited on a target which creates a uniform layer [10]. Copper is then sputtered on the wafers forming a seed layer followed by the wafers being electroplated with copper (Figure 6 e). Electroplating is a process in which a metal is coated on an object by immersing the object and a bar of the metal in a solution containing the metal ions. By applying a current, the metal bar dissolves and plates on the object which forms a coating of the metal [11]. To create the RDL pattern, the

positive photoresist is once again sprayed on the wafers and the RDL areas are exposed to light. Subsequently, the copper and titanium are etched away in all the unwanted areas and a thin layer of nickel and gold is plated on the RDL (Figure 6 f).

A negative photosensitive solder mask is then sprayed on the wafers. After light exposure and development, openings are created on the locations where the solder bumps will connect the RDL to the substrate (Figure 6 g). After the solder mask deposition, the trenches are filled with epoxy (trench fill) from a dispenser (Figure 6 g). Next, solder paste is deposited on the solder mask openings with stencil printing, a process where solder paste is deposited over a mask forming cylindrical shapes of solder paste. The wafers then go through reflow in which the temperature is elevated to 240 °C and then cooled down again to room temperature. The solder paste is first melted due to the elevated temperature, and as the temperature is cooled down, solder bumps are formed (Figure 6 h). The glass carrier wafers are then debonded from the wafers whom are then diced and shipped to OSAT B (Figure 6 i).

2.5 PACKAGE ASSEMBLY

At OSAT B, the TSV processed sensor dies arrive from OSAT A (chapter 2.4). These dies together with a companion chip will form a system in package (SiP) in the form of an LGA package. The package assembly starts when solder paste is printed on a substrate and the sensor dies from OSAT A and the companion chips are placed on the substrate (Figure 7 a). The solder paste goes through reflow in where the sensor dies, the companion chips and capacitors are soldered and electrically connected to the substrate. The package is then cleaned by both a solvent and plasma to remove the flux residues from the solder paste.

Underfill is dispensed in the gap between the dies and the substrate and is then cured (Figure 7 b). The underfill provides stronger mechanical connection and distributes the thermal expansion mismatch between the dies and the substrate [12]. The substrate with attached dies is then molded by film assisted molding which improves the mechanical properties of the packages and protects the sides from contamination [13] (Figure 7 c). The packages are

then singulated and sent to a module house. If a new kind of package is assembled, instead of being sent to a module house, they go through a qualification test.

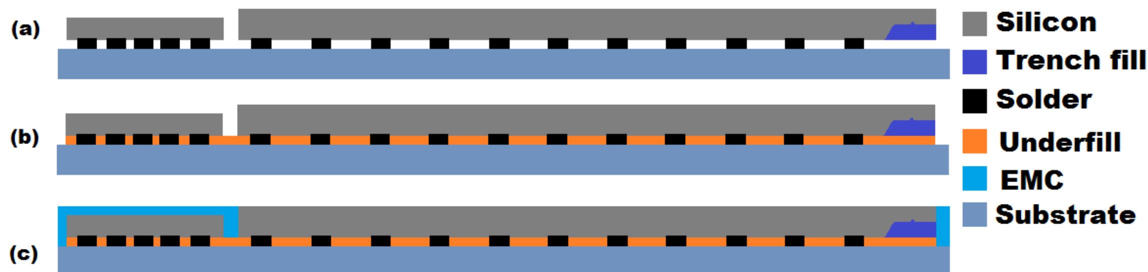

Figure 7: Schematics of a package assembly where smaller details such as the passivation layers and RDL are not shown. a) Surface-mount of sensor die and companion chip on substrate and reflow b) Underfill dispensing and cure c) Film assisted molding.

2.6 QUALIFICATION TEST

Before mass production, newly designed and manufactured packages need to be qualified to ensure that the sensors will function longer than the lifetime of the product it will be assembled into. Since a smartphone is expected to last for several years, tests that simulate years of usage are needed. FPC's own flowchart of the qualification for a new sensor package can be seen in Figure 8. To ensure that the time of manufacturing is not affecting the sensor performance, three non-consecutive lot sensor wafers and 3 non-consecutive lot companion chip wafers are built into three lots of packages. These lots contain 75 packages each for a total of 225 packages and 25 packages from each lot are then going through different kind of standardized tests that all follow JEDEC (Joint Electron Device Engineering Council) standard. Before going through these tests, the packages are going through final test (FT) and scanning acoustic tomography (SAT). The final test is testing the functionality of the integrated circuits and includes an open/short test where the package is probed to find open or short signals. SAT scan is a method where ultrasonic sound waves are probing the package for mechanical defects such as delamination [14].

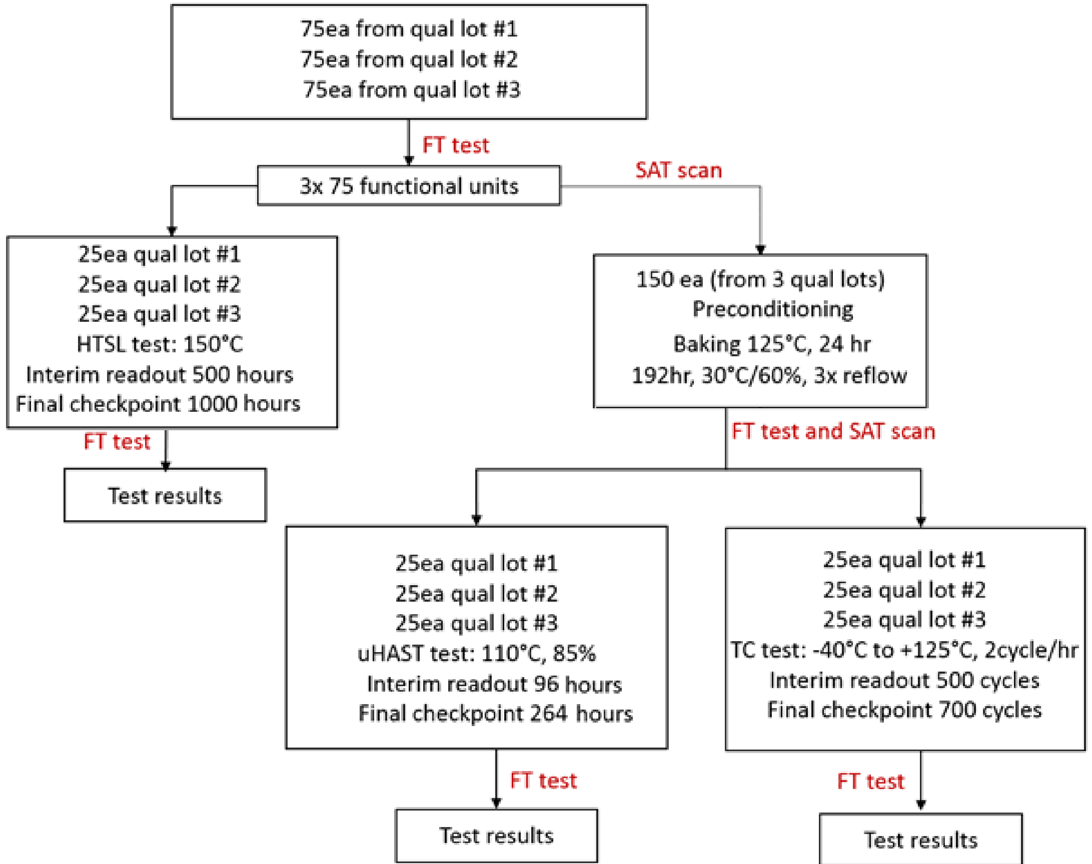

Figure 8: Flowchart of qualification for a new fingerprint package [6].

2.6.1 High temperature storage life

25 packages from each of the three different lots go through HTSL. In this test, the packages are stored at an elevated temperature of 150 °C without any bias applied to them for 1000 hours. After 500 hours, there is an interim readout to see if the sensors are functioning and after the full 1000 hours the test is completed, followed by final test. The results of the final test should match the results of the final test prior to the HTSL. Also, the package is checked for mechanical damage such as cracking, chipping, or breaking. To be qualified, all packages need to pass the open/short test and no mechanical damage can be observed [15].

2.6.2 Preconditioning

Before proceeding with temperature cycling and uHAST, a preconditioning test is performed. The aim for preconditioning is to simulate the floor life during module assembly. The preconditioning starts with 150 of the packages going through a baking step at 125 °C for 24 hours to remove all moisture from the package. Then the packages are exposed to a moisture soak step for 192 hours with a temperature of 30 °C and a relative humidity of 60%. This step resembles the storage times of the packages before module assembly. Lastly, the packages are going through reflow three times to simulate module assembly [16]. After preconditioning, the 150 units are going through final test and are SAT scanned. The 150 units are then divided, where one half goes through uHAST and the other half goes through TC.

2.6.3 Unbiased highly accelerated temperature and humidity stress test

After preconditioning, half of the packages go through uHAST with the aim to evaluate the reliability of the package in humid environments. The packages are exposed to a temperature of 110 °C and a relative humidity of 85% for a total of 264 hours with an interim readout at 96 hours. The test is highly accelerated since a combination of high temperature and high humidity accelerates the penetration of moisture through the external protective material [17]. After the 264 hours, the 75 units go through final test and all packages must pass the open/short test to be qualified.

2.6.4 Temperature cycling

After preconditioning, the other half of the packages go through a temperature cycle test to determine the ability of the interconnections and the components to withstand mechanical stresses induced by cycling temperatures. The packages are exposed to a cycling temperature between -40 °C and 125 °C

with two cycles each hour for 700 cycles with an interim readout at 500 cycles [18]. Since the TSV has many layers of materials with different properties such as the coefficient of thermal expansion (CTE), the layers will expand and shrink at different rates, which will induce stress in the TSV. After the 700 cycles, the 75 units go through final test and all packages must pass the open/short test to be qualified.

2.7 POR BUILD QUALIFICATION RESULTS

The POR build was packaged as described in chapter 2.4 and 2.5. and qualified as described in chapter 2.6. For HTSL and uHAST, all 150 units passed the open/short test, but for the temperature cycling test, two units failed. Since two of the units failed the open/short test, the package was not qualified for mass production. An open signal could be detected at the bond pad locations on both failed units. Cross-sectioning was performed at OSAT B to find the source of the open signal, in where the dies are cut across the bond pads and then grinded at the cut locations to create a smooth surface. From the cross-section images, the cause of the open signal was found to be a crack between the bond band and the RDL (Figure 9). In the same images, delamination could also be seen between the RDL and the passivation layers.

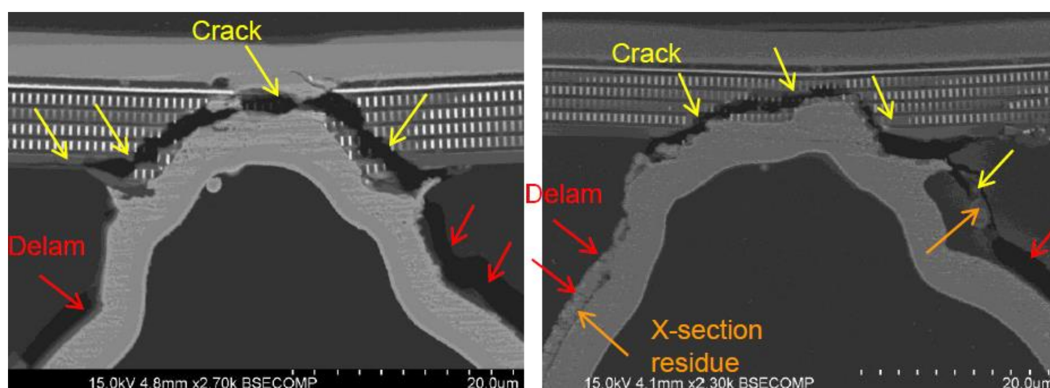

Figure 9: SEM images of the two failed units showing crack between the RDL and the bond pad resulting in an open circuit.

Other cross-section images showed that delamination had occurred at various locations in other TSVs which passed the open/short test. Most commonly the delamination occurred at the outer sidewalls of the RDL, but delamination was also found at the inner sidewalls and close to the bond pads. However, if there was no crack between the RDL and the bond pad, the sensor passed the open/short test. The cross-section images also showed that some of the trenches had not been filled with trench fill, resulting in a void in the TSV (Figure 10).

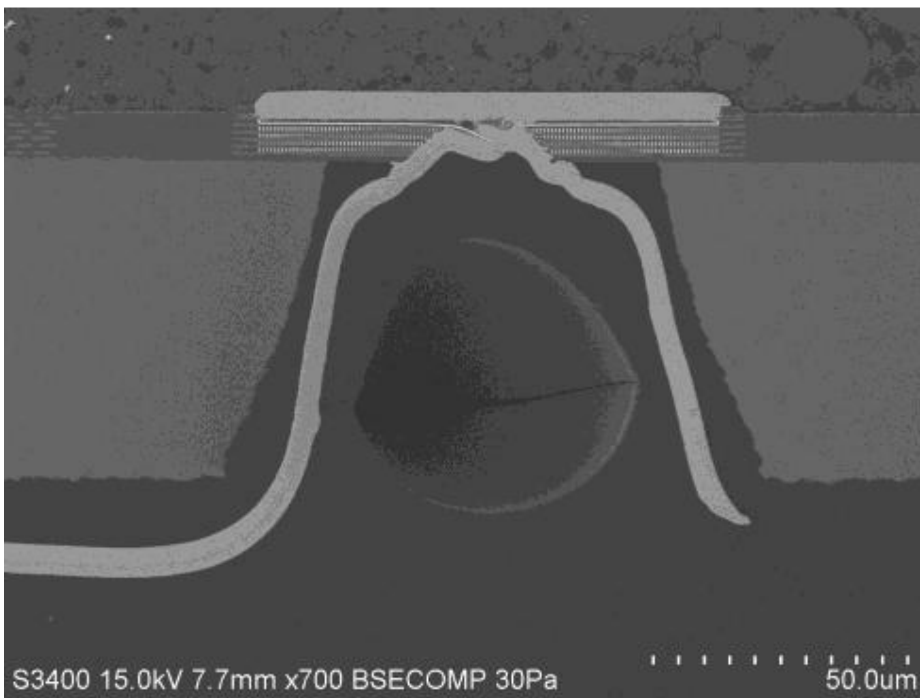

Figure 10: TSV with void.

3 METHODS

3.1 DESIGN OF EXPERIMENTS

Since the sensor package could not be qualified for mass production, the packaging process had to be changed. With a manufacturing time of a month and qualification tests taking an additional month, it is not reliable to only make a single change in the process and expect the new package to pass qualification. For that reason, a set of different changes of process parameters and materials used (Table 2) were proposed, also known as a DOE study. By using a DOE study, the relationship between input variables affecting a process and the output of that process can be determined. In this DOE study, the delamination ratio in different TSV structures will be evaluated. The properties affecting the delamination ratio between two materials after temperature cycling are the interfacial adhesive properties and the thermomechanical properties of the two materials.

The requirements for this DOE study were that the packages would not increase in prize or change dimensions. The DOEs were also limited on the polymers available at OSAT A. In total nine different DOEs were proposed to OSAT A and B (Table 1). Six of the DOEs were manufactured in parallel since two of the proposed DOEs could not be manufactured and one were delayed.

Since the titanium is used as an adhesive layer in the RDL, it is a possibility that the thickness of the titanium layer in the POR build (0.15 µm) is insufficient and thus causing delamination [19]. By testing out two different thicknesses of titanium, one thicker 0.3 µm (DOE 1) and one thinner 0.1 µm (DOE 9), the effect of the titanium thickness can be examined.

Another possibility for the cause of the delamination could be an insufficient curing time of the passivation layer. If the passivation is not cured enough, moisture can be trapped in between the passivation layer and the RDL which can induce delamination [19]. DOE 2 increases the curing time of the passivation layer from one hour to one and a half hours. The POR build is using the same cure time and temperature for the passivation layer that is recommended from the data sheet.

A third possibility for the delamination is a high CTE mismatch of the materials. If two adjacent materials with different CTEs are exposed to a thermal load, they will expand or shrink at a different rate and stress will be induced, particularly at the interfaces of the two materials. Due to the differences in the thermomechanical properties, some of the stresses are high enough that delamination will occur at locations with high stress [19]. DOE 3-9 changes the polymers used in the TSV structure to reduce the CTE mismatch.

DOE 3 uses underfill as trench fill. Compared to the POR build, this change could benefit from no CTE mismatch between the underfill and the trench fill. Due to the trench fill dispenser was not capable of using underfill polymer at the time of the initial DOE build, this DOE was not investigated further. DOE 4 has a trench filling material mixture of trench fill and underfill which could act as a transition material between the underfill and the solder mask. DOE 4 could not be manufactured since a mixture of trench fill and underfill could not be made at OSAT A.

DOE 5 has the same materials used as another OSAT, OSAT C in their TSV process which has already been qualified for mass production for FPC. In their process, another passivation 5100 is used where the main difference is that 5100 has lower CTE compared to WLP32. Also, the trench filled used in their process can also be used as solder mask. DOE 5 could not be manufactured since only WLP32 can be used as passivation layer at OSAT A. DOE 6 has the same solder mask and trench fill as DOE 5, but with WLP32 as passivation layer which is compatible with OSAT A.

DOE 7-9 uses a trench fill material with lower CTE compared to the trench fill used in the POR structure. DOE 8 has another manufacturing process where the trench filling step is before solder mask deposition. In this way, similar to DOE 6, the vias will only be filled with one type of polymer. The other DOEs have two layers of polymer inside the via, both the solder mask and the trench fill.

In total, DOE 1, 2, 6, 7, 8 and 9 were processed at OSAT A and shipped together with previously processed POR dies to OSAT B for package assembly and qualification tests.

Table 1: List of DOEs

	Passivation cure	Ti thickness (µm)	Passivation	Solder mask	Trench fill	Notes
POR	150 °C 1 hour	0.15	WLP32	WLP32	353ND	Original process
DOE 1	150 °C 1.5 hours	0.15	WLP32	WLP32	353ND	Change of process cannot be simulated
DOE 2	150 °C 1 hour	0.3	WLP32	WLP32	353ND	Change of process cannot be simulated
DOE 3	150 °C 1 hour	0.15	WLP32	WLP32	8410-73C	Underfill used as trench fill, delayed at OSAT A
DOE 4	150 °C 1 hour	0.15	WLP32	WLP32	50% 353ND, 50% U410-73C	Not possible to create mixture at OSAT A
DOE 5	150 °C 1 hour	0.15	5100	LSF60	LSF60	5100 used at another OSAT, not possible to use at OSAT A
DOE 6	150 °C 1 hour	0.15	WLP32	LSF60	LSF60	
DOE 7	150 °C 1 hour	0.15	WLP32	WLP32	323LP	
DOE 8	150 °C 1 hour	0.15	WLP32	LSF60	323LP	Trench filling first, then solder mask
DOE 9	150 °C 1 hour	0.1	WLP32	WLP32	323LP	Change of process cannot be simulated

Table 2: List of materials used and their properties.

	Type	Tg (°C)	CTE<Tg (1/K)	CTE>Tg (1/K)	E<Tg (GPa)	E>Tg (GPa)	Poisson's ratio	Data from
WLP32	Passivation/Solder mask (Spray)	121	78	158	4.8	-	0.35*	Datasheet
353ND	Trench fill	90	54	206	3.56	-	0.35*	Datasheet
LSF60	Solder mask/Trench fill (Spin)	125	55	123	5.6	2.2	0.35*	Datasheet
323LP	Trench fill	100	31	132	2.67	-	0.35*	Datasheet
8410-73C	Underfill	88	31	95	11	0.08	0.35*	Datasheet
5100	Passivation (Spray)	291	54	-	2.5	-	0.35*	OSAT C
Silicon	Die	-	2.6	-	170	-	0.28	COMSOL material library
Copper	RDL	-	17	-	110	-	0.35	COMSOL material library
Aluminum	Pad	-	23	-	70	-	0.33	COMSOL material library

* *Property not characterized, the value is taken from similar materials.*

3.2 SIMULATIONS

During the manufacturing and the qualification tests, FEA simulations were performed to obtain the thermal stresses of the TSV structures induced by the temperature cycling for the different DOEs. One aim of the simulations was to simulate the different DOEs to make a comparison with the cross-section images obtained after temperature cycling. Another aim was to simulate how the material properties were affecting the induced stresses. COMSOL Multiphysics 5.2a with the structural mechanics module was used to perform the FEA simulations.

The simulations were done in 3D mode and the dimensions of the model (Figure 11) was built from data obtained from build instructions of the TSV and from SEM images of the TSV. Several simplifications were made to

make the simulations take less time and memory. The TSV was assumed in the model to be symmetric. The symmetry boundary condition was assigned on the two larger sides visible in Figure 11 making the simulations faster and less memory consuming compared using a full model of the TSV. In reality, the RDL extends on one side to connect with the solder bumps, but this model is neglecting that. Also, several material simplifications were made. The bond pad material was set as aluminum because that is the element it consists the most of. In reality, the bond pad is a complex structure which can be seen in Figure 5. The RDL was simplified to only consist of copper where the thin titanium, nickel and gold layers were neglected. The model also assumes perfect adhesion between the layers in which DOE 1, DOE 2 and the POR build will get the same simulation results. Also, DOE 7 and DOE 9 will get the same simulation results. Consequenty, the simulation results for DOE 1, DOE 2 and DOE 9 will not be presented in the results.

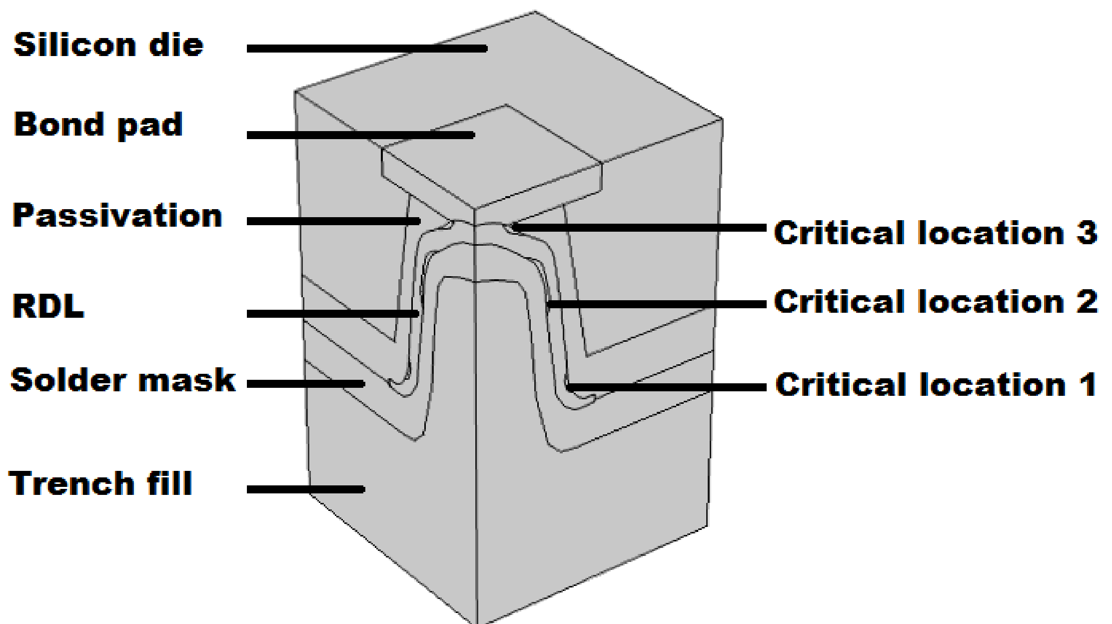

Figure 11: 3D model of the TSV structure with descriptions.

The material parameters used in the simulations were CTE, Young's modulus (E), Poisson's ratio and the glass-transition temperature (T_g). The material parameters used and from where the data were received, can be seen in Table 2. The viscoelastic properties of the polymers were not used in the model because they were not characterized. Viscoelasticity is a property which

means that materials are elastically and viscously deformed simultaneously, a common behavior of polymer materials. The deformation that occurs for a given stress depends on both time and temperature. When for example a polymer is heated up and then cooled down to its initial temperature, the total elastic deformation is zero while the viscoelastic deformation remains. The characterization of the viscoelastic properties of a polymer takes a lot of effort and time and is not performed in this thesis [20].

Due to not having the viscoelastic data of the materials and due to simulations where the temperatures are cycled being more complex, a linear simulation was performed. In the simulations, a temperature decrease from 125 °C to -40 °C was simulated. The stress-free temperature was assigned to 125 °C since previous studies have found that regardless of initial stress-free conditions, a package will readjust the stress-free state after a few cycles during temperature cycling to the highest temperature reached [21]. Therefore, the induced stresses in the model is a result from a temperature decrease in total of 165 °C.

The average von Mises stress (Equation 3), also known as the equivalent stress was evaluated at three different locations (shown in Figure 11) for the different DOEs. Also, another model of the POR build with a void included was simulated to see what influence the void has on the induced stresses. The von Mises stress is a scalar stress that can be calculated from the Cauchy stress tensor. σ_{xx}, σ_{yy}, and σ_{zz} represent normal stresses in Cartesian coordinates while σ_{xy}, σ_{yz}, and σ_{xz} represents shear stresses [22].

$$\sigma_{VM} = \sqrt{\frac{1}{2}[(\sigma_{xx} - \sigma_{yy})^2 + (\sigma_{yy} - \sigma_{zz})^2 + (\sigma_{zz} - \sigma_{xx})^2 + 6(\sigma_{xy}{}^2 + \sigma_{yz}{}^2 + \sigma_{xz}{}^2)]} \quad (3)$$

The three locations were chosen because delamination had been found in these areas, but the locations were defined in the model after an initial simulation to fit where the stress was concentrated (Figure 13). Critical location 1 is located on the outer sidewall of the RDL, critical location 2 is located on the inner sidewall of the RDL and critical location 3 is located near the interface of the bond pad (Figure 11).

The effect on the induced stress during temperature cycling for different polymers properties was also simulated. Parametric studies on CTE and Young's modulus were performed for the trench fill and for the passivation

layer and solder mask assuming they are the same polymer. The induced stress for the three critical locations was simulated for the polymers in the CTE range of 5 ppm/K to 100 ppm/K and the modulus range of 0.5 GPa to 10 GPa. Each combination of properties was simulated in steps of 5 ppm/K and 0.5 GPa for a total of 400 simulations for each location.

After the model was built and all the material properties were assigned, the model was meshed. The meshed model can be seen in Figure 12. The mesh for the model was created using the default meshing setting of COMSOL but the critical locations were assigned to have a finer mesh to improve the accuracy of the simulations. A finer mesh means higher accuracy, but the simulations take longer time and more memory is used. When the meshing was completed, the simulations were performed.

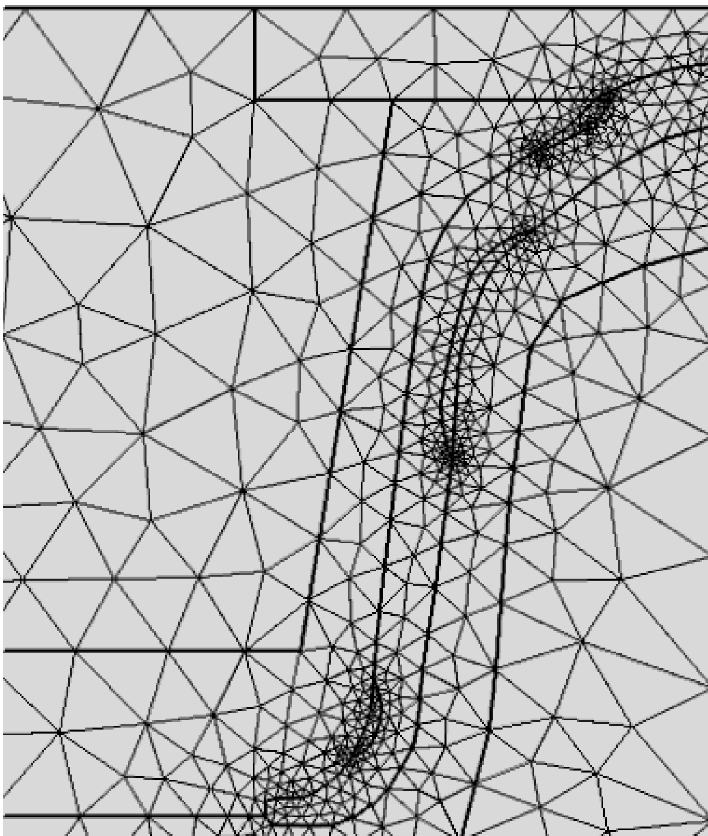

Figure 12: Part of the meshed model. The critical locations have a finer mesh compared to the rest of the model.

3.3 CROSS-SECTION ANALYSIS AND REQUALIFICATION TEST

To requalify the sensor package, the same test protocol as before was used (Figure 8) for the different DOEs, but with additional readouts during the temperature cycling tests. To get an early indication on if any DOE performed better than the other, TC 345 and TC 700 were performed on die level at OSAT A. After the temperature cycle tests, cross-sectioning was performed on the dies at OSAT A and the images from the cross-sections were obtained and analyzed.

The information extracted from the images was if the imaged TSV had a void, delamination at the outer sidewall, delamination at the inner sidewall or delamination near the interface of the bond pad. The extracted information was put into a matrix as binary data where each row represented a TSV and each column represented a material property or delamination/void data. If delamination was found, no matter the severity of the delamination, a value of 1 was put into the matrix and if a void was found no matter the size of the void, a value of 1 was put into the matrix. Binary logistic regression (Appendix 1) was used to determine if any of the material properties could statistically be related to the delamination.

The following tests were performed at OSAT A:

- Temperature cycling between -40 °C and 125 °C 345 cycles (TC 345) on die level with cross-sectioning over the bond pads after the test.
- Temperature cycling between -40 °C and 125 °C 700 cycles (TC 700) on die level with cross-sectioning over the bond pads after the test.

The following tests were performed at OSAT B:

- Standard qualification tests (chapter 2.6).
- Additional readout at 300 cycles during the temperature cycling.

4 RESULTS

4.1 SIMULATIONS

With COMSOL, the thermomechanical FEA simulations were performed where a temperature decrease from 125 °C to -40 °C was simulated. Because these simulations have many simplifications, only relative values will be presented. The results including stress profiles, DOE simulations and parametric sweeps of the critical locations are presented in this chapter.

4.1.1 Stress profiles

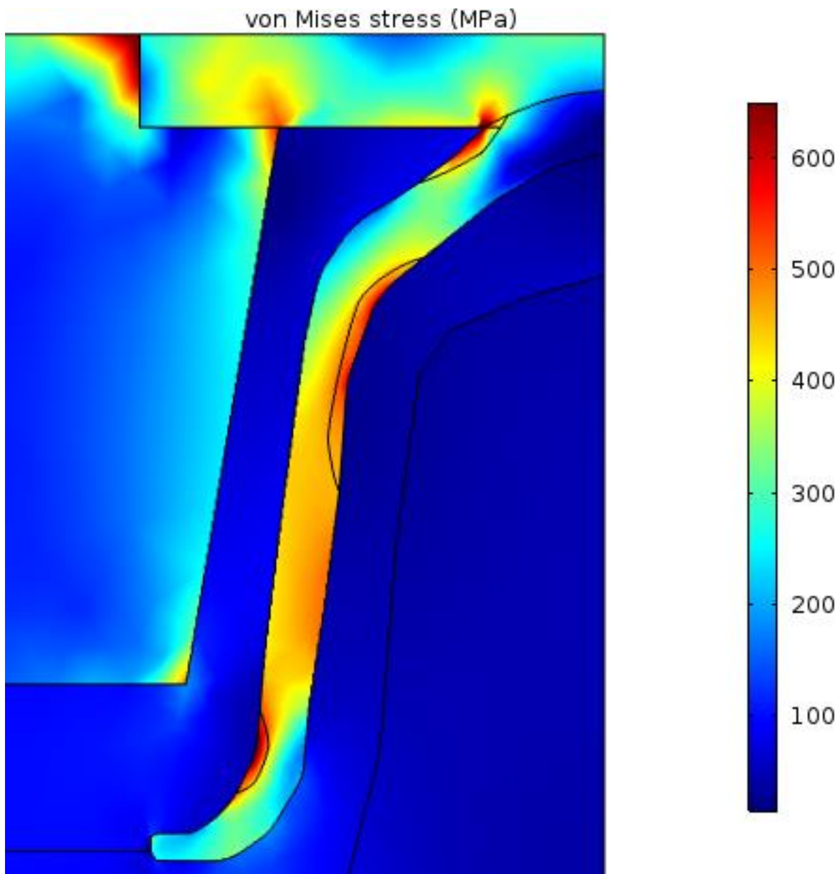

Figure 13: The stress profile for the POR structure where DOE 3-8 showed similar stress profile. The simulations showed three areas of high stress on the RDL and these locations were chosen for comparison in the DOE simulation and parametric sweep.

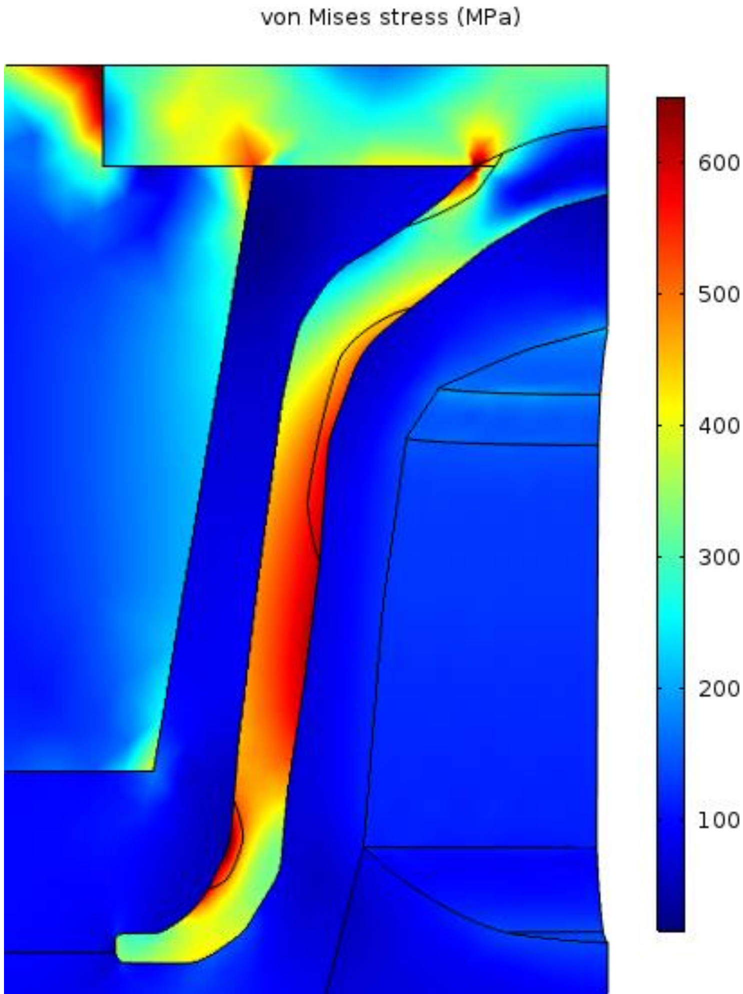

Figure 14: The stress profile of the voided TSV showing a different stress profile compared to Figure 13.

The stress profiles were received for the different structures (Figure 13 and Figure 14). Figure 13 shows the stress profile for the POR structure after a temperature decrease from 125 °C to -40 °C where three areas of high stress can be seen on the RDL. Similar stress profiles were received for the DOEs except when a voided structure was simulated (Figure 14). With a void added, another stress profile was received, where compared to the structures without a void, more stress is built up on the inner sidewall of the TSV.

4.1.2 DOE simulation and parametric sweep at critical location 1

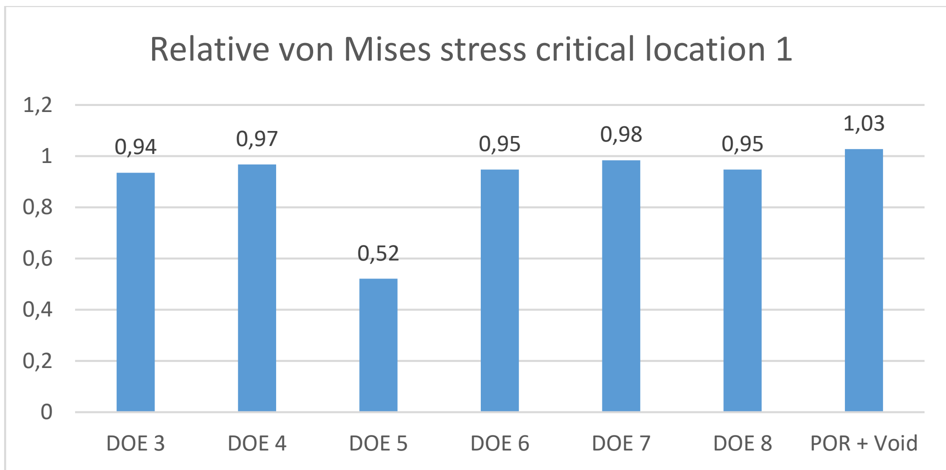

Figure 15: Simulated relative von Mises stress at critical location 1 where the POR structure is reference.

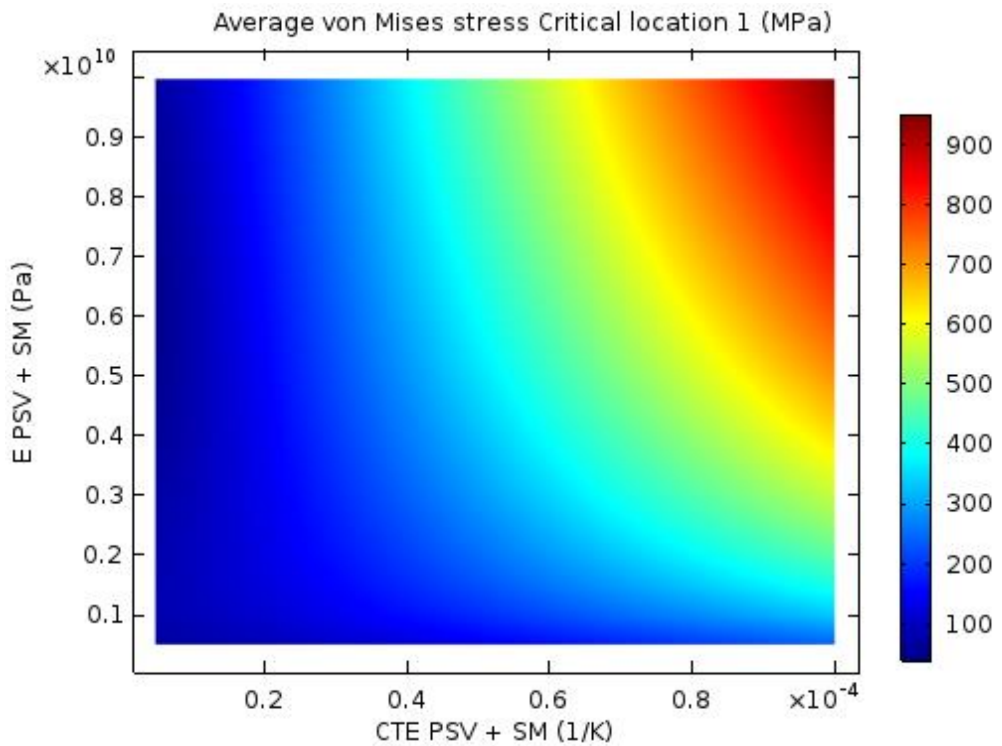

Figure 16: Parametric sweep of the passivation and solder mask for the average von Mises stress at critical location 1.

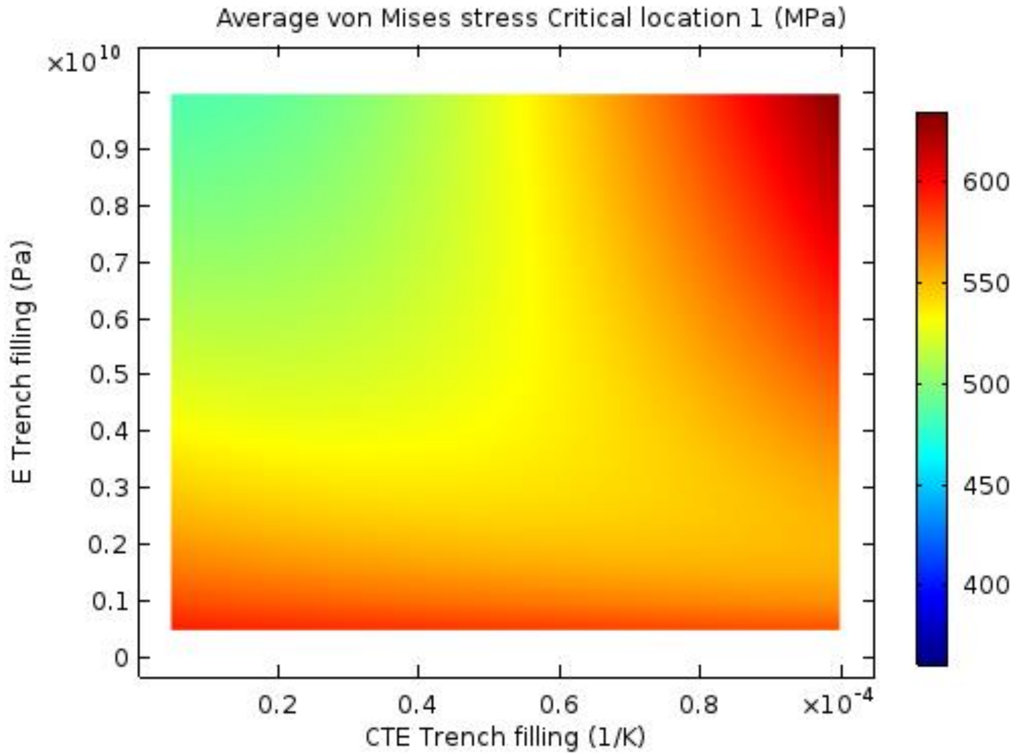

Figure 17: Parametric sweep of the trench fill for the average von Mises stress at critical location 1.

At critical location 1, DOE 5 induced the least stress compared to the other DOEs with 48% less stress compared to the POR structure (Figure 15). For the DOEs that were manufactured, both DOE 6 and 8 induced the least stress with 5% less stress compared to the POR structure. Only when a void was introduced the induced stress increased.

The parametric sweeps (Figure 16 and Figure 17) showed that the induced stress on critical location 1 has a strong dependency on the choice of passivation and solder mask material. Choosing a low CTE passivation and solder mask could reduce the induced stress dramatically. For the trench fill, a low CTE and high modulus choice of polymer would reduce the induced stress.

4.1.3 DOE simulation and parametric sweep at critical location 2

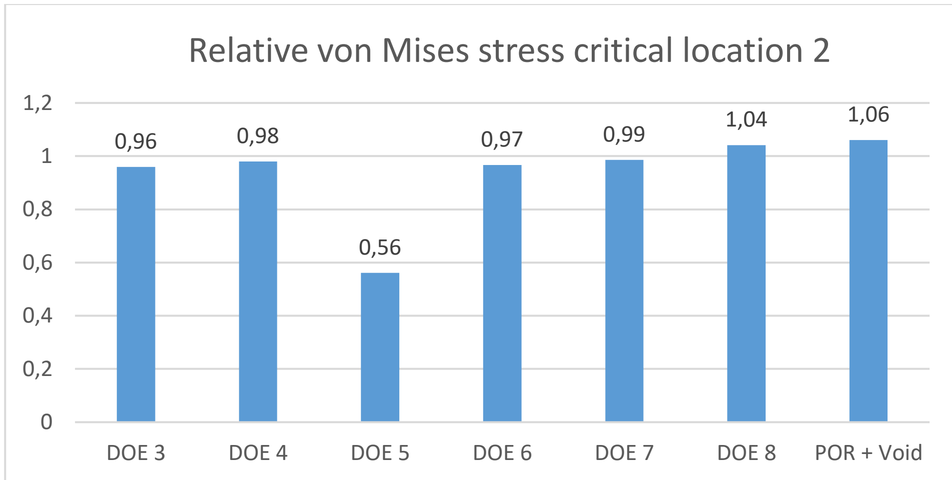

Figure 18: Simulated relative von Mises stress at critical location 2 where the POR structure is reference.

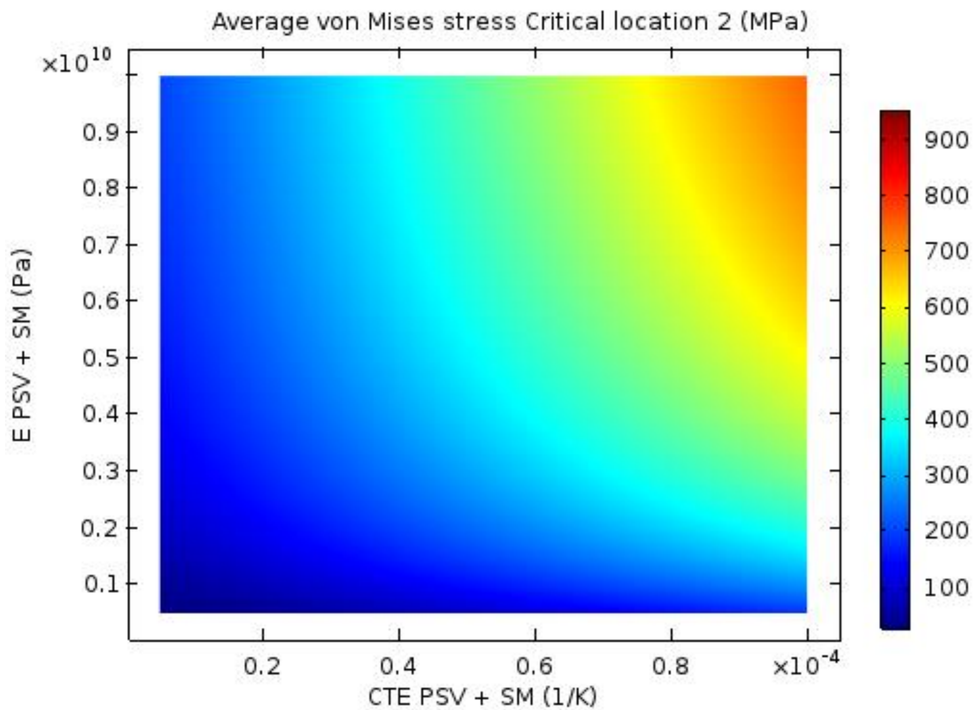

Figure 19: Parametric sweep of the passivation and solder mask for the average von Mises stress at critical location 2.

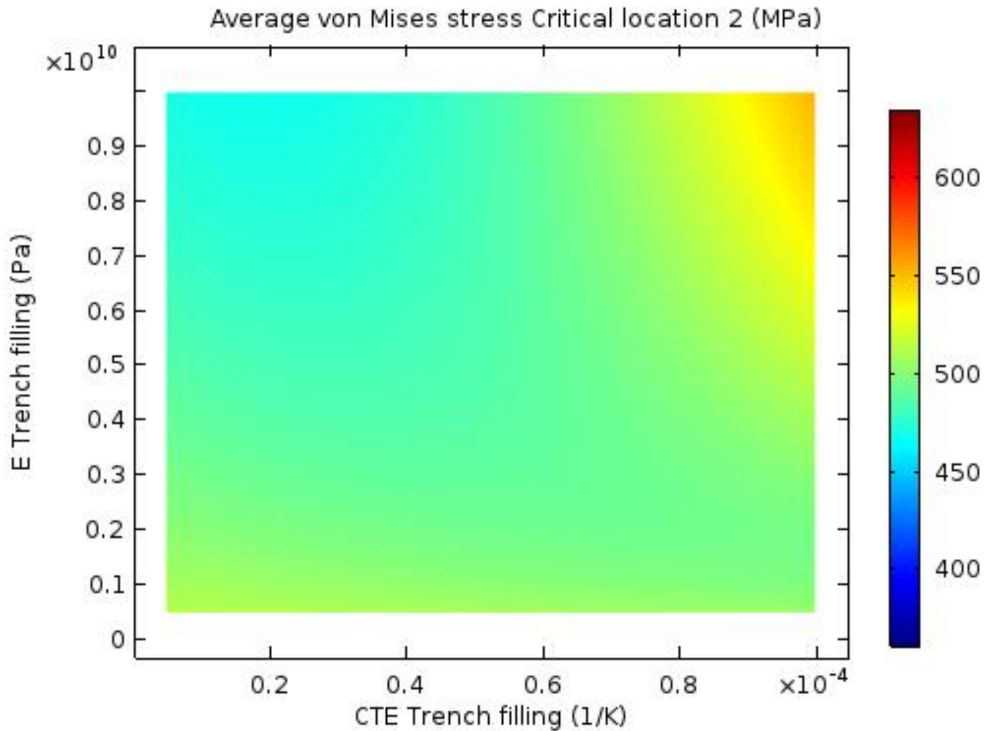

Figure 20: Parametric sweep of the trench fill for the average von Mises stress at critical location 2.

At critical location 2, DOE 5 once again induced the least stress compared to the other DOEs with 44% less stress compared to the POR structure (Figure 18). For the DOEs that were manufactured, both DOE 6 induced the least stress with 3% less stress compared to the POR structure. DOE 8 and the voided TSV induced the most stress with an increase of 4% and 6%.

The parametric sweeps (Figure 19 and Figure 20) showed that the induced stress on critical location 2 has a strong dependency on the choice of passivation and solder mask material, but not as strong compared to critical location 1. Choosing a low CTE passivation and solder mask could reduce the induced stress. For the trench fill, a change of properties would only make minor changes of the induced stress.

4.1.4 DOE simulation and parametric sweep at critical location 3

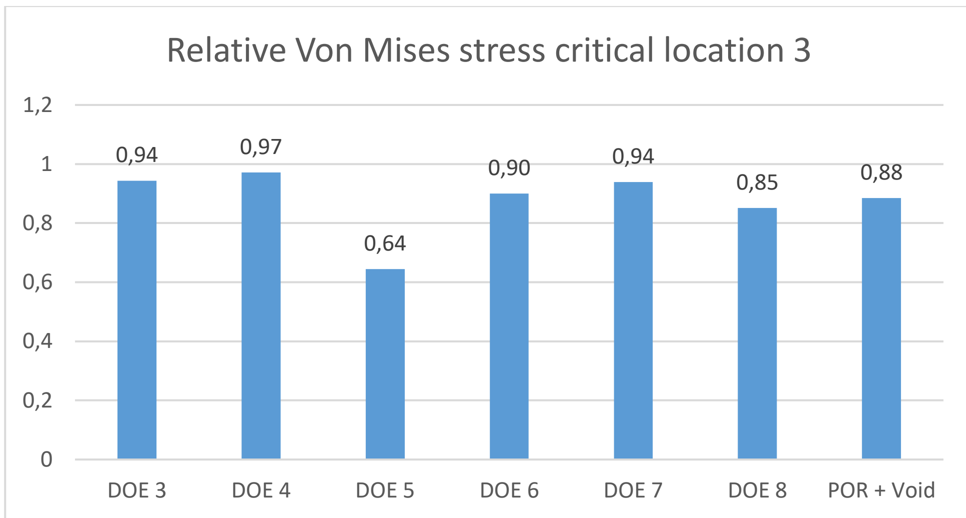

Figure 21: Simulated relative von Mises stress at critical location 3 where the POR structure is reference.

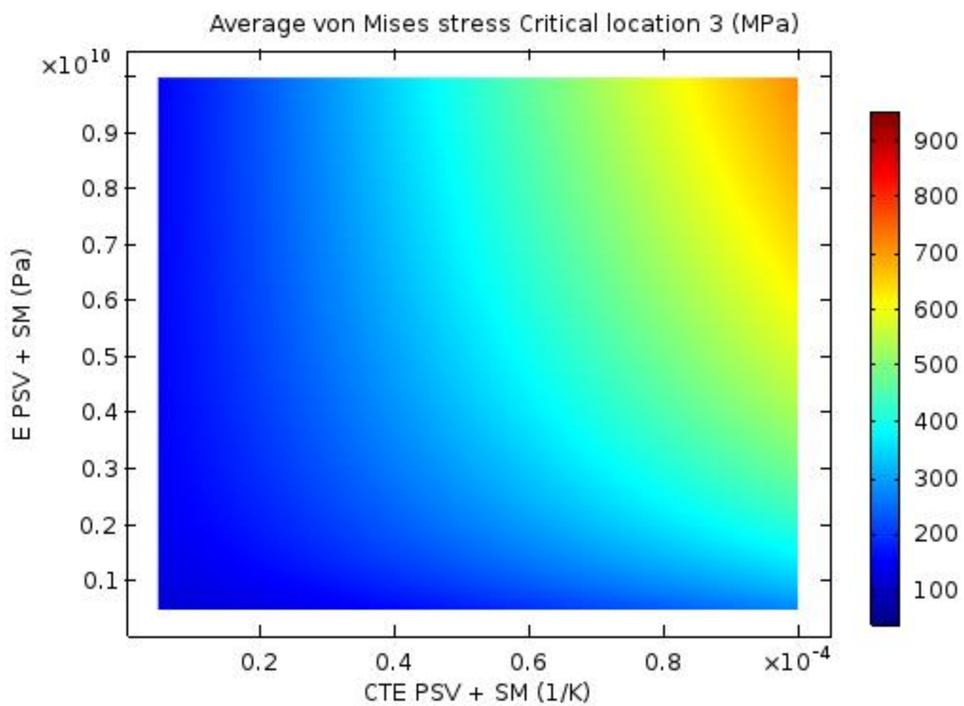

Figure 22: Parametric sweep of the passivation and solder mask for the average von Mises stress at critical location 3.

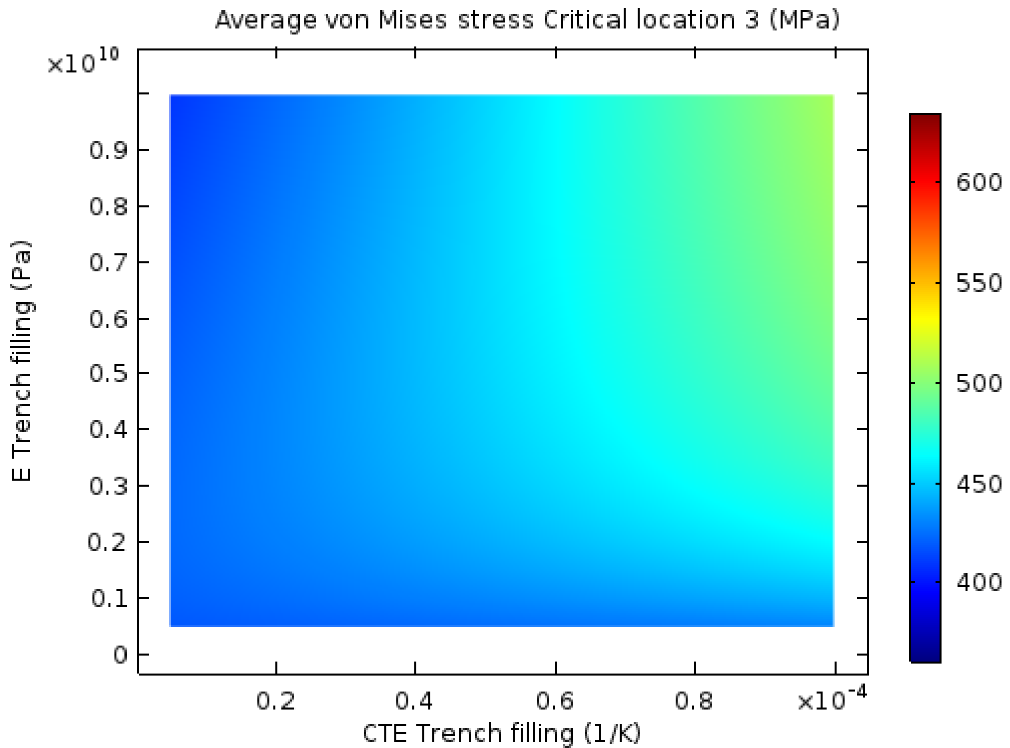

Figure 23: Parametric sweep of the trench fill for the average von Mises stress at critical location 3.

At critical location 3, DOE 5 once again induced the least stress compared to the other DOEs with 36% less stress compared to the POR structure (Figure 21). For the DOEs that were manufactured, all of them induced less stress compared to the POR structure with DOE 8 reducing the stress the most with a decrease of 15%. In contrast to critical location 1 and 2, a void would reduce the induced stress at critical location 3.

The parametric sweeps (Figure 22 and Figure 23) showed that the induced stress on critical location 3 has a strong dependency on the choice of passivation and solder mask material, but not as strong dependency as critical location 1 and 2. Once again, choosing a low CTE passivation and solder mask could reduce the induced stress. For the trench fill, a lower CTE would lower the induced stress at critical location 3.

4.2 CROSS-SECTION ANALYSIS

For the six DOEs that could be manufactured and the previously manufactured POR build (Table 1), the TSVs were processed as described in chapter 2.4 at OSAT A. TC 345 and TC 700 were performed at OSAT A where cross-sectioning was performed across the bond pad locations afterwards. Ten of each sensor die were cross-sectioned after TC345 and five of each sensor die were cross-sectioned after TC 700 where about half of the TSVs were imaged. In total 976 cross-section images were received and analyzed. The results from the cross-section analysis are presented in this chapter.

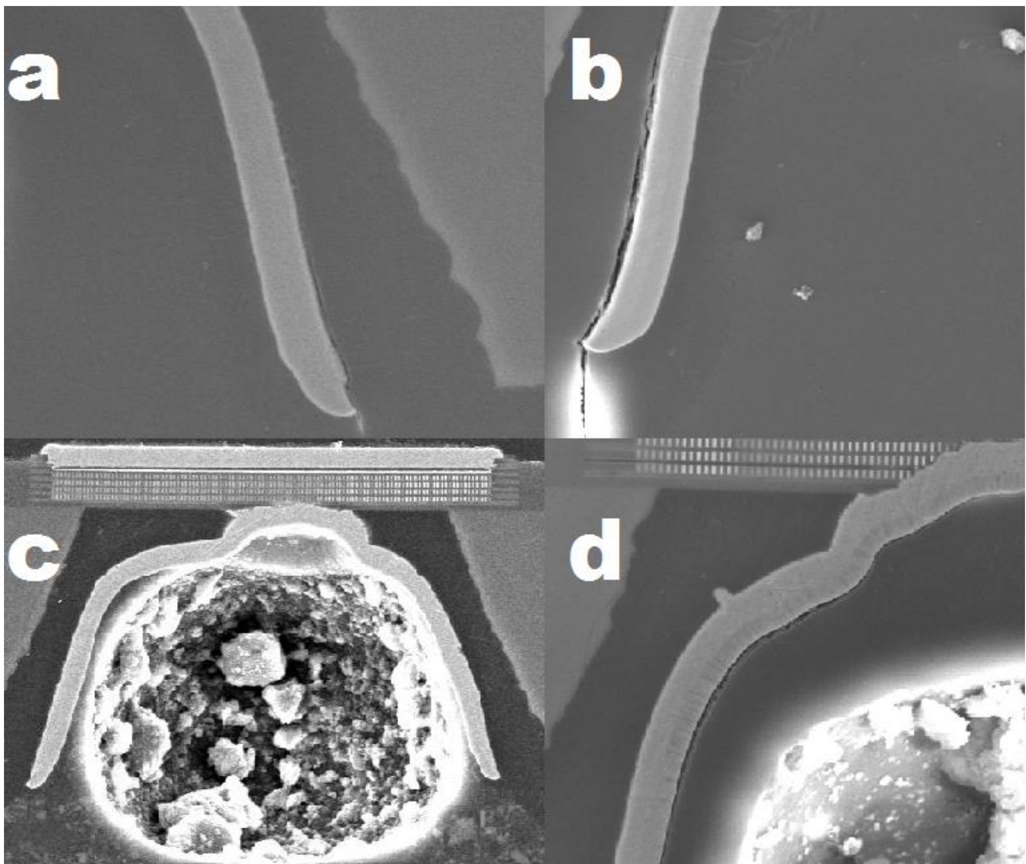

Figure 24: Four of the cross-section SEM images of the TSVs after temperature cycling. a) DOE 1 after 345 cycles showing minor delamination at critical location 1. b) DOE 1 after 700 cycles showing delamination along the outer sidewall of the RDL. c) DOE 6 after 345 cycles showing a large void. d) DOE 2 after 700 cycles showing delamination at critical location 2.

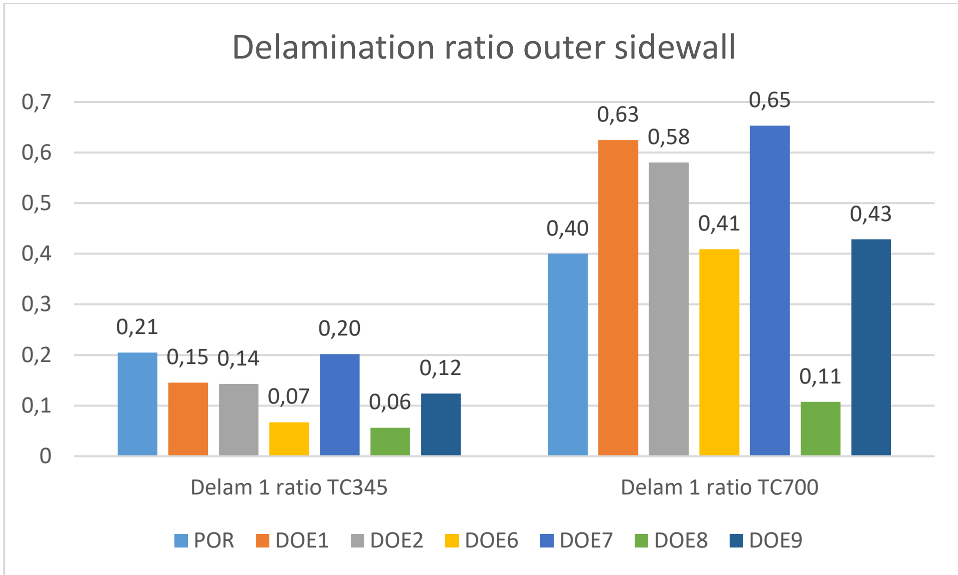

Figure 25: Delamination ratio at the outer sidewall.

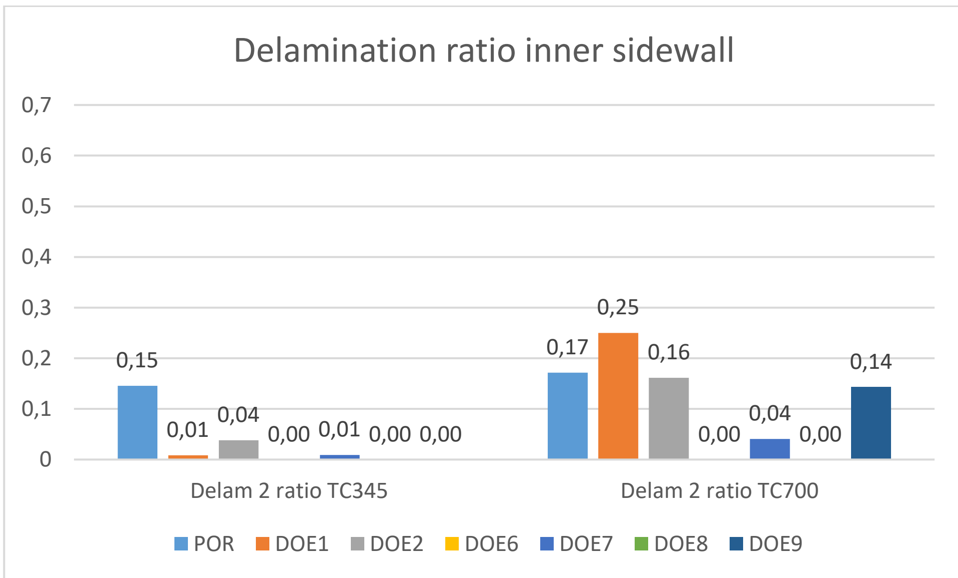

Figure 26: Delamination ratio at the inner sidewall.

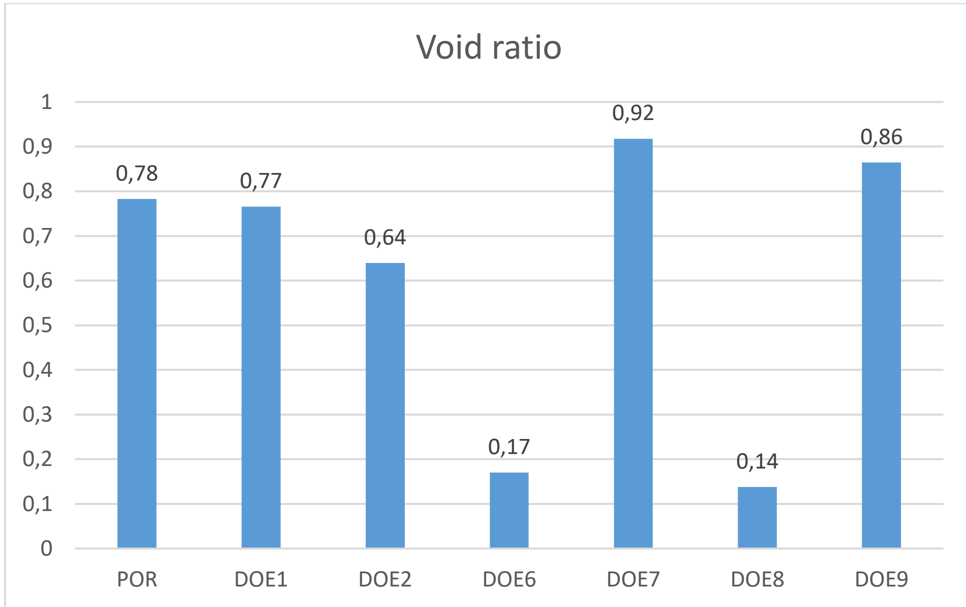

Figure 27: Void ratio of the cross-sectioned samples.

From the cross-section images, delamination was found for all DOEs, but the ratio of delamination was different between the DOEs (Figure 25 and Figure 26). Delamination was only found at the outer and inner sidewall of the RDL, no delamination was found near the interface of the bond pad. The delamination ratio was higher at the outer sidewall compared to the inner sidewall. Both the ratio and the severity of the delamination also increased after more cycles, Figure 24 a shows a typical delamination after 345 cycles while Figure 24 b shows a typical delamination after 700 cycles. Both DOE 6 and DOE 8 showed no delamination at all at the inner sidewall. Voids were also present in all the DOEs and for DOE 7, the void ratio was the highest where 92% of the TSVs included a void and DOE 8 had the lowest void ratio of 14%. The voids in DOE 6 and 8 were also larger compared to the voids in the other DOEs (Figure 24 c).

All the received 976 images were analyzed and information about the delamination and void along with the material properties for each TSV were put into a matrix. With the statistical software OriginPro, logistic regression was performed and the results are presented in Table 3Table 4.

Table 3: Results of binary logistic regression on delamination at the outer sidewall.

	Coefficients	Standard Error	z-Value	Prob>|z|	Conclusion at Level 5%
Intercept	-2.523	0.594	-4.2489	2.15E-05	Significant
CTE SM	0.021	0.008	2.5137	0.0120	Significant
E SM	0.301	0.164	1.8343	0.0666	Not significant
CTE Trench fill	-7.07E-04	0.011	-0.0625	0.9502	Not significant
E Trench fill	-0.549	0.089	-6.1397	8.27E-10	Significant
Ti thickness	0.384	1.592	0.2413	0.8093	Not significant
Cycles	1.632	0.184	8.8899	6.12E-19	Significant
Cure time	0.104	0.260	0.4022	0.6876	Not significant
Void	-0.396	0.218	-1.8157	0.0694	Not significant

Table 4: Results of binary logistic regression on delamination at the inner sidewall.

	Coefficients	Standard Error	z-Value	Prob>|z|	Conclusion at Level 5%
Intercept	-30.11	4734.2	-0.0064	0.995	Not significant
CTE SM	0.197	37.474	0.00526	0.996	Not significant
E SM	3.303	1308.2	0.00252	0.998	Not significant
CTE Trench fill	0.327	20.086	0.01629	0.987	Not significant
E Trench fill	-6.855	564.21	-0.0122	0.990	Not significant
Ti thickness	-0.187	2.352	-0.0794	0.937	Not significant
Cycles	1.63	0.343	4.769	1.85E-06	Significant
Cure time	-0.605	0.447	-1.351	0.177	Not significant
Void	1.071	0.481	2.229	0.026	Significant

Table 3 shows the results from the logistic regression performed on the delamination at the outer sidewall. If Prob>|z| is below 0.05, the parameter has according to the logistic regression model a significant effect on the delamination at 95% confidence interval. The coefficients are the coefficients used for $\pi(x)$ in where a positive coefficient means that an increase of the parameter will increase the probability for delamination and vice versa. Table 3 shows that a higher CTE solder mask, lower modulus trench fill and more cycles increased the probability for delamination at the outer sidewall.

Table 4 shows the results from the logistic regression performed on the delamination at the inner sidewall. The logistic regression showed that if more cycles were performed and if a void was present in the TSV, the probability for delamination at the inner sidewall increased. The logistic regression could not find any other parameter that had a significant effect on the delamination.

4.3 REQUALIFICATION TESTS

TSV-processed sensor dies from OSAT A were shipped to OSAT B where they were assembled into LGA packages as describe in chapter 2.5. Qualification tests were performed on the DOE and POR builds as described in chapter 3.3.

For the temperature cycling test, all DOEs passed the open/short test after 700 cycles and no open or short signals could be detected at the interim readouts at 300 or 500 cycles. For the POR build that previously failed qualification, failed once again the temperature cycling test with three units having an open signal after 300 cycles, five units having an open signal after 500 cycles and six units having an open signal after 700 cycles.

For the DOEs, no open or short signal could be detected after uHAST264, HTSL1000 or during the interim readouts. Since the POR build did not pass the temperature cycling test it did not go through uHAST or HTSL. One of the DOEs was selected and is now both qualified and in mass production.

5 DISCUSSION

Comparing the simulations with the results from the cross-section images, there are some similarities and differences. The cross-section images from TC 345 showed that the delamination at the outer sidewall of the TSV mostly appears to originate from critical location 1 which is shown in Figure 24 a. After more cycles, the delamination appears to propagate on the outer sidewall for a more severe delamination which is shown in Figure 24 b. If the delamination propagates even further than what is shown in Figure 24 b, the delamination can reach the bond pad which can cause the RDL to detach from the bond pad. However, after 700 cycles, the delamination had never propagated all the way to the bond pad for any of the analyzed TSVs.

The cross-section images also showed that the delamination at the inner sidewall of the TSV originates from critical location 2 which is shown in Figure 24 d. The simulations predicted delamination near the interface of the bond pad, but no delamination was found there, not even from the POR build which had from previous temperature cycling tests shown delamination at that location. Note that the images received from the first qualification were on package level in which they cannot fully be compared with the requalification images which were on die level.

The simulations showed that the choice of passivation polymer has the biggest impact on the induced stress (Figure 16, Figure 19 and Figure 22) in where DOE 5 with a lower CTE passivation always performed best in the simulations (Figure 15, Figure 18 and Figure 21). The passivation layer consists of a polymer sandwiched between the silicon die and the metal RDL, two structures with low CTE and high modulus. The passivation used (WLP32) will shrink and expand at a much higher rate compared to the silicon die and the RDL during temperature cycling. Because of the CTE mismatch and the limited space where the passivation can shrink and expand, this could explain why the choice of passivation polymer has the biggest influence on the induced stresses. As previously mentioned, the TSV process at OSAT A was only compatible with WLP32 as passivation polymer in which no other choice of passivation could be studied.

Both simulations and the cross-section analysis showed that the choice of trench fill and solder mask influenced the delamination rate. The simulations showed that the choice of trench fill mostly influenced the induced stress of the outer sidewall and near the bond pad (Figure 17 and Figure 23) while it did not have much effect on the inner sidewall (Figure 20). The simulations showed that a low CTE and high modulus trench fill would reduce the induced stresses on the RDL. A low CTE trench fill would reduce the CTE mismatch with the RDL and a high modulus trench fill would increase the mechanical stability of the whole TSV structure. Applying the logistic regression model on the cross-section images, a correlation between low modulus trench fill and a high ratio of delamination on the outer sidewall was found (Table 3) which matches the results of the simulations. The logistic regression model could not find a correlation between the CTE of the trench fill and the delamination ratio.

The higher cure time of DOE 1 and the thicker titanium layer of DOE 2 did not decrease the delamination ratio compared to the POR build. The cross-section analysis showed a slightly higher rate of delamination after 700 cycles for DOE 1 (Figure 25 and Figure 26), but the logistic regression model could not find a correlation between either the titanium thickness or the cure time on the delamination ratio (Table 3 and Table 4). These results show that an insufficient cure time of the passivation or an insufficient thickness of the titanium layer were not the reasons why the POR build failed the first qualifications.

Voids were present for all DOEs, but for DOE 6 and 8, the rate was found to be lower compared to the other DOEs (Figure 27). Simulations showed that a voided TSV overall induced more stress during temperature cycling compared to a TSV with no void, particularly at the inner sidewall (Figure 14 and Figure 13). Statistical data (Table 4) also showed that a voided TSV increased the rate of delamination at the inner sidewall. What differs DOE 6 and DOE 8 from the other DOEs is that the TSV is filled with a single polymer in one step. For the other DOEs, a solder mask is first deposited, then the TSV is filled with trench fill. To reduce the ratio of voids which also reduces the rate of delamination at the inner sidewalls, the TSVs should be filled in one step with a single polymer. However, no correlation on the reliability of the TSV and the delamination at the inner sidewall could be found.

Statistical data showed no correlation between voids and delamination at the outer sidewall (Table 3) while simulations showed an increase of induced stress at critical location 1 (Figure 15) which would result in a higher rate of delamination. Simulations also showed that a voided TSV induced less stress at critical location 3 compared to a TSV with no void (Figure 21). A void inside the TSV would remove the forces that the trench fill would act on the bond pad as the trench fill shrinks and expands during the temperature cycling. Since critical location 3 is located at the interface of the bond pad, it is the most critical stress to control due to if a crack would occur between the RDL and bond pad, it would lead to an open signal. It could not be statistically proven if a void would decrease the stress induced on the bond pad since no delamination was found near the bond pad after temperature cycling on die level.

Simulations and cross-sectional analysis showed that the choice of solder mask had the biggest impact on the DOEs that could be manufactured where DOE 6 and DOE 8 with another solder mask usually induced the least stress (Figure 15, Figure 18 and Figure 21). The cross-section analysis showed that DOE 8 had the least delamination compared to all the other DOEs. No delamination was found at the inner sidewall for both DOE 6 and DOE 8. The logistic regression model showed that a lower CTE solder mask reduces the delamination rate at the outer side wall (Table 3). For the inner side wall, no correlation between the solder mask CTE and the delamination rate could be found (Table 4). The reason why the logistic regression model did not find a connection between the solder mask and delamination rate at the inner side wall could be because of the low void rate in DOE 6 and DOE 8. It could also be because of the overall low delamination rate at the inner side wall in where the logistic regression model had an insufficient amount of data to analyze.

The new temperature cycling tests performed on the POR packages yielded open signals in the open/short test in where the failure mode most probably was the same as from the first qualifications. No cross-section studies were performed at OSAT B after the requalifying tests to confirm the failure mode due to a low time budget. Because the POR build both failed the first qualification and the requalification, something must have malfunctioned during the TSV process of the POR build. Since DOE 1 and 2 which included two different minor changes of process passed the full TC 700 but the POR

build did not even pass TC 300, this further supports that something must have malfunctioned during the TSV process for the POR build.

In between most of the TSV process steps, there are cleaning processes to remove residues from the previous process step. For some lots of the POR build, the cleaning processes could have malfunctioned during the RDL formation in which the residues from the previous process step would weaken the adhesive strength between the RDL and the passivation or solder mask. This could explain the high delamination rate at the inner sidewall after TC 345 (Figure 26) for the POR build where two of the ten tested sensors accounted for the majority of the delamination count.

Since the newly manufactured sensor package was qualified, this will enable the sensor to be placed under glass in a smartphone. It has been shown that there is a correlation between a technology's perceived ease of usage and the acceptance of that technology [23]. Enabling the sensor to be placed under the glass of a smartphone would make the sensor easier to use which could increase the acceptance of fingerprint recognition technology. Compared to a PIN-code, fingerprint data is more personal since it consists of information about someone's physical self. Unlike a PIN-code or a password, a fingerprint cannot be changed if it has been inappropriately released. As fingerprint recognition technology and biometric technology in general get more integrated into consumer electronics and accepted by its users, the biometric companies have further responsibilities to ensure that the users biometric data will not be inappropriately released or taken advantage of.

For future studies, the effect the void inside a TSV has on the reliability could be further investigated. By doing temperature cycling with more than 700 cycles, the effect the void has on the delamination would be increased. Also, TSVs with passivation polymers with lower CTE could be manufactured and tested to see if the passivation will have as much of an impact on the induced stresses and delamination ratio as the simulations showed.

6 CONCLUSIONS

In this thesis, different manufacturing processes for TSV structures in a fingerprint package were investigated. Every DOE that was manufactured passed the qualification test according to JEDEC standard. For the POR build, in which no new TSV dies were manufactured, it failed the requalification test after package assembly. The reason of the POR build failing both the qualification and the requalification has not been determined, but it could be due to insufficient cleaning during the TSV process.

A linear thermomechanical model showed decent agreement with cross-section images after temperature cycling. The model predicted three locations of high stress on the RDL which would translate to three locations of delamination. Two of the three locations showed delamination in the cross-section images.

Delamination was found for all the DOEs after temperature cycling, but the ratio was different between the DOEs. Simulations and cross-section analysis showed that using low CTE polymers in the TSV structure would decrease the induced stress and the delamination ratio. Simulations and cross-section analysis also showed that a high modulus trench fill would decrease the induced stress and the delamination ratio.

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APPENDIX 1 – LOGISTIC REGRESSION

If a model has a binary response value (example yes/no, success/failure positive/negative), the relationship between the dependent variable and the independent variables are usually nonlinear. If $\pi(x)$ denotes the probability of the outcome for the response value, its maximum value must be 1 and minimum value must be 0. If $\pi(x)$ is modeled from linear regression, $\pi(x)$ will not have the maximum value of 1 and minimum value of 0. Instead, using logistic regression where $\pi(x)$ has the function

$$\pi(x) = \frac{e^t}{1 + e^t} \quad (4)$$

where t is a linear function of explanatory variables x_i, $\pi(x)$ will have an S-shaped curve and a maximum of 1 and minimum of 0 (Figure 28).

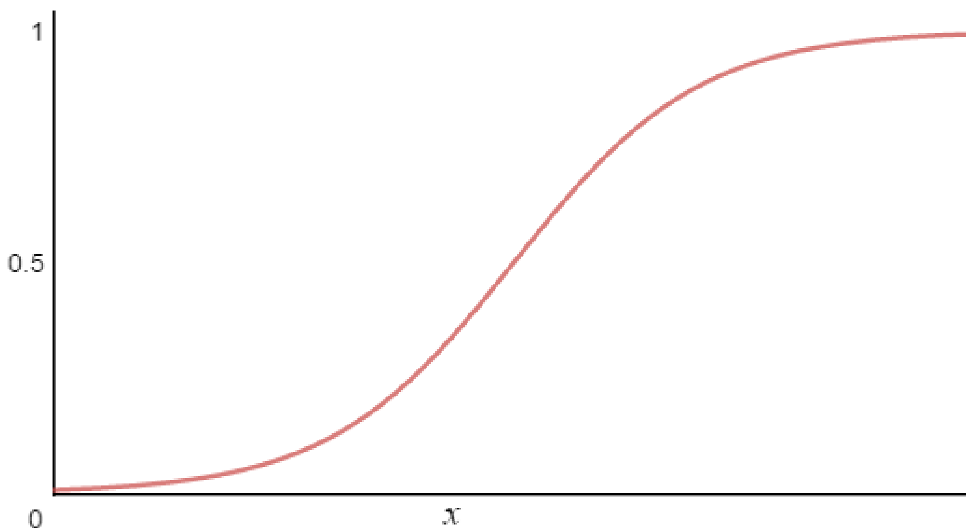

Figure 28: Example of a logistic regression function.

As can be seen in Figure 28, when the function $\pi(x)$ is approaching 0 or 1, a change of the variables x will not change $\pi(x)$ as much as when x is changing when $\pi(x)$ is 0.5.

To test if an independent variable has significant effect on the dependent variable, a Wald-test can be performed [24].