Digitally Controlled Oscillator for mm-Wave Frequencies

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Digitally Controlled Oscillator for mm-Wave Frequencies

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Abstract

In the fifth generation of mobile communication, 5G, frequencies above 30 GHz, so-called millimeter-wave (mm-wave) frequencies are expected to play a prominent role. For the synthesis of these frequencies, the all-digital phase locked loop (ADPLL) has recently gained much attention. A core component of the ADPLL is the digitally controlled oscillator (DCO), an oscillator that tunes the frequency discretely. For good performance, the frequency steps must be made very small, while the total tuning range must be large.

This thesis covers several coarse- and fine-tuning techniques for DCOs operating at mm-wave frequencies. Three previously not published fine-tuning schemes are presented: The first one tunes the second harmonic, which will, due to the Groszkowski effect, tune the fundamental tone. The second one is a current-modulation scheme, which utilizes the weak current-dependence of the capacitance of a transistor to tune the frequency. In the third one, a digital-to-analog converter (DAC) is connected to the bulk of the differential pair and tunes the frequency by setting the bulk voltage. The advantages and disadvantages of the presented tuning schemes are discussed and compared with previously reported fine-tuning schemes.

Two oscillators were implemented at 86 GHz. Both oscillator use the same oscillator core and hence have the same power consumption and tuning range, 14.1 mW and 13.9%. A phase noise of -89.7 dBc/Hz and -111.4 dBc/Hz at 1 MHz and 10 MHz offset, respectively, were achieved, corresponding to a Figure-of-Merit of -178.5 dBc/Hz. The first oscillator is fine-tuned using a combination of a transformer-based fine-tuning and the current modulation scheme presented here. The achieved frequency resolution is 55 kHz, but can easily be made finer. The second oscillator utilizes the bulk bias technique to achieve its fine tuning. The fine-tuning resolution is here dependent on the resolution of the DAC; a 100 µV resolution corresponds to a resolution of 50 kHz.

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Abbrevations

ADPLL	All-Digital Phase-Locked Loop
CB	Coarse Bank
CCW	Coarse Control Word
DAC	Digital-to-Analog Converter
DCO	Digitally Controlled Oscillator
FCW	Frequency Control Word
FD-SOI	Fully-depleted, Silicon-on-Insulator
FF	Fast-fast process corner
LF	Loop filter
LSB	Least Significant Bit
MB	Mini Bank
PLL	Phase-Locked Loop
PD	Phase Detector
SS	Slow-slow process corner
TDC	Time-to-Digital Converter
TB	Transformer Bank
TCW	Transformer Control Word
TT	Typical-typical process corner
VCO	Voltage-Controlled Oscillator

Chapter 1

Introduction

In recent years, global mobile data traffic usage has increased by unprecedented numbers. From 2011 to 2016, the global monthly mobile data usage grew from 0.5 exabytes to 7 exabytes, and the growth rate is increasing for every year [1]. This expansion shows no signs of slowing down and is putting higher and higher demands on bandwidth. However, since cellular communication today is limited to below 2.7 GHz, frequency congestion that severely limits data speeds is expected to occur by 2020 in densely populated areas [2]. This has caused telecommunication companies such as Ericsson to design radio circuits for the fifth generation of mobile communication, 5G, operating at the mostly unused millimeter-wave spectrum, i.e. frequencies from 30 GHz to 300 GHz [3][4]. Not only will this take care of the problem of congestion, but it will also allow for bandwidths much larger than what is used in 4G today, thus drastically increasing data rates [2].

A key aspect in all modern radio transceivers is the ability to synthesize the frequency of the communication channel of interest[1]. Adjacent communication channels can be spaced by only tens of kilohertz, while operating at several gigahertz [5]. Therefore, the frequency synthesis must be extremely precise, otherwise different transceivers will interfere with each other. To achieve such a precision, a *phase-locked loop* (PLL) is almost exclusively used. The PLL takes a low, stable input frequency, usually from a crystal oscillator, and multiplies it to the desired frequency. A core component of the PLL is the voltage-controlled oscillator (VCO), which sets the output frequency of the PLL. The output frequency can be continuously tuned by applying a control voltage to the VCO.

However, the PLL has some problems, which have been aggravated by today's deep-submicron silicon processes. Therefore, much attention has recently been paid towards an alternative to the regular PLL, called the all-digital phase-locked loop (ADPLL). The ADPLL can take better advantage of the improved silicon technology, while still providing the high precision of a regular PLL. Instead of a VCO, a digitally controlled oscillator (DCO) is used in the ADPLL. The DCO takes a digital word as its input, instead of a control voltage, and tunes its frequency discretely.

---

[1] Or a frequency at a fixed distance to the channel, if heterodyning is used.

1.1 This thesis

This thesis was conducted at the RFIC unit at Ericsson AB in Lund, Sweden. The purpose was to investigate how mm-wave DCOs with fine frequency resolution and wide tuning range can be implemented, and implement a DCO operating at 86 GHz, with a tuning range of 20 % and a frequency resolution of at least 1 MHz.

All simulations were done using *Cadence Virtuoso*, except for the inductor simulations, which were done using *Keysight Momentum*. The design kit used was a 22 nm, fully-depleted Silicon-on-Insulator (FD-SOI) CMOS from GlobalFoundries and the supply voltage used was 800 mV.

1.2 Report organization

The thesis is organized as follows:

- **Chapter 2:** A brief introduction of PLLs and ADPLLs is given.
- **Chapter 3:** Covers the basics of an LC oscillator, including a description of phase noise.
- **Chapter 4:** The implementation of inductors at mm-wave frequencies is discussed.
- **Chapter 5:** Covers the fundamentals of a digitally controlled oscillators. Several frequency tuning schemes used at mm-wave frequencies are presented.
- **Chapter 6:** In this chapter, two DCOs operating at 86 GHz are proposed.
- **Chapter 7:** The two proposed oscillators are discussed and a conclusion of the thesis is made.

Chapter 2

Phase-Locked Loops

2.1 Analog PLL

A basic PLL for frequency synthesis is shown Fig. 2.1. The PLL strives to remove the phase difference between f_{ref} and f_{s}, or the phase error, by utilizing negative feedback. It consists of a phase-detector (PD), a loop filter (LF), a voltage-controlled oscillator (VCO), and a frequency divider (shown a ÷N in Fig. 2.1). An input frequency, f_{ref}, is supplied by a very clean, fixed frequency oscillator, usually from an oscillator with an off-chip crystal. The phases of f_{ref} and f_{s}, the output from the frequency divider, are compared in the phase detector, which outputs a voltage proportional to the phase difference. The voltage is stabilized and filtered by the loop filter and then fed to the VCO, which outputs a frequency determined by this voltage. This output frequency will also be the output frequency f_{out} of the PLL. f_{out} is divided by a factor N, which is an integer in the basic PLL, in the frequency divider and is then fed to the PD and the loop is closed.

When the phase error is removed or at least fixed at a constant value, the loop is said to be locked, otherwise it is in acquisition. When locked, the derivate of the two phases must be equal and since frequency is the derivative of phase, f_{s} must be equal to f_{ref} in the locked state. Since $f_{\mathrm{s}} = f_{\mathrm{out}}/N$, the output frequency will be [6]:

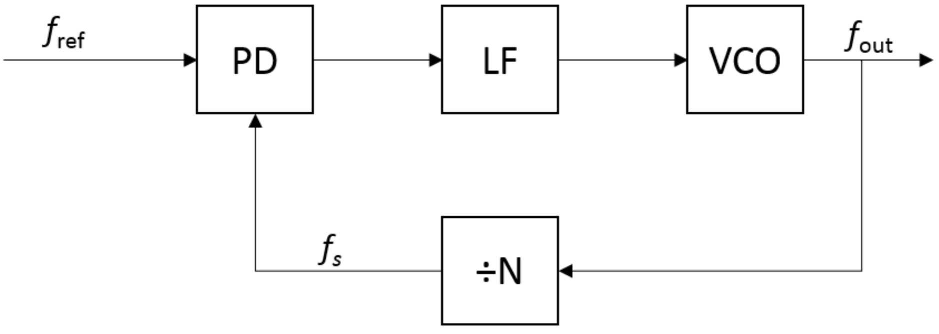


Figure 2.1: A basic phase-locked loop.

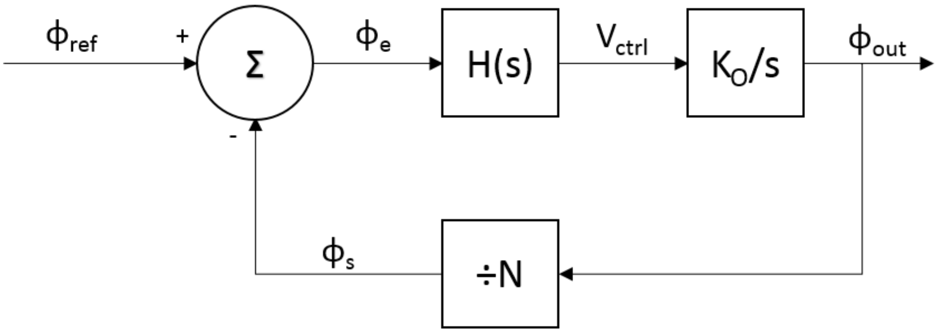


Figure 2.2: Linearization of the basic PLL.

$$f_{\text{out}} = N f_{\text{ref}} \tag{2.1}$$

We can thus set the output frequency to an arbitrary frequency with a resolution of f_{ref} by changing N (it must of course be a frequency supported by the PLL, e.g. a frequency the VCO can oscillate at). Thanks to the feedback, the loop will compensate any frequency drift of the oscillator, so that the output always stays the same. If a higher resolution is required, a so-called *Fractional-N* architecture can be used, where N can be a fractional number [6].

Fig. 2.2 shows a linearized model of a PLL in the Laplace domain. ϕ_{ref}, ϕ_{out}, ϕ_{s}, and ϕ_{e} are the reference phase, the output phase, the divider output phase and the phase error, respectively. $H(s)$ is the transfer function of the loop filter and K_O is the gain of the VCO, given in (rad/s)/V, i.e. how much the oscillation frequency changes per volt. Since phase is the integral of frequency, K_O is divided by s.

In its simplest form, the loop filter is only a scalar gain, i.e. $H(s) = K$. The PLL is then called a first-order PLL, since only one pole is present in the open loop (found in the VCO). This kind of PLL will have large phase margins and is easy to implement, but it can easily be shown that it will cause a non-zero steady-state phase error. Moreover, the control voltage will be noisy and unstable. Therefore, one or more poles are usually added in the loop filter, which results in zero steady-state phase error. In order to achieve loop stability, one or more zeros also have to be added. Fig. 2.3 shows two typical, second-order loop filters; one implemented with an op-amp and one with passive components in conjunction with a charge-pump. Higher order loops will provide better filtering of unwanted ripple on the control voltage, but will also be more complex, making it harder to achieve loop stability [7].

The bandwidth of the loop filter is also important. A higher bandwidth will make the loop lock faster. However, higher bandwidth means worse filtering on the control line, leading to more voltage ripple. In addition to this, a high bandwidth can lead to instability due to the sampling nature of the phase detector. Therefore, the bandwidth is commonly set to less than 10% of the reference frequency. [6]

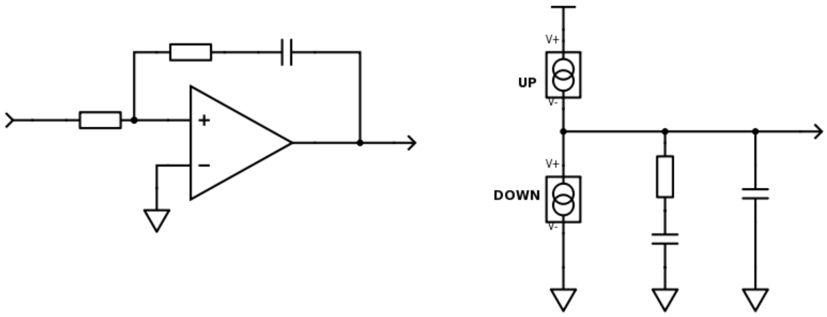


Figure 2.3: Two common loop filters, one implemented with an op-amp and one without.

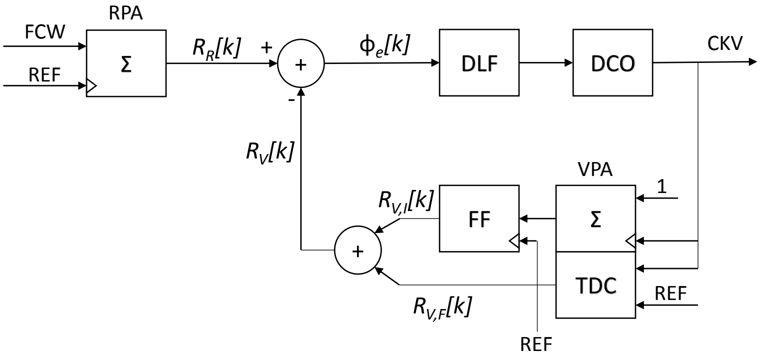


Figure 2.4: A basic all-digital PLL.

2.2 All-Digital Phase-Locked Loops

The traditional PLL described above has been the go-to choice for frequency synthesis in RF applications since the 70's [7]. However, in today's deep-submicron CMOS processes, the PLL is facing problems. One issue is that the supply voltage is decreasing with decreasing transistor sizes, thus reducing the signal-to-noise ratio. This makes it harder to achieve a precise oscillation frequency [8]. Another issue is that analog PLLs require large passive components in the loop filter, which either take up a large silicon area or have to be implemented off-chip [9][10]. Analog filters will also have some current leakage, which will cause spurs in the output spectrum [11]. Furthermore, more and more digital circuitry are implemented in today's RF chips, causing severe switching noise, which degrades the performance of an analog PLL [8].

Recently, much attention has been directed towards so-called All-Digital Phase-Locked Loop (ADPLL), which was first demonstrated for multi-gigahertz applications in 2004 by Staszewski et al [12]. A slightly simplified version of the ADPLL used in that paper is shown in Fig. 2.4. In principle, it is very similar to its analog counterpart. The phase difference is measured between the reference clock and the output frequency, and the frequency of the controllable oscillator is shifted to eliminate this difference. However, there are two major differences between the two. Firstly, except for its input and output, the ADPLL only uses digital words between its building blocks. Since digital words are virtually unaffected by noise, the ADPLL becomes very noise-resilient [9]. Secondly, the ADPLL operates in the time-domain to detect phase differences. This means that the ADPLL becomes almost independent of supply voltage and can take full advantage of the improvements in CMOS technology [12].

The ADPLL described in [12] operates in a digitally synchronous fixed-point phase domain. That is, phase measurements and phase comparisons are done synchronously at regular points k, which occurs every reference period, 1/REF. The target output frequency is set by the Frequency Control Word (FCW) (the equivalent to N in the analog PLL), which can be a fractional number. The FCW is fed to the Reference Phase Accumulator (RPA), along with the reference clock (REF). The RPA detects rising edges on REF and will add a reference phase signal to the vector $R_R[k]$, where each point in the vector is given by $k \cdot \text{FCW}$. $R_R[k]$ is subtracted by $R_V[k]$, the variable phase signal vector, to produce a phase error vector $\phi_e[k]$. $R_V[k]$ can be divided into two parts, one fractional part, $R_{V,f}[k]$, and one integer part, $R_{V,i}[k]$. The integer part is generated by another accumulator, the Variable Phase Accumulator (VPA). The VPA uses CKV, i.e. the oscillator output, as its clock and increases its output by one for every rising edge of CKV. The output of the VPA is sampled by a flip-flop (FF), clocked with REF to make the output synchronized with $R_V[k]$. The fractional part is generated by a Time-to-Digital Converter (TDC), which measures the time difference between a rising edge of REF and a rising edge of CKV.

Just as in the analog PLL, the ADPLL strives to make the phase error zero, i.e. $R_R[k] = R_V[k]$. Since $R_R[k] = k \cdot \text{FCW}$ and $R_V[k] = k \cdot \text{CKV}/\text{REF}$, the output frequency will be:

$$\text{CKV} = \text{FCW} \cdot \text{REF}. \tag{2.2}$$

After the phase detection, $\phi_e[k]$, which is only a digital word, is fed through a digital loop filter (DLF). The DLF consists of only logic building blocks, thus erasing the need for large passive components. The DLF also has another major advantage; given its digital nature the loop parameters can easily be modified when active to give it more beneficial properties, e.g. increased bandwidth during acquisition for faster locking [13]. Following the DLF, the digital word reaches the Digitally Controlled Oscillator (DCO), which is tuned discretely by the control word, compared to continuous tuning by a control voltage in the regular PLL. As we will see in chapter 5, the tuning is usually achieved by turning on and off capacitance banks of varying sizes.

Although the discrete frequency tuning of the ADPLL makes it very noise-resilient, it also comes with a major drawback: The ADPLL will never have the correct output frequency due to its finite frequency resolution. This will cause a quantization noise, which is added to the regular phase noise of the oscillator, (more on phase noise in chapter 3) in the DCO according to [14]:

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{1}{12}\cdot\left(\frac{\Delta f_{res}}{\Delta f}\right)^2\cdot\frac{1}{f_{ref}}\cdot\text{sinc}\left(\frac{\Delta f}{f_{ref}}\right)\right], \tag{2.3}$$

where Δf_{res} is the frequency resolution, Δf the frequency offset from the oscillation frequency, and f_{ref} the input reference frequency. Thus, in order to minimize the phase noise, the frequency resolution of the DCO should be made as small as possible.

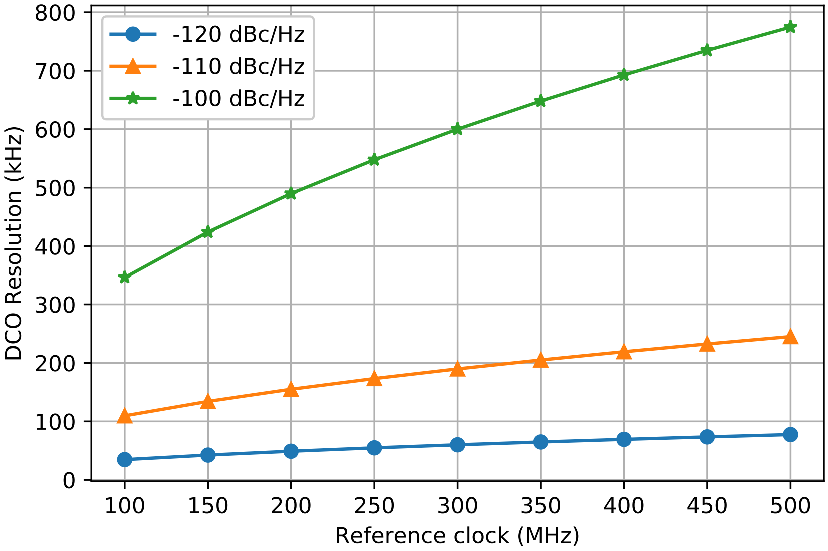


Figure 2.5: The frequency resolution required to keep the quantization noise below -120 dBc/Hz, -110 dBc/Hz and -140 dBc/Hz at 1 MHz offset at various reference clocks.

Fig. 2.5 plots how fine the resolution must be to keep the quantization noise below -100 dBc/Hz, -110 dBc/Hz and -120 dBc/Hz at 1 MHz offset at various reference frequencies. If the resolution is 100 kHz or finer, the quantization noise will be below -110 dBc/Hz for all reference frequencies. Since the phase noise for most mm-wave oscillators is around -90 dBc/Hz at 1 MHz offset, the quantization noise can then be considered negligible in this case.

A quantization noise will also be present in the TDC, since it will have a finite time resolution, and is given, in dBc/Hz, by [9]:

$$\mathcal{L}_{TDC} = 10\log\left[\left(2\pi\frac{\Delta_{TDC}}{T_V}\right)^2\cdot\frac{T_{ref}}{12}\right], \tag{2.4}$$

where Δ_{TDC} is time resolution of the TDC, T_V the period of the DCO output and T_{ref} the period of the reference clock. This can be a substantial part of the output noise [9].

Chapter 3

Oscillators

The oscillator is a central unit in PLLs, as discussed in chapter 2. This chapter gives a brief introduction to the important metrics of electrical oscillators. For a more in-depth discussion we refer to the excellent textbooks [7],[15], or our personal favorite [5].

3.1 Cross-coupled LC Oscillators

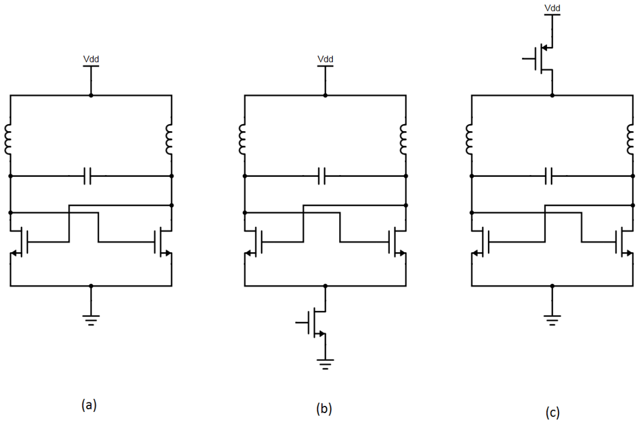


Figure 3.1: Three different oscillator topologies.

There are countless number of different oscillators described in the literature. For integrated radio applications, the cross-coupled LC oscillator is the most popular one [5]. In Fig. 3.1, three common implementations of this oscillator are shown. All the oscillators in Fig. 3.1 consist of an LC tank and a differential pair. The oscillators in Fig. 3.1(a) and Fig. 3.1(b) also have a current source. The differential pair is shown in Fig. 3.2. If a test voltage is applied over the pair, it is easy to show that it will generate a negative resistance, $R = -\frac{2}{g_m}$, as shown in Fig. 3.2. This assumes that g_{ds} is small and can be neglected. The negative resistance injects power into the LC tank. If the negative resistance can overcome the loss in the

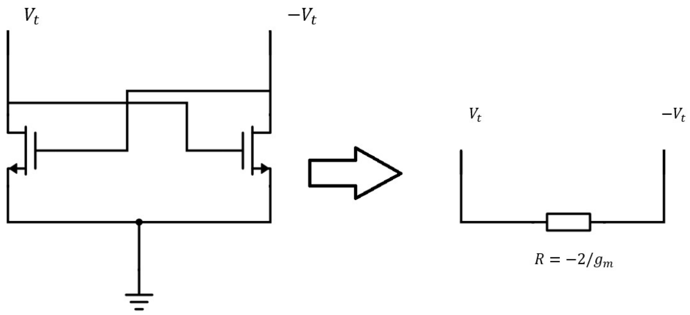


Figure 3.2: The differential pair modeled as a negative resistance.

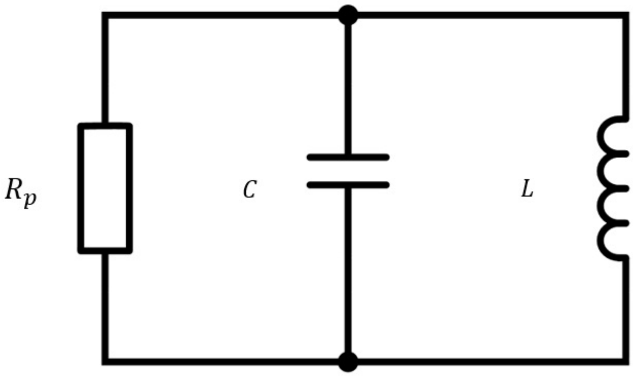


Figure 3.3: LC tank where the losses are modeled with a parallel resistance.

LC tank the circuit will start to oscillate. The oscillators amplitude will continue to grow until the nonlinearities of the transistors limits the amplitude.

The important metrics of electrical oscillators are power consumption, phase noise and tuning range.

3.2 LC Tank

The LC tank has a big impact on the performance of an LC oscillators. Fig. 3.3 shows a LC tank with a resistor in parallel, where the capacitor and inductor are considered ideal. The resistor R_p is non-physical, and is inserted to account for the losses in the capacitor and inductor. The value of R_p can be calculated from the physical series resistance of the inductor and capacitor [5], [7] and [15].

An important metric of the LC tank is its quality factor Q, which tells how small its resistive losses are. The quality factor is defined according to equation

3.1. The Q value of a lone capacitor with a series resistance is given by equation 3.2. The Q value of a lone inductor with a series resistance R_s is given by equation 3.3. The total Q value of the tank is given by equation 3.4 [5]. Equation 3.5 gives the Q value when the capacitance consists of multiple capacitors, which is the case in a DCO and some VCOs [5]. C_t in this case is the total capacitance of the tank, while $C_i, Q_i, i \in 1, 2...n$ are the capacitance and quality factor of each capacitor. From this equation it can be seen that it is most important that the largest capacitor have a high Q value in order to maintain a high total Q value.

From Fig. 3.4, it can be seen that the bandwidth of the LC tank is closely connected with the Q value. A high Q value gives rise to a narrow bandwidth. In next the section it will be shown that a high Q suppresses phase noise.

$$Q = 2\pi \frac{stored\ energy}{dissipated\ energy\ per\ cycle} \tag{3.1}$$

$$Q_C = \frac{1}{CR_s\omega_0} \tag{3.2}$$

$$Q_L = \frac{L\omega_0}{R_s} \tag{3.3}$$

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{3.4}$$

$$\frac{1}{Q_t} = \frac{1}{Q_L} + \frac{C_1}{C_t}\frac{1}{Q_1} + \frac{C_2}{C_t}\frac{1}{Q_2} + \cdots + \frac{C_n}{C_t}\frac{1}{Q_n} \tag{3.5}$$

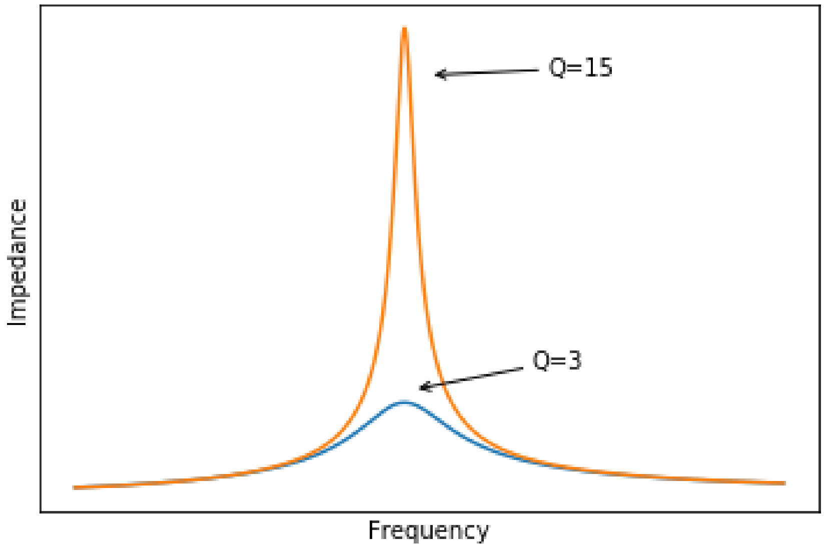
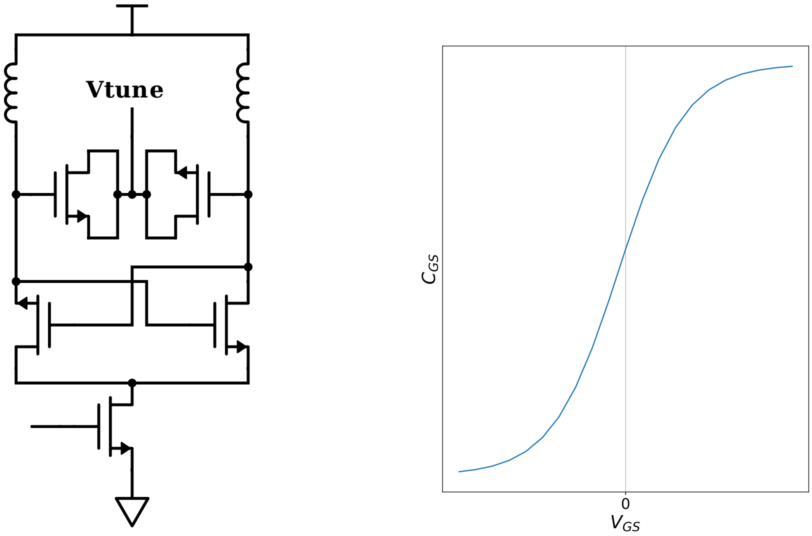


Figure 3.4: Impedance of two different LC tanks, one with Q=3 and next with Q=15.



(a) **(b)**

Figure 3.5: (a) A MOS varactor used in an LC oscillator. (b) Typical $C_{GS} - V_{GS}$ characteristic of an accumulation-mode NMOS varactor.

3.3 Tuning

So far, oscillators with fixed passive components have been described. In order to use the oscillator in a PLL, the resonance frequency must be possible to tune electronically. The inductance of the tank is difficult to vary electronically, so it is usually the capacitance that is changed[1]. The most common way to do this in an integrated circuit is to use a MOS varactor, a MOSFET with its source and drain shorted, as shown in Fig. 3.5a [5]. The used MOSFET is usually in accumulation-mode, meaning that the surrounding well is doped that same way as the transistor, i.e. NMOS in n-well or PMOS in p-well. This results in a $C_{GS} - V_{GS}$ characteristic that has the same sign on the slope for all voltages. The $C - V_{GS}$ characteristic for a typical NMOS varactor is shown in Fig. 3.5b. Thus by changing V_{tune}, the capacitance and thereby the resonance frequency in Fig. 3.5a can be changed.

3.4 Phase Noise

Ideally, we would want an oscillator that oscillates at a single frequency with an infinitesimal small spectrum width. Such an oscillator would ensure that a

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[1] Though there are methods to tune the inductance instead, as is described in chapter 5.

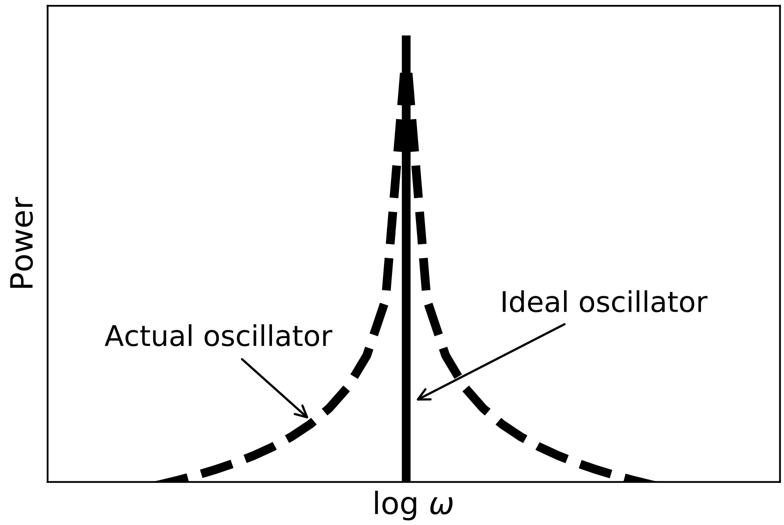

Figure 3.6: Frequency spectrum of ideal and actual oscillator.

transceiver would not disturb or be disturbed by nearby channels. This is of course not possible. In reality, an oscillator produces a skirt-like spectrum with its center at the resonance frequency, see Fig. 3.6. This widening of the resonance peak is due to random fluctuations of the phase in the oscillator, and is thus called *phase noise*. In this section, a short derivation of the phase noise in an LC oscillator is given, following the reasoning in [7].

Consider the circuit in Fig. 3.7. The inductor and capacitor provides the desired resonance frequency, while the active device acts as an energy-restoring device by providing a negative resistance equal in magnitude to the resistor. If we assume that the active device is noiseless, the noise in this circuit will be purely thermal noise from the LC tank and is given by:

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R}, \tag{3.6}$$

where $\overline{i_n^2}$ is the mean-square noise current spectral density, Δf the noise bandwidth, k Boltzmann's constant and T is the temperature in Kelvin. In order to get the voltage noise, we multiply this current noise with the effective impedance of the oscillator. Since the active device cancels the resistance of the tank, the impedance will simply be that of the lossless LC network, which will act as a bandpass filter. Therefore, we are only interested in noise close to resonance frequency. The impedance of the circuit for a small frequency offset $\Delta\omega$ from the resonance frequency ω_0 can be approximated by:

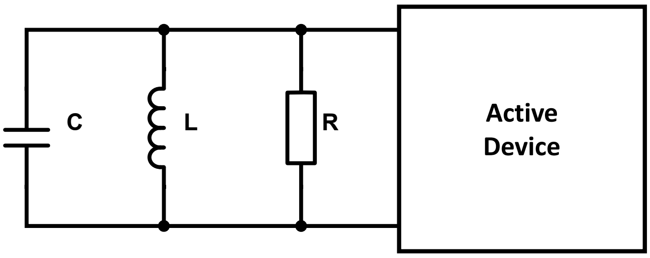

Figure 3.7: A basic resonance circuit.

$$|Z(\omega_0 + \Delta\omega)| \approx \frac{\omega_0 L}{2(\Delta\omega/\omega_0)} = R \cdot \frac{\omega_0}{2Q\Delta\omega}. \tag{3.7}$$

The spectral noise density then becomes:

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot |Z|^2 \approx 4kTR\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{3.8}$$

This noise density accounts for both amplitude and phase fluctuations, which are equally large. Since we are only interested in phase fluctuations, eq. 3.8 should be divided by two.

The phase noise is usually expressed in decibels normalized to the signal power. Eq. 3.8 then becomes:

$$\mathcal{L}(\Delta\omega) = 10\text{log}\left[\frac{2kT}{P_{sig}} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right], \tag{3.9}$$

where P_{sig} is the signal power. The unit for $\mathcal{L}$ is dBc/Hz, i.e. decibels below the carrier per hertz. We can see that in a logarithmic scale, the phase noise should have slope of -2 relative to the offset frequency. Furthermore, we should maximize Q of the bank and the signal power, in order to minimize the phase noise.

During this analysis, we have made some approximations. We have assumed that the active device is noiseless, which of course is not true, and that the oscillator is a linear, time-invariant (LTI) system, when it should be considered as a linear, time-varying system (LTV) [16]. In addition to this, the noise can't decrease forever, but will eventually reach a noise floor. A more correct formula for phase noise is given by Leeson in [17]:

$$\mathcal{L}(\Delta\omega) = 10\text{log}\left[\frac{2FkT}{P_{sig}}\left(1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right]. \tag{3.10}$$

Here, flicker noise in the active devices has been accounted for by adding a $1/\Delta\omega^3$ area with a corner frequency of $\Delta\omega_{1/f^3}$. Moreover, an empirical fitting parameter F has been added to account for additional white noise added by the active devices, along with a noise floor corner frequency of $\omega_0/2Q$. Fig. 3.8 shows the difference between the two equations.

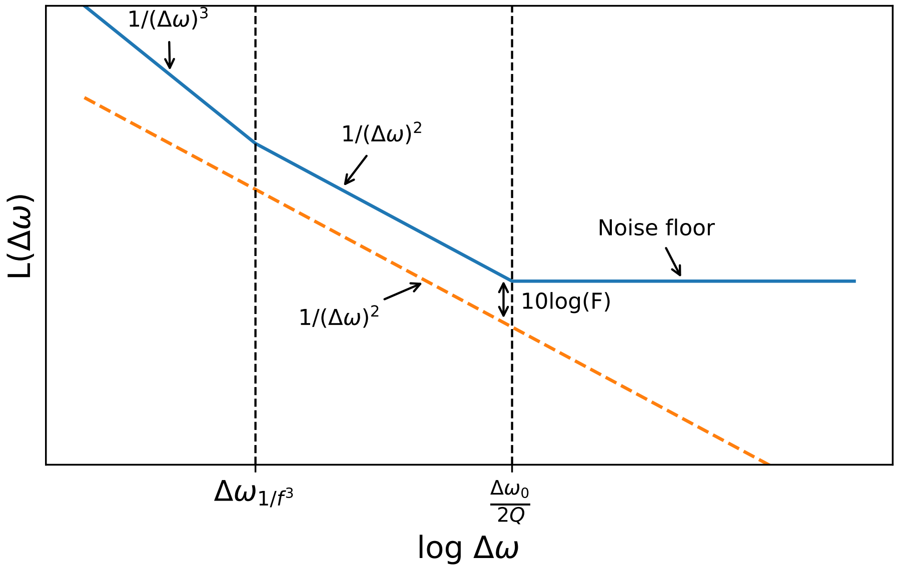

Figure 3.8: Comparison of eq. 3.9 (dashed curve) and eq. 3.10 (solid curve).

3.5 Figure-of-Merit

From the Leeson's formula, it is clear that there is a direct trade-off between P_{sig}, ω_0, Q and $\Delta\omega$. It is therefore possible to define a Figure-of-Merits 3.11 for the total oscillator on physical grounds.

$$\mathrm{FoM} = \mathrm{PN} - 20 \cdot \log_{10}(f_0/\Delta f) + 10 \cdot \log_{10}\left(\frac{\mathrm{P_{DC}}}{1\mathrm{mW}}\right), \tag{3.11}$$

where PN is the phase noise given in dBc/Hz at a frequency offset Δf and P_{DC} is the power consumption of the oscillator.

The Figure-of-Merit above doesn't account for the tuning range, which is a very important metric for an oscillator. Therefore, another Figure-of-Merit has been proposed [5]:

$$\mathrm{FoM_T} = \mathrm{PN} - 20 \cdot \log_{10}(f_0/\Delta f \cdot \mathrm{TTR}/10) + 10 \cdot \log_{10}\left(\frac{\mathrm{P_{DC}}}{1\mathrm{mW}}\right). \tag{3.12}$$

Here, TTR is the total frequency tuning range given in percent.

Furthermore, a third Figure-of-Merit for digitally controlled oscillator has been proposed in [14], which also considers the frequency resolution of the oscillator:

$$\mathrm{FoM_{DT}} = \mathrm{PN} - 20 \cdot \log_{10}(f_0/\Delta f \cdot \mathrm{TTR}/10) \cdot \mathrm{N_{eff}}/10 + 10 \cdot \log_{10}\left(\frac{\mathrm{P_{DC}}}{1\mathrm{mW}}\right), \quad (3.13)$$

where $\mathrm{N_{eff}}$ is the effective number of tuning bits in the DCO and is given by:

$$\mathrm{N_{eff}} = \log_2\left(f_0 \frac{TTR}{100 \cdot \Delta f_{res}}\right), \quad (3.14)$$

i.e. it is the number of bits required to cover the entire frequency range.

3.6 Groszkowski Theory

In his 1933 paper, Groszkowski analyses the interdependence of frequency variation of the harmonic content [18]. In other words, the fundamental frequency is dependent of the amplitude of the harmonics. In [18] a closed formula connecting the amplitude of the harmonics and the fundamental frequency is derived for a single ended LC oscillator. It is shown that an increase in the harmonics leads to drop in fundamental frequency. Physically this can be understood as follows: When the voltage over the tank reaches its peak, no current travels trough the inductor. Hence all the energy is stored over the capacitor. When the voltage is at its DC level, the capacitor stores no energy and the inductor stores all the energy. Since the oscillator is assumed to be stable, the electrostatic energy in the capacitor and the magneto-static energy in the inductor must be exactly equal over a cycle. If only the fundamental frequency is present in the oscillator. The impedance of the inductor and the capacitor would be exactly equal. The harmonics will however see a much lower impedance over the capacitor than over the inductor and thus load more energy over the capacitor than the inductor. The fundamental frequency compensate for this by decreasing. In this way the fundamental frequency will see a lower impedance over the inductor than the capacitor. The fundamental frequency will load more energy over the inductor and in this way ensure that the energy in the capacitor and the inductor is exactly equal.

The situation is somewhat different for the differential oscillators depicted in Fig. 3.1. Since the even harmonic doesn't see the capacitor at all, the analysis in [18] can't be applied without some modifications. The even harmonics only see the inductor and will increase the magneto-static energy. If the even harmonics increase the fundamental frequency will rise. The odd harmonics see both the inductor and the capacitor, hence an increase in these harmonics will decrease the fundamental frequency.

Chapter 4

Inductor

If capacitive tuning is used, the many tuning banks in an DCO create a large parasitic capacitance that can potentially limit the oscillators frequency. For exactly this reason the inductor should be small. The natural question becomes how small can the inductor become while maintaining a reasonable Q value. In order to investigate this, one-turn inductors were simulated for different widths, defined as shown in Fig. 4.1.

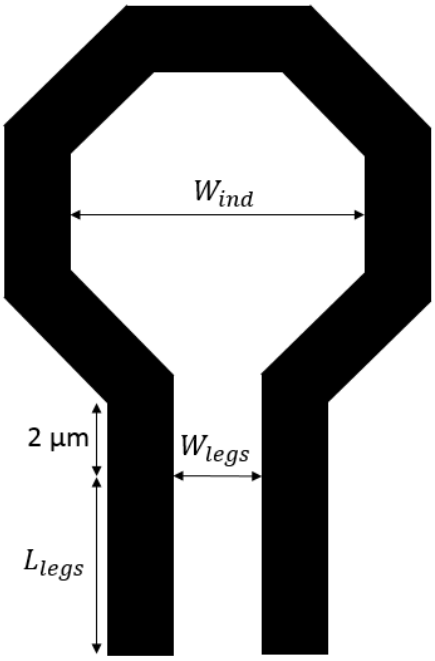

Figure 4.1: Conceptional picture of the inductor.

Fig. 4.2 shows the Q value for three different inductors. The inductor with width 18.4 µm were chosen as a compromise between small inductance and large Q. Fig. 4.3 shows how the inductance relates to L_{legs} for the inductor with width

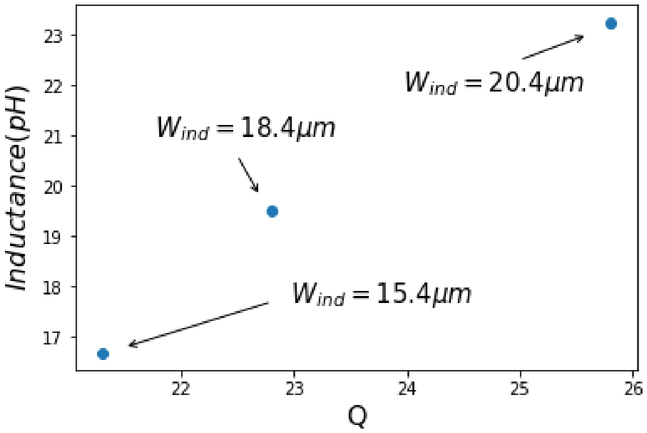

Figure 4.2: Q plotted versus L for inductors of different sizes W_{ind}, simulated at 90 GHz.

18.4 µm. Fig. 4.4 shows how the Q decreases with increasing L_{legs}, also for the 18.4 µm inductor. Simulations showed that with increasing width W_{legs} of the inductor, the inductance increased while only having a very small effect on the Q value. Hence W_{legs} was chosen to be as small as possible with respect to the design rules. The performance of the inductor obviously decreases with increasing L_{legs}. The bank should therefore be designed so that the length of the legs are minimized.

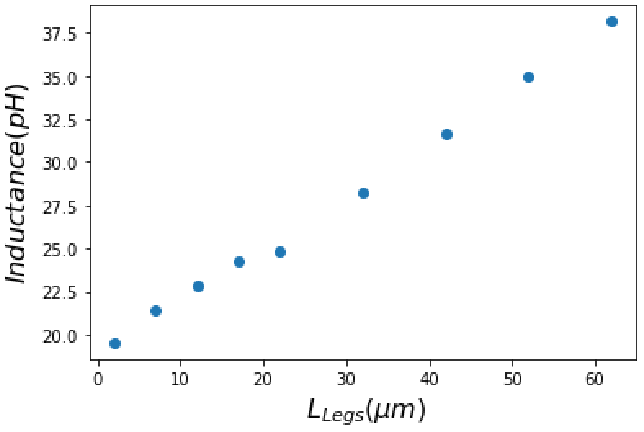

Figure 4.3: Inductance plotted versus L_{legs}, simulated at 90 GHz.

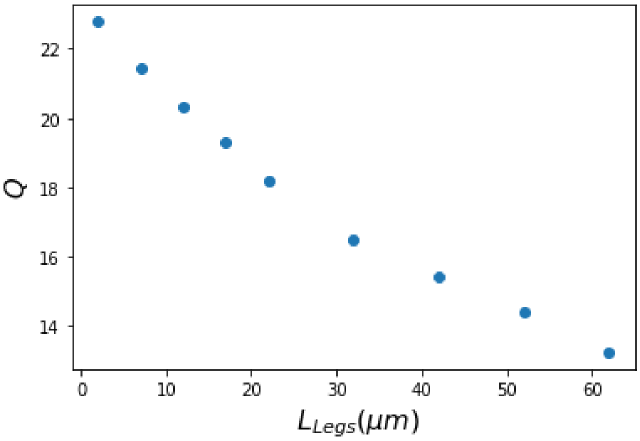

Figure 4.4: Q plotted versus L_{legs}, simulated at 90 GHz.

Chapter 5

Digitally Controlled Oscillator

What differs the digitally controlled oscillator from the voltage controlled oscillator is how the frequency tuning is achieved. As described in chapter 2, the frequency tuning in the VCO is achieved by varying the control voltage continuously. In a DCO on the other hand, the frequency tuning is done by digitally turning on and off tuning cells. These tuning cells usually changes the capacitance of the LC tank when switched, since it is easier to change a capacitance than inductance electrically [19].

The tuning cells are usually combined into three or more banks [19]; a coarse bank to deal with process, voltage and temperature (PVT) variations, a middle bank for acquisition, and a fine bank for tracking when the ADPLL is locked. The coarse and middle banks are generally implemented using either switched capacitors or varactors, or a combination of both, which are connected between the inductor and the cross-coupled transistor pair, i.e. to the core of the oscillator. However, at mm-wave frequencies this approach is generally not possible for the fine bank, since the capacitance steps would have to be extremely small. To overcome this obstacle, several methods have been proposed in the literature and are covered in section 5.2, along with some methods not covered in the literature.

5.1 Coarse and Middle Banks

The coarse and medium banks set the total tuning range (TTR) of the DCO. To achieve a large tuning range, the C_{on}/C_{off} ratio, i.e. the capacitance when all the banks are turned on and turned off, respectively, must be large, thus C_{off} should be as small as possible. This can be done by reducing the size of wires and transistors in the tuning cell to reduce parasitic capacitances. However, this increases the resistance of the cell, which reduces the Q value, which in turn increases phase noise. Hence, there is a trade-off between tuning range and phase noise. This is especially prominent at mm-wave frequencies, where the Q value of the whole oscillator is mainly dominated by the capacitance bank, rather than the inductor [20].

Another important factor for these banks are of course their resolution, i.e. the smallest frequency step that can be made. The smallest frequency step of the bank must be smaller than the total tuning range of the smaller bank, since otherwise frequency gaps would exist.

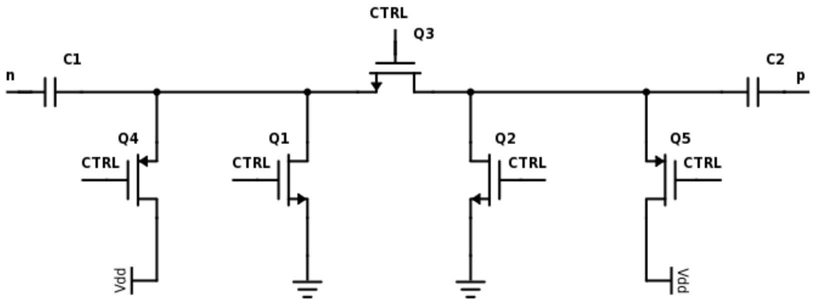

Figure 5.1: Typical design of switched capacitor cell.

As mentioned earlier, switched capacitor and varactor cells are by far the most common coarse tuning method, and are covered below. In addition to this, some other proposed methods are described.

5.1.1 Switched capacitor

A typical switched capacitor (SC) design is shown in Fig. 5.1. Two metal-oxide-metal (MOM) capacitors, $C1$ and $C2$, are connected to five transistors, $Q1$-$Q5$. $Q3$ has the largest width-to-length ratio, followed by $Q1$ and $Q2$, while $Q4$ and $Q5$ have the smallest ratio. When $CTRL$ is pulled high, $Q1$, $Q2$, and $Q3$ are turned on and $Q4$ and $Q5$ turned off. Since $Q3$ is large, an almost pure capacitance is seen between n and p. $Q1$ and $Q2$ help reduce the resistance by pulling the voltage towards ground and thereby increasing V_{GS} of $Q3$. When $CTRL$ is pulled low, $Q1$, $Q2$, and $Q3$ are turned off, while $Q4$ and $Q5$ are turned on. Since $Q4$ and $Q5$ are smaller than the other transistor, and have lower mobility due to being PMOS, a much larger resistance will be seen in this off-state than in the in on-state. By pulling the nodes to VDD in the off-state, the nodes are not left floating, which could cause $Q3$ to turn on if the voltage dropped to below 0 (V_{GS} of Q3 would then be positive), which would increase C_{off} [21]. Also, this reverse-biases the drain-bulk diode in $Q3$, further reducing C_{off} [22].

Fig. 5.2 shows an equivalent circuit seen from one of the input nodes, p or n, to AC ground. C_{mom} is the capacitance from the MOM-capacitor, R the resistance from the transistors, and C_{par} the parasitic capacitance from the transistors. We assume that $C_{par} << C_{mom}$. When the bank is in the on-state, R will be very small, and will basically short C_{par}. Thus, the capacitance seen from p or n will approximately be C_{mom}. In the off-state, R will be large, and can, in a simplified analysis, be ignored. The capacitance will then be a series combination of C_{mom} and C_{par}, which, given our previous assumption, will approximately be C_{par}. The conclusion to draw from this is that C_{par} should be minimized in order to minimize C_{off}. This can be done by reducing the dimensions of the transistors involved. However, this leads to higher resistances and thereby a lower Q-value. Therefore, great care must be taken when dimensioning the transistors.

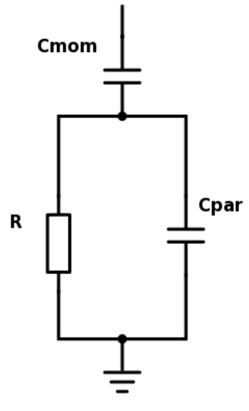

Figure 5.2: Equivalent circuit for the switched capacitor cell seen from input node to AC ground.

The benefit of the switched capacitor bank is that very high C_{on}/C_{off} ratios can be achieved, thus allowing for a large tuning range [22]. They are also easy to scale when used for a binary weighted bank, see section 5.1.4. However, in most process, the smallest possible MOM-capacitor is several femtofarads, and the smallest possible capacitance step for a SC will be on the same order. This corresponds to a frequency step of hundreds of megahertz at mm-wave frequencies, making this type of bank only suitable for coarse frequency tuning [23].

5.1.2 Varactor

Fig. 5.3 shows a typical varactor cell, which is the same as one would use in a VCO. The only difference is that $CTRL$ is pulled either to high or low, instead of being continuously tuned. For an NMOS varactor, the capacitance is at its highest when $CTRL$ is low and at its lowest when $CTRL$ is high, and vice versa for a PMOS varactor.

The capacitance step taken by the cell is determined by the dimensions of the transistors and the bias voltage V_{bias}, which is connected via two resistors to not short the AC signal [5]. To actually be able to set a custom DC level, the DC level of the oscillator core must be blocked, which is done by the two fixed capacitors. Moreover, the capacitors filters out supply noise, which would be converted to phase noise due to the non-linear $C - V$ characteristic of a varactor [24].

The advantage of the this varactor cell is that the smallest possible capacitance step is much smaller than for a SC cell. In fact, a varactor bank is often used for the fine tuning in DCOs operating at frequencies below 10 GHz [19][25][26]. At frequencies around 80 GHz, a frequency step of around 100 MHz can be achieved with varactors. However, the C_{on}/C_{off} ratio will be lower than for a SC cell. Moreover, as mentioned above, a varactor will cause more phase noise due to its intrinsic amplitude-to-phase conversion.

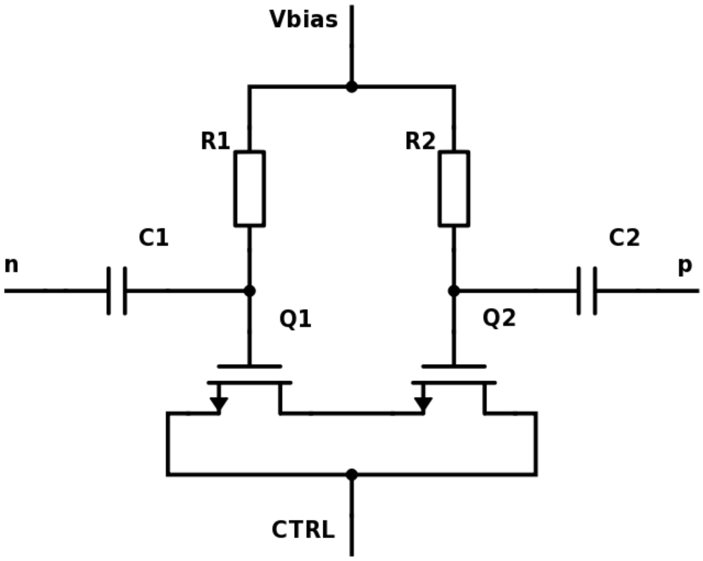

Figure 5.3: Typical design of varactor cell.

5.1.3 Other coarse-tuning techniques

While switched capacitors and varactors are the most common coarse- and mid-tuning techniques, several other methods have been suggested in the literature.

In [14], two parallel transmission lines are used for the coarse tuning. Beneath the lines, metal wires are placed perpendicular to the transmission lines. Each metal wire is divided in two, with a transistor placed between them, acting as a switch. When the transistor is turned on, the capacitance between the transmission lines and the metal line will change, causing a frequency shift of the DCO. In [14], they achieve a tuning range of 10 % at 60 GHz, with a capacitance resolution of 0.13 fF (for the coarse bank). Further, the worst-case Q-value is around 12 for the bank, which leads to low phase noise. However, the bank consumes a large chip area and has a rather low C_{on}/C_{off} ratio. This technique also requires extensive, time-consuming electromagnetic simulations.

Another solution is to use a DAC and connect it to a varactor [27]. The frequency is then set by the output voltage from the DAC, similar to a regular VCO. However, since varactors in a deep-submicron process posses a very steep capacitance-versus-voltage characteristic over a very small voltage range, they are highly sensitive to noise [19]. Thus, any noise from the DAC will be directly translated to a significant amount of phase noise. In addition to this, the DAC will increase the power consumption of the oscillator.

All the coarse tuning techniques described thus far have been capacitance-based. In [28], an inductance-based coarse tuning is instead utilized. This is done by coupling two open inductors, L_2 and L_3 to the primary inductor L_1. L_2 and L_3 can be shorted by transistors, which increases the effective inductance of L_1. By doing this, they manage to change the effective inductance from 117 pH to 154 pH and achieve a total tuning range of an impressive 24 % at 55 GHz. This method must of course be used in combination with other coarse tuning techniques for most purposes, since the number of tuning steps is equal to the number of coupled inductors, which is limited for physical reasons. The Q-value of the inductor also drops severely when L_2 and L_3 are shorted, from 21.4 to 12.2 in this case.

5.1.4 Binary-weighted versus unary-weighted

There are two common ways to design the capacitance banks; binary-weighted and unary-weighted, also known as thermometer encoded. In a unary-weighted bank, each cell is the same size. The cells are selected using unary coding, i.e. in order to activate for instance five cells, an 8-bit control word would be 00011111. In a binary-weighted bank on the other hand, each cell corresponds to a capacitance step that is twice as large as the previous cell. For instance, if the smallest cell has a capacitance step of ΔC_0, the second cell will have a capacitance step of $2\Delta C_0$, the third a step of $4\Delta C_0$ etc. These cells are activated using binary coding, so if cells corresponding to $5\Delta C_0$ are to be activated, an 8-bit control word would be 0000101.

Binary-weighted banks have two distinct advantages over unary-weighted; smaller chip area and less C_{off}. Some dimensions in a capacitance cell are fixed, regardless of the size of the capacitance step. For instance, in a SC cell, while the dimension of the MOM-capacitor scales roughly linearly with capacitance step, the transistors, guard rings, VDD and GND connections etc. stays roughly the same in size. In addition to this, since less cells are required for the same number of frequency steps for a binary-weighted bank, less wiring is required. Therefore, a binary-weighted bank with three cell, corresponding to eight frequency steps, will require less chip area than a unary-weighted bank with eight cells. The same argument can be made for the off-capacitance, since the parasitic capacitance is closely related to area.

One issue with binary-weighted banks is high switching noise due to several cells turning on and off at once, for instance when switching from 15 to 16. This would cause four cells to turn off and one cell to turn on (01111 to 10000), while it would only change the state of one cell for a unary-weighted bank. Another issue is mismatch between two cells in binary-weighted cells, which can cause frequency gaps in the tuning. This is a much smaller issue for unary-weighted cell, since every cell will be affected roughly the same by process variations and any local variations would most likely cancel out on average. [19]

Given these reasons, binary-weighted banks are usually used for coarse banks, where high resolution is not really an issue and since the cells will most likely not switch during active operation, thus making switching noise non-existent. Unary-weighted can be used for every type of bank, as long as C_{off} is not too large.

5.2 Fine-tuning techniques at mm wave frequency

Equation 5.1 relates a small change in frequency to a small change in capacitance. Assuming that a frequency change of 10 kHz is of interest at 90 GHz, the change in capacitance would need to be smaller than 0.2 aF. In order to get a feel for how extremely small this capacitance actually is, consider a 0.2 aF capacitor with one volt applied to it. The charge accumulated on the capacitor would correspond to approximately one electron. Thus, circuit solutions need to be employed to ensure that the oscillator can be tuned with capacitors drastically larger then 1 aF.

$$\Delta f_0 = -\frac{1}{4\pi} f_0 \frac{\Delta C}{C} \tag{5.1}$$

When considering a fine-tuning technique, there are several aspects to take into consideration. Here follows a brief explanation of the four most important:

Capacitive load If a oscillation frequency of 60 GHz or higher is to be reached, the capacitive load of the core may not exceed 250 fF with a 30 pH inductor. A large fine bank consisting of over 100 element can easily have a capacitance of over 100 fF, without layout parasitics. This means that the oscillator frequency would drop drastically. It is therefore imperative that the fine tuning scheme is capacitively shielded from the oscillator.

Tuning range and resolution As discussed above the smallest coarse tuning range that is practically achievable is about 100 MHz. The resolution of the fine bank should ideally be finer than 100 kHz (see Fig. 2.5). If this were to be implemented with unary-coding it would require 1000 fine tuning elements. Instead the fine tuning banks could be divided in two, which would only require 32 fine tuning elements in each bank. Hence in broad terms two types of fine tuning banks is of interest, one that can tune from 100 MHz down to a few MHz and one that can tune from a few MHz down to a few kHz. Using three fine banks an even finer resolution could potentially be obtained.

Area consumption and simulation. If the fine bank is to be implemented unary, it may well occupy a considerably area of the total oscillator. The smallest available capacitor is typically 3 µm × 3 µm. A fine bank using a 100 of these capacitors, along with control transistors, might occupy an area of 40 µm × 40 µm. Apart from the obvious drawback of increasing area consumption, a large area of the fine bank also come with a another disadvantage. A large layout results in large parasitic capacitance and inductances. Parasitic capacitance can affect the fine tuning making the frequency step uneven. Resonance with parasitic inductance can have devastating effect on the fine tuning scheme. For this reason capacitors are ill-suited for large fine tuning banks. Because of their smaller size, varactor are better suited for a large fine tuning bank. If a very large fine bank is implemented the designer have to take great care to ensure that the parasitics doesn't deteriorate the performance of the fine bank.

Process and temperature variation Many fine tuning schemes is limited by process variations. If the parasitics are on the same scale as the component, the total capacitance might be highly sensitive to process variations. If active devices are used for fine frequency tuning, the temperature dependency have to be closely investigated. Further, noise from control transistors or varactors of the fine bank should not be injected into the oscillator core.

5.2.1 Capacitive Degeneration

In [29], a high frequency resolution is achieved by using source degeneration on the cross-coupled transistor pair using capacitors. Fig. 5.4 shows three different way to implement this. The implementations differ in how they achieve an impedance to ground, since without this the variable capacitor would be shorted. In the following analysis, we have assumed that the impedance to ground is much larger than the impedance of the capacitance and can thus be ignored. Although the oscillator in [29] only operates at 3 GHz, this method has also been successfully used at mm-wave frequencies [28].

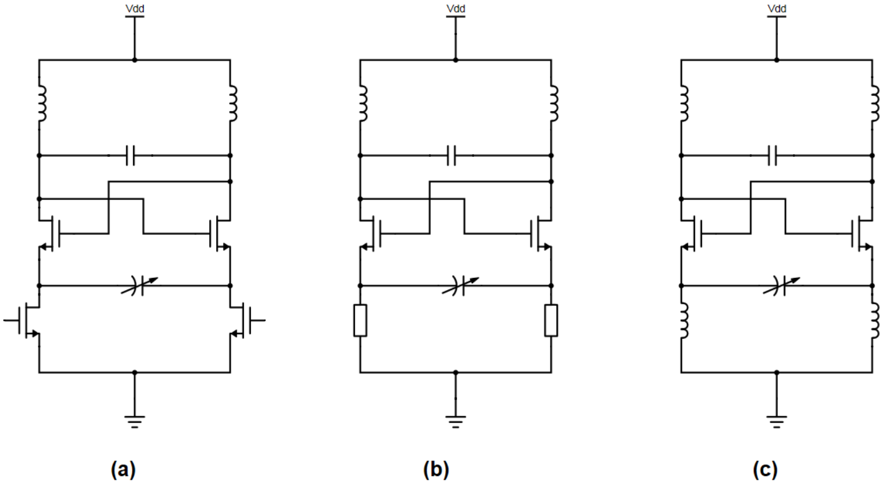

Figure 5.4: Three different implementations of capacitive degeneration using transistors, resistors and inductors, respectively.

When using source degeneration, the extrinsic transconductance of a transistor will be [30]:

$$G_m = \frac{g_m}{1 + g_m Z_S} = \frac{1}{\frac{1}{g_m} + Z_S}, \tag{5.2}$$

where g_m is the intrinsic transconductance of the transistor and Z_S the degenerating impedance. For our case, with two transistors, each degenerated with $C/2$, the transconductance becomes a transadmittance:

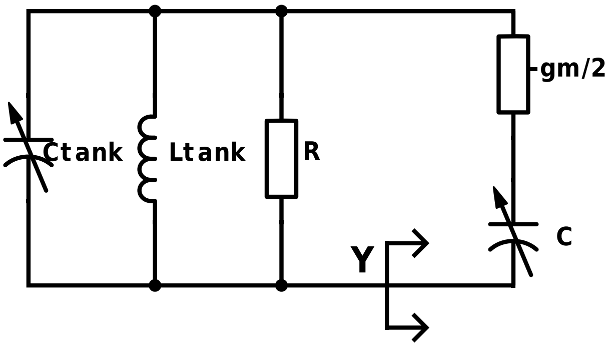

Figure 5.5: Equivalent schematic of oscillator with capacitive degeneration.

$$Y = \frac{1}{\frac{2}{g_m} + \frac{1}{jwC}}. \tag{5.3}$$

Thus, the oscillator can be modeled according to the schematic shown in Fig. 5.5. Rearranging Y gives:

$$Y = -\frac{g_m}{2} \cdot \frac{4C^2\omega^2}{g_m^2 + 4C^2\omega^2} - j\omega C \frac{g_m^2}{g_m^2 + 4C^2\omega^2}. \tag{5.4}$$

The imaginary part of Y divided by ω becomes the equivalent capacitance, C_{eq}, seen by the oscillator core:

$$C_{eq} = -C \frac{g_m^2}{g_m^2 + 4C^2\omega^2}. \tag{5.5}$$

C_{eq} is thus shrunk by a factor $\frac{g_m^2}{g_m^2+4C^2\omega^2}$. It is plotted in Fig. 5.6, along with the real part of Y, i.e. the equivalent transconductance seen by the oscillator core, $g_{m,eq}$. At first, C_{eq} decreases with increasing C with a rather steep slope (although the slope is of course below unity), then it reaches its minimum point before starting to increase, but with a slope much smaller than unity. By operating in this second region, very small frequency steps can be achieved by using switchable capacitance banks as the degeneration capacitance.

This method is easily implemented, since cells already used for the coarse bank can be used here as well. The cells also do not capacitively load the core. In fact, they do the opposite, since they provide a negative capacitance and thereby reduce C_{off}. Thanks to this, an impressive tuning range of 24 % is achieved in [28]. Further, this method improves the phase noise slightly. However, as seen in Fig. 5.6, unless C is very large, $g_{m,eq}$ will be reduced, which can cause oscillation to stop. Further, the previous analysis has been done assuming an ideal capacitance. Of course, some resistance will be present. In eq. 5.2 and eq. 5.3, one can easily see that a resistance added to Z_S will reduce $g_{m,eq}$.

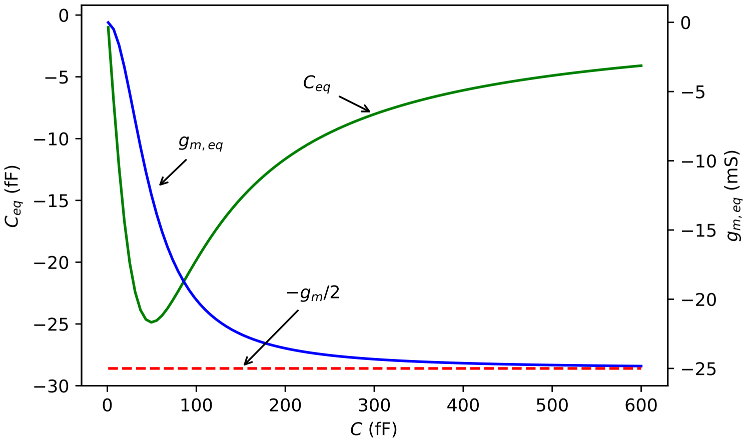

Figure 5.6: Plot showing $g_{m,eq}$ and C_{eq} versus C. Also plotted is the transconductance without capacitive degeneration, -$g_m/2$. Used values are g_m = 50 mS and f_0 = 80 GHz.

Another issue with this method is perhaps a more subtle one. Referring back to eq. 5.1, one can see that the frequency change for a certain change in capacitance connected directly to the oscillator core will decrease with decreasing frequency. However, since the shrinking factor for capacitive degeneration *increases* with decreasing frequency, the frequency change will be the largest for a fixed capacitance change at the *lowest* frequency. In addition to this, our simulations showed that the frequency step will decrease when in the *slow-slow* process corner due to the decrease in g_m using this method, while it will increase the frequency step for the coarse bank, and vice versa in the *fast-fast* corner. The consequence of these two observations is that the bank must be designed to cover the smallest frequency step of the coarse bank at the highest frequency in the *slow-slow* corner in order to ensure that no gaps are possible. However, this will lead to a rather poor frequency resolution at the lowest frequency, especially in the *fast-fast* corner.

5.2.2 Improved Varactor design

In [31], a fine-tuning technique utilizing an improved varactor design was suggested. Two varactor pairs are used, as shown in Fig. 5.7, and an inverter is connected between the two. In one of the pairs, the transistors has a certain width W_0. In the other pair, the transistors has a width of W_0+W_{min}, where W_{min} is the smallest increment in width allowed by the design process. Because of the inverter, only one of the pairs will be activated in the cell's on-state, while the other pair will be activated in the off-state. Thus, the capacitance step will be the difference between the varactor pairs in their on-state, which will be extremely small due to the very small, but non-zero, difference in width. In [31], a capacitance step of 2 aF was achieved.

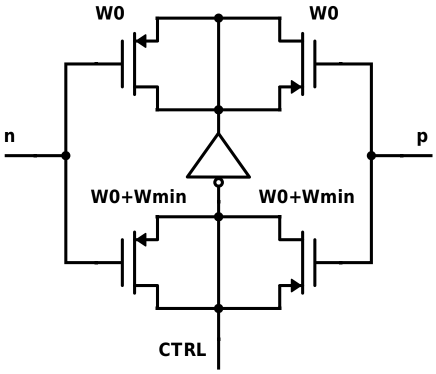

Figure 5.7: Proposed design for a fine-tuning varactor cell.

An issue with this method is that C_{off} for the cell will be C_{on} for a regular varactor cell (since one varactor pair is always activated), which will be a substantial amount for a bank with 32 cells, as used in [31]. This will limit both the tuning range and will make it harder to achieve a high center frequency.

5.2.3 Transformer-coupled fine-tuning

In [14], a transformer-based fine-tuning is described. If a secondary coil L_s with a capacitance C_L is coupled to the primary inductor L_p of the oscillator with a coupling factor k_m, the inductance of L_p will appear to change to an equivalent inductance L_{eq} according to:

$$L_{eq} = L_p \left(1 + k_m^2 \frac{\omega^2 L_s C_L}{1 - \omega^2 L_s C_L} \right). \tag{5.6}$$

If we assume that $\omega^2 L_s C_L << 1$, i.e. we are operating far from the resonance frequency of the secondary inductor, this simplifies to:

$$L_{eq} \approx L_p (1 + k_m^2 \omega^2 L_s C_L) \tag{5.7}$$

If the C_L were connected directly to L_p instead of using a transformer, the equivalent inductance would then be:

$$L_{eq} = \frac{L_p}{1 - \omega^2 L_p C_L} \approx L_p (1 + \omega^2 L_p C_L). \tag{5.8}$$

By comparing these results, we see that the tuning sensitivity is attenuated by a factor $k_m^2 L_s / L_p$ when using a transformer. Since k_m can be set well below unity and L_p can be made larger than L_s, the frequency steps can be made very small.

This method has two major benefits. The first one is that it since the C_{off} of the bank will also be attenuated by a factor $k_m^2 L_s / L_p$, it will put a very small capacitive load on the oscillator core. The second one is that both in [14] and in our simulations, a uniform frequency step from each capacitance cell was achieved,

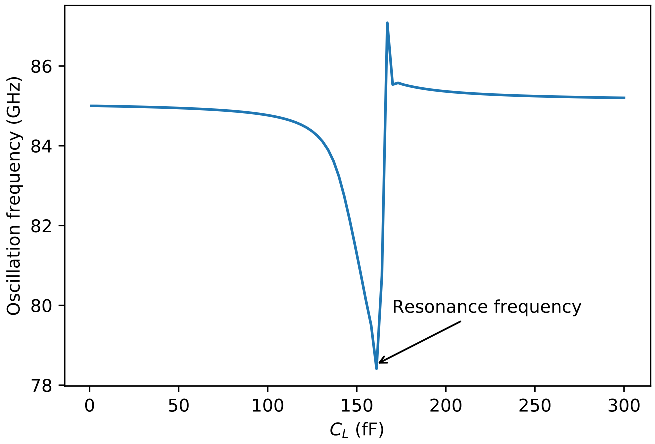

Figure 5.8: Oscillation frequency versus C_L. Clearly, resonance in the secondary inductor is something to be avoided. Used values were k_m = 0.05, L_p = 50 pH, L_s = 25 pH.

resulting in a highly linear frequency tuning. An issue with this method is that to achieve a high frequency resolution, the coupling factor must be very small. This makes it highly sensitive to process variations and thus puts a limit to the practical achievable frequency resolution [23]. In [14], the resolution is only 2.5 MHz, which is worse than all other techniques suggested in this chapter. The design must also be done carefully so that the resonance frequency of the secondary inductor does not coincide with the operating frequency, since this would cause very large frequency shift for a small change in C_L, see Fig. 5.8.

5.2.4 Switched-Capacitor Ladder

In [23], a fine-tuning method which achieves an impressive extrapolated frequency resolution of 4 Hz at 60 GHz[1] is proposed. This is done by connecting capacitors in a ladder, as shown in Fig. 5.9. Each step i consist of two large, fixed capacitors, C and $2C$, and two smaller, switchable capacitors, $2\Delta C$ and ΔC, controlled by bits b_{2i-1} and b_{2i}, respectively. The fixed capacitor will reduce the capacitance step of the switchable capacitors at each step by a scaling factor k, for a total reduction of k^i at step i.

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[1] This is of course not possible to measure at these frequencies, thus they measured the average capacitance change from the early stages and extrapolated to get the capacitance change from the last stage.

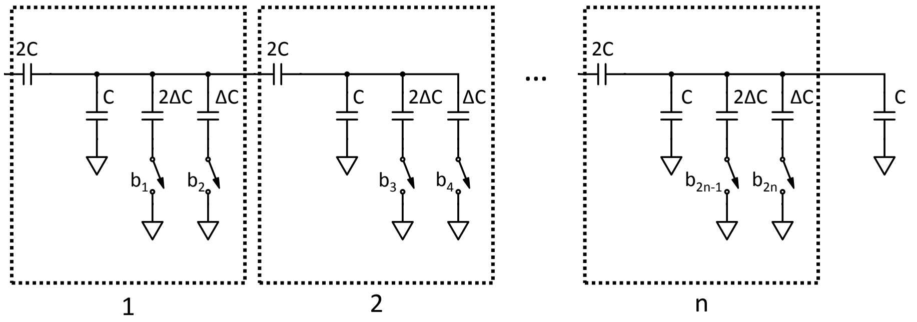

Figure 5.9: Schematic showing the capacitance ladder used in [23].

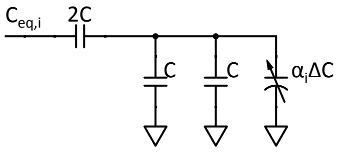

Figure 5.10: Equivalent circuit for the ith stage in the ladder.

For an initial analysis of the schematic in Fig. 5.9, let's begin with the nth stage of the ladder. There, an extra capacitor with capacitance C has been added, giving a total capacitance of approximately $2C$ after the series capacitance $2C$, assuming that the tunable capacitors are much smaller than the fixed. The input capacitance for this stage will then be C. Moving on to $(n-1)$th stage, it will thus see an extra capacitance of C from the nth stage. By repeating the previous analysis, it is easily shown that the input capacitance of this stage will also be C. Thus, a general schematic of the ith stage in the ladder can be created, where the capacitance of all the subsequent stages are modeled with a capacitance C, as shown in Fig. 5.10. $\alpha_i \Delta C$ is the tuning range of the ith stage, plus the effective tuning range, $\alpha_{i+1}\Delta C/k_{i+1}$, of the $(i+1)$th stage. The equivalent capacitance of this circuit will be:

$$C_{eq,i} = \frac{2C \cdot (2C + \alpha_i \Delta C)}{4C + \alpha_i \Delta C} = C + \frac{C \cdot \alpha_i \Delta C}{4C + \alpha_i \Delta C} \approx C + \frac{1}{4}\alpha_i \Delta C. \quad (5.9)$$

The scaling factor k_i is thus approximately a constant of $1/4$. Using this equation, the total capacitance of the ladder can be calculated:

$$\begin{aligned} C_{tot} &\approx C + \frac{1}{4}\left[2b_1 + b_2 + \frac{1}{4}(2b_3 + b_4) + ... + \frac{1}{4^n}(2b_{2n-} + b_{2n})\right] = \\ C &+ \left(\frac{1}{2}b_1 + \frac{1}{2^2}b_2 + \frac{1}{2^3}b_3 + \frac{1}{2^4}b_4 + ... + \frac{1}{2^{2n-1}}b_{2n-1} + \frac{1}{2^{2n}}b_{2n}\right)\Delta C. \end{aligned} \quad (5.10)$$

Here, we can clearly see that that the total tuning range of the bank is almost ΔC and the least-significant bit (LSB) can control a capacitance change of $1/2^{2n}\Delta C$. Thus the resolution can be chosen almost arbitrarily just by adding more stages to the ladder.

The approximation done in eq. 5.9 leads to a constant k_i of $1/4$, which in reality only is viable for a low $\Delta C/C$ ratio and for a limited number of steps. If k_i varies too much between stages, it will affect the control sensitivity and the loop bandwidth of the ADPLL. Thus, $\Delta C/C$ must be kept small, thereby greatly limiting the tuning range. Another issue with this method is that since C has to be large, it will severely load the oscillator if connected directly to the core. Therefore, they use a transformer coupling in [23], which scales down the capacitance seen from the DCO core. However, this will reduce the Q of the primary inductor. Furthermore, mismatch between the stages will lead to frequency gaps. Therefore, the fixed capacitors should not be designed with an 2-to-1 ratio, but rather a 5-to-3 ratio or similar, which reduces k, leading to an overlap in frequency tuning between stages.

5.2.5 Groszkowski fine-tuning[2]

As discussed in section 3.5 and [18], the fundamental frequency change with the amplitude of the harmonics. The even harmonic in Fig. 5.11 appears in a common mode fashion over the main tank capacitor. Hence the even harmonic only sees the impedance from the current source in series with half the inductor in parallel with the differential pair. If the capacitor $C_{variabel}$ grows large the current source is shorted for high frequencies. This will lead to decreasing amplitude of the even harmonics, resulting in a lower fundamental frequency. At some point the capacitor will resonate with the inductor. When $C_{variabel}$ grows past resonance the amplitude will begin to increase leading to higher fundamental frequency. The second harmonic at millimeter wave frequency can be well over 100 GHz. Because of the high frequency, the node connected to $C_{variabel}$ must be very carefully simulated, where all the parasitics inductances and capacitance are included.

Simulations showed that a very fine resolution is achievable using this method, and since the fundamental tone sees an AC ground at the node, it will not capacitively load the core. However, the tuning range is very limited and non-linear.

5.2.6 Inductor-based fine-tuning

This fine-tuning scheme was first reported in [14]. Thin metal strips are drawn under the inductor, see Fig. 5.12 (a), which can be connected and disconnected using a transistor. The fine tuning (change in inductor inductance) is highly non-linear, as seen in Fig. 5.12(b), which makes a unary implementation very hard to achieve. An advantage of this method is that the fine-tuning scheme occupies almost no additional area, due to the fact that the tuning elements are located under the inductor. It also does not capacitively load the core. However, the number of metal strips underneath the inductor, and thereby the number of tuning

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[2] This method has not been published in the literature, but Ericsson has applied a patent for it.

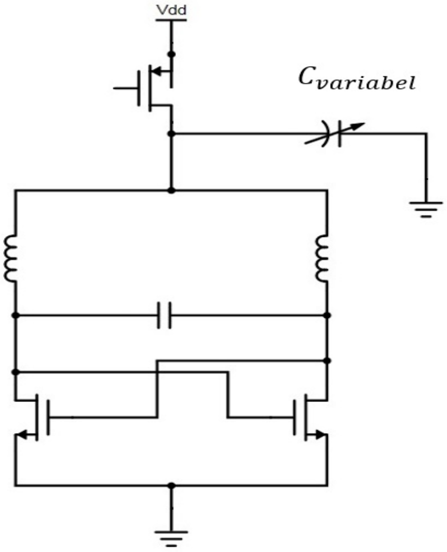

Figure 5.11: Conceptual view of fine tuning using the Groszkowski theory.

steps, are limited by the size of the transistor and the metal strip. A resolution of 160 kHz is achieved in [14].

An improvement of the linearity of this technique is suggested in [32]. Instead of running the metal strips across the whole inductor, they form loops by connecting the strip back to the inductor leg it originated from. The change of inductance will then only depend on the area of the loop and be independent of its position in the inductor, thus making it more linear. However, these loops will occupy a larger area and thereby even further limit the number of possible tuning steps.

5.2.7 Capacitive voltage division [3]

Another way to scale down the capacitance can be seen in Fig. 5.13. If $C1 = C4$ and $C2 = C3$, then a balanced voltage division will occur over $C_{variable}$, which will scale down its capacitance. Naturally, any fine tuning scheme that implements capacitive division will be limited by mismatch. Hence $C1$, $C2$, $C3$ and $C4$ ought to be chosen so that an appropriate scaling is achieved while maintaining some robustness towards process variations.

Since the capacitance cluster will be connected directly to the oscillator core, it will capacitively load the core.

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[3] This method is not presented in the literature, but was suggested by our supervisor Henrik Sjöland.

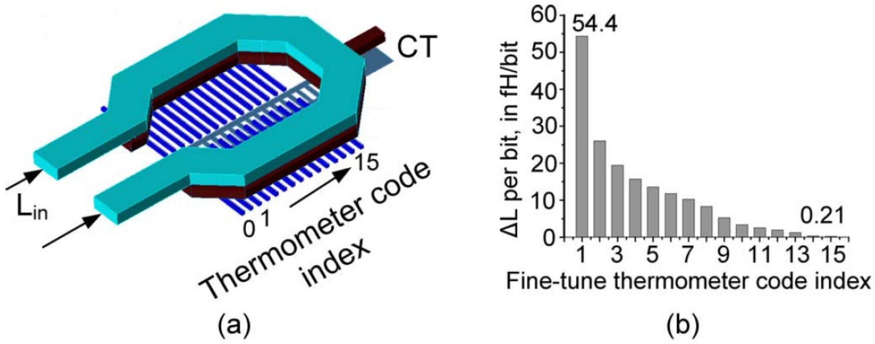

Figure 5.12: Conceptual picture of inductive fine tuning scheme. Taken from [14].

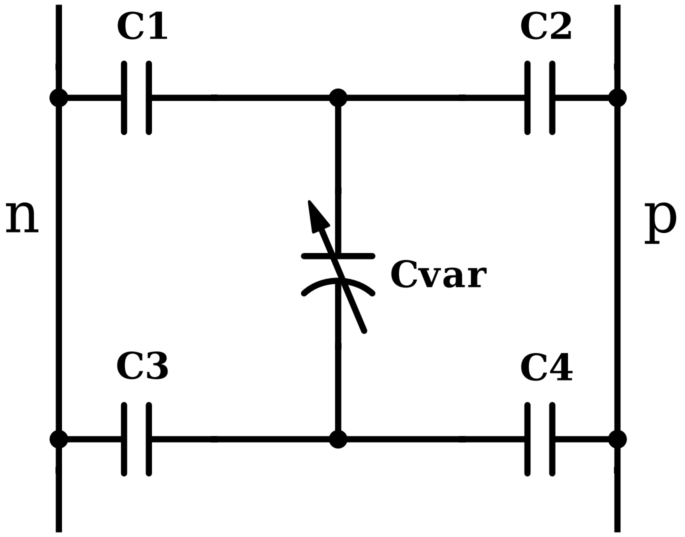

Figure 5.13: Schematic illustrating capacitative voltage division.

5.2.8 Transistor-based fine-tuning [4]

Another way of achieving fine-tuning is to implement an array of small transistors in parallel with the current source. Figure 5.14 shows an example with three fine-tuning elements. The small transistors in parallel with the current source modulates the total current through the differential pair. This will lead to a small frequency shift due to the detailed physics of the devices. Since the impedance of the even harmonics also is modulated by the small transistors, the Groszkowski effect discussed above will also affect the frequency. If the frequency tuning resulting from the Groszkowski effect can be neglected, the tuning scheme has several advantages. Unlike most of the other tuning techniques described in this thesis, no considerations have to be taken regarding inductive and capacitive parasitics, which greatly simplifies the simulation and layout implementation. The tuning scheme also occupies a very small area, since only a single transistor is needed for each cell. A very large number of cells can be implemented unlike some other tuning techniques. The tuning scheme is also capable of a very high resolution. If the tuning scheme is implemented as depicted in Fig. 5.14, then when the fine tuning transistors all are turned off the gate bias is set to VDD. If the on state is chosen so that the gate bias is $VDD - 20$ mV a very small tuning step can be achieved. If a DAC is used to set the on-voltage bias, the resolution is for practical purposes unlimited. If a longer tuning range is desired the on-state voltage can be lowered. As the transistors leave the active region the impedance change drastically, and the designer have to check that the Groszkowski effect can be still be neglected. If this is not the case the advantage described above disappear. In such case, it is better to implement the tuning scheme with a capacitor or varactor, since the transistor tuning scheme has some drawbacks. A resistor could be inserted between the fine tuning bank and the oscillator to ensure that the impedance in the node stay approximately constant. Not only the frequency but also the amplitude of the output voltage is modulated by the small transistors. Detailed simulations in the ADPLL have to be done to show to what extent this is a problem. Since the tuning scheme is directly based on the transistors the tuning scheme will have some temperature dependence. Noise could potentially also be injected from the tuning transistors. The small transistors should only change the frequency by a small amount and for this reason the transistors are considerably longer than wide. Due to these very small frequency steps, the injected noise only increases the phase noise with much less than one dB.

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[4] This method is not presented in the literature, but is an invention of our own.

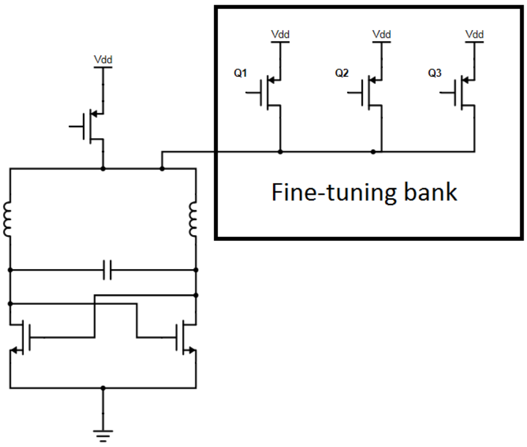

Figure 5.14: The picture shows an implementation of transistor fine tuning, using three transistors Q1-Q3.

5.2.9 Bulk biasing [5]

Another way of using the non-linearity of the transistors is to tune by connecting the bulk to a DAC. The bulk biasing change C_{Bulk}, see Fig. 5.15, leading to a frequency shift. This work was carried out in a fully-depleted SOI process. In an standard process the bulk can still be connected. The bulk couples relatively strongly to the transistor due to the the ultra-thin buried oxide. In the next chapter a DCO using bulk biasing for fine-tuning is implemented. In Fig. 6.21 it can be seen that a wide fine tuning range can be achieved. It should also be noted that that the bulk can be biased up to 2 V. In a standard non-depleted process the bulk bias is highly limited, and the coupling to the transistor is weaker. Thus, a shorter tuning range is expected for a non-depleted process.

An issue with this method is that any amplitude noise on the DAC output will be directly translated to phase noise. Further, the DAC will of course consume power, increasing the overall power consumption.

5.2.10 Dithering

Dithering is not a method that is implemented in the DCO directly, but rather in the ADPLL to improve resolution [19]. A $\Sigma\Delta$ modulator is used to turn on and off, or *dither*, the LSB in the control word at a much higher frequency than the reference frequency. The oscillator will then "see" an average capacitance that is in-between the two capacitances when the LSB is 0 and 1, and by varying the duty cycle of the dithering, the capacitance can be shifted more towards the 1 or the 0 state. Thus, a higher resolution than usual can be achieved since more steps are introduced. For instance, in [19], the resolution was improved from 23 kHz to 3 kHz.

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[5] This method is not presented in the literature either, but is also an invention of our own.

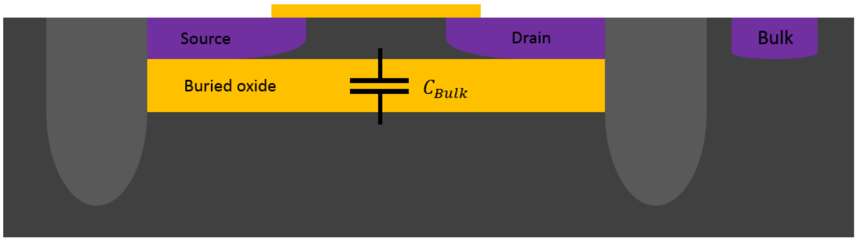

Source
Drain
Bulk
Buried oxide
C_{Bulk}

Figure 5.15: Cross-section of a fully-depleted SOI transistor.

The drawbacks with dithering is that the DCO will consume more power due to the modulator and that the modulator will generate spurs in the output spectrum, since it will cause a periodic frequency modulation [19].

Chapter 6

Proposed DCO

In this thesis, we propose two DCOs. Both use the same oscillator core, with identical cross-coupled transistors, bias transistor, inductor, load and coarse and mid bank, but uses different fine-tuning techniques. The first one utilizes a combination of transformer-coupled tuning and current-modulation to achieve a very high resolution, which we will refer to as current-modulating DCO (CM-DCO) and is shown in Fig. 6.1. The second one is based on bulk biasing the cross-coupled transistor pair with a DAC to achieve high resolution, which we will refer to as DAC-DCO and is shown in Fig. 6.2.

6.1 Inductor

The inductor with width W_{ind}=18.4 µm were chosen for the oscillator. In order to facilitate all the coarse tuning banks, the length of the legs had to be L_{legs}=60 µm. It is hard to estimate the Q value of the inductor since the coarse bank is distributed and different Q values are seen from different points. If the average from Fig. 4.4 is chosen as an estimate, then the Q value 18 is found.

6.2 Biasing, cross-coupled transistor pair and load

The biasing is done using a PMOS transistor, due to the improved noise performance owing to less flicker noise compared with NMOS transistors [5]. The dimensions of the transistor are W/L = 500 µm / 120 nm and is biased at 250 mV. These values were chosen for optimal noise performance and resulted in a DC current of 17.7 mA.

The cross-coupled transistors pair are NMOS transistors with dimensions W/L = 25 µm / 20 nm. Even though PMOS would result in better phase noise performance, the higher speed of NMOS transistors are required to sustain oscillation without using too large transistors, which would add a large parasitic capacitance.

Each side of the oscillator was loaded by a 40 fF capacitor in parallel with a 1 kΩ resistor.

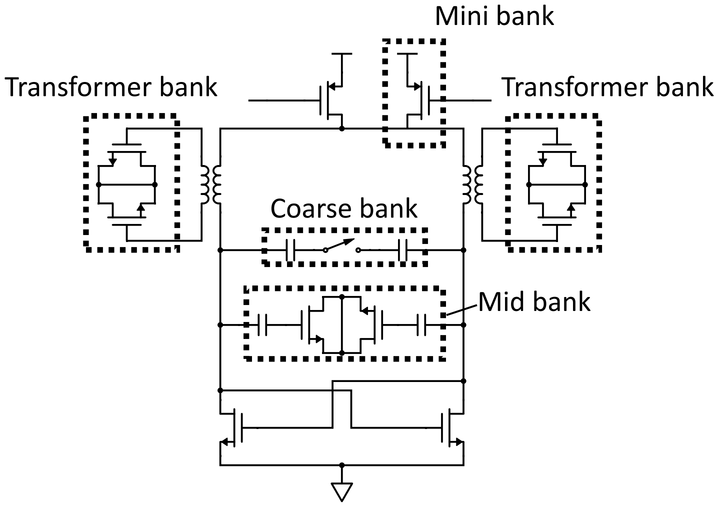

Mini bank
Transformer bank
Transformer bank
Coarse bank
Mid bank

Figure 6.1: Schematic of the proposed CM-DCO.

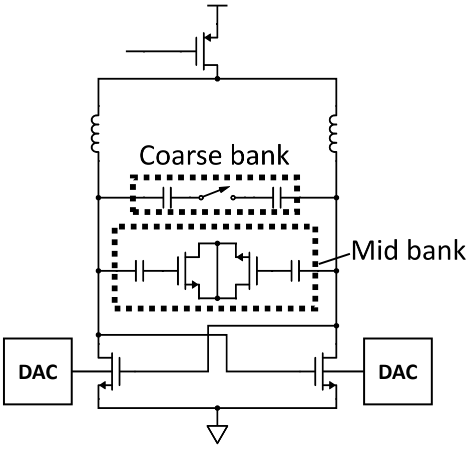

Coarse bank
Mid bank
DAC
DAC

Figure 6.2: Schematic of the proposed DAC-DCO.

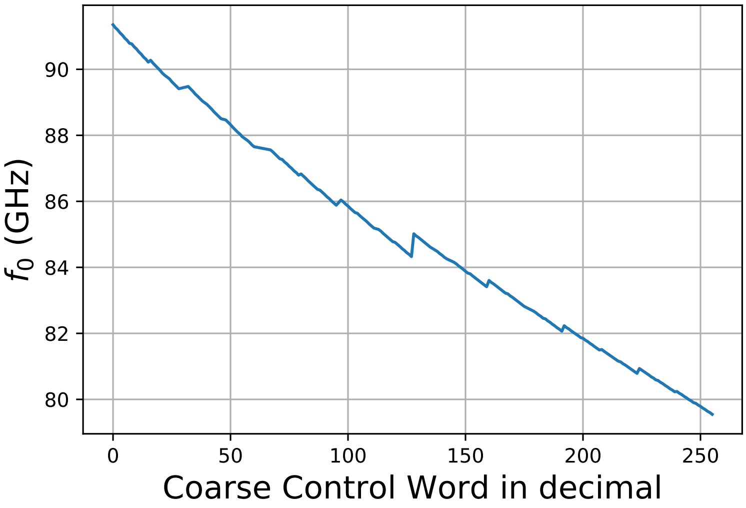


Figure 6.3: Plot showing oscillation frequency versus coarse control word.

6.3 Coarse- and mid-tuning

The coarse bank is implemented as a 6-bit binary-weighted switched capacitor bank, connected directly to the oscillator core. Each cell is implemented as shown in Fig. 5.1, except that all transistors are NMOS (Q3 and Q4 are therefore connected to an inverted control signal) and that the bulk of the large center-transistor is pulled to VDD to reduce R_{on}, as suggested in [33]. The widths of $Q1$ and $Q2$, and $Q3$ and $Q4$ are 4 µm and 300 nm, respectively, for every cell. The width of $Q3$ varies from 50 µm for the largest cell to 15 µm for the smallest one. All transistors have a length of 20 nm.

The middle bank is implemented as a 2-bit binary-weighted varactor bank, also connected directly to the oscillator core. Thus, the coarse and middle bank can together effectively be seen as a 8-bit binary-weighted bank. The varactor cells are implemented as shown in Fig. 5.3. The fixed capacitors are minimum sized (3 µm x 3 µm) MOM-capacitors, the bias resistors are 3 kΩ NWELL-resistors, and the bias is set to VDD. The dimensions of the transistors are $W/L = 1.2$ µm / 0.35 µm and $W/L = 1.0$ µm / 0.1 µm for the larger and smaller cell, respectively.

Coarse-tuning will henceforth be used to describe the tuning done by both the coarse and the middle bank.

Fig. 6.3 shows oscillation frequency versus the coarse control word (CCW) for all 256 steps (8 bits) in the coarse-tuning. The frequency spans from 91.35 GHz to 79.47 GHz, resulting in a center frequency of 85.41 GHz and a total tuning range of 13.9 %. The resolution of the coarse tuning is 90.9 MHz or better for a typical process variation.

The Q varies between 38.6 and 10.2 when all cells are turned off and turned

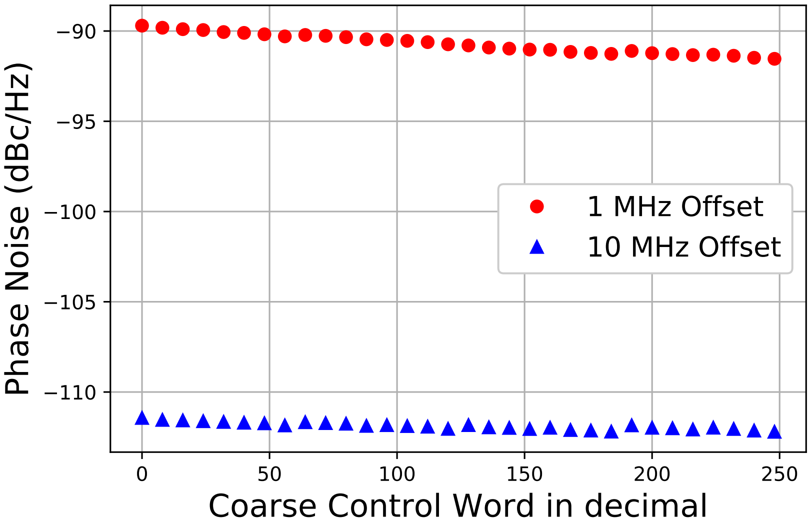


Figure 6.4: Plot showing phase noise at 1 MHz and 10 MHz offset versus coarse control word.

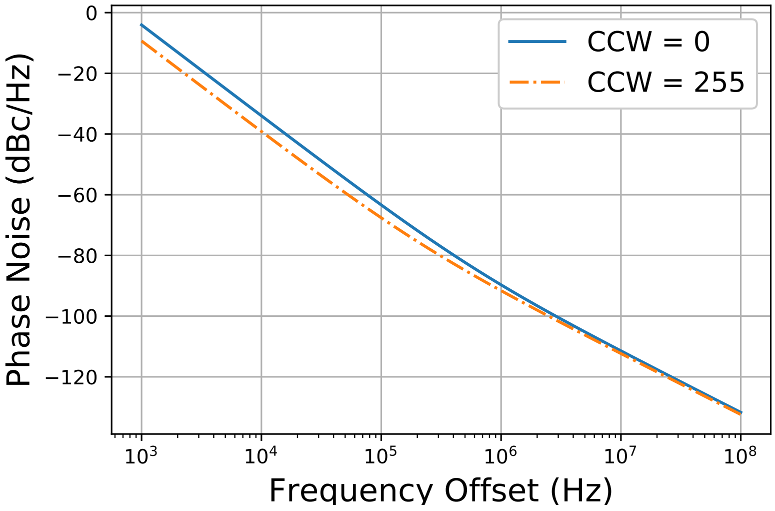
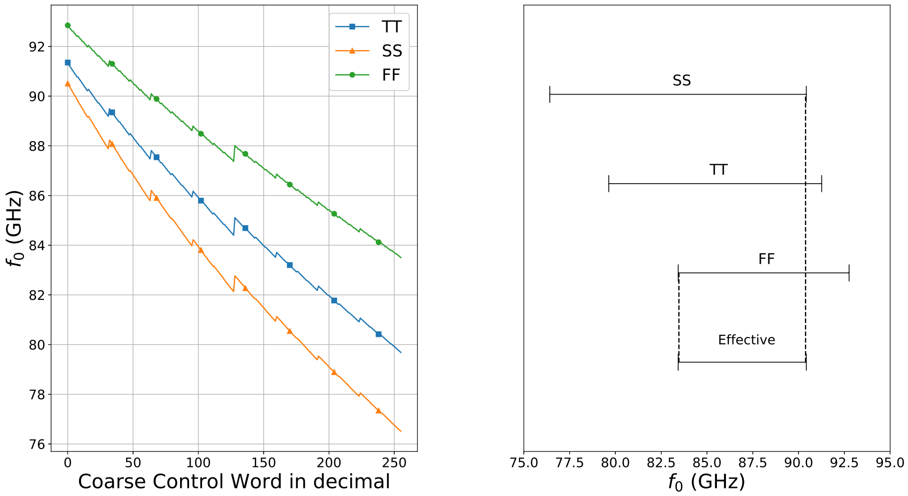


Figure 6.5: Phase noise swept from 1 kHz to 100 MHz at CCW = 0 and CCW = 255.



(a) **(b)**

Figure 6.6: (a) Plot showing how process variations affect the coarse tuning. (b) Tuning range in various process corners, and the effective tuning range.

on, respectively. C_{off} of the bank is 44.4 fF, while C_{on} is 83.8 fF, resulting in a C_{on}/C_{off} ratio of 1.9.

Fig. 6.4 shows the phase noise at 1 MHz and 10 MHz offset versus CCW. It varies from -89.7 dBc/Hz and -111.4 dBc/Hz to -91.2 dBc/Hz and -112.2 dBc/Hz at 1 MHz and 10 MHz offset, respectively. A sweep of the phase noise from 1 kHz to 100 MHz at CCW = 0 and CCW = 255 is shown in Fig. 6.5. The $\Delta\omega_{1/f^3}$ corner is situated at around 500 kHz and 250 kHz for CCW = 0 and CCW = 255, respectively.

In Fig. 6.6a, the effect of process variations on the frequency tuning. The simulated corners were *typical-typical* (TT), *slow-slow* (SS) and *fast-fast* (FF). In Fig. 6.6b, the tuning range for the various corners are shown, along with an effective tuning range, i.e. the tuning range that can be guaranteed no matter what process variation occur. The effective tuning range is found to be from 83.3 GHz to 90.5 GHz.

While the coarse tuning is rather sensitive to process variations, it is very robust regarding temperature variations. In Fig. 6.7, the coarse tuning is shown at temperatures -30°C, 27°C, 90°C and 120°C. The oscillation frequency is reduced by about 500 MHz when going from the coldest to the warmest temperature and the total tuning range is virtually unaffected.

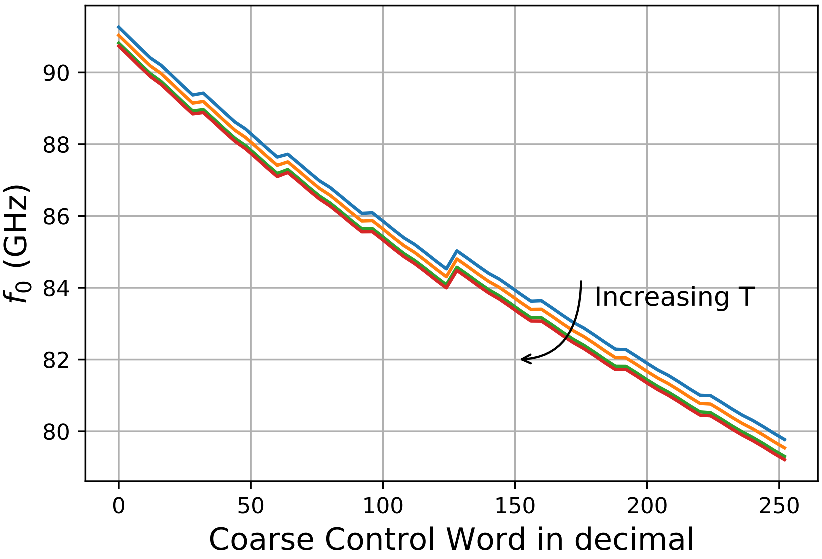


Figure 6.7: Plot showing the coarse tuning at various temperatures.

6.4 Proposed oscillator 1: Current-modulating DCO

Due to the large inductance stemming from the long legs of the inductor, the off-capacitance must be minimized to achieve a wide tuning range. Therefore, the fine-tuning must be done using techniques that do not capacitively load the oscillator core too much.

In this proposed oscillator, two banks are implemented for the fine-tuning; a transformer-coupled bank where the tuning cells are connected to a secondary inductor which is weakly coupled to the primary inductor, which will be referred to as the transformer bank, and a bias current-modulating, transistor-based tuning, as suggested in section 5.2.8, which will be referred to as the mini bank. Both of these banks have negligible effect on the off-capacitance. The off-capacitance from the transformer bank is attenuated by a factor well below unity and the mini bank is connected at a common-mode ground, thus its capacitance will not be seen by the fundamental tone.

6.4.1 Transformer Bank

The transformer bank (TB) is implemented as a 32-bit unary-weighted varactor bank, with 32 cells on each side of the primary inductor, as seen in Fig. 6.8a. The cells are similar to the ones used in the middle bank, but does not have any fixed MOM-capacitors, see Fig. 6.8b, since noise is much smaller problem in this bank than in the middle bank due to the attenuation factor described in section 5.2.3. No bias is used in these cells, thus the resistors can also be removed. Instead, the

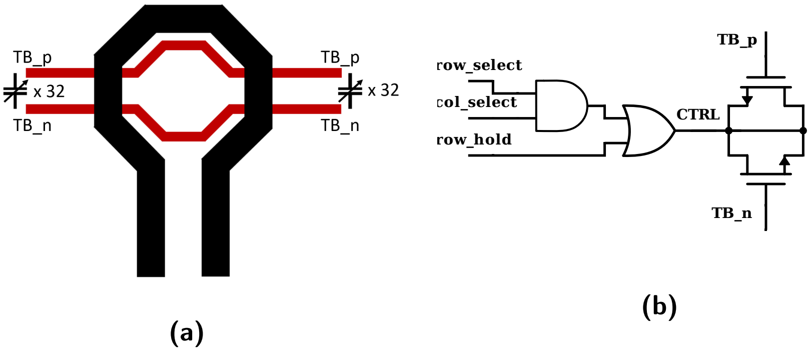

TB_p
x 32
TB_n
TB_p
x 32
TB_n
(a)
row_select
col_select
row_hold
CTRL
TB_p
TB_n
(b)

Figure 6.8: (a) Overview of TB, showing how the secondary inductor is coupled to the primary. (b) Individual cell of transformer bank, including control logic.

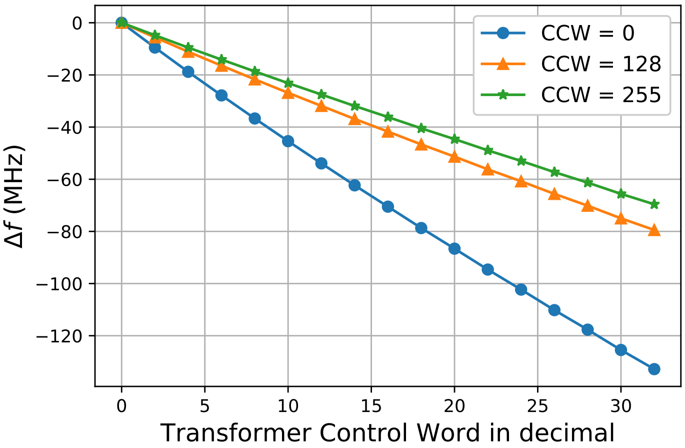


Figure 6.9: Plot showing tuning of transformer bank versus control word for various CCWs.

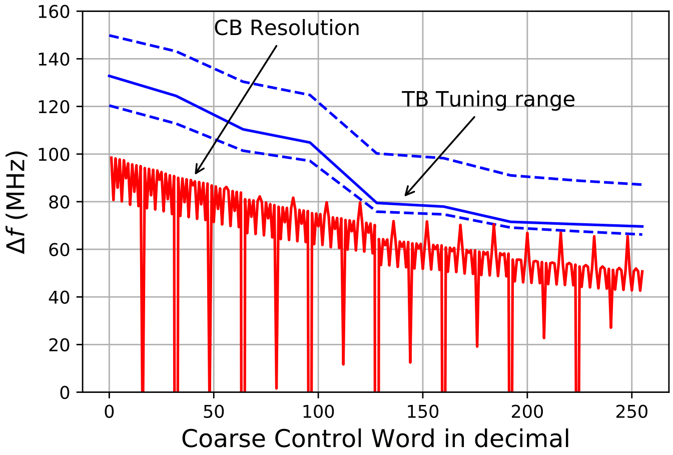


Figure 6.10: Plot showing tuning range of transformer bank and frequency change of each step in the coarse tuning versus coarse tuning word. The lower dashed line is the *slow-slow* corner and the upper is the *fast-fast* corner.

legs of the secondary inductor L_s are pulled to VDD to ensure proper operation of the varactor cells. Each cell is controlled by a digital control circuit, as seen in Fig. 6.8b. $CTRL$ will go high when either row_select and col_select go high or when row_hold goes high. The capacitance of the bank can be changed from 21.8 fF to 38.5 fF, resulting in a C_{on}/C_{off} ratio of around 1.77 and a ΔC of 16.7 fF.

The frequency tuning of the bank is shown in Fig. 6.9 for various CCW, i.e. various oscillation frequencies. The bank achieves a highly linear tuning with a frequency resolution of 5 MHz or better for a typical process. The total tuning range of this bank varies between 132 MHz and 70 MHz, depending on which coarse control word is used. This corresponds to a capacitance change in the oscillator core of roughly 400 aF, meaning that the attenuation factor is 0.024.

Fig. 6.10 shows the total tuning range, including process variations, of this bank versus the coarse control word. Also plotted is the frequency change of every step in the coarse tuning in the *slow-slow* corner, which causes the largest frequency steps. While this corner causes the largest steps in the coarse tuning, it causes the smallest tuning range of the transformer bank. Despite this, there is enough overlap between them that there will be no frequency gaps, even in the worst case.

Fig. 6.11 shows how the tuning of the transformer bank varies with temperature. As shown in the plot, increasing temperature results in a slightly smaller tuning range.

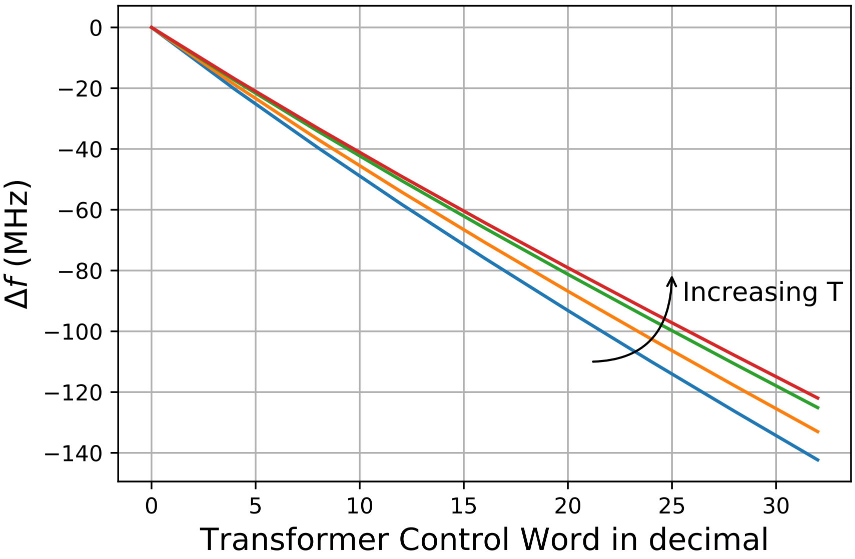


Figure 6.11: Plot showing frequency tuning of transformer bank at temperatures -30°, 27°, 90° and 120°.

6.4.2 Mini Bank

The "mini" tuning bank (MB) is implemented with the transistor-based tuning scheme described in section 5.2.8. The proposed fine tuning bank is 128-bit unary-weighted and uses 128 fine-tuning cells. The current changes from 17.67 mA to 17.72 mA, which correspond to only to a change of 50 µA, or 0.2 percent. To achieve a very high frequency resolution, each individual transistor needs to have a very low on-current. For this reason, the length has to be considerably longer than the width. The width of the transistors were chosen to 80 nm while the length were set to 1 µm. The smallest allowed width of the transistor is often somewhat longer 3-4 then the process node. When the width of the transistor increase the length must also increase by the same factor, in order to hold the current constant. This increase the area of the fine tuning bank. The mini tuning bank and all the addressing wires in the proposed oscillator occupies 55 µm × 5 µm. The addressing wires occupied approximately half of this area. Simulation also showed that the injected noise from the tuning bank was less then 0.2 dB.

Figure 6.12 shows the achieved tuning range for different gate bias voltage in the on-state of the bank. The on-bias voltage of the transistors were set to 280 mV in the proposed oscillator. This ensures a substantial overlap between the resolution of the transformer bank and tuning range of the mini bank, as seen in Fig. 6.14. From Fig. 6.14, it is clear that the crudest resolution is when the CCW equals 0. At CCW = 0 the frequency resolution is approximately 55 kHz and at CCW = 255 the resolution is approximately 40 kHz. Fig. 6.13 shows the

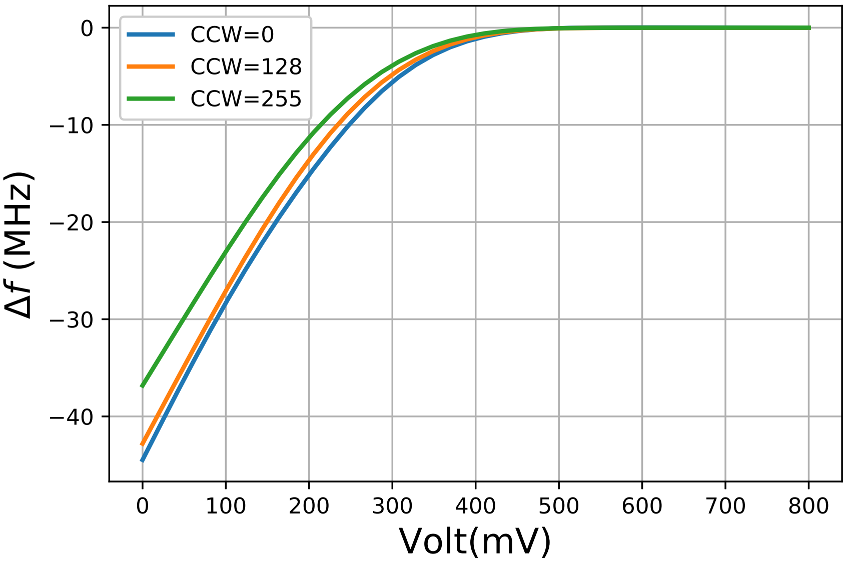


Figure 6.12: The plot shows the achieved frequency tuning range of the mini bank for different gate bias voltage at different CCW.

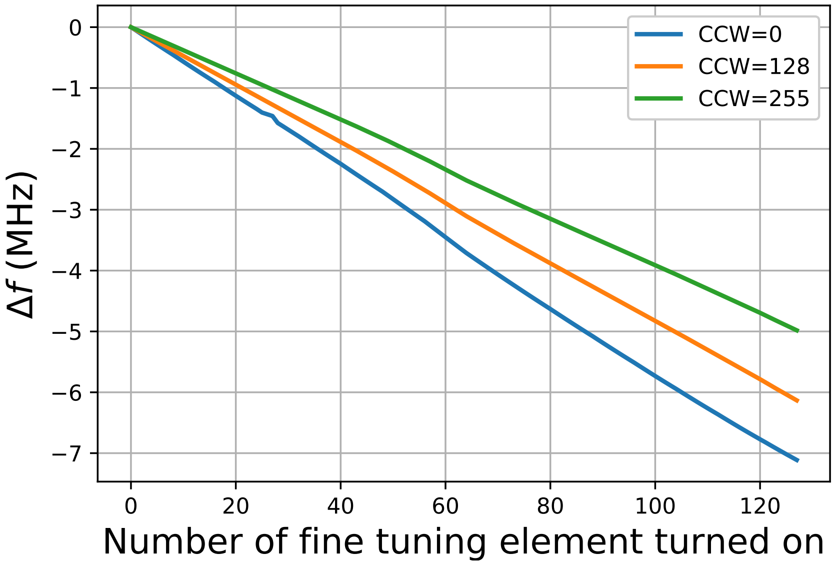


Figure 6.13: Plot showing the tuning range as increasing number of transistors are turned on.

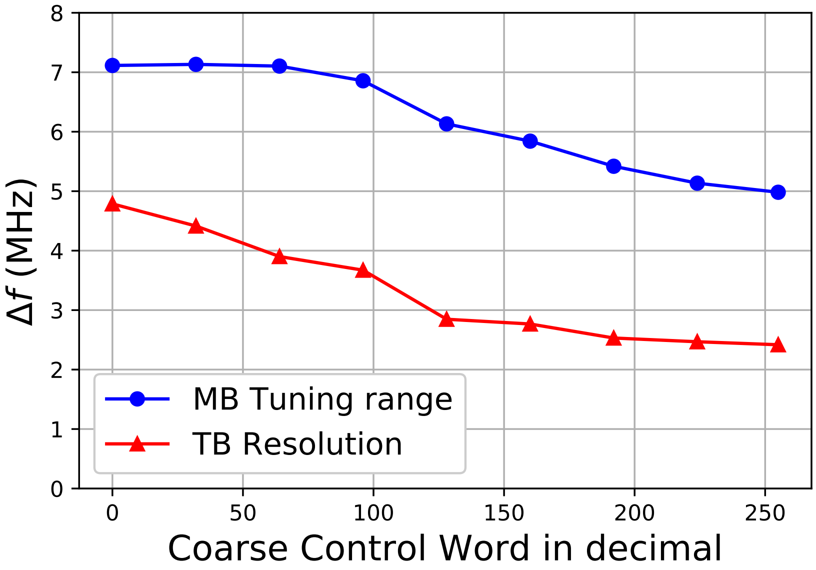


Figure 6.14: Plot showing tuning range of the mini bank and frequency resolution of the transformer bank versus coarse tuning word.

frequency tuning for different number of transistors turned on at different CCW. From the figure, it can be seen that the tuning scheme is very linear.

Since an active device is directly involved in the frequency tuning, the tuning scheme is expected to have a relatively strong temperature dependence, which can be seen in Fig. 6.15 and Fig. 6.16. The difference in frequency tuning between 27°C and 90°C is small, and in Fig. 6.15 and Fig. 6.16 the two curves overlap. It is very interesting that the curves cross each other at approximately 200 mV.

When the transistors turn on and off, the impedance in the current source node changes. As a consequence, some of the frequency tuning stems from the Groszkowski effect, which is unwanted for reasons discussed in chapter 5. By comparing the tuning range of the bank with the tuning range achieved when using an ideal current source, whose impedance is constant and will thus not contribute to the Groszkowski effect, the tuning that comes from the DC shift can be isolated. This is plotted in Fig. 6.17. From the comparison, it can be seen that about 80-90 percent of the tuning comes directly from the change in DC.

If the designer wants total control of the frequency tuning a resistor can be connected in series with the fine tuning transistors. The small current trough the fine bank makes it possible to choose a large resistor without a significant voltage drop. If the resistor is large enough, then the impedance in the node stays almost constant when the transistors are turned on and off. Fig 6.18 shows how the frequency corresponds to DC shift with a 1 kΩ resistor inserted in series. The frequency shift can then almost entirely be attributed to the DC change.

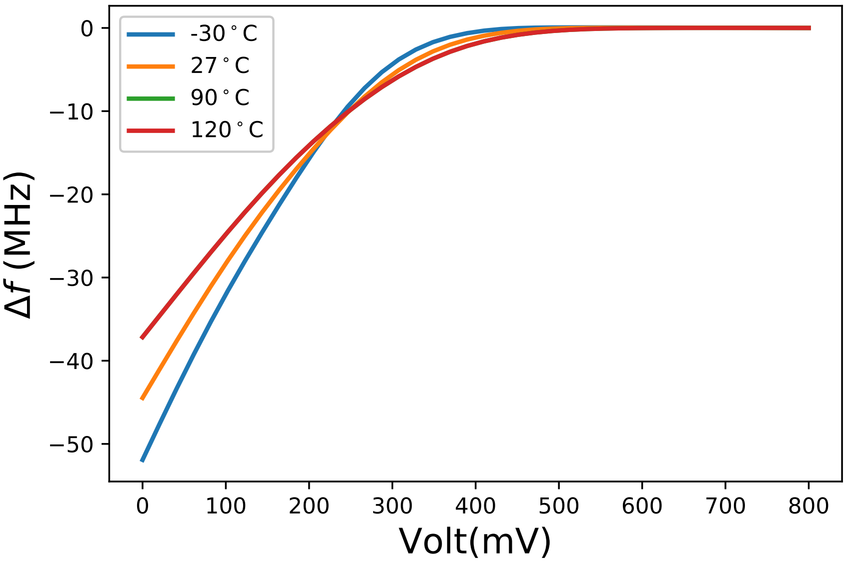


Figure 6.15: The plot shows how the frequency change with gate bias voltage of the fine tuning transistors for varying temperature, at CCW=0. The yellow and green curves overlap.

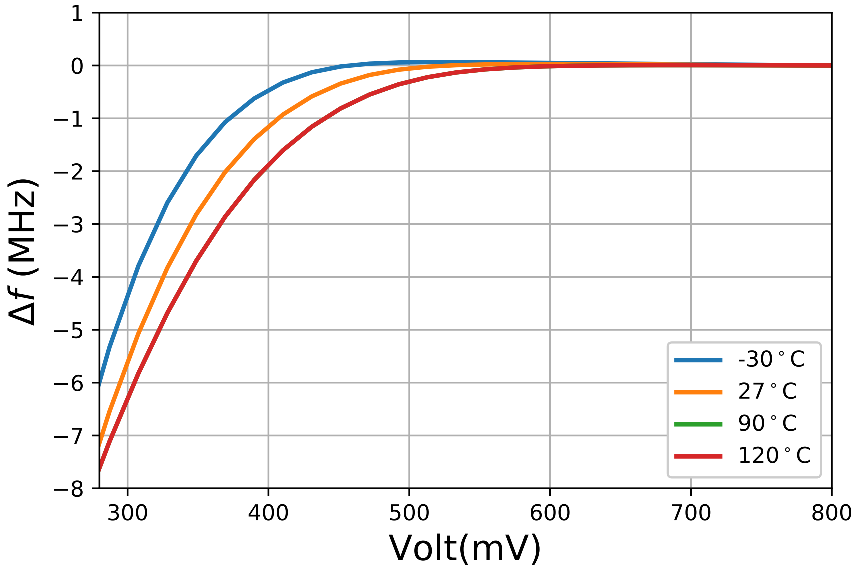


Figure 6.16: The plot shows a zoom of 6.15.

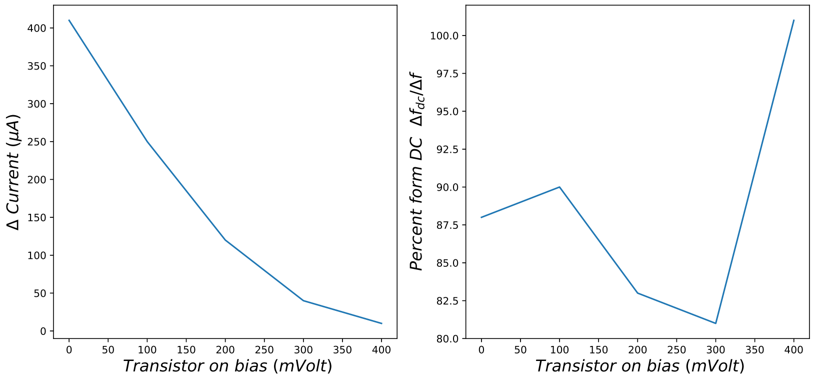


Figure 6.17: Plot showing tuning range of the mini bank and frequency resolution of the transformer bank versus coarse tuning word.

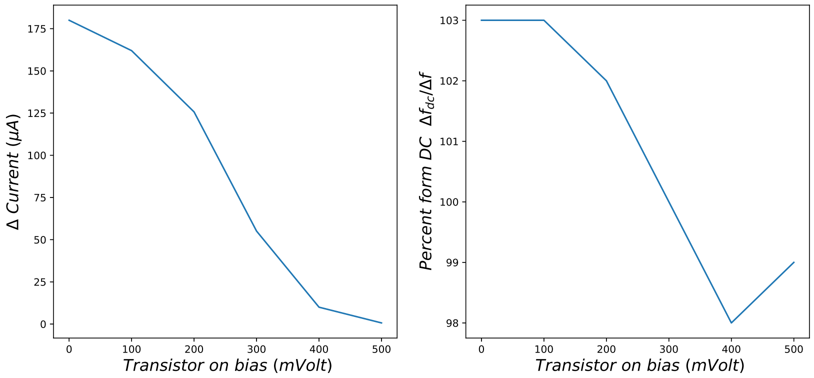


Figure 6.18: Plot showing tuning range of the mini bank and frequency resolution of the transformer bank versus coarse tuning word, with 1 $k\Omega$ resistor.

The fine tuning bank can also be divided in two, a larger mini bank and a smaller mini bank, in order to achieve an improved resolution. This can be done without any change to the layout, it is enough to change the on-bias of half of the transistors. The on-gate bias on the larger mini bank was set to 200 mV. In fig 6.19a it can be seen that this ensure a substantial overlap between the transformer bank and this bank. The gate bias voltage on the smaller mini bank was set to 410

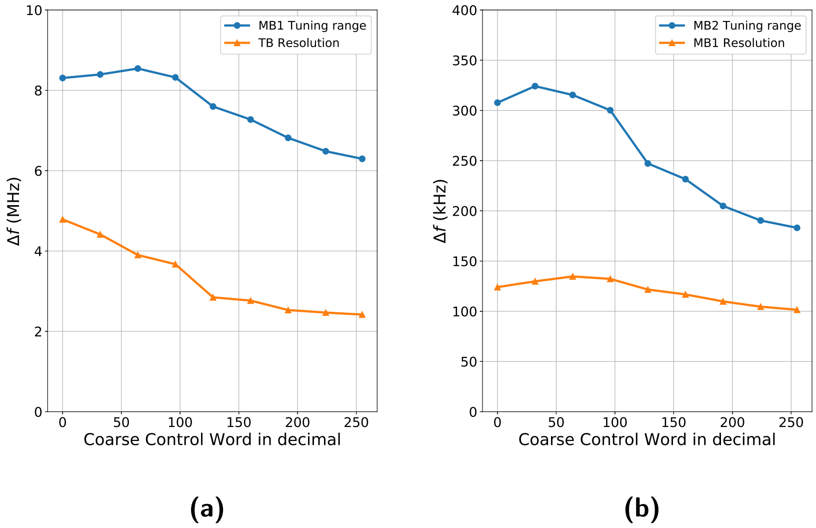


Figure 6.19: (a) Resolution of the transformer bank (TB) and tuning range of MB1 versus coarse control word. (b) Resolution of the larger mini bank (MB1) and tuning range of the smaller mini bank (MB2) versus coarse control word.

mV. Fig. 6.19b shows the overlap between the smaller and the larger mini bank. This gives a worst case resolution of approximately 6 kHz.

If the designer needs an even smaller resolution the number of fine-tuning transistor could be increased and a "super mini bank" could be implemented. Simulations showed that if the V_{GS} was set to 30 mV a resolution of 2 Hz was achieved.

The plot 6.20 shows frequency tuning with current modulation using an ideal current source. A large frequency tuning can be achieved that cover the 100 MHz interval. The side effect is that the the change in current is rather substantial, 10-20 %. This might make the oscillator leave the sweet spot where the phase noise performance is optimal. If the ADPLL is used for modulation, i.e sigma delta. The amplitude modulation could potential give rise to spurs.

6.5 Proposed oscillator 2: DAC-DCO

As mentioned earlier, the second proposed oscillator utilizes the same oscillator core as the first oscillator, but uses bulk biasing for the fine tuning, which does not load the oscillator core.

Since an actual DAC has not been implemented, the following simulations have been done using an ideal voltage source as the DAC (except for the phase noise simulation), which obviously will result in better performance than if an actual DAC were used.

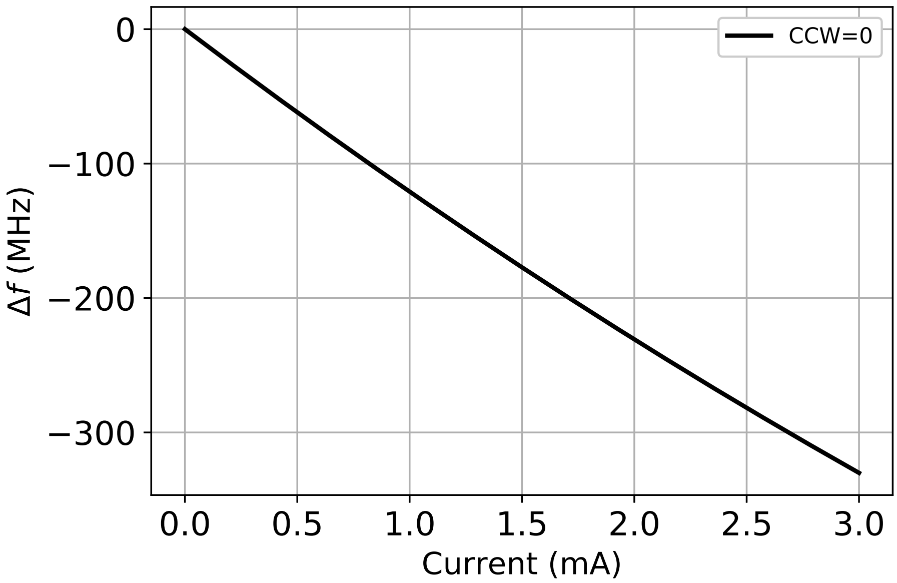


Figure 6.20: Shows frequency tuning over a wide range using an ideal current source.

Fig. 6.21 shows the tuning range versus bulk bias at CCWs 0, 128 and 255. As seen in the figure, the tuning is extremely linear and covers the frequency resolution of the coarse tuning by a great margin, thus preventing any frequency gaps. For a resolution of 100 kHz or better, the DAC must have a resolution of 200 μV. This corresponds to 13 bits, assuming that the whole range of 800 mV should be covered.

Fig. 6.22a and Fig. 6.22b shows how the tuning at CCW = 0 varies with process variations and temperature variations, respectively. Simulated corners were *typical-typical* (TT), *slow-slow* (SS) and *fast-fast* (FF) and simulated temperatures were -30°C, 27°C, 90°C and 120°C. As seen in the plots, the tuning scheme is very robust towards variations. It should be noted that these simulations did not include variations in the DAC.

Fig. 6.23 shows phase noise at 1 MHz offset at CCW = 0 versus spectral noise density, applied as white noise at the bulk bias. At around 40 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, the phase noise has increased by just above 1 dB and at around 70 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, the phase noise has worsened by an unacceptable 3 dB.

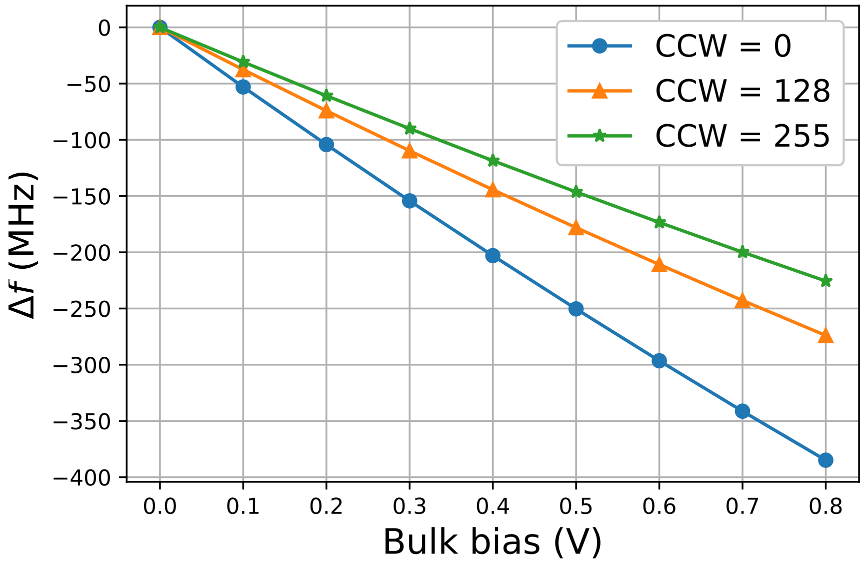
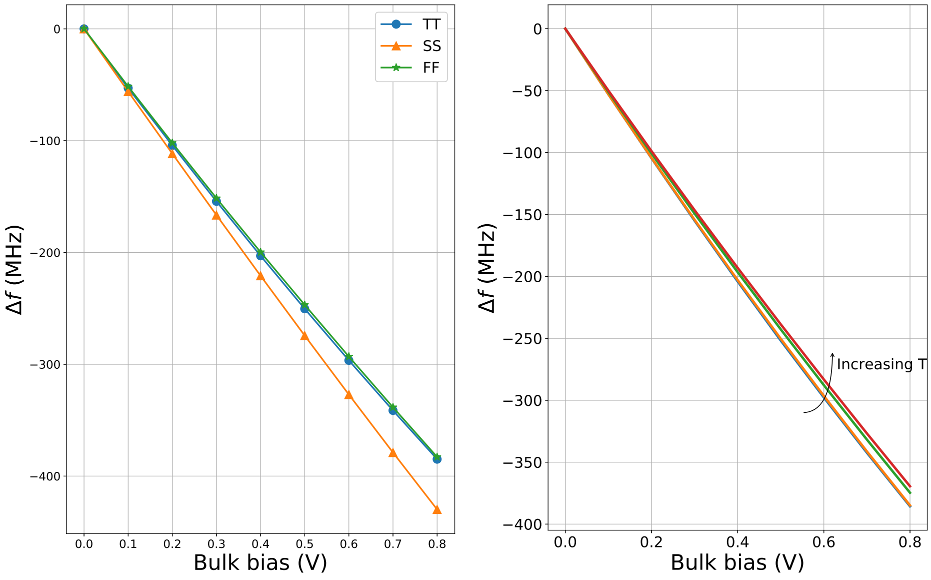


Figure 6.21: Plot showing tuning range versus bulk bias for various CCW.



(a) **(b)**

Figure 6.22: Plots showing how process and temperature variations affect the bulk tuning.

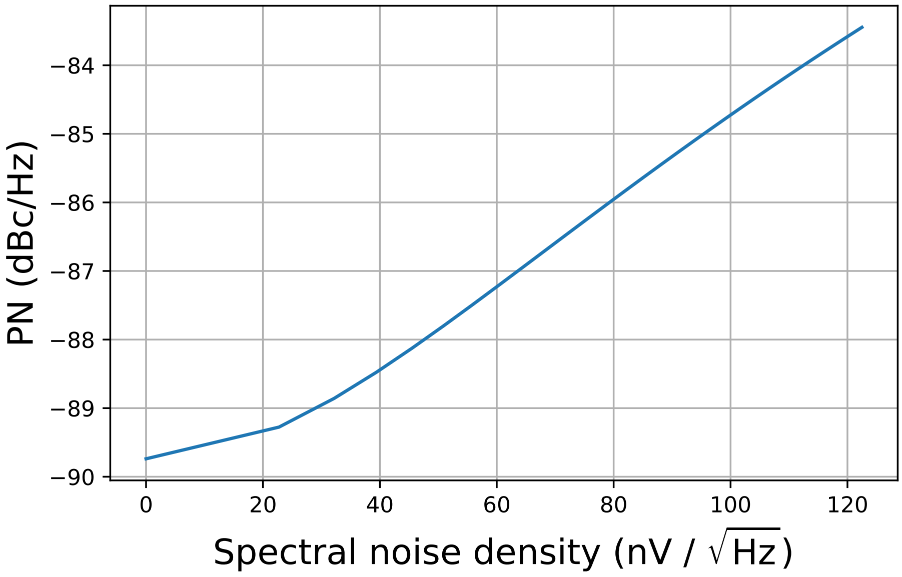


Figure 6.23: Plot showing phase noise versus spectral noise density.

Chapter 7

Discussion and Conclusions

Table 7.1 compares the first proposed oscillator to DCOs operating at mm-wave frequencies presented in the literature. The second proposed oscillator is left out of this comparison, since it would not be a fair comparison without an implemented DAC.

7.1 Discussion

The simulations have shown that a +80 GHz oscillator can be implemented with a Figure-of-Merit of almost -180 dBc/Hz and >10 % tuning range, in fully-depleted SOI CMOS. These frequencies have traditionally been dominated by silicon germanium technologies. Below follows a comparison with other presented mm-wave DCOs, a brief discussion about the coarse- and fine-tuning and some possible future work.

7.1.1 Coarse-tuning

The coarse tuning does not manage to reach the targeted 20% tuning range. To reach this tuning range with conventional capacitance banks would require a significant drop in Q, which would yield a much worse phase noise performance. Still, the proposed oscillators have the third highest reported tuning range at mm-wave frequencies, as shown in Table 7.1. It should also be noted that two oscillators with higher tuning range operates at significantly lower frequencies.

As mentioned earlier, the Q factor for the coarse tuning has a minimum value of 10.2, while the inductor has a Q factor of roughly 18. Thus, the total Q is mainly set by the capacitance bank. Therefore, inductively tuned coarse tuning can be used in future work to achieve wider tuning, without significantly worsening the performance. However, this will make the transformer bank very difficult to implement, since the resolution and tuning of this bank is dependent on the inductance of the primary inductor.

The use of transmission lines for the coarse tuning can also be investigated in the future. As mentioned earlier, a Q factor of 12 or higher is achieved in [14], using a 65 nm CMOS process. A slightly higher Q would likely be possible to achieve in a 22 nm FD-SOI process.

Table 7.1: Performance summary and comparison of mm-wave DCOs.

	This work (CM-DCO)	[23]	[14] (Induct.-based)	[14] (Transf.-based)	[34]	[28]	[32]
f_0 (GHz)	79.5 - 91.4	54.8 - 63.2	56.2 - 62.2	55.8 - 61.6	51.3 - 53.3	48.1 - 61.3	74.6 - 83.6
Tuning range (%)	13.9	14.2	10	9.75	4	24.1	11.4
Resolution (Hz)	55k	4 / 300k	160k	2.5M	1.8M	39k	370k
PN (dBc/Hz)	-111.4	-90.5	-93	-94	-116	-88.8	-114.9
Offset (MHz)	10	1	1	1	10	1	10
Power (mW)	14.1	18	12	14	2.34	10	15.6
FoM (dBc/Hz)	-178.5	-173.4	-177.9	-177.9	-187.2	-173.6	-180.9
$\mathrm{FoM_T}$ (dBc/Hz)	-181.4	-176.6	-177.9	-177.9	-179.2	-182	-182.1
$\mathrm{FoM_{DT}}$ (dBc/Hz)	-186.4	-186.4	-181.3	-179.3	-179.4	-187.3	-185.3
VDD (V)	0.8	1.2	1.2	1.2	1.2	1.0	N/A
Area (mm^2)	0.01	0.10	0.16	0.16	0.09	0.032	0.10
Process	FD-SOI 22nm	CMOS 65nm	CMOS 90nm	CMOS 90nm	CMOS 90nm	CMOS 65nm	CMOS 65nm

7.1.2 Fine-tuning

Only four of the fine-tuning schemes discussed in chapter 5 appears to be able to cover the 100 MHz gap without severely capacitively loading the core; the bulk biasing, the transformer-based tuning, the inductor-based tuning and capacitive degeneration.

The capacitive degeneration has issues with a frequency tuning that decreases with increasing frequency, which is opposite to the behavior of the other banks, and reduction in transconductance of the differential pair, as discussed in section 5.2.1. The reduction in transconductance was the most severe problem in our case, making it impossible to sustain oscillation at certain CCWs. The inductor-based tuning suffers from high non-linearity and, given our small inductor, could not be implemented with enough frequency steps. Therefore, these two methods had to be dismissed. This left the transformer-based and the bulk biasing-based schemes as the only viable options.

An attempt was made to combine the bulk bias fine-tuning scheme with the transistor fine-tuning scheme. Simulations showed that a change in bulk bias had a big impact on the transistor fine-tuning scheme. Thus, the two tuning schemes were not compatible. It should also be noted that mismatch between the transistor in the differential pair can to some extent be retributed with appropriate bulk bias. This possibility disappears if the bulk is used for fine tuning. This left only two viable options: Either use a combination of the transformer-based and the transistor-based tuning or use the bulk bias method to cover the whole frequency tuning up to 100 MHz.

In [14] it was reported that the Q value of the inductor dropped with less than 0.5 when the transformer was implemented. Our own simulations showed similar results where no real difference was found between the inductor with and without the transformer. In our work, there is a small difference regarding the way the transformer was implemented. In [14] the transformer was implemented with a large loop going up over the current source. The area of such a loop provided a large coupling factor. In our DCO, the transformer was instead implemented according to figure 6.9. This allowed for a smaller area, hence a smaller coupling factor, with maintained symmetry. From design time perspective this was highly preferable, since the area of the loop inside the inductor can be changed instead of the many fine tuning banks.

The transistor fine-tuning scheme has many merits. It is with a suitably chosen resistor entirely DC dependent, which is a substantial advantage. The otherwise problematic fine-tuning bank becomes very easy to implement. Another advantage is that the fine-tuning bank can be implemented far away for the oscillator. This can also substantially simplify the addressing of the fine bank. The transistor-based fine-tuning scheme also allows for the implementation of very large fine-tuning banks, with high resolution. Simulation also showed that many of the feared disadvantaged discussed in chapter 5 do not deteriorate the oscillators performance. The noise injected for the fine bank was below 0.2 dB. The change in amplitude was simulated to be approximately 0.2 percent. Simulations in a complete ADPLL have to show if the amplitude modulation affect the overall ADPLL performance. If the circuit operate at room temperature or somewhat higher due to heating from circuit elements it is rather temperature independent, between 27 and 90 degrees. If the circuit operates at more extreme temperatures, the circuit have a rather pronounced and mysterious temperature behavior. A temperature calibration circuit could compensate for the temperature variations seen in chapter 6. If the addressing is done intelligently a fine bank with 512 elements could probably be implemented within 40 µ× 40 µm. This would result in a resolution of approximately 15 kHz, where all the elements would be unary coded. This would be enough to implement an ADPLL with completely negligible quantization noise from the DCO, as seen in Fig. 2.5.

7.1.3 Future Work

A literature study of the trade off between noise and power consumption of DAC should be conducted. The DAC should be implemented and the performance of the the second proposed oscillator should be re-evaluated.

Another way of achieving very good resolution is to use the Groszkowski-based tuning scheme, as seen in Fig. 7.1, which could also be combined with the bulk bias scheme. The Groszkowski fine-tuning scheme is not as temperature-dependent as the transistor-based tuning, and do not give rise to amplitude modulation. This tuning scheme would however be very hard to implement, because of the high frequency, $2\omega_0$.

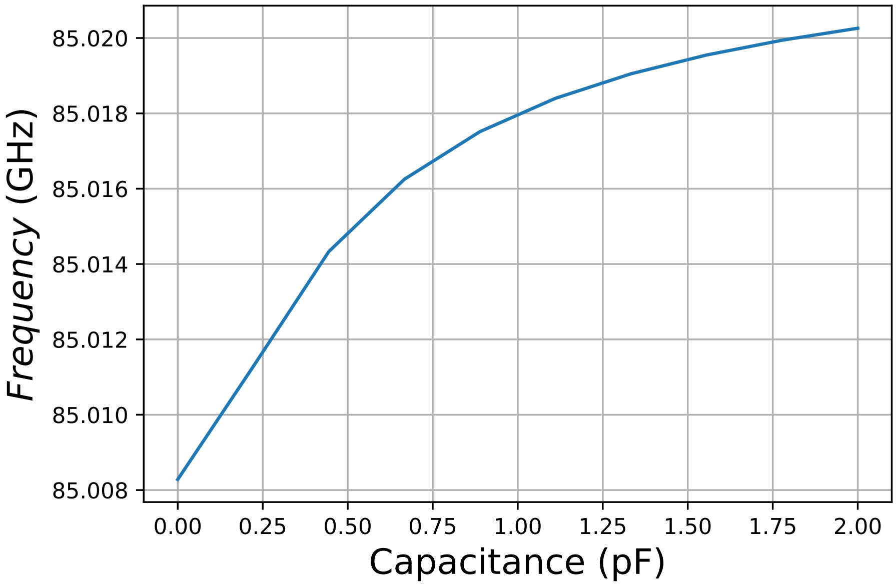


Figure 7.1: Prospect of fine tuning using Groszkowski fine tuning. The capacitance used here is ideal.

7.2 Conclusion

In this thesis, we have described several methods to coarse- and fine-tune a digitally controlled oscillator operating at mm-wave frequencies, and discussed their benefits and drawbacks. We have also proposed two 86 GHz DCOs for future mobile communication applications. Both DCOs have the same oscillator core and coarse tuning and achieves a tuning range of 13.9% and a phase noise of -89.7 dBc/Hz and -111.4 dBc/Hz at 1 MHz and 10 MHz offset, respectively. This results in FoM = -178.5 dBc/Hz and $\mathrm{FoM_T}$ = -181.4 dBc/Hz To the authors' knowledge, this is highest reported oscillation frequency for a DCO[1]. Despite this, the DCO performs highly competitively with other state-of-the-art mm-wave DCOs, as seen in Table 7.1.

The first one, the CM-DCO, uses a transformer-based tuning and a unique current-modulating tuning and achieves a resolution of 55 kHz. The current-modulating scheme is implemented as an array of transistors in parallel with the current source which are turned on and off. The scheme has several virtues, including small area, no capacitive or inductive loading of the core, and possibility to alter the tuning range post-manufacture. By changing the tuning voltage, a much finer resolution can easily be achieved. The drawbacks are temperature-dependence and that the scheme modulates the amplitude, although by a small amount for narrow tuning range. The consumed chip area is 0.01 mm^2, significantly smaller than the DCOs reported in table 7.1.

The second one, the DAC-DCO, uses bulk biasing with a DAC of the differential pair. If the DAC can achieve a resolution of 100 µV, a frequency resolution of 50 kHz is possible. Noise simulations showed that if the spectral noise density of the DAC output can be kept below 40 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, the phase noise will only be worsened by 1 dB or less.

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[1] It should be noted that the proposed oscillators only have been simulated and not yet manufactured.

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