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FABRICATION OF TUNNELING FIELD EFFECT TRANSISTORS (TFET'S) AND THE STUDY OF GRAPHENE

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Abstract

After the discovery of graphene in 2004, a single layer of graphite, the assembly of 2D materials became a promising research area in solid state Physics. This thesis explores fabrication of 2D-heterostructures that aim to probe into graphene's electronic structure with the Tunneling Field Effect Transistor (TFET).

In the fabrication process, we used mechanical exfoliation to obtain monolayer graphene and Si-SiO_2 as the substrate and back gate of the device. Then, atomically thin hexagonal boron nitride (hBN) was used as the tunneling barrier because of its insulating properties and smooth surface. Gold (Au) leads were evaporated on the devices so that a tunneling current could be extracted from the sample.

In this thesis, TFET's are suggested as a complementary alternative to Scanning Tunneling Microscopy (STM) in order to study the electronic properties of 2D materials. Our results showed several spectroscopic features of graphene, some of which could be tuned by an applied gate voltage while others could not . Analysis of the gate tunable spectroscopic feature suggests it may be the Dirac point (E_D), a signature of graphene's unique band structure. On the other hand, the spectroscopic feature that is insensitive to gate voltage could be attributed to inelastic tunneling processes i.e. a phonon excitation.

Future research will be able to use these devices under high magnetic fields ($\sim$ 45T) and low temperatures ($\sim$ 25mK). TFET's also open the door to an alternative probing method to study the electronic properties of any 2D-material by simply replacing graphene by the desired sample to be studied.

Popular science. The graphene era: One-atom-thick electronics

The wonder material, as some like to address graphene, has drawn an extensive interest for being the strongest, most flexible and first one-atom-thick structure to be found. The unexpected discovery in 2004 of this structure, made of carbon atoms, laid the groundwork for the broad spectrum of new slim materials yet to come. The combination of graphene with these highly thin materials (2D-materials) allows not only to study graphene's remarkable properties, but also to create novel microscopic devices out of it. Because of its unique nature, graphene is steadily working its way into today's silicon dominated electronic industry.

It was not long ago when transistors made of silicon revolutionized our computers and phones. These small devices, presently of the size of ten to a few nanometers (1 nm = 0.0000000001 meters), are able to act as a switch when a voltage is applied. The larger the number of "electrical switches" the faster our computers or phones will work. The discovery of graphene and its great conducting properties has led scientists to try and integrate it in silicon-based transistors by combining it with other new 2D-materials.

It seems rather fictional to be dealing with atomically thin layers of materials. However, graphene is a material that comes from the very same graphite that our pencils are made of. Imagine a stack of post-its representing bulk graphite; then, each post-it would correspond to precisely one graphene layer. Surprisingly, isolating a thin layer of graphene is as simple as placing scotch tape on top of bulk graphite and peeling away graphene layers as the tape is lifted. In the same way a post-it is placed onto a paper, once isolated, graphene can be placed onto a substrate and then observed through a microscope. This entire process is called exfoliation and it is an important part of this thesis, because it can be repeated with a plethora of other materials to create unique 2D-material devices.

The work in this project shows how one graphene layer, sandwiched between a silicon substrate and a thin insulating material (e.g. boron nitride), can be a prototype for a transistor if a bias is applied. For this purpose, a very thin film of metal (gold) must be evaporated onto the device, to function as an electrical contact. Theoretically, current should not be able to flow due to the insulating material. However, in the realm of quantum mechanics (i.e. at the atomic scale), some of the current is able to tunnel through the insulator. Thus, this special type of transistors bears the name of 'tunneling field effect transistor' and the current extracted through it will give intrinsic information about graphene, such as its conductive properties. Before tunneling transistors are realizable in the market, the properties of graphene can be studied with these actual devices. Understanding them is of utter importance for future applications of graphene in not just electronics, but also areas like solar cells technology or even medicine.

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Nomenclature

E_D Dirac point, page 25

V_b Bias, page 10

V_g Gate voltage, page 8

AFM Atomic Force Microscopy, page 13

BF Bright field (optical microscopy), page 13

CB Conduction band, page 2

DAC Digital to analog converter, page 21

DCM Dichloromethane, page 16

dI/dV Differential conductance, page 4

DIC Differential interference contrast (optical microscope), page 15

DOS Density of states, page 4

EBL Electron Beam Lithography, page 17

FET Field Effect Transistor, page 1

hBN Boron nitride, page 3

IPA Isopropyl alcohol, page 16

MMA Methyl methacrylate, page 14

STM Scanning Tunneling Microscopy, page 4

STS Scanning Tunneling Spectroscopy, page 4

TFET Tunneling Field Effect Transistor, page 1

UHV Ultra-high vacuum, page 4

VB Valence band, page 2

Contents

1 Introduction

Shortly after the discovery of graphene, a single layer of graphite, a whole spectrum of thin materials was found to complement graphene's remarkable electronic structure. By assembling thin layered materials — also called van der Waals heterostructures — many possibilities emerged for exploring rich physical phenomena. One exciting direction is also realizing novel technological applications by designing new types of transistors [1].

Field Effect Transistors (FETs), made of silicon, constitute a fundamental pillar in microelectronics, yet they are inevitably constrained by Moore's law. As these transistors shrink in size, their packing density is limited due to the excess of power dissipation and quantum tunneling [2].

However, the very same phenomenon of quantum tunneling can be exploited as an alternative method that enhances FETs [3]. To this end, graphene heterostructures combined with an insulator, such as boron nitride (hBN), present a viable option to construct Tunneling Field Effect Transistors (TFETs) . This poses graphene as a potential substitute for silicon in the semiconductor industry [1,3]. Before such technological advancements can be made, the fundamental physics within graphene heterostructures must be studied.

In the following sections of the introduction (chapter 1), we will describe graphene's intrinsic properties, its use in the fabrication of TFET's, and how graphene can be studied using tunneling spectroscopy. In chapter 2, Theory, we explore a model for the tunability of graphene and also the concept of quantum tunneling. Chapter 3 is dedicated to describe the fabrication process of TFET devices, which we will then measure in chapter 4 and 5. Results obtained in this thesis will be summarized in the last chapter.

1.1 Graphene and its properties

Graphene is a single and atomically thin layer of graphite. Carbon atoms bond covalently in sp^2 hybridization i.e. a spatial configuration in which the s-orbital combines with two p-orbitals (Fig 1a). This allows the bonding to be coplanar and in a honeycomb shape lattice (Fig. 1b). As a result, graphene is not only the strongest material ever measured [4], but also a flexible lattice that can be studied under ambient conditions.

Though invisible to the bare eye, graphene has always been right in front of us. Its discovery, by A. Geim and K. Novoselov, led to the study of the first two- dimensional sheet of atoms, for which they were awarded the Nobel Price in 2010 [5]. However, graphene's history goes back to the nineteenth century, when British chemist Benjamin Brodie in 1859 observed accidentally what he called "graphon" [6]. These laminated sheets of carbon were found in graphite samples exposed to acidic solutions. Today, we now know he observed a suspension of graphene oxide [6]. Almost a hundred years later, theoretical predictions for

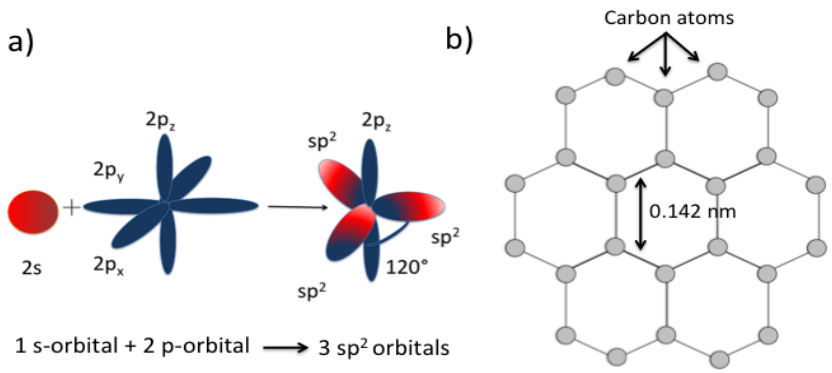

Figure 1: (a) Hybridization of sp2 orbitals with its characteristic 120° separation between orbital. (b) Graphene's honeycomb shape lattice.

"a monolayer of graphite" were developed [5]. But it was not until 1989 when the name graphene was first coined by Boehm et al [6].

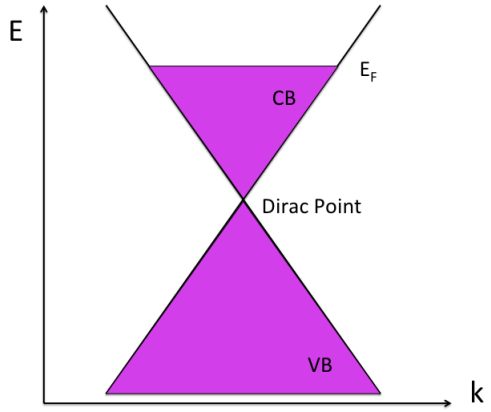

Figure 2: Model of the band structure of graphene, energy vs k vector (or momentum) at low energies. Electronic features are marked such as the Dirac point, where VB and CB meet. The Fermi Energy (E_F), which is the last occupied energy state for the electrons, is drawn arbitrarily in the CB.

One of the most remarkable properties of graphene is its unique band structure at low energies. The valence band (VB) and conduction band (CB) are conically shaped and join at a single point called the Dirac point (Fig.2). Evidently, for graphene, unlike semiconductors or insulators, there is no gap between VB and CB. This unique property contributes to the measured high electronic mobility [4]. Moreover, graphene does not have partially filled bands, as is the case of metals, because its bands meet at the Dirac point where no available states can be accessed. Thus, graphene behaves unconventionally. Regardless of the position of the Fermi Energy—the last occupied energy state— it cannot be described as a metal, a semiconductor or an insulator [7]. Instead, it is known as a zero gap semiconductor.

The band structure of conventional materials scales energy with the square of momentum, shaping parabolic band structures. However, the linear relationship between energy and momentum for the electrons in graphene

$$E = \hbar \nu_f |p|, \tag{1.1}$$

is similar to that of photons, where $\hbar$ is Plank's constant,ν_f is the speed of the electrons

(Fermi velocity) and p is their corresponding momenta. Due to its unique electronic properties as a 2D material, graphene can also be used to study relativistic quantum mechanics.

1.2 Boron Nitride (hBN)

The combination of thin sheets of materials followed the discovery of graphene and the rise of 2D heterostructures. As such, hexagonal hBN is an insulating material that drew the attention of the scientific community. Just as graphene is obtained from graphite, hBN can be cleaved in the same manner from its bulk crystal to get atomically thin sheets of hBN (Fig. 3).

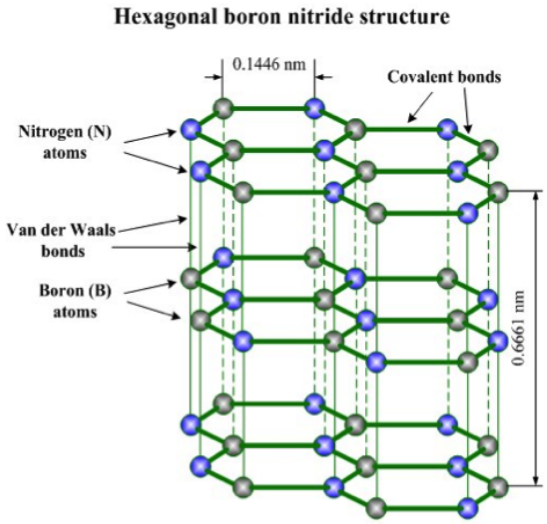

Figure 3: Layers of Boron Nitride joined by Van der Waals forces. Obtained from [9]

Boron nitride was the selected tunneling material to build TFET's. Its large band gap of nearly 5.9 eV [8], smooth layers, and other similarities with graphene— lattice mismatch smaller than 2% [8] — make it the perfect tunneling barrier for the construction of TFET devices. However, it has been shown that hBN thickness should not exceed 2 nm [8] as tunneling current depends on the width and height of the tunneling barrier.

1.3 Scanning Tunneling Microscopy (STM) and Tunneling Spectroscopy

From the invention of optical microscopy to the development of STM , scientists have extensively tried to characterize and investigate materials. STM has been a powerful and widely used technique that is able to provide structural information of surfaces with atomic resolution. Although the study of surface properties with STM does not always provide fine knowledge of the bulk material, 2D materials e.g. graphene present a great advantage because the surface material is the material itself [9].

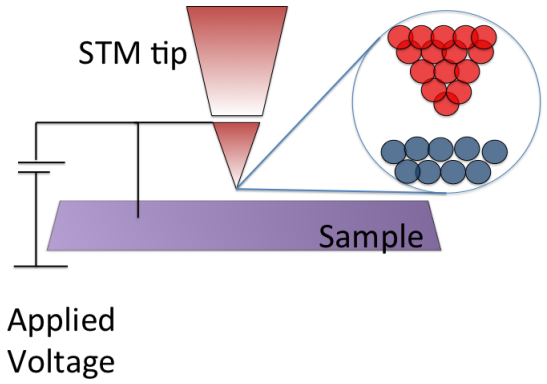

Figure 4: STM tip on top of the probed surface. A voltage is applied between the tip and the sample. The extracted tunneling current provides information about the topography and the DOS of the material. Tunneling current depends exponentially on the tunneling barrier i.e. the vacuum gap between the tip and the sample

STM is based on the principle of quantum tunneling. It consists of a sharp atomic-sized tip, usually made of tungsten or platinum-iridium, placed closely above the surface to be studied, leaving a vacuum gap in between (Fig.4). Once a voltage between the tip and the surface is applied, a tunneling current is extracted. This quantity can be used to access the topography of the material by either scanning the surface at constant height or constant current.

On the other hand, tunneling current can be used to obtain the probability density or density of states (DOS) of the surface electrons underneath the atomic sharp asperity. In doing so, differential conductance (dI/dV) of the sample is measured. This mode of operation is also called Scanning Tunneling Spectroscopy (STS). Tunneling spectroscopy enables then a closer look to the electronic properties of materials, where the information provided by the tunneling current scales exponentially with the height of the tip.

However, there are numerous drawbacks to using STM for investigating electronic structure of 2D materials:

- Experiments can take a long time since samples are required to have pristine surfaces. Techniques to achieve and maintain such clean surfaces demand ultra-high vacuum (UHV) which takes several hours. To obtain precise tunneling measurements, the tip of the STM must also be atomically sharp, making it highly fragile and in need of

constant calibration.

- Measurements are sensitive to mechanical noise, which limits experimental conditions:
  - Ultra low temperatures (order of 10-25 mK) cannot easily be achieved because they require cryogenic refrigerators, which induce vibrations to the system and perturb the measurements.
  - High magnetic fields (order of 40 T) cannot be applied either, due to the vibration produced in resistive magnets.

Dealing with these experimental concerns makes STM an expensive research direction that not all the research groups can afford.

1.4 Motivation

To address the shortcomings of STM, we utilize a device alternative that is based on tunneling spectroscopy. This method, used by other research groups [8,11], has been shown to be a powerful technique to study not only the electronic structure of 2D surfaces, but also the quantum vibrational properties of the material (phonon spectrum). We will realize TFET structures such that future research can use these devices to perform tunneling spectroscopy studies under high magnetic fields ($\sim$45T) and low temperatures ($\sim$ 25mK).

By using cutting edge nanoscience fabrication techniques, we replace each part of the STM with an appropriate 2D material. First, a thin insulator (hBN) is laid on top of a single graphene layer on Si-SiO_2. This element replaces the vacuum gap in a STM measurement between the sample and the tip. Secondly, electrodes (made of gold or graphite) are evaporated on top of the stack and function as a tunneling contact, which compensates for the need of an atomically sharp tip in STM (Fig. 5a, 5b).

In this thesis, fabrication of layered materials to study graphene's electronic structure was achieved through mechanical exfoliation, described in the following chapters. Several Van der Waals heterostructures were built and studied with the following configuration (from bottom to top layer):

Si-SiO_2/Graphene/hBN/Au (Fig.5b), Si-SiO_2/hBN/Graphene/hBN/Au and Si-SiO_2/hBN/Graphene/hBN/Graphite

In addition to fabrication, tunneling spectroscopy measurements were performed. A probe station was used to apply a bias, read the tunneling current and measure dI/dV through the device. This was accomplished by attaching needles to the microscopic electrodes that were patterned around the sample. In order to avoid thermal smearing, these devices were measured at cryogenic temperatures (order of 77 K).

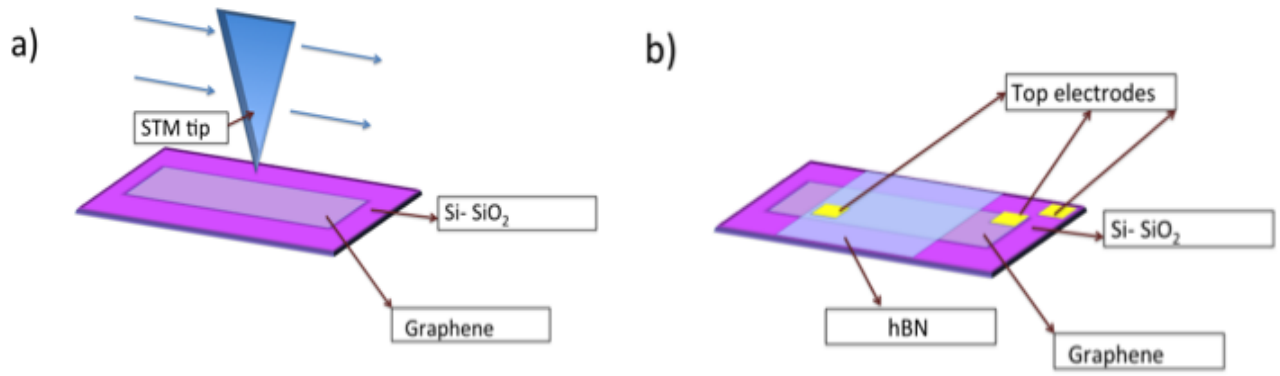

Figure 5: (a) Scanning tunneling spectroscopy with a STM tip probing graphene on Si-SiO_2 substrate; (b) Layout of the alternative device: Si-SiO_2 is the substrate (pink/purple), graphene (light violet) is the material probed and hBN (transparent blue) is the tunneling barrier. Electrodes (yellow) are placed on top of the graphene layer, the tunneling junction and the substrate.

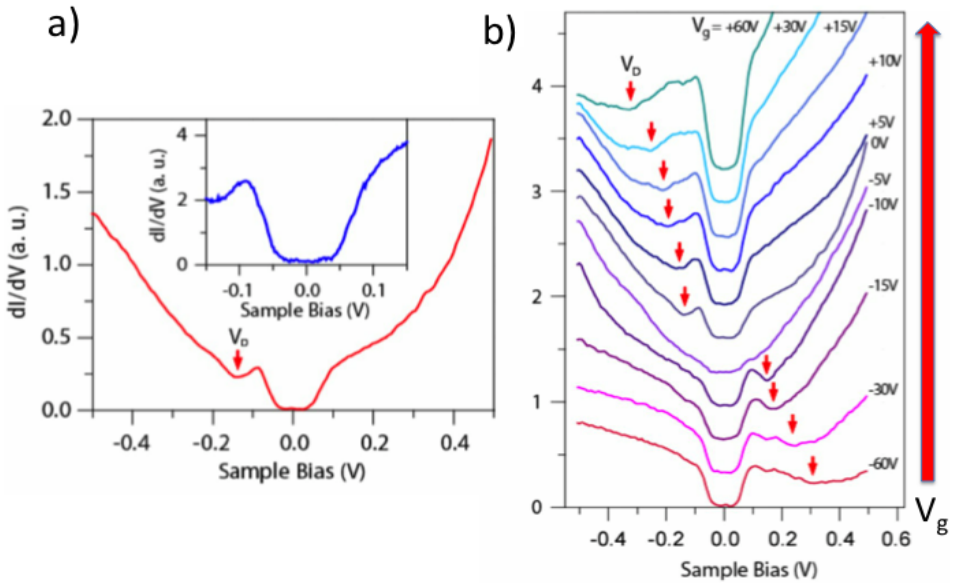

Figure 6: (a) Conductance of graphene vs bias obtained with a STM measurement, from [12]. Local minimum, marked as V_D, and global minimum, around zero bias, are displayed. Inset is a close up of the low bias region (b) Conductance of graphene that shows the gate tunability of V_D, while the global minimum is independent of the gate voltage.

According to previous studies, graphene's transport shows a local minimum in dI/dV displayed in fig. 6a. This shoulder in conductance is tunable [10,11,12] when a perpendicular electric field emanating from the back gate electrode (Si-SiO_2) is applied, as shown in fig. 6b. Moreover, a global minimum, which is pinned to zero bias, is shown to be gate voltage independent. The local minimum was identified to likely correspond to the Dirac point of graphene [10,11,12]. On the other hand, the global minimum can be attributed to inelastic tunneling processes that are not part of graphene's electronic structure [8,10,11,12].

Characteristics of the TFET's devices should mirror those obtained through STM in the literature. The use of tunneling transistors is presented then as a good complement to STM, setting the basis for further research of graphene under high magnetic fields and ultra low temperatures.

2 Theory

2.1 Tunability of DOS in graphene: Parallel plate capacitor model

A simple FET model to describe graphene tunability of its DOS is the parallel plate capacitor model. The charge and density carriers of graphene can be varied controllably by applying a perpendicular electric field to the sample (also known as gating, V_g). The p-doped Silicon and graphene act as the parallel plates, while an insulating layer of SiO_2 functions as the dielectric material between the plates (Fig. 7a).

The potential difference in the capacitor (V_g) will be proportional to the perpendicular electric field (E) and the distance between both plates (d), where $E = Q/(A\epsilon_0\epsilon_d)$ and hence $V_g = Ed = Qd/(\epsilon_0\epsilon_d A)$. In these expressions, ϵ_d and ϵ_0 are the relative permittivities of the dielectric and vacuum respectively and A is the area of the capacitor. Then, we can calculate the charge of the capacitor to be $Q = V_g C_g$, such that the capacitance is $C_g = \epsilon_0\epsilon_d$ A / d. For a parallel plate model, the charge density (n) of the device can also be found using $n = V_g C_g/e$, where e is the electron charge.

The position of the Fermi level in graphene's DOS will shift accordingly to the applied gate voltage due to the build up of charge carriers in SiO_2. The relationship of this change (equation 2.2) can be calculated to be [10],

$$E_F = \hbar\nu_F\sqrt{\pi V_g}, \tag{2.2}$$

where ν_F is the Fermi velocity approximated to be 10^6 m/s and $\hbar$ is the reduced Planck's constant. Thus, we can change graphene's DOS by modulating its Fermi Energy and make it p-doped (hole excess), neutral or n-doped (electron excess) (Fig. 7 b,c,d).

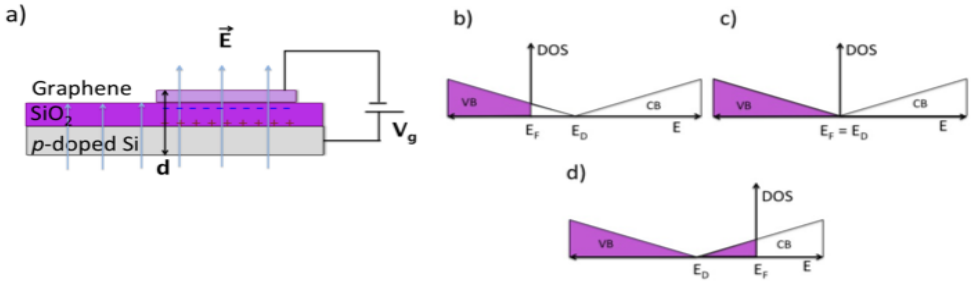

Figure 7: (a) Parallel plate capacitor model with graphene and p-doped silicon acting as conducting materials and SiO_2 as the dielectric (insulator). Charge builds up and controllably changes the DOS of graphene; For (b), (c), (d) (modified from [10]) E_F is the Fermi Energy and E_D Dirac point; (b) DOS of graphene when a negative gate voltage is applied (hole or p-doped); (c) DOS of graphene configured to charge neutrality (Fermi Energy is at the Dirac point); (d) DOS of graphene when a positive gate voltage is applied (electron or n-doped)

2.2 Tunneling through a potential barrier

To provide an intuition for the quantum tunneling exploited in STM measurements and TFETs, the problem of a rectangular potential barrier is solved in this section. The tunneling barrier in STM is the vacuum gap between the tip and sample, whereas for the case of the TFET devices it is the thin sheet of hBN sandwiched between gold and graphene.

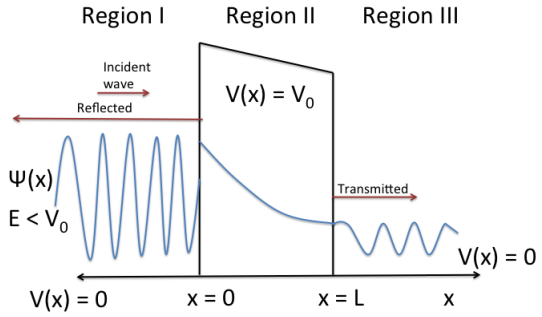

Figure 8: Illustration of tunneling through a potential barrier (V_0). **Region I** ($x < 0$) shows an incoming wave $\Psi(x)$ with energy (E) where $E < V_0$. The wave decays exponentially in **Region II** ($0 < x < L$) and partially reflects in **Region I**. Then, the transmitted part continues its trajectory with smaller amplitude in **Region III** ($x > L$). Modified from [14].

A rectangular potential barrier is simply represented as $V(0 < x < L) = V_0$ and otherwise $V(x < 0 \text{ and } x > L) = 0$ as in Fig. 8. The solution for a quantum particle that encounters such a barrier is given by Schrodinger's equation(2.3). The former can be further simplified using $k = 2m(E - V(x))/\hbar^2$ to give equation (2.4),

$$-\frac{\hbar^2}{2m}\frac{d^2}{dx^2}\Psi(x)+U(x)\Psi(x) = E\Psi(x) \quad (2.3)$$

$$\frac{d^2}{dx^2}\Psi(x) = -k^2\Psi(x). \quad (2.4)$$

The piecewise solution of $\Psi(x)$ for a wave with an energy $E < V_0$ is found in equation 2.5 for the different regions displayed in Fig.8.

$$\Psi(x) = \begin{cases} C_1 e^{ik_1 x} + C_2 e^{-ik_1 x}, & \text{if } x < 0 \\ C_3 e^{k_2 x}, & \text{if } 0 \leq x \leq L \\ C_4 e^{ik_1 x}, & \text{if } x > L \end{cases} \quad (2.5)$$

(1) In **Region I** ($x < 0$) the k value is given as $k_1 = \sqrt{2mE/\hbar^2}$ and the solution shows a superposition of waves. There is an incoming wave traveling in the positive direction – represented by the first term with positive exponent – and a reflected counterpart, which is described by the second term with negative exponent.

(2) In **Region II** ($0 < x < L$), if the energy of the quantum wave is smaller than the potential barrier ($E < V_0$), k becomes $k_2 = \sqrt{2m(E - V_0)/\hbar^2}$. Hence, an exponential solution for equation (2.4) is found. However, we must disregard the positive exponential solution because the amplitude of the wave can only decrease in this region.

(3) In **Region III** ($x > L$), the wave is transmitted with a smaller amplitude than initially and traveling in the positive direction.

Using the boundary conditions in Fig. 8 and the continuity of the wave function in each region we can calculate the reflection (R) and transmission (T) coefficients [17] such that $T + R = 1$, where,

$$R = \frac{|C_2|^2}{|C_1|^2} = \frac{sinh^2(k_2 L)}{1 + \frac{1}{4}\frac{V_0^2}{E(V_0 - E)} sinh^2(k_2 L)} \text{ and } T = \frac{|C_4|^2}{|C_1|^2} = \frac{1}{1 + \frac{1}{4}\frac{V_0^2}{E(V_0 - E)} sinh^2(k_2 L)}. \quad (2.6)$$

Notice that for low energies ($E << 1$) and wide barriers ($L >> 1$) we can approximate T in equation (2.6). We see then that $k_2 L >> 1$ is large and $sinh(k_2 L) = \frac{1}{2}(e^{k_2 L} - e^{-k_2 L}) \approx \frac{1}{2} e^{k_2 L}$, where this term will exponentially increase as L gets wider. We can now neglect the second term in the denominator of T and obtain

$$T \approx \frac{1}{\frac{1}{4}\frac{V_0^2}{E(V_0 - E)} \left(\frac{1}{2} e^{k_2 L}\right)^2} = \frac{16E(V_0 - E)/V_0^2}{e^{2k_2 L}} = \frac{16E(V_0 - E)}{V_0^2} e^{-2k_2 L}. \quad (2.7)$$

Thus, with the help of this picture we can determine that tunneling is dependent on the width (L) and the height (V_0) of the barrier, which on STM measurements is modified by the tip-sample height.

2.3 Elastic and inelastic tunneling

TFET's are based on the principle of tunneling spectroscopy, of which there are two ways for tunneling to manifest. **Elastic tunneling** is the process through which electrons will go from the constant DOS of the metal (filled up to the Fermi Level) to the lowest DOS of graphene. In contrast, **inelastic tunneling** is the process through which electrons will jump into an excited energy state and effectively create an excitation as they enter the sample [10]. The electron will then loose energy from the excited state of graphene to the lower electronic state. The difference between those energy states is denoted here $\hbar\omega_0$.

When a bias (V_b) is applied between two metals (e.g. graphite or Au) separated by an insulating layer (hBN), the Fermi Energies of the metals will shift. Then, electrons that have an energy $\hbar\omega_0$ can either tunnel elastically from one metal to the other or proceed through inelastic tunneling [14].

In graphene, elastic tunneling is expected to follow a V-shape in conductance according to its band structure (Fig.9a). However, inelastic tunneling opens an additional channel for conduction and suppresses the elastic processes [8,10,11]. This changes the slope of the IV around zero bias and makes tunneling conductance remain zero until the electrons achieve a threshold of $\hbar\omega_0$, i.e. $eV_b > \hbar\omega_0$ (Fig.9b,c).

The energy of the excitation is released through phonons (vibrations of the lattice). The so-called phonon gap is calculated to have a width of approximately 100-150 mV around the zero Fermi Energy [8,10,11]. A diagram of inelastic tunneling and gate tunability is shown in Fig.10.

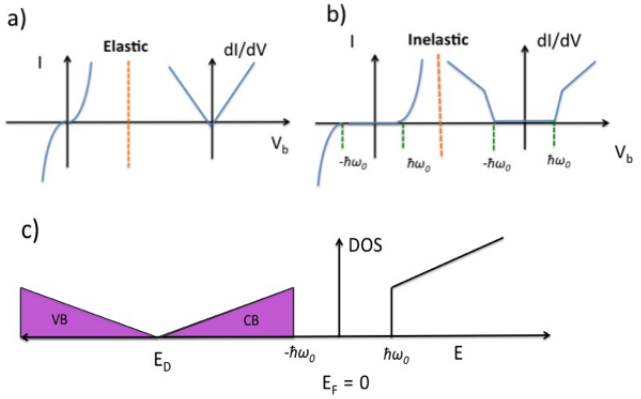

Figure 9: (a) IV and dI/dV for elastic tunneling. The V-shape in dI/dV is shown in agreement with graphene's band structure; (b) IV and dI/dV for inelastic tunneling and the gap of width $2\hbar\omega_0$. (c) Model of the probed DOS of graphene (modified from [10]), where inelastic tunneling opens an additional channel for conductance and suppresses elastic tunneling. No conduction is measured around the Fermi Energy until a threshold energy, $\hbar\omega_0$, is attained (phonon gap). .

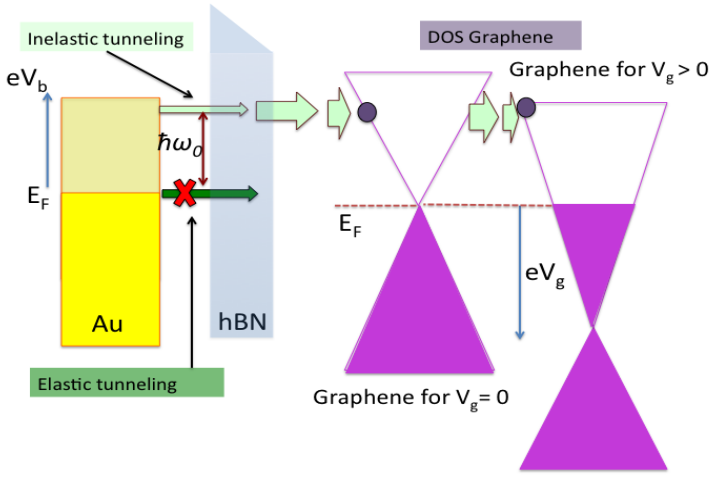

Figure 10: Diagram of tunneling through the heterostructure. Au is the electrode with constant DOS (yellow), hBN is the barrier (blue) and graphene the probed sample (purple). Applying a bias (V_b) shifts the Fermi level of Au, and once a threshold is reached ($eV_b > \hbar\omega_0$) electrons can tunnel through hBN to graphene's DOS releasing a phonon (light blue arrow). Here, elastic tunneling (green arrow) is suppressed. Moreover, to access more states of graphene we can vary the gate voltage according to section (2.1).

3 Fabrication

We will focus for now on the fabrication of devices with the following layout: Si-SiO_2/Graphene/hBN/Au. We utilize thermally grown 285 nm thick SiO_2 on Si (Si-SiO_2) as the supporting substrate of the heterostructure and the back gate of the device. SiO_2 is then cut in squares of ~ 7 mm with a diamond pen (Fig. 11a). These squares are washed, sonicated and heated (Fig. 11b,c where arrows show marks on chip), in order to clean the substrate sufficiently and promote adhesion of graphene when placed on top.

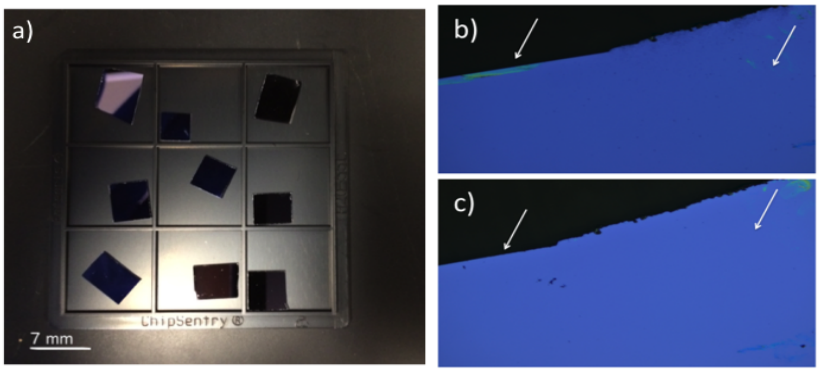

Figure 11: (a) 9 chips cut of SiO_2 , (b) Optical microscope image before the SiO_2 chip is cleaned; c) After the SiO_2 chip is washed, sonicated and heated.

3.1 Graphene exfoliation

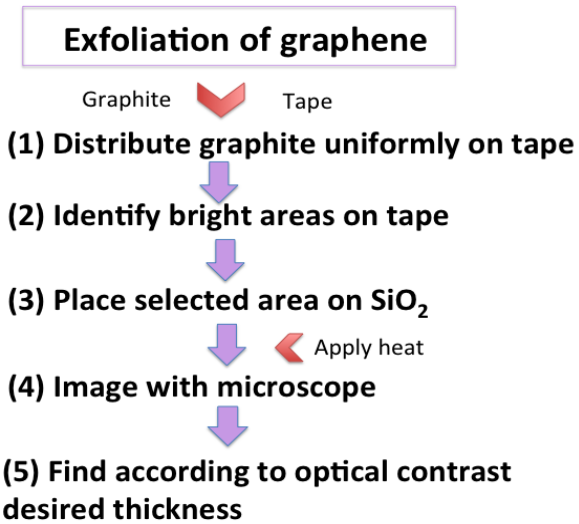

Figure 12: Diagram on steps of how to exfoliate graphene on SiO_2. Red arrows represent materials and/or heat.

Mechanical exfoliation is a method that uses scotch-tape to cleave graphene layers from bulk graphite (Fig.12). For the experiments we used a dehumidifier to keep the room dry at all times. First, the tape is placed directly on top of the graphite crystal and lifted off carefully. The graphite that is stacked to the tape is then cleaved further by folding the former in a 45- degree angle around the same area. Lastly, graphite is distributed uniformly throughout the tape.

In order to find graphene, the tape is observed under a light source to find windows where graphite appears to be thinnest (Fig. 13a). Once an area is selected, the tape is placed and rubbed onto the SiO_2 wafer. Finally, the exfoliated substrate (with the tape on top) is placed on a hot plate at 115 ^oC for 15 min to promote uniform contact at the interface between the source crystal and the SiO_2 [15]. Numerous graphene flakes on SiO_2 are found under optical microscopy in bright field (BF) mode, but only one flake is selected for further stacking (Fig 13b). A program in python was developed to find the direct relationship between the opacity of the flake under the microscope and its real thickness. Ideally, we are looking for monolayer graphene, but this program can be used for bilayer and trilayer graphene as well. Additionally, one could also check that it is a suitable graphene flake by measuring its thickness with advanced techniques such as Atomic Force Microscopy (AFM) .

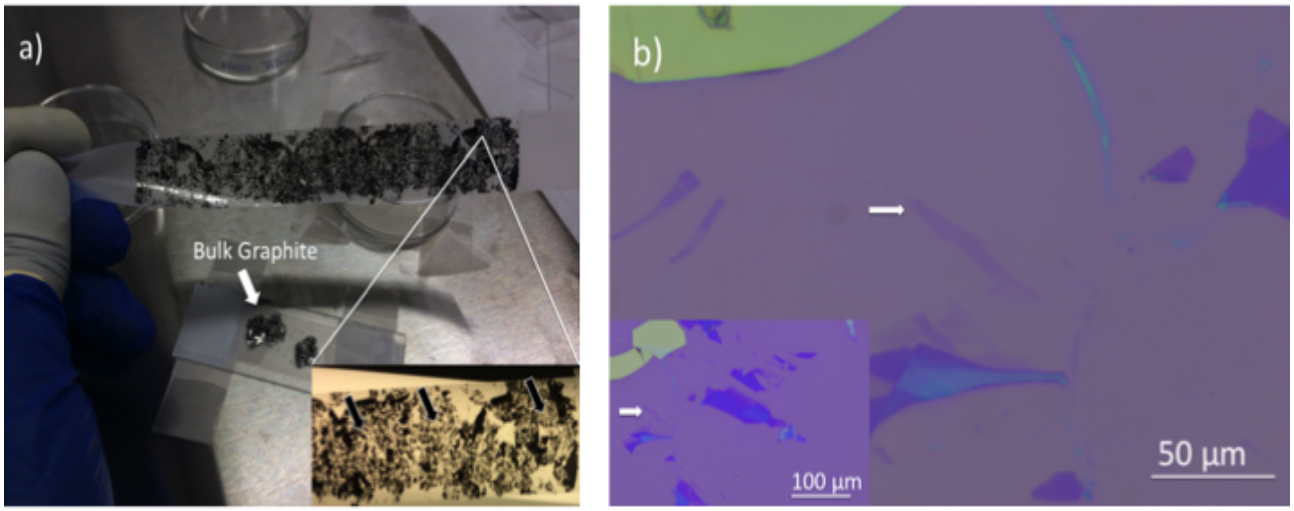

Figure 13: (a) Exfoliation of graphene with tape from bulk graphite. Graphene is evenly distributed around the tape, then observed against the light (inset) to find the regions where it appears to be thinnest; (b) Monolayer graphene flakes on SiO2 under the microscope; inset displays bird eye of the same flake.

3.2 Boron Nitride exfoliation and identification

A similar procedure is followed, (Fig. 14), for exfoliating hBN from its parent crystal, where the SiO_2 substrate is replaced by the polymer methyl methacrylate (MMA) . The exfoliation process (scotch tape method) evenly distributes hBN crystal throughout the tape, and the most reflective area is selected to be placed on top of MMA (Fig. 15a).

Prior to the exfoliation process, preparation of MMA slides is thus required. First, a glass slide with tape is cleaned with acetone and a solution of isopropyl alcohol (IPA). Secondly, the clean glass slide is spin-coated with MMA in a clean room. The spin-coater is set to spin 1200 revolutions per minute, and the glass slide is fixed with vacuum.

When the hBN tape is placed on the coated MMA slide, it should be rubbed slowly onto it with a small metal piece (e.g. a hook). The tape is then stamped to promote better adhesion of the crystal to the polymer. MMA will later be dissolved chemically after transferring onto the fabricated G/SiO_2 substrate (next section). Unlike for graphene, no heat shall be applied to the hBN tape when placed on MMA to avoid corrugation of the polymer. To maintain the purity of the parent crystal, hBN is kept in a desiccator under a pressure of 0.5 Torr and constant nitrogen flow. Additionally, tapes of hBN are reused several times due the high cost of this material as opposed to graphite.

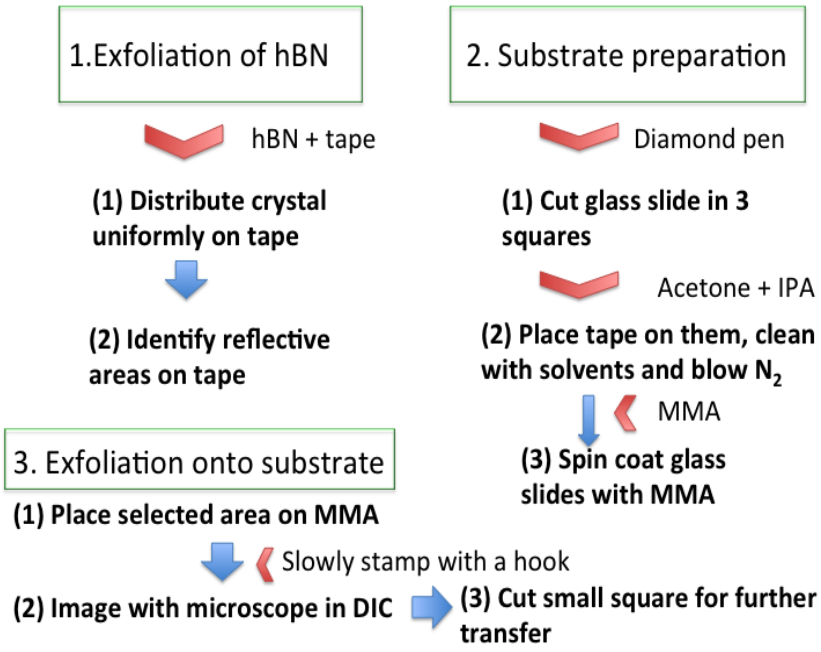

Figure 14: Diagram on the steps of how to exfoliate hBN on MMA. Red arrows represent materials and/or techniques.

Boron nitride is used as a tunneling barrier and thus it is necessary to find atomically thin sheets of hBN (< 2 nm). Differential interference contrast (DIC) microscopy is utilized for this purpose, because flakes on MMA appear almost invisible to the bare eye under BF mode (Fig. 15b). Hence, searching for thin hBN is a long process that requires a trained eye. Once a flake of thin of hBN is found on the slide, a clean razor blade is used to isolate a small square of the selected area to be transferred.

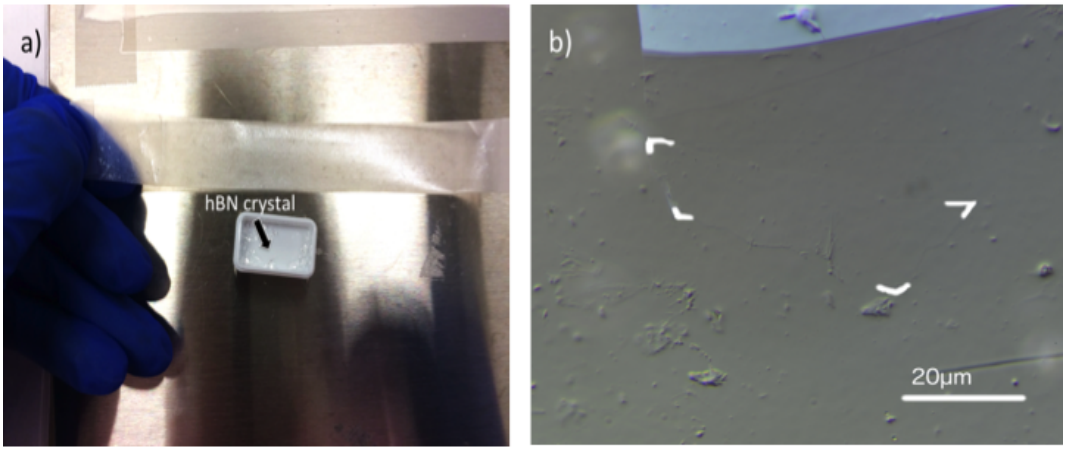

Figure 15: (a) hBN exfoliation; (b) DIC microscope image with a thin sheet of hBN on MMA. Corners of the flake are marked in white instead of outlining the whole flake for a better understanding of thickness.

3.3 Dry transfer procedure

A transfer station is used to stack layered materials. It consists of a stage (Fig. 16a), where the substrate is set, and an aluminum bracket that holds the slide with the sample to be placed on top.

In addition, the stage is connected to a voltage source so that can be heated. Micromanipulators are used to move the stage and bracket in the x, y and z directions (Fig. 16b). The selected flakes can be aligned live on the monitor thanks to a lens placed right above the main stage.

The stage must be properly leveled before contact is made between the target substrate and the 2D material As MMA starts spreading out over the substrate, the stage is heated up to a range of 50-60 °C. When the flakes are completely covered in MMA, temperature is lowered and a time of 15 min is waited before the stack (attached now to the glass slide) is lifted up.

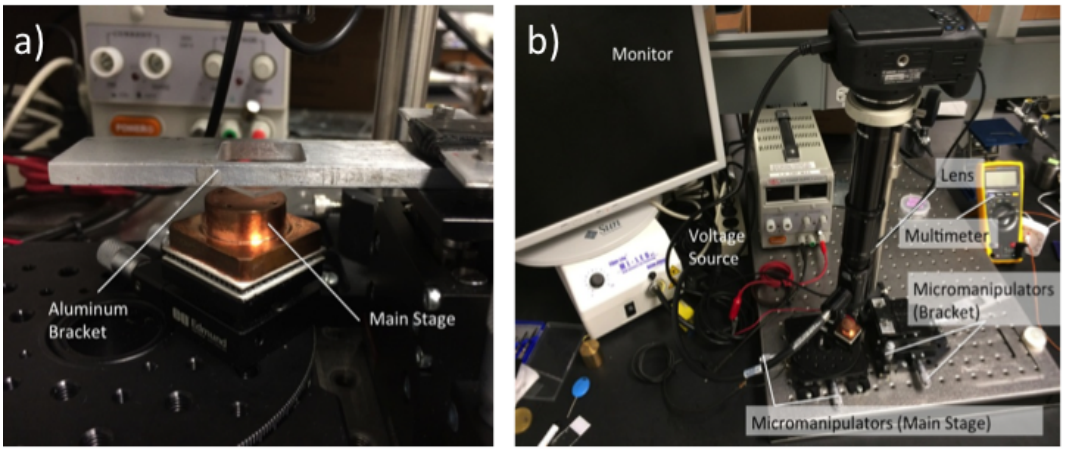

Figure 16: (a) Stage parts; (b) Transfer station and its components

3.4 Dissolution of MMA

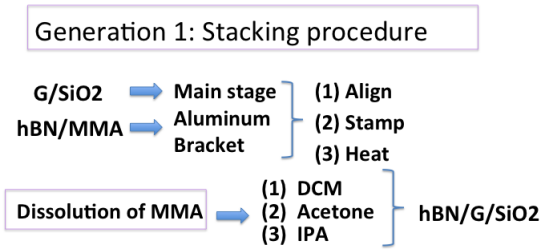

Figure 17: Diagram on steps to perform dry transfer and dissolution of MMA.

When the transfer is completed, MMA must be dissolved in a solution of dichloromethane (DCM) according to Fig.17.

The transfer is then placed in a petri dish filled with DCM and set on a hot plate under 40 °C for 20 min. To avoid quick evaporation of DCM, the dish is covered with aluminum foil.

Finally, two extra petri dishes will be prepared with acetone and isopropyl alcohol (IPA) . The sample is now removed from DCM immediately into acetone and then IPA. After the last chemical bath, nitrogen must be blown rapidly and delicately on the stack, such that no residues remain on the chip. The result for the fabrication is shown in fig. 18a.

3.5 Electron Beam Lithography (EBL)

EBL is a powerful technique used to create microscopic and custom patterns with an electron beam as a drawing pen. The final step for the devices involves the placement of thin electrodes of gold with EBL (Fig. 18b and inset). These will act as leads on the final stack for conduction measurements. This process was, however, performed in another laboratory by graduate students in the solid state department and the received samples were then already patterned.

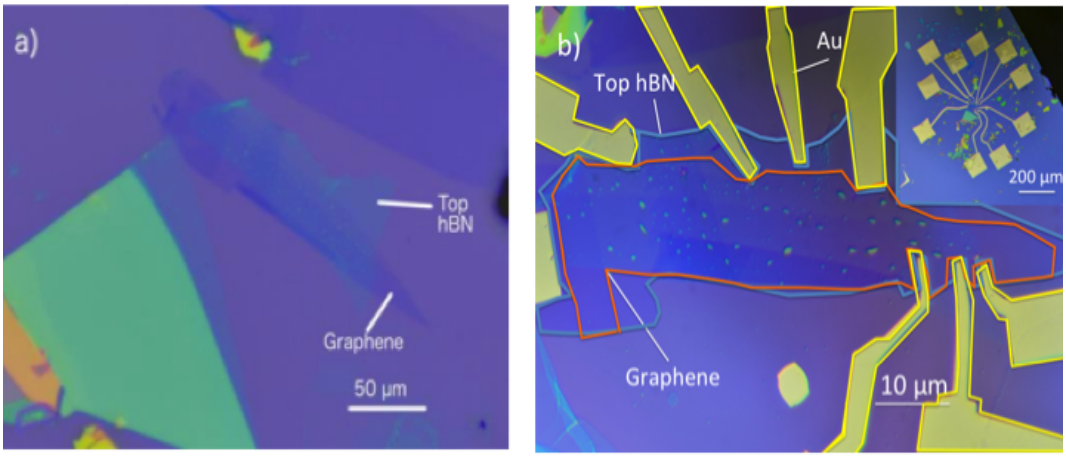

Figure 18: (a) Final transfer of hBN on top of graphene; (b) TFET Generation 1. Top gold electrodes designed with EBL on the fabricated heterostructure; Inset is a bird eye image of the patterned gold electrodes.

The leads were placed above the tunneling junctions (i.e. the intersection of graphene and thin hBN) and on top of graphene, so that tunneling current can be measured. The resultant devices were named Generation I TFET devices.

3.6 Other devices: Generation 2 and 3-device fabrication

To obtain better conduction measurements we fabricated three types of TFET devices in table 1 and their corresponding layout in figure 19. Up to this point, we have only described for simplicity the fabrication process of Generation I devices. .

Table 1: Layout of the devices fabricated

Generation 1 (Fig.19a)	Generation 2 (Fig.19b)	Generation 3 (Fig.19c)
Si-SiO_2/Graphene/ hBN/Au	Si-SiO_2/hBN/Graphene/ hBN/Au	Si-SiO_2/hBN/Graphene/ hBN/graphite

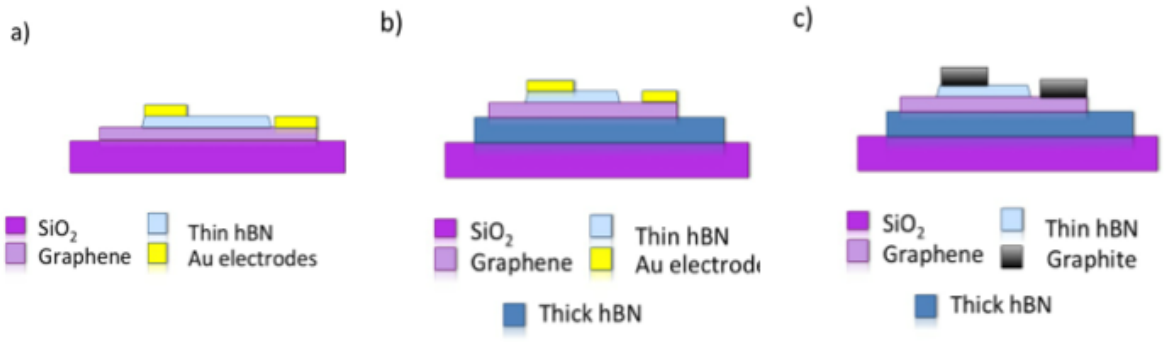

Figure 19: Device layouts: (a) Generation 1; (b) Generation 2; (c) Generation 3.

The study of graphene remains the research goal for the construction of Generation 2 and 3 devices. However, these devices posses significant advantages as opposed to Generation 1. First, the bottom hBN acts as a clean and flat support for graphene compared to the rough SiO_2 [16]. Additionally, intrinsic properties of graphene, which were originally hidden by the charge inhomogeneity of SiO_2, can be observed better using hBN as a substrate [16]. Thus, better conduction measurements can be obtained with Generation 2 and 3 devices.

Fabrication for both types of devices begins with exfoliation of hBN onto the SiO_2 wafer (same procedure as section (2.1) but with hBN). To assure pristine substrates, the hBN on SiO_2 is annealed in a furnace at 500 °C for 5 hours. The selected flake has to be thick in comparison to the top hBN (dark blue under BF mode in the microscope $\sim$ 10 nm as opposed to close to transparent for the top hBN on MMA) and serve as a solid and clean base for the stack (Fig. 20a).

Next, graphene is exfoliated on MMA (same procedure as section (2.2)) and monolayer graphene is to be found with the microscope (Fig. 20b). Transfering of graphene onto the hBN/SiO_2 stack is performed according to section (2.3). To dissolve the remaining MMA, DCM is used (section (2.4)). The next steps are equivalent to the fabrication of Generation

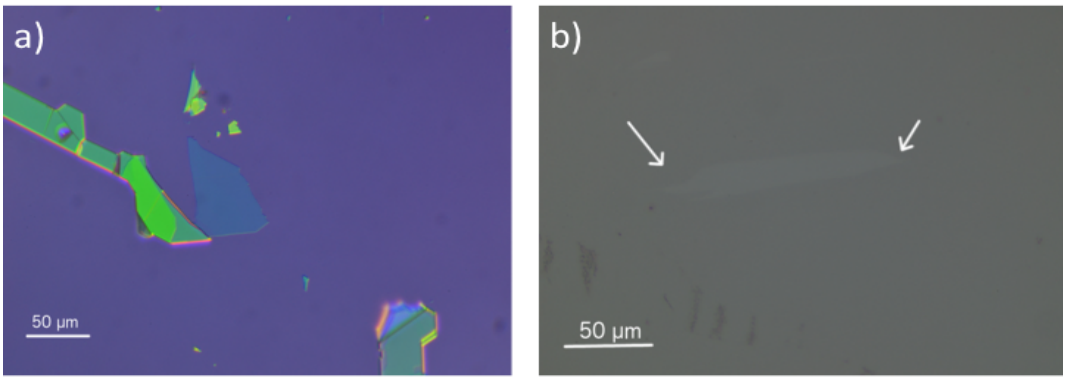

Figure 20: (a) Bottom hBN sample on SiO2; (b) Monolayer graphene on MMA.

1 (Fig.21): the resulting stack is encapsulated with a top few atoms thick layer of hBN (Fig. 22a,b) and EBL is utilized to evaporate top leads on the device (Fig. 23a).

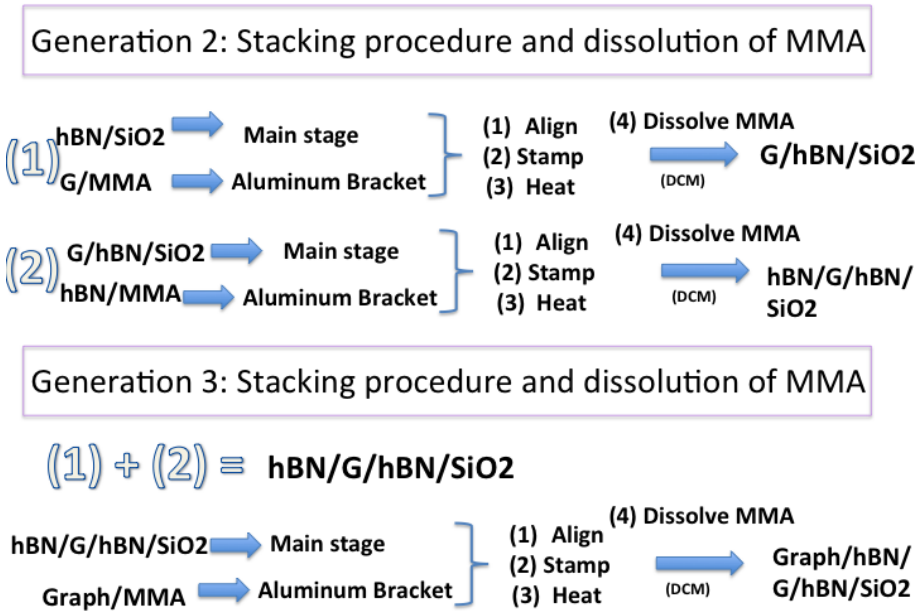

Figure 21: Steps on how to perform dry transfers dissolution of MMA for Generation 2 and 3 devices.

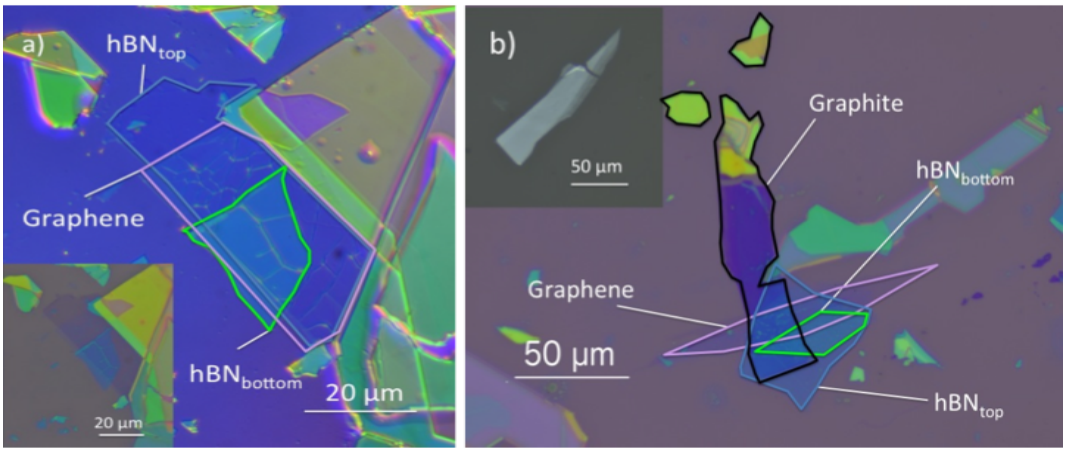

Figure 22: (a) Final transfer for Generation 2 in DIC. Inset is a BF image of the same stack; (b) Final transfer for Generation 3. The inset is an image of the graphite on MMA before it is transfered.

Generation 3 devices are similar to Generation 2 except for its last layer in which graphite is placed instead of the Au leads. To make graphite contacts another exfoliation of the former on MMA is required (inset Fig. 22b). The last step of EBL is then replaced by a graphite transfer, which will act as a top lead of the final stack (Fig.22b). However, gold leads can also be made with EBL to facilitate conduction measurements (Fig. 23b).

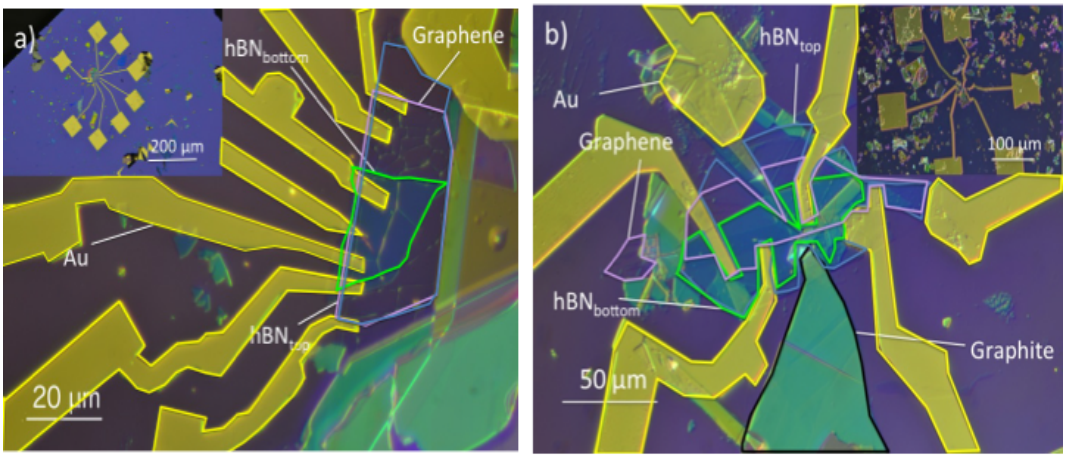

Figure 23: (a) TFET Generation 2. The inset is a bird eye of the device with the golden patches designed as squares; (b) TFET Generation 3. The inset is a bird eye of the device.

4 Method

Tunneling spectroscopy measurements were performed with a probe station (Fig. 24a) at cryogenic temperatures using nitrogen (77K). The devices were placed in the chamber (Fig. 24b) that is connected to a vacuum pump and a cryogenic feed-through. The micromanipulators of the probe station move the needles to the top electrodes of the device, and a lens monitors the chamber. There were two goals with these measurements:

- Find differential conductance (dI/dV) at different biases (V_b).
- Change the gate voltage (V_g) and measure dI/dV at some finite V_b.

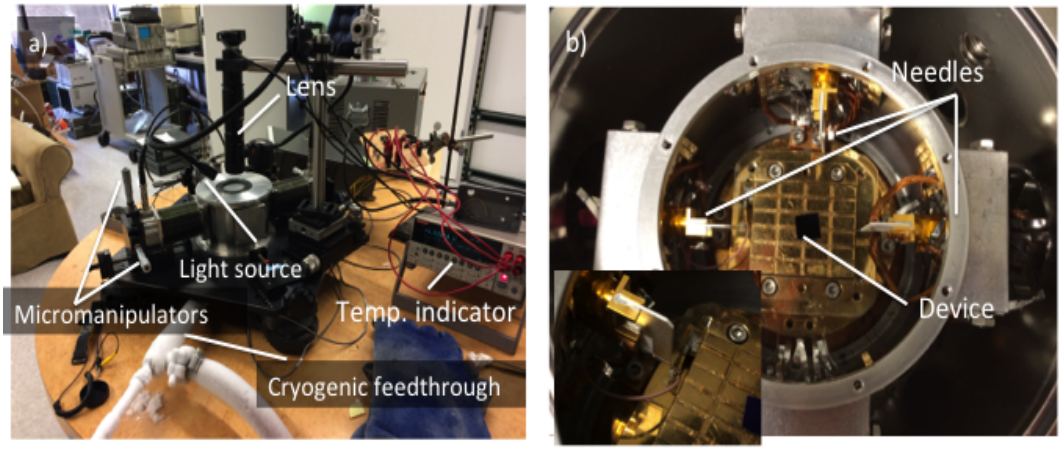

Figure 24: (a) Probe station and its components; (b) Chamber where the device/s to be tested is/are placed. This chamber is in vacuum and cooled at cryogenic temperatures. The inset is a close up of one of the needles.

Several electronic systems were used to achieve these goals (Fig. 25). First, a digital-to analog-converter (DAC) is used to apply the V_b. We utilize a lock-in amplifier for the measurement of the dI/dV because it can extract small signals that are buried in noise when mixed with a reference source. Hence, the input signal is the bias applied by the DAC and the reference signal is a sinusoidal perturbation of 100 μV.

After the mixing of reference and input signal, we used an amplifier to enhance the signal and the former is fed back into the lock-in to determine the conductance.

Lastly, before the devices are placed inside the chamber, it is necessary to make a deep cut in the Si-SiO_2 wafer with a diamond pen. One of the probes is to be placed on this cut such that we can tune the DOS of graphene (vary the V_g). A Keithley was used to then sweep the V_g i.e. a perpendicular electric field through the sample, and measurements were taken at a zero and finite V_b.

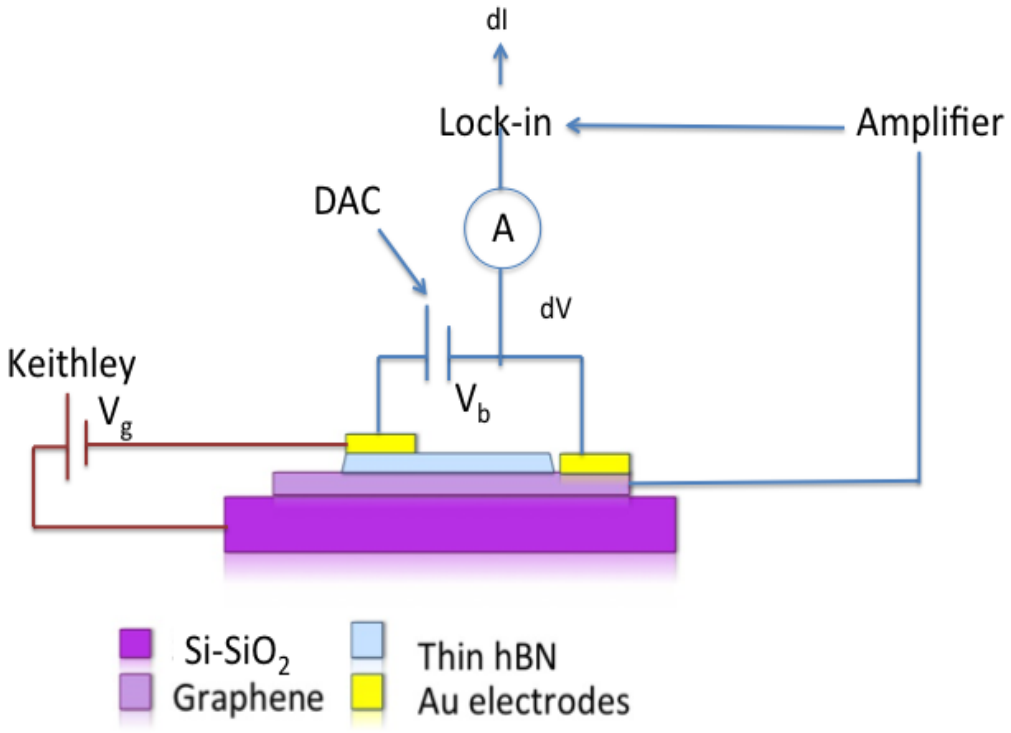

Figure 25: Diagram of electronics in the probe station. The DAC applies a V_b, the lock-in adds the perturbation (dV) and the output signal is amplified and fed back into the lock-in. This way the tunneling current can be extracted from the sample and dI/dV can be measured. In addition, the Keithley controls the V_g.

5 Results

Experiments were performed for several fabricated devices. I assisted and helped graduate student John Davenport on the measurements discussed in this section. Several devices displayed similar behaviors in IV and dI/dV measurements. These measurements are in agreement with those taken by other studies with STM [10].

However, some of the devices were unsuccessful. We attribute this to the fabrication process. Limitations for tunneling were found to be thick hBN top layers (> 2 nm) because tunneling current depends on the width of barrier. Additionally, excess on the thickness of the bottom hBN ($> 10 - 15$ nm for Generation 2 and 3) led to device failure because it makes it hard to see the stack assembly. Finally, we found that superfluous graphite flakes surrounding the active area of the device led to shorts. Therefore, it is important to have a clear area surrounding the tunneling junctions.

Generation 3 devices required additional gold probes to be measured and results were similar to Generation 2. Generation 2 devices showed the best conduction measurements and the following plots correspond to such.

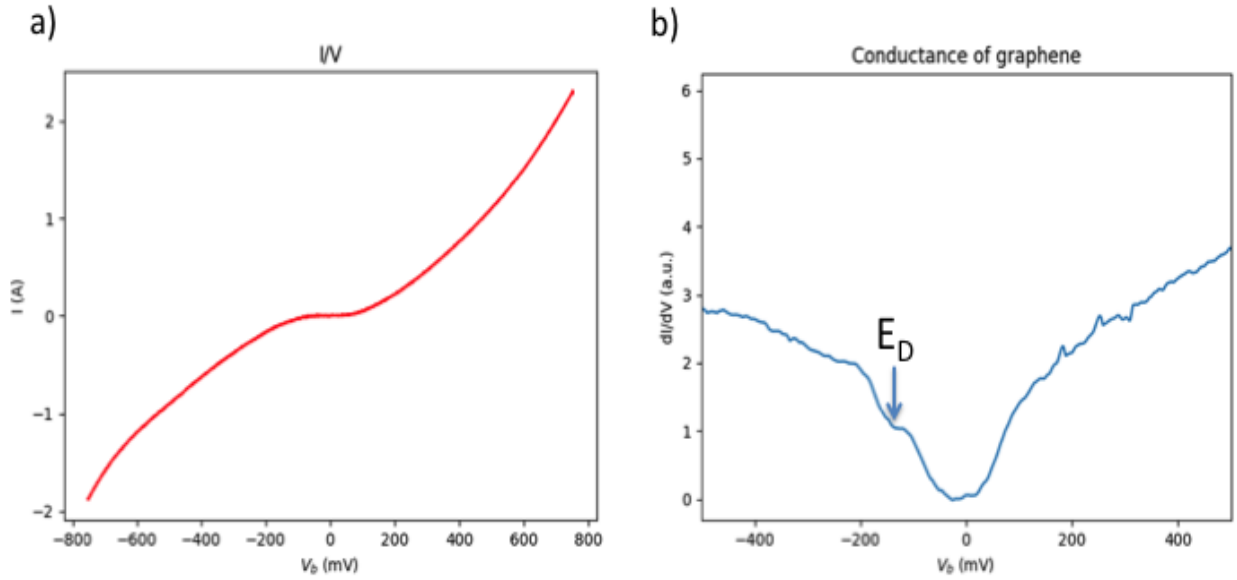

Figure 26: (a) IV curve for the device at 77 K. (b) dI/dV with respect to V_b. Features, such as small shoulder in conductance (E_D) and a broad global minimum, can be observed.

The IV plot, shown in Fig. 26a, is highly non linear and displays a current that is close to zero at low biases. The corresponding dI/dV in Fig. 26b was measured directly with a lock-in amplifier. It displays two dominant features:

(a) A broad dip at low bias in the range -60 mV $< V_b <$ 60 mV that is close to zero conductance.

(b) A small shoulder at -180 mV. Here, the broad dip feature is a global minimum in dI/dV, whereas the shoulder feature is a local minimum. Fig.26b shows the non V-shape of the DOS in graphene, as predicted with inelastic tunneling processes (see Theory section).

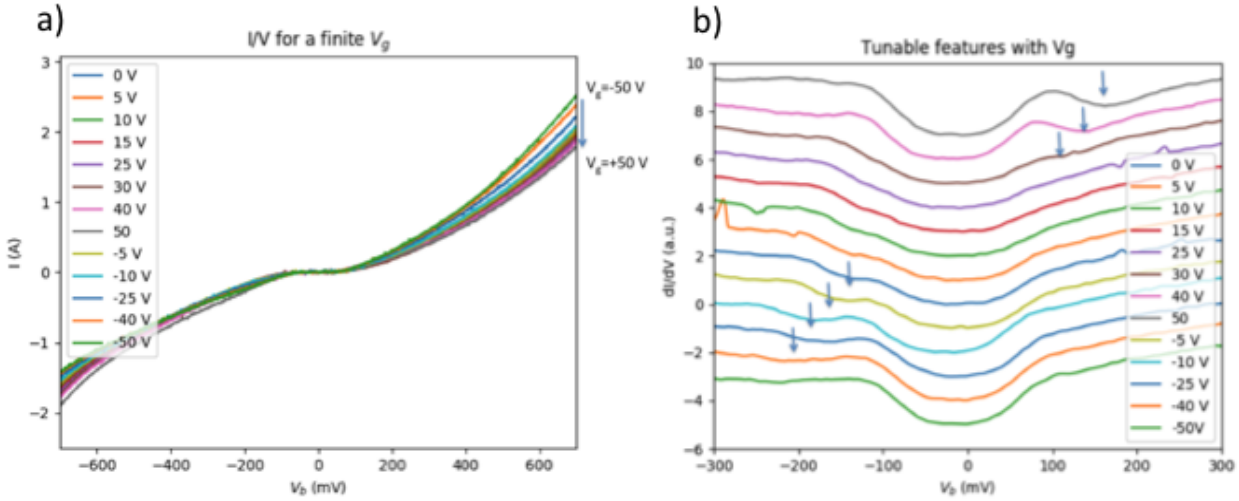

Figure 27: (a) IV curve increasing gate voltage from -50V to +50V at 77 K. (b) dI/dV with respect to bias (V_b) for the range of gate voltages shown in the IV curve. The dip in conductance (blue arrow) moves from the left side to the right side as gate voltage is increased.

To further understand these two spectroscopic features, we measured dI/dV as a function of gate voltage. These data are shown in Fig. 27 where IV is included as well. When V_g is varied between -50 V and +50 V (Fig.27a), the broad dip in conductance remains pinned to the zero Fermi Level in dI/dV (Fig 27b). Temperature dependence of the global minimum has also been investigated in previous literature, showing no significant change of the gap [10]. On the other hand, the small shoulder shifts as a finite V_g is applied.

Local minima (small shoulders in conductance) were found and plotted for the different gate voltages applied to the device in Fig. 28. An observed and expected square root of V_g-dependence is found following equation 2.2 in the Theory section. The data show that a linear relationship is also possible for the fit.

These results suggest that the small shoulder in conductance could be the Dirac point (E_D), a unique feature of graphene where conductance is minimized. Additionally, we can deduce that the feature that is insensitive to the gate voltage is not related to the band structure of graphene. Thus, the broad dip in conductance may correspond to inelastic tunneling electrons. The momenta of the electrons are released to a certain energy threshold, which in this case is at $\hbar\omega_0 \sim 60$ mV, in agreement to previous literature where this broad feature was observed [8]. Hence, we can also address this feature as the phonon gap.

Finally, one possible explanation for the linear (V-shape) behavior in the fit of Fig 28 lies on the thickness of graphene. When the DOS of bilayer graphene is probed instead of monolayer (as initially intended in the fabrication of the device), the behavior of E_D with Vg should be linear [17]. This may explain our observations of Fig. 28 but further experiments are needed to determine the exact nature of the gate dependent feature.

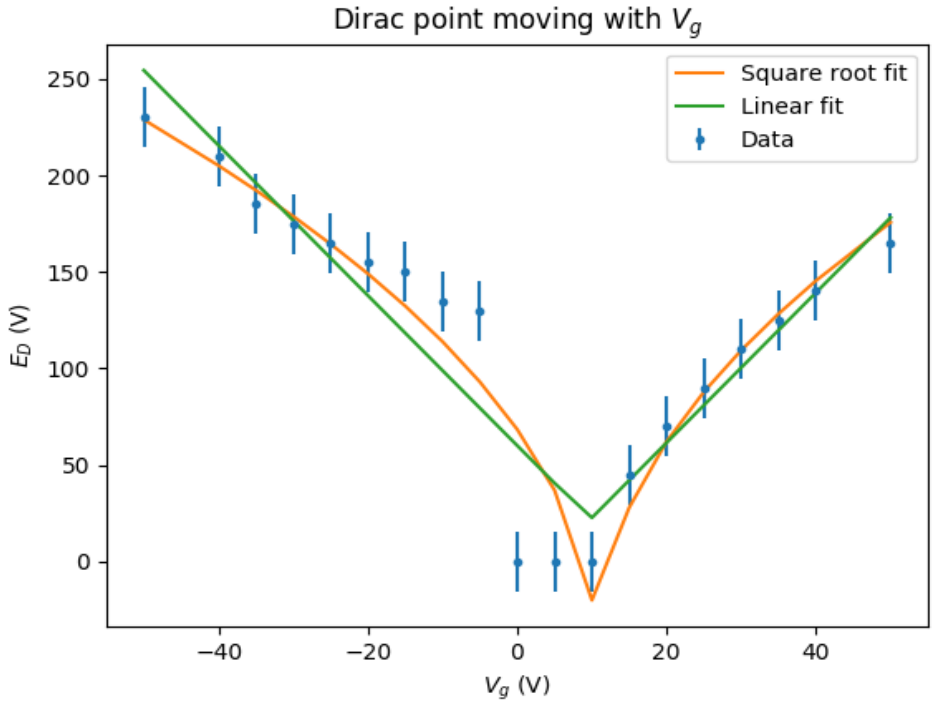

Figure 28: Square root or linear dependence candidates of the local minimum (E_D) as it shifts with the gate voltage.

6 Conclusion and outlook

In summary, TFET's are fabricated heterostructures that present a potential complement to the use of STM for spectroscopy measurements. Fabrication of TFET's is a rather uncostly method (as opposed to STM) to explore any materials' electronic structure. Being the first 2D material, graphene is an excellent sample to be probed with TFET's because of its unique linear band structure at low energies.

The construction of TFET devices was performed by mechanically exfoliating the parent crystal onto Si-SiO_2 as the main substrate. In order to cleave thin layered materials — graphene from graphite and thin sheets of hBN from hBN crystal (Generation 1) — the scotch method was used. Finding thin sheets of hBN was, however, a tedious work since only devices with hBN thinner than 2 nm responded to the measurements.

Moreover, devices with graphene sandwiched between a flat bottom layer of hBN and a top thin sheet of hBN (Generation 2) presented the best measured results. Using a bottom hBN layer avoided the roughness of the original substrate Si-SiO_2 and its charge inhomogeneity, which obscured the electronic structure of the sample (in agreement with the literature). On the other hand, devices with graphite as the contact probe (Generation 3) yielded unclear results and needed gold probes to be attached so that conduction measurements could be performed.

In order to measure IV and dI/dV, a probe station was used at cryogenic temperatures of 77 K. These measurements showed clearly a broad dip and a shoulder in dI/dV, which reflects results obtained with STM in [10,11,12]. When the gate voltage was varied, the broad dip remained pinned to the Fermi Level (width $\sim$ 120 mV, in close agreement with V. Brar in [10]) whereas the small shoulder shifted as a negative and positive V_g was applied. According to previous literature, the local minimum can be identified as a band structure feature of graphene i.e. the Dirac Point. Additionally, the static gap (broad dip feature) in conductance is associated to inelastic tunneling processes and agrees with the phonon gap of STS measurements shown in recent literature.

Finally, when the shift of the local minimum was plot against the V_g an inconclusive relationship was found. The data seem to follow the square root of V_g-dependence covered in the Theory section, but a possible linear relationship can also be found. These results may lead to believe that the probed sample was not monolayer graphene but rather some thicker stacking of graphene layers [17].

Future work could replace graphene by any other thin layered material to study its electronic structure. Additionally, we can use these devices to study graphene's (or any materials') properties under high magnetic fields ($\sim$ 45T) and low temperatures using helium instead of nitrogen ($\sim$ 25 mK). This poses TFET devices as an advantageous option relative to STM, where experiments cannot be performed under such conditions. However,

the power of STM creating topographic images of the sample cannot be achieved with the construction of TFET's. Thus, these devices are a great complement to the electronic study of 2D materials and perhaps, a step towards fabrication of commercial transistors using graphene as a silicon replacement.

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