LUND UNIVERSITY
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GaN-nanowire as probe for scanning tunneling microscopy

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Acknowledgment
All praises are due to Allah and Allahs blessings be upon his final messenger Muhammad (SAW) and his pure family (AS). I would like to say thank you to my parents who have always supported me in my decisions, Love you! I would also like to express my heartfelt thanks to my supervisors, Anders Mikkelsen and Sofie Yngman who helped me throughout my thesis in every steps.

Contents

Table of acronyms
STM Scanning tunneling microscopy
STS Scanning tunneling spectroscopy
SEM Scanning electron microscopy
GaN Gallium nitride
Au Gold
Pt Platinum

Abstract
Scanning tunneling microscope (STM) has in recent years been one of the most used microscopy approaches in surface science. The STM probe allows for the investigation of atomic resolution electrical properties of a material, these probes are usually of metallic characters. In this project efforts have been made to investigate how good semi-conducting materials are as scanning probes. GaN-nanowires are used as probes for scanning tunneling microscopy, where a single GaN-nanowire was positioned on top of a tungsten tip, using a nanowire manipulator.
In this thesis Au(111) was scanned and we achieved resolution of atomic layers on Au(111) surface. Scanning tunneling spectroscopy measurements were performed showing the semiconductor nature of the tip.

1 Introduction

Scientists have always been interested to see objects that are not possible to see with our eyesight, these objects are either far away or too small to observe. Through out the history, telescopes and microscopes, one with more complicated and better function than the other have been invented. Scanning tunneling microscopy has allowed for investigating materials ranging from conductors to semiconductors, a direct contact between the scanning tip and the sample is avoided due to tunneling which is a major advantage. Different approaches have been made towards using semiconducting nanowires as scanning tip, although the approach in this thesis, is unique since only one nanowire is used as scanning probe. In recent years nanowires have revolutionized the world of electronics, these semiconducting materials are widely used in all technology, e.g. in our cellphones. Using nanowires, allows for investigating the electrical and mechanical property of the semiconducting material and also one can confirm how good these materials are as scanning probe. In this thesis GaN-nanowires were used as scanning probes. Using GaN-nanowire as probe, one combines fields of Nanotechnology and Material science and it opens the door for more research. It allows to preform experiments which one would not be able to if a metallic tip was used. Experiments such as scanning approach with semiconducting tip on surface of a semiconductor or scanning with presence of a laser would have been very interesting. STM also contributes in determining the design of the GaN-nanowire. These nanowires are grown in two steps, in step 1, the GaN-core is grown and in step 2, one grows an underlayer around the GaN-core. By performing STM/STS measurements one can determine how good the GaN-nanowires electrical and mechanical properties are. One can also contribute in the growth of these wires using STM, where different GaN-nanowires of different shapes can be used and investigated. So, using GaN-nanowires are not only good for STM/STS measurements one can also gain an understanding about the nanowires that are been used. In future one can use different semiconductors as scanning probes in order to determine their mechanical, electrical properties and also to make an effort in designing these nanowires in order to become a good candidate for these type of measurements. [11]

2 Scientific Background

In order to gain an understanding about the thesis, in the theory section I will explain different areas that will be mentioned further in the thesis.

2.1 Semiconductor materials and Nanowires

Semiconductor materials have in recent years been one of the most interesting fields of research and technology, due to its extensive use in more or less all electronics. The lattice spacing in the crystalline structure of semiconductor materials provides valuable properties such as controllable electrical conductivity, which separates these materials from conductors and insulators [1]. The crystal structure of semiconducting materials are built up by bonds between atoms or ions [1]. Each bond gives rise to localized energy states occupied by electrons. Having a cluster of atoms creates a chain of these localized energy states, one calls these chains valence band and conduction band. The separation between the valence and conduction band depends on

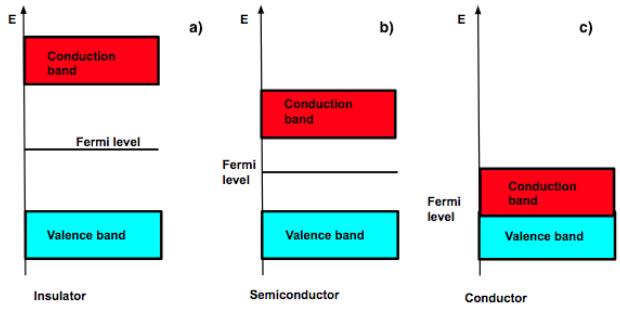

Figure 1: a) The energy gap between the valence band and conduction band indicates how good of a conductor a material is, in the case of insulators the energy gap is large therefore the amount of energy for exciting electrons up into the conduction band has to be in the same order. b) For materials to be indicated as semiconductors the energy gap must be < 3eV. c) Metals are typical conductors where no such energy gap is available, and therefore the smallest change in energy can excite an electron up to the conduction band.

the type of material, see Figure 1. Fermi level indicates the highest occupied energy state, where in Figure 1(b), it is positioned in the middle of the energy gap for intrinsic semiconductor. Probability of occupied energy states are given by the Fermi-Dirac distribution function [3]:

$$f(E,T) = \frac{1}{e^{(E-E_F)/k_BT} + 1} \qquad (1)$$

Where E_F indicates Fermi-energy and k_B the Boltzmann constant. For temperatures, T = 0, the probability for occupied states below the Fermi level is equal to 1 and for states above the Fermi level is equal to 0, this indicates that all energy states above the Fermi level, it is empty while all energy states below the Fermi level is occupied.
The density of states is given by :

$$g(E)dE = \frac{V}{2\pi^2}(\frac{2m_e}{\hbar^2})^{3/2}E^{1/2}dE \qquad (2)$$

Eq.2 describes the number of available states per energy interval dE, combining and integrating (1) and (2) results in the total number of electrons [3]:

$$N = \int_0^\infty g(E)f(E,T)\ dE$$

2.1.1 Intrinsic semiconductors

As shown in Figure 1, the Fermi level lies in between the valence band and conduction band for semiconductors, where the density of states is zero. Assuming that the Fermi-energy lies very close to the valence band results in less occupied states in the valence band and even fewer occupied states in the conduction band, which gives rise to a positively charged solid. Such a situation violates charge conservation and is unphysical. [3]

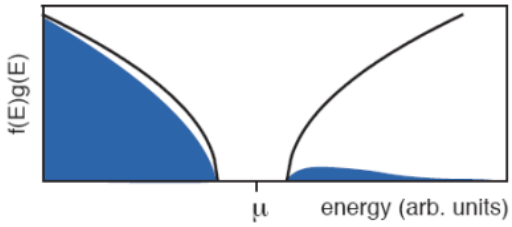

Figure 2: Illustration of unoccupied and occupied states in respective band. Observe that the Fermi energy is in the middle of the gap.[7]

Therefore at a finite temperature the Fermi energy must lie in between the valence and conduction band (see Figure 2) in order to have an equal number of missing electrons and holes. Such a behavior can only be observed for intrinsic semiconductors (undoped semiconductors). [3]

2.1.2 p-type and n-type semiconductor

Attempts are made towards changing the electronic properties of a semiconductor, one can exchange some of the atoms in the crystal lattice with atoms with more or fewer electrons in their valence shell. This process is known as doping. There are two types of semiconductors, p-type and n-type. P-type semiconductors have higher concentration of holes than electrons, this is due to higher doping of holes. A p-type semiconductor is created by doping an intrinsic semiconductor with acceptors leading that the higher majority carriers are holes, and the minority carriers are electrons.
n-type semiconductor is the opposite of a p-type semiconductor. In an n-type semiconductor there is a higher concentration of electrons than holes, such a semiconductor is created by doping an intrinsic semiconductor with donors, which makes the electrons the majority carriers.

2.1.3 p-n junction

A p-type semiconductor and a n-type semiconductor being sandwiched together results in a p-n junction. In a n-type semiconductor there is a large concentration of electrons, therefore the Fermi level lies close to the conduction band and in a p-type semiconductor there is a large concentration of holes, and the Fermi level lies close to the valence band. [2] Whenever junction is achieved, there is a diffusion of electrons from the n-side to the p-side and a diffusion of holes into the n-side. The diffused electrons from the n-side leave behind ionized donor atoms which results in a positively charged n-side, while the holes from the p-side leaves behind charged acceptor ions which results in negatively charged p-side. The region in between the n-side and p-side is called the depletion region where there is a concentration of both ionized donors and ionized acceptors. [2]
Connecting the p-n junction to a battery where the positive terminal of the battery is connected to the p-side and the negative terminal is connected to the n-side, one says that the junction is under a forward bias. Applying a voltage to the circuit, the electrons will flow into the p-side and electrons will flow into the n-side.The size of the depletion region will decrease as some of the additional carriers leaves uncompensated ions in the depletion region, and this cause large diffusion current of majority carriers to flow, see Figure 3(a). Electrons diffuse from the n-side to the p-side and a current is created as they reach the other side of the junction and diffuse. This can be illustrated by studying the relationship between the current and voltage, see Figure 4(a).The reversed bias indicates when the positive side of the battery is connected to the n-side and the negative side of the battery is connected

to the p-side. For a current to be created, the so called reversed current, the electrons must flow from the n-side to the p-side and holes needs to flow in the opposite direction. The size of the depletion region increases as the number of acceptors and donors increases. The height of the potential barrier increases (see Figure 3(b)) due to the increased size of the junction voltage and no current flows through the junction. The reverse current is so small due to few minority carriers present.[5] Figure 4(a) can be compared to the current-voltage characteristic of a conductor, see Figure 4(b), one can see that the IV relationship for a conductor represents a linear I-V relation between the current and the voltage, where V indicates the voltage and I indicates the current. The relation can be described by Ohms law where $R = V * I$ where R indicates the resistance. The resistance in the conductor is due to collisions between free electrons and ions in the lattice.

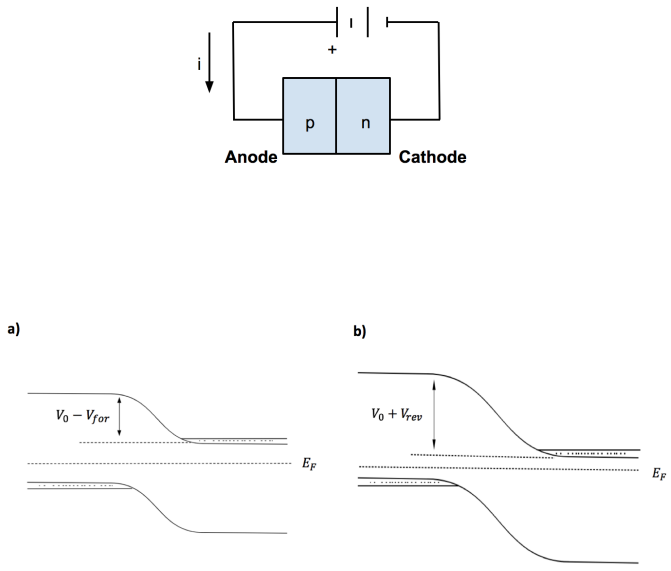

Figure 3: a) When a reversed bias is applied the height of the potential is increased and less carriers can make it over the potential. b) As a forward bias is applied the length of the depletion region decreases and more charge carriers can flow.

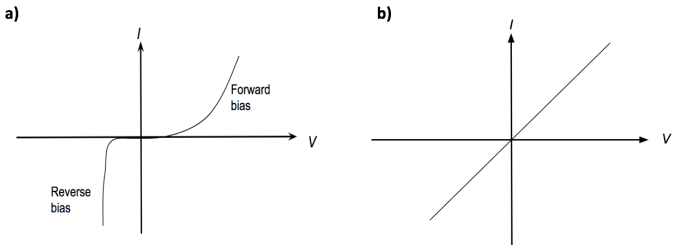

Figure 4: a) IV-curve for an semiconductor. b) IV-curve for a metal.

2.1.4 Gallium nitride (GaN)

Gallium nitride compound is a combination of Ga atoms,(eg. group III) and N atoms (eg. group V). GaN is the III-V of semiconductors with a bandgap of 3.4 eV making it the semiconductor with the second largest bandgap, the semiconductor has high heat capacity and thermal conductivity.[17] The compound of GaN is very hard and it has Wurtzite crystal structure, see Figure 5.

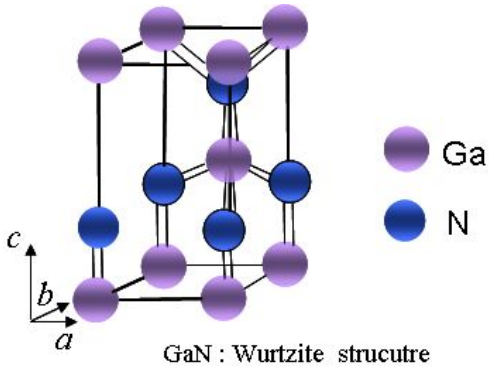

Figure 5: The unit cell of the GaN. Taken from ref[19]

2.1.5 Nanowires

The so called nanowires are long and rod shaped crystalline objects. These objects often have lengths the in micrometer range and diameter in the nanometer range.[20] There are several methods for growing nanowires, the two main methods are molecular beam epitaxy(MBE) and metal-organic vapor phase epitaxy(MOVPE). In this thesis the method MOVPE was used for growing n-doped GaN-nanowires, see Figure 6.[4]

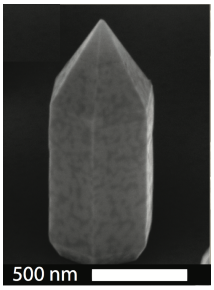

Figure 6: A single GaN-nanowire

2.2 Tools

2.2.1 Tunneling

Considering two closely spaced semiconductors with separation d and a potential barrier see Figure 7(a). The height of the potential barrier is qV_0, if the electron energy is much less than this height the electrons will go through the barrier from the left to the right semiconductor, this process is know as quantum tunneling. Assuming the classical situation when an electron approaches the barrier, if $E < qV_0$ the electron is reflected after hitting the barrier, although in the quantum case there is a probability for the electron to tunnel through the barrier. Looking at Figure 7b, at $qV(x) = 0$ the behavior of the particle can be explained by the SchrÃűdinger equation [6] :

$$-\frac{\hbar^2}{2m_n}\frac{d^2\psi}{dx^2} = E\psi \qquad (3)$$

Solving 3 gives us the solutions:

$$\psi(x) = Ae^{jkx} + Be^{-jkx} \qquad x \leq 0 \qquad (4)$$

$$\psi(x) = Ce^{jkx} \qquad x \geq d \qquad (5)$$

where $k = \sqrt{-2m_nE/\hbar^2}$. There is a reflected and an incident wave function for $x \leq 0$, and a transmitted wave function occurs for $x \geq d$. For the region $0 < x < d$ in Figure 9b, the following Schrodinger equation can be determined [6]:

$$-\frac{\hbar^2}{2m_n}\frac{d^2\psi}{dx^2} + qV_0\psi = E\psi \qquad (6)$$

and the following solution is given as $E < qV_0$ (7):

$$\psi(x) = Fe^{\beta x} + Ge^{-\beta x} \qquad (8)$$

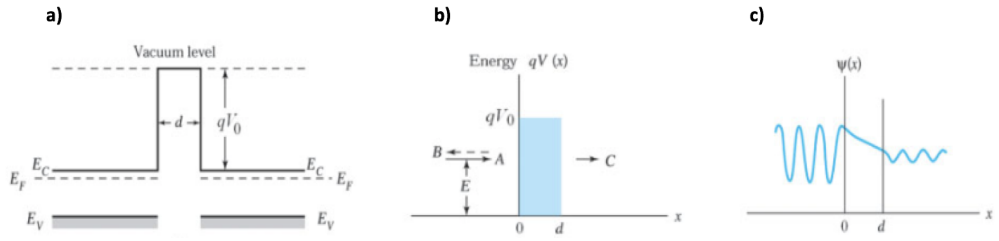

Figure 7: a) Two semiconductors brought together, where the potential barrier indicating distance, between them. In order for electrons to cross the barrier, tunneling is required b) In the classical situation the electron will never be able to cross the barrier if $E < qV_0$, although looking at the situation from a quantum mechanical perspective there will be a finite probability for tunneling through the barrier. c) Illustration of electron transmission through the potential barrier. Taken from ref [6]

where:

$$\beta = \sqrt{\frac{2m_n(qV_0 - E)}{\hbar^2}}$$

Figure 7(c), representing the wave function crossing the potential barrier, this transmission coefficient is given by [6]:

$$\left(\frac{C}{A}\right)^2 = \left[1 + \frac{(qV_0 sinh\beta d)^2}{4E(qV_0 - E)}\right] \qquad (9)$$

As the energy E decreases the transmission coefficient decreases and as $\beta d >> 1$ the transmission coefficient becomes very small:

$$\left(\frac{C}{A}\right)^2 = e^{-2d\beta} \qquad (10)$$

In order to achieve a finite transmission coefficient requirements such as small tunneling distance d, a small effective mass and a low potential barrier qV_0 have to be fulfilled. [6]

2.2.2 Scanning tunneling microscopy

Scanning tunneling microscopy (STM) is a powerful tool used for surface investigation and relies on electron tunneling. STM is widely used in fields such as, material sciences, chemistry and etc. At high spatial resolutions STM

provides 3D and real space images of surfaces. Using scanning tunneling microscopy one studies the tunneling current of electrons between the scanning tip and the surface of the material. The contrast in an STM image is given by local density of states. The scanning tips are usually metallic but efforts have been made towards semi-conducting materials. The important properties that needs to be achieved by semi-conducting tips in order to fulfill the requirements for usage as scanning tips are, desired electrical properties, mechanical stability and atomic resolution. [5] STM has two operational modes, constant current mode and constant height mode. In constant current mode, the current is kept constant but the distance between the tip and the sample can vary. The height is changed by using an electronic feedback loop and is controlled by changing the potential that is applied to piezoelectric actuator. A piezo electric material that converts electric field to mechanical strain is often used for controlling movements in nanometer region. [5] In constant height mode the current is varying while the height is kept constant. This mode is used for very flat surfaces otherwise the tip will crash into the rough surface. In this project we use constant current mode. [12]

2.2.3 Metallic tip on metal surface

The most usual approach to STM is to scan with a metallic tip on a metallic surface. Figure 8 represents three cases where one can describe the STM operation using this approach. Figure 8(a) shows a situation where no bias is applied, and therefore there are no trace of electron tunneling or current. By applying a positive bias on the sample one changes the direction of the electron tunneling, so that the electrons tunnel through the vacuum barrier from the tip into the empty sample states, this creates an electrical current in the opposite way, Figure 8(b). As one applies a negative bias on the sample**,** electron tunneling takes place, see Figure 8(c). Electrons from the sample tunnels through the vacuum barrier and occupying the empty tip states, there is also a electrical current created in the opposite way. [14]

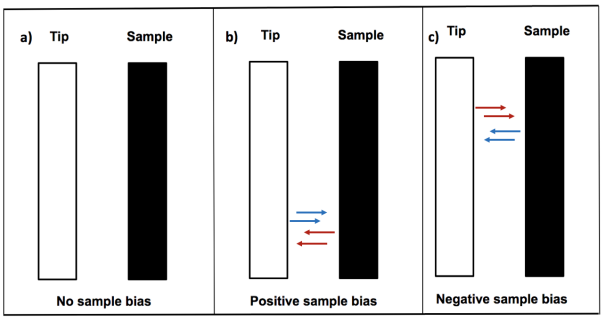

Figure 8: a) No sample bias applied, therefore no tunneling current. b) Positive sample bias applied, the blue arrows are indicating the electrons which are tunneling through the vacuum barrier and occupying empty states inside the metallic sample, the red arrows are indicating the flow of the electrical current. c) When a negative sample bias is applied the electrons occupy empty states inside the metallic tip.

2.2.4 Semiconductor surface and metal tip

Tunneling takes place between the tip and the sample, where there is a vacuum barrier that the electron can tunnel through. The induced tunneling current is exponentially dependent on the vacuum barrier width, this dependence is given by:

$$I_t = e^{-2\kappa d}$$

where κ denotes the inverse electron decay and is dependent on sample bias and d indicates the separation distance between the tip and the sample. The polarity of the sample bias is a casual property, this property determines the direction of the electron flow. There are three different cases to take into consideration, see Figure 9a, where there is no sample bias applied and no tunneling current or electron flow. In Figure 9b) a negative sample bias is applied where the electrons (indicated as blue arrows in the figure) tunnel from the valence band of the semiconductor through vacuum barrier and occupy the empty states in the tip. As a positive sample bias is applied electrons (indicated as blue arrows in the figure) from the tip tunnel through the vacuum barrier and occupy empty states inside the conduction band of the semiconductor, see Figure 9c).

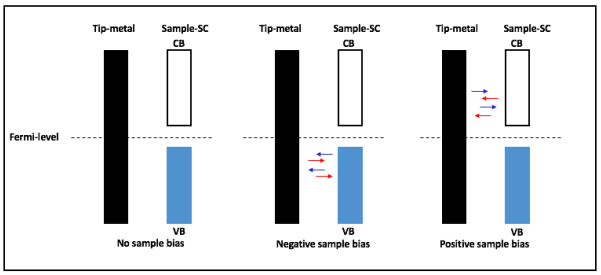

Figure 9: a) No sample bias applied leading to no current and no flow of electrons. b) A positive bias applied to the sample: a current is flowing from the sample to the tip leading to electrons flowing from the tip to the sample and occupying empty states in the conduction band. c) A negative bias is applied on the sample, a current is induced from the tip to the sample leading to electrons from the sample flowing to the tip, occupying empty states.[4]

2.2.5 Semiconductor tip and semiconductor surface

Using a semiconductor tip in order to scan on the surface of a semiconductor, makes this approach a bit more difficult than the previous approaches. In this case one has to make sure in order for tunneling to occur between the tip and sample, that there are indeed available states for the tunneling electrons to occupy. Otherwise the current set point will never be reached and the tip will crash into the sample. Here again three different cases are represented in Figure 10. When no bias is applied there is no tunneling taking place, see Figure 10(a), one can also obtain that the Fermi-levels are aligned. When a negative bias is applied to the sample, the valence band of the tip must become parallel to the conduction band of the sample. By doing so the electrons that tunnels through the vacuum barrier from the tip occupies the empty states in the conduction band of the sample. This displacement also gives rise to the displacement between the two Fermi-levels which were aligned when no bias was applied, see Figure 10(b). In order to perform STM measurements one has to calculate or estimate the distance between the two Fermi-levels, this is done by simply taking $E_{F_1} + E_{F_2} = E_{F_3}$. If a positive bias is applied, the conduction band of the scanning tip moves relative to the sample and becomes parallel to the valence band of the sample. In this case the electrons from the tip valence band tunnel through the vacuum barrier into the empty states in the conduction band of the sample giving rise to an electrical current in the opposite direction, see Figure 10(c).

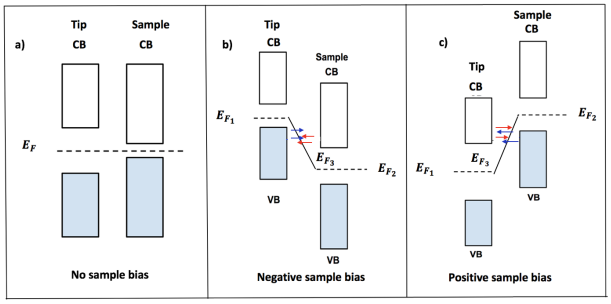

Figure 10: a) when no bias is applied, there are no electrons tunneling. b) A negative sample bias is applied to the sample, the blue arrows indicating electrons, tunnel through the vacuum barrier and occupy empty states inside the conduction band of the semiconductor sample. The Fermi levels are not aligned anymore. c) When a positive sample bias is applied, electrons from the valence band of the semiconductor sample, will tunnel through the vacuum barrier and occupy the empty states inside the valence band of the semiconductor tip.

Note that in highly doped semiconductors, a tunnel current can arise, and a reverse bias can be observed. This interesting effect is known as an Esaki diode and is part of the motivation of the work.

2.3 Scanning tunneling spectroscopy

Scanning tunneling spectroscopy is a method that is performed in order to measure electrical properties and gain information about the local density of states on the surface of the material. By stopping the scanning tip on a specified location on the sample the induced tunneling current is recorded for different voltages in that point and the result is represented as an IV-curve. [13] Studying Figure 11(a), three different regions on IV-curve is pointed out, region 1 (see Figure 11(b)) indicates a positive voltage on the sample, where the tunneling current is in the positive direction, region 2 (see Figure 11(c)) indicates a negative voltage on the sample, where the tunneling current is in the negative direction, and region 3 (see Figure 11(d)) indicates both positive and negative voltage where the current is zero.

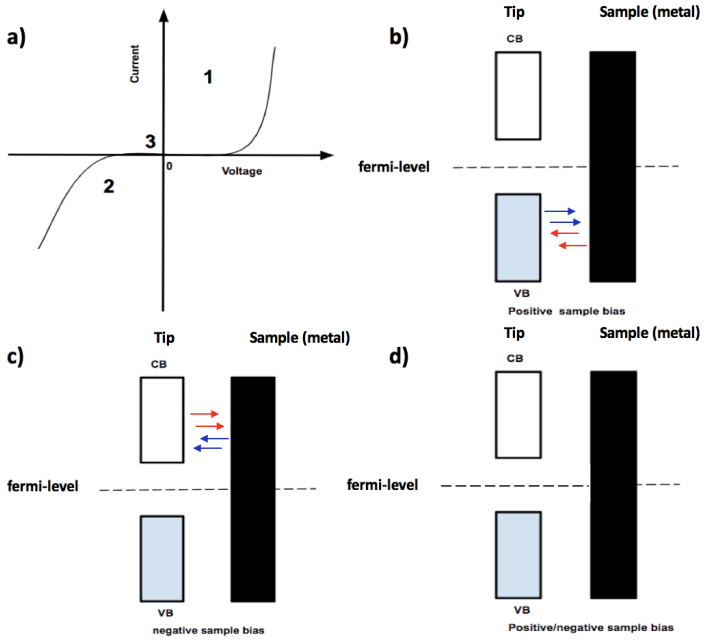

Figure 11: a) Illustration of IV-curve measured by preforming STS measurements. b) Representing (region 1) the behavior of the tip and the sample as a positive voltage is applied on the sample, the black arrows indicates the electrical current and the blue arrows indicating the electron tunneling. The electrons tunnels from the valence band of the tip to fill the empty states in the sample. c) As the voltage is shifted also the electron tunneling and electrical current flow is shifted (region 2). d) No tunneling and no electrical current, this indicates region 3 in Figure 11(a).

2.3.1 Tip induced band bending

Tip induced band bending is a consequence of when the metallic tip is brought close to the semiconductor surface. This procedure gives rise to formation of a metal-insulator-semiconductor junction, where the bands in the semiconductor are effected by the presence of the tip. Depending on different parameters such as the separation distance between the tip and the surface of the sample, carrier concentration, tip work function and the Fermi level of the tip and the sample the bands will bend in the semiconductor. [9,10]

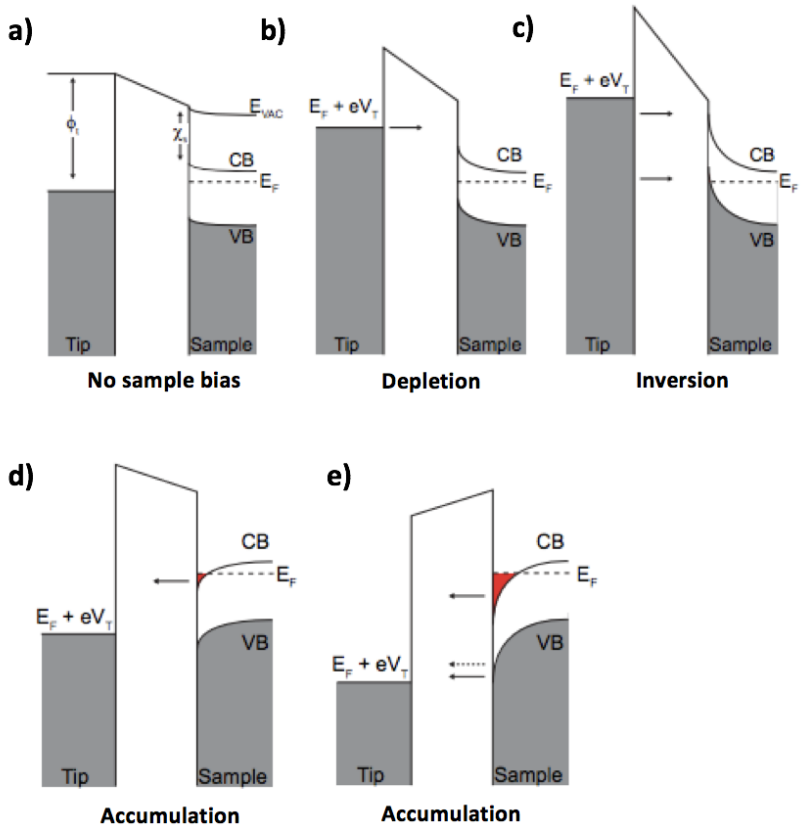

Figure 12: a) No sample bias. b) The bands are bend upward as one applies a sample bias. c) If the sample bias is large, the band are bended more giving rise to inversion. d) and e) the same yields as negative sample bias is applied, the bands are bend downward giving rise to accumulation.[18]

Two different cases can be studied, when a positive bias or a negative bias is applied. In the first case, where a positive bias is applied some of the bias will be dropped on the vacuum barrier and some will be dropped on the, see Figure 12(b). The amount of electrons at the surface will be reduced due to electrons from the tip occupying empty states in the conduction band of the sample. If the bias is large enough, the Fermi level will be positioned inside the valence band, this is called inversion. In the case of inversion the electrons will also tunnel into the valence band. The second case where a negative bias is applied, the bands are being bent downward, and there is an increment of electrons at the surface, this is known as accumulation, see 12d. If the negative bias is high enough, the Fermi level is positioned inside the conduction band and this opens up for electrons to tunnel the valence band

in the sample to the tip, see Figure 12(e). [4]

2.4 Scanning electron microscope

Scanning tunneling microscope provides images of samples, by using focused beam of electrons. By interaction between the electrons and the atoms on the surface information about the topography and composition of the surface is known.

3 Experimental method

Different experimental methods were used in order to preform use the GaN-nanowire as probe for STM/STS. In this section I will go through each method and describe the work that was done. I will also give a brief introduction on the software that was used during STM measurements.

3.1 Preparation of GaN-probe

Here we describe the procedure of manufacturing the GaN-nanowire probes. This is done in several steps. First the tungsten wire is etched. This will be used as the support for the GaN-nanowire. Then using a nanowire manipulator inside an SEM, a nanowire is transfered onto the tip of the tungsten wire. The GaN nanowire probe is then used as a probe in the STM. The different steps are described in more detail below.

3.1.1 Etching of tungsten wire

A piece of tungsten wire was cut and carefully mounted on an etching holder. An omicron tip etching control unit (see Figure 13a) was used, the voltage was set to V = 9.0 V, and the tip was dipped into a beaker containing NaOH solution for 20 minutes.

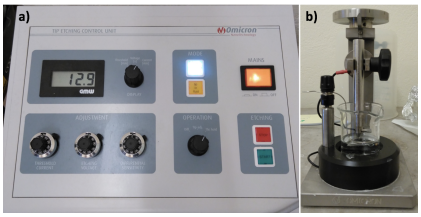

Figure 13: a)Unit control that was used. b) The etching setup, the beaker contains NaOH solution. The tungsten tip was dipped into the solution for 20 minutes while under influence of an induced current.

3.1.2 Nanowire manipulation inside SEM

The following procedure took place in the clean-room at Lund Nano Lab, using a Scanning electron microscopy (SEM). The tungsten tip was mounted inside an STM holder, the STM holder was in its turn mounted on a SEM holder and the substrate with nanowires on were placed inside the SEM. Using a control unit the holder inside the SEM was positioned underneath the electron beam, and an single nanowire was picked up by an ominiprobe, see Figure 13c and positioned on top of the tungsten tip, see Figure 13f. To further secure the nanowire to the tungsten probe beam induced deposition of Pt was used. In this procedure Pt molecules are introduced in the chamber and cracked under the electron beam. One can think of the Pt as a glue acting between the GaN nanowire and the tungsten probe.

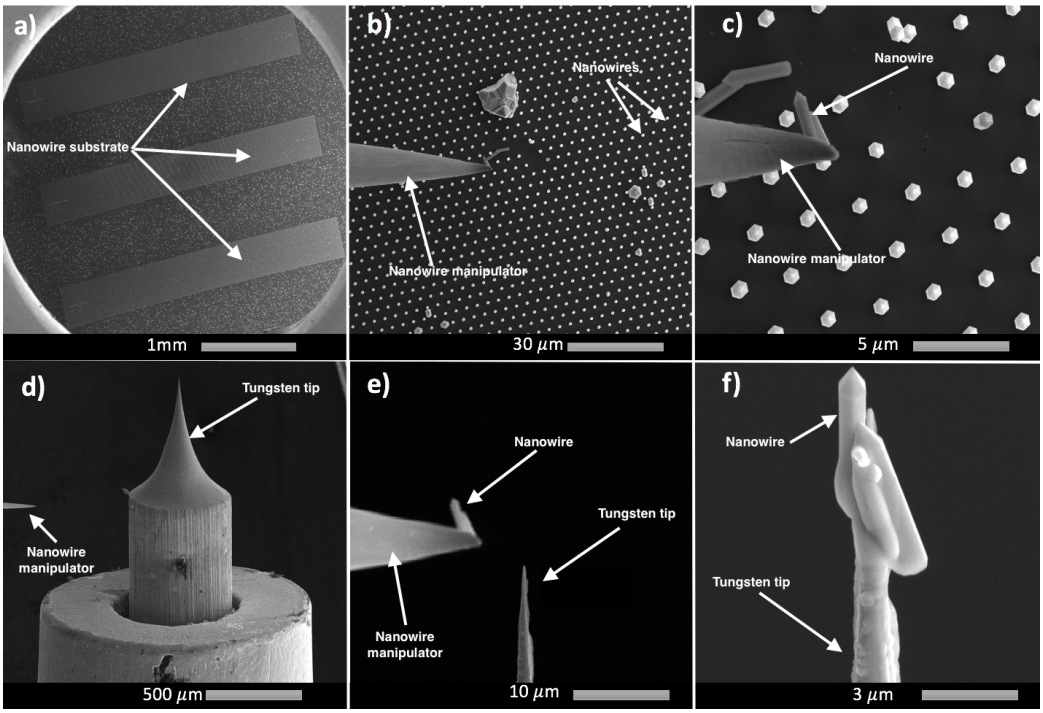

Figure 14: a) The substrate with nanowires on. b), c) Picking up a single nanowire using an ominiprobe, the wire is held by Van der waals forces. d) Approaching with nanowire manipulator towards the tungsten tip. e) Positioning the nanowire on top of the tungsten tip. f) The location where the nanowire was positioned on, was bombarded with Pt-source by this procedure the nanowire was "glued" to the tungsten tip.

3.1.3 Mounting of GaN-nanowire probe in STM

A variable temperature omicron XA STM was used. The device has three different vacuum chambers, load lock, preparation and STM chamber To transfer the tip holder inside the STM, the tip in its holder was positioned inside the load lock that is isolated from the preparation chamber by a valve. The air was pumped out from the load lock. The valve between the load lock and the UHV chamber was opened and the tip holder was positioned inside preparation chamber. Closing the load lock is crucial to make sure that the pressure inside the UHV chamber is stable 10^{-10} mbar. By using the transfer arm the tip holder was transferred into the STM chamber, by rotating the transfer arm 180° the tip holder was released and it was positioned on a transfer arm inside the STM chamber. A wobble stick used to transfer the tip holder from STM arm into STM device. Inside the STM, there is an STM head where the scanning tip is placed, this procedure is done using STM unit control, where the STM head can be moved upward, downward and in x and y direction. The STM head was moved upward to mount the scanning tip, when the tip was mounted the STM head was moved in x direction and moved downward to release the tip from the tip holder. The tip holder was transfered with the wobble stick and it was put inside the STM storing carrusel. Inside the storing carrusel the Au(111) sample was placed, and it was picked up with the wobble stick and transferred inside the STM, above the scanning tip with a separation in between. The last step of the process is to approach the scanning tip to the Au(111) sample, this procedure is also performed in two steps using the STM unit control. The first step one has to approach manually to move the scanning tip close to the Au(111) sample, keeping the scanning tip at a safe distance. The second step is by approaching automatically using piezo electronics where the current and voltage parameters are set using an omicron matrix software, the current set point was set to 40pA and the voltage was set to -3.4 V. The scanning tip approached the sample, and the rest of the experiment was performed using the omicron matrix software.

3.2 Software Omicron Matrix

To perform STM measurements the software omicron Matrix was used, see Figure 15a and 15b, where the Figures represents the window control of the software. In Figure 15a, the given numbers shows the parameters that are set in order to initiate the tip approach. To approach one has to set the parameters of voltage and current, where in Figure 15a, 1) represents the voltage, V-gap and 2) represents the current, I-setpoint. In this experiment

the voltage gap, V-gap = -3.4V and current-setpoint I = 40pA. The parameter loop gain allows the tip to be sensitive and react quickly to rough points on the surface, to prevent accident into the surface. As the tip approached the samples surface, the window in Figure 15b was used to set the different parameters. By adjusting the parameters the scanning area on the sample was set. In Figure 15b the numbers are indicating:

1. Points and lines, where one can decide how many points should be scanned upon and how many lines of these points. In this experiments the number of points was set to 100 and the number of lines was set to 100. This basically sets the resolution of the image.

2. Width and height allows to set a scanning area.

3. The scanning angle can be adjusted, this setting provides with different scanning angles.

4. By adjusting these parameters one can decide where on the scanning area one wants to scan upon.

5. The main window where the scanning can be initiated.

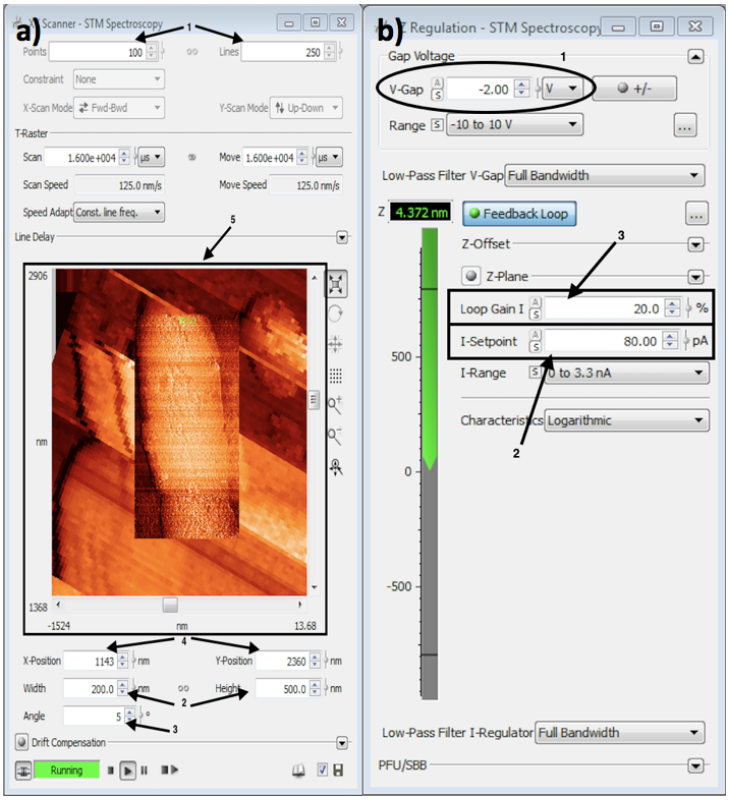

Figure 15: Omicron matrix window

3.3 Scanning tunneling spectroscopy measurements

Performing scanning tunneling spectroscopy the tunneling current between the GaN-tip and Au(111) surface was measured. To preform STS, the range of voltage was set to 4V to -4V, and the tip is stopped over a certain point and the tunneling current over the point was recorded. This was done over ten different point on the surface where each measurement contained ten different data sets.

4 Result

In this thesis four tips with nanowires manipulated on were made, where two of these tips gave result. Here the result from the SEM and manipulation of these two nanowires will be presented. I will also present the STM measurements where, atomic steps of Au(111) was observed. STS measurements where the tunneling current was recorded as a function of voltage and it will be represented as IV-curve.

4.1 SEM

Nanowires that were used in this thesis were grown in two steps. 1) the GaN-core was grown and 2) the underlayer was grown around the GaN-core. The difference between the two tips are the way the nanowires are mounted on the tungsten tip, tip 1 see Figure 16, the wire is manipulated on to the tip with the sharp side of the nanowire pointing outward. Although during STM approach we came across a problem regarding current flow through the wire, we concluded that the area between the GaN core and the underlayer is too small for the current to flow through to the tungsten tip. In Figure 16, we show the manipulation procedure of the first nanowire. Figure 16a the tungsten tip is shown and the wire is manipulated onto the most sharp point of the tip. The substrate with nanowires on is shown in Figure 16b where three spots are pointed by the arrows, on these spots nanowires are grown. By zooming in, over one of these spots, see Figure 16c, the nanowires can be seen. Using a nanowire manipulator, see Figure 16d, one single nanowire was picked up and it was mounted on the tungsten tip, see Figure 16e.[15] The second nanowire that was manipulated on the tungsten tip, was mounted with the other end pointing outward see Figure 18. We believed that the current flow will be more efficient due to the large area between the GaN-core and the underlayer.
After STM/STS measurements the scanning tips was further investigated in the SEM see Figure 17 and 19. In Figure 17, one can see that the structure of the tip has changed, this can be due to the voltage that was applied and caused the nanowire to lose atoms at the pointy side of the wire while scanning. Although scanning the nanowire mounted "upside down" on the tungsten tip, see Figure 19, one can see that there are no changes at all on the nanowire. This led us to suspect that the core is too bad of a conductor to quick the electrons from the pointy nanowire tip to tungsten wire.

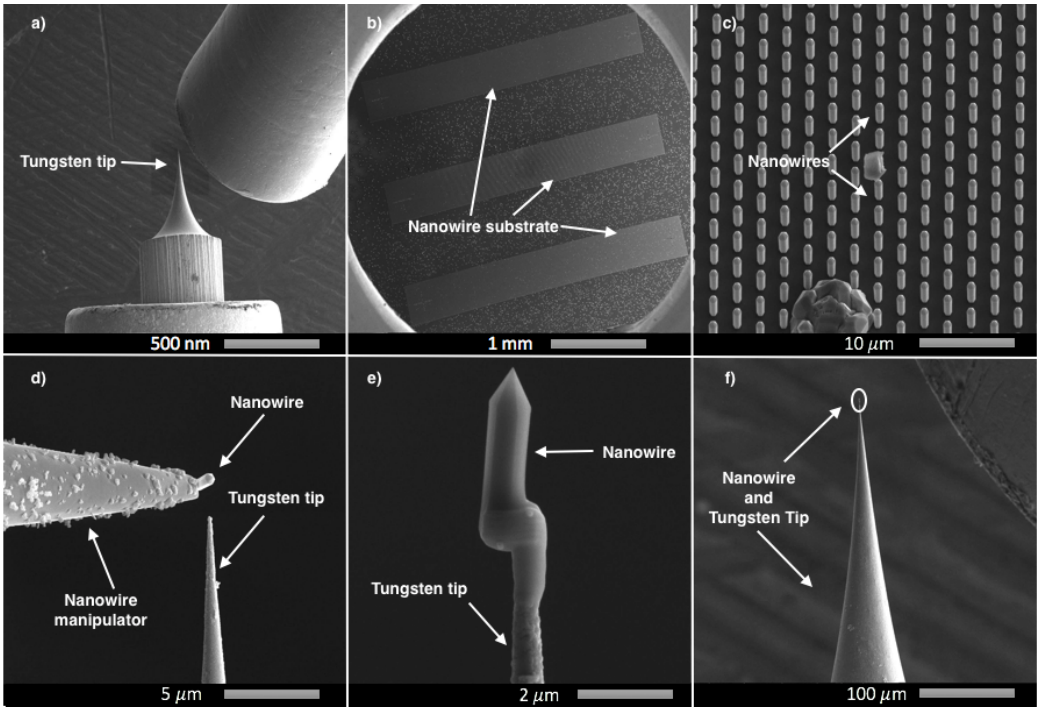

Figure 16: a) Tungsten tip before nanowire manipulation. b) Three layers are shown, on these layers the nanowires were initially grown. c) Showing single nanowires, we zoom on one of these layers. d) Using a nanowire manipulator one single nanowire was transfered and mounted on the tungsten tip. e) and f) Tungsten tip after nanowire manipulation.

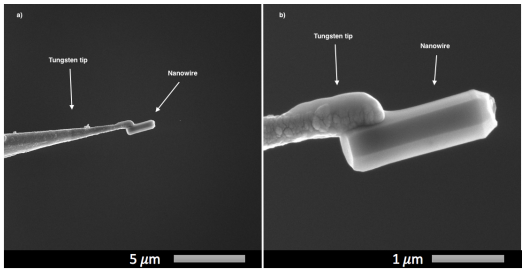

Figure 17: a) Nanowire after usage. b) A closer look at the nanowire after usage, one can see change in structure on the pointy side of the wire.

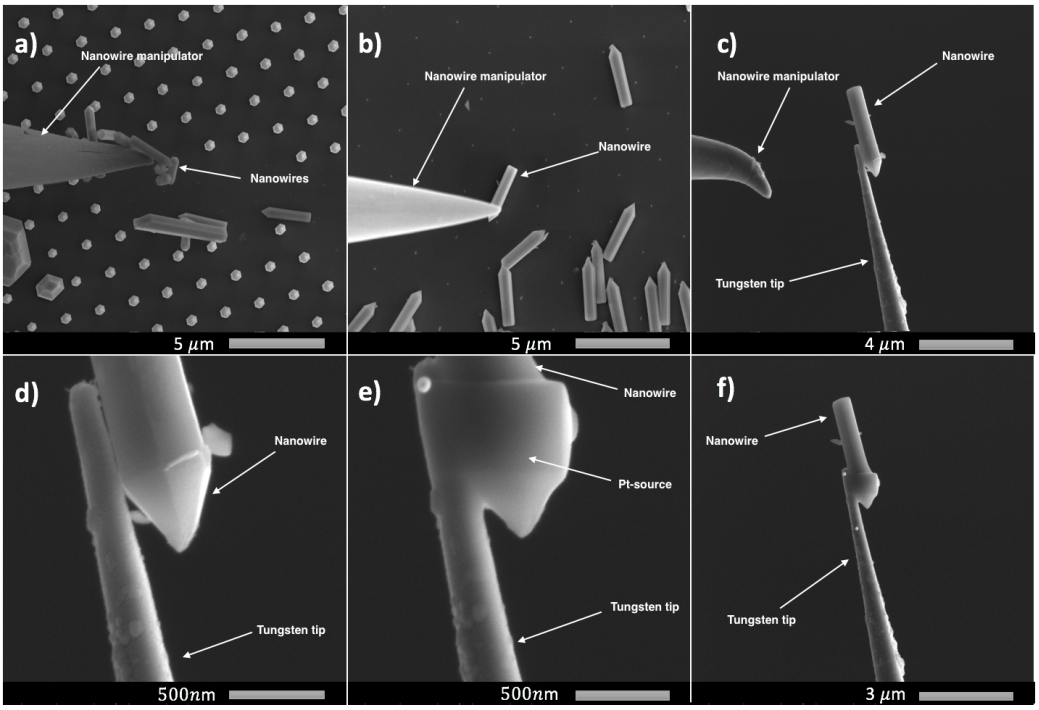

Figure 18: a) and b) Using a nanowire manipulator, one single nanowire was picked up. c) and d) The nanowire was mounted on the tungsten tip, this time with the other end pointing outward. e) Pt molecules were introduced inside the chamber and the the wire was glued to the tungsten tip. f) The tungsten tip after the nanowire manipulation.

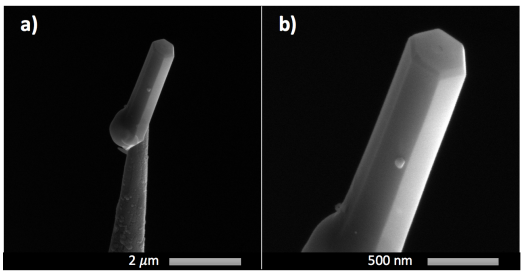

Figure 19: a) and b) Nanowire after STM/STS measurements

4.2 STM

The main purpose of STM, in this experiment is to measure the atomic steps between the atom layers of Au(111). Observing Figure 20, the atomic steps

of gold can be distinguished between a noise taking place between these steps, possibly due to an effect from the tip. In order to determine the distance between these layers, the software ImageJ was used. A straight line was drawn from one point where we estimated to be the lowest point on the surface to a point where we estimated to be the highest point, these lines are indicated as 1, 2 and 3 in Figure 20(a). The height between these points were calculated, and to achieve an accurate value the average of the three heights was taken. The average was calculated to $d_{exp} = 3.2$Å. Figure 20(b), these steps are imaged, the steps are indicates as 1, 2 and 3. The dark areas in Figure 20(b) are the lower steps, and the lighter areas are the area close to the surface.

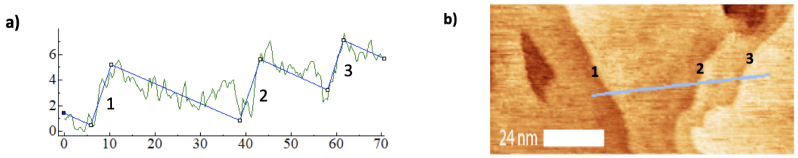

Figure 20: a) Spectrum over the surface of Au(111), three steps have been indicated. b) STM image over the Au(111) surface, the numbers are indicating the steps given in (a).

The atomic steps between atom layers in Au(111) can be calculated theoretically by preforming the following calculation. The structure of Au is known to be fcc, as shown in Figure 21. The two triangles are representing each layer. In Figure 21, d is the distance between the two layers and a is the lattice constant. The lattice constant a for Au is $a = 407.8pm$.[16] In Figure 21(b), the distance is shown by the triangle, and using this figure, we calculate d.

$$d_{theory} = \frac{1}{2}\sqrt{a^2 + a^2}$$

$$d_{theory} = 2.88\text{Å} \approx 3.0\text{Å}$$

Comparing d_{theory} and d_{exp} one can conclude that d_{exp} which is the experimental value of the atomic steps are close to the theoretical which was calculated above. We can conclude that the GaN-tip worked well as scanning probe for microscopy approach, although the noise observed in Figure 20(a), is due to the change in GaN-tip.

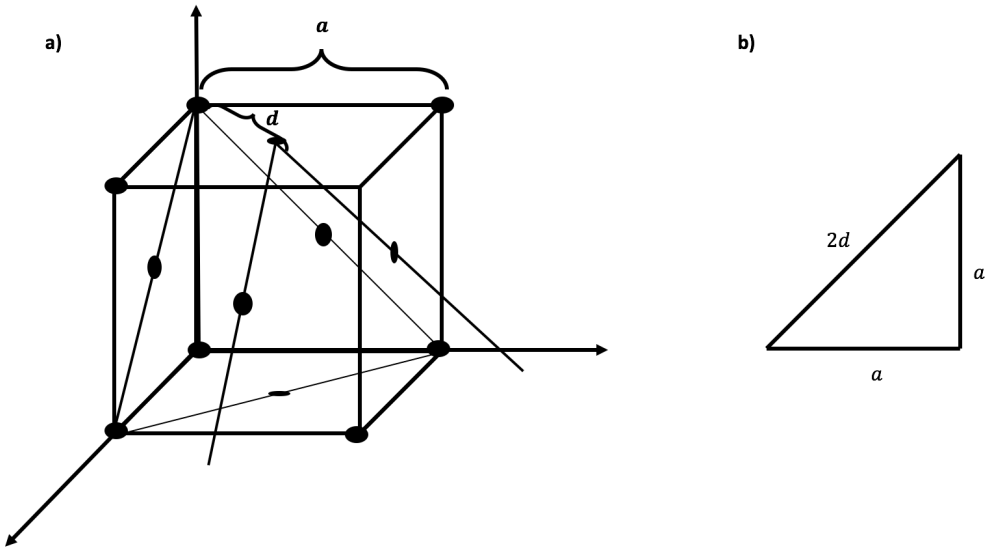

Figure 21: a) Fcc structure, a is indicating the lattice constant. b) Triangle indicating the distance between two atomic layers.

4.3 STS

The current vs voltage curve was plotted for three different measurements, see Figure 22a, 22b and 22c. Since we are scanning with GaN-tip we expect the IV-curve to have a semi-conducting behavior, meaning a region where there is no current recorded, the so called band gap. This band gap is expected to be 3.4 eV for GaN. [17] As we can see in current-voltage Figures below we obtain such a region in every plot. Theoretically the conduction and valence band edges should be linearly proportional to the voltage, although in Figures 22a, 22b and 22c, one can see that the proportionality does not exist, rather the conduction and valence band edges behave exponentially, this can be due to possible surface states. In order to calculate the no current region which indicates the band gap, the onset of valence and conduction band edges was linearly fitted using a fitting procedure described in [8], as one can see in Figures 22a, 22b and 22c. Calculating the linear fittings zero values, the bandgap for each curve was calculated. The following values for the bandgaps were calculated for each curve, $V_{gap1} = 5.88V$, $V_{gap2} = 5.85V$ and $V_{gap3} = 5.90V$.

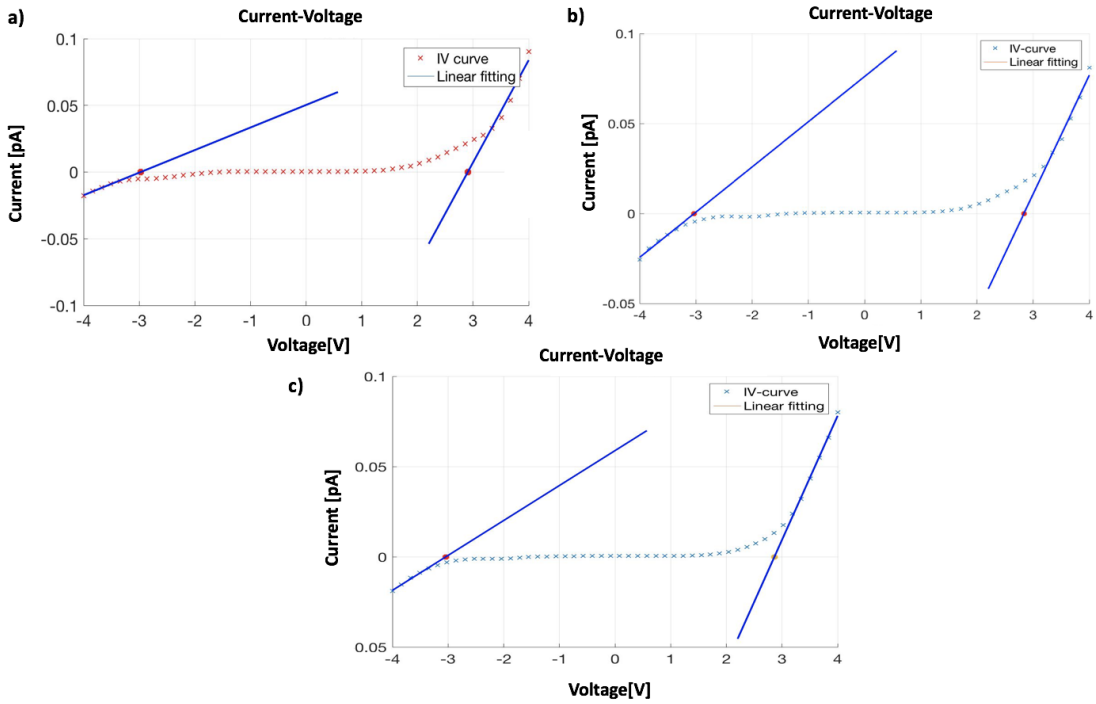

Figure 22: a), b) and c) Three different current-voltage curves with linear fitting at the band edges.

Studying Figures 22(a),(b) and (c) one can determine the location of the Fermi-level to be most close to the conduction band. By this we can indicate that the GaN-nanowire that was used as scanning tip were n-doped. One can also see trace of band bending in these figures, since the real band gap of the GaN is 3.4eV, this value does no match with the calculated values for the band-gap and are clearly larger. Performing STS the voltage applied was between -4 and 4 V. In the theory section we discussed that when a positive bias is applied some of the bias will be dropped on the sample and some on the vacuum barrier. In our case, the bias is dropped on the GaN-tip, leading to bands being bent upward meaning depletion and less states on the surface of the semiconductor. The electrons that tunnel from the sample to the tip, have less probability of occupying these states. Therefore although, when a negative voltage is applied the conduction and valence bands are bent downward, leading to more electrons on the surface of the CB and less electrons on the surface of the VB. This leads to less electrons from the valence band participating in the tunneling process therefore less electrical current is recorded as we can study from the Figures 22(a),(b) and (c) in the negative

voltage region.
Another approach to investigate the band edges is by looking at the $log(abs(I))$ and plotting it against the voltage, see Figure 23 where the same STS-data as above has been plotted. This makes the surface states much more clear to observe and one can have a better estimation of where the current is as smallest. The band edges were linearly fitted using a fitting procedure described in [8] in order to calculate the band gap The calculated values for the band gaps are, $V_1 = 2.84V$, $V_2 = 2.53V$ and $V_3 = 3.02V$ As one can see, there is a clear difference between the band gap of log(abs(I))-Voltage curve and the band gap of the IV-curve, despite the same data has been used. One can argue that the band gap calculated from Figure 23, should be wider. Although, due to possible surface states the band gap becomes smaller in Figure 23. This can be avoided by cleaning the surface of the GaN-nanowire.

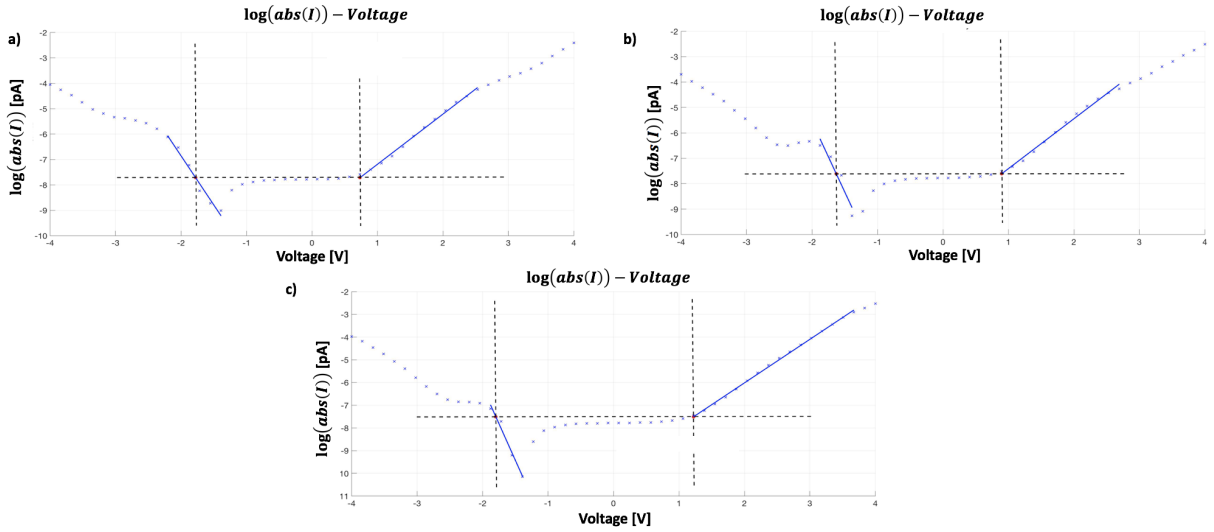

Figure 23: a),b) and c) Three different log(abs(I))-voltage plots with linear fitting at the band edges.

5 Discussion and outlook

The focus of the work in this thesis was to develop a technique of using GaN-nanowires as probes for scanning tunneling microscope, before I joined the group different techniques had been used. This approach was done by manipulating a single sharp grown nanowire on the top of a tungsten tip. The advantage of this approach was, that we actually scanned with a single nanowire and by doing this we could find the mechanical and electrical properties of the wire. Although there is a disadvantage, and that is that the wire could be lost after manipulation, so we had to be very careful. That first wire that was used as scanning probe, gave us no results after investigating the tip in the SEM we saw that the wire was lost, we believe that the reason was that as we were approaching the tip to the surface, the GaN-tip crashed into the surface of Au(111). We concluded that the GaN-core is a too bad conductor and hinders the electrical current to flow from the pointy nanowire tip to the tungsten wire. This conclusion was confirmed as we manipulated a new GaN-nanowire but with the other end where the passage area was larger, pointing outward. The end result was a perfect approach, so we conclude that the future GaN-nanowires should have a double underlayer in order to prevent any accidents with the surface of the material when STM is performed.

After performing STM and STS measurements with a new manipulated GaN-nanowire, the structure of the wire was changed. The change in structure led to noise in the STM spectrum. These noises observed are due to the GaN-nanowire tip not being sharp enough. The roughness of the surface caused different parts of the GaN-nanowire to take place in STM measurements.

The calculated value of the distance between the atomic layers matched well with the theoretical calculated value, by this we can conclude that the GaN-nanowire worked well for scanning probe microscopy, even though the roughness of the GaN-nanowire caused some noise in the spectrum. Although the deviation between the values can also be due to the way we estimated the lines of each layer in Figure 20a.

The STS measurements was shown in two different figures, where one represented the IV-curve and the other one represented the log(abs(I))-V curve. The band gaps from both curves was calculated and then compared to each other, the difference between the calculated values was very large. Where in log(abs(I)) the band gaps was found to be smaller than the one calculated for IV-curve. The reason for IV-curve having a large band gap can be due to the linear fitting on the band onsets where not all of the surface states was not included in the fitting. Another argument over the log(abs(I)) can be that the band gap is too small for GaN-nanowire, this can be due to the

surface states on the GaN-nanowire and also the linear fitting of the curve. For reducing the amount of surface states, one can for instance clean the surface of the GaN-nanowire from oxides.
GaN-nanowire as probe for STM makes experiments such as STM on other semiconductors or experimenting with presence of a laser possible. These two experiments will be performed this time using a double underlayer grown around the GaN-core.
This kind of experiments opens up the door for using other semiconductors with different shape and properties as scanning probes.

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