

RF system for mmwave massive MIMO

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Abstract

Due to rapid developments in communication technology, it is likely that 5G networks will be rolled out in 2019. To adapt to 5G, hardware will have to develop to meet the requirements of this new technology.

The mmWave communication is one of the main elements of 5G technology. The mmWave frequency bandwidth is used to carry the data links and can achieve a higher transmission data rate than the current LTE system. There are few continuous frequency resources under 3GHz that can be allocated. As such, the International Telecommunication Union (ITU) and the 3GPP organization mutually agree that the mmWave is the most suitable option for exploring new frequency resources.

However, the mmWave has the one key weakness: high path loss for short transmission range. To compensate for this negative effect, a massive MIMO system can be used to have spatial multiplexing gains and array antenna gains. This article seeks a method that can acknowledge the fundamental concepts and requirements of the mmWave massive MIMO system, from both theoretical and practical perspectives. In order to find proof of the concepts, the practical limitations, and the guild of the real design, a prototype of the system has been built. The current industry standard when creating a prototype is to use PCB.

We will develop our system proposals from the prototype. To do so we use the evaluation boards to test system level performances such as link budget and identifying the most suitable components etc. Then in the PCB design, we integrate the radio frequency of the mmWave system. This has the scalability to collaborate with massive MIMO system test-bed to observe the system level performance.

Finally, to verify our methods, we carry out experiments on both component level and system level in order to identify the feasibility of the prototype system. The performance of each individual component is tested using an evaluation board. Separate tests are performed for both transmitting (Tx) and receiving (Rx) chains. Finally, over-air-tests are conducted at the system level to evaluate the performance of our design.

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List of Acronyms

3GPP	3 rd Generation Partnership Project
3/4/5 G	3 rd /4 th /5 th Generation
bps	Bits Per Second
CAD	Computer-Aided Design
DA	Driver Amplifier
DC	Direct Current
EIRP	Equivalent Isotropically Radiated Power
FDD	Frequency Division Duplexing
G	Gain
I/Q Mixer	In-Phase and Quadrature Mixer
LNA	Low Noise Amplifier
LO	Local Oscillator
MIMO	Multiple Input Multiple Output
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PCB	Printed Circuit Board
PL	Path Loss
PTFE	Polytetrafluoroethylene
QoS	Quality of Service
RF	Radio Frequency
Rx	Receiver
SMA	SubMiniature Version A
SMD	Surface Mount Device
SPDT Switch	Signal Pole Double Through Switch
TDD	Time Division Duplexing
Tx	Transmitter
USRP	Universal Software Radio Peripheral
VCO	Voltage Control Oscillator
via	Vertical Interconnect Access

CHAPTER 1

1 Introduction

In this chapter, the background of this project will be presented. In the first subchapter, the background of the current 4G technology and future 5G trends will be outlined. In the second subchapter, the printed circuit board technology with system requirements will be presented. Finally, the purpose of the projects will be described.

1.1 mmWave and Massive MIMO

Telecommunications have made great progress; right now it is moving towards its 5th generation (5G). As mobile vendors are looking to make 5G commercially available in 2019, the 3GPP organization has had a great effect on the development of the 5G standard. In the final days of 2017, the 3GPP successfully completed the first specification of 5G, which is one part of the Release 15[1]. This is huge milestone on the way to 5G.

The Release 15 contains two parts: Non-standalone (NSA) version and the Standalone (SA) version [1]. The first specification related to 5G of the Release 15 is the NSA version, and the SA version will be frozen in the second half year of 2018 [1]. The NSA version will continue to enhance and develop the current Long-Term Evolution (LTE) network and the radio (LTE Advanced Pro) specifications. Meanwhile, the 5G carrier will be introduced. The SA version implies a full system architecture network with full user and control plane abilities [1]. The Release 15 is aiming to utilize and optimize the current LTE system, so as to use it as the main part of the 5G network. There are five essential inventions in the Release 15:

- (i) Massive MIMO: (Multiple-Input Multiple-Output) the extension of Multi-user MIMO: high capacity and coverage by supporting large numbers of the antennas in the antenna array.

- (ii) mmWave (millimeter waves): extremely high frequency band to achieve high data throughput.
- (iii) The Advanced Channel coding: CA-Polar code for Enhanced Mobile Broadband (eMBB) control channel for 5G new radio interface and ME-LDPC (Multi-Edge LDPC) for data channel. Both codes provide reliable transmissions and can support large data transmission.
- (iv) The scalable OFDM methodology: This technology can provide high spectrum efficiency, low complexity in the receiver, and low energy consumption etc.
- (v) The self-contained slot structure: low latency, high flexibility and compatibility [2].

For this project, we are working with the first two technologies of the Release 15: Massive MIMO and mmWave. We are targeting the electronic circuits design for the 5G radio frequency subsystem to support mmWave data transmission.

The reason we are accessing the mmWave frequency resources is that frequency bandwidth resources for less than 3GHz are becoming scarce; right now it is hard to find new frequency bandwidth resources for the 5G system below the 3GHz frequency spectrum. Therefore, we are aiming at a higher frequency spectrum: the general 5G NR mmWave frequency range is between 24 GHz-100GHz. 10GHz to 30GHz is also included since it has similar propagation characteristics [3]. The investigation results show that the frequency range between 26.5GHz and 40GHz (Ka-band) is more suitable for outdoors-to-outdoors communication [4].

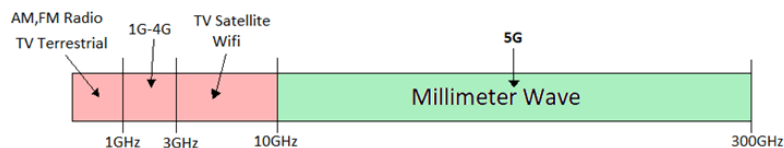


Figure 1 Frequency Spectrum Allocation and Its Usages

In Figure 1 we present the current frequency spectrum allocation and how it is being used. Between 1GHz and 3GHz of the frequency spectrum is distributed for 1G-4G cellular communication use (there are some frequency bands occupying below 1GHz as well). In the frequency below the 1GHz we have: AM (Amplitude Modulation) and FM (Frequency Modulation) for radio broadcasting, radar, and terrestrial TV etc. Above the 3GHz but below the 10GHz, there is TV satellite, WIFI etc. For the frequency spectrum over 10GHz, there are much wider bandwidth resources available and less occupied usages. This means mmWave is optimized for 5G as the new mobile communication system.

In the extremely high frequency part of the spectrum, we have high availability to allocate from and achieve high data transmission speeds, up to Gbps on the large bandwidth. There is high network capacity due to the dense spatial reuse. However, when comparing the current mobile communication system to the low frequency band, there are some shortcomings: the mmWave has a shorter signal transmitting range, which means it travels mostly in the line of sight. The increased propagation loss (for example, 90dB path loss over 30m on 28GHz) [5] is problematic, as well as the susceptibility to physical obstacles like buildings, walls and foliage etc. Furthermore, for everyday use for mmWave devices, we also need to consider a hand-sized device, of low complexity for mobile architecture, with low power consumption.

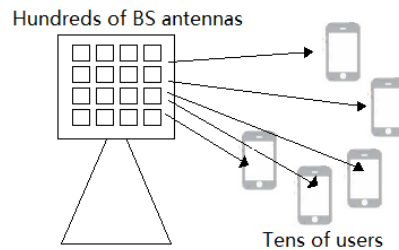


Figure 2 Massive MIMO Example System

In Figure 2 we present an example schematic of a massive MIMO system. The base station has an enormous number of antenna elements in the antenna array, which can serve tens of users simultaneously whilst providing a good quality of service.

To compensate for the inherent disadvantages of mmWave, we need to find some solutions to combat these negative factors. The Massive MIMO is an excellent solution that collaborates with the mmWave. Massive MIMO refers

to multiple data transmissions simultaneously including transmitting and receiving over the same radio channel. As the name would suggest, the massive refers to the number of the antennas in the antenna array. For a general MIMO system, we usually use 2x2 or 4x4 antenna numbers [6]. As for the massive MIMO, there is a specific MIMO case for massive antennas elements in the antenna array. The key benefits we can obtain from the MIMO system are:

(i) Spatial multiplexing: Transmitting the encoded data signals (streams) from each independent and separate transmit antennas. Hence, the space dimension is multiplexed multiple times. The enormous number of antennae elements could deliver the spatial multiplexing gains to compensate for the mmWave path loss and is lower down the radiated power requirements (the number of streams rising the data rates and system capacity etc.).

(ii) Precoding: supporting different signal beamforming to different users. By applying some weight on the transmitting side signal, beamforming can deliver a high receive gain on the receive side. This strategy reduces the channel fading effect, raising the channel capacity and coverage.

In summary, the massive MIMO has high spectral efficiency and a low energy consumption [7]. In general, the combination of mmWave and massive MIMO has the potential to improve the performance of communication data rates [3].

Based on the characteristics of the 5G system, an exclusive prototype of the radio frequency (RF) mmWave massive MIMO system needs to be designed. The performance of the prototype will be evaluated to make sure that it has met all the requirements for the future 5G communications.

1.2 Prototype and Printed Circuit Board

1.2.1 Importance of Prototype System

So far, we have outlined two essential technologies in the previous subchapter: the mmWave and the massive MIMO. To understand the theoretical concepts behind these technologies is essential to this project. As well as understanding the theory, we need to look for some means to combine these technologies together and make them collaborate in order achieve our goal. We

need to realize these theoretical conceptions and verify them. This realization method is achieved by building a prototype in order to transition from theory to practice. A prototype is a significant part of the procedure to verify the results before we move to manufacture. The benefitions to build the prototype are [8]:

- (i) **To acknowledge the theoretical standpoints.** In the early stage of building the prototype, we need to completely understand the theoretical points of view: what kind of electronic components do we need to use, how can we connect them properly? As the primary phase of prototype construction, it is very important to design a suitable system architecture, which contains all the required features. Then we need to verify if the theoretical conceptions have been satisfied in practice. A prototype is a method to implement the theories, which we can evaluate and verify. Based on collected measurement data evaluations, we can then adjust and improve the initial proposals in order to make it more suitable for the system requirements.
- (ii) **To acknowledge the physical/practical standpoints.** Not only do we need to understand the fundamental concepts, but also, we need to consider some hardware/commercial aspects. In general, the prototype performance always deviates from the theory. Moreover, there are many tangible elements that need to be considered when the engineers design the prototype. For physical consideration: the best material choice for prototype, thermal management for temperature-sensitive components, the physical placement of the prototype in case of interference etc. These factors will also affect the prototype's performance. While we are building the prototype, we need bear these factors in mind.
- (iii) **Shorten the turnarounds/less time consumption/less expenditure [9].** Nowadays, engineers are able to utilize computer software to aid them in prototype design, and this is a great convenience. We can build the virtual design in hours or days and it is easy to edit our initial design anytime and anywhere, once we receive the measurement feedback. Compared to the old way of manually connecting the components together, prototyping saves time; especially when the circuit complexity rises. If we skip the prototype step and manufacture the product directly, it is obvious that making changes to rectify the deviations in the final product will be hard (even more so when you

have a large quantity of products). It will take too much time and also drive up expenditure. Therefore, it is important to have an approved prototype before making any products.

In general, a prototype is the proper method to simulate the performance. This approach will bring out any inconsistencies (improper operations and errors) during the design construction. The discovery of inconsistencies will catch the attention of the engineers and seek the best solution to the problem. By developing a prototype, we can demonstrate the functionality, which can help the engineers to solidify requirements and finalize the design

As for the individual work of the prototype, the mmWave already has many mature applications for satellite and radar. One example is that the authors have made one mmWave antenna PCB for research study. A wideband mmWave antenna element of which the aperture region is approximately 0.2 mm by 5.0 mm, operational frequency from 18 GHz to 40 GHz, and achieves 10 dB receive gain at broadside between 32 GHz and 38 GHz [10]. As for the massive MIMO area, it already has some successful prototypes such as LuMaMi in Lund University, the world's first real-time testbed for massive MIMO. It was designed at 3.7 GHz, 10dB bandwidth of 183 MHz and 160 dual polarized patch antenna array elements [11].

However, in this phase, there is very little existing work that we can reference for the mmWave massive MIMO system. The mobile mmWave is a new era of communication that has just started; there is no state of the art simulation system model that we can take as an example. Therefore, we neither have the hardware device model nor the transmission measurements of the channel effect. So, there is only one way we could discover these elements: to build a prototype and run over air tests to harvest the measurement data then we can use to evaluate system performance. Prototyping also has another benefit in that it flags potential issues to developers who can build upon our work to create more advanced prototypes.

In the electronic industry, the conventional method to build the prototype for RF subsystem is with printed circuits boards (PCB). Engineers use computer aided design (CAD) software to manage the mass circuit distributions and the physical layouts while the system manufacturing and assembly will be automated. At the last stage, the components will be mounted on it. PCBs can be duplicated easily, allowing high volumes to be produced at the same time.

1.2.2 RF PCB Design

In this instance we would like to design an extremely high frequency transmitting and receiving system on the PCB. The PCB should have a small area with a compact circuit design, which is mounted by micro-size electronic components. This mounting technology is called surface mount technology (SMT) and the mounted electronic components are called surface mount devices (SMD). In general, these SMDs are the resistors, capacitors, or other active devices like LNA (low noise amplifier), PA (power amplifier), and mixer etc.

The SMD contains the conductive pad and electronic components packages and is connected by conductive tracks or wires. The components are then mounted on a copper layer sheet on the non-conductive substrate. PCBs may have different layers: single (single side or double side) layer or multiple layers. To transmit through the different layers we use through, blind, or buried vias to connect. In the case of this extremely high frequency and high intensity component design, we are using four layers: top layer (layer 1), ground layer (layer 2), power layer (layer 15) and bottom layer (layer 16).

This PCB design contains multiple layers for 5G mobile hardware, which will require even more accurate placement in such a compact area. This is necessary to adapt to the different properties and technologies, so as to deliver a high quality of service. In this area there are some fundamental principles to take note of. Firstly, all the circuit components should be unified and matched to 50 Ohms unless any other specific demands are proposed. Secondly, no wires may cross paths in the same layer. Thirdly, less length of connection and straight or 45-degree wire connections are recommended for less transmission losses etc. In order to have satisfied the circuit architecture with the minimum negative effect factors, there are some considerations during the design as well: the phase shift, impedance mismatch, power gain calculation, and budget [9]. Since the PCB operating frequency is extremely high (about 30GHz), a small issue may severely impact performance, even though it may not have had an effect at lower frequencies.

For the mmWave system of PCB, design is a huge challenge. At such a high frequency, we need to select the PCB material/components carefully. This raise concerns over how their parameters and characteristics will perform at mmWave frequency. Any issue with the PCB can lead to severe complications down the line These issues include limiting spurious wave mode

propagation problems, minimizing conductor and radiation losses/insertion loss, achieving effective signal launch, minimizing unwanted resonances, and controlling dispersion [12]. Therefore, it is essential that we develop and refine our mmWave PCB design.

1.3 Thesis Contribution

In this phase, we are focusing on the mmWave massive MIMO RF sub-system. In this subchapter, we present the contributions related to this thesis.

- *The schematic of mmWave massive MIMO system will be proposed.* We propose the system schematic overview for both the transmit chain and the receive chain. We specifically present the system from the signal flow point of view. Then we decide suitable categories, functions, and requirements of RF components that are requested in our project, such as PA, LNA and mixer etc. This will be carried out in chapter 2.
- *Components identification and link budget analysis.* As the components categories have been settled, we propose the specific component for each function that is suitable for our system's needs. Then we test the components individually to verify if they perform as we expect them to. Once we finish the components identification, we assemble the components for the both chains to verify the system performance and link budget. The detail of this section will be carried out in the chapter 2 and chapter 3.
- *PCB design for RF Subsystem.* We design a PCB as the primary prototype for practical experiment and data analysis, based on the approved system architecture and the components selection. We implement the system architecture in one PCB design. There were some concerns raised during the design: material selection, vias settlement, ground plane placement etc. These will be carried out in the chapter 4.
- *Over-air-test for PCB.* We will operate the PCB in the field to verify its suitability and reliability. We explore the experiment's performance and collect data to compare with the theoretical link budget. We verify the performance and results to use as the basis of further discussion. There are potential issues based on the collected data and we relate some ideas

of ways which we could modify and improve the system design in the future. These will be carried out in the chapter 4 and chapter 5.

CHAPTER 2

2 System Diagram

In this chapter we will describe the RF subsystem diagram first, then we will focus on the components with their key functions in this system. The component usage and important parameters will be discussed in detail.

2.1 System Overview

In this project, we plan to design a four layers PCB, the PCB contains two transmit chains and two receive chains. In Figure 3 we present the original system block diagram. This block diagram is the ideal solution, but after the actual measurements, some of the block diagram will be modified based on the test results. The important components usage and parameters will be discussed in this chapter, the entire Rx and Tx link test and the final schematic we plan to use in PCB design is described in the next chapter.

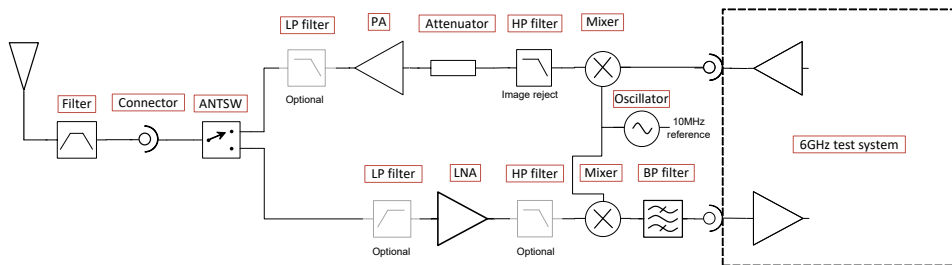


Figure 3 Original System Schematic Block Diagram

The transmit chain is presented on the top side of Figure 3. The signal flows from the right side to the left side. Firstly, LuMaMi test-bed will be responsible for the baseband processing, for example the source generation. The generated signal at 2.5GHz from test bed will be mixed with the oscillator signal. The up-converted signal is 27.95-GHz, a high pass filter is used for removing the unwanted frequencies. And then there is an attenuator to ensure that the input level of the power amplifier will not saturate. The

signal will be amplified by the power amplifier and then spread by the antenna.

The bottom side of Figure 3 presents the receive chain. The signal in this case will flow from the left side to the right side. A 27.95GHz signal will firstly be absorbed by the antenna, then the filter will remove the unwanted frequencies. The signal will pass through the switch and then enter the Rx chain. The LNA is located at the first stage of the Rx chain which we use it to amplify the signal with a low noise figure. And then, the signal will get mixed with the oscillator output signal and output down-converted signal at 2.5GHz. Finally, the filter will ensure the 2.5GHz signal can be read by the LuMaMi test bed for further analyze.

Based on Figure 3, a list of selected components is presented in Table 1, the reason why we are using these components will be discussed in this chapter.

Table 1 Components List

Function name	Model number
Power Amplifier	HMC383LC4
Switch	SDRF5020 SPDT
I/Q Mixer	HMC1063LP3CE
Low Noise Amplifier	HMC1040LP3CE
Bandpass Filter	SAFEA2G35MA0F0A
Power Splitter	Self-made by LTH
Oscillator	PLDRO25.500-10
Array Antenna	Self-made by SONY
USRP	National Instruments

The process of the signal transmitting and receiving is significant, however, when the system block diagram is built here is another problem needs to be considered carefully: the input power level of both Tx and Rx chains' LO port. As we know I/Q mixer will have a minimum input power level requirement, if the input power level is not sufficient, the mixer will not work. In this case, we are planning to use one single oscillator with at least 13dBm

output power to feed the entire 32 Tx and Rx chain by using some power splitters. If we feed the mixer LO port from only one oscillator, the input power of the LO port is definitely not enough. Then the structure in Figure 4 is important and necessary.

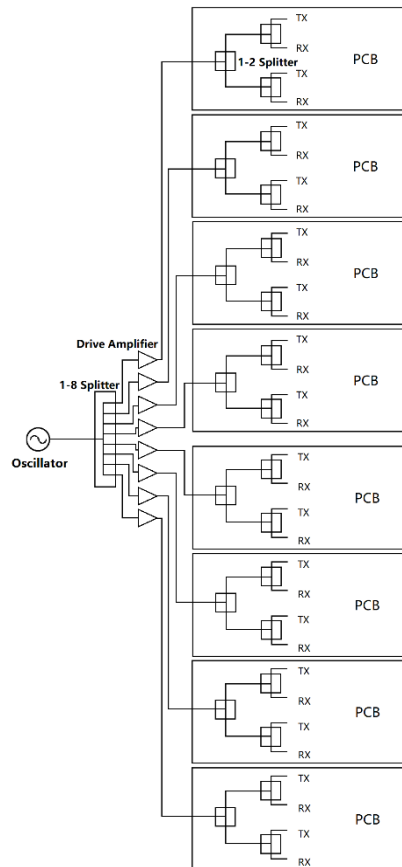


Figure 4 PCB Clock Distribution

Figure 4 is a clock distribution system. Firstly, there is only one oscillator supply. Secondly, we have a one-to-eight power splitter connect to the oscillator output, which all eight branches have the equivalent power separated and distributed. To compensate some power loss in the power splitter, the output of each branch connects to a drive amplifier with enough gain to boost up the signal. Finally, signal enters the PCB and then splits by three Wilkinson power splitters to each chain.

2.2 Components for RF System

2.2.1 Single Pole Double Through (SPDT) Switch

Function:

The SPDT switch is used to switching between the RFC-RF1 path and RFC-RF2 path, where the RFC is the common port of the switch, RF1 and RF2 are the ports connect the Rx and Tx chain. The 'EN' and 'CTRL' pins are the key to achieve the switching operation, the different input voltage level of these two pins will trigger the path-switching function.

Considerations:

Frequency range: This SPDT switch has wideband frequency range between 100MHz to 30 GHz.

Isolation: The isolation between RFC, RF1 and RF2 ports are typical 60 dB .

High input linearity: The 1dB power compression point is 28dBm and it can handle 24dBm on the through/terminated path.

Low insertion loss: The component insertion loss is about 2dB.

Component Description:

In Figure 5 we present the pins configuration and the application circuit for ADRF5020 SPDT switch.

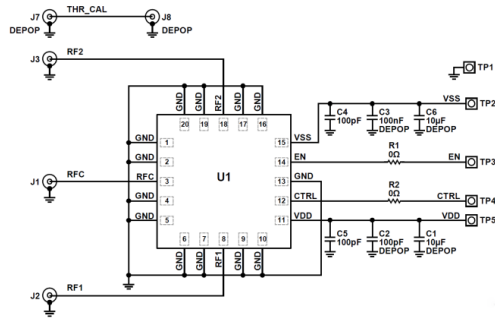


Figure 5 SPDT Switch Pins and Application circuit [13]

The SPDT switch requires a 5V supply voltage for pin VDD and another -2.5V for pin VSS [13]. To reduce the RF coupling effect, the bypassing capacitors are placed on the power supply lines.

All the RF ports are designed to match with 50Ω internally [10], so the external matching components are not required. Moreover, RF ports are dc-coupled to 0V which means dc blocking is unnecessary. The RF common port (RFC) could be used as single input, and then RF1 and RF2 are the output or vice versa. Either RFC to RF1 path or the RFC to RF2 path is controlled by the EN and CTRL pins. ‘Low’ level means 0V supply and ‘High’ level means 3.3V-5V supply (We choose 5V to match the power supply), and the control voltage truth table is given in Table 2 [13].

Table 2 SPDT Switch Truth Table [13]

Digital Control Input		RF Paths	
EN	CTRL	RF1 to RFC	RF2 to RFC
Low	Low	Isolation(off)	Insertion Loss (on)
Low	High	Insertion Loss (on)	Isolation(off)
High	Low	Isolation(off)	Isolation(off)
High	High	Isolation(off)	Isolation(off)

2.2.2 The Power Amplifier

Function

Power amplifier that boost the low-power radio signal to a high-power radio signal. In general, the power amplifier is used in the transmit chain to provide the enough power and drive the antenna to spread the signal.

Consideration:

Gain: This power amplifier could deliver a 15dB gain.

Frequency range: The component operating frequency range is from 12GHz to 30GHz.

Output saturated power: The output power level larger than 18dBm will no longer be linear amplification, make sure the input and output level is suitable [14].

Component Description:

This power amplifier only needs one single positive supply to VDD pin, the RFIN and RFOUT pins are used for signal input and output, and the rest pins connect to the ground [14].

In Figure 6 we present the HMC383LC4 power amplifier pin configuration and its application circuits [14]. All the input and output ports are matched to 50Ω, 24 pins but only three pins are functional [14], RFIN and RFOUT are used for signal input and output, VDD is used for power supply. The rests N/C pins refers to no connection and they are suggested to connect ground.

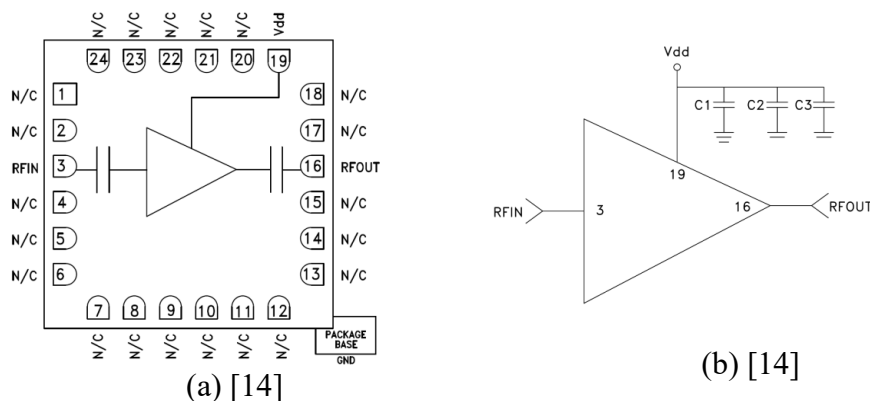


Figure 6 Power Amplifier Pin Configuration and Application Circuit

2.2.3 The I/Q Mixer

Function

I/Q mixer is a passive device, it has two IF ports, one RF port and one LO port. IF port is used for intermediate frequency input and output, RF port is radio frequency input and output port, LO port is the local oscillator input port.

The mixer is commonly used to achieve the frequency up-conversion and down-conversion. When the up-conversion mode is selected, the RF port will generate an output frequency which is the sum of intermediate frequency and local oscillator frequency. When the down-conversion mode is selected, the IF port will generate a frequency which is the difference of the radio frequency and local oscillator frequency.

Consideration:

There are some considerations when using an image reject mixer.

Conversion loss: The conversion loss is the total loss through the mixer. For normal applications, around 10 dB is acceptable [16].

Image Rejection: When the mixer is up-converting or down-converting, an image frequency appears on the other side of the local oscillator frequency. For example, the up-converting frequency is at $F_{LO}+F_{IF}$, its image frequency will appear at $F_{LO}-F_{IF}$. If the wanted frequency and its image frequency are at same power level, the image frequency will interfere to the wanted frequency significantly. To avoid this problem, the image rejection of the mixer needs to be considered carefully. HMC1063LP3E can provide a 21dBc image rejection which is good enough.[16].

Component Description:

In Figure 7 we present the HMC1063LP3E in-phase and quadrature (I/Q) mixer. This I/Q mixer contains two standard double balance mixer cells with a 90-degree hybrid cell. Both IF, LO and RF ports are internally match-ed to 50Ω, other pins are connected to the ground.

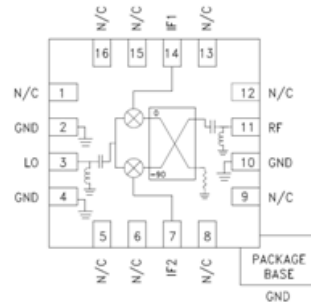


Figure 7 I/Q Mixer Pins Configuration [15]

2.2.4 The Low Noise Amplifier

Function

The low noise amplifier is the key components of receive chain in a communication system. This LNA can be used to amplify the weak signal received by the antenna with a very low noise figure. The Friis formula [1] is used for calculating the total noise figure and we can know that, the first component of the entire Rx chain will dominate the total noise figure. To minimize the total noise figure of the entire Rx chain, using a low noise figure amplifier to be the first component in a Rx chain is essential. That is the reason why we use a LNA here.

Consideration

Gain: The LNA has a 23dB gain, which is high enough to amplify the received signal.

Noise figure: The noise figure is an important parameter of LNA, which measures the degeneration of the SNR, the lower noise figure states the better performance. The LNA only have 2.2dB noise figure, this will dominate the entire receive chain on a low level of total noise figure.

Frequency range: This LNA have the frequency range from 24GHz to 43.5-GHz.

1dB output power: The 1dB output power is 12dBm. In general, the received signal that antenna absorbed is very week, and 12dBm considered as a strong level for the received signal, but still needs to be taken care.

Component Description:

The HMC1040LP3CE LNA operates on between 24GHz and 43.5 GHz to deliver about 23dB power gain, with only 70mA and 2.5V positive supply voltage.

In Figure 8 we present the pins configuration and application circuit of the LNA. The Vdd1, Vdd2 and Vdd3 are the drain bias voltage for the amplifier, RFIN and RFOUT ports are signal input and output, both are AC coupled and 50Ω matched [17].

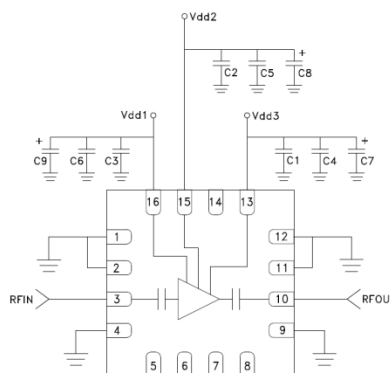


Figure 8 LNA Pins Configuration and Application Circuit [17]

2.2.5 Other Components

2.5.1 Band Pass Filter

This component is a passive filter with five pins and has the best theoretical performance when it is operating between 2.4 GHz to 2.484GHz [18]. This

filter is placed after the mixer to ensure that only the down-converted signal in the correct frequency range can pass the filter and eliminate the others unwanted frequencies. In Table 3 presents the insertion loss of the filter [18].

Table 3 Band Pass Filter Insertion Loss [18].

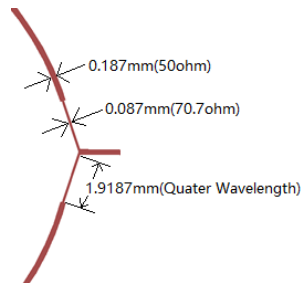
	Frequency	Characteristics			Unit dB
		Min	Typically	Max	
Insertion loss	2400 to 2484 MHz	/	1.9	2.6	/
		/	1.9	2.3	23 to 27 deg.C

2.5.2 Power Splitter:

In the initial experiment, the PE2078 was used for splitting the oscillator output signal, but in the PCB layout, another power splitter using Wilkinson hybrid model was designed by LTH. In Figure 9 presents the power splitter in box and the Wilkinson power splitter model.



(a) Power splitter in box [19]



(b) Wilkinson power splitter model

Figure 9 Power Splitter

2.5.2 Oscillator:

The oscillator PLDRO25.500-10 generates a 13dBm signal at 25.5GHz is used as a local oscillator in the system. In Figure 10 we present the oscillator appearance.



Figure 10 Oscillator PLDRO25.500-10

2.5.4 Array antenna

The array antenna is made by the Sony, the antenna gain is approximately +5dB. The appearance of array antenna is presented in Figure 11.

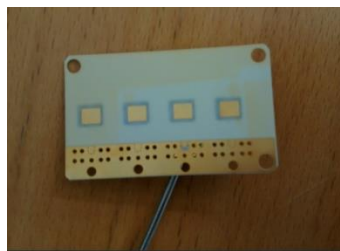


Figure 11 Array Antenna Appearance

2.5.5 Horn Antenna

In addition, we run another test using horn antenna which was made by Pasternack instead of array antenna. The horn antenna has 15dB gain and operates from 26.5GHz to 40GHz [18]. It has a vertical half power beam width of 31.3 degrees and horizontal half power beam of 32.1 degrees. The horn antenna appearance is presented in Figure 12 [20].



Figure 12 Horn Antenna Appearance

However, the antenna gain varies slightly due to operating on the different frequency. The horn antenna has approximately 13dB gain on 27.95GHz.

CHAPTER 3

3 Tx/Rx Chain Testing and Over Air Testing

In this chapter, we will process the developments by two phases. Firstly, we need to verify the Tx/Rx chains performance. Furthermore we need to calculate the link budget. Comparing both experiment and theoretical data to knowledge whether the results are reasonable or not. The system block diagram is presented in the Figure 13.

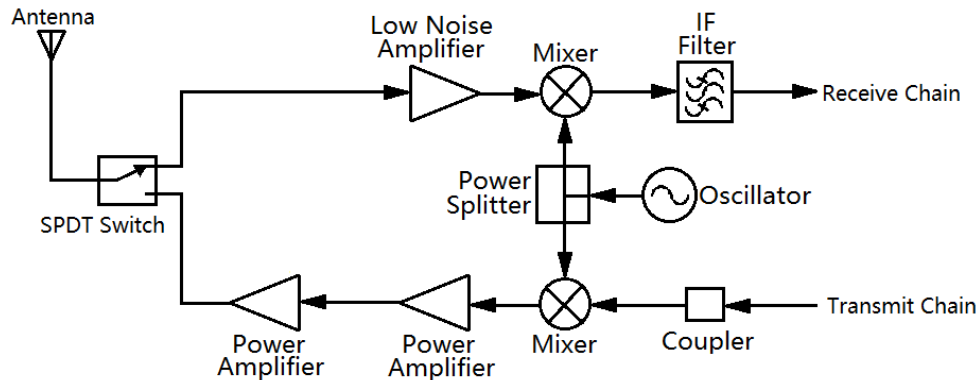


Figure 13 System Block Diagram

The first phase we have two steps. Firstly, we have preliminary Tx/Rx evaluation boards manually assembled and all the electronic components connected based on the system block diagram. In Rx chain, the signals generator is used for simulating the received signal. At the Rx chain output, we place a spectrum analyzer to inspect the received signal performance. Similarly, we manually feed an input signal to Tx chain by the signal generator. At the Tx chain output, we place a spectrum analyzer inspect the system performance. The two chains experiments are operating individually with no interference to each other.

The second phase we arrange two array antennas, one in the Tx chain and the other one in the Rx chain. Two antennas are placed face to face with some specific distance, and two chains operate at the same time. This time only

one signal generator at Tx chain and one spectrum analyzer at Rx chain. We will verify the system performance on the spectrum analyzer to confirm whether the two chains are functional or not.

Once the second phase has finished, the signal generator and spectrum analyzer will be replaced by USRPs to manage the signal generating, receiving and data detection.

3.1 Individual Components Testing

Examining the individual components before connecting the entire chain together is prerequisite. In practical experiment, each component performance will deviate slightly from the datasheet. In our test, calculating the link budget for Tx and Rx chain is important, because from the results we can verify our chain is feasible or not. Based on this consideration, an individual components test has made.

3.1.1 SPDT Switch Insertion Loss Measurement

The evaluation board is used for testing the component insertion loss; the link setup follows the Figure 14.

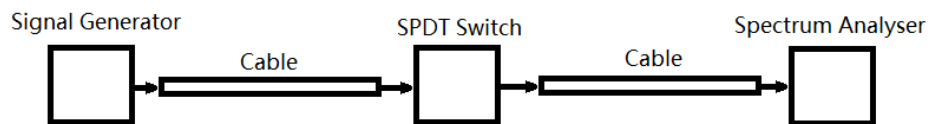


Figure 14 SPDT Switch Testing Setup

The signal generator is generating a -20dBm signal at 25.5GHz, the signal transmits through two cables (26dB loss in total) and the SPDT switch. The spectrum analyzer can detect a -48dBm signal at 25.5GHz.

The SPDT switch insertion loss can be calculated as:

$$\text{SPDT Switch Insertion Loss} = 48\text{dBm} - 20\text{dBm} - 26\text{dB} = 2\text{dB}$$

The measured value compared to the datasheet is presented Table 4

Table 4 Insertion Loss Measured Versus Datasheet

	Measured	Datasheet
Frequency	25.5GHz	20-30GHz
Insertion Loss	2dB	2dB [13]

3.1.2 I/Q Mixer Gain Measurement

In Figure 15 we present the mixer testing setup, the gain will be tested together with coupler. The 90-degree coupler here is used for making the two IF input port 90-degree phase shifted: IF1 port is 0-degree and IF2 port is 90-degree.

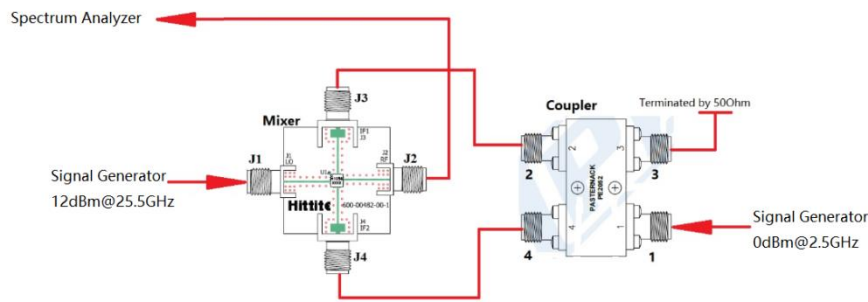


Figure 15 Mixer Measurement Setup

The coupler has 5dB attenuation and the cable loss was totally 18dB. The LO port is fed with a 12dBm signal at 25.5-GHz and the coupler input port is fed with a 0dBm input at 2.5GHz.

Two signals peaks could be observed from the spectrum analyzer, the result is presented in Table 5.

Table 5. Output from the Spectrum Analyzer

Frequency	Power
28GHz	-34dBm
23GHz	-64dBm

From the Table 5, a 30dB image rejection is showed clearly, and the mixer attenuation could be also calculated as:

$$\text{Mixer Gain} = 34\text{dBm} - 5\text{dB} - 19\text{dB} - 0\text{dBm} = 10\text{dB}$$

3.1.2 LNA Gain Measurement

The measurement setup follows the Figure 16:

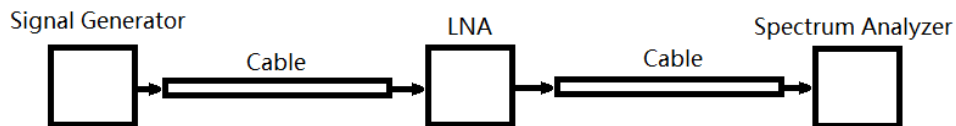


Figure 16 LNA Gain Measurement Setup

The signal generator is feeding a -30dBm signal at 28GHz, the signal is passing through two cables (totally 19dB loss) and the LNA, the spectrum analyzer reads a -30dBm output at the very same frequency. The LNA gain is measured to be 19dB.

3.2 Tx/ Rx Chain Testing

3.2.1 Tx Chain

In the Figure 17 we present the Tx chain block diagram. This Tx chain block diagram is designed based on the system block diagram in Chapter 2.

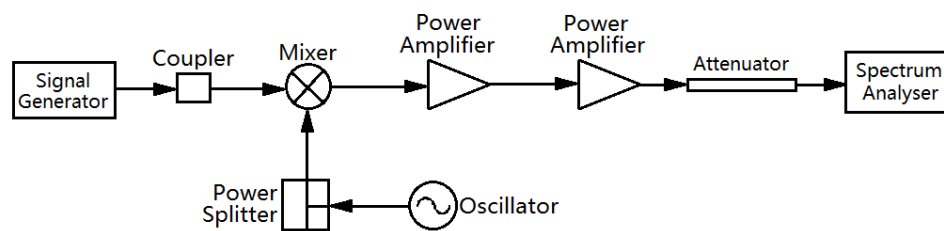


Figure 17 Tx Chain Block Diagram

In additional, we first add one 90-degree SMA hybrid Coupler PE2052 made by Pasternack after Tx input signal and before the mixer. This component splits an input signal into two paths with a 90-degree phase difference. This coupler has 50ohm impedance, operates between 2GHz and 4GHz with 3.1 ± 0.8 dB coupling loss. In the component testing the measured coupling loss is approximated 5dB [20]. Secondly, there are two identical 6dB attenuators placed in front of the spectrum analyzer to reduce the outcome power level, which ensure it is located on the secure measurement region of the spectrum analyzer.

Results

In the first experiment, the Tx chain is fed by 0dBm at 2.5GHz and the Tx output detected by spectrum analyzer is -5dBm at 28GHz. And in the second experiment, the Tx chain is fed by 10dBm at 2.5GHz and the Tx Output detected by spectrum analyzer is 4.2 dBm at 28GHz.

Comparing these two experiments , the input has increased 10dB and the output result maintains linearity that increased almost 10dB. Therefore, this input variation does not affect the gain of the whole chain, the results are still valid and not reaching the compressing point of the amplifiers. The image rejection test is observed by the differences between two sidebands. We checked in the second experiment, the output power level at 23GHz is -26dBm and the output power is -4.2dBm at 28GHz. There is about 24dB difference which is good.

In the Equation 1.1, we present the expect output power in theoretical .

$$P_{out} = P_{in} + \sum G_{component,rx} - \sum L_{cable} \quad (1)$$

Where P_{out} is the Tx output power, P_{in} is the Tx input power, $\sum G_{component}$ is the sum of gain or attenuation for all evaluation board components through the Tx chain. $\sum L_{cable}$ is sum of the cable loss.

In the datasheet, the coupler is -4dB, mixer is -9dB , two power amplifiers are 24 dB, two attenuators are -12dB, and we have 6dB cable loss in total. In our measurements, the coupler is -5dB, mixer is -10dB, power amplifiers are 26 dB, two attenuators are -12dB and 6dB cable loss as well.

The expectation results number from Eq (1) is $P_{out} = P_{in} - 7\text{dB}$ from components datasheet. For the first experiment, P_{in} is 0dBm, P_{out} should be -7dBm at 28GHz. And in the second experiment, P_{in} is 10dBm, P_{out} should be 3dBm at 28GHz. The comparison between theoretical and experiment results, present in Table 6.

Table 6 Tx Chain Testing Result

2.5GHz	Theoretical	Experiment	Difference
0dBm	-7dBm	-5dBm	2dB
10dBm	3dBm	4.2dBm	1.2dB

In the Table 6, both two cases experiment results are slightly outperformed than the expectation number. However, we estimate the worst circumstance when we considering the cable loss. In practical the cable loss is smaller than 1dB. Above all, these measurements can basically satisfy the expectation.

3.2.2 Rx Chain

Similarity, the Rx testing block diagram has some modification also. In the Figure 18 we present the Rx testing block diagram.

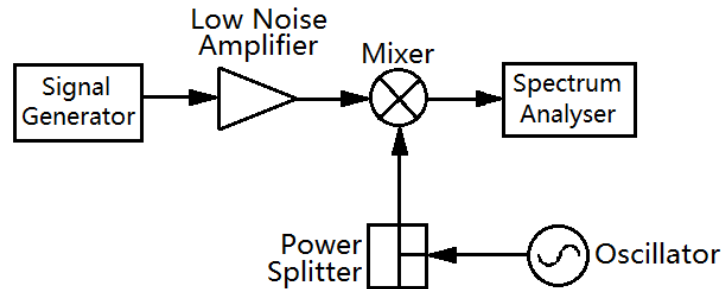


Figure 18 Rx Chain Block Diagram

The signal generator here is used for simulating the received signal absorbed by the received antenna. The received signal is assumed to be -60dBm at 28GHz. The signals get boost from the low noise amplifier and mixed with the local oscillator. The mixer will return one lower sideband signal and another unwanted higher sideband signal. In the current phase, the IF filter is not added, to read the correct signal, the spectrum analyzer should change

the center frequency to the lower sideband frequency, which is 2.5GHz in this case.

Results

We use the same the formula in Eq (1)to calculate the output power in Rx chain. The final output power level of the Rx chain is -49dBm at 2.5GHz, the input is -60dBm at 28GHz so the total gain is 11 dB.

In this case where P_{out} is the Rx output power, P_{in} is the Rx input power, $\sum G_{component}$ is the sum of gain or attenuation for all evaluation board component through the Rx chain, including one LNA(+19dB) and one mixer(-10dB). $\sum L_{cable}$ considering the worst case has 2dB in total. The expectation results number from Eq 1.1 is $P_{out}=P_{in}+7dB$, which means we have total gain of 7dB. In Table 7 we present the experiment result and also compared the theoretical (7dB gain) with experiment (11dB gain) results, the experiment outperformed than the expectation.

Table 7 Rx Chain Testing Result

28GHz	Theoretical	Experiment	Difference
-60dBm	-53dBm	-49dBm	4dB

3.3 Over the Air Test

In the chapter 3.1, we have tested the Tx chain and Rx chain individually. We were using the signal generator and spectrum analyzer to produce the signal and inspect the system performance. However, the spectrum analyzer can only detect the received spectrum and the power level. Furthermore, the bit error rate, signal to noise ratio and the signal constellation points also need to be observed. For this reason, we determine to test the Tx and Rx chain over the air simultaneously with the USRP equipment.

3.3.1 Equipment Setup

In Figure 19 we present the block diagram for the over the air test. The USRP on Tx side will generate a 4-QAM signal and propagate the electromagnetic

wave into the air after passing through the Tx chain. The USRP on Rx side will absorb and demodulate the received signal, and then we can observe the received constellation points and read the received power level. In Figure 19 we present the equipment setup in the lab, lower side in the blue frame is the Tx chain setup and upper side in blue frame is the Rx chain setup.

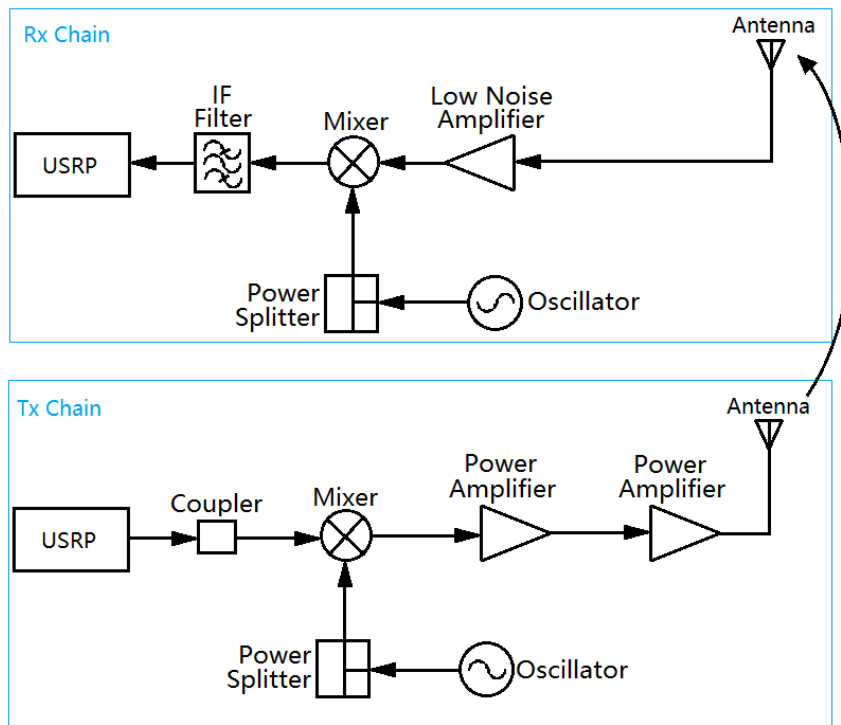
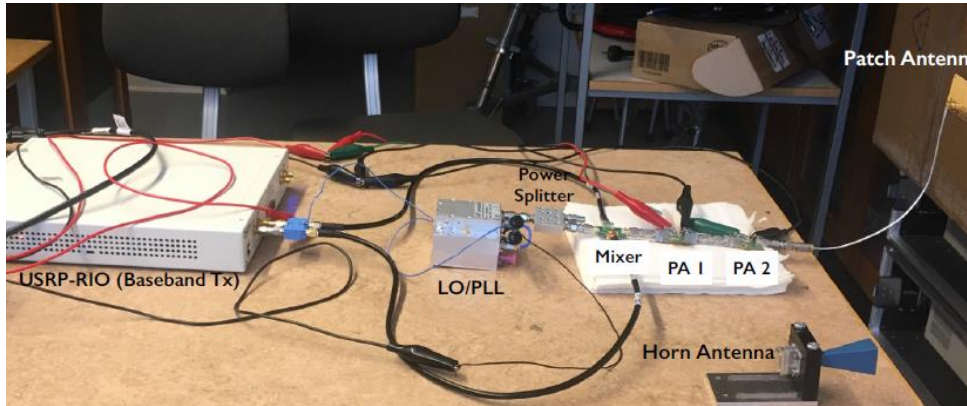
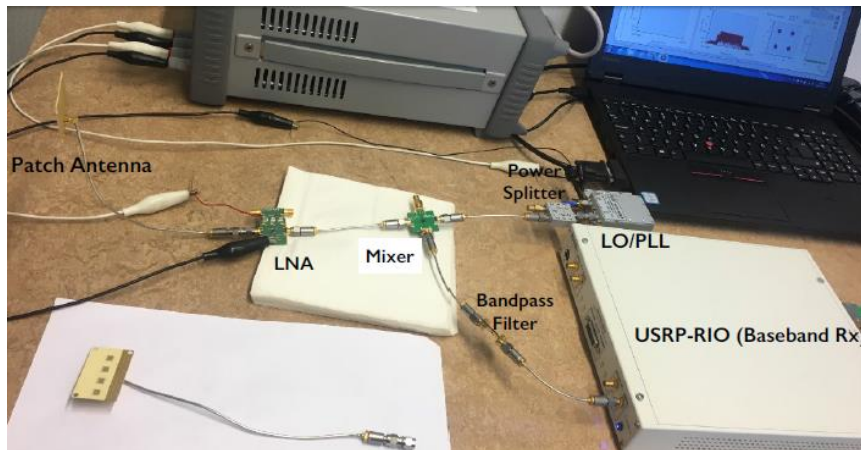


Figure 19 Over the Air Test Block Diagram

For the equipment set up, two array antennas are designed by SONY. These two antennas are used for signal transmitting and receiving. To observe the best performance, the two antennas put on the same horizontal level, face to face that antenna could absorb maximum incoming wave beam.



(a)Tx chain



(b) Rx chain

Figure 20 Equipment Setup

The USRP hardware is made by National Instrument. It contains 2x2 MIMO transceiver tunable independent frequencies with options from 50MHz to 6GHz [19]. This equipment could either generate the modulated signal by any specific power level within the operation range or absorb the receiving signals and monitor dynamic state of SNR performance. In Figure 21 we present the USRP RIO equipment [22].

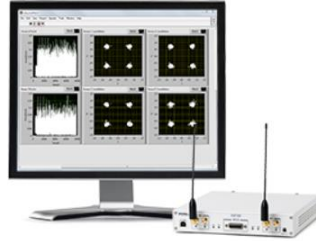


Figure 21 The USRP Equipment [22]

3.3.2 Link budget

Link budget is a method of accounting the entire gain and the loss from the transmitter, the propagation loss through the medium like air to receiver side. The total gain and loss including both transmitter and receiver side such as antenna gain, cable loss. The propagation loss is modeled as free space path loss [20]. In general, the link budget express in text as:

$$\text{Transmitted power} + \text{Gain}(s) - \text{Loss}(es) - \text{Propagation loss}(es) = \text{Received power} \quad (2)$$

The Eq (2) calculates in decibel (dB) unit and this equation is also the modified version of the Friis transmission equation for link budget calculation. In Figure 22 present the link budget diagram.

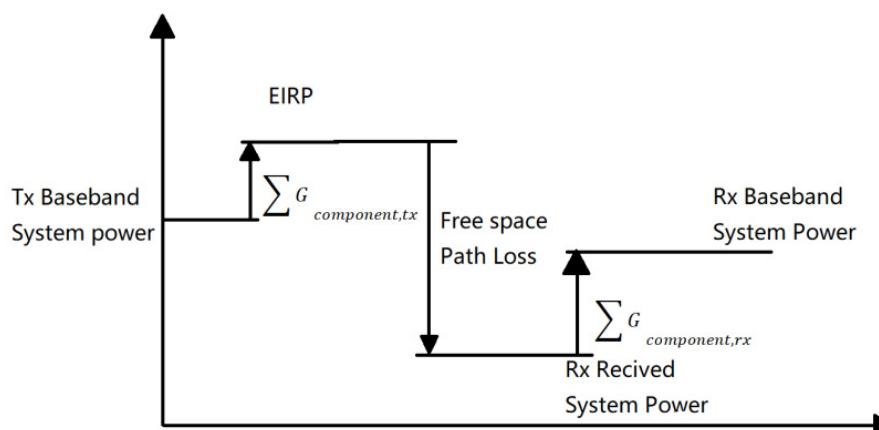


Figure 22 Link budget

In this figure, $\sum G_{component,tx}$ is the total gain of the components in Tx chain, $\sum G_{component,rx}$ is the total gain of components in Rx chain. The upwards arrow indicates the gain and the downwards arrow indicates the loss.

Tx chain

The sum of the transmitting gain in the Tx chain involves one coupler (-5dB), one mixer(-10dB), two drive amplifiers (+13dB each) and one array antenna (+5dB) which accounts total +16dB gain supporting the system. Therefore, the EIRP (Equivalent Isotropically Radiated Power) in the Tx Chain is 8dBm.

Rx Chain

For RX chain, the entire gain of the components involves one LNA (+19dB), one mixer (-10dB), one IF filter (-2dB), one array antenna (+6dB) which all accounting to be +13dB in total.

Free Space Path Loss

The free space path loss defined as the attenuation of radio energy between the Tx and Rx antenna feed-points. This phenomenon is caused by the combination of the receiving antenna's capture area, line-of-sight path through the air [23]. In general, the path loss is exponentially rising with the distance in the line of sight path over the air [23]. The theoretical free space path loss formula in dB, follows by

$$PL = 10 \log_{10} \left(\frac{4\pi d}{\lambda} \right)^2 \quad (3)$$

In this Eq (3), the λ is the signal wavelength, d is the distance between the antennas, they are in the same unit of length. Expanding and simplifying the formula in dB unit, then Eq. 1.3 becomes $PL = 20 \log_{10} d + 20 \log_{10} f - 27.55$. Where f is the transmission frequency, in MHz unit, d is distance in meter unit. In our case, the distances d are 0.40m and 1.20m, and f is 27.95 GHz, the path loss in calculation is approximately 53.41dB and 62.95dB.

In this experiment, we are focusing on the free space path loss calculation since the gains/losses are calculable, Tx and Rx power can be measured by the USRP- RIO. This means the only thing we need to verify is the measured path loss matches the calculated theoretical free space pass loss or not.

3.3.3 Experiment Results

Array antenna

In Figure 23 and Figure 24 we present the experiment results on Rx chain from USRP. The distance between the antennas is 0.4m in Figure 23 and 1.2m in Figure 24. The output power level can be detected by the USRP. The received power is -33dBm when the distance between the antennas is 0.4m and the received power is -42dBm when the distance has increased to 1.2m. In Table 8 we present the link budget calculation using the Friis equation based on results in chapter 3.2.2

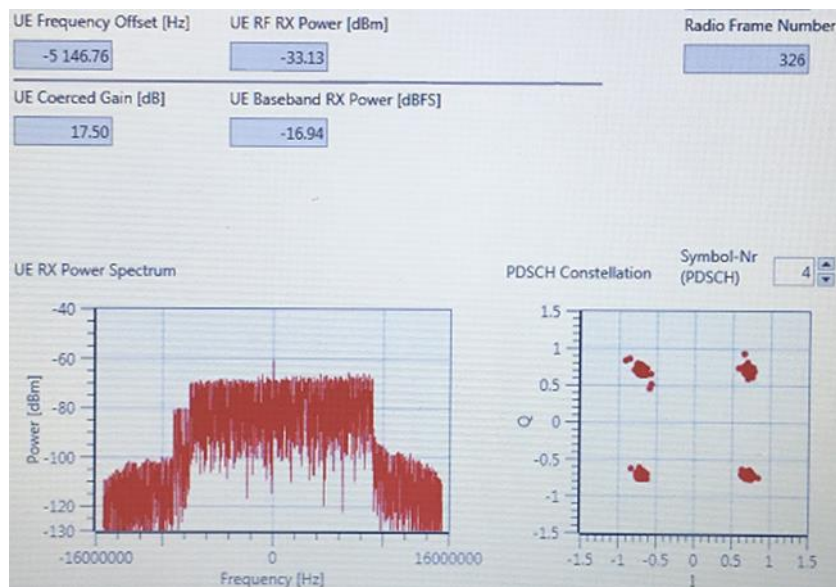


Figure 23 Received Constellation and Power (d = 0.4m)

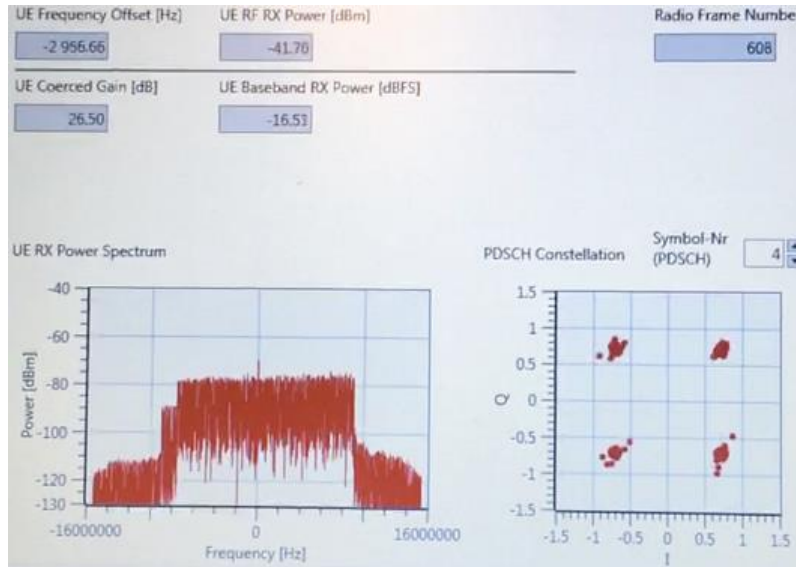


Figure 24 Received Constellation and Power (d = 1.2m)

In the Table 8, we could estimate the measured free space path loss by calculating the difference between the Rx Received Signal Power and EIRP. The measurement results and theory of the free space path loss results are almost the same (53.4 dB/53 dB and 63 dB/62dB).

Table 8 Link Budget Calculation Using Patch Antenna

Antennas Spaced Distance	Tx Base-band System Power	EIRP	Free Space Path Loss		Rx Received Signal Power	Rx Base-band System Power
			Theory	Measured		
0.40m	-8dBm	8dBm	53.41 dB	53.0dB	-46dBm	-33dBm
1.20m	-8dBm	8dBm	62.95 dB	63.0dB	-55dBm	-42dBm

Horn Antenna

We intend to have more experiment data to support our previously testing results. Therefore, we change the transmit antenna into a horn antenna to verify whether the results still valid or not. The distance spacing between the Tx horn antenna and Rx patch antenna maintains 1.20m.

In Table 9 we present the link budget calculation based on the formula. In this table, the measurement results and theory results basically the same (62.95 dB / 63dB), the horn antenna experiment case is also successful.

Table 9 Link Budget Calculation Using Horn Antenna

Antennas Spaced Distance	Tx Base-band System Power	EIRP	Free Space Path Loss		Rx Recived Signal Power	Rx Base-band System Power
			Theory	Meas-ured		
1.20m	-8dBm	16 dBm	62.95 dB	62.0dB	-47dBm	-34dBm

CHAPTER 4

4 PCB Design and Test

The PCB design is based on the Tx and Rx evaluation board test in Chapter 3. In this chapter we are focusing on the details when we are designing the PCB layout, for example the electromagnetic interference and power management.

4.1 Layer Stack and Design Rule

4.1.1 PCB Board Material Selection

Different board materials have different parameters. For the high frequency design: firstly, the dielectric constant and the dissipation factor need to be considered. There are also other parameters, for example the 'Tg' value will give the board size stability during the high temperature PCB making process.

We determined to use the Rogers 4350B in the high frequency layers, and the FR4 material is used between the ground and power layers. These two materials will be discussed individually to show their advantages in this project.

Rogers 4350B:

The Rogers 4000 series product especially Rogers 4350B was widely used in high frequency PCB. This material has the similar artisanship like FR4 but much cheaper compare to other material used for high frequency.

Besides the price factor, the most important reason is the dielectric constant of Rogers 4350B is only 3.5. This constant has strong stability against the temperature variation comparing to other materials. This characteristic provides the convenience on transmission line and matching design. When we

are designing a 50Ohm transmission line in a certain frequency, width of transmission line is depending on the board dielectric constant and board width. The board width is a certain value, which means the board dielectric constant needs to be stable to make transmission lines stable. .

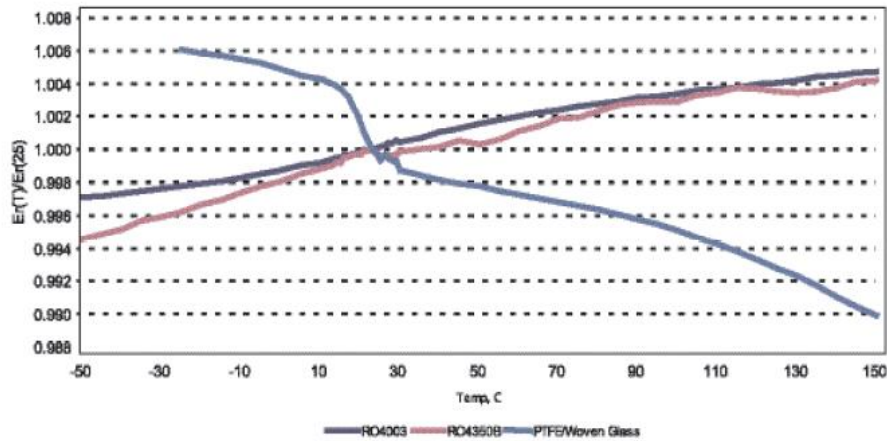


Figure 25 Dielectric Constant Comparisons in Different Temperature [23]

In Figure 25 we present the dielectric constant comparison between the Rogers 4350B and PTFE in different temperatures. It can be clearly read on the graph that the Rogers 4350B has the best stability performance of dielectric constant.

The dissipation factor describes the single and energy losses when the signal passing through the medium. Rogers 4350B has only 0.003 of this, which gives very low energy loss. Also, the thermal coefficient of expansion for Rogers 4350B is similar with copper, making the size stable during the layer stacking and the drilling [23].

FR4:

This material is using for both the ground layer and power layer, where there is no high frequency signal passing through. This type of material is glass-reinforced epoxy laminate with good mechanical and dielectric performance, typically the dielectric constant for FR4 is about 4.5 [24]. This material also has excellent thermal resistance and low cost.

4.1.2 Layer Stacking

In our design, we have four layers: one top layer, one ground layer, one power layer and one bottom layer. The top layer is used for mounting the components and routing. To minimize the high frequency signal loss, we keep all transmission lines for 27.95GHz on the top layer. Inevitably, there are some intermediate frequency signal transmission lines will passing through the board by vias to the bottom layer.

The second layer is the ground layer, there is a massive ground plane area that distributed with thousands of ground vias on different layers. The third layer is used as the power layer, all the power supply lines are placed here. The bottom layer is used for routing the 2.45GHz wires, which are originally coming from the top layer to avoid the wire cross each other on the same layer in case of interference.

In Figure 26 we present the layer stacking method, which contains the entire board width, copper foil width and the material width as well.



Figure 26 Layer Stacking

4.1.3 Design rules

The design rules should follow the requirements which are provided by the manufacturers. The typically transmission line width, distance between wires and vias are 4mil and the minimum size can reach 3mil if needed. Also, the default vias diameter is 0.2mm and the minimum size can reach 0.15mm. The fabrication limitation is executable for project design and manufacturers; however, we are not recommending this operation. This will

jeopardize the signal at high risks and increasing the manufacturing cost rapidly.

The PCB design is prohibited using the blind and buried vias, all the vias we applied in the project are through vias. In the Figure 27 we present: (a) ground vias between top, power and ground layers' ground plane, (b) signal vias and (c) power vias from top layer to power layer.

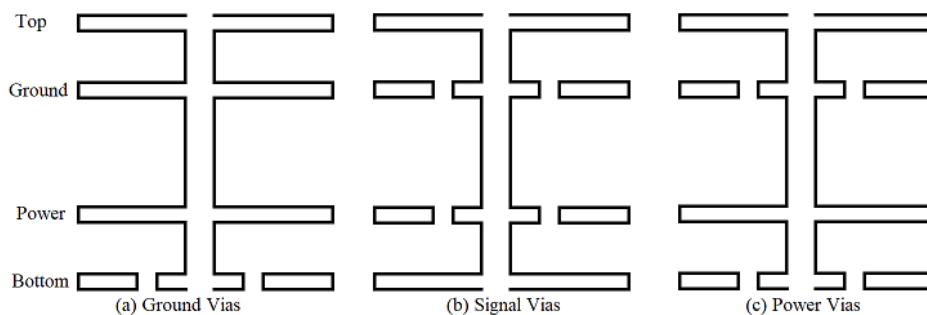


Figure 27 Vias Sectional View

4.2 Ground Plane

The ground plane of the PCB refers to the large area of copper foil which is placed on different layer and connected by the vias. They will feed back to the ground terminal on the external power supply eventually and works as a return path for the current that comes from the components. For this specific reason, the ground plane can be also named as the return plane.

Another significant reasons for the ground plane is it can effectively reduce the system electromagnetic interference. The electromagnetic interference is caused by the electromagnetic wave getting into the system from both outside system and system itself. This interference will generate the additional noise to the signal which could deteriorate the signal quality.

4.2.1 Reduce the Cross-talk effect

The cross-talk effect is the electromagnetic interference which is generated by the system itself. This phenomenon is caused by one route on the four

layers board inducing the interference into the adjacent signal route. This phenomenon will be appeared according to Faraday’s law of induction Eq. 1.4 [25]. The interference induced in the conductor which is caused by the changes on the magnetic flux with respect to the time.

$$E = -\frac{d\phi}{dt} \quad (4)$$

In this Eq (4), $d\phi$ is the magnetic flux variation, dt is the time variation, and the E is the electric field intensity. This phenomenon is called “self-inductance” in electromagnetism. Furthermore, the secondary conductor is self-induced by the electromagnetic filed from the primary conductor, it will also influence the way back to the primary conductor, which is called “mutual inductance”.

Every closed loop circuit where the current flows in the PCB will generate the magnetic field. The best way to minimize the effect of the electromagnetic induction phenomenon is to reduce the loop inductance which caused by the closed circuit. The inductive reactance was described as Eq (5) [25]:

$$X_L = 2\pi fL \quad (5)$$

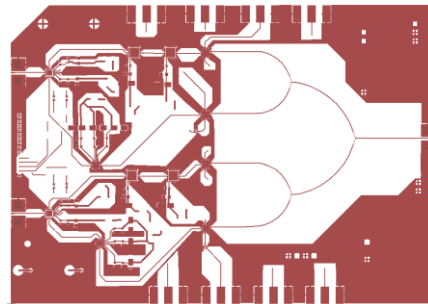
In this equation, X_L is inductive reactance, f is the frequency, and L is loop inductance. To make the X_L as low as possible, the return path design should be wider to reduce the self-inductance and route should be close to the signal. This is the reason why a large area of ground plane is added on top, ground and power layer [25].

4.2.2 Ground Plane on PCB

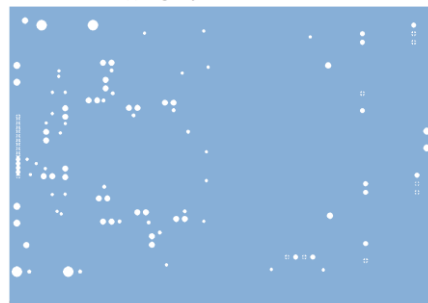
In Figure 28 we present the ground planes on each layer. In this figure, some large size ground planes can be seen clearly. As we discussed in chapter 4.2.1, they are used to minimize the electromagnetic interference.

To get the best connection quality with ground, abundant mount of vias are placed on the ground plane to connect the ground together. The “green points” in Figure 29 are the ground vias with 0.2mm diameter. The current

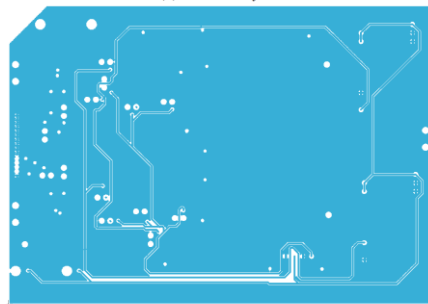
from the ground pins will find a shortest way through the ground vias to the ground layer inside the board.



(a) Top Layer Ground Plane



(b) Ground Layer



(c) Power Layer Ground Plane

Figure 28 Ground Planes for PCB

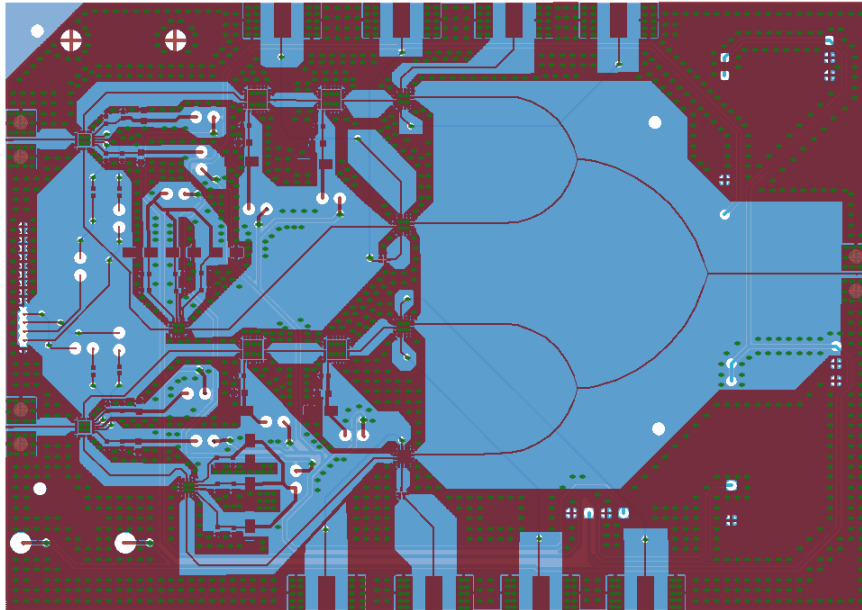


Figure 29 Ground Vias

4.3 High Frequency Vias

For high frequency PCB system, the extra capacitance and inductance in the trace can affect the high frequency signal quality significantly. This influence is produced by signal vias invariably. Therefore, the vias that are working at high frequency need to be handled carefully.

4.3.1 Models for Vias

The lumped pi model and cascaded model are used for explaining the vias effect. The lumped pi model only works when the delay of the vias is less than 0.1 second of the signal rise time but, is still useful to understanding the vias effect. On the other hand, the cascaded model is common model for most of the 4 layers PCBs.

Lumped pi Model:

In Figure 30 we present the equivalent circuit for a two layers PCB: (a) presents a two layers PCB via and (b) presents the lumped pi model for this via.

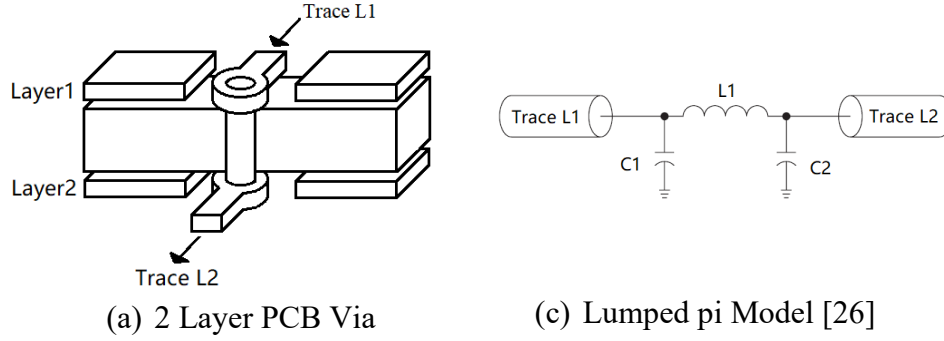


Figure 30 Vias and Equivalent Circuit

The capacitive of the vias was caused by the insulation distance between the vias pad and the anti-pad, the capacitance can be calculated [26]as:

$$C_{via} = \frac{1.41\epsilon_r D_1 T}{D_2 - D_1} \text{ pF} \quad (6)$$

Where ϵ_r is the dielectric constant of the board material, D_1 is via pad diameter, D_2 is anti-pad diameter and T is the board width. The formula shows the capacitance of via only related to the size of via, and the parameters of the board material. In order to control the capacitance as low as possible, one good way is to make the via diameter smaller and the distance between the via pad and anti-pad larger. Another method is keeping the board width as thin as possible and pick a low dielectric constant material.

The inductance of the vias can be calculated as:

$$L_{via} \approx 5.08h \left[\ln\left(\frac{4h}{d}\right) + 1 \right] \text{ nH} \quad (7)$$

Where h is the via length and d is the via barrel diameter. The inductance of the via is unrelated with the board material, but only depend on the size of the via. To reduce the inductance the best way is to reduce the via length and the via barrel diameter [26].

Cascaded Model:

The Lumped pi model is the most accurate model for understanding. For a 4 layers PCB, the most consistent model is the cascaded model. For example, the high frequency signal via is used for signal to travel from the top layer to the bottom layer. The signal will travel through the entire board including the ground and power layer and there is no copper foil between these two layers and vias. In Figure 31 we present the detail of the signal vias.

The via on Figure 31 is used for high frequency signals on PCB. The distance between the via pad and the anti-pad on top and bottom layer are designed to be big enough compare to the distance on ground and power layer. According to the Eq (6) and Eq (7), the capacitance of the via on top and bottom layer can be ignorable, and then the Cascaded model can be presented like Figure 32 [27].

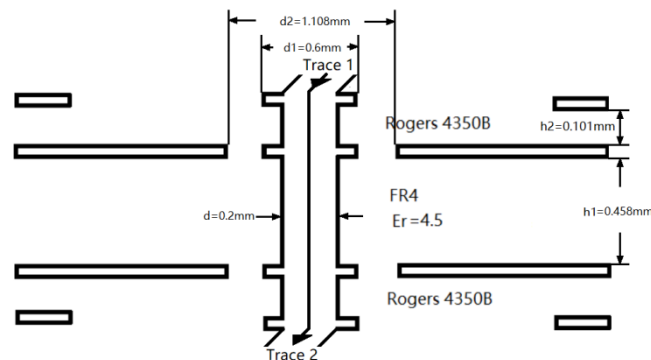


Figure 31 Details for Signal Vias

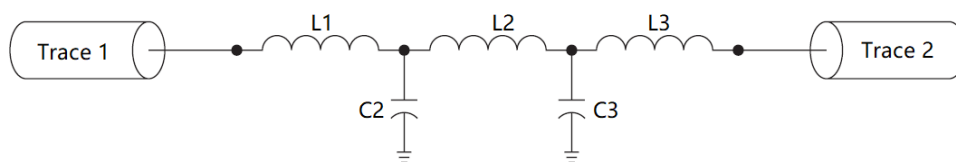


Figure 32 Cascaded Model for Signal Via [27]

According to the Equation 4.5, ϵ_r is 4.5, d_1 is 0.6mm, d_2 is 1.108mm, h_1 is 0.458mm. The capacitance of the signal via is:

$$C2 = C3 = \frac{1.41\epsilon_r d_1 h_1}{d_2 - d_1} = 0.135 \text{ pF} \quad (6)$$

According to the Equation 4.6, d is 0.2 mm, h_2 is 0.101mm. The inductance of the signal via is:

$$L2 = 5.08h_1 \left[\ln \left(\frac{4h_1}{d} \right) + 1 \right] = 0.212 \text{ nH} \quad (7)$$

$$L1 = L3 = 5.08h_2 \left[\ln \left(\frac{4h_2}{d} \right) + 1 \right] = 0.022 \text{ nH} \quad (8)$$

The calculation results are small enough to ignore, so that the high frequency signal won't get negative influence by the effect of vias.

4.4 Power Management

Different components need different supply voltages to drive. In our system +2.5V, -2.5V and 5V are needed. If directly feed the voltage to the components, the PCB board need 3 connectors for voltage input, which means 3 external power supplies are needed. The final prototype in the future we will have 32 chains working together, massive number of cables and power supplies are needed if we do not have power management. The more external equipment we use, the more flexibility we have, and they will cause some additional losses during the experiment, in order to solve the multi-power supply problem, a good power management for PCB becomes necessary.

The external power supply has decided to be 12V; the DC to DC converters are used in PCB to convert the 12V into the different required voltage. The THD12-1209 can convert the voltage into $\pm 2.5V$ and TME1205S can convert the voltage into 5V. The power management method is in Figure 33.

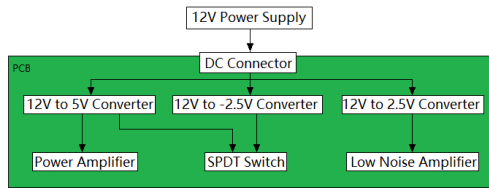


Figure 33 Power Management Method

4.5 PCB Prototype Test and Future Test Plan

In Figure 34 we present of PCB prototype. This is only a PCB prototype; we do the experiments on this PCB, find the problems and earn more experience. This will help in the next PCB design and future work.

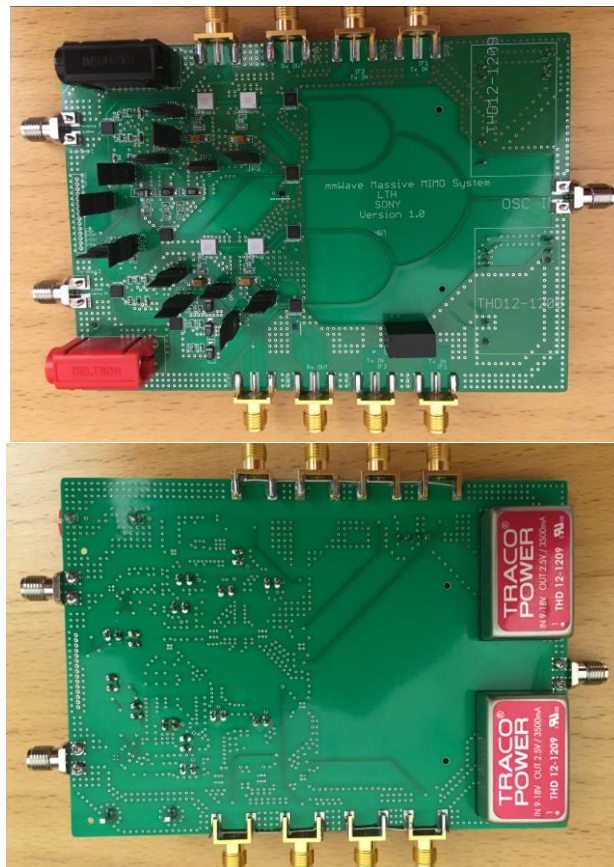


Figure 34 . PCB Outward

Same as the previously testing, firstly we are using the signal generator and spectrum analyzer to test the entire chain. Find the gain of the entire chain; observe the image rejection between higher sideband and lower sideband. If the system performance is not as good as the results on evaluation board, find the problem and solve it in the next version of PCB. Two pieces of PCB (PCB1 and PCB2) are produced together; the Tx chain testing results present in Table 10.

Table 10 PCB Tx Chain Testing Result

	Chain	Maximum Power Level	Gain Difference with Evaluation Board	Note
<i>PCB 1</i>	TX 1	PA not working		
	TX 2	-42dBm	-44dB	Not enough gain
<i>PCB 2</i>	TX 1	-7dBm	-9dB	Not enough gain
	TX 2	2dBm	0dB	IF phase different

One power amplifier on ‘PCB 1’ is not working; the issues was found by reading the current on power amplifier when the voltage drives in. One damaged amplifier can destroy the entire board, which is the reason why the gain performance on the first PCB is extremely low. Compare to the first PCB, the second board PCB has the better performance, the gain has a significantly increase, but the performance is not good as we expect. The image rejection between higher sideband and lower sideband is not good enough. The different phase input to the IF1 and IF2 ports on mixer cause the problem. In the next PCB, the mixer will be rotated in another direction, to make sure the length of the IF input microstrips are the same.

The second step, we do the over the air test using the USRP. We connect the PCB 2 ‘Tx 2’ to transmit the signal and we connect the PCB 1 ‘Rx 2’ to receive the signal . The Tx chain is transmitting a QPSK signal to the receiver side. From the receiver USRP we can observe the constellation points in Figure 35.

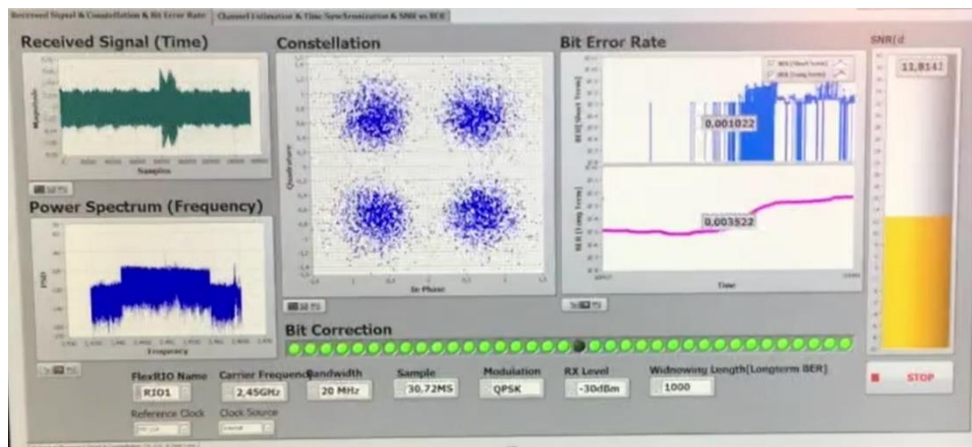


Figure 35 USRP Receiver Side

CHAPTER 5

5 Conclusion and Future Work

This chapter illustrates the thesis conclusion, what could be done in the future based on the experience and results we obtained during the design and experiment process.

5.1 Conclusion

Firstly, the system schematic architecture is proposed and implemented. The fully functional circuit diagram has been designed and achieved. Secondly, we have connected the Tx and Rx chains based on the schematic and then verified their performance.

In array antenna case, for distance in 0.36m we have free space path loss is 53.4dB in calculation and 53dB in measurement. In horn antenna case, we have free space path loss is 63dB in calculation and 62dB in measurement. The results reveal the experiments are successful.

The succeed experiments means the system block schematic is precise and then PCB can be designed and manufactured. More tests and adjustments will be done in the future on PCBs.

5.2 Future Work

The prototype test result will be the main reference in the future works. The weak received signal and poor image rejection need modifications based on the results in the future.

Regarding to the components selection, we are now using two power amplifiers with 15dB gain on the transmit chain. If we can use one power amplifier with a 30dB or higher gain instead of two 15dB gain amplifier, then the system performance will be better.

The PCB is only a demo version right now; lots of jumpers and pin headers placed on the board will help us to do the adjustment during the experiments. In the future, these parts can be removed. All the components and the related capacitors and resistors can be adjusted to a better location and make the board more perfect.

In the current phase, over the air test was from one transmit chain to another receive chain. However, in the future, there will be 32 chains working together to test the mmWave massive MIMO system. By that time the measurement result will be more rich compare to what we have now.

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