Integrated Antenna Switch for NB-IoT

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Integrated antenna switch for NB-IoT

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List of Acronyms

3GPP	3rd Generation Partnership Project
ACLR	Adjacent Channel Leakage Power Ratio
ADC	Analog to Digital Converter
BC	Body Contacts
BLE	Bluetooth Low Energy
BOX	Buried Oxide Layer
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital to Analog Converter
DC	Direct Current
DNW	Deep N-Well
DPDT	Double Pole, Double Throw
ESD	Electrostatic Discharge
FB	Floating Body
FD	Fully Depleted
FDD	Frequency Division Duplex
FEM	Front-End-Module
GaAs	Gallium Arsenide
GSM	Global System for Mobile Communications
HCI	Hot Carrier Injection
IF	Intermediate Frequency
IL	Insertion Loss
IoT	Internet of Things
ITT	Impedance Transformation Technique
LNA	Low Noise Amplifier

LO	Local Oscillator
LPF	Low Pass Filter
MMIC	Monolithic Microwave Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NB-IoT	Narrowband IoT
NF	Noise Figure
NMOS	Negative Metal Oxide Semiconductor
PA	Power Amplifier
PCB	Printed Circuit Board
PD	Partially Depleted
PNP	Positive, Negative, Positive
pPA	Pre-Power Amplifier
RF	Radio Frequency
RX	Receive
S/S	Series/Shunt
Si	Silicon
SoI	Silicon On Insulator
SP4T	Single Pole Four Throw
SPDT	Single Pole, Double Throw
SPnT	Single Pole, n Throw
T/R	Transmit/Receive
TDD	Time Division Duplex
TT	Typical-Typical
TX	Transmit
VSWR	Voltage Standing Wave Ratio

Abstract

Transistors are used in all digital devices today. The demand of faster and smaller devices such as mobile telephones and computers constantly drives the development of smaller transistor technologies. Transistors can also be used in analog applications. Today there are commercial chips with both radio and digital systems in the same package. Cellular Internet of Things (IoT) is expected to make a big impact in large quantities, which requires low-cost solutions. Most cellular communication devices needs a Front-End-Module (FEM) implemented in Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC), which is an expensive technology, or Silicon On Insulator (SoI) that offeres low leakage. The more functionality that can be integrated in to the same chip, instead of using FEM or "off-chip" components on Printed Circuit Board (PCB), the cheaper and more robust the end product will be when produced.

The focus of this master thesis is to investigate solutions that integrate the Transmit (TX)/Receive (RX) switch on bulk Complementary Metal-Oxide Semiconductor (CMOS). Three switch architectures were investigated during the thesis work. The solutions were evaluated using four metrics: insertion loss, linearity, power handling capability and bandwidth. Due to high bandwidth and power requirement for IoT, the series shunt switch was found to be the most suitable solution. The proposed solutions pass reliability tests used for typical market front-end module. A novel method for reducing insertion loss and improving switch linearity by increasing substrate resistance has been proposed.

Keywords: *T/R (Transmit/Receive) switch, RF switch, integrated RF switch, Narrowband Internet of Things (NB-IoT), CMOS, frontend*

Popular Science Summary

Integrating more to IoT

Internet of Things (IoT) is expected to grow in large scale as more and more every day devices are connected to the internet. To make it possible, small, inexpensive and low energy consuming solutions are required. A part of realizing those requirements is by integrating a full IoT-solution on a single chip.

One of the main applications suitable for NB-IoT is low data rate sensors that can be integrated to houses, refrigerators, traffic systems and much more. These sensors have to be able to function for years without any maintenance such as changing batteries. The sensor information is transmitted over air to data centers where it is processed and evaluated. The main goal of large scale IoT is to make life easier and more connected.

The new 3rd Generation Partnership Project (3GPP) Narrowband IoT (NB-IoT) standard makes it possible to connect devices in large scale to the internet via the already available cellular network. In IoT communication, the transceiver is either transmitting or receiving data. This requires a switch that can isolate the sensitive receive circuits and at the same time provide low signal attenuation. The switch is usually a separate component that is outside of the IoT system chip. By integrating the switch into the same chip as the rest of IoT system makes it possible to cut down on over all production costs.

During this thesis work multiple switch solutions have been investigated and evaluated.

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Chapter 1

Introduction

1.1 Background

Narrowband IoT (NB-IoT) is way to communicate for 'things', such as street lights, gas meters etc. that transmit small amounts of data for years using a small energy source. Billions of these 'things' are expected to be deployed, so they need to be cheap. The organization, 3rd Generation Partnership Project, responsible for NB-IoT have provided specification that allows for developing cheaper and energy efficient transceivers.

A typical transceiver consists of transmitter, receiver and a T/R switch or diplexer as shown Fig. 1.1. The transmitter consists of a Digital to Analog Converter (DAC), a mixer, a Pre-Power Amplifier (pPA) and a Power Amplifier (PA). The DAC converts the digital modulated signal to analog signal. This Intermediate Frequency (IF) signal is up-converted to Radio Frequency signal by the mixer. The pPA amplifies the RF signal and helps driving the off-chip PA. The PA further amplifies the signal to required output power which is then transmitted. The receiver consists of a Low Noise Amplifier (LNA), a mixer, a IF amplifier and a Analog to Digital Converter (ADC). The LNA amplifies the received RF signal which is then down-converted to IF by the mixer. The IF signal is them amplified further by the IF amplifier and converted to digital signal using the ADC.

A T/R switch or a diplexer is used to isolated the transmitter and receiver. A diplexer is expensive, bulky and lossy compared to a T/R switch. The T/R switch is an important block in the Radio Frequency (RF) FEM. The switch provide a conducting path from the antenna to the Low Noise Amplifier (LNA) or the Power Amplifier (PA) when receiving or transmitting, respectively. Isolation between LNA and PA is necessary when transmitting, protecting the sensitive LNA input.

NB-IoT uses half-duplex FDD and TDD, thus needing a T/R switch. A TDD system separates the communication links by using different time slots. FDD uses different frequencies during Transmit (TX) and Receive (RX).

Half-duplex communication is done by either transmitting or receiving radio during a given time-slot. This can be compared to a full-duplex radio system where the device can transmit and receive at the same time. When using full-duplex, send and receive is done at different frequency channels using two different antennas at the same time. By introducing a switch that alternates between transmitter and receiver, only one antenna is needed.

Most cellular T/R switches are part of the FEM which often are implemented in GaAs or SoI technologies. GaAs technology is well suited for RF applications because of its low losses. On the other hand, the bulk CMOS is cheap while having low performance for RF applications. Nonetheless, low performance can be traded for lower costs and ease of integration.

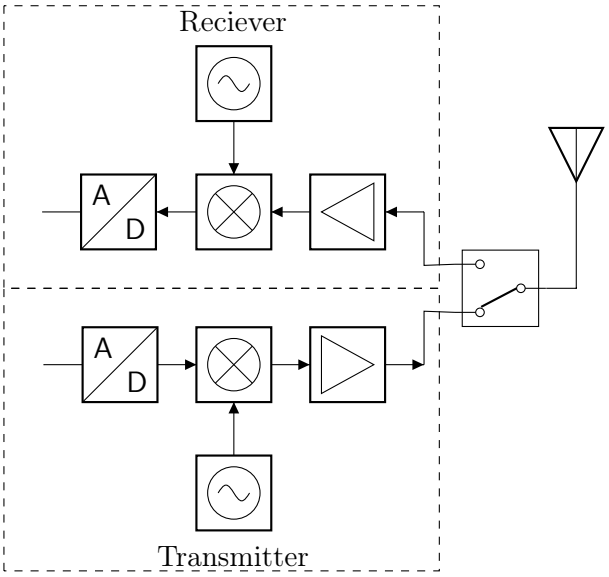


Figure 1.1: Transceiver

1.2 Targets and requirements

The switch is characterized using four metrics: insertion loss, linearity, power handling capability and bandwidth. Insertion loss the power lost when switch is on state. Linearity is a measure of distortion caused by the switch. Power handling capability is the maximum power that the switch can handle without permanent degradation in performance. Bandwidth of the switch span of frequencies for which the switch has reasonable loss.

Since the thesis focuses on a switch design for NB-IoT, the requirements have been derived using the specification provided by 3GPP [27]. Based on

the on-market solutions, the target insertion loss was decided to be 0.5 dB. The linearity, power handling capability and bandwidth are well defined by the specification, shown in in table 1.1 and 1.2. The tables below summaries the requirements.

Requirement	Value
Insertion loss	$<$ 0.5 dB
Isolation	$>$ 20 dB
Spurious Emissions	$<$ -30 dBm from 1 GHz to 12.5 GHz
OIP2	$>$ 43 dBm
OIP3	$>$ 33 dBm
Power classes	23, 20 & 14 dBm
Performance	Upto VSWR 3:1
Operation	Upto VSWR 10:1

Table 1.1: Requirements for Switch

Frequency Band	Range	Bandwidth
Ultra-low band	400-500 MHz	100 MHz
Low band	675-925 MHz	250 MHz
Mid band	1400-2200 MHz	800 MHz

Table 1.2: Frequency band for NB-IoT [27]

In Table 1.1, the OIP_2 and OIP_3 were calculated using ACLR provided by the 3GPP specification [27]. The ACLR for Global System for Mobile Communications (GSM) band is 20 dB. Using this as IM_3, it is possible to extrapolate the IP_3. A more detailed requirement for spurious emission is shown in appendix B.1. Table A.2 in appendix defines the maximum output power and tolerance for all the bands in NB-IoT. For the certification process, these requirements should be meet using a 50 Ω antenna. A on-market product needs to be more robust and handle antenna mismatch. It should perform upto a VSWR of 3 and withstand voltages upto a VSWR of 10. Isolation requirement is depending on the LNA configuration. During this work the aim was to achieve an of isolation 20 dB.

1.3 Thesis structure

The rest of the thesis is organized into following sections:

- Chapter 2: Theory - The basic functionality of a transistor is described in this chapter.
- Chapter 3: Switch topologies - An investigation of previous work is presented.
- Chapter 4: Filters - Solutions to reduce the harmonic contents are presented.
- Chapter 5: Results and conclusions - The results from simulations and conclusions.
- Chapter 6: Future Work - Outlines the next steps to improve performance of the switch

Chapter 2
Theory

2.1 MOSFET

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) acts as a voltage controlled current source. MOSFET has a drain terminal, a source terminal and a gate terminal, shown in Fig. 2.1. Apply voltage on the gate and current will flow from source to drain. The Negative Metal Oxide Semiconductor (NMOS) transistor lets electrons flow from source to drain (or the other way around) when a positive voltage is applied to the gate. In table 2.1, the three modes of operation and conditions are presented for a NMOS transistor.

	Condition	Drain current
Cut off	$0 < V_{GS} < V_{th}$	$I_D = 0$
Linear	$V_{GS} \geq V_{th}$ and $V_{DS} < V_{GS} - V_{th}$	$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$
Saturation	$V_{GS} \geq V_{th}$ and $V_{DS} > V_{GS} - V_{th}$	$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2$

Table 2.1: Modes of operation for a NMOS transistor

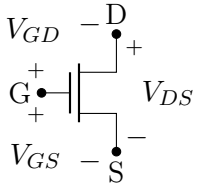


Figure 2.1: NMOS transistor voltages

The substrate used in this project is a silicon p-doped material, meaning that there is an excess of holes. The drain and source are n-doped where

there are an excess of electrons. A pn-junction is formed were the two doped materials intersect, creating a diode.

As mentioned earlier these components are mostly used in digital circuits where the signal power is minimal. The application explored in this work has to be able to handle relatively high power RF signals. The development becomes challenging because the transistor device has to operate on the verge of what it is actual capable of. The parasitic effects also has to be taken in to carefully consideration when designing, which will be explained in the following sections.

2.2 Deep-N-well device

To get better isolation between the transistor and the substrate one can use the Deep N-Well (DNW) device. This isolation makes it possible to apply a separate potential to the body of the transistor without affecting the substrate and near by devices and also keeps the device isolated from other disturbing effects such as digital switching logic. In the deep n-well process the p-substrate is illuminated with high energy negatively charged ions creating a n-type region deep within the substrate. N-doped regions are created around this deep region forming an deep n-well. A cross section of the deep n-well transistor is shown in Fig. 2.2.

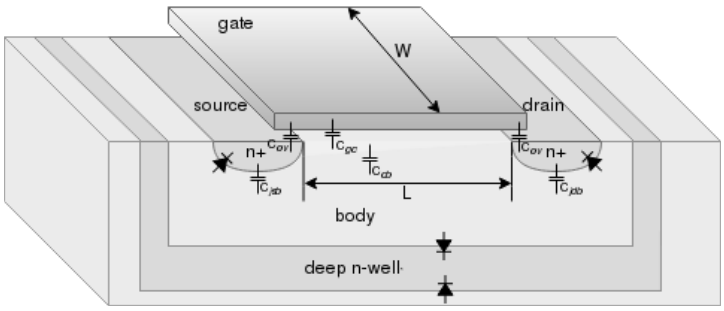


Figure 2.2: Cross-sectional view of a deep n-well NMOS transistor

2.2.1 Capacitance

Multiple intrinsic parasitic capacitances are created from the physical construction of the transistor, these capacitances can not be avoided and has to be considered when designing integrated circuits. Extrinsic capacitance arise from such as metal connections and wires in the layout and can be minimized with clever designs. A depletion region is formed when two different doped materials intersect. The width, x_d, of this region depends on

the doping levels of the materials. The junction capacitance per unit area is calculated as

$$C_j = \frac{\varepsilon_s}{x_d} \tag{2.1}$$

where $\varepsilon_s = \varepsilon_0 \varepsilon_r$ is the semiconductor permittivity.

Holes from the p-side region with a acceptor density of N_A diffuse into the n-side with a donor density of N_D and electrons from the n-side diffuse into the p-side, creating the depletion region. This continues until a steady state is reached called thermal equilibrium. That is when enough holes and electrons has diffused and an electric field is created by the ionized donors and acceptors keeps the free charge carriers apart. The electrostatic potential difference between the n-side and p-side at thermal equilibrium is called the built in potential V_{bi} and is calculated as [2]

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{2.2}$$

where n_i is intrinsic carrier concentration concentration, k is Boltzmann constant, q is the electronic charge and T is temperature in kelvin. The width in (2.1) is calculated as [2]

$$x_d = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A N_D}{N_A + N_D}\right)(V_{bi} - V)} \approx \sqrt{\frac{2\varepsilon_s (V_{bi} - V)}{q N_B}} \tag{2.3}$$

where N_B is the light doped region in an one-sided abrupt junction and V is the applied voltage to the heavy doped region. Equation (2.1) can now be written as

$$C_j = \sqrt{\frac{q\varepsilon_s N_B}{2(V_{bi} - V)}} \tag{2.4}$$

Fig. 2.2 shows the main parasitic capacitances contributors within the MOSFET device. The reverse-biased junctions formed between the heavy n-doped source and drain regions and the light p-doped body creates parasitic capacitances C_{jdb} and C_{jsb}. The total junction capacitance are dependent on the physical shape of the drain and source regions.

During manufacturing the drain and source regions tend to extend slightly in under the gate. This is highly unwanted because it creates parasitic overlap capacitance, C_{ov}. The overlap distance, L_D, can be estimated as 2/3 to 3/4 of the diffusion depth for source or drain regions. The total overlap capacitance can be estimated as [1]

$$C_{ov} = \frac{\varepsilon_{ox}}{t_{ox}} W L_D = C_{ox} W L_D \tag{2.5}$$

where ε_{ox} is the oxide's dielectric constant and t_{ox} is the oxide thickness.

When voltage is applied to the gate, a channel is formed and current can flow from source to drain or vice versa. The gate-potential attracts the few free electrons (for a NMOS transistor) in the p-doped body making the region closest to the gate n-doped. Two junction capacitances are formed, gate to channel, C_{gc}, and channel to body, C_{cb}. The total capacitance for this junctions are estimated as [1]

$$C_{gc} = C_{ox}W(L - 2L_D) \tag{2.6}$$

and

$$C_{cb} = \frac{\varepsilon_s}{x_d}W(L - 2L_D) \tag{2.7}$$

Since the overlap distance, L_D, reduces the total channel length, L, on both sides, hence the $L - 2L_D$ term.

When operating the transistor as a switch two regions of operation are interesting, off-mode and linear-mode. Depending on region of operation, the capacitance will vary. When no channel is formed and the transistor operates in off-mode the only contribution to gate-source and gate-drain capacitance are the overlap capacitance. The gate-body capacitance is varies between just C_{gc} or the series combination of C_{gc} and C_{cb}. In saturation the gate-body capacitance can be neglected because the channel forming under the gate isolates the the gate form the body.

In linear mode there are a channel between the source and drain regions and it is assumed that source and drain share the same charge. Half of C_{gc} and one C_{ov} adds to each of C_{gs} and C_{gd} and half of C_{cb} and C_{jsb}/C_{jdb} adds to each of C_{sb} and C_{db}.

In saturation the potential variations at the drain doesn't change the channel charge and there for the only contribution to C_{gd} is the overlap capacitance C_{ov}. The channel capacitance adds to the total C_{gs} capacitance by 2/3 of C_{gc} because of the channel. The same applies to the C_{sb} where 2/3 of C_{cb} adds to the total capacitance and the only contribution to C_{db} is the C_{ov}. The C_{gb} capacitance is assumed to be near or equal to zero when operating in linear or saturation due to the channel acting as an isolating layer between gate and body. A summary is presented in table 2.2 [1].

One more yet not described parasitic capacitance is the drain-source capacitance that arises from the layout. The transistors are usually divided in to multiple fingers when dealing with large devices, such as RF-switches. The metal wires that connect source and drain will have some mutual coupling creating parasitic capacitance C_{ds} [6]. Fig. 2.3 shows only the described capacitances from Fig. 2.2.

The capacitances described in this section are the main contributors to the overall parasitic capacitance. When using the provided computer

Table 2.2: Approximate MOSFET intrinsic terminal capacitances

	Off	Linear	Saturation
C_{gs}	C_{ov}	$C_{gc}/2 + C_{ov}$	$2C_{gc}/3 + C_{ov}$
C_{gd}	C_{ov}	$C_{gc}/2 + C_{ov}$	C_{ov}
C_{gb}	$C_{gc}C_{cb}/(C_{gc} + C_{cb}) < C_{gb} < C_{gc}$	0	0
C_{sb}	C_{jsb}	$C_{cb}/2 + C_{jsb}$	$2C_{cb}/3 + C_{jsb}$
C_{db}	C_{jdb}	$C_{cb}/2 + C_{jdb}$	C_{jdb}

models of transistors a lot more parasitic elements are taken in to consideration. Simplifying the circuit in Fig. 2.3 by using Y-Δ transformation of C_{gd}, C_{db}, C_{gb} into C_1, C_2, C_3, the total capacitance is calculated as:

$$C_{total} = C_{ds} + \frac{C_1\left(\frac{C_3C_{gs}}{C_3+C_{gs}}\frac{C_2C_{sb}}{C_2+C_{sb}}\right)}{C_1 + \left(\frac{C_3C_{gs}}{C_3+C_{gs}}\frac{C_2C_{sb}}{C_2+C_{sb}}\right)} \tag{2.8}$$

where

$$C_1 = \left(\frac{C_{gd}}{C_{db}C_{gb} + C_{gd}C_{gb} + C_{gd}C_{db}}\right)^{-1} \tag{2.9}$$

$$C_2 = \left(\frac{C_{db}}{C_{db}C_{gb} + C_{gd}C_{gb} + C_{gd}C_{db}}\right)^{-1} \tag{2.10}$$

$$C_3 = \left(\frac{C_{gb}}{C_{db}C_{gb} + C_{gd}C_{gb} + C_{gd}C_{db}}\right)^{-1} \tag{2.11}$$

2.2.2 Resistance

When designing a switch it is desired to keep the resistance low in on-mode and high in off-mode. The on-resistance between drain and source operating in linear region, R_{on}, is calculated with equation (2.12) [3] where it is clear that resistance scales with the W/L-ratio. Making the transistor wide will lower the resistance.

$$R_{on} = \left(\frac{\delta I_D}{\delta V_{DS}}\right)^{-1} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th} - V_{DS})} \tag{2.12}$$

where I_D is the drain current, V_{DS} is the drain-source voltage, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage and μ_n is the mobility of electrons.

When ground voltage is applied to the gate and the resistor is operating in off-mode, no channel is formed under the gate and no current can flow between drain to source.

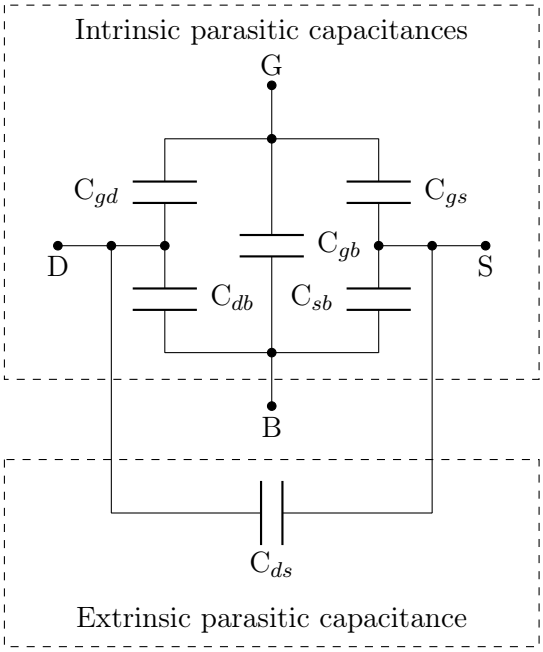


Figure 2.3: Capacitance model of a deep-N-well transistor

2.2.3 R_{on} vs. C_{off}

When designing a switch for RF-signals both resistance and capacitance must be taken in to careful consideration. Most important is to keep the on-resistance, R_{on}, and off-capacitance, C_{off}, as low as possible. Low capacitance is important when having transistors in off-mode interfacing the RF-signal path. As mentioned earlier, on-resistance is lowered by wide transistors and capacitance is lowered by small transistors.

By using the simulation tools it is possible to find the best W/L-ratio with respect to the time constant $\tau = R_{on} \cdot C_{off}$.

2.2.4 Diodes

There are multiple diodes shown in Fig. 2.2. The diodes are, as mentioned in section 2.2.1, caused by n- and p-doped interfaces within the transistor.

Junction diodes

Two junction diodes are formed between n-doped drain and source and the p-doped body. These junction diodes must be reverse biased at all time. If a junction diode becomes forward biased or reach breakdown, RF-signal will leak, increasing Insertion Loss (IL) and cause distortion of the signal.

Voltage applied to the drain or source should not exceed junction threshold voltage, $V_{j,th}$, and breakdown voltage, $V_{j,bd}$. Since $V_{j,th} < |V_{j,bd}|$, it is $V_{j,th}$ that sets the limit, as described with the condition in (2.13). Fig. 2.4 shows a larger version of a junction diode.

$$|V_{D/S,peak}| < V_{j,th} < |V_{j,bd}| \tag{2.13}$$

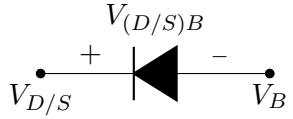


Figure 2.4: Junction diode

This criteria can be hard to maintain when dealing with relatively high RF-signals which causes large voltage swings at drain and source junctions. Possible solutions are presented in chapter 3.

Deep N-well diodes

Due to the DNW, two back-to-back connected diodes are formed between the body and substrate, increasing RF-isolation and isolating from disturbances such as switching logic transistors. This is done by connecting supply voltage to the Deep N-Well (DNW) and keep the body grounded and substrate grounded.

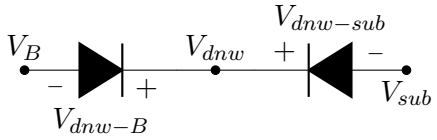


Figure 2.5: Back to back deep-N-well diodes

2.2.5 Insertion Loss in MOSFET

The effect insertion loss by substrate resistance

Using a simplified small-signal model as shown in Fig. 2.6, [7] have investigated the the effect of substrate coupling on IL. To quantify the IL they have investigated a single transistor where source and drain are terminated with characteristic impedance Z_0.

The total capacitance in Fig. 2.6 is given by,

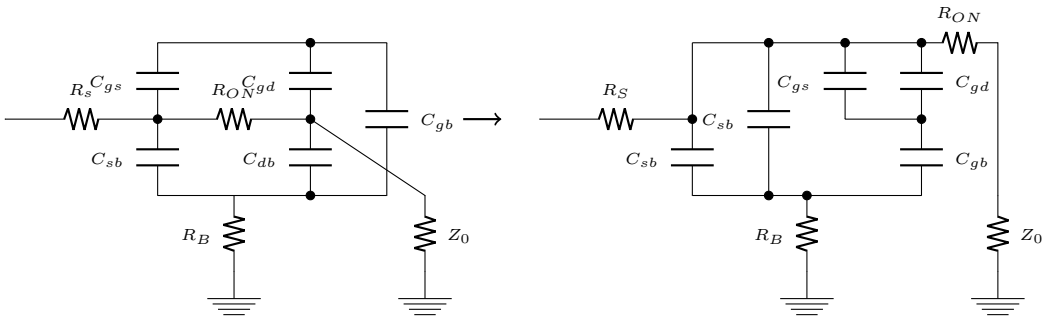


Figure 2.6: Small-signal model of on-switch

$$C_T = C_{db} + C_{sb} + \frac{(C_{gd} + C_{gs})C_{gb}}{C_{gd} + C_{gs} + C_{gb}} \tag{2.14}$$

Since C_{gb} is negligible in triode region, (2.14) can be simplified to

$$C_T = C_{db} + C_{sb} \tag{2.15}$$

The IL is then given by,

$$\text{IL} = \frac{1}{|S_{21}|^2} = \frac{(R_{ON} + 2Z_0)^2 + (\omega C_T)^2[(R_{ON} + 2Z_0)R_B + (R_{ON} + 2Z_0)Z_0]^2}{(2Z_0)^2(1 + (\omega C_T R_B)^2)} \tag{2.16}$$

If C_T is zero, (2.16) simplifies to (2.17) and the IL at low frequencies and is given by,

$$\text{IL} = \frac{1}{|S_{21}|^2} = \frac{(R_{ON} + 2Z_0)^2}{(2Z_0)^2} \tag{2.17}$$

Varying the R_B, [7] have shown that maximum IL is obtained when substrate resistance is around 80-100 Ω at characteristics impedance of 50 Ω. IL can minimized by either increasing the substrate resistance or reducing it close to zero. Reducing Z_0 to 30 Ohms can help the IL at the typical substrate impedance (80-100 Ω) but its not as effective as increasing the substrate impedance.

Based on this results, researchers have proposed techniques such as LC tuned body floating and resistive body floating using triple-well devices to minimize insertion loss by increasing the substrate resistance.

Insertion loss in a triple-well device

Fig. 2.8 shows the small signal model of a triple-well device. The gate is connected with a large resistor so it can be considered as floating. The body

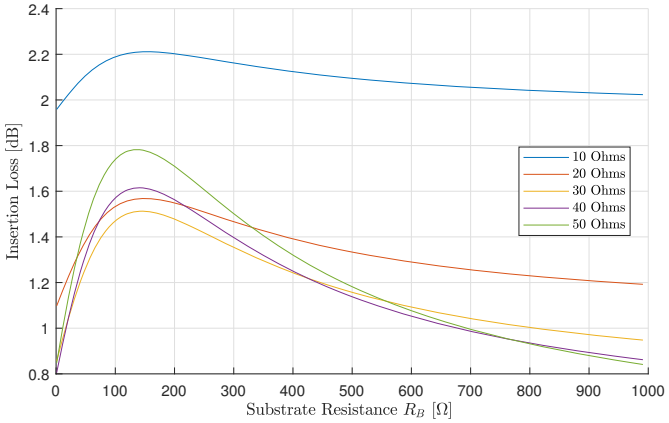


Figure 2.7: Insertion loss with respect to substrate resistance [7]

is also floating and connected to ground via the parasitic capacitance from the n-well.

At low frequencies, the loss I_1 and I_3 are negligible and I_{Load} is equal to I_2. So the majority of loss is caused by on-resistance of the switch. At higher frequencies, I_1 and I_3 are considerably higher and thus we have $I_{Leakage}$ going through the substrate to ground.

$$\text{IL} = \frac{1}{|S_{21}|^2} = \frac{P_{available}}{P_{load}} = \frac{P_{load} + P_{R_{ON}||C_{DS}||C_{BS}} + P_{loss,sub}}{P_{load}} \tag{2.18}$$

$$P_{load} = \frac{1}{2} I_{load}^2 Z_{load} \tag{2.19}$$

$$P_{R_{ON}||C_{DS}||C_{BS}} = \frac{1}{2} I_2^2 R_{ON} \tag{2.20}$$

$$P_{loss,sub} = \frac{1}{2} I_{leakage}^2 R_{sub} \tag{2.21}$$

From above equations, there are two main contributors of losses; R_{ON} and R_{SUB}. Losses due to R_{ON} are frequency independent. Since the IL of the switch is frequency dependent, we can conclude that majority of losses are dominated by substrate losses.

Using a triple-well device to increase substrate resistance gives better performance than a dual-bulk transistor. The substrate losses are still dominating even with the extra isolation of the n-well. If the depletion capacitances, $C_{dnw-pwell}$ and $C_{dnw-psub}$, are reduced to a few femto farads or the

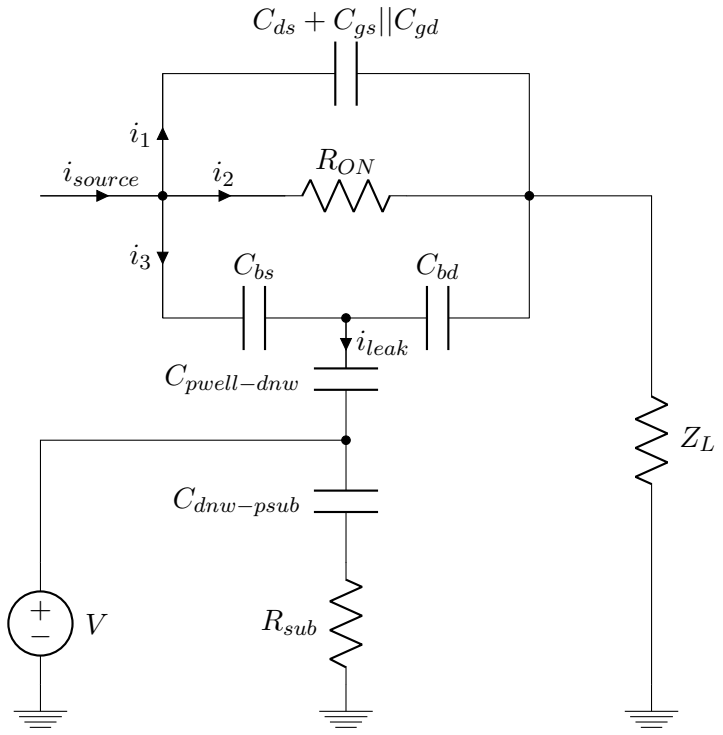


Figure 2.8: Small-signal model triple-well device [10]

substrate resistance, R_{sub}, is increased to kΩ, then $I_{leakage}$ becomes negligible and the substrate losses reduce close to zero. By biasing the the n-well with a voltage potential higher than the body and substrate potential, it is possible to reduce depletion capacitance shown in [10].

An alternative to reduce losses is by forming a deep n-well ring around the complete switch design, as shown in 2.9. The substrate in the ring is isolated from ground by using a 100 kΩ resistor. Although the n-well ring doesn't completely isolate the switch p-substrate from the rest of the chip, it increases the substrate resistance to a few kΩ. There also needs to be reasonable clearance between the deep n-well ring and any-other body contact.

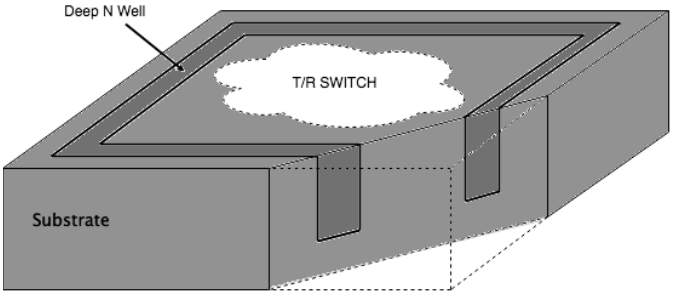


Figure 2.9: Cross-sectional view of a deep-well isolating ring

In [9], authors has proposed a novel substrate isolation technique to increase body impedance of the series TX switch as an alternative to using a triple-well device. They accomplish this by blocking the p-implants near the switch while remotely biasing the body of the transistors through a high resistivity substrate. The body isolation technique is illustrated in Fig. 2.10.

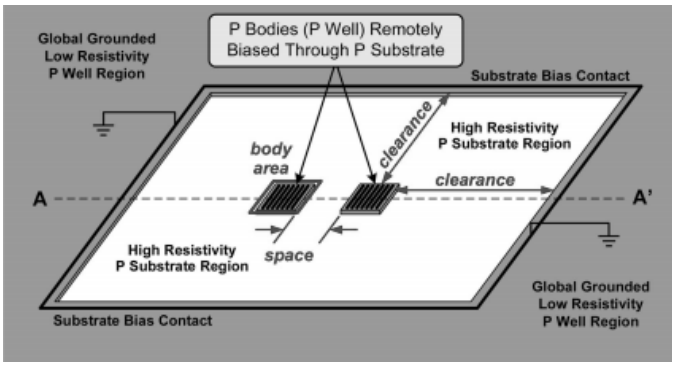


Figure 2.10: Body isolation technique [9]

2.2.6 Reliability in MOSFET

Impact Ionization

Impact ionization is becoming more significant for short channel devices as reduction in channel length can lead to strong lateral electric fields. This can create something called the *hot carriers*. If these hot carriers collide with atom of silicon lattice, they can knock out electrons from valance to conduction band. This creates an electron-hole pair. The electrons move towards the drain while holes are attracted to the bulk. A parasitic bipolar Positive, Negative, Positive (PNP) transistor is formed between the source-bulk-drain, as shown in Fig. 2.11. If too many holes are created due to

collision from hot carriers, the parasitic PNP transistor can turn-on due to parasitic resistance in the bulk. This can lead to creation of more electron-hole pairs and cannot be controlled by the gate voltage. If these electrons become hot carries as well then it can cause a avalanche leading to device failure.

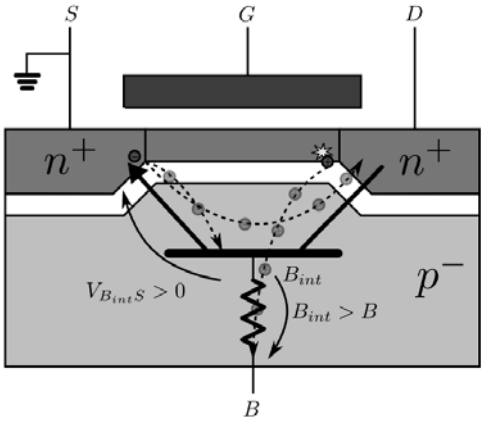


Figure 2.11: Impact ionization of a NMOS transistor [26]

To avoid impact ionization, special care has to be taken in to account to reduce the bulk resistance by putting p-well contacts close enough to the transistor. Using techniques such as floating body switches, it is important to make sure that the junction diode is reverse biased [3].

Hot Carrier Injection

As explained earlier, the hot carrier generated due to strong electric fields. These hot carriers can get trapped in gate-oxide instead of going to the drain contact. This causes *ageing* of transistors which changes the electrical characteristics such threshold voltage, current factor and output conductance of the transistors. HCI doesn't cause device failure but reduces the life of the transistors. HCI can be a problem for transistors in off-mode that might have high V_{DS} when used in high power RF applications. A solution is stacking of transistors, which on the other hand increases the over all IL.

2.3 Silicon on Insulator

The SoI technique has been used since early 2000. It was developed to solve the fundamental physic limits of bulk-Si transistors as they are constantly scaled down to smaller and smaller devices. Problems arise when scaling, resulting in thinner gate insulation that leads to tunneling currents and leakages from the junction diodes as the junctions gets shallower. SoI have less parasitic capacitance, is less temperature dependent, no latch-up, high resistivity substrate and can handle higher voltages. The main physical difference between bulk-Si and SoI is the extra isolating layer of silicon dioxide in the bulk called the Buried Oxide Layer (BOX). The BOX layer is located just below the surface of the silicon wafer. The drain and source regions are stretching all the way down to the BOX layer, leaving only a small body-region between the terminals as shown in Fig. 2.12.

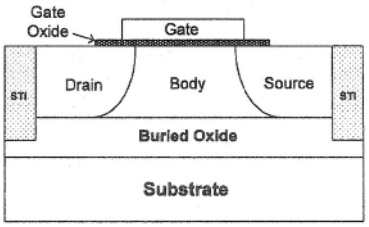


Figure 2.12: Cross-sectional view of a SoI transistor [17]

There are two main types of SoI transistors, Fully Depleted (FD) and Partially Depleted (PD). In linear mode only parts of the body is depleted in PD devices, while the whole body is depleted in FD devices. The junction diodes are only interfacing the body at one side, reducing the leakage significantly. It is possible to isolate each transistor by a oxide region down to the BOX layer between each device. The capacitance model of an SoI transistor is shown in Fig. 2.13. The body-substrate capacitance, C_{bs}, is small because of the BOX layer and can be neglected. The drain-body and source-body capacitance are significantly smaller than the corresponding capacitance of a standard bulk-Si transistor because of the smaller junction areas [5].

In [5] it is mentioned that SoI has a benefit when designing T/R switches. A comparison between a bulk-Si switch and a SoI switch with similar requirements state that both insertion loss and isolation improves with SoI technique.

The authors of [17] have developed a PD SoI S/S switch where a combination of devices with Body Contacts (BC) and Floating Body (FB) devices are used. Small FB devices have lower drain-source capacitance resulting

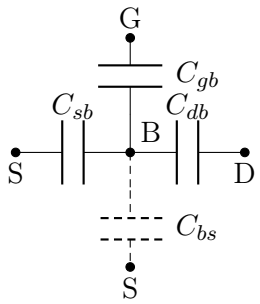


Figure 2.13: Capacitance model of a SoI transistor

in better isolation, C_{sb} in parallel with C_{db}, and are used as main switches. Authors mention that there are stability issues with FB devices that has to be further investigated. The BC devices offers more stability and are used in all other cases.

The proposed switch in [18] claim power handling capability of +35 dBm with low harmonic generation and an insertion loss below 1 dB using SoI technique. The proposed switch uses a series-shunt topology with stacked SoI transistors. Authors metricize the time constant $\tau = R_{ON}C_{OFF}$ and present different switch setups.

2.4 Mismatch and VSWR

The Voltage Standing Wave Ratio (VSWR) is a measurement of impedance matching between the load and the characteristic impedance of the system. In a matched system, all of the signal power is delivered to the load. In an unmatched system, the load is not equal to the characteristic impedance and the transmitted RF signal is reflected back in to the system. The reflected signal will cause either an increase or a decrease of the signal power delivered to the load by constructive or destructive interference.

The impedance of a load is described by

$$Z_L = R_L + jX_L \tag{2.22}$$

The characteristic impedance of the system is in the same way described as

$$Z_0 = R_0 + jX_0 \tag{2.23}$$

The reflection coefficient (Γ) is calculated as

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.24}$$

The VSWR is calculated as

$$\text{VSWR} = \frac{\Gamma + 1}{\Gamma - 1} \tag{2.25}$$

The extremes are presented in table 2.3.

Short-circuit	$Z_L = 0$	$\Gamma = -1$	VSWR $= 0$
Matched	$Z_L = Z_0$	$\Gamma = 0$	VSWR $= 1$
Open-circuit	$Z_L = \text{inf}$	$\Gamma = 1$	VSWR $= \text{inf}$

Table 2.3: Impact of load impedance

Shown in [24], the antenna impedance change depending on the close by surroundings. If the VSWR becomes large during transmitting, large constructive reflections will occur that can damage or even destroy RF equipment such as the switch.

As specified in table 1.1, it is desired that the switch withstands a VSWR of 10 and perform up to a VSWR of 3.

Chapter 3
Switch topologies

In this chapter different topologies studied during the thesis work are presented.

3.1 Switch architectures

The requirement of covering a large frequency span and high transmit power results in two types of switches:

- **Single pole, n throw switch**
  The Single Pole, n Throw (SPnT) architecture offers more than one input and output pair connected to a single antenna port. By using multiple inputs and outputs it is possible to have special designed PAs and LNAs that covers separate frequency bands. The switches requires to cover a large frequency span. In most cases this is a ideal solution but not always possible when transmitting at high power. The increase of input and output pairs comes with the cost of increased IL. A benefit is that only one antenna connection is needed. A SP4T switch is shown in Fig. 3.1.

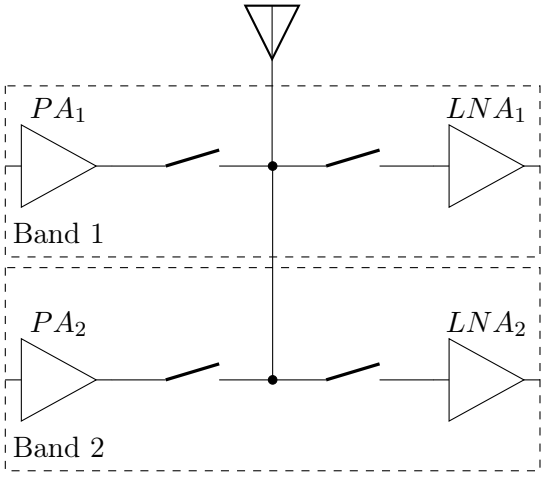


Figure 3.1: Single pole, four throw switch

- **Double pole, double throw switch**
  The DPDT switch has multiple antenna outputs where each output is connected one output and input. Each covered frequency band has its own separate antenna port. This design results in lower IL since each switch can be individually designed to perform best for a certain frequency band. A DPDT switch is shown in Fig. 3.2. According to 3GPP specifications [27], NB-IoT doesn't support mobility which allows to have only one functional band. The antenna port that covers the unused band can be terminated to ground.

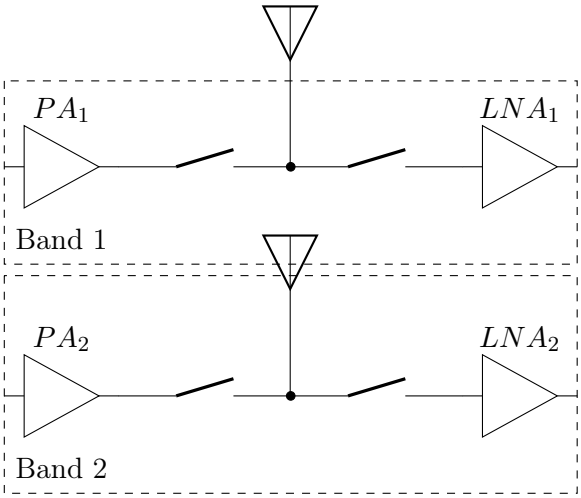


Figure 3.2: Double throw, double pole switch

3.2 Series-shunt switch topology

The series/shunt switch is one of the most basic switch designs. It is a scalable design and can be configured as all kind of switch types. The design allows for multiple PA and LNA designs that each covers a separate frequency band. Fig. 3.3 shows a series/shunt SPDT T/R topology.

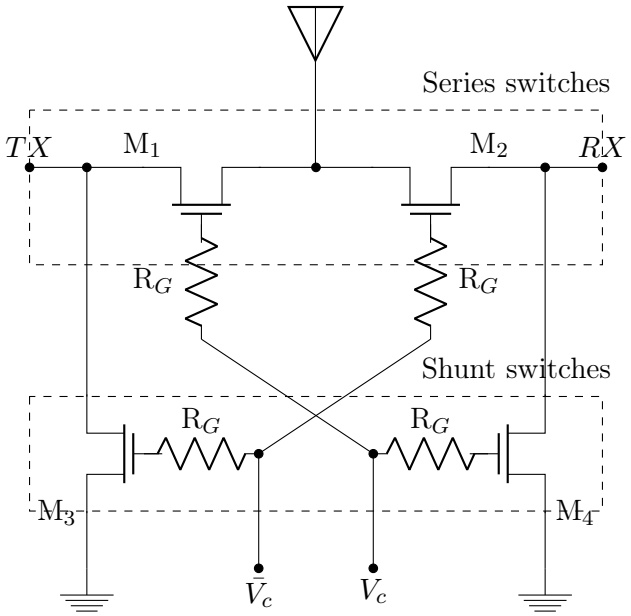


Figure 3.3: SPDT T/R switch

The series transistors, M_1 and M_2, functions as the actual switch for TX and RX paths. Transistors M_3 and M_4 are shunt switches and turns on when M_1 or M_2 are off, respectively, pulling the undesired leaked signal to ground. When transmitting, the control voltage V_c is high and M_1 is turned on allowing the RF signal to pass from the PA to the antenna and isolating the LNA by turning off M_2. When receiving, $\bar{V}_c$ is high, allowing signals from the antenna to pass to the LNA and isolating the PA.

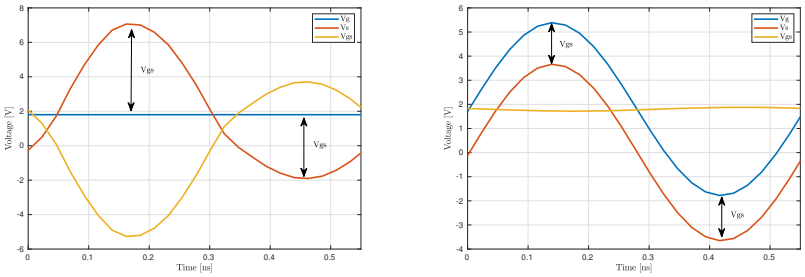
As the shunt switches help with isolation, they also adds parasitic capacitance when in off-mode as mentioned in section 2.2.1. In switch designs where only one PA is used, the PA-shunt arm could be removed if it is possible to turn of the transmission when receiving. When multiple PAs are connected to the same antenna port, isolation is more important and shunt arm should be used.

As mentioned in 2.2.4, it is critical to ensure that all junctions are reverse biased to maintain performance and reduce signal leakage. Voltage swings when transmitting RF signals are usually higher than what a transistor can

handle as a standalone device. Ways to solve this problem are presented in following subsections.

3.2.1 Floating body and gate

To reduce signal leakage and increase the bias isolation, large value resistors are connected to gate and body of the transistors handling RF-signals. The resistors bootstraps gate-drain and gate-source and limits the voltage fluctuation across terminals which would otherwise change the channel resistance and cause a high voltage swing over the gate-oxide. The price of large gate resistor is that it limits charging and discharging of gate capacitance, resulting in an increased switching time. Switching time is not a limiting factor for RF-switches. Figure 3.4a shows voltage of V_{gs} without floating resistor. In Fig. 3.4b it is shown that V_{gs} is low and the gate voltage follows the source.



(a) Gate-source voltage without floating resistor

(b) Gate-source voltage with floating resistor

Figure 3.4: Impact of floating resistor

Floating body resistor is used for two reasons. First, it helps in bootstrapping the drain/source to body diodes similar to gate-source voltage. Secondly, it helps in reducing insertion loss as mentioned in section 2.2.5.

3.2.2 Inductive substrate bias

As mentioned in section 3.2.1, using body floating technique can improve insertion loss and linearity. Another technique to achieve the same functionality is to use inductive substrate biasing. A floating body node can be created by connecting the substrate through a inductor as it acts as high impedance at higher frequencies. Inductive substrate biasing also prevents latch-up even if the drain/source-body diode gets forward biased as the current is severely limited due to the impedance of inductor. This also improves insertion loss based on analysis in section 2.2.5.

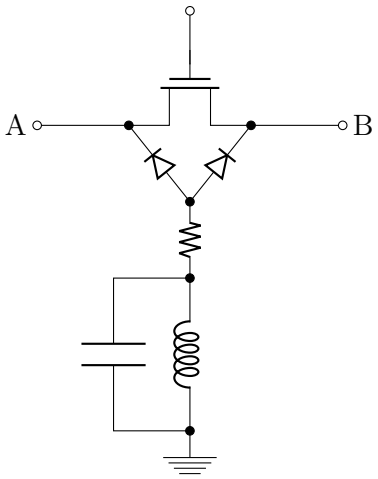


Figure 3.5: Inductive Substrate Biasing

On-chip inductors has high parasitic capacitance, making it is difficult to use them as RF chokes. A solution is to use a LC-tank tuned to the operating frequency, creating a high impedance node connected to the body. The drawback of this technique is that it becomes narrowband and require more area due to the inductor.

3.2.3 Negative bias

The usage of DNW devices opens up the possibility of biasing the body with a separate voltage. The potential difference between the junctions drain to body and source to body will increase leaving more headroom for voltage swings and help with reducing the distortion by clipping of the RF-signal. Introducing negative body biasing, V_b to (2.13) gives

$$|V_{D/S,peak}| < V_{j,th} + V_B < |V_{j,bd} + V_B| \tag{3.1}$$

Fig. 3.6 shows the impact of negative body biasing. It is clear that a signal without any DC-component exceeds the threshold voltage of the diode during the negative half cycle. Lowering the body potential lowers the threshold voltage and no clipping occurs.

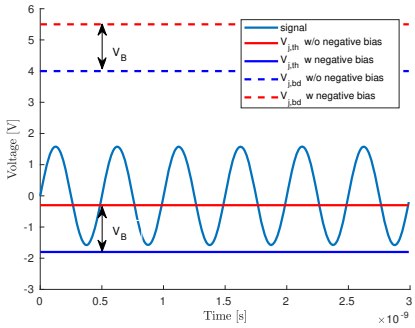


Figure 3.6: Impact of negative body biasing

Although negative body biasing increases the V_{th} of the device, it reduces the IL caused by the loss through substrate.

By using a charge pump, such as [20], negative voltage could be generated for biasing of the DNW devices. The generated voltage has to be heavily filtered to avoid introducing interference or doesn't affect the RF signal.

3.2.4 Stacking

By connecting multiple transistors in series, as shown in Fig. 3.7, it is possible to lower the voltages over each transistor allowing to withstand higher power [8]. There are different challenges when operation in on and off mode and a trade off must be made.

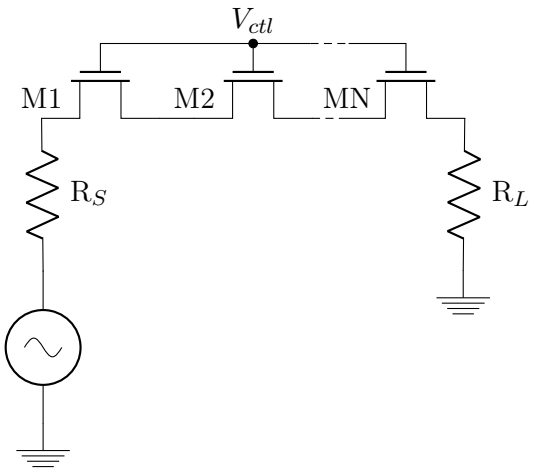
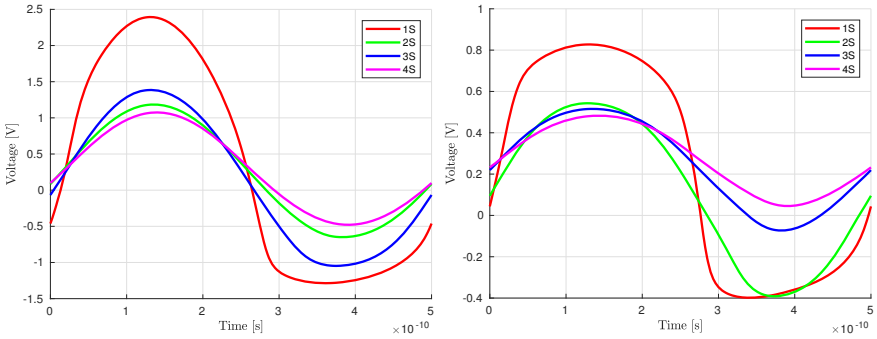


Figure 3.7: Transistor stacking



(a) Drain-source voltages **(b)** Gate source voltages

Figure 3.8: Impact of stacking devices

ON-mode

In on-mode there are losses from each transistor caused by current leakage and voltage drop over each on-resistance which adds to the total insertion loss. The losses due to stacking has to be weighted against the number of

devices necessary to keep the transistors off when operating the switch in off-mode.

OFF-mode

The condition for off-state is problematic to maintain when V_{ctl} is low. The transistor turns on since the RF signal present at the drain/source has a voltage swing that exceeds the threshold voltage, V_{th}. The interfacing signal will get distorted if an off-switch turns on in a SPnT configuration. Fig. 3.8 shows how the gate-source and drain-source voltages for the first transistor interfacing the RF signal decreases when stacking is increased. The impact of stacking are further discussed in following sections.

3.2.5 Feed-forward capacitors

A capacitor can be used to improve the capability of keeping the switch in off-mode by connecting it between drain and gate. This allows the gate to follow the drain voltage, making sure that the condition for linear operation is maintained. This also ease the high voltage swing on the first transistor interfacing the RF signal and allows for a more evenly signal distribution over the stacked transistors.

Feed forward capacitors are also used to provide following between drain and body, ensuring that the junction diodes are kept reverse biased [8].

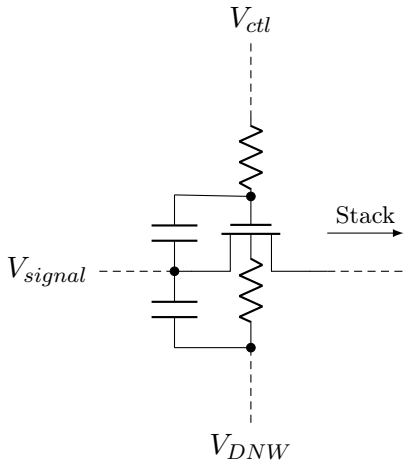


Figure 3.9: Feed-forward connected capacitors

3.2.6 Impedance transformation

For given power, voltage is dependent on resistance and is given by the following equation.

$$V = \sqrt{P * R} \tag{3.2}$$

As the resistance is reduced, the voltage decreases for given power level. Impedance transformation can be handy for delivering high power in modern CMOS technology as the devices handle current better than voltage.

As mentioned in section 3.2.4, stacking is needed to handle high power. The RX side needs stacking to withstand high voltage during off-state. This also increases the IL on RX side.

Authors of [11] propose a Impedance Transformation Technique (ITT) that lowers the RF voltage swings in the switch and hence lower the required stacking in the RX switch setup. A matching network is used at the output to transform the impedance back to the interfacing antenna impedance, usually 50 Ω. The simplest matching network is the LC match, consisting of a series capacitor and a shunted inductance to ground. The efficiency of LC match is given by (3.3). It is mentioned that the losses from the two matching networks increase the IL and the receiver Noise Figure (NF). Due to the lower voltages it is possible to balance the losses from stacking and from matching network.

$$\eta_{LC} = \frac{Q^2 + 1}{Q^2 + \frac{r + \sqrt{r_2 + 4Q^2(r-1)}}{2}} \tag{3.3}$$

where Q is the quality factor of the inductor used in the matching network, and r is the impedance transformation ratio, which is R_{load}/R_{in}. Since the efficiency of matching network is dependent on the Q of the inductor, the losses can be reduced by using an off-chip matching network. Using the small signal model shown in section 2.2.5, it is possible to calculate the efficiency of the switch for a particular operating impedance by using (3.4).

$$\eta_{SW} = \frac{R_{SW}}{R_{ON} + R_{sub}(\omega C_T)^2 \frac{(R_{SW}+R_{ON})^2}{1+(\omega C_T R_{sub})^2} + R_{SW}} \tag{3.4}$$

Where R_{ON} is the on-resistance of the switch, R_{SW} is the switch operation resistance, C_T is the total parasitic capacitance and R_{sub} is the substrate resistance.

By using (3.3) and (3.4) it is possible to analyze the total loss of the switch. According to the equations, the lowest RX IL is archived when the

switch operating impedance is set to 50 Ω. The power handling increases with lower operating impedance and higher stacking, as expected.

3.3 DC-block topology

This solution is similar to the negative bias topology. Instead of lowering the body potential, the drain/source potential is raised. The main benefit with DC-block topology doesn't require a negative voltage source.

In the DC-block switch topology, shown in Fig. 3.10, the drain/source voltage are raised to a higher potential during off-state. This helps keeping the junction diodes revere biased and the switch in a stable off-state. The gate and source voltages for an switch in off-state are shown in in Fig. 3.11 where it is clear that V_{gs} always is below zero. Large capacitors connected to source and drain are blocking the DC voltage from interfering with PA, LNA and antenna. The DC-block capacitors must have low impedance, not to degrade the RF signal.

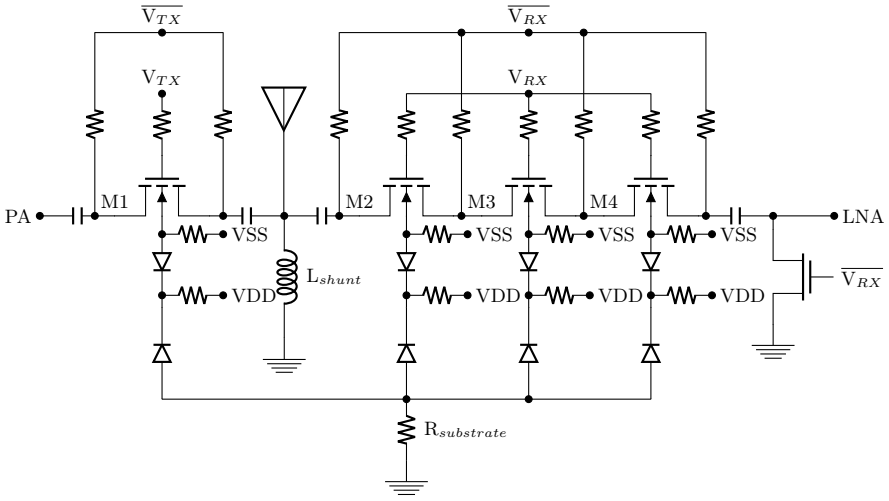


Figure 3.10: DC-block switch schematic

During on-state, drain/source terminals are left floated via large resistors, the gate is connected to VDD and follows the RF signal by using floating resistors.

An issue with dc-block switch is the large on-chip DC-block capacitors. Not only that they have require a large area, they have parasitic coupling capacitance to substrate. This parasitic capacitance causes losses as shown in Fig. 3.12. The parasitic capacitance be can reduce by having the on-chip capacitors on higher metal layers. By using a shunt inductor at the output,

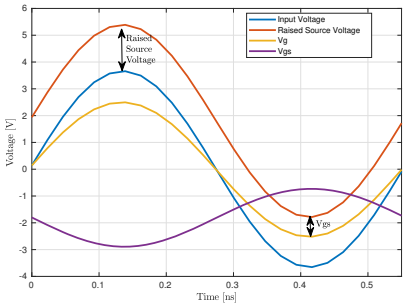


Figure 3.11: DC-block voltages

we can resonate the effect of this parasitic capacitance. Resonating reduces the bandwidth capability of the switch. Nonetheless, the switch is usable for particular bands and the shunt inductor provides ESD protection.

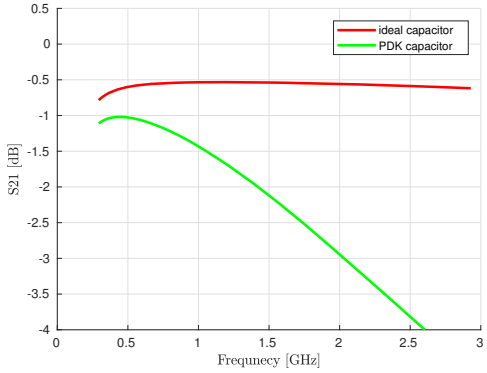


Figure 3.12: Impact of PSK capacitor

3.4 Resonance topology

This topology, shown in Fig. 3.13, employs a parallel LC circuit to create high impedance path on the RX side by reusing the LNA matching network and uses a conventional CMOS switch in TX path. By using a variable resonance circuit in series with the LNA it is possible to block the transmitted RF signal from interfering with the LNA without degrading the LNA NF during RX-mode.

Impedance of the inductor and capacitor as a function of ω is given by (3.5) and (3.6), respectively.

$$Z_L(\omega) = j\omega L + R_L(\omega) = j\omega L + \frac{\omega L}{Q_L} \tag{3.5}$$

where Q_L is the quality factor of the inductor.

$$Z_C(\omega) = \frac{1}{j\omega C} \tag{3.6}$$

Impedance of parallel LC tank is given by

$$Z(\omega) = \frac{Z_L(\omega)Z_C(\omega)}{Z_L(\omega) + Z_C(\omega)} \tag{3.7}$$

which simplifies to,

$$Z(\omega) = -j\left(\frac{1}{C}\right)\left(\frac{\omega}{\omega^2 - \omega_0^2}\right) \tag{3.8}$$

where,

$$\omega_0 = \frac{1}{\sqrt{LC\left(1 + \frac{1}{Q_L}\right)}} \tag{3.9}$$

Using (3.8),

$$\lim_{\omega \to \pm\omega_0} Z(\omega) = \infty \tag{3.10}$$

From equation (3.10), we see that impedance of parallel LC circuit reaches infinity at resonance frequency.

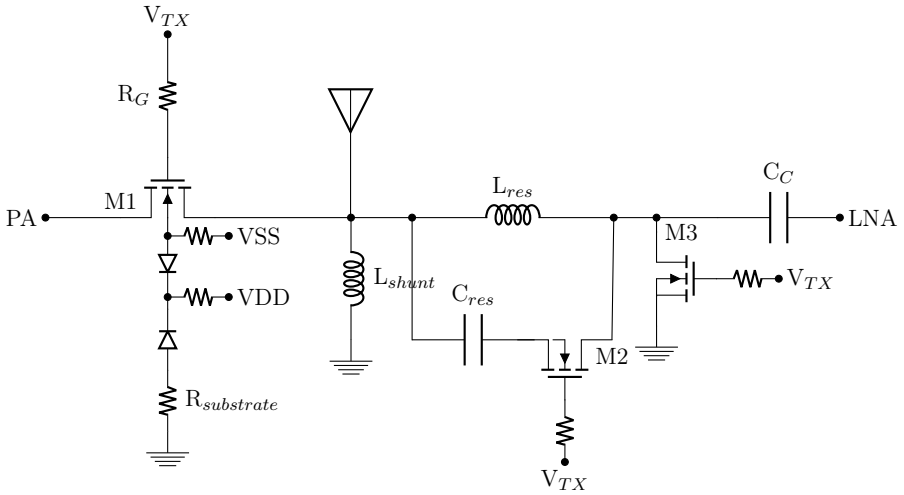


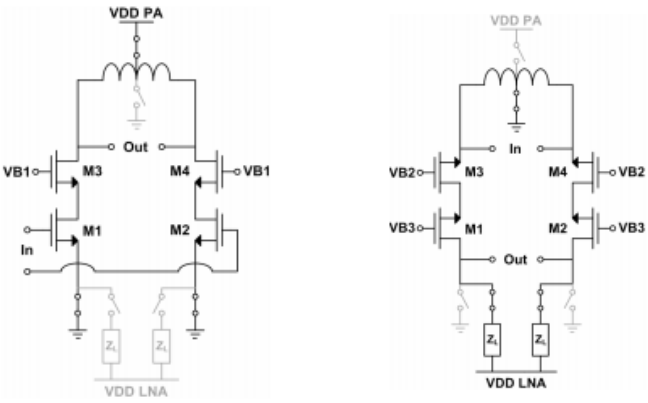
Figure 3.13: Resonance switch schematic

In TX Mode, M_1 and M_2 are turned on, connecting the PA to the antenna and forming a LC tank, respectively. This creates a high impedance in

RX path and signal from the PA is transmitted to the antenna port. Transistor M_3 is on, providing even better isolation by connecting the leaked signals to ground. During RX Mode, M_1, M_2 and M_3 are off. The capacitor C_{res} is now disconnected while the inductor L_{res} forms the matching network for the LNA along with capacitor C_C. An on-chip shunt inductor can be added at the output to provide ESD protection. The main benefit of resonance topology is that no extra loss are introduced in the signal path between antenna and LNA which is important to be able to achieve a good NF. There is no requirement for negative voltage generation for body bias. One downside to this solution is that it can only resonate for a narrow frequency range. The NB-IoT switch must be able to handle a large spectrum. Nonetheless, this switch topology can used as a multiport solution with very competitive insertion loss.

3.5 Reusable LNA-PA topology

In [12], authors have designed a wideband integrated T/R switching technique that doesn't require any conventional switch. The paper describes a reconfigurable PA that performs both as PA and LNA. A typical inverse class D configuration is used where it is possible to switch the supply and ground voltages. The PA topology of an input pair and a cascode pair is identical to a cascode common-gate LNA. The circuit is shown in Fig. 3.14.



(a) PA configuration **(b)** LNA configuration

Figure 3.14: Reusable PA [12]

When configured as PA, Fig. 3.14a, transistors M_1 and M_2 are the switched input and M_3 and M_4 are cascodes to support output power. By changing the polarity of supply and ground, the circuit now performs as a

LNA, shown in Fig. 3.14b. Transistors $M_{3,4}$ are now input devices and $M_{1,2}$ are output cascodes connected to load, Z_L and supply.

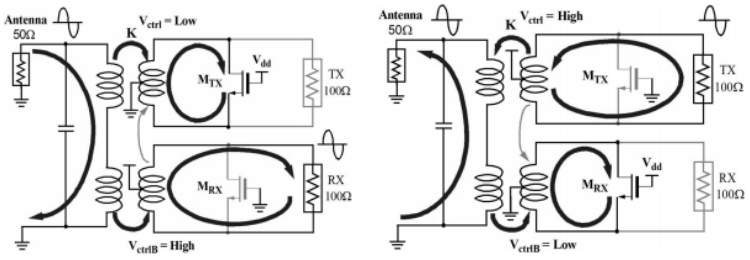
This topology is a candidate as an alternative to a more conventional switch. The aim during this thesis have been focused around more conventional switch topologies since the PA and LNA designs already exist and no further investigation was made into the reusable PA topology.

3.6 Transformer-based topology

The authors of [13] have presented a transformer-based switch, shown in Fig 3.15, which performs impedance matching and transforms single-ended to differential (and viceversa). The conventional switch topology is replaced with a three coupled coil with two center tap shunt switches. The matching is easily done by shunt capacitors at each of the three ports.

The RF signal is transmitted either from the PA to antenna or from antenna to LNA by magnetic coupling provided by the three coupled coil.

When in RX-mode, shown in Fig. 3.15a, M_{TX} is on, shorting the differential output from the turned off PA. This increases the isolation significantly compared to not using a shunt transistor. M_{RX} is off and the signal is received by the LNA. When transmitting the M_{TX} is off and M_{RX} is on, isolating the LNA.



(a) RX mode **(b)** TX mode

Figure 3.15: Transformer topology [13]

The proposed design provides a wideband switch solution for higher frequency bands than the aim of this thesis work and an IL of -2.65 dB at 6 GHz. This solution unfortunately doesn't fit for the intended purpose of an IoT-switch.

3.7 Reusable matching network topology

This topology uses reconfigurable matching network as a switch. It provides good performance but are more suitable for low power applications. In most cases, a shunt switch to protect the low-voltage LNA transistors.

In [14], the authors propose a +8 dBm reconfigurable matching network switch used in Bluetooth applications. The Fig. 3.16 illustrates the switch.

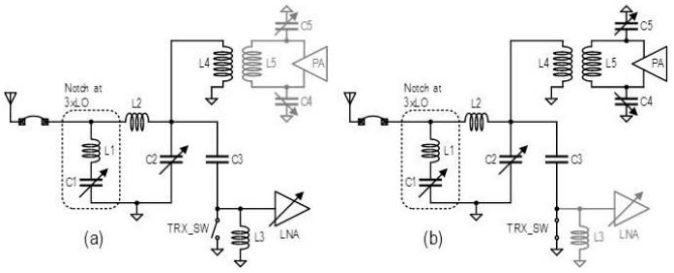


Figure 3.16: +8dBm BLE Matching network switch [14]

The inductor L_1 and C_1 forms a notch filter at three times the Local Oscillator (LO) frequency to remove the third harmonic, while L_2 and C_2 forms a Low Pass Filter (LPF), removing out of band blockers. During TX mode, TRX_SW switch is closed. Capacitor C_2 along with the balun becomes part of the matching network of the PA, while the switch TRX_SW provides low-impedance to ground, protecting the LNA transistors. This kind of shunt switches can provide about 5 dB of extra isolation. In RX mode, TRX_SW is kept open with the PA off providing a high impedance. L_4 from the balun acts as a shunt inductor forming a tunable band-pass filtering effect together with the capacitor C_2 with a center frequency around 2.4 GHz.

In [15], engineers at Renesas Electronics-Japan have proposed a reconfigurable matching network that also provides filtering, shown in Fig. 3.17. In RX mode, the PA matching network acts as a notch filter while the parallel switch with inductor L_S is kept open. In TX mode, the combination of L_1, C_1, C_2 and C_{gs} from the LNA acts as a pi LPF. The switch in parallel to L_S is closed and shorts the inductor. Since this switch is designed for Bluetooth Low Energy (BLE), the low output power of PA doesn't cause reliability issues for LNA transistors.

In [16], authors have proposed a promising 17.5 dBm switch using matching network reuse, shown in Fig. 3.18. By using a capacitive divider C_1 and C_2, a voltage attenuation of factor C_1/C_2 is achieved.

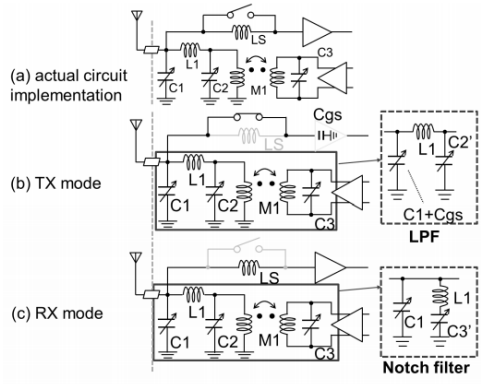


Figure 3.17: BLE matching network switch [15]

During TX mode, the switches S_1 and S_2 are closed. C_1 along with the balun provides matching network for the PA. According to the authors, S_1 attenuates the signal by 20 dB while S_2 adds an extra 5 dB of attenuation. The presence of matching network between C_1 should degrade the attenuation provided by C_1 and C_2.

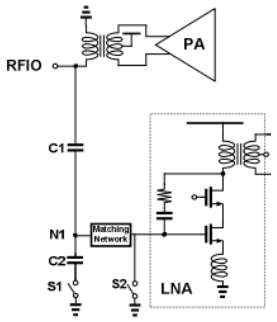


Figure 3.18: WLAN switch [16]

In RX mode, the switches S_1 and S_2 are open. C_1 along with shunted inductor from PA balun becomes a part of the matching network.

In [16], to achieve wide-band operation, the switch and receiver are designed for operation at the 5 GHz band and they have used a LNA with shunt-shunt feedback and inductive degeneration.

3.8 Summary

A summery of studied papers are presented in table 3.1.

Ref	Technology	topology	Freq (GHz)	$IL_{Tx/Rx}$ (dB)	$Iso_{Tx/Rx}$ (dB)	P_{1dB} (dBm)
[6]	130 nm CMOS	Series/Shunt	2.4 - 20	0.9 - 2	34 - 21	30
[7]	90 nm CMOS	Resonance	2.4	0.4/0.1	30	30
[8]	260 nm CMOS	Series/Shunt	0.9	0.5/1.0	37/29	31.3
[9]	500 nm CMOS	Series/Shunt	0.928	0.73	41.8	17.1
[10]	180 nm CMOS	Series/Shunt	1.8	0.75/1.1	20/35	33*
[11]	180 nm CMOS	Impedance trans.	1.9	1.5/1.2	-	33.7
[12]	65 nm CMOS	Reusable PA	3.4 - 5.4	-	-	20**
[13]	90 nm CMOS	Transformer	5 - 7	2.65 / 2.52	50	34
[14]	55 nm CMOS	Matching network	2.4	-	-	8**
[15]	40 nm CMOS	Matching network	2.4	-	-	1.2**
[16]	28 nm CMOS	Matching network	2.4	-	-	8**
[17]	SOI CMOS	Series/Shunt	2.4	1	40	-
[18]	SOI CMOS	Series/Shunt	1 - 2	0.75/-	32/-	+35**

Table 3.1: Summery of papers

* $P_{0.1dB}$ (dBm)
** Tx power (dBm)

The drawbacks and benefits for the most common used topologies are presented in table 3.2.

Topology	Insertion loss	Isolation	Power handling	Bandwidth	Complexity
Series/shunt	Fair	Good	High	Wide	High
Resonance	Low	Good	High	Narrow	Low
Matching	Low	Bad	Low	Narrow	Low

Table 3.2: Summery of topologies

Chapter 4
Filters

An investigation of how to perform harmonic rejection was made during the thesis work.

4.1 Impedance matching harmonic rejection filter

In [19], authors have proposed a low-pass image rejection matching network.

The filter is based on transforming a low-pass LC-matching network to a band-reject filter where series inductor is replaced by a parallel LC network that have same effective impedance at ω_0 and acts as a notch at a multiple of ω_0. In same way, the shunt capacitance is replaced with series LC network that have same effective impedance at ω_0 and acts as a band-stop filter at a multiple of ω_0.

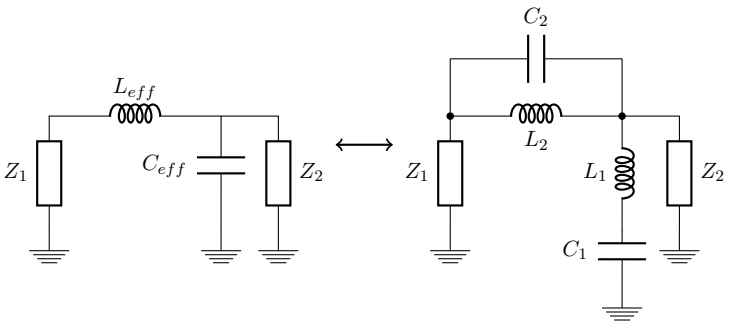


Figure 4.1: Low-pass harmonic rejection matching filter

L_{eff} and C_{eff} transforms the load Z_1 to Z_2. The impedance $Z_{C,eff}$ is calculated using (4.1). L_1 and C_1 is set to create the same impedance as C_{eff} by (4.2).

$$Z_{C,eff} = \frac{1}{j\omega_0 C_{eff}} = \frac{1}{j\omega_0 C_1} + j\omega_0 L_1 \tag{4.1}$$

$$C_{eff} = \frac{C_1}{1 - \omega_0^2 L_1 C1} \tag{4.2}$$

In the same way, the impedance $Z_{L,eff}$ is calculated using (4.3). L_2 and C_2 is set to create the same impedance as L_{eff} by (4.4).

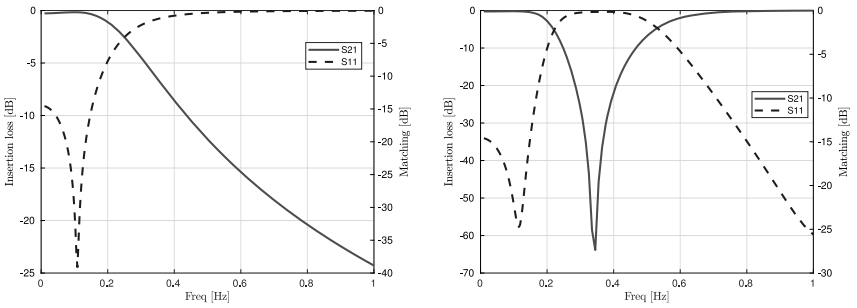
$$Z_{L,eff} = j\omega_0 L_{eff} = \frac{\frac{1}{j\omega_0 C_2} j\omega_0 L_2}{\frac{1}{j\omega_0 C_2} + j\omega_0 L_2} \tag{4.3}$$

$$L_{eff} = \frac{L_2}{1 - \omega_0^2 L_2 C_2} \tag{4.4}$$

The series notch filter and shunt band-stop filter is resonant for a n multiple of ω_0 and the component values have to correspond according to (4.5).

$$(n\omega_0)^2 = (L_1 C_1)^{-1} = (L_2 C_2)^{-1} \tag{4.5}$$

Figures 4.2a and 4.2b shows the response of the LC-matching in Fig 4.1 with and without the band-reject filter, respectively. The matching network transforms a source impedance of 35Ω to a load of 50Ω.



(a) Matching network **(b)** Matching filter with band-reject

Figure 4.2: Band-reject matching network

4.2 High power tunable notch filter

During the thesis work it was discovered that a tunable filter might be needed to reduce harmonics generated by the PA in order to fulfill the 3GPP specifications [27] for out-of-band harmonic transmissions. A differential filter that can be tuned to attenuate a specific harmonic was investigated.

A first order notch filter gives a better attenuation, a faster roll off, than a first order low-pass filter. The disadvantage is that the bandwidth

of a notch filter is narrow compared to the low-pass filter. This can be seen by comparing Fig. 4.3b and Fig. 4.4b. By using a first order filter, the component count and RF signal attenuation due to parasitic effects are kept to a minimum.

The n:th harmonic is attenuated by designing a first order butterworth low-pass filter, then transform it into a notch using the methods described in [4], tuned to attenuate a signal with a frequency of n times the fundamental frequency:

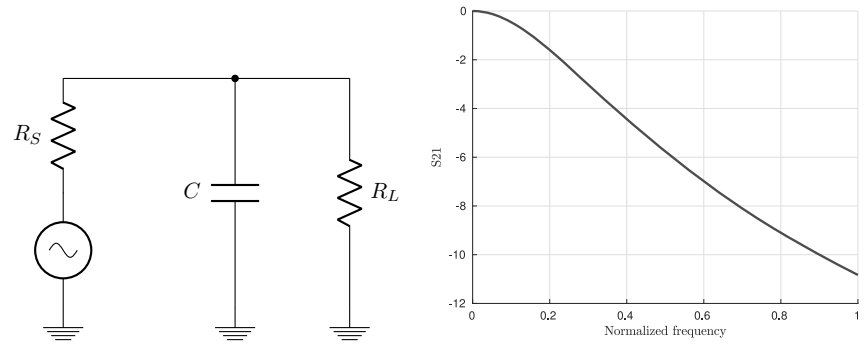
$$\omega_n = n2\pi f_c \tag{4.6}$$

The single-ended notch filter is then converted in to a differential filter by mirroring the components as shown in Fig. 4.5a.

The first order low-pass filter shown in Fig. 4.3a has a response of:

$$H(\omega) = \frac{1}{j\omega R_s C + 1} = \frac{1}{j\frac{\omega}{\omega_0} + 1} \tag{4.7}$$

where $\omega_0 = 1/(R_s C)$. The response is shown in Fig. 4.3b.



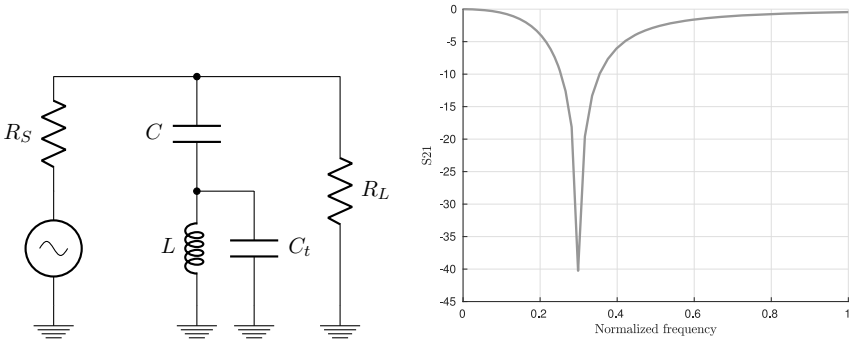
(a) Singel ended first order **(b)** Filter response

Figure 4.3: Lowpass filter

The first order notch filter shown in Fig. 4.4a has a response of:

$$H(\omega) = \frac{1 - \omega^2 L(C + C_t)}{j\omega C(1 - \omega^2 L C_t)} = \frac{1 - \frac{\omega^2}{\omega_0^2}}{j\omega C(1 - \omega^2 L C_t)} \tag{4.8}$$

where $\omega_0 = 1/\sqrt{L(C + C_t)}$ and $L = 1/(\omega_n^2 C)$. The response is shown in Fig. 4.4b. As shown in the graph, when $\omega \to \omega_0$, $H(\omega) \to 0$. The capacitor C_t is added and by changing the capacitance it is possible to tune the filter.



(a) Single ended first order **(b)** Filter response

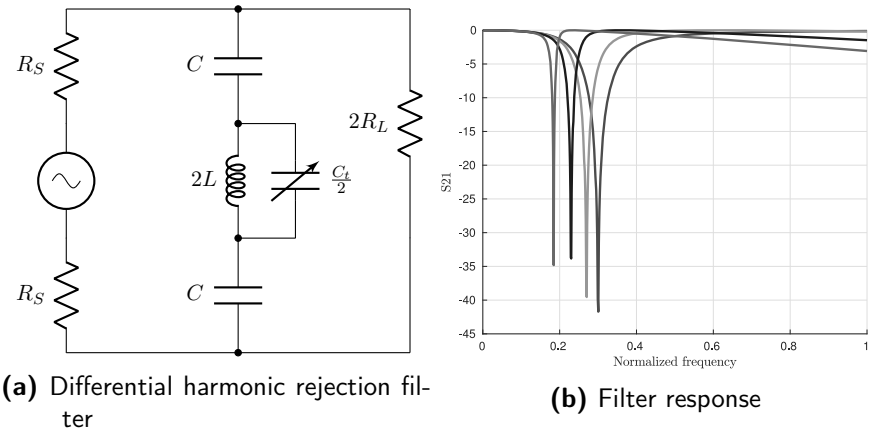
Figure 4.4: Notch filter

By transforming the single ended notch filter into a differential filter and adding a network of parallel capacitors that can be switched in and out, changing the total capacitance C_t, it is possible to tune the filter to attenuate a desired harmonic. A circuitry monitoring the the transmitted signal harmonics can then tune the filter and remove the unwanted frequency content.

The first order differential notch filter shown in Fig. 4.5a has a response of:

$$H(\omega) = \frac{1 - \omega^2 L(2C + C_t)}{j\omega C(1 - \omega^2 LC_t)} = \frac{1 - \frac{\omega^2}{\omega_0^2}}{j\omega C(1 - \omega^2 LC_t)} \tag{4.9}$$

where $\omega_0 = 1/\sqrt{L(C + C_t)}$. The response is shown in Fig. 4.5b. As shown in the graph, when $\omega \to \omega_0$, $H(\omega) \to 0$.



(a) Differential harmonic rejection filter **(b)** Filter response

Figure 4.5: Differential notch filter

The filter allows for low in band attenuation and high out of band harmonic rejection. The impedance, X_C, from the capacitors C is high resulting in only a small voltage over the inductor and the variable capacitance network making it possible to relieve the demand of power handling of the switches used to realize C_t. By using this setup it is possible to implement a tunable filter, removing unwanted harmonics.

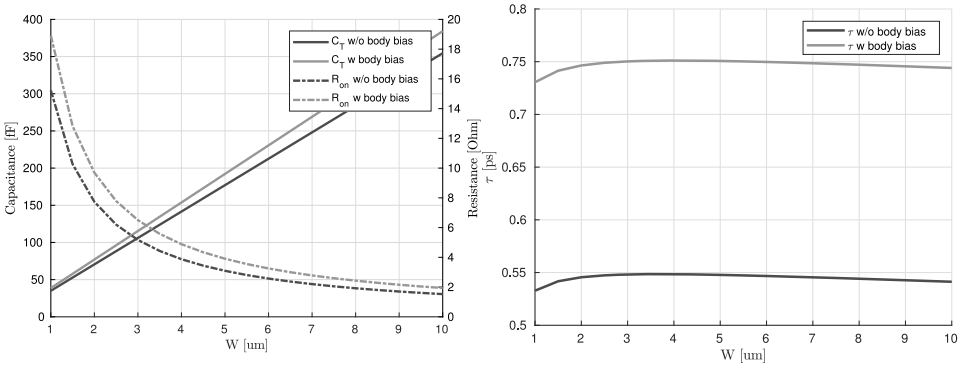
Chapter 5

Results and conclusions

5.1 Sizing

To find the best performance in terms of R_{on} and C_{off} with respect to finger width, a simple simulation were made. To find the C_{off}, all DNW transistor terminals were connected to ground and parasitic capacitance was extracted. The total capacitace were calculate using methods described in section 2.2.1. The on-recistance, R_{on}, was extracted in linear operation mode.

Fig. 5.1b shows the time constant, $\tau = R_{on} \cdot C_{off}$, with and without negative bias applied to the body. As seen, finger width doesn't have a big impact on time constant. Since substrate leakage is a more significant factor in bulk CMOS than the time constant, conclusions from this simulations doesn't hold when choosing the size of transistors.



(a) Total off-capacitance and on-resistance

(b) Time constant $R_{on} \cdot C_{off}$

Figure 5.1: Time constant

5.2 Negative bias topology

In section 3.2.3, benefits of using negative bias is discussed. In this section, performance from our simulations are presented. Each simulation setup is evaluated by the insertion loss, linearity and isolation performance. Performance of the series and the shunt switch is simulated and evaluated independently. The results will be used to later determine the final setup for the complete switch. All simulations were done using periodic steady state analysis with periodic S-parameters and an operation impedance of 50 Ω.

5.2.1 Insertion loss

This test setup, shown in Fig. 5.2, measures the insertion loss. The switch consist of triple-well devices where the body is floated with a negative voltage of −1.5 V, the DNW is connected to VDD (1.8 V) and the substrate is connected to ground using large resistor. As described in section 2.2.5, using DNW-ring can isolate the substrate near the transistors from the rest of the substrate. The gate of the transistors are also floated to bootstrap the voltage swing.

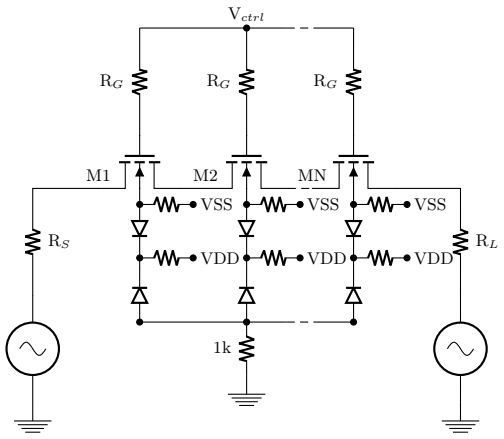


Figure 5.2: Series switch test setup

The losses at an input power of 23 dBm are shown in Fig. 5.3 where S21 is the insertion loss and S11 is the matching. It is clear from the graph that insertion loss decrease with the number of stacked transistors due higher on-resistance and substrate losses. Also, S11 is better than 20 dB implying that the losses due to mismatch are negligible.

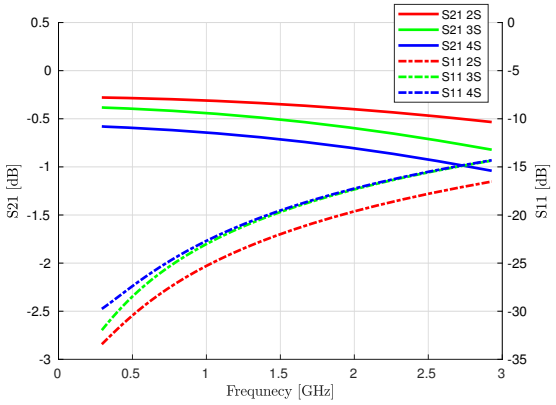


Figure 5.3: Insertion loss and matching for a series switch

Fig. 5.4 shows the shunt switch testbench used to evaluate the impact on the RF-signal by an interfacing off-switch. The insertion loss is shown in Fig. 5.5. The four stack switch has least impact while two stack has the most due to transistors turning on. Due to better voltage division in a off-state using a four stack shunt switch, the transistors doesn't turn on when a high power signal is applied to the drain. Too many stacked transistors in a shunt switch can increase insertion loss at high frequencies due to the parasitic capacitance to ground.

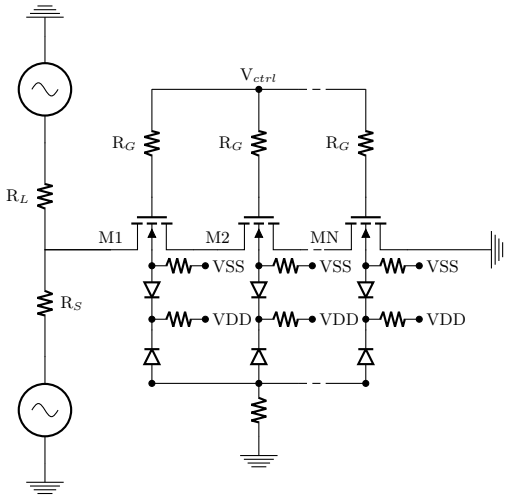


Figure 5.4: Shunt switch test setup

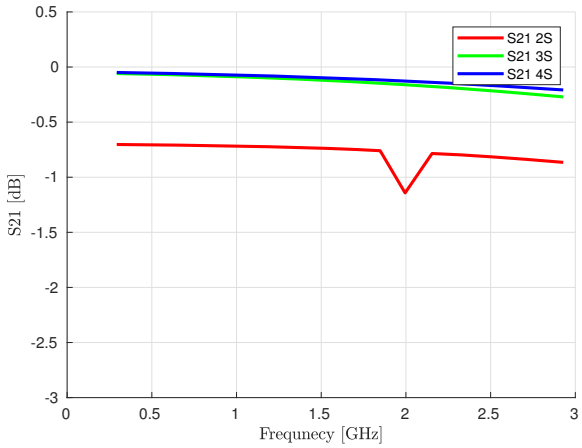


Figure 5.5: Shunt off-switch insertion loss

5.2.2 Linearity

The generated harmonics for the series switch is shown in Fig. 5.6. The best performance is achieved when a stacking of three transistors are used. The harmonics is lower than the requirement from 3GPP [27]. Since the harmonics for all versions of stacking are low, series switch harmonics are not considered when deciding the best series switch alternative.

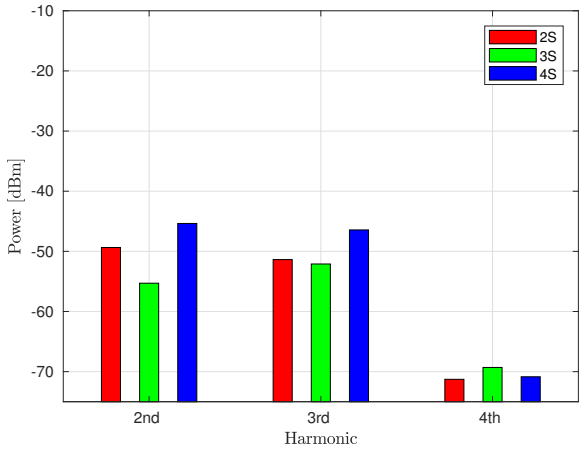


Figure 5.6: Harmonics generated by a series switch in on-state

Harmonics generated by a shunt off-switch have a large impact and must be taken in to account, as shown in Fig. 5.7. The two stack shunt switch causes high harmonics as it can't handle the high power during off-state (turning on), just as shown in Fig. 5.5.

The four stack shunt switch has the least impact on interfacing RF-

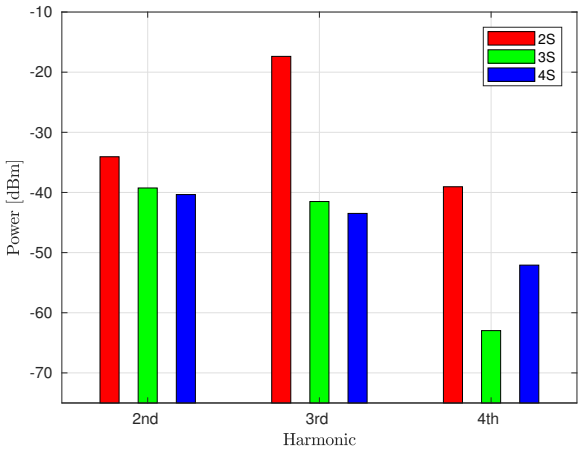
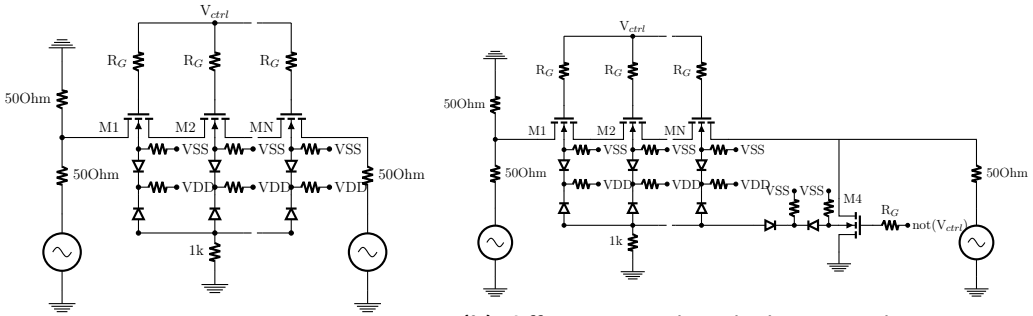


Figure 5.7: Harmonics generated by a shunt switch in off-state

signals regarding insertion loss and harmonic generation.

5.2.3 Isolation

Fig. 5.8 shows the testbench used when measuring isolation of a off-series switch with and without a shunt switch. To make the simulation more realistic, a 50Ω resistor were connected to the source representing the load. If no load is connected, the VSWR will be high due to mismatch caused by high impedance of the off-series switch.



(a) Off series switch

(b) Off series switch with shunt switch

Figure 5.8: Isolation test setup

Isolation with different number of stacking is shown in Fig. 5.9. The simulation shows that an increase of stacking by one transistor improves the isolation by 5 dB. The figure also shows that isolation improves by almost 20dB with a shunt switch.

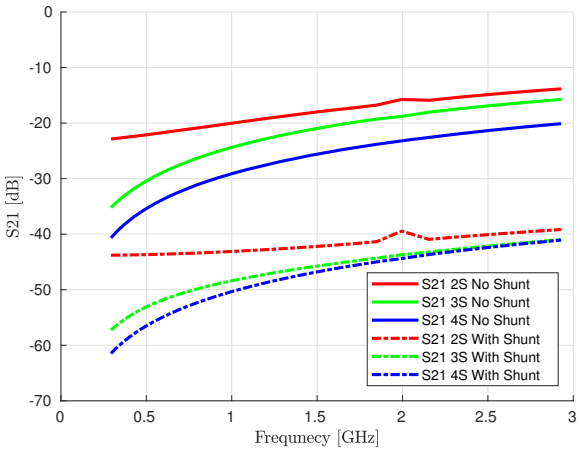


Figure 5.9: Series switch isolation

The four stack series switch provides sufficient isolation as stated in table 1.1 and a shunt switch can be avoided, while the two stack and three stack switch need shunt switches.

5.2.4 Final setup performance

Fig. 5.11 shows the schematic of the complete negative bias switch setup. It is a Single Pole Four Throw (SP4T) switch which supports dual band operation. In this setup, each transistor body is connected to -1.5 V, improving the power handling capability of switch as discussed earlier. The substrate is isolated using a DNW-ring and connected to ground through a large resistor. This provides isolation from the rest of the circuit and helps reducing insertion loss and improve linearity. To improve linearity, the stacking is increased. This is done without increasing insertion loss due to low R_{ON}.

The design is asymmetric to improve the performance. Since there is no high power seen by the off-state RX shunt arms during receive mode, a single transistor is used. Due to presence of two power amplifiers, one highband and one lowband, all series switches are identical. In the case where there is only one power amplifier, the series switch at TX side can be made up of a single transistor as the RX power is low. In the four stack switch simulations, no shunt switches is used as the series switch provide enough isolation.

In Band1 TX mode, the V_{tx1} is high which turns the series switch of PA1 on and the shunt switch off, while V_{tx2}, V_{rx1}, V_{rx2} are low which keeps the rest of the series switch off and the shunt-switches on. Thus the power from PA1 is transmitted to the antenna as it sees high impedance for the rest

of the paths. In RX mode for Band1, V_{rx1} is high and rest of the control voltages are low causing a low-impedance path from antenna to LNA_1. The negative voltage generation is not necessary when receiving since the voltages are low.

Transistors width and length were chosen to get the best performance for second and third harmonic without compromising the insertion loss. To improve the linearity of the switch, feed-forward capacitors have been employed between source and the gate of the first and last series switch transistors and the shunt arms first transistor. It was found that the performance of a three stacked switch with a small feed-forward capacitor used on the second transistor can improve linearity even more for high voltages due to mismatches (not shown in Fig. 5.11). A shunt inductor at the output of switch was added which provides ESD protection.

Design and simulations were made for a 14 dBm negative bias switch. Results are presented in appendix C. The transistor width has been reduced to half the size due to the lower power.

Operation impedance

The best insertion loss with respect to operating impedance, 10 Ω to 50 Ω, was investigated. Fig. 5.10 shows that the setup with a two stack series switch has the lowest insertion loss. Unfortunately it can only operate upto 20 Ω, higher impedance causes reliability issues due to higher voltage swings. The three stack switch gives best insertion loss at 25 Ω and the four stack switch at 45 Ω.

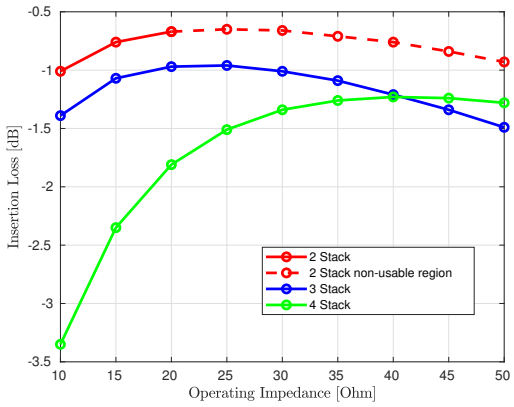


Figure 5.10: Insertion loss with respect to operating impedance

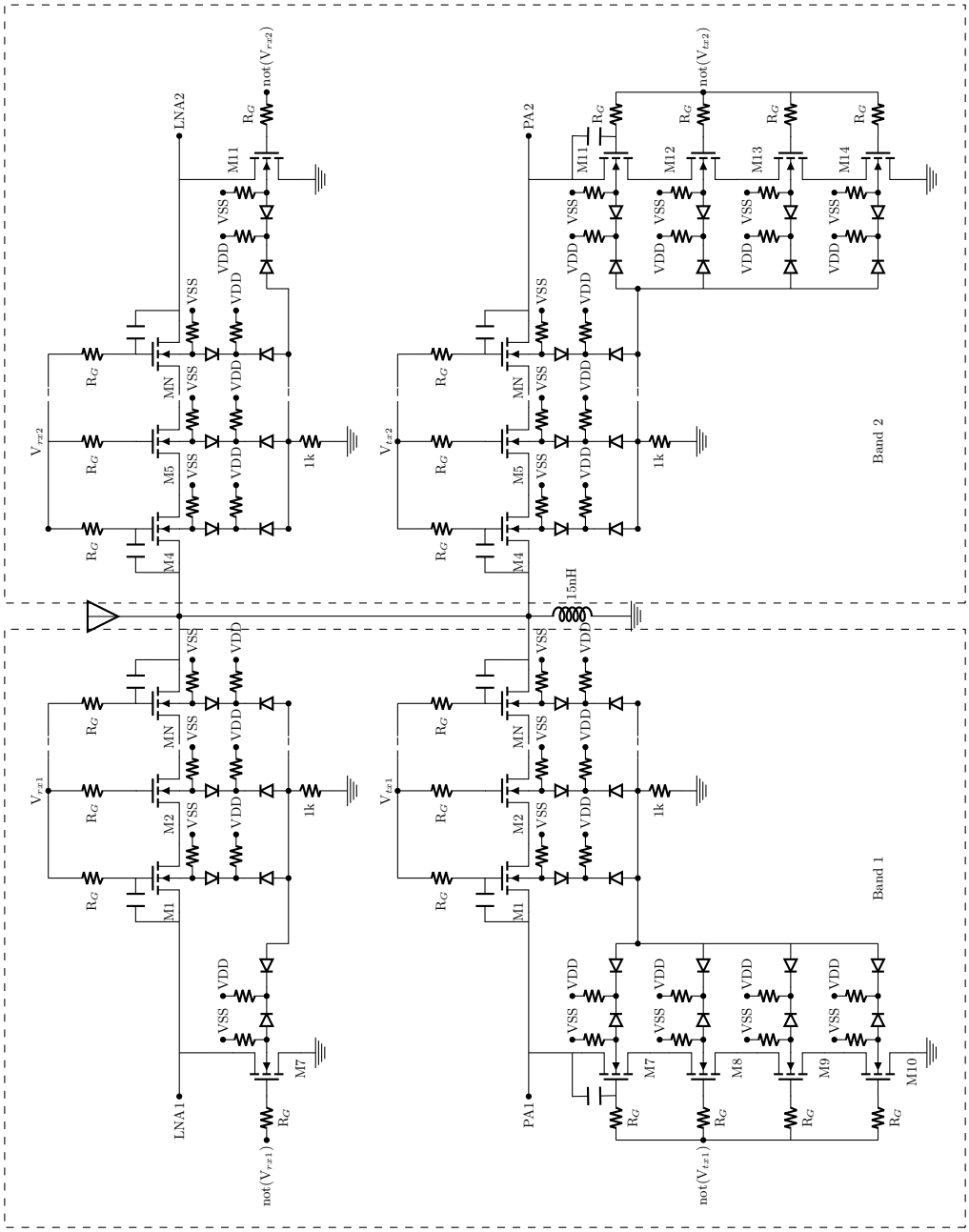
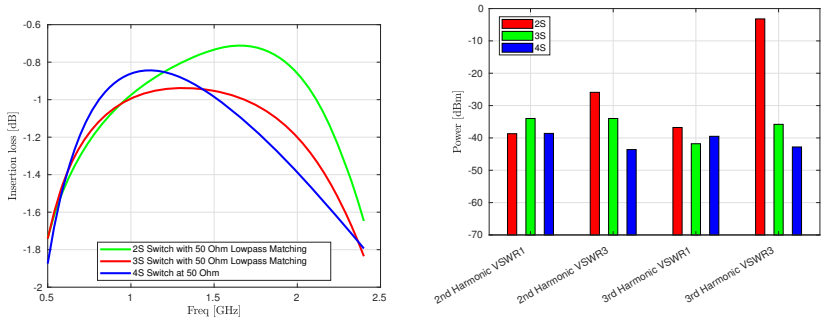


Figure 5.11: Negative bias series switch

Insertion loss, linearity and power handling

Fig. 5.12a shows the insertion loss for the full switch setup matched to a 50 Ω load. The two stack switch operates at 20 Ω and three stack switch operates at 25 Ω, both matched to a 50 Ω load using a two component lowpass matching network. The presented insertion loss include the losses due to the matching network, which is mostly dependent on the Q-value of the inductor, in this case 30. The two stack switch has the best insertion loss over the complete frequency range.



(a) Full system insertion loss

(b) Harmonics with respect to stacking and VSWR

Figure 5.12: Full system insertion loss

The harmonics generated are shown in Fig. 5.12. According to 3GPP requirements [27], the output harmonics should be less than -30 dBm. The two stack switch meets the requirement and provides the best insertion loss at an operating impedance of 20 Ω. In a real scenario, there might be an antenna mismatch causing high VSWR. Taking this into account, two stacked switch cannot be used as a 20 dBm switch because of reliability issues. The three and four stacked switches both make a strong case as a final design since they are more robust. We have chosen the three stacked switch operating at 25 Ω used with low-pass filtering and matching network as the final switch design.

Fig. 5.13 shows the complete transfer function of three stacked switch. The switch offers low attenuation in-band and good matching. It also provides $20 - 30$ dB of attenuation of high band harmonics, sufficient to meet the 3GPP requirement [27]. The low band still needs filtering before the switch (or integrated in the PA balun) as the harmonics fall within the bandwidth of the switch.

Table 5.1 shows the $P_{0.1dB}$ compression point, IP_2 and IP_3 of the negative bias switch. The three and four stack switches have a higher compression point than the requirement. The $P_{0.1dB}$ does not completely represent

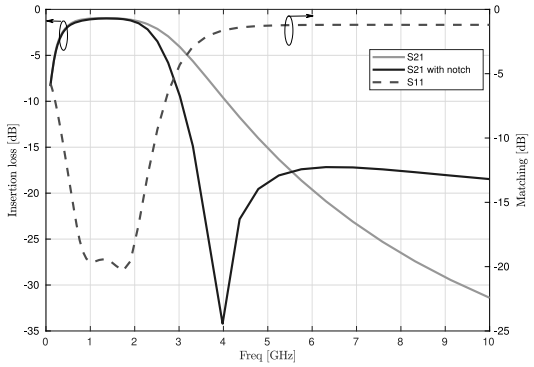


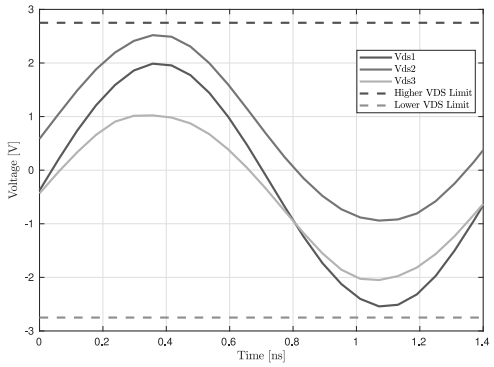
Figure 5.13: Transfer function for the full setup

the power handling capability. To find the correct power handling it is necessary to check the critical voltages (diode voltage, drain-source voltage) of the transistors in the switch. The switch meets the OIP2 and OIP3 requirements and are presented in table 5.1.

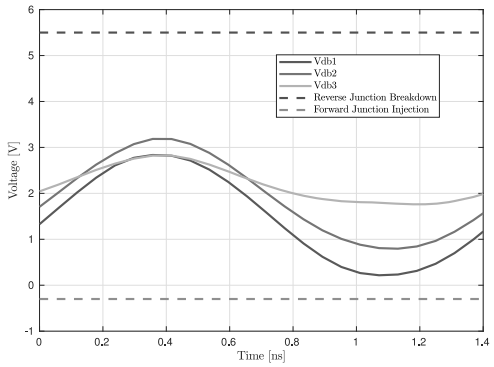
Stacking	$P_{0.1dB}$	IP_2	IP_3
2S	21.32 dBm	80.94 dBm	39.0 dBm
3S	25.42 dBm	77.50 dBm	42.1 dBm
4S	25.80 dBm	81.45 dBm	44.6 dBm

Table 5.1: Linearity of negative bias switch

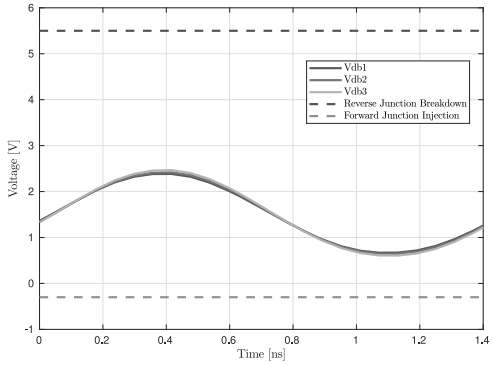
Fig. 5.14 shows the drain-body diode voltage and drain-source voltage of the series off-transistor and on-transistor in three stack negative bias switch at a VSWR of 10. The voltages are within the limits for reliable operation at an input power of 23 dBm. Only the critical voltages have been shown here. Gate-source, drain-gate voltages are always within the limit because of bootstrapping.



(a) Off switch drain-source voltage



(b) Off switch diode voltage



(c) On switch diode voltage

Figure 5.14: Series switch voltages at VSWR of 10

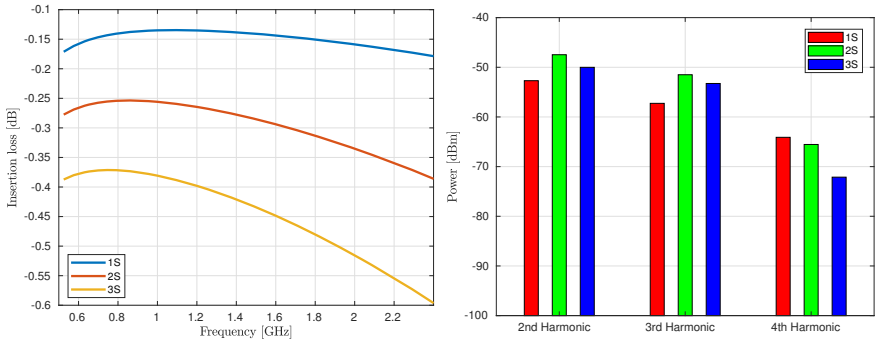
5.3 DC-block topology

The second topology investigated was the DC-block switch with biased drain/source. This topology is popular in GaAs switches where parasitics doesn't have the same impact as in bulk-CMOS. The main benefit of this topology is that it doesn't require any negative bias. There are problems using large DC-block capacitors in bulk-CMOS as explained in section 3.3. The same stacking evaluation method used for negative bias series and shunt switches done again for the DC-block switch. The DC-switch performance is characterized by insertion loss, linearity and isolation. The switches was build using a triple well devices. The DNW is floated to 1.8 V while the body and substrate are floated by large resistors to ground. All tests were performed with 23 dBm input power.

5.3.1 Insertion loss and Linearity

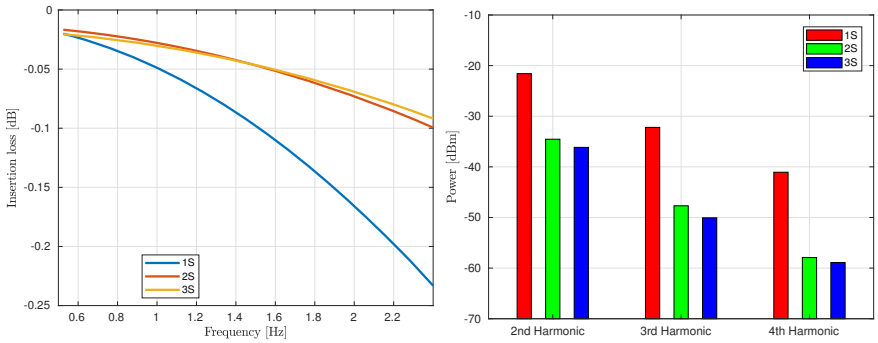
Fig. 5.15a shows the insertion loss for a series switch. As the stacking is increased, the losses increase by about 0.15 dB. The generated harmonics by a series switch are lower than the requirements. The four stack series switch generates lower harmonics compared to three stack, shown in Fig. 5.15.

Fig. 5.16a shows insertion loss and Fig. 5.16b shows the harmonics impact of a shunt off-switch. The three stack shunt switch causes the least insertion loss and harmonics generation. Simulations show that a single shunt transistor with DC-block can't handle the 23 dBm input power when it is off.



(a) Insertion Loss **(b)** Harmonics

Figure 5.15: Insertion loss and harmonics generated by a series switch in on-state



(a) Insertion loss **(b)** Harmonics

Figure 5.16: Insertion loss and harmonics generated by a shunt switch in off-state

5.3.2 Isolation

Fig. 5.17 shows the isolation by an off-state series DC-block switch, the shunt switch improves isolation by about 15 dB as expected.

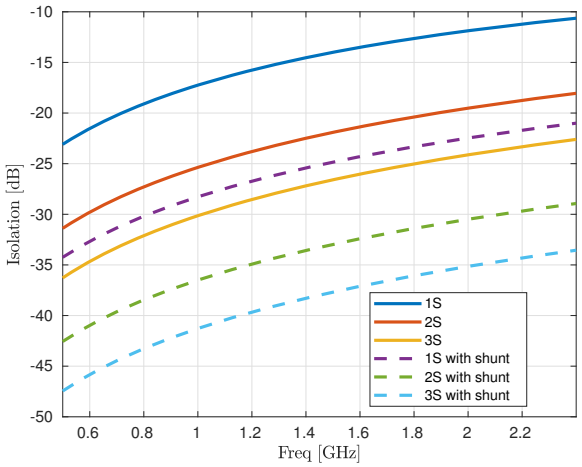


Figure 5.17: Isolation of with with respect to stacking

5.3.3 Final setup performance

Fig. 3.10 shows the schematics for the asymmetric DC-switch with drain/source bias and DC-block capacitors. The performance simulations was made using a single transistor at TX side and two or three stacked transistors at RX side. A standard transistor is used as shunt switch to provide extra isolation at RX side. Since the received signal power is low, no shunt switch is used at TX side. During off state, the use of drain/source bias helps keeping the drain/source-body diodes reverse biased. The drain-body junction diode at RX side is kept reverse biased in by connecting a capacitor from drain to body when transmitting.

The transistors sizes are smaller in this configuration than the negative bias configuration. The sizing was chosen to get the best performance regarding second and third harmonic without compromising the insertion loss. A shunt inductor is used to resonate the parasitics from the DC-block capacitors and provides ESD protection. This reduces the bandwidth of the switch and a multiport solution must be used. In upcoming sections the results for the switch resonated for high-band is shown.

Operating impedance

In Fig. 5.18 it is shown that two stack and three stack switches give best insertion loss when operated at 40 Ω. We propose that the switch should use an operating impedance of 35 Ω to improve reliability and the capability to handle miss-matches. The ESD inductor can be used to tune the switch to the antenna impedance.

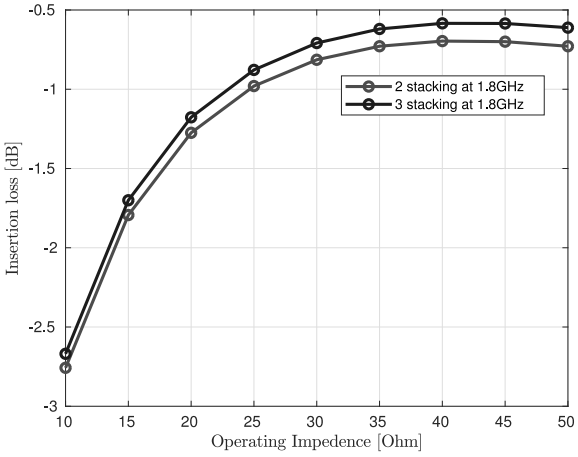


Figure 5.18: TX insertion loss with respect to operating impedance

Fig. 5.19 shows insertion loss for transmit and receive mode when a two

stack and three stack asymmetric switch is used. The TX loss for two stack switch is higher than that of three stack switch due to poor isolation. On contrary, the RX loss in two stack switch is lower compared to three stack. This is as expected as we are passing the signal through more switches in three stack switch.

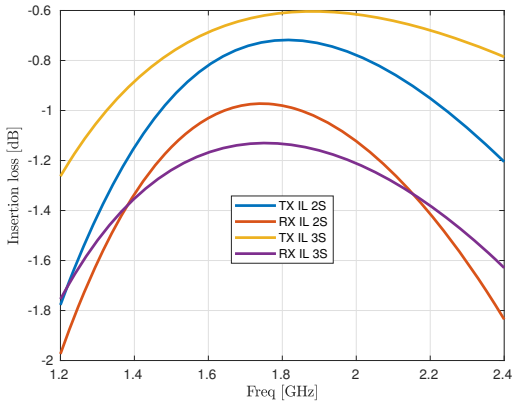


Figure 5.19: Insertion Loss

It can be beneficial to accept higher loss in the TX path and reduce loss in RX path as the RX insertion loss directly affects the NF of receiver. The loss in TX can be recovered by increasing the output power in the PA. The full switch simulation for the DC-block topology have been performed at 35 Ω operating impedance and 50 Ω antenna load using a matching network with filtering.

Fig. 5.20 shows the insertion loss and matching for a two stack DC-block switch with an off-chip matching network, with and without the impedance matching harmonic rejection filter tuned to filter second order harmonics.

Fig. 5.21 shows the second and third harmonics generated by two stack and three stack DC-block switches. The requirement for both two stack and three stack switch is met according to the 3GPP requirement of a harmonic levels [27].

Fig. 5.21 also shows harmonics at VSWR of 3. Even though the 3GPP certification is set by a VSWR of 1, it is important for a functional product to work up to a VSWR of 3. The harmonics at VSWR of 3 also meet the 3GPP requirements.

Table 5.2 shows the $P_{0.1dB}$ compression point, IP_2 and IP_3 of the DC-block switch. The compression point for three stack switch is about 3 dB higher than two stack switch. Both the switches has a $P_{0.1dB}$ compression point that is higher than the requirement. Again, this numbers doesn't reflect the true power handling capability of the switch, junction voltages

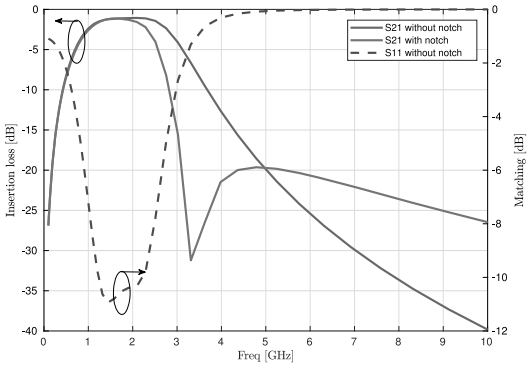


Figure 5.20: Insertion Loss and Matching

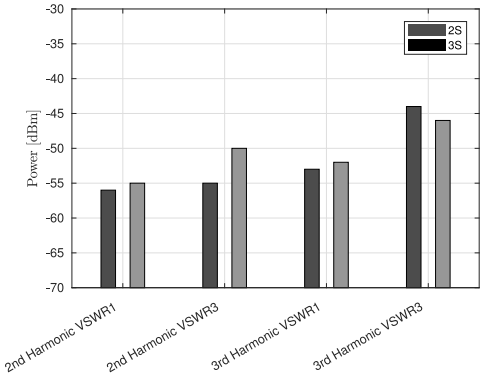


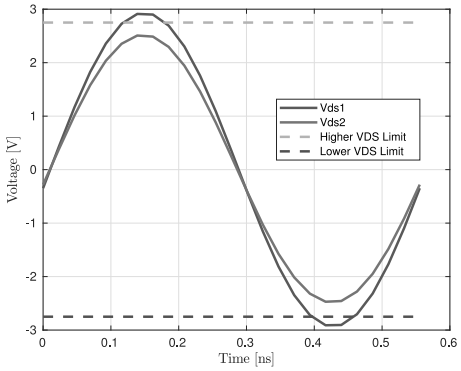
Figure 5.21: Harmonics generated at VSWR of 1 and 3

still needs to be confirmed

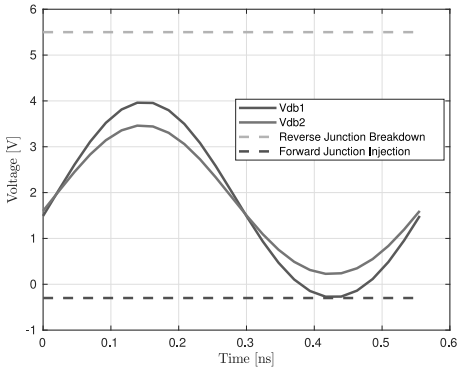
Stacking	$P_{0.1dB}$	IP_2	IP_3
2S	26.69 dBm	78.86 dBm	47 dBm
3S	29.67 dBm	83.66 dBm	48 dBm

Table 5.2: Linearity of DC-block switch

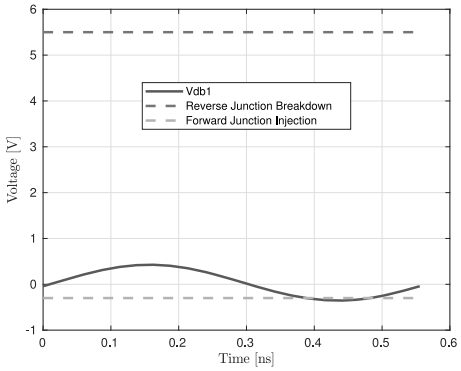
Fig. 5.22 shows the switch voltages at a VSWR of 8. The V_{ds} shown in 5.22a, for the first transistor in RX-side is higher than the prescribed limit. Since high V_{ds} only causes device life degradation, due to hot carrier injection, it is acceptable to violate drain-source voltage for a VSWR higher than 3. The junction voltages shown in Fig. 5.22b does meet the requirements. The diode voltage for the on-switch, shown in Fig. 5.22c, violates the forward junction injection limit by only 25 mV.



(a) Off switch drain-source voltage



(b) Off switch junction diode voltage



(c) On switch junction diode voltage

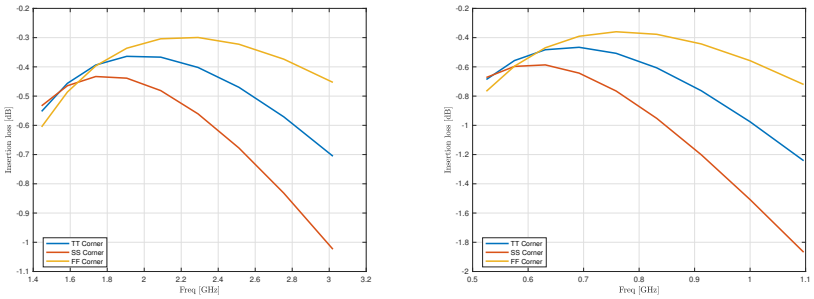
Figure 5.22: Series switch voltages at VSWR 8

5.4 Resonance topology

The last topology investigated was the resonance topology, shown in Fig. 3.13. The LNA matching network is reused to form a high impedance LC tank as explained in section 3.4. Since the LC tank is not wideband enough to cover all frequency bands, one switch for each band will be needed. To model the LNA balun, a 7 nH inductor was used. On the TX side, a single DNW with body and substrate floated to ground and n-well floated to the supply voltage, 1.8 V was used.

5.4.1 Insertion loss

Simulations were made using different corners to get an estimate of how the shift in the resonance frequency affects the performance, shown in Fig. 5.23. In low band the insertion loss is $0.45 - 0.7$ dB and $0.35 - 0.5$ dB in the high band when simulating using the Typical-Typical (TT) corner. The switch still covers the complete band for the worst corners with some increase in the insertion loss.



(a) TX insertion loss, high band **(b)** TX insertion loss, low band

Figure 5.23: Insertion loss

5.4.2 Linearity

Table 5.3 shows $P_{0.01dB}$ compression point, IP_2 and IP_3 for the resonance switch. Since there are no RX off-switches that turns on when high power is applied, the compression point is much higher compared to the other switches. As mentioned before, it is necessary to check all voltages in order to tell the real power capability.

Fig. 5.24 shows the harmonic content generated by the resonance switch. The switch fulfills the 3GPP requirements at a VSWR of 3 [27].

Freq Band	$P_{0.01dB}$	IP_2	IP_3
Lowband	36.02 dBm	98.95 dBm	54 dBm
Highband	25.39 dBm	92 dBm	50.45 dBm

Table 5.3: Linearity of resonance switch

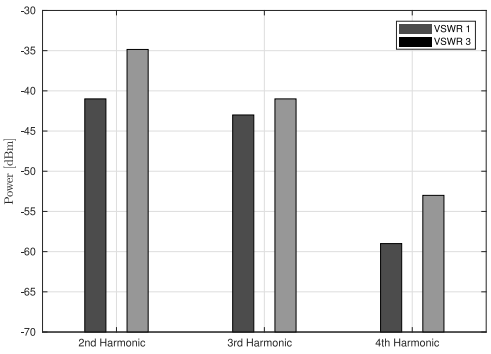
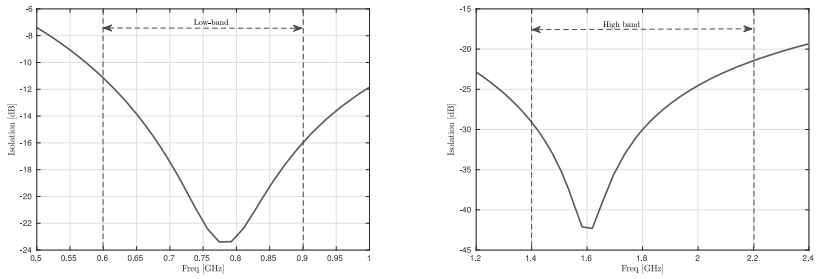


Figure 5.24: Harmonics generated at VSWR of 1 and 3

5.4.3 Isolation

Fig. 5.25 shows the isolation of the resonance switch. The switch isolation is +30 dB in high band and +25 dB in low band. In hindsight, its complementary to the low insertion loss of this switch.



(a) Low band isolation **(b)** High band isolation

Figure 5.25: Resonance switch isolation

5.5 Conclusion

Most of the papers found and studied during this thesis work relate to wireless LAN and low power Bluetooth solutions. Designing switches for such applications doesn't require wideband solutions.

We have evaluated three different switch topologies and found the best configuration for each switch. Since the switches use different architectures, it is not completely fair to compare them based on insertion loss only. We found that our original requirement for the thesis wasn't feasible but parts of the requirement could be meet by each topology.

Negative Bias

The negative bias topology allows for a easy integration single port solution with low insertion loss. With negative bias to body, it is possible to build a SP4T switch. Generating the negative voltage can potentially introduce unwanted noise and harmonics to the RF signal. The linearity compared to the other two tested typologies is degraded.

This switch was combined with matching filter to provide harmonic rejection for highband. Insertion loss was found to be 1-1.4 dB and a 0.1 dB compression point of 25.42 dBm.

DC-block switch

The DC-block topology also allows for a less complex solution since no negative voltage generation is needed. The insertion loss is lower than the negative bias solution. The large capacitors needed to block the DC voltage introduces parasitic capacitance to ground that can be reduced with a resonating inductor. This makes the switch narrowband and a multiport solution is required to cover all frequency bands. Insertion loss was found to be 0.7 - 1.4 dB and a 0.1 dB compression point of 26.69 dBm.

Resonance switch

The resonance switch doesn't require any stacked transistors which reduces the insertion loss and improves linearity and power handling. No negative voltage generation is needed. A multiport solution is required since the resonance tank isolating the LNA from the transmitted RF signal only covers one band. Insertion loss was found to be 0.3 - 0.7 dB and a 0.01 dB compression point of 25.39 dBm. Compression doesn't occur at the same power level as the two other topologies since no interfacing transistors turn on during high power transmission.

Switch	TX IL	RX IL	$P_{0.1dB}$	IP_2	IP_3	Max VSWR	3rd Harm. Rej.
Neg. Bias	1.0-1.4 dB	1.0-1.4 dB	25.4 dBm	78.8 dBm	42.1 dBm	10:1	20.0 dB
DC Block	0.7 - 1.1 dB	1.0-1.4 dB	26.7 dBm	77.5 dBm	47.0 dBm	8:1	20.0 dB
Resonance	0.3-0.7 dB	-	25.4 dBm ($P_{0.01dB}$)	92.0 dBm	50.5 dBm	10:1	-

Table 5.4: Summary

Chapter 6
Future work

This chapter outlines some ideas for future work.

Device modeling

For high power application, the models provided are not accurate enough. To gain more confidence in the during design and reduce re-runs, a sample transistors could be measured to verify the I-V characteristics. A 3-dimensional electron microscopy model of the substrate can be used to get more confidence when simulating substrate resistance and switch linearity.

It is well known that at V_{DS}=0, MOSFET models have discontinuity in 2nd derivative of the drain current. Thus, the third order non-linearity measured with BSIM4 model is incorrect. Surface potential model could be used to correctly quantify the non-linearities but was not available for the design kit. Authors in [25] have provided an alternative solution that could be used with BSIM4 model to fix the discontinuity issue. In future, this workaround could be implemented to get the correct non-linearity of switch.

Layout simulations

By making a full layout of the switch it would be possible to extract parasitics and evaluate each topology more thoroughly. The high power used by NB-IoT requires careful design consideration since each parasitic contribution degrades the performance.

The parasitic effects that are introduced by capacitors can be reduced by providing a ground shield between the substrate and the capacitor. By resonating this shield with the use of an inductor, it is possible to reduce the parasitic effects significantly.

Full system implementation

The switch is a critical component in a RF-system since all later parts in the transmitter chain is affected by the switch performance. With the PA and LNA designs available it is possible to design a switch well suited for the specific application.

SOI implementation

As we saw during our investigation, harmonic content of bulk-CMOS is high. In [22], authors have proposed a RF SoI switch with insertion loss of 0.25-0.3 dB and harmonic content of -85 dBc at 35 dBm input power. Investigation using SoI could be performed as it is known for high linearity and low insertion loss.

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Appendix A

NB-IoT channels and power classes

Table A.1: NB-IoT channels [27]

Band	Identifier	TX [MHz]	RX [MHz]
1	IMTCore Band	1920 - 1980	2110 - 2170
2	PCS 1900	1850 - 1910	1930 - 1990
3	1800	1710 - 1785	1805 - 1880
5	850	824 - 849	869 - 894
8	900	880 - 915	925 - 960
11	1500 (Japan #3)	1427.9 - 1447.9	1475.9 - 1495.9
12	US 700 Lower A,B,C	699 - 716	729 - 746
13	US 700 Upper C	777 - 787	746 - 756
17	US 700 Lower B,C	704 - 716	734 - 746
18	850 (Japan #4)	815 - 830	860 - 875
19	850 (Japan #5)	830 - 845	875 - 890
20	CEPT 800	832 - 862	791 - 821
25	PCS 1900 G	1850 - 1915	1930 - 1995
26	E850 Upper	814 - 849	859 - 894
28	APT 700	703 - 748	758 - 803
31	LTE 450 Brazil	452.5 - 457.5	462.5 - 467.5
66	AWS Extension	1710 - 1780	2110 - 2200
70	AWS-3/4	1695 - 1710	1995 - 2020

Table A.2: User Equipment Power Class [27]

EUTRA band	Class 3 (dBm)	Tolerance (dB)	Class 5 (dBm)	Tolerance (dB)	Class 6 (dBm)	Tolerance (dB)
1	23	±2	20	±2	14	±2.5
2	23	±2	20	±2	14	±2.5
3	23	±2	20	±2	14	±2.5
5	23	±2	20	±2	14	±2.5
8	23	±2	20	±2	14	±2.5
11	23	±2	20	±2	14	±2.5
12	23	±2	20	±2	14	±2.5
13	23	±2	20	±2	14	±2.5
17	23	±2	20	±2	14	±2.5
18	23	±2	20	±2	14	±2.5
19	23	±2	20	±2	14	±2.5
20	23	±2	20	±2	14	±2.5
21	23	±2	20	±2	14	±2.5
25	23	±2	20	±2	14	±2.5
26	23	±2	20	±2	14	±2.5
28	23	±2	20	±2	14	±2.5
31	23	±2	20	±2	14	±2.5
66	23	±2	20	±2	14	±2.5
70	23	±2	20	±2	14	±2.5

Table A.3: Power classes, 50 Ω

P_{dB}	P_W	V_p
14 dBm	0.0251 W	1.5849 V
20 dBm	0.1000 W	3.1623 V
23 dBm	0.1995 W	4.4668 V

Appendix B

3GPP Spurious Emissions

Table B.1: Spurious emissions limits [27]

Frequency Range	Maximum Level	Measurement bandwidth
9 kHz $\leq$ f $<$ 150 kHz	-36 dBm	1 kHz
150 kHz $\leq$ f $<$ 30 MHz	-36 dBm	10 kHz
30 MHz $\leq$ f $<$ 1000 MHz	-36 dBm	100 kHz
1 GHz $\leq$ f $<$ 12.5 GHz	-30 dBm	1 MHz
2.75 GHz $\leq$ f $<$ 5th harmonic of 2.2 GHz	-30 dBm	1 MHz
12.75 GHz $\leq$ f $<$ 26 GHz	-30 dBm	1 MHz

Appendix C

14 dBm switch data

Fig. C.1 shows IL and return loss of one series on-switch.

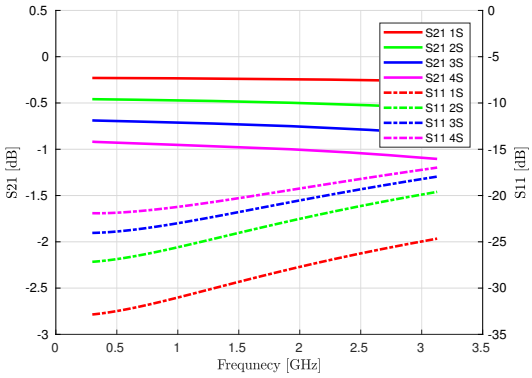

Figure C.1: Insertion loss and matching, series on-switch

Fig. C.2 shows the harmonic content generated by one series on-switch.

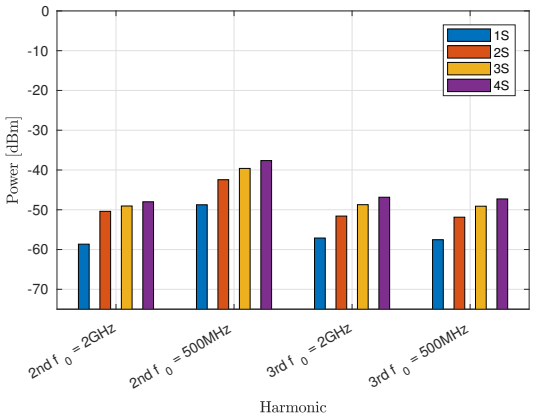

Figure C.2: Harmonic generation, series on-switch

Fig. C.3 shows the isolation by by one off-switch.

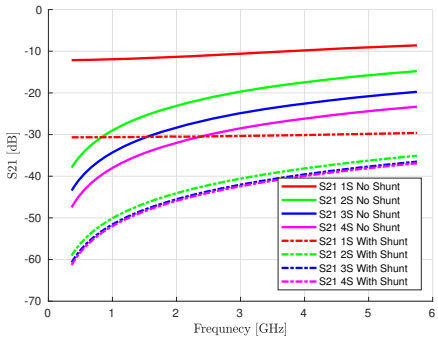

Figure C.3: Isolation, shunt off-switch

Fig. C.4 shows harmonics generated by one shunt off-switch.

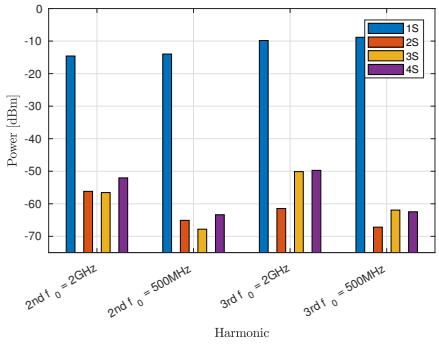

Figure C.4: Harmonics generation, shunt off-switch

Fig. C.5 shows the performance with respect to operating impedance.

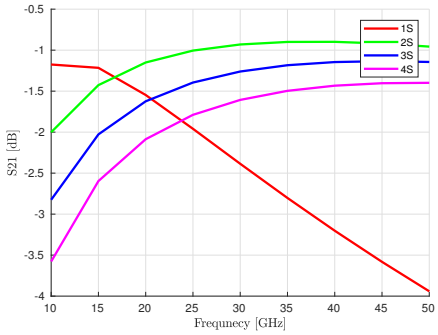

Figure C.5: Full system performance with respect to operating impedance

Fig. C.6 shows IL and isolation of the full system where a stacking of two transistors is used.

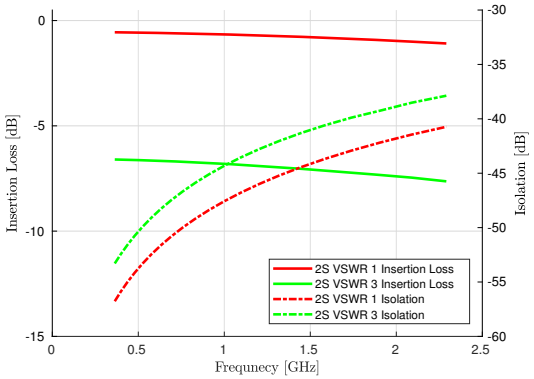

Figure C.6: Full setup insertion loss and isolation

Fig. C.7 shows the harmonic content from the full system setup with respect to load impedance.

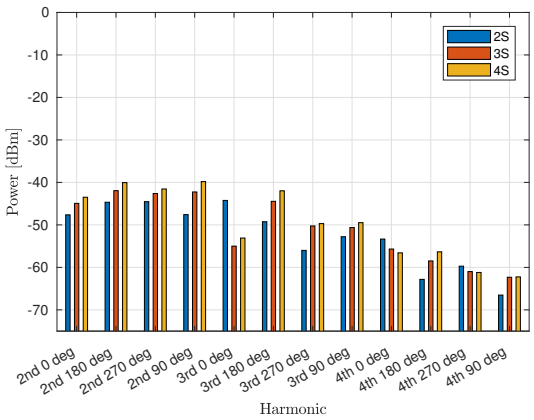

Figure C.7: VSWR of 3 and deg from 0 to 270, full setup

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