Phase Locked Loops in Fully Integrated NB-IoT Transceivers

Adam Waks
fek13awa@student.lu.se

Department of Electrical and Information Technology
Lund University

Supervisor: ARM: Staffan Ek, Magnus Nilsson and Tobias Tired
LTH: Henrik Sjöland

Examiner: Pietro Andreani

2018/06/07

Printed in Sweden
Tryckeriet i E-huset, Lund

Abstract

This thesis investigates how to fulfill the Narrow Band - Internet of Things (NB-IoT) specification for a fully integrated transceiver in the phase locked loop's (PLL) perspective. Designing a fully integrated transceiver, integrating a power amplifier (PA) is challenging as it leads to frequency pulling of the voltage controlled oscillator (VCO) in the PLL, deteriorating the performance. By increasing the bandwidth of the PLL, the frequency pulling can be suppressed, especially when the bandwidth is increased to at least twice the baseband bandwidth. The frequency pulling can be further suppressed by designing the PA balun in such a way that a common mode current cancels as well as designing the VCO inductor in an eight shape fashion, reducing the coupling from balun to inductor. The NB-IoT specification is extracted from 3GPP and translated to a phase noise requirement for the PLL and a parameterization of the PLL is made to ease the evaluation of the phase noise performance.

Keywords: *Phase locked loops, Narrow Band Internet of Things, Frequency pulling, Balun, Inductor*

Acknowledgments

I would like to thank Arm for the opportunity of writing this thesis, especially to my supervisors Staffan Ek, Magnus Nilsson and Tobias Tired who always seemed to have time to answer my questions and for giving input in the progress throughout this work.

To my supervisor at Lunds University, Henrik Sjöland for an academic view on my work.

To my friends Mattias and Axel who when I was in need for discussion regarding mathematics always had good input.

Lastly I would like to thank my girlfriend Lotta for enduring constantly hearing me talk about frequency pulling.

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

This work will on behalf of Arm investigate the performance of an existing phase locked loop (PLL) in a Narrow Band - Internet of Things (NB-IoT) transceiver with an integrated power amplifier (PA). Optimization of the PA is outside the scope of this work and focus will be on the PLL performance. The work has been carried out with Arm and in association with Lunds University, the department of Electrical and Information Technology at the faculty of engineering.

1.1 Background

In the last decade, Internet of Things (IoT) and the demand for smart devices has grown massively and in June 2016 the specification for NB-IoT was completed. The use of PLLs in transceiver architectures has been widely examined and evaluated, but with new technologies comes new challenges. The demand from customers on NB-IoT developers is low power consumption, low maintenance, low cost and low complexity. Optimization of the transceiver can greatly reduce the power consumption and area and hence the cost, leading to a competitive edge. By integrating as much as possible on a single chip, the complexity as well as the cost can be greatly reduced giving a competitive edge.

1.2 Thesis objective

The goal with this work is to evaluate the feasibility of a fully integrated transceiver topology for NB-IoT from the PLL's perspective. The starting point of the work is an existing integrated $\Delta\Sigma$ PLL with up-converter. A linear PA has already been constructed but no evaluation of the different impairments this PA has on the transceiver has been made. This work will aim to investigate to what extent this existing PLL can be used with the PA. The work will include:

- The 3GPP specifications for NB-IoT will be studied and a mapping of the PLL requirement will be made in order to set the requirements for the PLL.
- A parameterisation of the performance of all blocks in the PLL will be made to ease the investigation of the overall performance.
- Investigation of the effects the integration of the PA has on the PLL.
- An implementation of the PLL for a fully integrated solution with integrated PA will be made.

1.3 Thesis outline

The thesis outline is as follows;
Chapter 2, Theory: Presents the theory covered in this thesis.
Chapter 3, Narrow band internet of things phase noise requirements: Translates the 3GPP specifications for NB-IoT to phase noise requirement for the PLL.
Chapter 4, Parameterization PLL: This chapter presents how the PLL is parameterized.
Chapter 5, Pulling assessment: This chapter presents different balun and inductor designs and how to alter the PLL to reduce the effect of pulling as well as how to construct the inductor for best voltage controlled oscillator performance phase noise performance.
Chapter 6, Conclusion: Conclusion of the thesis and future work.

Chapter 2

Theory

In communication systems, a PLL is used in the transceiver to generate a programmable frequency. This frequency is a rational multiple of a reference frequency generated by a crystal oscillator (XO).

A PLL can be described as a control system that fixes the phase of the output to a relation of the input phase [9]. A PLL will maintain lock over the hold in range; for a charge pump phase detector PLL given by [5]:

$$\pm\Omega_H = \pm\omega_0 * \pi, \tag{2.1}$$

where ω_0 is the loop velocity constant and is defined as:

$$\omega_0 \triangleq \lim_{s\to 0} s * G(s) \tag{2.2}$$

G(s) is the forward transfer function times the feedback transfer function in Laplace domain. A flowchart describing a charge pump based fractional-N PLL is presented in figure 2.1. This is the PLL topology in focus throughout this work.

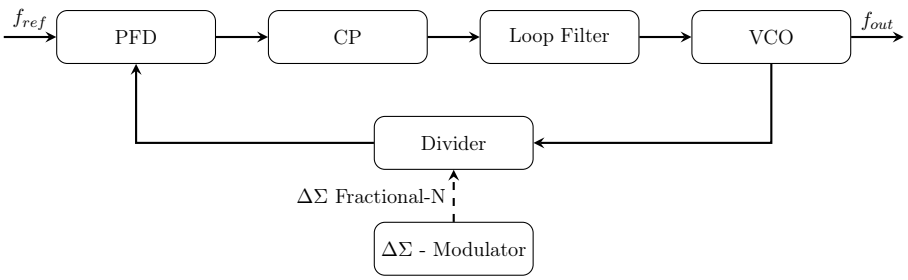


Figure 2.1: Flowchart presenting the blocks constituting the PLL

2.1 Thermal noise

The thermal noise from a passive component can be expressed as

$$\overline{v^2} = 4 * k * T * R * \Delta f \tag{2.3}$$

$$\overline{i^2} = 4 * k * T * \frac{1}{R} * \Delta f \tag{2.4}$$

where k is Boltzmann's constant, T is the temperature in Kelvin and R is the resistance of the component generating the noise. The noise is an RMS noise and can be expressed as an RMS noise voltage (2.3) or as an RMS noise current (2.4). The thermal noise due to reactive components is due to its real part, this real part is small for the capacitors and will not contribute to the overall noise performance and will be omitted in this work [17]. However, the inductors might have a low Q and hence have a relative high real part. This real part has to be considered when calculating the thermal noise. If the thermal noise is represented as a voltage, it can be modeled as an ideal resistor in series with a voltage source equal to (2.3). If it is modeled as a current it can be represented as an ideal resistor in parallel with a current source equal to (2.4).

2.2 Phase noise

Phase noise is a noise performance measure in the frequency domain. The IEEE definition of phase noise is:

$$\mathcal{L} \triangleq \frac{S_\varphi}{2}, \tag{2.5}$$

where S_φ is the phase power spectral density.

To measure phase noise, one looks at the integrated power over one Hz related to the carrier at a certain frequency offset. Deviation in time from the true periodicity of a signal is called jitter. When examining the jitter in the frequency domain, it will appear as a frequency offset. Phase is the integral of frequency, hence jitter causes phase noise.

2.3 Phase frequency detector

When the PLL is locked, the phase frequency detector (PFD) acts as a phase detector (PD). The PD together with the charge pump (CP) is to deliver a current proportional to the phase error to the loop filter.

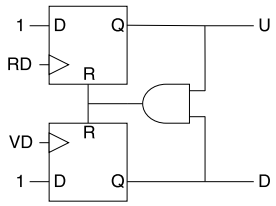


Figure 2.2: Phase detector

2.4 Charge pump

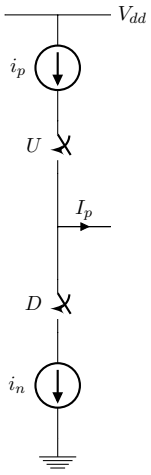


Figure 2.3: Charpe pump concept

The gain of the CP together with the PFD is given by the current delivered from the CP over one cycle of operation, hence:

$$K_{cp} = \frac{I_{cp}}{2\pi} \tag{2.6}$$

It is important that the current $i_n = i_p$ in order to ensure the same gain for both negative and positive phase error. If this is not satisfied, negative and positive phase error will generate different K_{cp} and the transfer function off the PLL will deviate from the intended.

Net up and down currents have to be zero in order to minimize frequency spikes

2.5 Loop filter

The transfer function of the PLL will mostly be determined by the characteristics of the loop filter. Extra poles and zeros can be introduced which will set the transient behavior of the PLL. By inserting an extra integrator in the loop, ω_0 becomes infinite (equation 2.2), hence the theoretical hold in range becomes infinite (equation 2.1). Introducing another pole at DC will cause instability and as a consequence an extra zero (ω_z) has to be inserted in order to ensure stability. More poles (ω_p) can be placed after the unity gain frequency (ω_L) without causing instability in order to suppress high frequency noise. To achieve maximum stability, ω_L should be placed at the geometrical mean of ω_z and ω_p; $\frac{\omega_L}{\omega_z} = \frac{\omega_p}{\omega_L}$. Doing this also gives a good compromise between suppression of VCO noise, response speed, phase margin and rejection of side bands [5]. In figure 2.4, a third-order passive filter is presented.

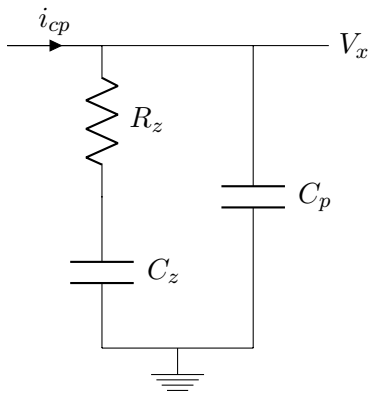


Figure 2.4: Passive third-order filter; integrator plus lead-lag

The transfer function for the filter in figure 2.4 from i_{cp} to V_x is given by:

$$G_x = \frac{s * (C_z + C_p)}{s^2 * R_z * C_z * C_p + s * (C_z * C_p)} \tag{2.7}$$

The bode plot for this filter is shown in figure 2.5.

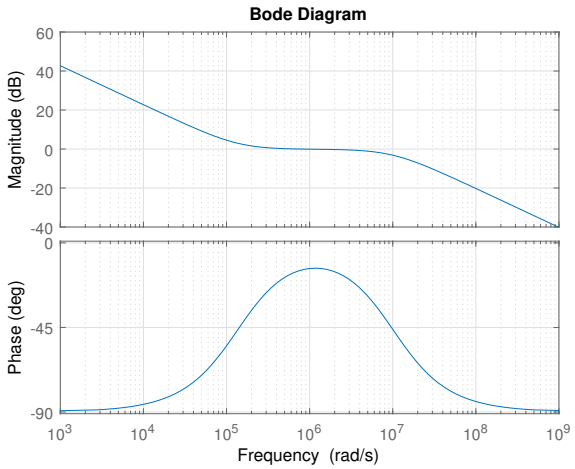


Figure 2.5: Bode plot of the third-order filter

Using a passive filter as in figure 2.4 is advantageous in the sense that it is easy to design, however there are some drawbacks. As discussed in section "Charge pump", the operation voltage for the CP is limited. Due to varying temperature, the frequency tuning characteristics of the VCO might change. Also the voltage V_x, from figure 2.4 will change with temperature, and as a consequence of the change frequency tuning of the VCO. This change in V_x might lead to a mismatch in the CP's Up and Down currents, hence changing K_{cp} and altering the transfer function for the PLL. Also the threshold voltage (V_t) of the transistors in the CP are temperature and process dependent. A combination of all this might lead to that the operation voltage for the CP is drifting out of the well defined operation region. In order to solve this, an active filter can be used where a reference voltage is set in order to assure an operation well inside the well defined operation region for the CP [4]. It should be mentioned that it is possible to compensate for this voltage drift in digital domain by compensating for the changed frequency tuning characteristics. Another drawback with using a passive filter is the finite input impedance.

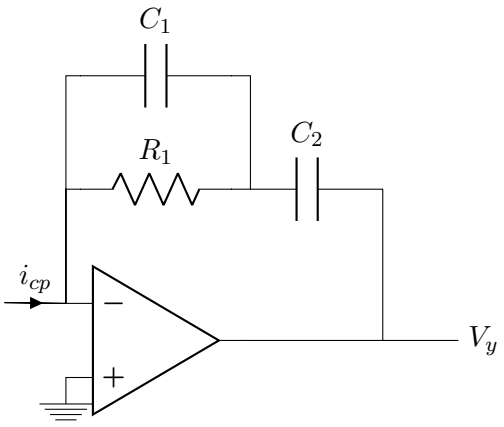


Figure 2.6: Active filter; integrator plus lead-lag

The transfer function for the filter in figure 2.6 from i_{cp} to V_x is given by:

$$G_y = \frac{1 + s * R_1 * (C_1 + C_2)}{s * C_2 * (1 + s * C_1 * R_1)} = \frac{1}{C_1} * \frac{1 + \frac{s}{\omega_z}}{s * (1 + \frac{s}{\omega_p})}, \tag{2.8}$$

where $\omega_z = \frac{1}{R_1 * (C_1 + C_2)}$ is a zero and $\omega_p = \frac{1}{R_1 * C_2}$ is a pole. The bode plot for this filter will be identical to its passive counterpart and is shown in figure 2.5.

In order to further suppress high frequency noise, a forth-order filter as in figure 2.7 can be utilized. However the low-pass filter constituting of R_2 and C_3 will increase the low frequency thermal noise.

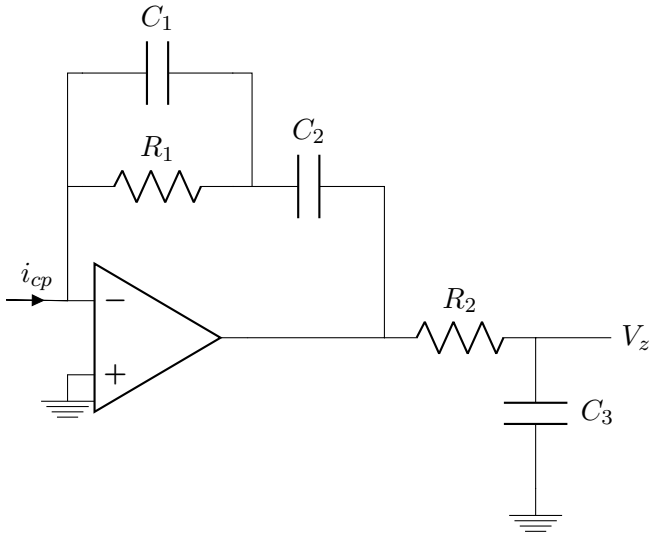


Figure 2.7: Active filter; integrator plus lead-lag with added low pass filter

By comparing figure 2.6 and 2.7, it can be noted that the transfer function for V_z will be given by V_x times the transfer function for a low pass filter comprised of R_2 and C_3.

$$G_z = G_y * \frac{1}{1 + s * R_2 * C_3} \tag{2.9}$$

The bode plot for this filter is shown in figure 2.8.

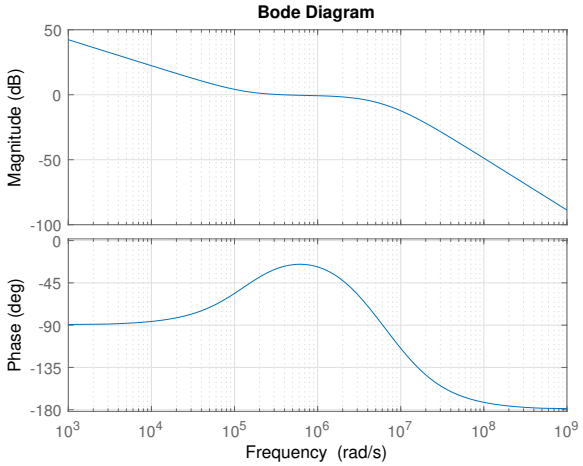


Figure 2.8: Bode plot of the forth-order active filter

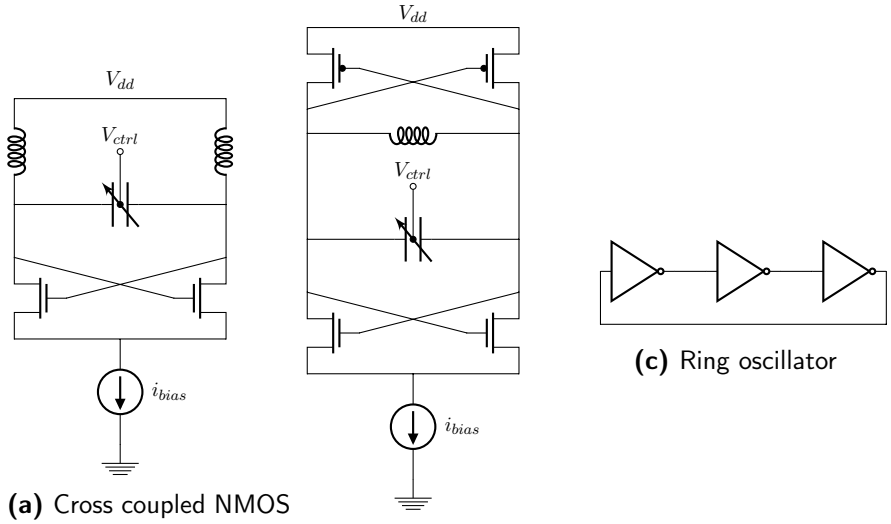
2.6 Voltage controlled oscillator

Oscillators consisting of an uneven number of inverters in a feedback system as shown in figure 2.9c are called Ring oscillators. They are easy to implement but have phase noise that is generally to high to consider them as a viable solution in communication systems [4]. The Q is typically low for these oscillators, and due to the switching nature of the ring oscillator, the noise is further increased [5]. Due to theses aspects, ring oscillators will not be considered here. In order to achieve a sufficient phase noise and Q for an integrated oscillator, an LC-oscillator topology can be used (shown in figure 2.9a and 2.9b). Q and the operational frequency will be determined by the LC-tank, where the frequency is determined by equation 2.10 and the unloaded Q is given by the inverse of equation 2.11.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.10}$$

$$\frac{1}{Q_{tank}} = \frac{1}{Q_{ind}} + \frac{1}{Q_{cap}} \tag{2.11}$$

In order to achieve full voltage swing from ground to V_{dd} a complementary topology (as in figure 2.9b) can be utilized in contrast to the only NMOS tolopogy (figure 2.9a) where the full voltage swing is $2 * V_{dd}$. Utilizing a complementary topology provides a robust operation voltage for thin oxide transistors, this is beneficial as the process variation is lower in thin oxide transistors compared to thick oxide [8], the transconductance is higher and there is less parasitic capacitance. By matching the transconductance of the NMOS and PMOS, phase noise up conversion can be lowered. This is due to that injected current in the output node will be canceled, also disturbance will generate equal current in the transistors and hence the negative effect will be minimized [20].



(a) Cross coupled NMOS LC VCO

(b) Cross coupled LC complementary push-pull VCO

(c) Ring oscillator

Figure 2.9: VCO

By using a varactor and applying a voltage (V_{ctrl}) to it, it is possible to alter the frequency of the VCO. In a PLL, this frequency change will correspond to the gain of the VCO, which is denoted K_{VCO} and is given by the tangent of the tuning characteristics of the VCO in Hz/volt. By inspecting figure 2.1 one can see that the VCO is the last block in the PLL, this implies that noise generated by preceding blocks will be multiplied by the transfer function of the VCO. In a transceiver, all frequency bands for the intended purpose have to be covered and hence the tuning range has to cover all frequency bands. In figure 2.10 the dashed line illustrates a varactor used to cover all bands, the gain of the VCO will be as high as the slope of the tuning range. In order to lower the gain of the VCO, capacitance can be switched in depending on the frequency band in operation and a smaller varactor can be used (illustrated by the solid lines in figure 2.10). Furthermore, the linearity of a CMOS varactor is limited, hence having a large coverage of the

varactor will likely jeopardize linearity of the tuning characteristics.

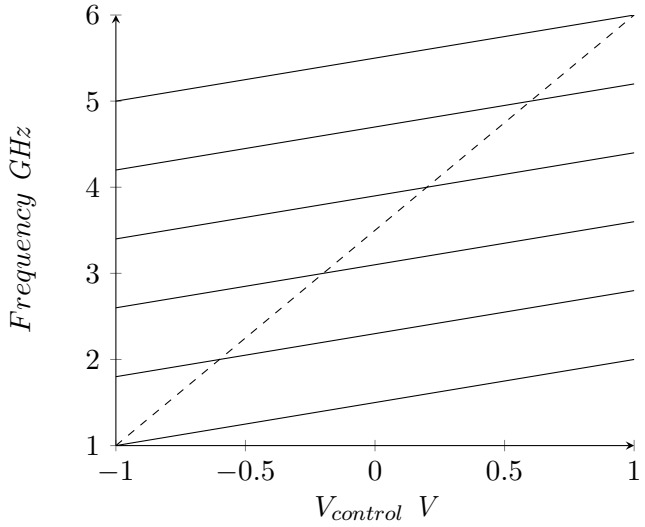


Figure 2.10: Illustration of tuning characteristics of a VCO

2.6.1 VCO phase noise

The phase noise of a VCO is given by Leeson equation:

$$\mathcal{L}(\omega_m) = 10{*}log\left(\frac{2*F*k*T}{P_{sig}} * (1 + \left(\frac{\omega_0}{2*Q*\Delta\omega}\right)^2) * (1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|})\right), \quad (2.12)$$

where, F is the noise factor of the VCO viewed as an amplifier, Q is the loaded Q, P_{sig} is the output power of the signal, ω_0 is the carrier frequency, $\Delta\omega$ is the frequency offset from the carrier frequency, T is temperature in Kelvin and k is Boltzmann's constant. From this equation it is possible to deduce that the roll off close to the carrier is $1/\omega^3$ up to the corner frequency of the device, and $1/\omega^2$ up to $\omega_0/2Q$ where the noise flattens out to a constant value of $10log(\frac{2FkT}{P_{sig}})$. It should be noted that measurements have shown that these frequencies can deviate from these values [9].

As Q_{ind} is generally much lower than Q_{cap} for frequencies below 5 GHz, Q_{tank} will mostly be determined by Q_{ind} (equation 2.11). Based on this assumption and further assuming a constant Q_{ind} regardless of inductor size and constant current bias, an analysis regarding phase noise as a function of inductor size can be made. The voltage swing in the VCO will be

$$V_{VCO} = I_{bias} * R_p, \quad (2.13)$$

where R_p is the equivalent parallel resistance in the tank. Based on the assumption that Q_{ind} will determine Q_{tank} implies that

$$Q_{tank} = Q_{ind} = \frac{R_p}{\omega_0 * L} \tag{2.14}$$

The power of the signal is

$$P_{sig} = \frac{V^2}{R_p} = \frac{(I_{bias} * R_p)^2}{R_p} \propto R_p, \tag{2.15}$$

based on the assumption that I_{bias} is constant. From equation 2.12 and 2.15 it is apparent that;

$$\mathcal{L}(\omega_m) \propto \frac{1}{P_{sig}} \propto \frac{1}{R_p} = \frac{1}{Q * \omega_0 * L}, \tag{2.16}$$

hence $\mathcal{L}(\omega_m) \propto \frac{1}{L}$. When the inductance is made so large that V_{VCO} no longer increases ($V_{VCO} = V_{dd}$ in a complementary VCO topology), equation 2.15 becomes;

$$P_{sig} \propto \frac{1}{R_p} \Rightarrow \mathcal{L}(\omega_m) \propto \frac{1}{P_{sig}} \propto R_p \propto L \tag{2.17}$$

From this analysis it can be concluded that increasing the size of the inductor will improve the phase noise performance of the VCO until the point where the voltage swing is no longer increased and then the phase noise performance will start to degrade.

2.6.2 Frequency pulling VCO

Interfering frequencies on the VCO may lead to sidebands appearing on each side of the VCO output due to frequency pulling of the VCO [5]. Based on the findings in [22], these sidebands will be visible at the frequencies $\omega_0 \pm (\omega_i - \omega_0)$ when the interfering frequency (ω_i) is far from the VCO frequency (ω_0). When the interfering frequency is closer to the VCO frequency and the power of the interferer is sufficiently high the VCO will be in a so called "quasi lock". The first side bands will appear at $\omega' \pm \Omega$ and the other side bands will appear asymmetrical around the VCO frequency. To increase the readability, table 2.1 will serve as a conspectus of the variables describing the pulling effects.

Variable	Description
ω_0	Free running VCO frequency
ω_i	Interfering frequency
$\Delta\omega_0$	$\omega_0 - \omega_i$
ω_L	Lock range = $\frac{\omega_0}{2Q}\frac{E_i}{E_{osc}}$
ω'	$\omega_0 + \frac{a^2}{2}\Delta\omega_0$
a	$\frac{\omega_L}{\Delta\omega_0}$
A_0	Amplitude of the VCO
Ω	$\Delta\omega_0 - \alpha(t)$
$\alpha(t)$	$\frac{a^2}{2\Delta\omega_0}$

Table 2.1: Description of the variables used to describe the frequency pulling effect of the VCO.

The maximum amplitude when in "quasi lock" will be $A_0 * (1 - \frac{a^2}{4})$ for the VCO frequency, $\frac{A_0 a}{2} * (1 + \frac{a^2}{4})$ for the sideband at frequency $\omega' + \Omega$ and $\frac{A_0 a}{2}$ for the sideband at $\omega' - \Omega$. When the interferer is well outside the frequency locking range, there will be two sidebands with the relative amplitude of [15]:

$$\textit{Relative sideband amplitude} = \frac{1}{2} * \frac{\omega_L}{\Delta\omega_0}, \tag{2.18}$$

2.7 Frequency pulling PLL

Figure 2.11 illustrates the origin of frequency pulling considered in this thesis for a fully integrated transceiver. N will be 2, 4 or 8 depending on which frequency band to transmit on. When N is 2, the second order harmonic of the PA is approximately the same frequency as the VCO frequency. This second order harmonic, through the coupling from the PA balun to the VCO inductor will cause frequency pulling. As the pulling is caused by the PA, through the balun; the balun is called aggressor and the inductor is called victim.

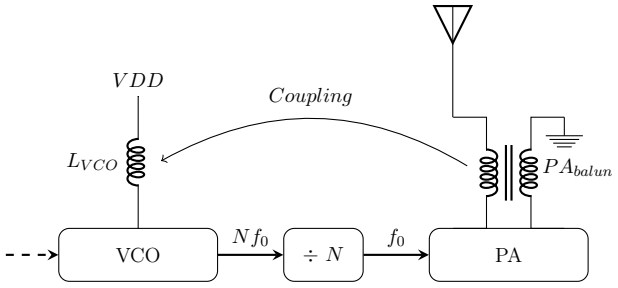


Figure 2.11: Flowchart illustrating the source of frequency pulling in a fully integrated transceiver.

In [19] an analysis of frequency pulling of a PLL with a first order filter is made. It is stated here that if the difference between the pulling frequency and the operating frequency of the VCO is inside the range of the PLL bandwidth, the effect of pulling is suppressed.

In [13] and [3] an analysis of the effects of pulling of the VCO in a PLL is made for a transmitter. The equation describing the phase deviation from the original due to frequency pulling is given by

$$\Theta(j\omega) = \frac{\omega_0 * I_2(j\omega)}{2 * Q * I_s * (j\omega + \frac{K_{VCO}}{N} * \frac{I_{CP}}{2*\pi} * H_{filter}(j\omega))} \tag{2.19}$$

where Q is the Q of the LC tank in the VCO, ω_0 is the operating frequency of the VCO, I_s is the bias current of the VCO, N is the divide ratio of the divider in the feedback of the PLL, H_{filter} is the transfer function of the PLL filter and $I_2(j\omega)$ is the Fourier transform of the current of the second order harmonic from the power amplifier (PA) with a modulated signal (equation 2.20).

$$k * i_2 * A_{BB}^2(t) * sin(2 * \theta_{BB}(t)) \xrightarrow{\mathcal{F}} I_2(j\omega) \tag{2.20}$$

where, k is the coupling from the PA to the VCO, i_2 is the current of the second order harmonic from the PA, $A_{BB}(t)$ is the amplitude of the baseband modulation and $\theta_{BB}(t)$ is the phase of the baseband modulation.

2.8 Fractional-N PLL

In order to implement a feasible PLL for NB-IoT the frequency accuracy has to be higher than the spacing between the channels. Utilizing only the divider in the feedback of the PLL architecture results in a fixed integer division ratio. This implies that only an integer of the reference frequency can be generated by the PLL, hence the reference frequency has to be as low as the channel spacing. A low reference frequency leads to a limited loop bandwidth and according to [4] the loop bandwidth can be maximum a tenth of the reference frequency in order to assure linear operation of the phase detector. Also, a low reference frequency leads to a high N multiplying the noise of the reference frequency, the loop filter and the phase frequency detector with a larger number.

By letting the divider alter between N+1 and N the PLL can lock to the average of the two, making the output frequency an integer plus a fraction where the fraction will set the resolution of the output frequency and hence mitigating the need of a low reference frequency. It is from this fraction the architecture got its name $Fractional - N\ PLL$.

The technique presented above introduces spurs due to the multiplying pattern when generating the fraction, and reference sub-harmonics corresponding to the least common divisor of the fractional frequency and the reference frequency is to

be expected [5]. The problem with this architecture is intensified when the fraction is close to 0 or 1 as the frequency of the switching between N and N+1 is low and will introduce low frequency noise which cannot be filtered by the PLL. To reduce this problem a $\Delta\Sigma$ modulator (DSM) can be used.

2.8.1 Delta sigma modulator

A DSM has noise-shaping properties and shifts the frequency from DC to higher frequencies for all multiples of the reference frequency. However, this noise shaping properties are not valid for first order DSM with DC-inputs, and hence a higher order DSM should be used [23] [21]. This high frequency noise will be filtered by the loop filter and it should be noted that a higher PLL bandwidth reduces the filtering of spurs from the DSM modulator.

Chapter 3

Narrow band internet of things phase noise requirements

3.1 Receiver requirement

3.1.1 Selectivity

Signals close to the frequency band of the desired signal, called blockers, might affect the performance of the receiver. These out-of-band blockers in combination with the phase noise of the PLL can lead to down conversion of the blocker to the intermediate frequency (IF) of the receiver, called reciprocal mixing. This happens if the blocker and the phase noise of the PLL are at the same offset as the desired signal is to the center frequency of the PLL. The maximum phase noise in order to achieve a selectivity of a given value is determined by:

$$\mathcal{L}(f_m) = C - S - I - 10log(B), [dBc/Hz], \tag{3.1}$$

where $\mathcal{L}(f_m)$ is the phase noise at the offset frequency f_m, C is the desired signal in dBm, S is the selectivity in dB, I is the interfering signal in dBm and B is the bandwidth of the Intermediate frequency filter in Hz [18]. One could argue that equation 3.1 overestimates the required phase noise performance of the PLL, as mixing of the desired signal with the blocker will be spread out over the frequency spectra of the frequency from the desired signal to the frequency of the blocker (figure 3.1). To account for this, the phase noise can be integrated over the frequency spectra. From equation 2.12 the noise figure can be estimated as a $1/f^2$ roll-off from the VCO, leading to equation 3.2.

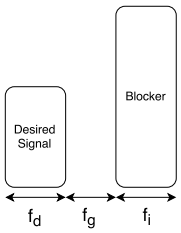


Figure 3.1: Interfering signal

$$K = \frac{1}{f_i * f_d} * \int_0^{f_i} \int_{f+f_g}^{f+f_g+f_d} \left(\frac{f_g}{f}\right)^2 df df = \frac{f_g^2}{f_i * f_d} * (ln\left(\frac{f_i + f_g}{f_i + f_g + f_d}\right) - ln\left(\frac{f_g}{f_g + f_d}\right)), \tag{3.2}$$

where f_d is the bandwidth of the desired signal, f_g is the frequency difference between desired and interfering signal and f_i is the bandwidth of the interfering signal (figure 3.1). Notice the factor $(f_g/f)^2$ from equation 2.12, w_0 is changed to f_g here as it is the phase noise at the frequency f_g we are weighting. Equation 3.1 can now be rewritten as:

$$\mathcal{L}(f_m) = C - S - I - 10log(B) - K, [dBc/Hz], \tag{3.3}$$

The specification for the receiver in NB-IoT constitutes of three requirements that will determine the phase noise of the PLL; Adjacent channel selectivity (ACS), In-band blocking and Out-of-band blocking. Some parameters are needed in order to perform the calculations.

- The Signal-to-noise ratio (SNR, corresponding to S in equation 3.1 and 3.3) is 0 dB (given from simulations previously made by ARM).
- The reference sensitivity (REFSENSE) is -108.2 dBm.

Table 7.5.1F: Adjacent channel selectivity parameters for category NB1 and NB2

ACS1 test Parameters		
Interferer	**GSM (GMSK)**	**E-UTRA**
Category NB1 or NB2 signal power (P_{wanted}) / dBm	REFSENS + 14 dB	
Interferer signal power ($P_{Interferer}$) / dBm	REFSENS + 42 dB	REFSENS + 47 dB
Interferer bandwidth	200 kHz	5 MHz
Interferer offset from category NB1 or NB2 channel edge	±200 kHz	±2.5 MHz
ACS2 test Parameters		
Interferer	**GSM (GMSK)**	**E-UTRA**
Category NB1 or NB2 signal power (P_{wanted}) / dBm	-53 dBm	-58 dBm
Interferer signal power ($P_{Interferer}$) / dBm	-25 dBm	
Interferer bandwidth	200 kHz	5 MHz
Interferer offset from category NB1 or NB2 channel edge	±200 kHz	±2.5 MHz

Figure 3.2: ACS from 3GPP specifications [1].

Table 7.6.1.1F-1: In-band blocking parameters for category NB1 and NB2

IBB1 test Parameters	
Category NB1 or NB2 signal power (P_{wanted}) / dBm	REFSENS + 6 dB
Interferer	E-UTRA
Interferer signal power ($P_{Interferer}$) / dBm	- 56 dBm
Interferer bandwidth	5 MHz
Interferer offset from category NB1 or NB2 channel edge	+7.5 MHz + 0.005 MHz and -7.5 MHz - 0.005 MHz
IBB2 test Parameters	
Category NB1 or NB2 signal power (P_{wanted}) / dBm	REFSENS + 6 dB
Interferer	E-UTRA
Interferer signal power ($P_{Interferer}$) / dBm	- 44 dBm
Interferer bandwidth	5 MHz
Interferer offset range from category NB1 or NB2 channel edge	From +12.5 MHz to F_{DL_high} + 15 MHz and From -12.5 MHz to F_{DL_low} - 15 MHz

Figure 3.3: In-band-blocking from 3GPP specifications [1].

Table 7.6.2.1F-1: Out-of-band blocking parameters for category NB1 and NB2 UE

Parameter	Units	Frequency		
		Range 1	Range 2	Range 3
P_{wanted}	dBm	REFSENS + 6 dB		
$P_{interferer}$ (CW)	dBm	-44	-30	-15
$F_{interferer}$ range	MHz	F_{DL_low} - 15 to F_{DL_low} - 60	F_{DL_low} - 60 to F_{DL_low} - 85	F_{DL_low} - 85 to 1 MHz
	MHz	F_{DL_high} + 15 to F_{DL_high} + 60	F_{DL_high} + 60 to F_{DL_high} + 85	F_{DL_high} + 85 to 12750 MHz
NOTE 1: For operating bands which downlink band frequency range is between 729 MHz < f < 1 GHz the power level of the interferer ($P_{Interferer}$) for Range 3 shall be modified to: -18 dBm for the frequency range which is bounded by F_{DL_low} - 150 MHz of the lowest band that UE supports in frequency range 729 MHz < f < 1 GHz and F_{DL_high} + 150 MHz of the highest band that UE supports in frequency range 729 MHz < f < 1 GHz.				
NOTE 2: For operating bands which downlink band frequency range is between 1475.9 MHz < f < 2200 MHz the power level of the interferer ($P_{Interferer}$) for Range 3 shall be modified to: -20 dBm for the frequency range which is bounded by F_{DL_low} - 200 MHz of the lowest band that UE supports in frequency range 1475.9 MHz < f < 2200 MHz and F_{DL_high} + 200 MHz of the highest band that UE supports supports in frequency range 1475.9 MHz < f < 2200 MHz.				
NOTE 3: For operating bands which downlink band frequency range is between 462.5 MHz < f < 467.5 MHz the power level of the interferer ($P_{Interferer}$) for Range 3 shall be modified to: – 18 dBm for the frequency range which is bounded by F_{DL_low} - 150 MHz of the lowest band that UE supports in frequency range 462.5 MHz < f < 467.5 0 MHz and F_{DL_high} + 150 MHz of the highest band that UE supports supports in frequency range 462.5 MHz < f < 467.5.				

Figure 3.4: Out-of-band blocking from 3GPP specifications [1].

Inserting the parameters from figure 3.2, 3.3 and 3.4 in equation 3.2 and 3.3 results in the values presented in table 3.1. The bandwidth (interferer bandwidth) given in the 3GPP specification has been scaled with 0.9*bandwidth as LTE utilizes 10 % of the bandwidth as guard bands.

Requirement	Blocker	Frequency offset KHz	$\mathcal{L}(f_m)$ dBc/Hz
ACS1	GSM	110	-75.4
	E-UTRA	250	-83.6
ACS2	GSM	110	-73.2
	E-UTRA	250	-71.5
IBB1	E-UTRA	5255	-96.0
IBB2	E-UTRA	10250	-109
Out-of-band blocking	Range 1	15000	-110.8
	Range 2	60000	-124.8
	Range 3	85000	-139.8
	NOTE 1	15000	-136.8
	NOTE 2	20000	-134.8
	NOTE 3	15000	-136.8

Table 3.1: Phase noise requirements due to blockers, calculated using equation 3.3 and values from figure 3.4.

3.2 Transmitter requirement

3.2.1 Adjacent Channel Leakage Ratio

Table 6.6.2F.3-1: category NB1 and NB2 UE ACLR requirements

	GSM_{ACLR}	$UTRA_{ACLR}$
ACLR	20 dB	37 dB
Adjacent channel center frequency offset from category NB1 or NB2 Channel edge	±200 kHz	±2.5 MHz
Adjacent channel measurement bandwidth	180 kHz	3.84 MHz
Measurement filter	Rectangular	RRC-filter α=0.22
Category NB1 and NB2 channel measurement bandwidth	180 kHz	180 kHz
Category NB1 and NB2 channel Measurement filter	Rectangular	Rectangular

Figure 3.5: ACLR requirement from 3GPP [1].

$$\mathcal{L}(f_m) = ACLR - 10log(B_{ACLR}) - K, \tag{3.4}$$

where ACLR is the maximum power and B_{ACLR} is the adjacent channel measurement bandwidth given in figure 3.5 and K is calculated using equation 3.2.

3.2.2 Spurious emission

Table 6.6.3.2-1: Requirements

E-UTRA Band	Spurious emission				
	Protected band	Frequency range (MHz)		Maximum Level (dBm)	MBW (MHz)	NOTE
1	E-UTRA Band 1, 5, 7, 8, 11, 18, 19, 20, 21, 22, 26, 27, 28, 31, 32, 38, 40, 41, 42, 43, 44, 45, 65, 67, 68, 69	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 3, 34	F_{DL_low}	F_{DL_high}	-50	1	15
	Frequency range	1880	1895	-40	1	15, 27
	Frequency range	1895	1915	-15.5	5	15, 26, 27
	Frequency range	1915	1920	+1.6	5	15, 26, 27
2	E-UTRA Band 4, 5, 10, 12, 13, 14, 17, 25, 26, 27, 28, 29, 30, 41, 42, 48, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 2, 25	F_{DL_low}	F_{DL_high}	-50	1	15
	E-UTRA Band 43	F_{DL_low}	F_{DL_high}	-50	1	2
3	E-UTRA Band 1, 5, 7, 8, 20, 26, 27, 28, 31, 32, 33, 34, 38, 39, 40, 41, 43, 44, 45, 65, 67, 68, 69	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 3	F_{DL_low}	F_{DL_high}	-50	1	15
	E-UTRA Band 11, 18, 19, 21	F_{DL_low}	F_{DL_high}	-50	1	13
	E-UTRA Band 22, 42	F_{DL_low}	F_{DL_high}	-50	1	2
	Frequency range	1884.5	1915.7	-41	0.3	13
4	E-UTRA Band 2, 4, 5, 7, 10, 12, 13, 14, 17, 24, 25, 26, 27, 28, 29, 30, 41, 43, 46, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 42	F_{DL_low}	F_{DL_high}	-50	1	2
5	E-UTRA Band 1, 2, 3, 4, 5, 7, 8, 10, 12, 13, 14, 17, 24, 25, 28, 29, 30, 31, 34, 38, 40, 42, 43, 45, 48, 65, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 26	859	869	-27	1	
	E-UTRA Band 41	F_{DL_low}	F_{DL_high}	-50	1	2
	E-UTRA Band 18, 19	F_{DL_low}	F_{DL_high}	-40	1	39
	E-UTRA Band 11, 21	F_{DL_low}	F_{DL_high}	-50	1	39
	Frequency range	1884.5	1915.7	-41	0.3	8, 39
6	E-UTRA Band 1, 9, 11, 34	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	860	875	-37	1	
	Frequency range	875	895	-50	1	
	Frequency range	1884.5	1919.6	-41	0.3	7
		1884.5	1915.7			8
7	E-UTRA Band 1, 2, 3, 4, 5, 7, 8, 10, 12, 13, 14, 17, 20, 22, 26, 27, 28, 29, 30, 31, 32, 33, 34, 40, 42, 43, 65, 66, 67, 68	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	2570	2575	+1.6	5	15, 21, 26
	Frequency range	2575	2595	-15.5	5	15, 21, 26
	Frequency range	2595	2620	-40	1	15, 21
8	E-UTRA Band 1, 20, 28, 31, 32, 33, 34, 38, 39, 40, 45, 65, 67, 68, 69	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA band 3, 7, 22, 41, 42, 43	F_{DL_low}	F_{DL_high}	-50	1	2
	E-UTRA Band 8	F_{DL_low}	F_{DL_high}	-50	1	15
	E-UTRA Band 11, 21	F_{DL_low}	F_{DL_high}	-50	1	23
	Frequency range	860	890	-40	1	15, 23
	Frequency range	1884.5	1915.7	-41	0.3	8, 23
9	E-UTRA Band 1, 11, 18, 19, 21, 26, 28, 34	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 42	F_{DL_low}	F_{DL_high}	-50	1	2
	Frequency range	945	960	-50	1	
	Frequency range	1839.9	1879.9	-50	1	
	Frequency range	1884.5	1915.7	-41	0.3	8
	Frequency range	2545	2575	-50	1	
	Frequency range	2595	2645	-50	1	
10	E-UTRA Band 2, 4, 5, 10, 12, 13, 14, 17, 24, 25, 26, 27, 28, 29, 30, 41, 43, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 22, 42	F_{DL_low}	F_{DL_high}	-50	1	2
11	E-UTRA Band 1, 11, 18, 19, 21, 28, 34, 42, 65	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	945	960	-50	1	
	Frequency range	1839.9	1879.9	-50	1	
	Frequency range	1884.5	1915.7	-41	0.3	8
	Frequency range	2545	2575	-50	1	
	Frequency range	2595	2645	-50	1	
12	E-UTRA Band 2, 5, 13, 14, 17, 24, 25, 26, 27, 30, 41, 48,	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 4, 10, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	2
	E-UTRA Band 12	F_{DL_low}	F_{DL_high}	-50	1	15
13	E-UTRA Band 2, 4, 5, 10, 12, 13, 17, 25, 26, 27, 29, 41, 48, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 14	F_{DL_low}	F_{DL_high}	-50	1	15
	E-UTRA Band 24, 30	F_{DL_low}	F_{DL_high}	-50	1	2
	Frequency range	769	775	-35	0.00625	15
	Frequency range	799	805	-35	0.00625	11, 15
14	E-UTRA Band 2, 4, 5, 10, 12, 13, 14, 17, 25, 24, 25, 26, 27, 29, 30, 41, 48, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	769	775	-35	0.00625	12, 15
	Frequency range	799	805	-35	0.00625	11, 12, 15
17	E-UTRA Band 2, 5, 13, 14, 17, 24, 25, 26, 27, 30, 41, 48	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 4, 10, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	2
	E-UTRA Band 12	F_{DL_low}	F_{DL_high}	-50	1	15
18	E-UTRA Band 1, 11, 21, 34, 42, 65	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	758	799	-50	1	
	Frequency range	799	803	-40	1	15
	Frequency range	860	890	-40	1	
	Frequency range	945	960	-50	1	
	Frequency range	1839.9	1879.9	-50	1	
	Frequency range	1884.5	1915.7	-41	0.3	8
	Frequency range	2545	2575	-50	1	
	Frequency range	2595	2645	-50	1	
19	E-UTRA Band 1, 11, 21, 28, 34, 42, 65	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	945	960	-50	1	
	Frequency range	1839.9	1879.9	-50	1	
	Frequency range	1884.5	1915.7	-41	0.3	8
	Frequency range	2545	2575	-50	1	
	Frequency range	2595	2645	-50	1	
20	E-UTRA Band 1, 3, 7, 8, 22, 31, 32, 33, 34, 40, 43, 65, 67, 68	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 20	F_{DL_low}	F_{DL_high}	-50	1	15
	E-UTRA Band 38, 42, 69	F_{DL_low}	F_{DL_high}	-50	1	2
	Frequency range	758	788	-50	1	
21	E-UTRA Band 1, 18, 19, 28, 34, 42, 65	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	945	960	-50	1	
	Frequency range	1839.9	1879.9	-50	1	
	Frequency range	1884.5	1915.7	-41	0.3	8
	Frequency range	2545	2575	-50	1	
	Frequency range	2595	2645	-50	1	
22	E-UTRA Band 1, 3, 7, 8, 20, 26, 27, 28, 31, 32, 33, 34, 38, 39, 40, 43, 65, 67, 68, 69	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	3510	3525	-40	1	15
	Frequency range	3525	3590	-50	1	
23	E-UTRA Band 4, 5, 10, 12, 13, 14, 17, 23, 24, 26, 27, 29, 30, 41, 66	F_{DL_low}	F_{DL_high}	-50	1	
24	E-UTRA Band 2, 4, 5, 10, 12, 13, 14, 17, 24, 25, 26, 29, 30, 41, 48, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
25	E-UTRA Band 4, 5, 10,12, 13, 14, 17, 24, 26, 27, 28, 29, 30, 41, 42, 48, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 2	F_{DL_low}	F_{DL_high}	-50	1	15
	E-UTRA Band 25	F_{DL_low}	F_{DL_high}	-50	1	15
	E-UTRA Band 43	F_{DL_low}	F_{DL_high}	-50	1	2
26	E-UTRA Band 1, 2, 3, 4, 5, 10, 11, 12, 13, 14, 17, 18,19, 21, 24, 25, 26, 29, 30, 31, 34, 39, 40, 42, 43, 48, 65, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 41	F_{DL_low}	F_{DL_high}	-50	1	2
	Frequency range	703	799	-50	1	
	Frequency range	799	803	-40	1	15
	Frequency range	945	960	-50	1	
	Frequency range	1884.5	1915.7	-41	0.3	8
27	E-UTRA Band 1, 2, 3, 4, 5, 7, 10,12, 13, 14, 17, 25, 26, 27, 29, 30, 31, 38, 40, 41, 42, 43, 65, 66	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 28	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	799	805	-35	0.00625	
28	E-UTRA Band 1, 2, 4, 10, 22, 42, 43, 65	F_{DL_low}	F_{DL_high}	-50	1	2
	E-UTRA Band 1	F_{DL_low}	F_{DL_high}	-50	1	19, 25
	E-UTRA Band 2, 3, 5, 7, 8, 18, 19, 20, 25, 26, 27, 31, 34, 38, 40, 41, 66	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 11, 21	F_{DL_low}	F_{DL_high}	-50	1	19, 24
	Frequency range	470	694	-42	8	15, 35
	Frequency range	470	710	-26.2	6	34
	Frequency range	662	694	-26.2	6	15
	Frequency range	758	773	-32	1	15
	Frequency range	773	803	-50	1	
	Frequency range	1884.5	1915.7	-41	0.3	8, 19
30	E-UTRA Band 2, 4, 5, 7, 10, 12, 13, 14, 17, 24, 25, 26, 27, 29, 30, 38, 41, 48, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
31	E-UTRA Band 1, 5, 7, 8, 20, 22, 26, 27, 28, 31, 32, 33, 34, 38, 39, 40, 42, 43, 65, 67, 68, 69	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 3	F_{DL_low}	F_{DL_high}	-50	1	2
	Frequency range	470	694	-42	8	
...						
33	E-UTRA Band 1, 7, 8, 20, 22, 28, 31, 32, 34, 38, 40, 42, 43, 65, 67, 69	F_{DL_low}	F_{DL_high}	-50	1	5
	E-UTRA Band 3	F_{DL_low}	F_{DL_high}	-50	1	15
34	E-UTRA Band 1, 3, 7, 8, 11, 18, 19, 20, 21, 22, 26, 28, 31, 32, 33, 38,39, 40, 41, 42, 43, 44, 45, 65, 67, 69	F_{DL_low}	F_{DL_high}	-50	1	5
	Frequency range	1884.5	1915.7	-41	0.3	8
35						
...						
36						
37						
38	E-UTRA Band 1, 2, 3, 4, 5, 8, 10,12, 13, 14, 17, 20, 22, 27, 28, 29, 30, 31, 32, 33, 34, 40, 42, 43, 65, 66, 67, 68	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	2620	2645	-15.5	5	15, 22, 26
	Frequency range	2645	2690	-40	1	15, 22
39	E-UTRA Band 1, 8, 22, 26, 34, 40, 41, 42, 44, 45	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	1805	1855	-40	1	33
	Frequency range	1855	1880	-15.5	5	15,26,33
40	E-UTRA Band 1, 3, 5, 7, 8, 20, 22, 26, 27, 28, 31, 32, 33, 34, 38, 39, 41, 42, 43, 44, 45, 65, 67, 68, 69	F_{DL_low}	F_{DL_high}	-50	1	
41	E-UTRA Band 1, 2, 3, 4, 5, 8, 10, 12, 13, 14, 17, 24, 25, 26, 27, 28, 29, 30, 34, 39, 40, 42, 44, 45, 48, 65, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 9, 11, 18, 19, 21	F_{DL_low}	F_{DL_high}	-50	1	30
	Frequency range	1884.5	1915.7	-41	0.3	8, 30
42	E-UTRA Band 1, 2, 3, 4, 5, 7, 8, 10, 11, 18, 19, 20, 21, 25, 26, 27, 28, 31, 32, 33, 34, 38, 40, 41, 44, 45, 65, 66, 67, 68, 69	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	1884.5	1915.7	-41	0.3	8
43	E-UTRA Band 1, 2, 3, 4, 5, 7, 8, 10, 20, 25, 26, 27, 28, 31,32, 33, 34, 38, 40, 65, 66, 67, 68, 69	F_{DL_low}	F_{DL_high}	-50	1	
44	E-UTRA Band 1, 40, 42, 45	F_{DL_low}	F_{DL_high}	-50	1	2
	E-UTRA Band 3, 5, 8, 34, 39, 41	F_{DL_low}	F_{DL_high}	-50	1	
45	E-UTRA Band 1, 3, 5, 8, 34, 39, 40, 41, 42,44	F_{DL_low}	F_{DL_high}	-50	1	
...						
47	E-UTRA Band 1, 3, 5, 7, 8, 22, 26, 28, 34, 39, 40, 41, 42, 44, 45, 65, 68	F_{DL_low}	F_{DL_high}	-50	1	
	Frequency range	5925	5950	-30	1	38, 40
	Frequency range	5815	5855	-30	1	38
...						
48	E-UTRA Band 2, 4, 5, 12, 13, 14, 17, 24, 25, 26, 29, 30, 41, 66, 70	FD_{L_low}	FD_{L_high}	-50	1	
65	E-UTRA Band 1, 7, 8, 20, 22, 28, 31, 32, 38, 40, 42, 43, 65, 68, 69	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 3	F_{DL_low}	F_{DL_high}	-50	1	15
	E-UTRA Band 5, 11, 18, 19, 21, 26, 27, 41	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 34	F_{DL_low}	F_{DL_high}	-50	1	36
	Frequency range	1884.5	1915.7	-41	0.3	37
	Frequency range	1900	1915	-15.5	5	15, 26, 27
	Frequency range	1915	1920	+1.6	5	15, 26, 27
66	E-UTRA Band 2, 4, 5, 7, 10, 12, 13, 14, 17, 24, 25, 26, 27, 28, 29, 30, 38, 41, 43, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 42, 48	F_{DL_low}	F_{DL_high}	-50	1	2
68	E-UTRA Band 3, 7, 8, 20, 22, 28, 31, 38, 40, 42, 43, 47, 68	F_{DL_low}	F_{DL_high}	-50	1	
	E-UTRA Band 1	F_{DL_low}	F_{DL_high}	-50	1	2
...						
70	E-UTRA Band 2, 4, 5, 10, 12, 13, 14, 17, 24, 25, 26, 29, 30, 41, 48, 66, 70	F_{DL_low}	F_{DL_high}	-50	1	2

Figure 3.6: 3GPP specifications for spurious emission, band 1, 2, 3, 5, 8, 11, 12, 13, 17, 18, 19, 20, 21, 25, 26, 28, 31, 66 and 70 are included in NB-IoT [1].

$$\mathcal{L}(f_m) = Maximum\ Level - P_{out} - 10 * log(MBW), \tag{3.5}$$

where P_{out} is the maximum output power from the transmitter as this will set the worst case, Maximum level and the measurement bandwidth (MBW) are given in figure 3.6.

3.2.3 Out of band emissions

Table 6.6.2F.1-1: category NB1 and NB2 UE spectrum emission mask

Δf_{OOB} (kHz)	Emission limit (dBm)	Measurement bandwidth
± 0	26	30 kHz
± 100	-5	30 kHz
± 150	-8	30 kHz
± 300	-29	30 kHz
± 500-1700	-35	30 kHz

Figure 3.7: Out of band emission specifications from 3GPP [1].

$$\mathcal{L}(f_m) = Emission\ limit - P_{out} - 10 * log(MBW), \tag{3.6}$$

where P_{out} is the maximum output power from the transmitter as this will set the worst case, emission limit and MBW are given in figure 3.7.

3.2.3.1 In-band emissions

Table 6.5.2F.3-1: Minimum requirements for in-band emissions

Parameter description	Unit	Limit (NOTE 1)		Applicable Frequencies
General	dB	$\max\{ -15-10\cdot\log_{10}(N_{lcrne}/L_{Clcrne}),$ $-18-5\cdot(\lvert\Delta_{lcrne}\rvert-1)/L_{Clcrne},$ $-57\ dBm/(3.75kHz\ or\ 15kHz)-P_{lcrne}\}$		Any non-allocated (NOTE 2)
IQ Image	dB	-25		Image frequencies (NOTES 2, 3)
Carrier leakage	dBc	-25	0 dBm ≤ Output power	Carrier frequency (NOTES 4, 5)
		-20	-30 dBm ≤ Output power ≤ 0 dBm	
		-10	-40 dBm ≤ Output power < -30 dBm	

NOTE 1: An in-band emissions combined limit is evaluated in each non-allocated tone. For each such tone, the minimum requirement is calculated as the higher of P_{lcrne} - 30 dB and the power sum of all limit values (General, IQ Image or Carrier leakage) that apply. P_{lcrne} is defined in NOTE 9.

NOTE 2: The measurement bandwidth is 1 tone and the limit is expressed as a ratio of measured power in one non-allocated tone to the measured average power per allocated tone, where the averaging is done across all allocated tones.

NOTE 3: The applicable frequencies for this limit are those that are enclosed in the reflection of the allocated bandwidth, based on symmetry with respect to the centre carrier frequency, but excluding any allocated tones.

NOTE 4: The measurement bandwidth is 1 tone and the limit is expressed as a ratio of measured power in one non-allocated tone to the measured total power in all allocated tones.

NOTE 5: The applicable frequencies for this limit are those that are enclosed in the tones containing the DC frequency if N_{lcrne} is odd, or in the two tones immediately adjacent to the DC frequency if N_{lcrne} is even, but excluding any allocated tone.

NOTE 6: L_{Clcrne} is the Transmission Bandwidth (tones).

NOTE 7: N_{lcrne} is the Transmission Bandwidth Configuration (tones).

NOTE 8: Δ_{lcrne} is the starting frequency offset between the allocated tone and the measured non-allocated tone. (e.g. $\Delta_{lcrne}=1$ or $\Delta_{lcrne}=-1$ for the first adjacent tone outside of the allocated bandwidth.

NOTE 9: P_{lcrne} is the transmitted power per 3.75 kHz or 15 kHz in allocated tones, measured in dBm.

Figure 3.8: In-band emission specifications from 3GPP [1].

3.2.4 Transmitter requirement summary

Specifications	Band	Frequency offset KHz	$\mathcal{L}(f_m)$ dBc/Hz
ACLR - GSM	N/E	110	-25.2
ACLR - UTRA	N/E	580	-26.8
Spurious emission	1	30000	-133
	2	30000	-133
	3	20000	-133
	5	10000	-110
		20000	-133
	8	10000	-133
	11	28000	-133
	12	18000	-133
	13	2000	-96
		21000	-133
	17	18000	-133
	18	12000	-123
		16000	-133
	19	27000	-133
	20	44000	-133
	21	37700	-133
	25	15000	-133
	26	10000	-133
	28	9000	-117
		10000	-115
		25000	-133
	31	5000	-133
		12500	-134
	66	150000	-133
	70	136000	-133
Out of band emissions	N/E	0	-41.8
	N/E	100	-72.8
	N/E	150	-75.8
	N/E	300	-96.8
	N/E	500 - 1700	-102.8
In-band emissions	N/E	0	-30

Table 3.2: Summary of phase noise requirement for transmitter concluded from figure 3.5, 3.6, 3.7 and 3.8 using equation 3.4, 3.5 and 3.6.

Figure 3.9 presents the non-normalized phase noise requirement from table 3.1 and 3.2 excluding the band specific requirement for the transmitter.

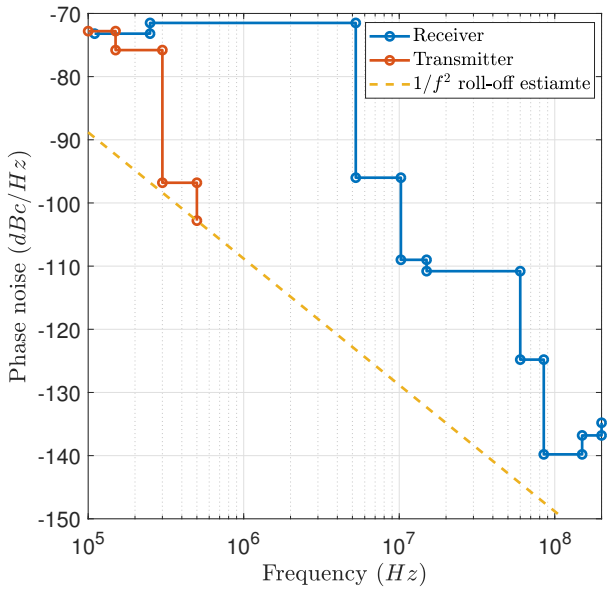


Figure 3.9: Non-normalized Phase noise requirement NB-IoT for blocker and transmitter by interpolating values from table 3.1 and 3.2. The dotted line presents the worst case $1/f^2$ roll-off estimate.

The operating frequency of the VCO is 2529.8 - 4538.1 MHz with a divider of two, four or eight depending on which band to be used. This divide ratio will reduce the noise requirement for the PLL corresponding to the divide ration, hence 6 dB for a divide ratio of two, 12 dB for a divide ratio of four and 18 dB for a divide ratio of eight. By altering the phase noise requirement correspondingly and by only including the bands from table 3.2 corresponding to the correct division ratio, an estimate for the phase noise of the PLL for each division ratio can be made (figure 3.10). As the requirement is stricter for the PLL when transmitting, focus will be on this scenario. From table 3.2, band 31 will set the requirement when the division ratio is eight, band 8 will set the requirement when the division ratio is 4 and band 25 will set the requirement when the division ratio is 2.

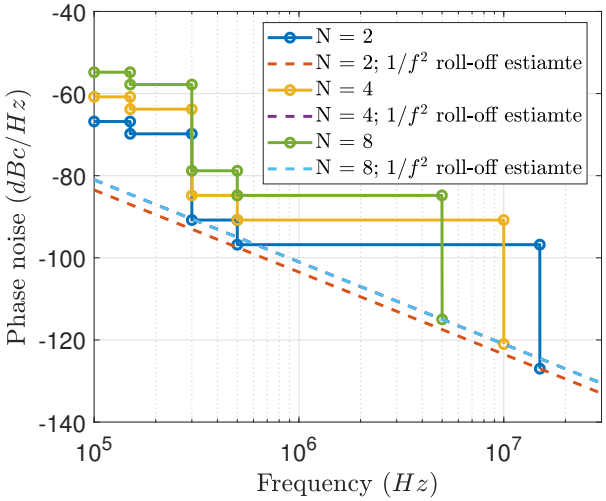


Figure 3.10: Phase noise requirement NB-IoT for the transmitter, normalized to division ratio. The dotted line presents the worst case $1/f^2$ roll-off estimate.

3.2.5 EVM

The error vector magnitude (EVM) is given by:

$$EVM = \sqrt{\frac{P_{error}}{P_{reference}}}, \tag{3.7}$$

where P_{error} is the average power in the error vector and $P_{reference}$ is the average power in the ideal reference vector.

Presumed that the contributing factors to the total EVM are uncorrelated, the total EVM of the transmission signal can be written as:

$$EVM_{total} = \sqrt{\sum_{n=1}^{k} EVM_n^2}, \tag{3.8}$$

where EVM_n denotes all the contributing sources. The contributing sources are due to imbalance in I and Q, nonlinearities, carrier leakage and phase noise [14]. The only parameter where the PLL performance is relevant in the degradation in the EVM is due to phase noise, hence focus will be on this parameter.

$$EVM_{rms} = \sqrt{\frac{1}{SNR} + 2 - 2 * e^{-\frac{\sigma^2}{2}}}, \tag{3.9}$$

where $SNR = \frac{E_s}{E_0}$ for the PLL and σ is the RMS LO phase error [6]. In [10] it is given that the rms phase error is

$$\phi_{rms}^2 = 2 * \int_0^{inf} 10^{\frac{\mathcal{L}(f)}{10}} df \tag{3.10}$$

By combining equation 3.9 and 3.10 and plotting EVM against integrated phase noise for different SNR, an estimate of how much the EVM will be degraded can be made.

In [2] another formula for calculating EVM is given:

$$EVM_{\%} = 100 * \frac{\pi}{180} * \sigma_{\phi(deg)}, \tag{3.11}$$

where $\sigma_{\phi(deg)}$ is given by equation 3.12.

$$\sigma_{\phi(deg)} = \frac{180}{\pi} * \sqrt{2 * \int_{x_2}^{x_1} 10^{\frac{\mathcal{L}(f)}{10}} df}, \tag{3.12}$$

where x_2 is set by how often the base station is sending out reference symbols and how the channel estimate is determined and x_1 is the channel bandwidth. For this work, x_2 will be set to 1 kHz and x_1 to 90 kHz.

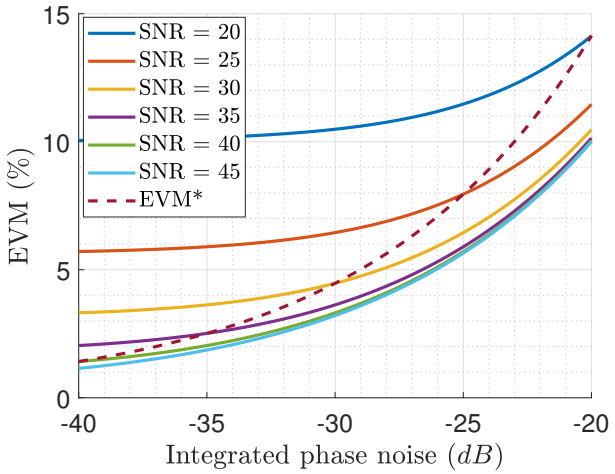


Figure 3.11: EVM as a function of integrated phase noise, where EVM* denotes equation 3.11.

The total EVM_{rms} for narrow band IoT is 17.5 %. However, the EVM degradation due to the PLL should be lower in order to relax the design of the PA where linearity can be traded for power efficiency. In consultation with Arm the allowed EVM contribution from the PLL was set to 5 % for the transmitter. When receiving,

the modulation scheme is QPSK (four symbols) and hence the EVM requirement can be further relaxed to 10 %.

$EVM_{\%}$	EVM_{dB}
17.5	-15.1
10	-20.0
5	-26.0

Table 3.3: Table presenting recalculation of $EVM_{\%}$ to EVM_{dB} single sideband.

Chapter 4

Parameterization PLL

4.1 Starting point

From figure 3.10 and table 3.2 it can be concluded that the frequency band that limits the phase noise is when transmitting on band 25, as the criterion points indicated for a 500 kHz and 300 kHz offset is due to "Out of band emissions" requirement; hence the approach to optimize the PLL will be for this scenario. The center frequency for band 25 when transmitting is 1882.5 MHz, making $f_{VCO} =$ 3765 MHz (due to the divide by two after the VCO).

4.2 Noise calculation

In order to ease the redesign of the PLL, all noise sources where parameterized and inserted into a MatLab script where they were used to approximate the total noise performance of the PLL. To do this, the transfer function for each block had to be accounted for. From figure 4.1 the transfer function for each noise source can be derived.

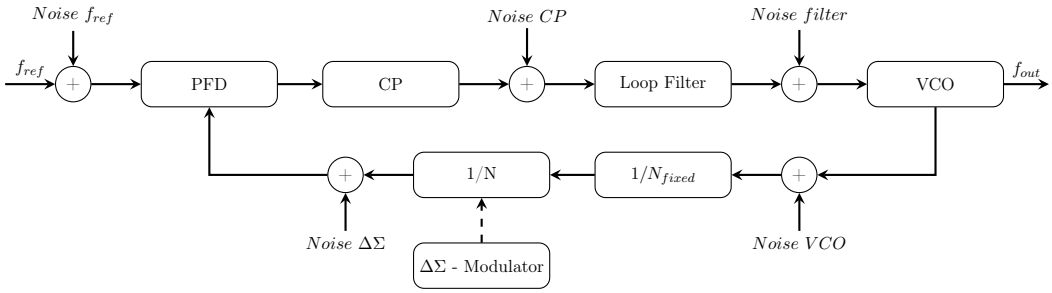


Figure 4.1: Flowchart for calculating noise transfer function for all PLL blocks.

$$H_{ol} = K_{PFD} * K_{CP} * K_{Loop\ Filter} * K_{VCO} * \frac{1}{N_{fixed}} * \frac{1}{N} = \frac{I_{cp}*K_{vco}*(s*R_1*(C_1+C_2)+1)}{(s^2*C_2*N*N_{fixed}*(s*C_1*R_1+1)*(s*C_3*R_2+1)} \tag{4.1}$$

$$H_{f_{ref}} = \frac{K_{PFD}*K_{CP}*K_{Loop\ Filter}*K_{VCO}}{1+H_{ol}} = \frac{I_{cp}*K_{vco}*N*N_{fixed}*(s*R_1*(C_1+C_2)+1)}{(s^2*C_2*N*N_{fixed}*(s*C_1*R_1+1)*(s*C_3*R_2+1)+I_{cp}*Kvco*(s*R_1*(C_1+C_2)+1))} \tag{4.2}$$

$$H_{CP} = \frac{K_{CP}*K_{Loop\ Filter}*K_{VCO}}{1+H_{ol}} = \frac{2*\pi*I_{cp}*K_{vco}*N*N_{fixed}*(s*R_1*(C_1+C_2)+1)}{(s^2*C_2*N*N_{fixed}*(s*C_1*R_1+1)*(s*C_3*R_2+1)+I_{cp}*K_{vco}*(s*R_1*(C_1+C_2)+1))} \tag{4.3}$$

$$H_{Loop\ Filter} = \frac{K_{Loop\ Filter}*K_{VCO}}{1+H_{ol}} = \frac{2*\pi*K_{vco}*N*N_{fixed}*(s*R_1*(C_1+C_2)+1)}{s^2*C_2*N*N_{fixed}*(s*C_1*R_1+1)*(s*C_3*R_2+1)+I_{cp}*Kvco*(s*R_1*(C_1+C_2)+1)} \tag{4.4}$$

$$H_{vco} = \frac{K_{VCO}}{1+H_{ol}} = \frac{s*2*\pi*C_2*K_{vco}*N*N_{fixed}*(s*C_1*R_1+1)*(s*C_3*R_2+1)}{s^2*C_2*N*N_{fixed}*(s*C_1*R_1+1)*(s*C_3*R_2+1)+Icp*K_{vco}*(s*R_1*(C_1+C_2)+1)} \tag{4.5}$$

$$H_{\Delta\Sigma} = \frac{K_{PFD}*K_{CP}*K_{Loop\ Filter}*K_{VCO}}{1+H_{ol}} = \frac{I_{cp}*K_{vco}*N*N_{fixed}*(s*R_1*(C_1+C_2)+1)}{(s^2*C_2*N*N_{fixed}*(s*C_1*R_1+1)*(s*C_3*R_2+1)+I_{cp}*Kvco*(s*R_1*(C_1+C_2)+1))} \tag{4.6}$$

4.2.1 Charge pump

The output of the CP is a current going through a filter, hence the noise source of interest is the current noise. The noise contribution can be divided in to two parts, one part from the flicker noise in the transistors and the second part is due to the thermal noise. The thermal noise is given by equation 2.4, where R is the total resistance in the CP given by $R = \frac{V_{dd}/2}{I_{Cp}}$. This thermal noise has to be multiplied by two in order to account for the noise in both "UP" and "DOWN" operation.

The flicker noise of the transistor is given by:

$$\overline{i^2_{1/f}} = K * \frac{I_D^a}{f} * \Delta f \tag{4.7}$$

where I_D is the drain bias current and K and a is process dependent fitting parameters [7]. In order to find the values of K and a, the current noise of the charge pump was simulated for different charge pump currents. The initial noise current for these curves (spot noise at 100 Hz) versus charge pump current where curve fitted as a power function using MatLab, resulting in $K = 0.02442$ and $a = 4.018$. By taking the sum of the thermal- and flicker- noise, the noise for different

currents could be validated by comparing the calculated values with simulations (figure 4.2).

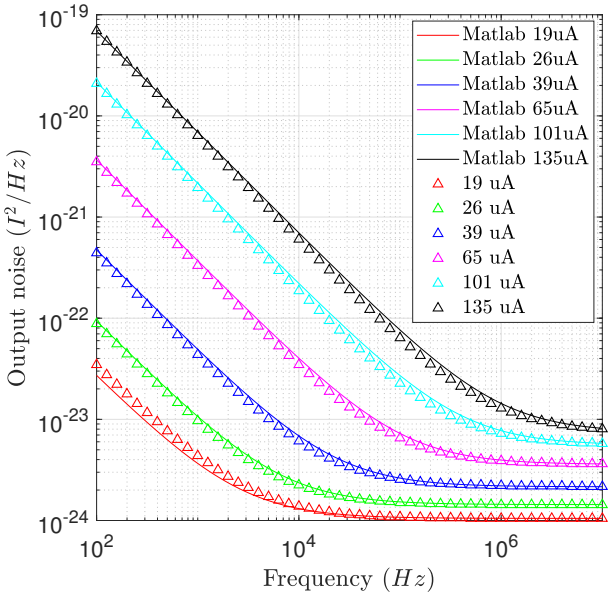


Figure 4.2: Output current noise from charge pump for different charge pump currents; "MatLab" is referring to equation 4.7 and Δ is simulated noise using Spectre.

The total noise from the charge pump has to be related to its duty cycle. In order to correct for this, a simulation to measure the *on time* had to be made, this time was then divided by the period time of f_{ref} (figure 4.3).

$$\alpha_{cp} = \frac{t_{on}}{t_{f_{ref}}} \tag{4.8}$$

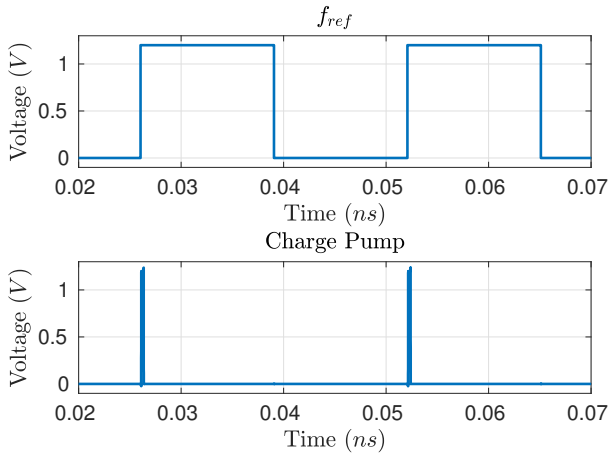


Figure 4.3: *On time* for CP in comparison to f_{ref} in order to calculate total noise.

The total noise from the CP is

$$\overline{i_{cp}^2} = \alpha_{cp} * (2 * 4 * k * T * \frac{1}{R} * \Delta f + K * \frac{I_D^a}{f} * \Delta f) \tag{4.9}$$

4.2.2 Filter

The noise contribution due to the filter presented in figure 2.7 can be approximated by transforming all the noise sources to the input as an *equivalent input noise source*. This input noise source is then transformed through the transfer function of the filter in order to get the noise at the output [25].

As the output of the filter is connected as a control voltage to the VCO, the noise source of interest from the filter in the analysis of the PLL is the voltage noise. The noise introduced by the passive components is given by equation 2.3. The Op-amp in the filter is constructed by a differential pair and a common source amplifier. The Op-amp will also generate noise but due to the gain in the differential pair, the noise of the common source will be suppressed.

$$\overline{v_{Th}^2} = 4 * k * T \frac{4}{3 * gm_{12}} * \left(1 + \sqrt{\frac{\mu_p * W/L_{34}}{\mu_n * W/L_{12}}}\right) * \Delta f \tag{4.10}$$

$$\overline{v_{1/f}^2} = \frac{2 * K_n}{s * W_{12} * L_{12} * C_{ox}} * \left(1 + \frac{K_p * \mu_p * L_{12}^2}{K_n * \mu_n * L_{34}^2}\right) \tag{4.11}$$

where gm_{12} is the transconductance of transistor M1 and M2 in figure 4.4, W is the width of the transistor, L is the length, K_n and K_p is flicker noise coefficients for n- and p-channel devices, μ_n and μ_p is the permeability for n- and p-channel devices and C_{ox} is the oxide capacitance. The differential pair is balanced, hence the W, L and gm are the same for transistor M1 and M2. Transistor M3 and M4 has also the same W, L and gm [9].

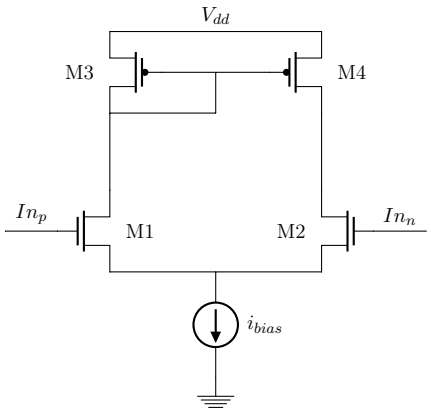


Figure 4.4

The voltage transfer function for the filter in figure 2.7 was first derived neglecting the output impedance of the OP-amp as

$$H_v = \frac{C_2*(s*C_1*R_1+1)}{C_2*(s*C_1*R_1+1)+C_3*(s*C_2*R_1+s*C_2*R_2*(C_1*R_1+1)+s*C_1*R_1+1)} \tag{4.12}$$

where C_1, C_2, R_1 and R_2 are from the active filter depicted in figure 2.7. Equation 4.12 was validated by disconnecting the OP-amp and plotting the output noise voltage for just the passive components (figure 4.5). It can be seen that the calculations correspond to the simulated values, however when the Op-amp was connected the calculations did not correspond to the simulated (figure 4.6).

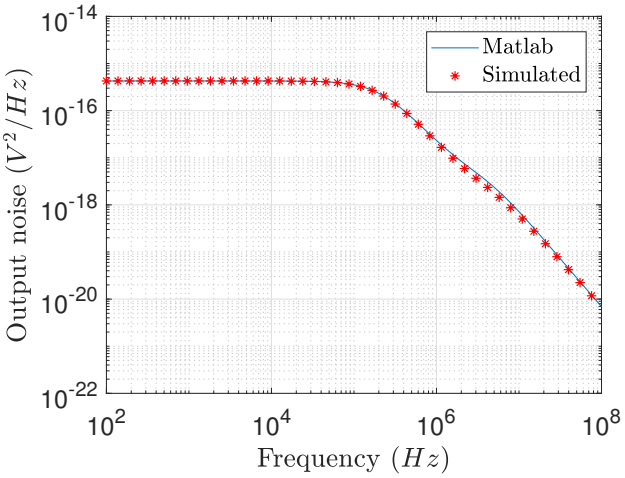


Figure 4.5: Validation of transfer function for noise for the passive components.

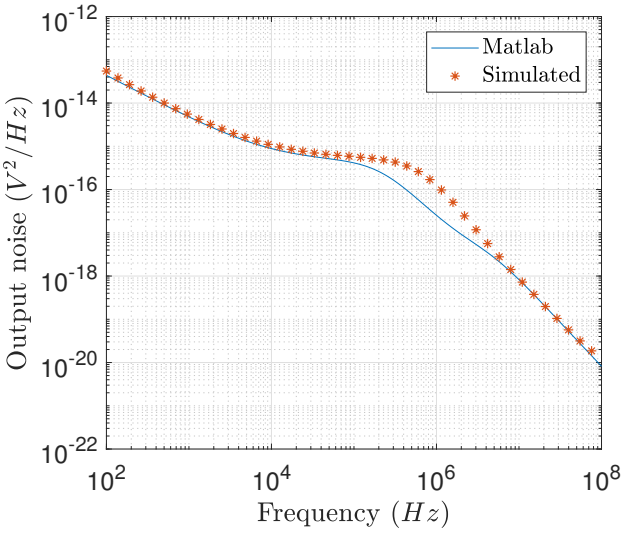


Figure 4.6: Validation of transfer function for noise for active filter without output impedance of OP-amp in the transfer function.

The transfer function was corrected for the output impedance of the OP-amp (equation 4.13) and validated (figure 4.7).

$$H_v = \frac{s*C_2*R_1+s*C_1*R_{op}*(s*C_1*R_1+1)+s*C_1*R_1+1}{s*C_3*R_{op}*(s*C_2*R_1+s*C_1*R_1+1)+(s*C_3*R_2+1)*(s*C_2*R_1+s*C_2*R_{op}*(s*C_1*R_1+1)+s*C_1*R_1+1)} \tag{4.13}$$

where R_{op} is the output impedance of the OP-amp.

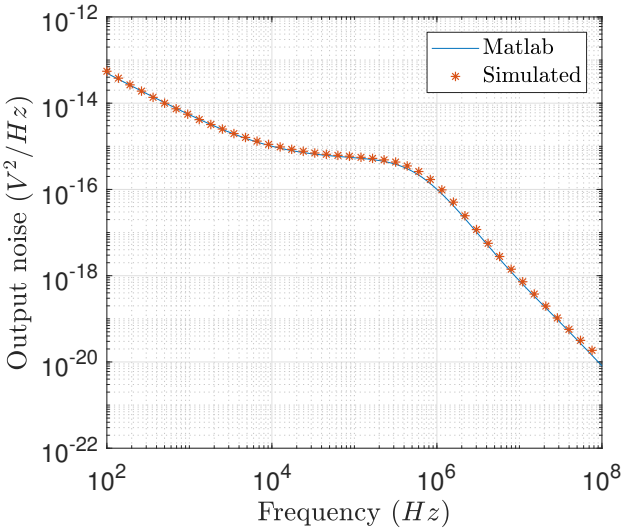


Figure 4.7: Validation of transfer function for noise for active filter, correcting for output impedance of OP-amp in the transfer function.

4.2.3 VCO

The phase noise of the VCO is not parameterized but is instead simulated for each design case.

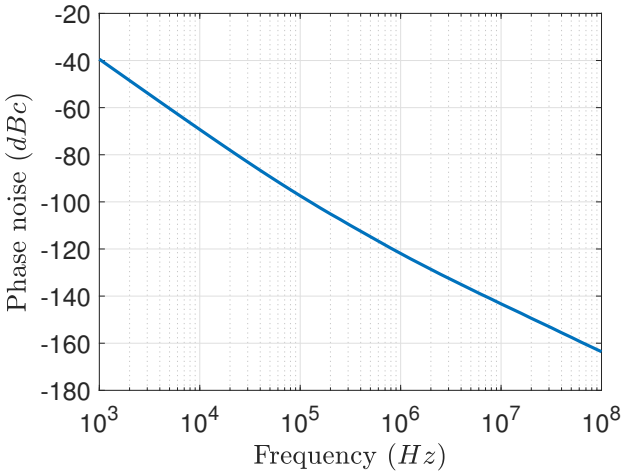


Figure 4.8: Phase noise from VCO when transmitting on band 25 (VCO frequency 3765 MHz)

4.2.4 ΔΣ Converter

The noise introduced by the ΔΣ converter was parameterized as suggested by [12].

$$\mathcal{L}(f) = 2 * \frac{(2*\pi)^2}{12 * F_{ref}} * 2 * sin\left(\frac{\pi * f}{F_{ref}}\right)^{2*(m-1)} * \left(\frac{N}{N_{fixed}}\right)^2 \tag{4.14}$$

where m is the order of the ΔΣ converter, F_{ref} is the reference frequency, N is the division ratio and N_{fixed} is the divider prior to the ΔΣ converter from figure 4.1.

4.2.5 XO

The XO specifications are Arm specific and are covered by a non-disclosure agreement. The reference frequency phase noise used for this work are made up values given by Arm typical for an XO and are presented in table 4.1.

Frequency Hz	Phase noise dB
100	-113
1 K	-131
10 K	-143
100 K	-153
1 M	-163
10 M	-165

Table 4.1: Table presenting made up phase noise values for the crystal oscillator given by Arm.

4.2.6 Total PLL noise

By multiplying the given noise with its corresponding transfer function in square and dividing by two (in order to get phase noise from amplitude and phase noise) the total output noise for each block can be calculated for the PLL.

Chapter 5

Pulling assessment

As presented in section 2.7, pulling of the VCO occurs when there is a signal with frequency close to the VCO frequency present. As the operating frequency of the VCO is twice of the transmitting frequency, second order harmonics from the PA might lead to pulling. The second order harmonics have to be investigated both on the primary and secondary side of the balun. As the PA is constructed using a differential topology, the second order harmonic on the secondary side of the balun should in theory be suppressed. In a real scenario, second order harmonics will be present due to mismatching in the PA and balun.

5.1 Pulling

In order to get a feel for the pulling effect for different bandwidths of the PLL, the pulling effect was calculated using equation 2.19 with i_2 set to 1 A. To calculate I_2, real I and Q data were used to generate A^2_{BB} and Θ_{BB}. The RMS value of $A^2_{BB}(t) * sin(2 * \theta_{BB}(t))$ was normalized prior to multiplying with the measured coupling from simulations. These measurements were measured at different distances between the balun and the VCO inductor to estimate the pulling effect with regards to distance (figure 5.1). By integrating the result of equation 2.19 from 2 Hz to the bandwidth of the envelope (90 KHz for NB-IoT) and combining equation 2.9 in 2.19 the EVM degradation due to frequency pulling of the VCO for different bandwidths could be made (figure 5.2). As this presents the pulling with a current of 1 A, the magnitude of the EVM degradation is not of interest, rather it is the characteristics of the EVM curve that is of interest.

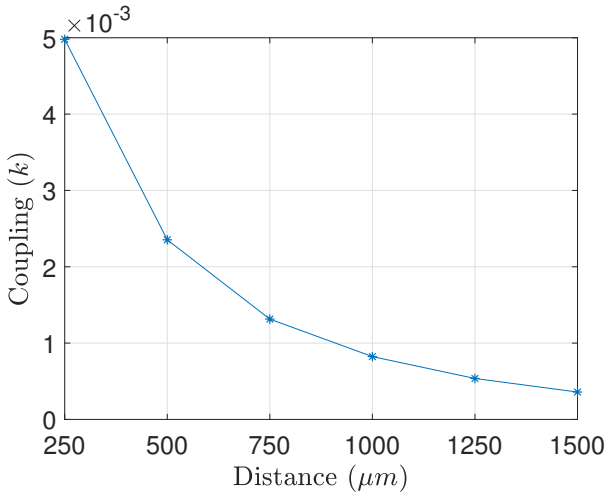


Figure 5.1: Coupling as a function of distance edge to edge between the PA transformer and the VCO inductor. Measured using the electromagnetic simulator EMX.

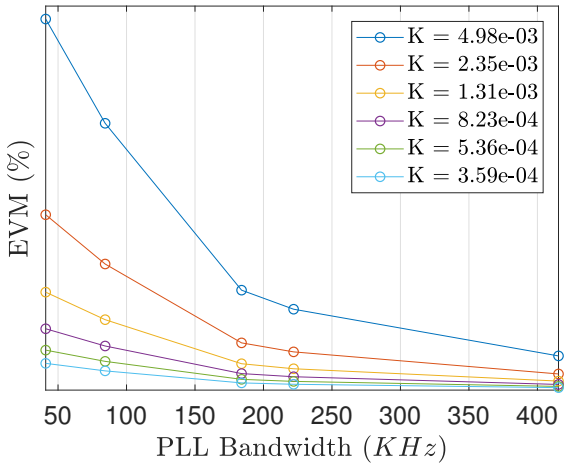


Figure 5.2: EVM degradation characteristics as a function of bandwidth due to pulling.

From the characteristics of the EVM curves presented in figure 5.2 it is evident that reducing the coupling in addition to increasing the bandwidth of the PLL limits the effect of pulling. As the slope of the EVM curve is highest for bandwidths lower than 180 KHz, the reduction of EVM impairment has highest impact when the bandwidth is set to at least 180 KHz (two times the base band frequency).

There are different approaches to mitigate the pulling; increasing the bias current of the VCO, increasing the Q of the VCO, increasing the bandwidth of the PLL and reducing the coupling between PA balun and VCO inductor. Increasing the bias current of the VCO is not an approach welcomed by Arm as it will increase the power consumption of the transceiver, in fact the power consumption should be reduced and hence the bias current will be kept at the lowest setting for the existing solution throughout this work.

5.2 Inductor design

As mentioned in section 5.1, one way of mitigating the pulling is to increase the bandwidth of the PLL. In order to do so, the phase noise has to be kept below the limits set by the NB-IoT requirement calculated in chapter 3. Different approaches can be made to reduce the phase noise, where one is optimizing the inductor size. The phase noise can also be reduced by increasing the Q of the RF-tank, this will also reduce the pulling. Another approach to reduce the pulling is to construct an inductor in such a way that the coupling is minimized. With these aspects in mind different inductors was constructed in order to increase Q or to reduce coupling, but also to reduce phase noise in order to be able to further increase the bandwidth of the PLL. As presented in chapter 3, the toughest requirement to be fulfilled is for $f_{VCO} = 3765\ MHz$ and hence the optimal inductor size was simulated according with the analysis proceeding equation 2.16 and 2.17 for this frequency (figure 5.3). The simulations were based on the lowest bias setting in the VCO (3.2 mA).

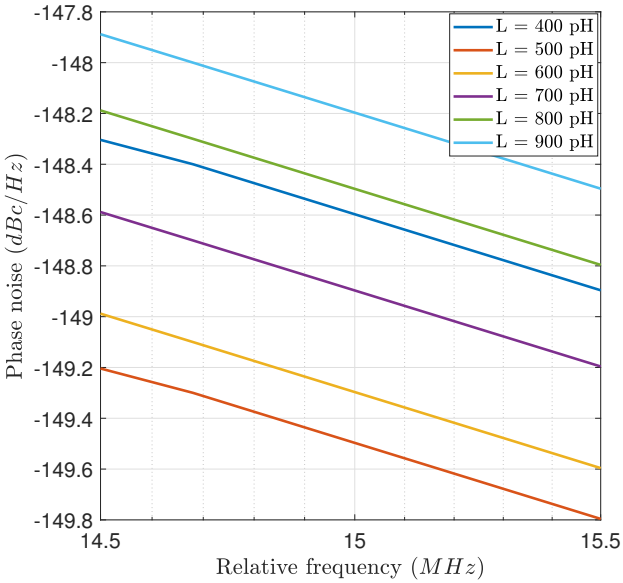


Figure 5.3: Phase noise versus inductor size at $f_{VCO} = 3765\ MHz$ at a relative frequency corresponding to band 25 with ideal capacitance.

From figure 5.3 it is evident that the best phase noise performance is when implementing the RF-tank in the VCO using an inductance of size 500 pH. The problem with reducing the size of the inductor is that the capacitance has to be reconfigured. Evaluating the size of the capacitance for a tuning range from 2.71 to 5.08 GHz for the original inductor (798 pH) compared to a 500 pH inductor:

$$\omega_0 = \frac{1}{\sqrt{LC}} => \omega_0 = \frac{1}{\sqrt{L * (C_{tank} + C_x)}} \tag{5.1}$$

where C_x is the capacitance in order to compensate for a smaller inductance and C_{tank} refers to the capacitance constituted by a digital controlled switched capacitance and a varactor.

$$L = 798\ pH\ @\ band\ 25;\ 3765MHz = \frac{1}{2\pi * \sqrt{798p * C_{tank}}} <=> C_{tank} = 2.24\ pF \tag{5.2}$$

Tuning range:

$$f_{min} = 2.71\ GHz => C_{tank} = 4.32\ pF \tag{5.3}$$

$$f_{max} = 5.08\ GHz => C_{tank} = 1.23\ pF \tag{5.4}$$

This implies that the digital controlled capacitance is 4.32 pF - 1.23 pF = 3.09 pF, assuming a constant capacitance not connected to the digital control logic of

1.23 pF.

$$L = 500\ pH\ @\ band\ 25;\ 3765MHz = \frac{1}{2\pi * \sqrt{500p * C_{tot}}} <=> C_{tot} = 3.57\ pF \tag{5.5}$$

$C_{tot} = C_{tank} + C_x, <=> C_x = 1.33p$ Tuning range:

$$f_{min} = 2.71\ GHz = \frac{1}{2\pi * \sqrt{500p * (C_{tank} + C_x)}} <=> C_{tank} = 5.57\ pF \tag{5.6}$$

$$f_{max} = 5.08\ GHz => C_{tank} = 0.63\ pF \tag{5.7}$$

This implies that the digital controlled capacitance is 5.57 pF - 0.63 pF = 4.94 pF, hence 4.94 $pF - 3.09\ pF = 1.85\ pF$ bigger in order to maintain the same tuning range. The constant capacitance in this case also has to be changed $C_x + 0.63\ pF = 1.96\ pF$, which is 0.73 pF larger than for the case with the original inductor. Due to the need of redesign of the the capacitance in the RF-tank if a smaller inductor is used, two design approaches were made; one with an inductor of the same size as the original and one with an inductor of 500 pH. Furthermore, the coupling between inductors will be dominated by the magnetic coupling below the resonance frequency [24]. By constructing an inductor as proposed by [11] and [16] in an eight fashion as in figure 5.4, the coupling can be reduced in the direction of the center of the inductor (indicated in figure).

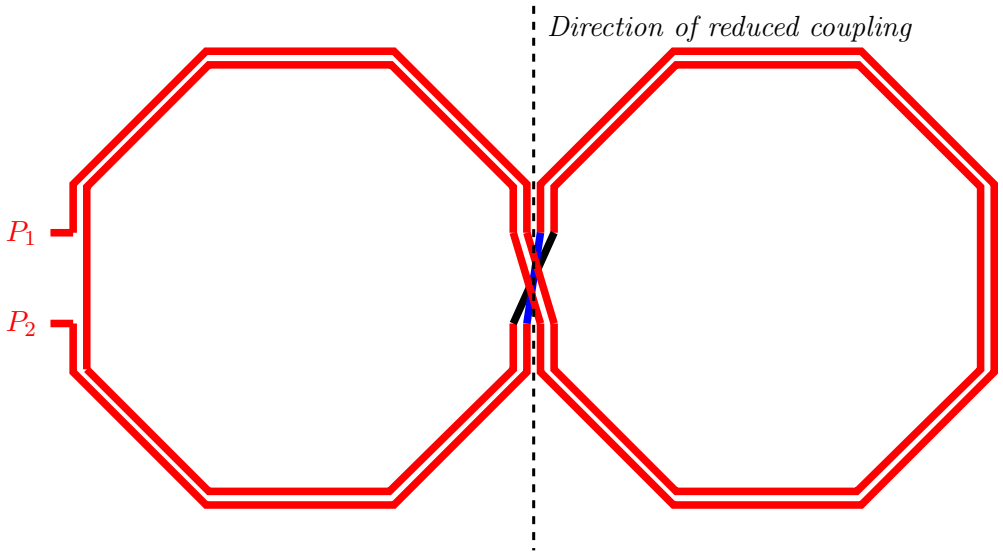


Figure 5.4: Sketch illustrating layout of eight shaped inductance with two windings.

Five different inductors were constructed and evaluated (table 5.1 and figure 5.5) where "Eight shape" refers to the shape of the inductor as presented in figure 5.4.

Design	L pH	Q_{ind}	Q_{VCO}	# Turns	Length μm	Height μm	# Cap
Original	798	15.8	9.9	2	164	145	84
Redesign 1	810	18.6	11.4	2	164	164	80
Redesign 2	670	17.2	10.5	2	145	145	118
Redesign 3	498	16.9	10.0	1	220	220	198
Eight shape 1	771	10.4	7.6	2	166	110	91
Eight shape 2	489	14.4	9.0	1	280	140	201

Table 5.1: Table presenting performance from different redesigns of the inductor in the VCO and corresponding digital control word for the capacitance to transmit on band 25.

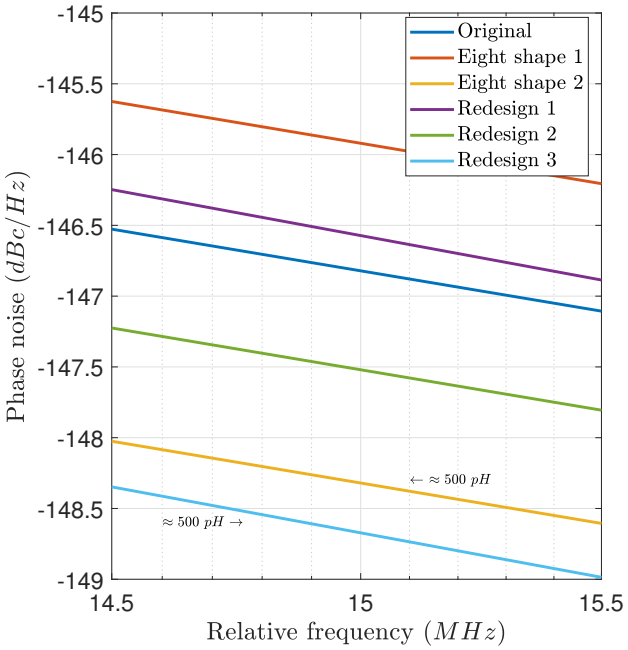


Figure 5.5: Phase noise for the VCO with $i_{bias} = 3.2$ mA at $f_{VCO} = 3765$ MHz measured at a relative frequency corresponding to the criterion set by band 25.

Looking into why the phase noise performance is reduced with the original inductor compared to using "Eight shape 2" even though the Q is higher for the original inductor, one can see that the shape of the current curve deviates from an ideal sinus curve when the original inductor is used. Increasing the bias current in the VCO is leading to higher deviation from an ideal sinus curve (figure 5.6). In figure 5.7 a DFT of the currents are presented. The frequency content for frequencies other than the center frequency for the original inductor is high, furthermore;

increasing the current does not improve the phase noise (figure 5.8). Observing these aspects, one can suspect that the transistors are current saturated when utilizing the original inductor for the bias current settings set by the original bias configuration.

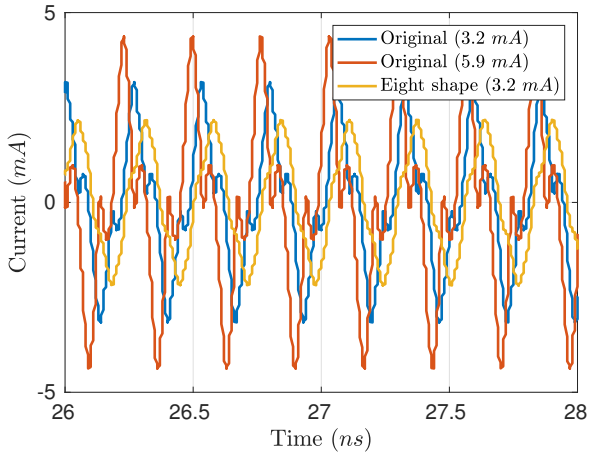


Figure 5.6: Current curves for the original inductor and the "Eight shaped 2" inductor.

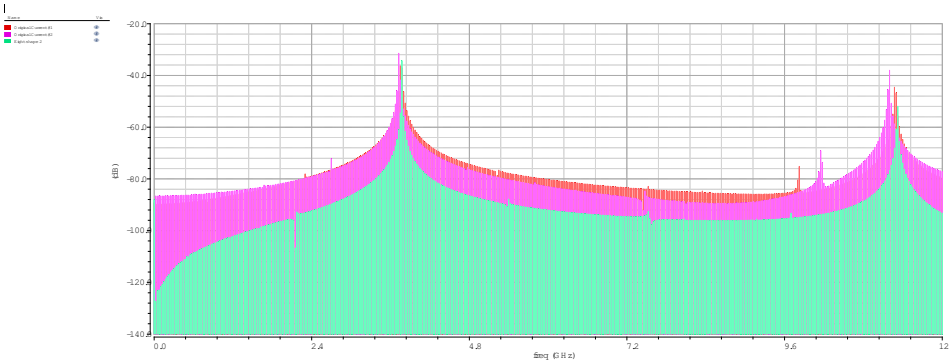


Figure 5.7: DFT of current curves from VCO where green is when using the "Eight shape 2" inductor with 3,2 mA bias current, orange is the original inductor with 3,2 mA bias current and pink is original inductor with 5.9 mA bias current.

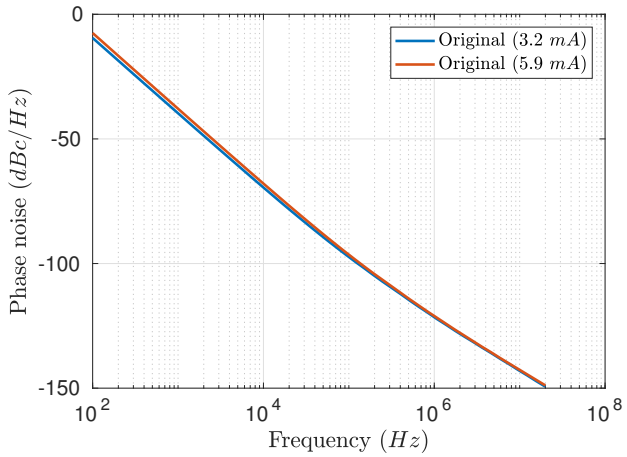


Figure 5.8: Phase noise for two different bias settings using the original inductor.

As the phase noise performance was improved when using an inductor of 500 pH, the capacitance had to be changed in accordance with discussion regarding equation 5.1 - 5.7. The tuning characteristics for the "Eight shape 2" inductor compared to the original is presented in figure 5.9.

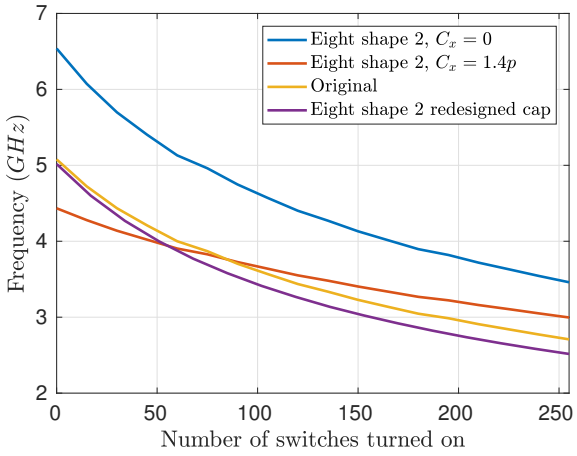


Figure 5.9: Tuning range for VCO with original inductor compared with Eight shape 2.

5.3 Balun design

As mentioned in section 5.1, the pulling can be reduced by reducing the coupling between PA balun and VCO inductor. This calls for a redesign of the balun in order to minimize this coupling without jeopardizing the performance of the PA.

In order to maximize the coupling in the balun (between primary and secondary side) and still be able to handle the high current generated in the PA, the balun was constructed as presented in figure 5.10. By doing this, the secondary winding constitutes of one conductor and the primary of two conductors. The width of the primary winding will be two times as wide as the two conductors are short circuited, giving it a higher robustness. By placing the secondary conductor between the primary conductors the coupling is increased. The lowest Z-layer up to and including top layer was used in order to increase robustness and coupling. Extensive theory regarding the PA is outside the scope of this thesis but it is worth mentioning that the load of the PA has to be kept low in order to deliver a high power and achieve a satisfying power added efficiency (PAE) [9]. As the load of the antenna is 50 Ohm, the antenna load has to be transformed to a lower value. The load of the PA is given by:

$$Z_{PA} = \frac{L_p}{L_s} * Z_L, \tag{5.8}$$

where Z_{PA} is the load seen by the PA, L_p is the inductance of the primary side of the transformer, L_s is the inductance of the secondary side of the transformer and Z_L is the load of the antenna. In order to keep the load low, the number of secondary turns will be kept to two times the primary turns.

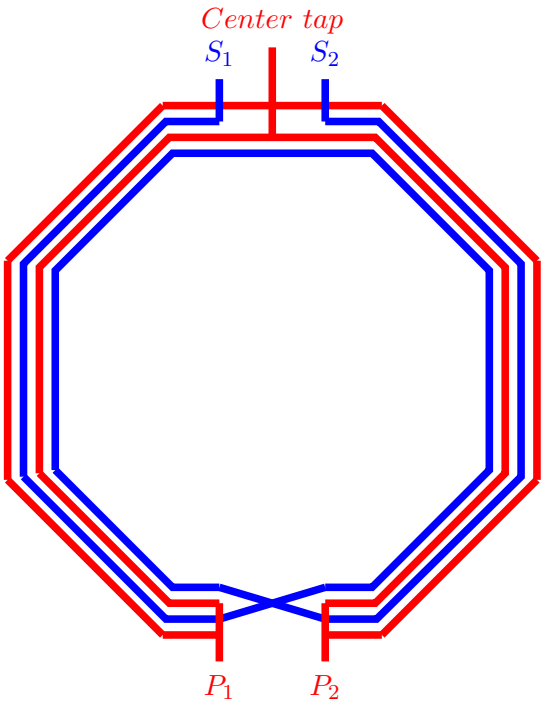


Figure 5.10: Sketch illustrating layout of balun.

The initial design of the balun was constructed using one turn on the primary side and two on the secondary (figure 5.10). Due to the differential topology, the second order current on the secondary side will be the difference between P_1 and P_2. In theory this current is zero but due to asymmetry, different load connected to S_1 and S_2 (in fact, one will be connected to the antenna and the other will be grounded) and mismatching in the PA some second order current can be expected on the secondary side. On the primary side, the current will be in phase at P_1 and P_2 and hence the current seen in far field will be the sum of the two. As this current is much higher than the current seen on the secondary side, focus will be on investigating the coupling from the primary side to a VCO inductor.

Evaluating the balun in figure 5.10, it is evident that the current will flow from P_1 and P_2 to *Center tap* generating a magnetic field. Increasing the number of windings to two will cancel this field as the current flowing back in the second winding will cancel the current flowing in the first (figure 5.11) making the current look like zero when the distance is larger than at least the width of two conductors in the balun. This balun was implemented overlooking the current flowing in the center tap generating a magnetic field, this called for another redesign of the balun in order to further reduce the coupling.

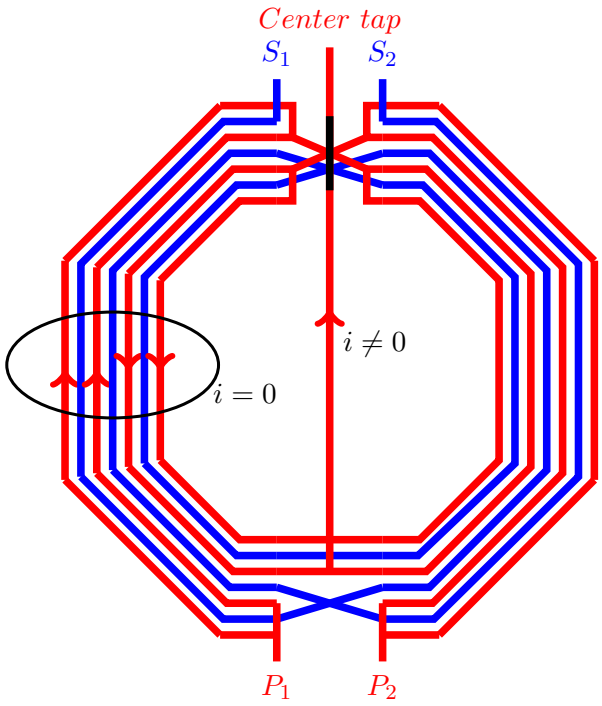


Figure 5.11: Sketch illustrating layout of redesign balun.

By changing the direction of the center tap in the topology presented in figure 5.10, the return path of the current flowing in the center tap will be opposite to the current flowing in the conductors from P_1 and P_2 (figure 5.12). This will further suppress the coupling from the balun to the VCO but the distance between the center tap to the conductors will lead to some magnetic field being generated. By adopting the idea of the topology with two windings (figure 5.11) and changing the direction of the center tap, the magnetic field generated by the balun could be further suppressed (figure 5.13).

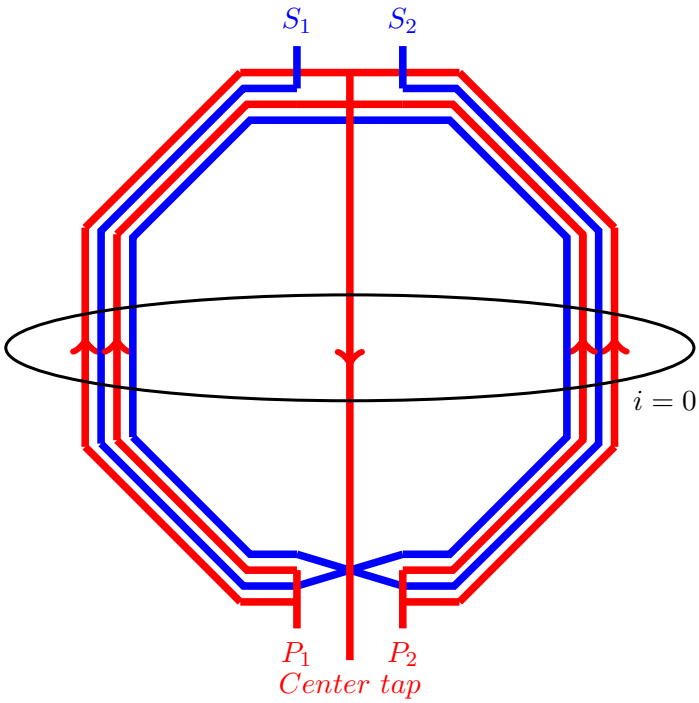


Figure 5.12: Sketch illustrating layout of balun with new center tap.

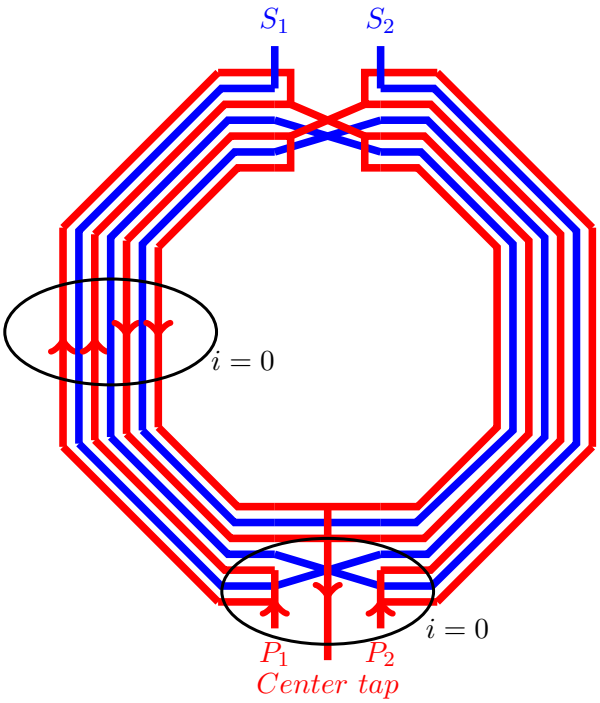


Figure 5.13: Sketch illustrating layout of balun with two windings and new center tap.

The coupling for all the baluns was simulated for different distances (edge to edge) and are presented in figure 5.14. It can be argued that simulating the coupling between the balun and the inductor with nothing in between is not a valid case as this is not true for the real chip. In order to get a better understanding for the coupling, a simulation was made with a dummy metal plate between the balun and the inductor. This metal plate filled the space between the inductor and the balun up to a distance of 20 μm to the edges.

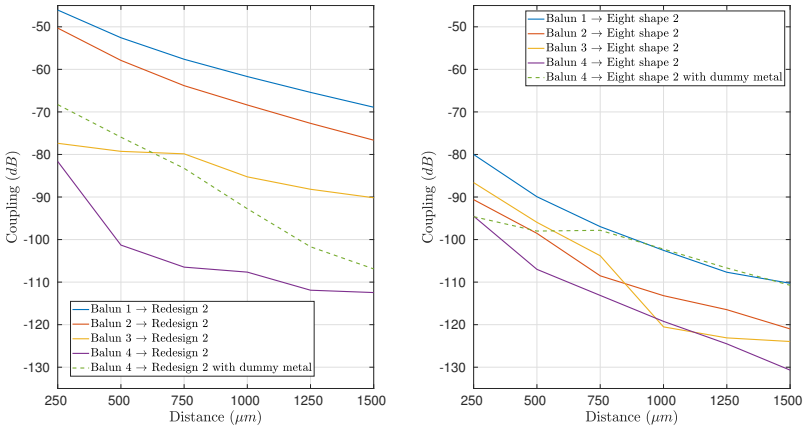


Figure 5.14: Coupling from the baluns to different inductors as a function of distance (edge to edge). The indexing of each balun is presented in table 5.2.

Balun	Figure	Insertion Loss @ 2 GHz *(dB)*
1	5.10	0.7345
2	5.11	0.8335
3	5.12	0.8663
4	5.13	0.8720

Table 5.2

5.4 Increasing PLL bandwidth

As discussed in section 5.1, the effect of the pulling is suppressed if the PLL bandwidth is high, especially when it is higher than two times the base band frequency. This section aims to increase the bandwidth as much as possible and still be able to fulfill the NB-IoT criterion. Figure 5.15 presents what effects to expect when increasing the PLL bandwidth. As one can see, a high bandwidth leads to low suppression of $\Delta\Sigma$ noise. To have a higher bandwidth then two times the base band frequency and still have some phase noise headroom a bandwidth of 220 KHz (figure 5.16) was a good trade of, Arm is requesting a 10 dB headroom. Having a slightly higher bandwidth than two times the base band frequency leaves room for reduced bandwidth due to temperature and process variations.

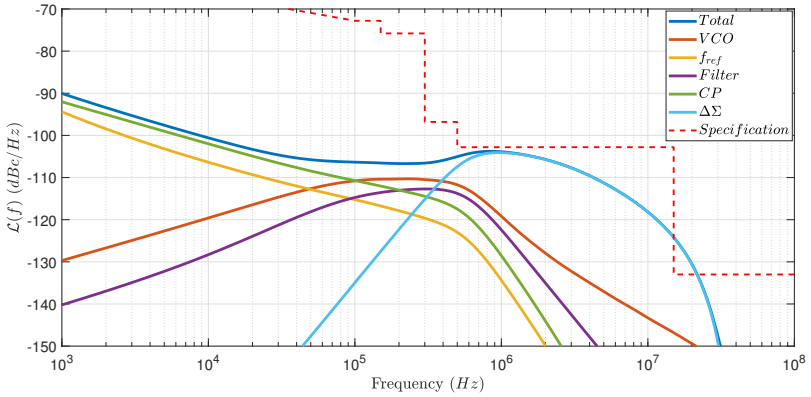


Figure 5.15: Bw = 400 KHz

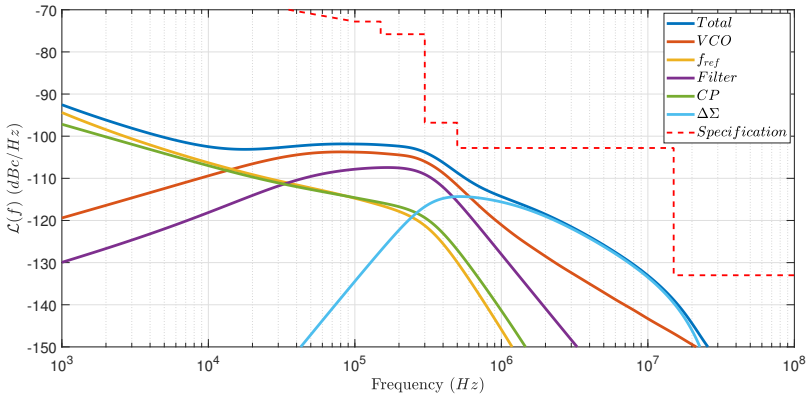


Figure 5.16: Bw = 220 KHz

By changing N_{fixed} from two to one, the resolution of the ΔΣ modulator is increased. This will reduce the phase noise from the ΔΣ modulator by 6 dB (figure 5.18). In order to validate this approach to increase the resolution, the performance of the divider had to be evaluated. This was done in the simulator and the results are presented in figure 5.17. By investigating the output from the divider, one can see that changing N_{fixed} to one is not jeopardizing the performance.

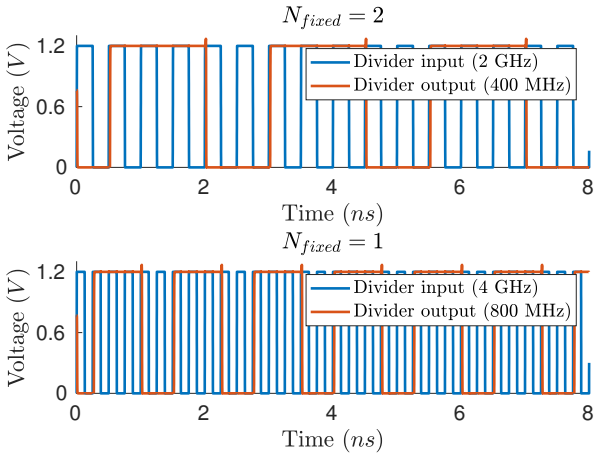


Figure 5.17: Validation of divider performance for $N_{fixed} = 1$.

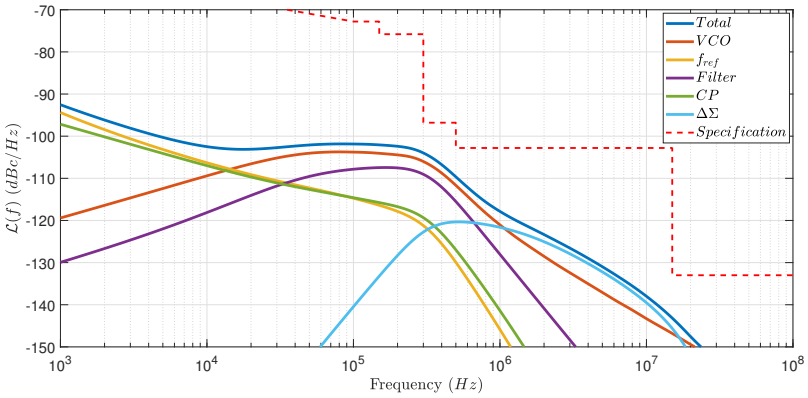


Figure 5.18: Bw = 220 KHz and $N_{fixed} = 1$.

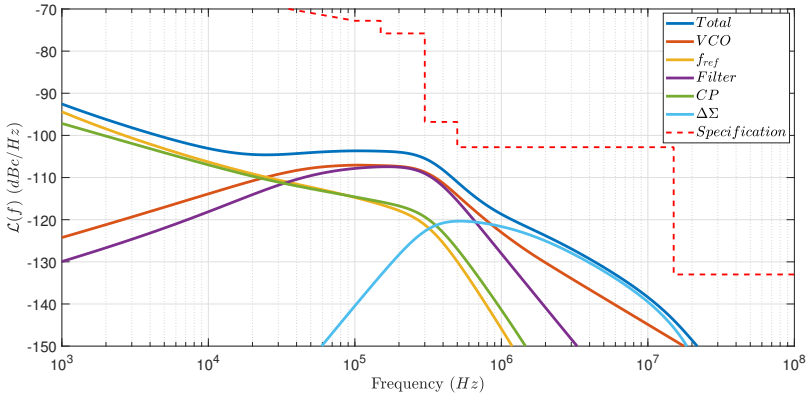


Figure 5.19: Bw = 220 KHz and $N_{fixed} = 1$ with eight shape 2 as inductor.

From equation 3.11 and 3.12, the EVM degradation due to the PLL phase noise is 0.3 %.

5.5 Pulling revisited

5.5.1 Setting up test bench for pulling analysis

To investigate the effects of frequency pulling of the VCO, a large signal time domain simulation was made. Using an S-parameter file generated by an electromagnetic simulator (EMX) for this case is not feasible as the S-parameter file has to be very detailed in order to get reliable results. Also, running the simulation with an S-parameter file will be extremely time consuming. To reduce the complexity of this simulation a schematic model of the balun was generated using EMX. In this model, coupling to the VCO inductor was generated with an "sp - simulation" to mimic the coupling measured using the N-port for the simulated coupling presented in figure 5.14. The VCO used in the test bench (TB) was the actual PLL VCO apart from the inductor, where an inductor from Cadence standard library "AnalogLib" with the same inductance and Q-value as the inductor intended for the test case was used. Two parallel circuits constituting of one capacitance, one resistance and one current source were connected to each side of the model of the balun. The capacitance and resistance are to mimic the impedance of the PA and was simulated with the PA in deep compression. The current source is the current going into the balun from the PA. Inspecting this current, one can detect a slight difference between the two sides of the PA. This common mode mismatch is due to asymmetries in the balun as well as one side of the secondary side being loaded with 50 Ω (antenna load) and the other being grounded. If the current in the TB would correspond to the current measured with the actual balun, this mismatch

would be accounted for twice as the asymmetry is included in the generated EMX model. In order to measure what current to set in the TB, another TB was set up with a balun constructed with Cadence Virtuoso standard library "AnalogLib" components with the same parameters as for the true balun. The current measured in this TB had no common mode mismatch and could be used in the TB for evaluating the effects of frequency pulling of the VCO.

To achieve a high resolution DFT, the offset of the VCO and the interferer has to be an integer multiple of the inverse of the simulation time. To ensure an integer multiple, the VCO was frequency locked. In order to attain an accurate approximation of the pulling effect for a free running VCO, the injected current to lock the VCO with was low but high enough to get the same voltage swing as for the VCO when free running. Also, the phase noise characteristics was investigated and an interfering offset was chosen to be higher than when the phase noise characteristics for the locked VCO is same as for the free running.

5.5.1.1 Pulling

Starting with the worst case; balun 1 as aggressor and redesign 2 as victim with a distance of 250 μm, one can detect from the characteristics of the DFT in figure 5.20 and the theory presented on frequency pulling of VCO (subsection 2.6.2) that the VCO is in "quasi lock". For ideal performance of the VCO, the voltage swing should be constant. Looking into the voltage characteristics for this case (figure 5.21), it is evident that the voltage swing is deteriorated. Without further investigation it can be concluded that the performance of the transceiver is ruined for this case due to the impairments of the VCO.

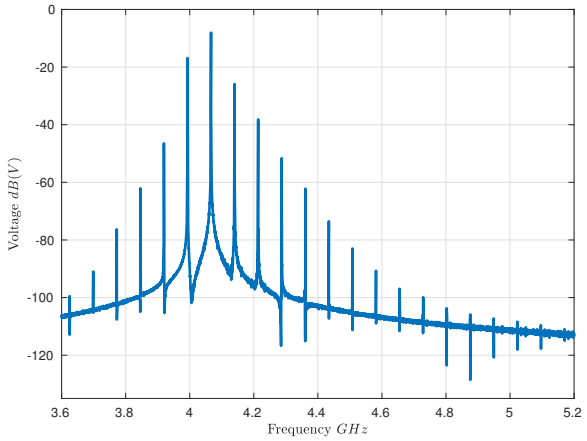


Figure 5.20: DFT of VCO output with balun 1 as aggressor and redesign 2 as victim with a distance of 250 μm

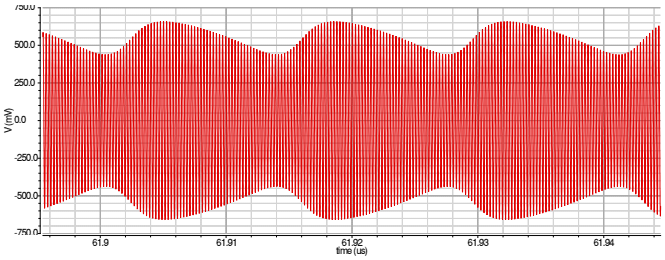


Figure 5.21: Voltage characteristic of VCO with balun 1 as aggressor and redesign 2 as victim with a distance of 250 μm

Looking into the performance with balun 4 as aggressor and redesign 2 as victim with a distance of 1000 μm with dummy metal, one can detect the sidebands at a 25 MHz offset from the VCO (5.23). These sidebands have to be recalculated to a frequency inside the frequency of the baseband using equation 2.18. From the frequency shifted sidebands, the relative magnitude of the sidebands can be calculated. Recalculating the sideband to 90 KHz using equation 2.18, the relative magnitude will be -4.5 dB. The effect of pulling for the closed loop PLL can then be calculated through the closed loop transfer function of the pulling $\frac{1}{1+H_{ol}}$ [3], presented in figure 5.22. The suppression of the pulling when the bandwidth is 220 KHz is -7.6 dB, this results in a relative harmonic of -12.1 dBc. One can argue that this interferer is not well outside the frequency locking range and hence equation 2.18 is not valid. Regardless whether or not equation 2.18 hold, the performance is ruined for this case. Looking at table 3.3 one can see that -12.1 dB would validate the EVM criterion; if the equation does not hold the VCO is most likely in a quasi lock or frequency locked state.

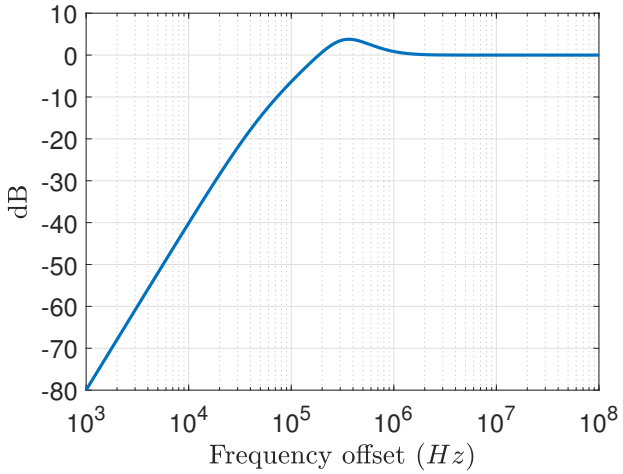


Figure 5.22: Transfer function for the frequency pulling injected into the VCO, Bw = 220 KHz.

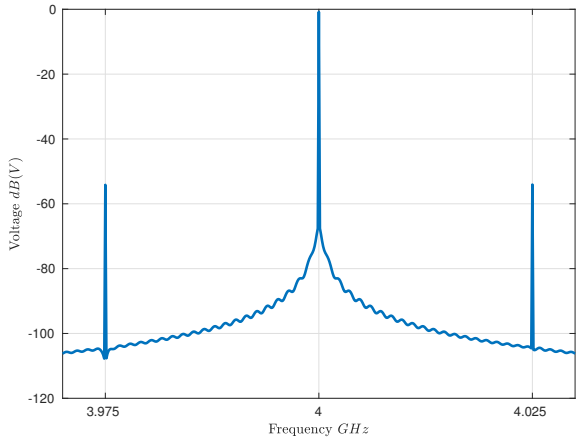


Figure 5.23: DFT of VCO output with balun 4 as aggressor and redesign 2 as victim with a distance of 1000 μm and dummy metal

With balun 4 as aggressor and eight shape 2 as victim with a distance of 1000 μm with dummy metal, the effect of pulling is below the noise floor in the DFT (figure 5.24). The maximum possible magnitude of the sideband is hence -125 dB (the level of the noise floor), recalculating this in accordance with equation 2.18 results in a relative sideband of -75.3 dB at a 90 KHz offset to the VCO frequency. After taking the suppression of the PLL into account, the relative harmonic is -82.9 dBc. From table 3.3 one can see that this is well inside the EVM criterion.

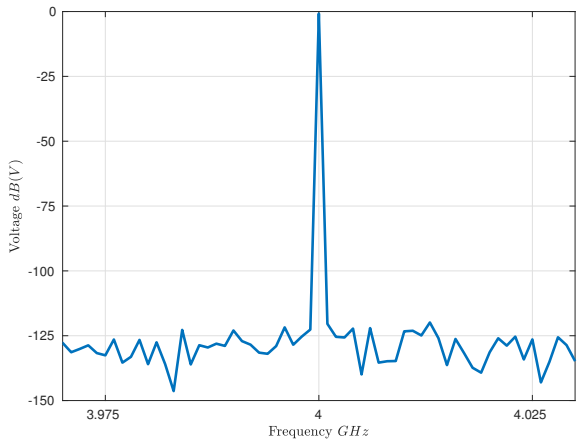


Figure 5.24: DFT of VCO output with balun 4 as aggressor and eight shape 2 as victim with a distance of 1000 μm and dummy metal

Looking at the characteristics of the transfer function presented in figure 5.22, it can be found that the suppression corresponds to a $1/f^2$ slope. The magnitude of the relative sidebands due to pulling (equation 2.18) increases with $1/f$, hence the worst case for pulling is when the frequency offset is maximized as shown in figure 5.25. The bandwidth of the baseband signal for NB-IoT is 90 KHz; as the second order harmonic is the interfering signal, the maximum offset will be two times the baseband signal.

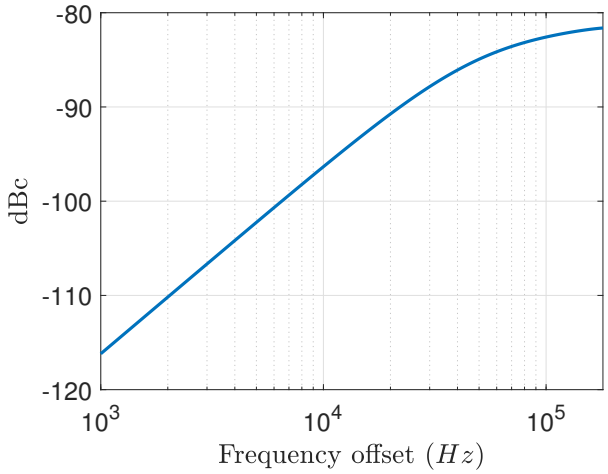


Figure 5.25: Magnitude of PLL sidebands due to pulling as a function of frequency offset with balun 4 as aggressor and eight shape 2 as victim with a distance of 1000 μm and dummy metal and a PLL bandwidth of 220 KHz.

Chapter 6

Conclusion

This thesis has presented a working solution for the PLL with an integrated PA. This has been done through design aspects for how to mitigate coupling between the PA balun and the VCO inductor and how to increase the bandwidth of the PLL without violating the NB-IoT requirement set by 3GPP. Furthermore the phase noise performance of the VCO has been increased and the critical operation band for the transceiver has been identified.

Looking at the thesis objectives (Section 1.2), the purpose of this thesis is fulfilled.

6.1 Future work

- Changing the PA from a linear architecture to a switched architecture changes the demand on the PLL. A future task could be to prepare the PLL for a transaction to a switched architecture.
- The requirement for receiving is much more relaxed than for transmitting, also the PA is not causing any pulling when receiving. This calls for an investigation if the transceiver can be run in a low power mode when receiving in order to save battery lifetime.
- Different PLL architectures with a different divide number following the PLL could be evaluated to mitigate the pulling from the PA.
- Looking into the charge pump and loop filter; the charge pump could be redesigned in order to enable the usage of a passive loop filter.
- Evaluate the worst allowed performance for the XO in order reduce cost and power consumption.
- Manufacture and measure the performance of the circuit.

Bibliography

[1] ETSI 3^{rd} Generation Partnership Project (3GPP). *LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception (3GPP TS 36.101 version 14.6.0 Release 14)*. Tech. rep. ETSI 3^{rd} Generation Partnership Project (3GPP), Jan. 2018.

[2] Dean Banerjee. *PLL performance, simulation and design*. English. OCLC: 1010941535. 2006. ISBN: 978-1-59858-134-8.

[3] Imran Bashir et al. "A Novel Approach for Mitigation of RF Oscillator Pulling in a Polar Transmitter". In: *IEEE Journal of Solid-State Circuits* 46.2 (Feb. 2011), pp. 403–415.

[4] J. Craninckx and M. Steyaert. *Wireless CMOS Frequency Synthesizer Design*. Kluwer Academic Publisher, 1998. ISBN: 0-7923-8138-6.

[5] William F. Egan. *Frequency Synthesis by Phase Lock Second Edition*. John Wiley and Sons, 2000. ISBN: 0-471-32104-4.

[6] A. Georgiadis. "Gain, Phase Imbalance, and Phase Noise Effects on Error Vector Magnitude". en. In: *IEEE Transactions on Vehicular Technology* 53.2 (Mar. 2004), pp. 443–449.

[7] Paul R. Gray, ed. *Analysis and design of analog integrated circuits*. eng. 5. ed., internat. student version. OCLC: 845993461. Hoboken, NJ: Wiley, 2010. ISBN: 978-0-470-39877-7.

[8] Alan Hastings. *The art of analog layout*. eng. 2. ed., Pearson internat. ed. Upper Saddle River, NJ: Pearson, Prentice Hall, 2006. ISBN: 978-0-13-129329-8.

[9] Thomas H.Lee. *The Design of CMOS Radio-Frequency Integrated Circuits Second Edition*. Cambridge University Press, 2017. ISBN: 978-0-521-61389-7.

[10] Mohammed Ismail and Delia Rodríguez de Llera González. *Radio design in nanometer technologies*. English. OCLC: 209939597. Dor-

drecht, the Netherlands: Springer, 2006. ISBN: 978-1-4020-4824-1 978-1-4020-4823-4 978-1-280-93567-1.

[11] Peter Martin, Richard Horn, and Kobi Ben Atar. "A multi-turn twisted inductor for on-chip cross-talk reduction". In: IEEE, Nov. 2016, pp. 1–5.

[12] B. Miller and B. Conley. "A multiple modulator fractional divider". In: IEEE, 1990, pp. 559–568.

[13] Ahmad Mirzaei and Hooman Darabi. "Pulling Mitigation in Wireless Transmitters". In: *IEEE Journal of Solid-State Circuits* 49.9 (Sept. 2014), pp. 1958–1970.

[14] Abbas Mohammadi and Fadhel M. Ghannouchi. *RF transceiver design for MIMO wireless communications*. Lecture notes in electrical engineering volume 145. New York: Springer, 2012. ISBN: 978-3-642-27634-7.

[15] Marc Molina et al. "Effect of high frequency substrate noise on LC-VCOs". In: IEEE, Aug. 2010, pp. 157–160.

[16] Nathan M. Neihart et al. "Twisted transformers for low coupling RF and mixed signal applications". In: IEEE, May 2009, pp. 429–432.

[17] H. Nyquist. "Thermal Agitation of Electric Charge in Conductors". In: *Phys. Rev.* 32 (1 July 1928), pp. 110–113.

[18] David M. Pozar. *Microwave engineering*. 3rd ed. Hoboken, NJ: J. Wiley, 2005. ISBN: 978-0-471-44878-5.

[19] Behzad Razavi. "A study of injection locking and pulling in oscillators". In: *IEEE Journal of Solid-State Circuits* 39.9 (2004), pp. 1415–1424.

[20] John Rogers and Calvin Plett. *Radio frequency integrated circuit design*. 2nd ed. Boston: Artech House, 2010. ISBN: 978-1-60783-979-8.

[21] Richard Schreier and Gabor C. Temes. *Understanding Delta-Sigma Data Converters*. John Wiley and Sons, 1998. ISBN: 0-471-46585-2.

[22] H.L. Stover. "Theoretical explanation for the output spectra of unlocked driven oscillators". In: *Proceedings of the IEEE* 54.2 (1966), pp. 310–311.

[23] T.A. Kwasniewski T.A.D. Riley M.A. Copeland. "Delta-sigma modulation in fractional-N frequency synthesis". In: *IEEE Journal of Solid-State Circuits* 28.5 (1993), pp. 553–559.

[24] F. Vecchi et al. "A simple and complete circuit model for the coupling between symmetrical spiral inductors in silicon RF-ICs". In: IEEE, June 2008, pp. 479–482.

[25] C. J. Verhoeven, ed. *Structured electronic design: negative-feedback amplifiers*. Boston: Kluwer Academic Publishers, 2003. ISBN: 978-1-4020-7590-2.