Ethernet Bypass Switch

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Abstract

An ASIC solution is studied and designed to solve a possible communication interruption due to power failures of automation servers connected in serial topologies.This installation method is widely employed in industrial Ethernet networks. However, it presents a disadvantage, a failure in a network's node isolates the following nodes until maintenance repairs it. The solution studied during this thesis bypasses the damaged node allowing the communication between the rest of the chain.

The circuit proposed consists on CMOS switches powered up by harvesting energy from the Ethernet communication lines. An analysis of the transmission data signals was conducted in order to model the application environment and determine the requirements for the project. Simulations were performed with schematics and layout in order to verify the concept. A solution based on an ASIC was proven to be feasible.

This research was conducted in collaboration with Schneider Electric.

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Popular Science Summary

Automation servers are tools that execute a plurality of tasks, more precisely in the task management domain. Being automated means this process does not require human intervention to function[1].

These units communicate through Ethernet data signals. Ethernet is the most popular way for a local area network (LAN) or wide area network (WAN) to connect to devices and servers that require a connection to the INTERNET[2].

The data signals follow the Ethernet protocol, which presents distinct characteristics on transmission methods, such as speed, amplitude voltage and signal encoding.

One of the most used installation methods for the automation servers is the star topology. It consists on having every server directly connected to the central hub. In this manner, the central hub can communicate directly to the desired device, without passing through intermediates. However, it requires an important amount of cabling to be placed. In order to reduce costs, industrial applications employ a different topology.

The common practice in automation buildings is to implement these servers in a daisy chain topology. This means that they are all connected in series, being placed one after the other and only physically connected to a directly preceding or following device.

The installation method mentioned above results in a possible communication break in case one of the servers in the network chain malfunctions. This is attributed to the fact that if one node in the chain is inoperable, the data signals experience a blockage, compromising the communication between the network hub and the servers.

The goal of this project is to propose a solution able to maintain the link path between units even if one of them fails. To achieve this, research on the Ethernet standard specifications has to be performed in order to determine the requirements that need to be met.

These requirements were defined based on research and experiments conducted at Schneider Electric, using an already existing device as a reference automation server.

The proposed solution consists on an integrated circuit which function is to isolate the damaged node and operate as a bridge between the input and output signals traversing this point.

We wish to present a chip able to extract energy directly from the communication wires, therefore not requiring any external power sources. This approach involves more research since energy harvesting from communication lines is not a subject that has been broadly explored, even in the Academic domain. A complete view of the design schematics can be found in figure A.2 in the Appendix section.

The nature of the Ethernet transmission signals and the different modes of operation also impose some extra issues regarding the performance of the integrated circuit proposed here. For instance, when the system is powered on during the first installation, if a unit is found to be in failure mode, the default set up of the server would not provide strong signals for the IC to become active and bypass the signals. Issues such as this one are also addressed in this thesis.

Abbreviations

AC	Alternating Current
ADE	Analog Design Environment
ASIC	Application-Specific Integrated Circuit
CMOS	Complementary Metal–Oxide–Semiconductor
DC	Direct Current
EMI	Electromagnetic Interference
FLP	Fast Link Pulse
GND	Ground
JFET	Junction Field-Effect Transistor
LTP	Link Test Pulse
MLT-3	Multilevel Signal - Three Levels
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NLP	Normal Link Pulse
NMOS	N-type Metal-Oxide-Semiconductor
NRZI	Non-Return-To-Zero/Inverted
PHY	Physical layer
PMOS	P-type Metal-Oxide-Semiconductor
SMT	Surface-Mount Technology
USB	Universal Serial Bus

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Chapter 1

Introduction

Ethernet is one of the most widely used forms of communication protocols in the field of automation, being the most successful LAN technology in history[3]. The automation servers are divided into branches when a considerable amount of these devices needs to be connected to a network. The units in each branch are connected to an Ethernet switch hub using a wire for each of them, forming a star topology. This configuration requires an extensive use of wiring. In order to reduce this amount, the devices in each branch could be connected in series, which is called daisy chain topology. However, this configuration has a limitation. When one of the units fails, the communication in the whole branch is compromised.

There are two approaches currently on the market in order to solve the communication cut. One of the options is to use relays between the two Ethernet wires going in and out of the units. Although it is a practical solution, it is not area effective and it might present mechanical deterioration in very low switching frequency. Another solution would be to use a ring topology, which provides an extra communication path but also requires extra wire lines and an advanced switch to control the direction of the communication flow.

This thesis will study the viability of another solution to the matter in the form of an application-specific integrated circuit while maintaining the serial topology.

1.1 Thesis' aim

The main goal of this master thesis is to prove the concept of a possible solution to cope with the problem mentioned previously. It will consist on a solid state Ethernet bypass switch that will be powered by harvesting energy from the Ethernet cables. The device will act as a closed switch in case of a power failure of one of the composing units of the system. Figure 1.1 shows the configuration of the switches in normal operation from the unit's perspective. In case of failure, switches S1 and S2 will close and the remaining will open. This action will physically disconnect the damaged unit from the network.

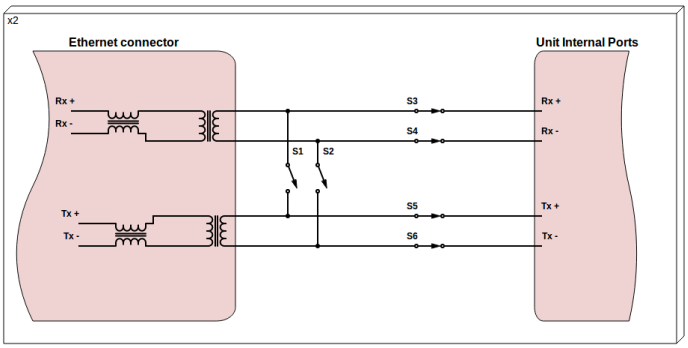

Figure 1.1: Ethernet Bypass Switch Operation.

For future reference, if the automation server is in working mode, the bypass switch is open. On the other hand, if the unit is in power failure, in other words in bypassing mode, then the bypass switches are closed.

In addition to the design of the solid state switches themselves, a solution for harvesting energy from the Ethernet communication lines will be investigated and implemented.

The procedure chosen is to split the concept's study process into two steps. A primary investigation from a practical point of view is needed to prove such a topology can be achieved, confirming the validity of the bypass switch solution. Once the concept is proven, we need to demonstrate that an ASIC can fulfill the established performance specifications. In other words, the current architecture of the automation devices connected through the Ethernet cables, as well as the cables themselves, need to be analyzed in order to determine the requirements and limitations of the circuit to be designed.

This project does not demand a physical chip since fabrication would only be carried out if the thesis is successful, in other words the claim is to test the concept and provide a structure ready to be manufactured. Thus, what we wish to deliver are the schematic and layout designs, measurements from the discrete test bench to describe the communication lines environment and the circuit simulation results.

1.2 Method

This study will be mainly structured in three parts. At first, a literature study will be performed. The focus of this research is to get acquainted with the system, the technology being used by the company and the requirements that need to be respected when designing the circuit.

The next step is to explore further the requirements and limitations for this solution by conducting a series of experiments and the creation of a test board with discrete components. Below there is a list of some of the questions that will be addressed:

- Would it be an issue to connect transformers back to back?
- What is the maximum acceptable resistance value of the switches?
- How many failed units in series are tolerable?
- What are the protection requirements for the circuit?
- Determine the best conditions for harvesting energy.
- How much power can we harvested before affecting the communication?
- Is a start up power needed?
- How much power is needed for the operation of the circuit?

Once the proposed prototype has been approved, the design of the ASIC can be implemented. This step will be performed at *Virtuoso Analog Design Environment* from Cadence Design Systems.

The circuit will be designed using a 65 nm process technology.

1.3 Scientific Background

Some of the key concepts mentioned previously are described in this section.

1.3.1 Energy Harvesting

Energy harvesting devices convert the available energy from the ambient to be used in low power electronic systems. This technology eliminates the need of batteries or another energy storing devices, providing autonomy to the system. The source of energy can be vibrations, temperature gradients, electromagnetic radiation, among other sources[4]. Clearly, this process can be achieved through many means, so we can infer that a lot of research has been done in this domain.

1.3.2 Energy Harvesting Using Communication Lines

A special interest for this thesis is the research done in energy harvesting from human made environments. Energy can be harvested from communications: both wireless [5] and wired[6].

In contrast to the previous section, this specific approach has not been explored in depth, which means there is not a lot of research papers or documents exploring this method.

1.3.3 Low Power Analog ASIC Design and Process

Ultra low power design is a demand for energy harvesting devices, which is why this is a requirement for this work[7].

Power reduction in the analog domain is not achieved in the same manner as in the digital domain. Noise and linearity are some of the analog requirements which limit the reduction of supply levels for instance. In this case, power is usually trade-off for speed or resolution. There are other techniques depending on the

application of the circuit, such as sub-threshold operation or transferring some of the blocks from the analog to the digital domain[8][9].

1.3.4 Prior Art on Ethernet Bypass Solutions

All prior Ethernet bypass solutions found are based on the use of relays[10][11]. A relay is an electromechanical device that reacts to a change in electrical current. It is inactive when powered off (unit still operational), but when powered on (unit in power failure mode), the relay closes. Thus it removes the local malfunction from the critical network connecting the input to the output cable, skipping the damaged unit.

1.3.5 Transformers

A transformer is a passive electrical device used to transfer energy between circuits through electromagnetic induction, based on the principle of Faraday's law of induction. In other words, a varying current in one coil of the transformer produces a varying magnetic field, which in turn induces a voltage in a second coil.

These devices are the connecting points between the units. It provides isolation from the input wires, protecting the system[12].

1.3.6 Ethernet Transmission Link

The circuit in question should be compatible with two types of media systems, 10 and 100 MBit/s, over twisted-pair cables. Their identifiers are 10Base-T, which is a traditional Ethernet system, and 100Base-TX, also known as Fast Ethernet. The number represents the transmission rate in Mbit/s, the second part (base) indicates that it is a baseband transmission and the final letters represent the physical media type (T for twisted-pair)[2].

Twisted-pair cables for Ethernet applications consist on two or four pairs of wires which are twisted around each other in order to cancel out EMI from external sources, such as crosstalk[13].

These wires have a maximum cable length requirement that needs to be respected[14], which is 100 meters for both cases[13]. Another specification to be considered is the impedance between the lines, which should be around 100 Ω, with a 15% margin of error[15].

1.3.7 AS-P Automation Servers

This device, later referred to as "unit", performs management tasks such as control logic functions, trend logging and alarm supervision[16]. It contains an Ethernet IC with an integrated PHY transceiver which is the main focus for this work since all data signals are transmitted and received through this medium.

All experiments carried out during this thesis were performed using AS-Ps. However, the ASIC solution proposed is to be implemented in any Ethernet-friendly environment since the standard specifications were respected.

Chapter 2
Ethernet Network

This chapter is dedicated to the description of specifications determined by the Ethernet protocol.

2.1 Standard Description

The official Ethernet standard is the IEEE 802.3, and the information below was extracted from documents and books referring to this standard[17].

Table 2.1 presents the main characteristics of 10Base-T and 100Base-TX media systems[6][18].

Media system identifier	10Base-T	100Base-TX
Encoding	Manchester	4B/5B
Signal Type	Sine Wave (+V, -V)	Multilevel (+V, 0, -V)
Frequency	Max 20 MHz	31.25 MHz
Max P-P Voltage	5 V	2.5 V
Min P-P Voltage at Receiver	585 mV	460 mV (typical value)
Idle Mode (no packet transmission)	LTP*	Continuous Signal
Busy Mode (packet transmission)	Continuous Signal	Continuous Signal
Auto-negotiation	LTP*	FLP**

Table 2.1: Protocol Characteristics.

*LTP (Link Integrity Test Pulse): 100 ns signal every 16 ms ± 8 ms. Also known as NLP (normal link pulse).

**FLP (Fast Link Pulse): 2 ms signal every 16 ms ± 8 ms. It is a sequence of 10Base-T LTPs.

Encoding schemes[18]:

- 10Base-T: works with Manchester encode and decode mechanism. A logic '1' is translated into a low-to-high transition whereas a logic '0' is represented by a high-to-low transition.
- 100Base-TX: works with 4B/5B encode and decode, non-return-to-zero/inverted NRZI coding, MLT-3 conversion and scrambling.
  - 4B/5B coding method: every 4-bit nibble is converted into a 5-bit word, providing more bit patterns.
  - NRZI coding method: Logic '1' represented by signal edges and logic '0' represented by a "keeping the value function", the signal polarity does not alter. It results in less signals edges than the Manchester encoding. In order to assure a minimum amount of signal edges to the receiver, the data is first converted with 4B/5B encoding method.
  - MLT-3: the data is transfered using the multilevel threshold-3 mechanism, which codes the NRZI signal into a three-level signal (+V, 0, -V) and vice versa. The goal is to decrease the frequency of the signal.
  - Scrambling: Transmission in 100 mbps speed requires scrambling to reduce the radiated emissions on the twisted-pair cables.

Ethernet frame size (values for 100Base-TX - fixed frequency):

- Minimum size of a packet of data: 576 bits or 72 bytes (4.6 μs);
- Maximum size of a packet of data: 12208 bits or 1526 bytes (97.66 μs);

2.2 Twisted-Pair Cable

IEE 802.3 specifies that for twisted-pair cabling, the 10 and 100 Mbit/s media systems have a maximum cabling distance recommendation of 100 meters. This applies for both full-duplex and half-duplex operation modes[17].

A 100-meter cable between two units is not realistic for this application. That is, if one unit in the network fails, the total cable length from one unit to the next active one would be of 200 meters. In other words, considering three units A,B and C, we would have 100 m from A to B, 100 m from B to C and 200 m from A to C if B fails. ***Therefore, in order to comply with the standard recommendations, the maximum cable length we can afford is 50 m between units.***

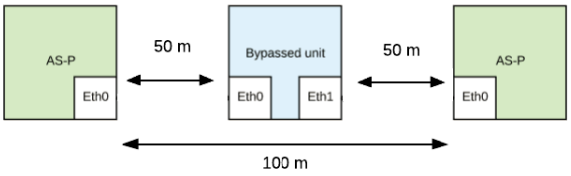

Figure 2.1: Cable Limitations.

The limitation mentioned above does not represent a major obstacle since a 50-meter cable length is long enough for daisy chain operations in buildings, which is the main future application of the ASIC in study. A daisy chain is a wiring scheme where multiple devices are connected in series[19].

It is worth stressing that typical installations usually place around 30 meters of cable between two units. Moreover, repeaters can be employed to increase the distance between the devices, but that would introduce a small delay in the propagation time of the signal through the network. This paper does not take into account the employment of repeaters, the environment being tested consists of only AS-P units and cables.

If the possibility of having more than one failed unit in series is considered, the maximum cable length between two units has to be smaller. The suitable cable length to be installed is given by the following equation:

$$C_{length} = \frac{100}{N+1};$$

where:

- 100 represents the maximum cable length between two units;
- N is the desired number of failed units between two operational devices.

Chapter 3
Transmission Signals

The transmission lines consist of two differential pairs, a transmitter and a receiver. These data signals transported over twisted-pair cables are polarized, one wire of each pair carries the positive signal and the other the negative[17].

A failed unit, in the middle of the chain between two active units, would receive the transmitting signals from both sides and forward it to the following device. These forward or bypassed signals would be perceived as receiving signals to the corresponding servers.

10Base-T and 100Base-TX provide transmission signals which are quite different. Encoding, peak-to-peak voltage, busy and idle behaviors and Auto-negotiation pulses are the main contrasts when it comes to the analysis of the signals.

In this chapter we will explore their behavior when trying to establish communication and the busy and idle mode that follow up.

3.1 Auto-Negotiation Protocol

Clause 28 of the IEEE standard defines the requirements for twisted-pair Auto-Negotiation.

The Auto-Negotiation protocol provides an automatic configuration feature for Ethernet interfaces over twisted-pair links. The stations can exchange information about their capabilities over a link segment and settle on a configuration respecting the highest set of common capabilities. Thus, they are able to detect and select the correct speed, duplex, and other features. This process follows a priority list, going from highest speed-full duplex to same speed-half-duplex. As the speed decreases so does the priority. For instance, 100 Mbit/s-full duplex has priority over 100 Mbit/s-half-duplex, which in turn has priority over 10 Mbit/s-full duplex and so on[17]. In other words, if both devices can operate at 10 and 100Mbit/s,

they will settle on 100Mbit/s since it is the highest set of common capabilities, therefore having priority over the lower speed.

Basic concepts:

- Operation over link segments: connects only two devices, one at each end.
- Occurs at link initialization: precedes any transfer of data. The characteristics set during Auto-negotiation are maintained for as long as the link is functional.
- Uses its own signaling system: suitable for any twisted-pair cabling that supports Ethernet.
- If a common mode of operation is not found, the communication will not be established.

The foundation of this concept is the link integrity test pulse (LTP), developed for the 10Base-T media system. Its main function is to assist in the detection of a failure in one of the transmission wires and it is transmitted when there is no data being sent. That is due to the fact that the transmission method for this speed results in the lack of signals in the segments if no data is being exchanged. For this particular case, LTPs are necessary to assure the interfaces at both ends of the link that they are working properly. On the other hand, 100Base-TX consists on a signaling method which employs a continual stream of signals even in idle mode, therefore LTPs are not required.

The Auto-negotiation protocol consists of fast link pulses (FLP) bursts, which are a sequence of LTPs. Each FLP can be described in the following manner[20]:

- There are 33 pulse positions;
- The 17 odd numbered positions are clock pulses.
- The 16 even numbered positions are data pulses.
- All clock positions are required to contain a link pulse. The same does not apply for data positions.
- A link pulse is translated into a logic ‘1’ , whereas a logic ‘0’ is represented by the lack of a link pulse.
- Approximately 1 V amplitude signal.
- The time between each pulse position is 62.5 us $\pm$ 7 us.

- The time between consecutive FLPs is 16 ms ± 8 ms.

As we can infer from the list above, each burst has a duration of approximately 2 ms. Some of the duration values can be verified in figures 3.1 and 3.2.

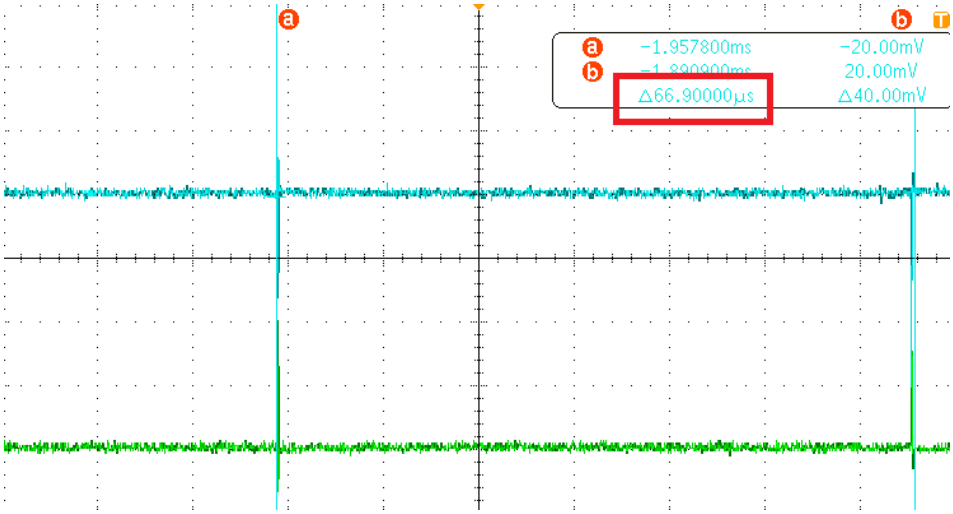

Figure 3.1: Fast Link Pulse.

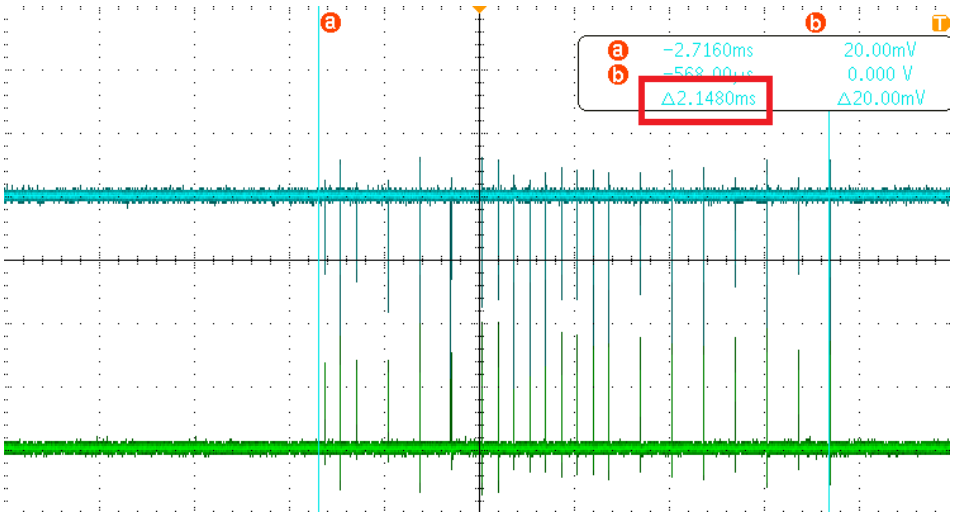

Figure 3.2: Fast Link Pulse in detail.

LTPs consist of a single uni-polar pulse that lasts 100 ns every 16 ms

± 8 ms. Both LTPs and FLPs have the same time interval between two consecutive transmission blocks. This was set in place so as to maintain compatibility with 10Base-T systems.

Figure 3.3: FLP and LTP Time Scale.

3.2 Established Communication

As mentioned before, idle and busy behaviors are different for the two media systems in study. This section is dedicated to the description of these two operational modes.

3.2.1 Idle Mode

Idle mode is best described as the behavior of the transmission signals on the link when no data is being transmitted. In other words, the communication has been established, the automation servers have recognized each other and settled on their common capabilities but are not exchanging data.

When automation servers that have selected a 10Mbit/s speed are in idle mode, the only signal on the segment for both pairs is the LTP, which was previously described.

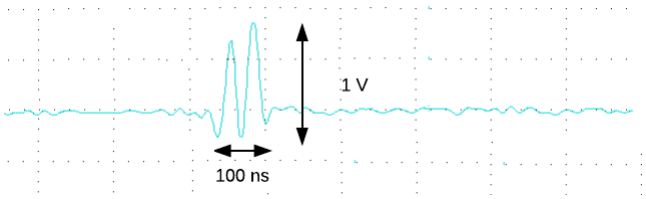

Figure 3.4: 10Mbit/s Idle Signal: One LTP Pulse.

Since there are no continuous signals present on the segment in this mode for the 10mbps speed, the LTPs fulfill their function of checking if the link is still up. Figure 3.4 illustrates a detailed image of one LTP pulse, which occurs every 16 ms. The signal above corresponds to a single line transmission.

In case the selected speed is 100Mbit/s, idle and busy behaviors are identical. Both cases result in continuous signals simultaneously on the two transmission pairs. Figure 3.5 presents the three-level signal which characterizes the 100Base-TX media system. It illustrates the signal on a single line, therefore presenting half of the full differential amplitude which is 2.5 V.

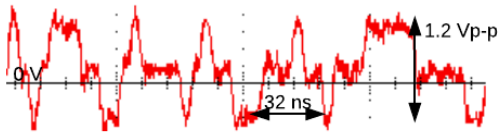

Figure 3.5: 100Mbit/s Idle Signal: Continuous MLT-3.

MLT-3 signals cycle sequentially through the three voltage levels available (+V, 0, -V). A full cycle requires four transitions to be considered complete, for instance -V to 0, 0 to +V, +V to 0 and 0 to -V[6]. As it can be observed on the image above, some transitions take slightly longer than others. Therefore, the period is not constant. The value presented is a descriptive value, an average corresponding to the 31.25 MHz signal frequency.

The voltage levels on figures 3.4 and 3.5 represent the maximum amplitudes the idle signals for both cases can reach. The data was captured at the transmitting end before suffering losses throughout the link segment.

3.2.2 Busy Mode

Busy mode consists on the behavior of the signals when data is being exchanged between the servers.

As mentioned before, if the selected speed is 100Mbit/s, both busy and idle modes provide continuous signals simultaneously on the two pairs. However, this does not apply for the other speed when transmitting data. Figures 3.6 and 3.7 illustrate the busy mode of these systems.

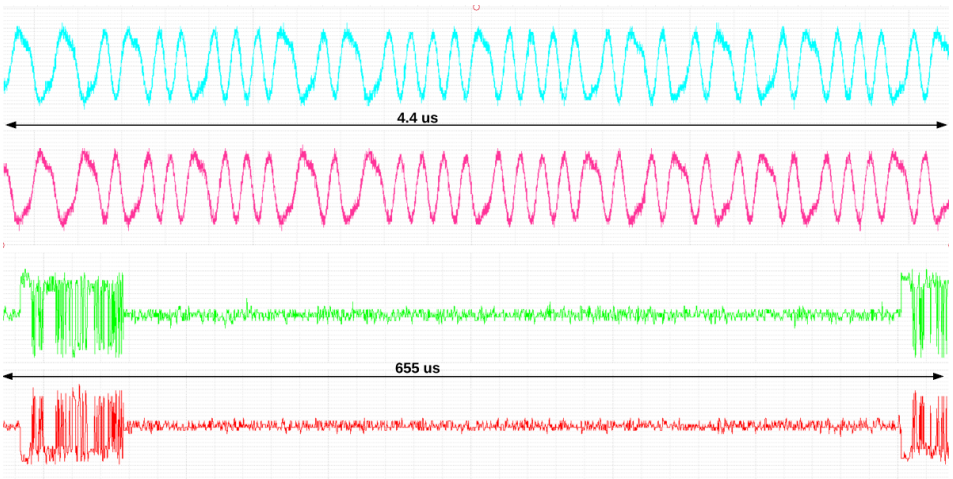

Figure 3.6: 10Base-T: Transmitting (Top) and Receiving (Bottom) Signals, Different Time Scale.

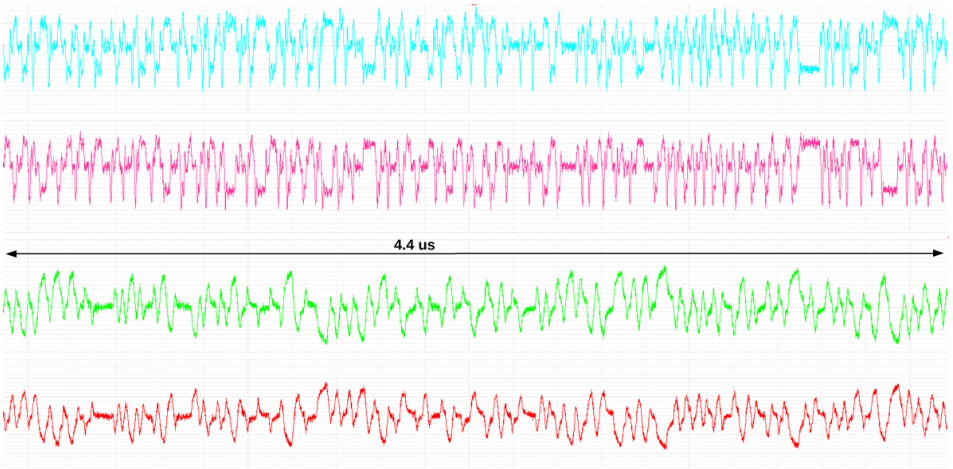

Figure 3.7: 100Base-TX: Transmitting (Top) and Receiving (Bottom) Signals, Same Time Scale.

10Base-T transmission method only presents a continuous signal when a packet is being sent and exclusively at the transmitting pair. The receiving signal is not continuous, being composed of bursts of pulses of approximately 65 μs every 620 μs. As it can be seen in figure 3.6, the receiving pair had to be extracted using a larger time scale than the transmitting pair in order to observe two different bursts.

This behavior generates difficulties to the implementation of the ASIC due to the following aspects:

- We wish to explore the two input transmission signal pairs in different manners. One pair is to be used for energy harvesting whilst the other will operate as a clock signal for a voltage multiplier block. If the units are not constantly communicating, there will be no signals on the lines.
- Even if they are communicating, only one pair presents a strong continuous signal. It is possible to harvest from the receiving signal lines and therefore use the transmitting pair as a clock, but not the opposite. The transmission lines are not predetermined, they can be either a transmitting or a receiving segment, which is randomly decided during Auto-negotiation. Therefore, in order to make it work with the current ASIC architecture, the transmitting and the receiving lines would have to be fixed since there is only one combination that is efficient.
- The signal connections could be different from the set-up mentioned on the first point: both transmission pairs could be used to harvest energy and the clock signals would be provided by an oscillator block. This solution works very well for the 10Base-T but not for the 100Base-TX. This is due to the fact that the amplitudes of the signals in the 10Base-T mode are quite high, harvesting enough energy to provide good clock signals. At 100Base-TX the clock signal is not good enough in order to guarantee a good performance from the step up block.

Even though both signal types were investigated, 100Base-TX media system is more broadly employed than 10Base-T. Due to the difficulties imposed by the 10Mbit/s signals, we are prioritizing the former. In other words, the current ASIC only guarantees a robust solution for the 100Base-TX mode.

It is worth stressing though, that there is a chance it could work with the 10Base-T system if the following requirements are met:

- During the Auto-negotiation process, the transmitting pair ends up being the one connected as a clock signal;
- The unit fails while a package is being sent (having enough time to charge the ASIC internal capacitors and turn on the bypass switches) or the unit fails in a short period after the last packet has been sent, so the capacitors are not fully discharged and the next packet arrives soon after.

3.3 Initialization of the Device

It has been previously mentioned that the Auto-negotiation burst signals lasts for 2 ms, every 16 ms and are composed of 33 pulses of 1 V. These signals are not enough to provide a high voltage at the output of the harvester and be used as clock signals to the step up. Consequently, the start up situation results in a problem.

The Auto-negotiation protocol is only successful if enabled on both sides of the link. If the two signals sent by one device do not reach the other (because the middle device is in power failure), communication is never established and the 3-multi level signals from the 100BASE-TX system are not present at the segment.

The AS-P units contain a PHY transceiver which default set-up is to enable the Auto-negotiation process. Our proposal to solve the start up issue is to implement a software modification regarding the default set-up of the chip. Referring to the PHY Control Register, Register 0, we suggest that whenever bit 15 (Reset bit) is '1' , bit 12 (Auto-negotiation enabling bit) should be '0' (Auto-negotiation disabled) for 1.3 s and then back to its default condition, '1' . The duration of this change is determined by adding the charging time of the step up capacitor (around 40 μs) to the duration of one burst of the disabled Auto-negotiation signal (1.19 s), rounding up to guarantee the incertitude is covered.

Whenever the Auto-negotiation protocol is disabled, the signals on the transmission lines look like the following:

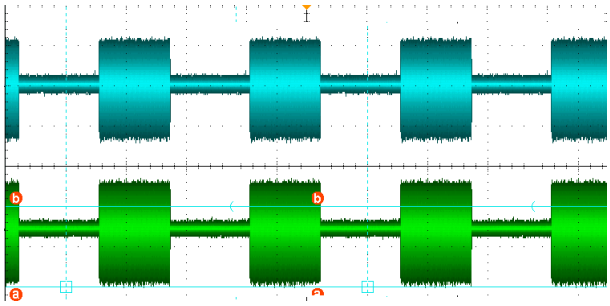

Figure 3.8: Signals on Transmission Lines For Disabled Auto-negotiation.

Transmitting and receiving pairs keep interchanging, in this manner it is not necessary to know beforehand which is the strongest signal, that should be used as clock.

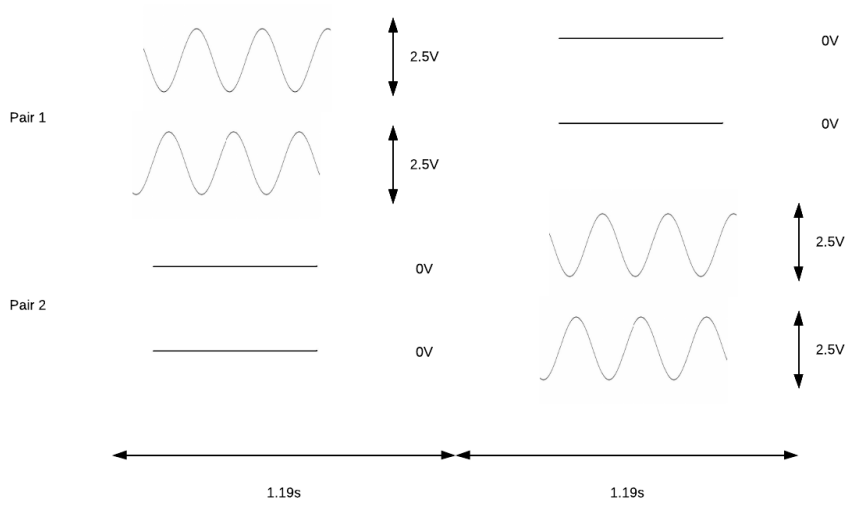

Figure 3.9: Disabled Auto-negotiation - Signal Behavior.

As it can be seen in figure 3.9, the full differential 2.5 V signal that was present in one pair in normal operation mode, is now present in one line. The overall voltage is kept the same since the other pair is at ground level. Each state lasts for around 1.19 s.

We bring attention to the fact that, to solve the start up issue, during installation, all units and cables should be placed before the system is powered on.

Chapter 4
Experiments

Multiple experiments were conducted to test the feasibility of the concept and to set the requirements for the ASIC design.

A description of the test bench is provided, as well as a detailed explanation of the different case studies.

4.1 Test Bench

Table 4.1 lists all the mediums required to perform the experiments.

Instrumentation	
Set-Up	Measurements
• AS-P devices; • Power unit: PS 24V; • RJ45 MagJack connector; • Cat5e cables; • Breadboards; • Resistors.	• Oscilloscope Tektronix DPO 3054; • Passive Probes; • Multimeter;

Table 4.1: Test Bench Equipment.

The signals observed in the oscilloscope were acquired through a USB cable and treated using *MATLAB*. These data files were also used in *Virtuoso ADE*, so as to perform simulations using the actual signals instead

of ideal sinusoidal sources.

4.2 Cable Influence

In order to cover longer areas in a building, more wire is needed between the servers. As the length of the transmission cables increases, so does the amplitude loss of the data signals. This effect will be further explained below.

4.2.1 Working Units

At this point, only fully operational automation servers are taken into account. The goal is to describe the system without considering failed nodes.

The amplitude loss caused by the cables was determined by measuring the amplitude difference in the transmitting and receiving signals between two units while varying cable lengths. The set-up was composed of two automation servers connected to each other with Cat5e Ethernet cables. A detailed image of the test bench can be found in figure 4.1.

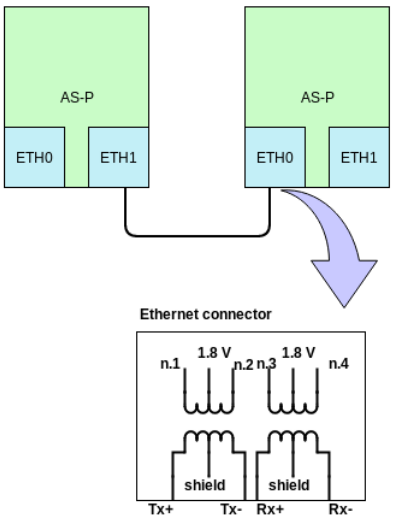

Figure 4.1: Cable Influence Test Bench.

The measurement nodes are labeled as "n1", "n2", "n3" and "n4". The middle windings of the transformers are connected to the unit supply of 1.8 V, which is the reference point for the signals and the ground connection for the oscilloscope. "n1" and "n2" constitute a transmitting pair while

"n3" and "n4" compose a receiving one. For future reference, the measurements between "nx" and the middle tap represent the signals per line while measurements between "n1" and "n2" or "n3" and "n4" constitute the full differential signals.

This first part consists on acquiring the transmitting signals on one unit and compare it to what will be received at the following unit. This acquisition happens at the same time on both ends. The data is then treated in order to account for the delay through the wires and align the corresponding signals. Figure 4.7 shows the full differential signals for different lengths of cable.

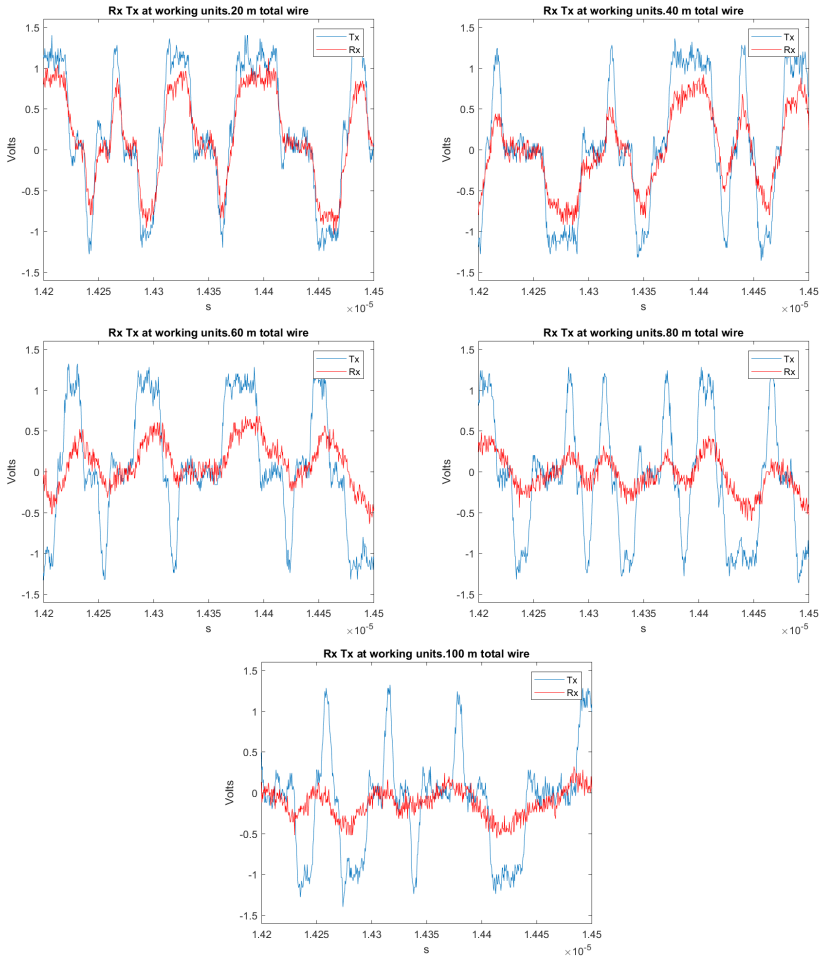

Figure 4.2: Transmitting and Receiving Signals for Varying Cable Lengths.

*Total cable length values consist on the total wire distance between two active units in

series.

It is noticeable that the cables have a detrimental impact in the amplitude of the signal which is a crucial aspect when it comes to the design of an ASIC powered by energy harvesting.

Table 4.3 presents the peak-to-peak amplitude voltage of the receiving signals and the voltage difference between the full differential transmitting and receiving signals, referred in the table as 'voltage loss'.

Total Cable Length*	100 m	80 m	60 m	40 m	20 m
Receiving Signal Amplitude (Vp-p)	0.76 V	0.82 V	1.02 V	1.41 V	1.84 V
Voltage Loss (Vp-p)	1.72 V	1.66 V	1.46 V	1.07 V	0.64 V

Table 4.2: Full Differential Signals Characteristics.

*Total cable length values consist on the total wire distance between two active units in series.

The voltage differences between the transmitting and receiving signals shown above were extracted and are presented in figure 4.4.

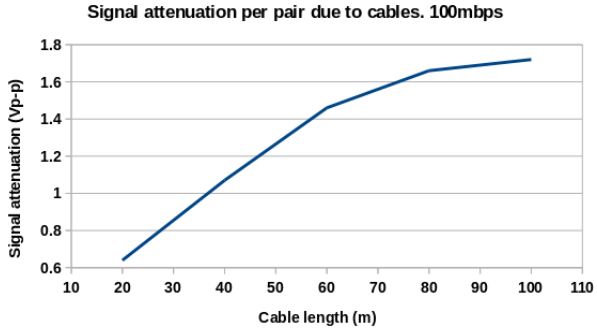

Figure 4.3: Signal Loss In Full Differential Pair In Respect To Increasing Cable Length.

*Total cable length values consist on the total wire distance between two active units in series.

The amplitude loss induced by the cables, for a single signal line, was determined based on the measurements collected above and is presented in figure 4.4

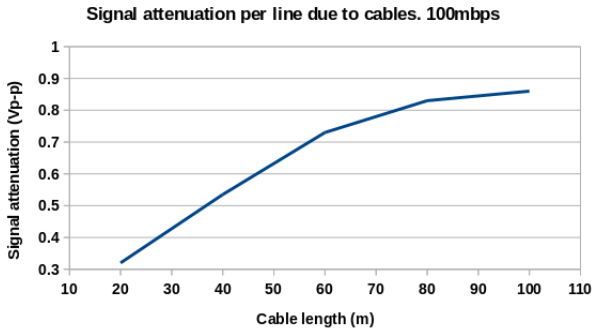

Figure 4.4: Signal Loss Per Signal Line In Respect To Increasing Cable Length.

*Total cable length values consist on the total wire distance between two active units in series.

Table 2.1 provides some information regarding the amplitude requirements of the signals. To recapitulate, the full differential signal at the transmitting point is 2.5 V, therefore 1.25 V per line, while the typical amplitude signal at the receiving point should not be lower than 460 mV full differential, 230 mV per line.

In order to determine the margin of voltage that can be sacrificed due to harvesting, the voltage levels of the receiving signals in red in figure 4.7, were compared to the minimum typical voltage accepted at the receiving end. In this manner, it is possible to quantify the affordable amplitude loss for each case without compromising communication. These values are presented in table 4.3.

Total Cable Length*	100 m	80 m	60 m	40 m	20 m
Affordable Voltage Loss	150 mV	180 mV	280 mV	475 mV	690 mV

Table 4.3: Available Voltage to be Handled.

*Total cable length values consist on the total wire distance between two active units in series.

4.2.2 Failed Unit

A model for the failed unit is introduced in the test bench set-up, as it can be seen in figure 4.5. The model implemented will be further discussed

in section 4.3.

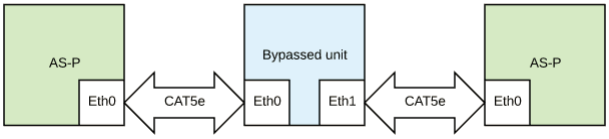

Figure 4.5: Test Bench Connections.

The measurements were acquired in the same manner as previously, in other words, taking into account the transmission signals after the transformers. While the middle windings at the working AS-P are connected to 1.8 V, at the bypassed unit they are only connected to each other, meaning they are not biased by any other supply. This is due to the model configuration employed in order to simulate the behavior of a bypassed unit, which consisted on a circuit using discrete components.

Figure 4.6 illustrates how the direction of the signals changes in different operation modes. Same color arrows represent the same signal.

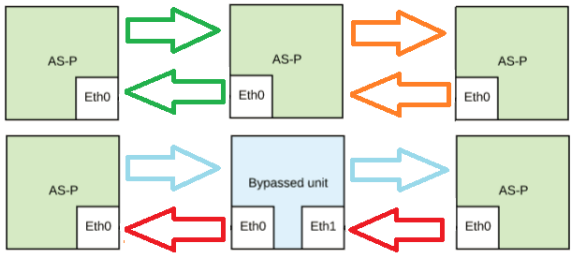

Figure 4.6: Signal Directions In Both Operation Modes.

In normal operation mode, only two devices communicate directly. Thus, unit A sends a signal to unit B (green arrow $\Rightarrow$) and unit B sends an answer (green arrow $\Leftarrow$). In bypassing mode, unit A sends a signal (blue arrow $\Rightarrow$) which passes through the failed node and is redirected to unit C (blue arrow $\Rightarrow$).

It can be inferred that only the signals arriving at the failed unit are of interest since the aim of this experiment is to evaluate the transmitting signals that will be bypassed at the failed node. These signals will be the input of the energy harvesting circuit. Therefore, an understanding of them is crucial for the design. Figure 4.7 illustrates these signals. Each signal on the images below represents the data in a single line, thus each image

translates the behavior of a transmitting pair.

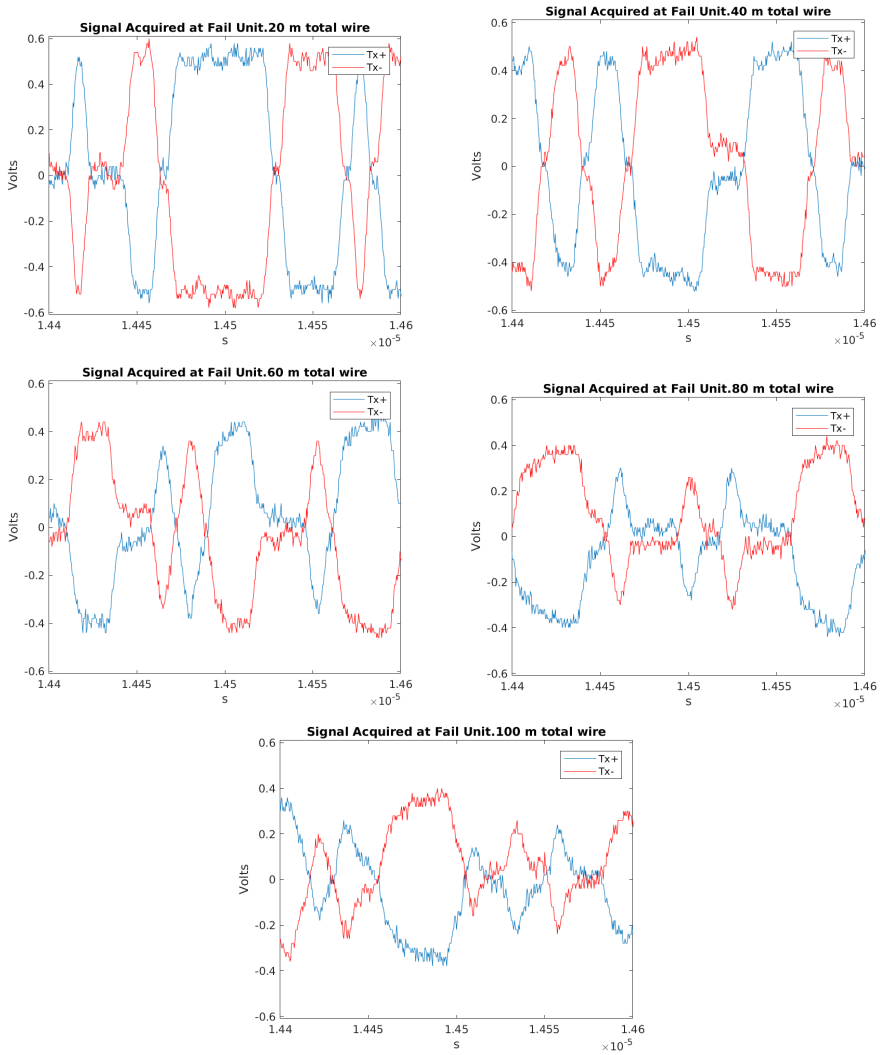

Figure 4.7: Signals at Failed/Bypassed Unit.

*Total cable length values consist on the total wire distance between two active units.

The amplitude of the signals can be found in table 4.4. It must be noticed that it represents the amplitude per line. At this point it can be determined that silicon conventional diodes are not suitable to build a rectifier for this application. Forward voltage drop of a silicon diode is around 0.6 V[33], which is higher than the amplitude of the signals. In other words, the amplitude of the signal to be rectified should be higher than the

forward voltage drop in the diode, otherwise the diode will not conduct. The architecture chosen and the alternatives considered are described in chapter 5.

Total Cable Length* (m)	100 m	80 m	60 m	40 m	20 m
Signal amplitude (V)	0.36	0.41	0.46	0.49	0.54

Table 4.4: Amplitude signal at the input of the energy harvester.

*Total cable length values consist on the total wire distance between two active units in series.

4.3 Resistance Influence

The use of MOSFETs as switches introduces resistance in the transmission lines. In order to verify the viability of the solution, resistors were added in series with each of these lines. They were placed between two RJ45 connectors, as seen in figure 4.5, so as to recreate the real conditions for the ASIC.

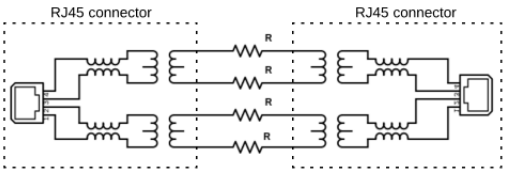

Figure 4.8: Bypassed Unit Model.

Figure 4.8 presents a diagram of the circuit designed to model a unit in failure mode. In other words, this can be viewed as a simplified version of the bypass switches to be employed in the ASIC. This circuit was placed between two AS-P units, with an equal cable length on both sides, as shown in figure 4.5

The connectivity was tested by sending files from one AS-P to the other and checking that the information arrived at the other end. The maximum resistance for length of wire was set by incrementing the value of the resistors and testing the connectivity for every case. The values shown in the next table present the highest values of resistance that allowed communication to be established in the 100Base-TX media system for different cable

lengths.

Total Cable Length*	100 m	80 m	60 m	40 m	20 m
Maximum Resistance	30 Ω	80 Ω	115 Ω	145 Ω	165 Ω

Table 4.5: Maximum Resistance per Cable Length. 100Base-TX.

*Total cable length values consist on the total wire distance between two active units in series.

The incertitude of the results is translated into a ± 5 Ω margin of error.

According to table 4.5, the worst case scenario consists on employing the maximum cable length specified by the standard, in other words 50 m between two units, 100 m total. That is due to the fact that the longer the cables, the less we can afford in resistance, which becomes a parameter limitation to the design.

We are aiming for an ultimate solution, which means the ASIC cannot introduce more than 30 Ω of resistance in each line.

Even though the 100Base-TX operation is being prioritized, this test was also carried out using 10 Mbit/s signals. The 10Base-T media system tolerates higher resistance than the 100Base-TX. For instance, the maximum resistor value corresponding to a 100-meter cable is 83 Ω. Since the resistance values for the 100 Mbit/s signals are lower, they are the ones being used as guidelines.

Considering the maximum cable length condition, the ASIC is limited to a maximum resistance of 30 Ω so as to not compromise the established communication.

4.4 Transformers

Transformers are used to isolate the units, as explained in the scientific background section. The Ethernet bypass switch circuit can be placed before the transformers to benefit from this protection, thus being located inside the unit. This results in several transformers connected back to back during bypass mode.

An experiment was conducted to test this situation. Several RJ45 connectors were connected back to back in the same manner as they would be if the ASIC was active, in other words the unit would be bypassing the data signals.

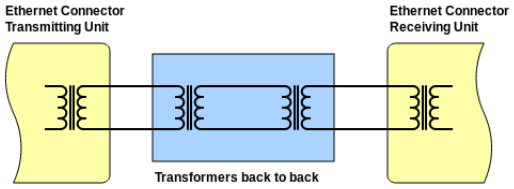

Figure 4.9: Diagram of Transformers Connected Back to Back.

The chain of connectors was linked with Cat5e cables, connecting two automation servers. The communication was tested and the result was satisfactory, proving feasible to have this type of configuration in the design.

Chapter 5
Circuit Design

Each of the main architecture blocks composing the ASIC is presented in this section whilst evoking some of the limitations that were overcome. Figure 5.1 shows a high level diagram of the whole system. A more detailed view of the full design can be seen in figure A.2 in the Appendix. The circuit is designed for 100 mbps signals.

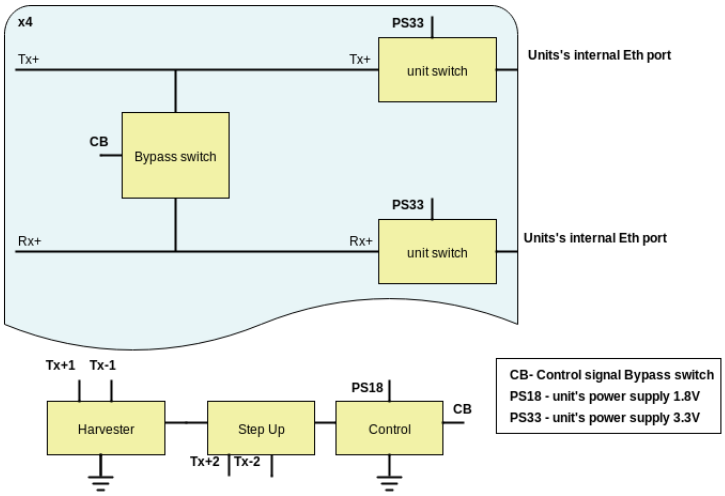

Figure 5.1: High Level Circuit Diagram.

5.1 Switches

The switches are the devices used to control the direction of the Ethernet signals. In working mode, unit switches are turned ON and bypass switches are turned OFF, which connects the automation server to the network. In case of a failure in the automation server, the bypassing mode is active

and the unit switches are turned OFF while the bypass switches are turned ON. In this case, the automation server is isolated from the network and the Ethernet signals are redirected to the next node of the network. This section contains a description of the configuration used to act as switches, the alternatives considered and the sizing of the devices in order to fulfill the requirements.

5.1.1 Description

The devices chosen to pass and block the Ethernet signals are MOSFETS due to their low resistance in comparison with JFETs[22]. Specifically, thick oxide NMOS. They offer better performance and lower $R_{DS\text{-}ON}$ than PMOS transistors[23], as well as allowing higher voltage supplies than thin oxide devices.

Each switch is composed of two NMOS transistors that share a terminal, to which the bulks are connected to. This connection method is called bidirectional switch, figure 5.2.

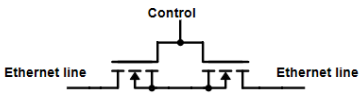

Figure 5.2: Bidirectional NMOS Switch.

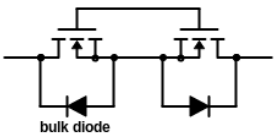

Figure 5.3: Equivalent Model.

5.1.2 Advantages

One of the main benefits of employing this configuration is related to the bulk connection. By being tied to the shared terminal, these nodes move along together which results in a quite stable threshold voltage. This is due to the fact that the voltage difference between source and bulk terminals remains practically unchanged. In this manner, it is possible to say that V_{TH} is independent of bias voltages and signal levels.

This architecture allows data to be transferred on both directions when the switch is turned ON and blocks current in both directions when the switch is turned OFF. The blocking function is made possible due to the reversed-biased bulk diodes, figure 5.3.

Moreover, this alternative does not require negative voltage supplies to provide robust results, although the availability of the latter would improve some performance functions. More information on this option is discussed in chapter 9.

The bidirectional switch configuration allows four operational states, which are presented in table 5.1:

Left Transistor	Right Transistor	State
ON	ON	Current can flow in both directions.
ON	OFF	Current can flow left to right, through left transistor and right bulk diode.
OFF	ON	Current can flow right to left, through right transistor and left bulk diode.
OFF	OFF	Current can't flow in either direction.

Table 5.1: Operational States For a Bidirectional Switch.

For this specific application, the gates of both transistors are connected together, so the devices are either both ON or both OFF.

The circuit implements two types of switches, referred to as bypass or unit switches. The latter do not constitute a change in the normal direction flow of the signal, they merely introduce the possibility of a blockage at the line. The bypass switches on the other hand, connect the receiving signal from one unit to the next, introducing a bridge between the inputs and outputs of the failed unit. Both switch functions are implemented through the bidirectional configuration.

When turned off, transistors connected between two communications lines act as capacitors[24]. The signals couple through the parasitic capacitance C_{DS} generating cross-talk[21]. Another important advantage of the architecture proposed for the bypass switches is that it allows the placement of an NMOS device connecting the shared terminal to ground. This is done in order to shunt the build-in charges in the parasitic capacitor and solve the cross-talk issue. This extra transistor is powered by the 1.8 V voltage supply provided by the automation server when in working mode.

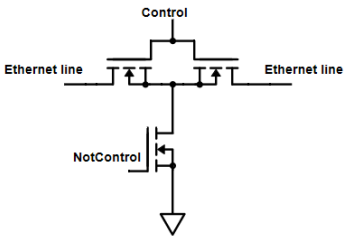

Figure 5.4: Decoupling Transistor.

There are a plurality of cross-talk models and calculation methods available depending on the applications[25][26][27]. It can be inferred that to properly determine its influence, a series of extra calculations and experiments would be necessary, which is out of the scope of this project. Therefore, the extra device mentioned above is implemented as a safety measure. However, due to the quite low frequency of the 100Mbit/s Ethernet signals, 31.25 MHz, cross-talking is not expected to have an important effect on the communication.

5.1.3 Other Alternatives

- Single transistor with bulk connected to Source terminal: In this configuration, the parasitic body diode would allow current to flow from bulk to drain. This would happen whenever the value of the signal is negative, even if the MOSFET is turned off.

- Single transistor with bulk connected to Source terminal in series with a diode: This implementation can be viewed as an improved version of the one mentioned above. In this case the current blocking is no longer an issue. However, the current flow would be unidirectional, which is not suitable for this application[28].

- Single transistor with bulk connected to a negative bias: This configuration requires a negative supply generator. The bias needs to be more negative than the Ethernet signal levels for every case in order to maintain the parasitic bulk reversed bias. If this condition is not fulfilled, it results in current flowing from the power supply to the transmission lines. This configuration would reduce the size of the switches but it would also increase the design complexity, besides not

allowing the possibility of tackling the cross-talk issue. This solution is discussed in chapter 9.

5.1.4 Sizing of Devices

The value of resistance introduced by this architecture should be within the limits showed in the experiments section.

In order to minimize the amplitude losses of the signals and to increase the number of allowable units in failure mode (always keeping in mind that there is a maximum cable length limitation imposed by the Ethernet protocol), the devices' parameters must be set in accordance.

The MOSFETs used in the bypass switches, in conduction mode, act as voltage controlled resistors [29]. The value of their resistance is described by the following equation:

$$R = \frac{L}{W \mu C_{\mathrm{OX}} (V_{\mathrm{GS}} - V_{\mathrm{TH}})}$$

Where μC_{OX} and V_{TH} are technology dependent.

Consequently, to obtain a low resistance, the transistor's length (L) should be small in relation to the width (W) whilst having a high control voltage (V_{GS}).

A lower resistance therefore results in an increase in area and consequently in manufacturing cost. A compromise between cost limitations and the physical limitations must be established.

Another drawback is the increase in the control voltage. To achieve a higher level, more step up stages need to be added. This solution results then in another issue, since there is a maximum voltage between terminals that has to be respected.

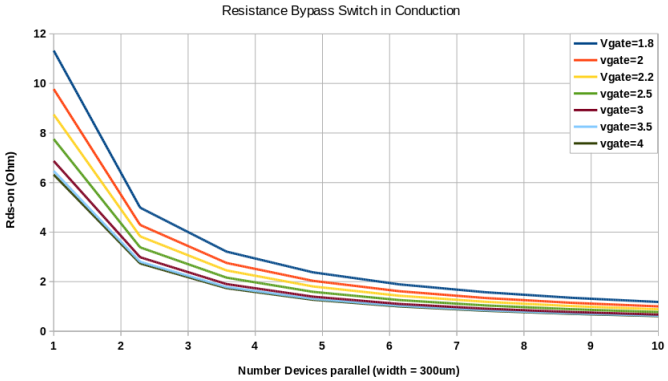

Figure 5.5: Bypass Switch Resistance for Different Control Voltages and Transistor Widths.

The resistance value for different levels of control voltage and transistor width can be seen in figure 5.5. The width is expressed in number of devices in parallel with a 300 μm width for each device. The simulation is for 65 nm technology and the length of the devices was kept to its minimum (0.280 μm for thick oxide devices). The resistance value is calculated for the worst case, which is having the biggest signal amplitude possible in 100 Mbit/s Ethernet (1.25 V peak-to-peak per line, amplitude ±625 mV).

The full resistance added in series to the transmission lines in case one unit is in failure mode is equal to: the resistance of the bypass switch plus two times the resistance of the switches that go into and from the unit.

$$R_{conducting} = R_{bypass} + 2R_{unit}$$

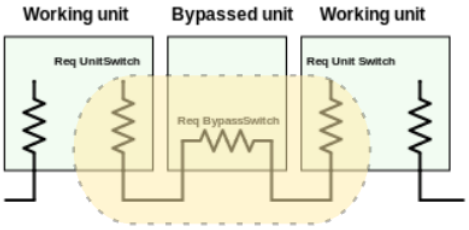

Figure 5.6: Total Equivalent Resistance Introduced In Series.

Figure 5.7 shows the effect of transistor sizing on the unit switches resistance, while keeping a fixed control voltage (supply: 3.3 V).

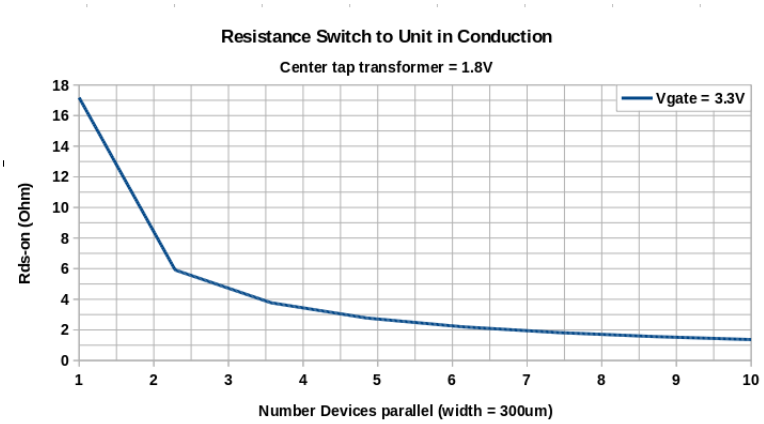

Figure 5.7: Resistance From/Into Unit Switches for Different Control Voltages and Transistor Sizes.

For this design, 3 devices in parallel, 900 μm wide each, were employed to ensure a high level of performance.

5.2 Harvester

The switches presented in the previous section require a voltage supply to operate. In case the automation server, where they are installed, has suffered a power failure, its power supply is not available. Therefore, the ASIC functionality depends on its own ability to harvest energy from the environment.

This solution explored the feasibility of using the Ethernet signals themselves as energy source. The alternating current(AC) signals need to be converted into a direct current (DC) signal. This section describes the different types of configurations and the type of the devices considered in the design.

Considering the requirements on minimum amplitude values presented in chapter 2 and the results of the experiments in chapter 4, it is possible to conclude that there is a margin of affordable loss for the signals. In other words, even though harvesting would result in a decrease in the amplitude of the signals, there is some margin to be explored while still respecting the set specifications.

As mentioned previously, the bypass circuit is placed inside the unit, benefiting from the isolation provided by the transformers. These devices present a middle winding referred to as center tap, which is connected to the 1.8 V power supply of the AS-P. Therefore, two scenarios must be

considered:

- Normal operation / Working unit: center tap connected to 1.8 V.
- Power failure / Bypassing unit: center tap is connected to ground level, 0V.

5.2.1 Configurations of rectifiers

Several architectures were explored in order to harvest energy from the transmission lines. The architectures considered can be seen in picture5.8.

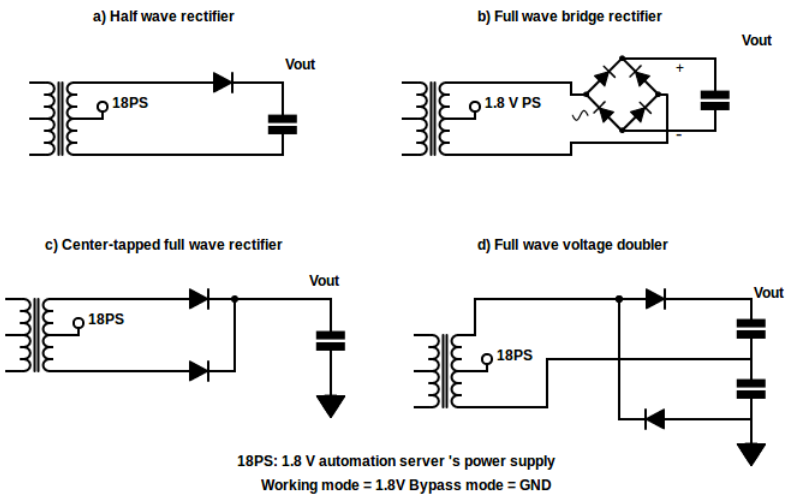

Figure 5.8: Different Configurations of Rectifiers.

a)Half wave rectifier:
It rectifies only the signal from one line, not the full differential[30]. The minus terminal of the capacitor moves with the signal. This reference point can not be grounded since it will ground half of the differential signal. However, if it is not grounded, the voltage on the positive terminal of the capacitor would be oscillating which would produce an alternating control voltage, which is why it is not suitable for this application.

b)Full wave bridge rectifier:
In theory, the full wave bridge rectifies the full differential signal[30], but in practice the center tap of the transformer is connected to GND during power failure. For this application, the full wave rectifier can only rectify half of the differential signal.

c)Center-tapped full wave rectifier:
It rectifies the signal from only one line[30] and provides a grounded reference without affecting the Ethernet signals. It solves the problem imposed by the half wave rectifier. It presents a comparable performance to the full wave rectifier and it requires less diodes. A comparison between the full wave bridge and the center-tapped full wave can be found in section 5.2.4.

d)Full wave voltage doubler:
This configuration was considered due to the fact that the value of the output voltage doubles the amplitude of the full differential signal[30]. In practice, however, this does not apply for this application. In bypass mode the center tap is connected to ground, what would result in an AC path from the center tap to the point between the two capacitors. This would produce an AC short circuit for one of the lines.

5.2.2 Rectifying Devices

Different types of devices can be used to build the previous configurations. A comparison among them was performed, both theoretical and experimental. The amplitude of the signals that are to be rectified were presented in table 4.4.

- MOSFET diode-connected: The main advantage of the diode connected MOSFET is its low forward voltage drop. The transistor is in the saturation region when it is in conduction mode since the voltage between drain and source is always greater than the voltage between gate and source minus the threshold voltage, $Vds > Vgs - Vth$. This condition always applies for a diode connected MOSFET.

  However, to be able to conduct, the voltage between gate and source needs to be greater than the threshold voltage. This implies a fundamental limit regarding how low the amplitude of the signal to be rectified can be.

  Another disadvantage of the diode connected MOSFET is the leakage current when it is reversed biased. Which can be mitigated by sizing the transistors properly[31].

- Standard diode: Formed by a PN junction. The main drawback of the standard silicon diodes is their high forward voltage drop of around 0.6 V[33]. They are not suitable for this application since the amplitudes of the signal are not high enough to make this diode conduct current properly.

- Schottky diode: Formed by the junction of a semiconductor and a

metal, it results in a lower forward voltage drop of around 300 mV for silicon devices[32].

The following picture shows a comparison between the contemplated devices. It can be seen that the diode connected MOSFET and the Schottky diode start conducting current around 330 mV and the standard diode around 640 mV. Another effect that can be noticed in the picture is the leakage current for the diode connected MOSFET when it is reversed biased.

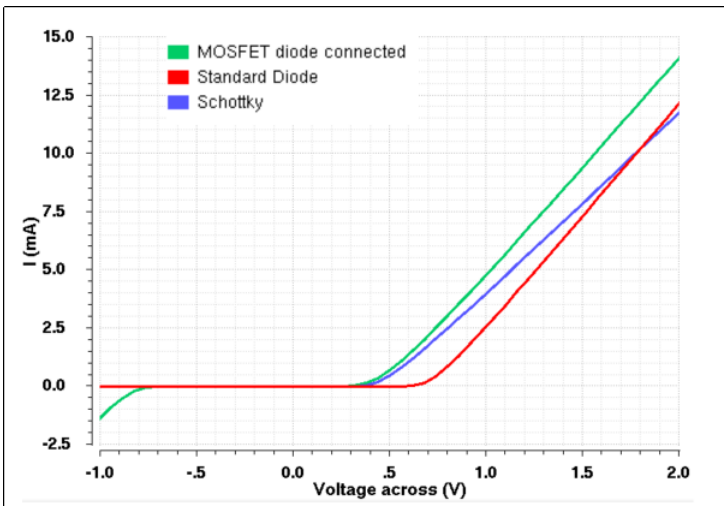

Figure 5.9: Comparison Rectifier Devices.

The device chosen was the Schottky diode because of its low forward voltage drop and its ability to block current when it is reversed bias.

5.2.3 Comparison Among Configurations

A comparison was drawn among different architectures in order to analyze their performance. The measurements were obtained for the 80-meter-total cable length case, harvesting from both input lines of a single transmission pair and employing three step up stages to deliver the gate voltage. The signals used in the simulation are the real Ethernet signals acquired with an oscilloscope. The results can be found below in table 5.2.

Harvester	Working mode	Failure mode		
	Time to fully charge	Time to fully charge	Output Voltage Harvester	Gate Voltage*
Center-tapped full wave	36 μs	85 μs	128 mV	1.79 V
Full wave bridge	37 μs	90 μs	125 mV	1.78 V
Full wave voltage doubler	35 μs	123 μs	1.03 V**	1.97 V

Table 5.2: Comparison Among Different Harvester Architectures.

*Section 5.3 explains how the voltage is stepped up to generate the gate voltage, which is the voltage used to control the switches.

**Voltage across both capacitors.

The results for the full wave voltage doubler are only indicative since the CMINUS terminal is not connected to ground. If analyzed separately, the CPLUS terminal presents an alternating signal that oscillates between 800 mV to 30 mV in failure mode, which is not suitable for the application. Also worth mentioning, it takes 123 μs for the gate voltage to reach its maximum value and stabilize, but to better compare the architectures, this solution takes 57 μs to reach the same gate voltage value as the other architectures (1.8 V). The connections can be seen in figure5.10.

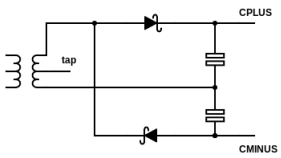

Figure 5.10: Full Wave Voltage Doubler Harvester.

*The tap node is either connected to the unit power supply of 1.8 V in working mode (power up) or to ground in failure mode (power down).

Different architectures and the devices that compose them were explored in order to harvest energy from the transmission lines. The selected devices are Schottky diodes due to their low forward voltage drop, which allows to harvest energy even for the worst case scenario of 100-meter-total cable length. The selected rectifier to act as an energy harvester is the center-tapped full wave. It is area efficient and provides a DC output.

However, the output voltage that it produces is not high enough to control the switches, which explains why the design requires a step up block.

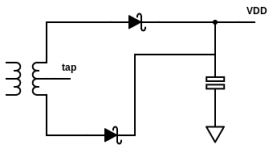

Figure 5.11: Center-tapped Full Wave Harvester.

*The tap node is either connected to the unit power supply of 1.8 V in working mode (power up) or to ground in failure mode (power down).

5.3 Step Up

The harvested energy is raised at the step up block, which provides the required gate voltage to close the bypass switches during power failure. This section contains a description of the chosen architecture and the alternatives that were considered during the design phase.

5.3.1 Description

The architecture chosen to achieve this is a charge pump with cascaded cross-connected NMOS cells and serial PMOS switches[35]. Figure 5.12 presents one stage of this implementation.

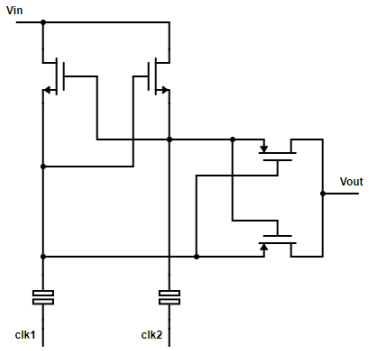

Figure 5.12: One Stage NMOS Cross-Connected Charge Pump.

The cascaded stages are introduced by connecting VOUT of the previous stage to VIN of the following one, in this manner the higher voltage generated in each stage is fed to the next one. A complete view of the step up block is found in figure 5.13.

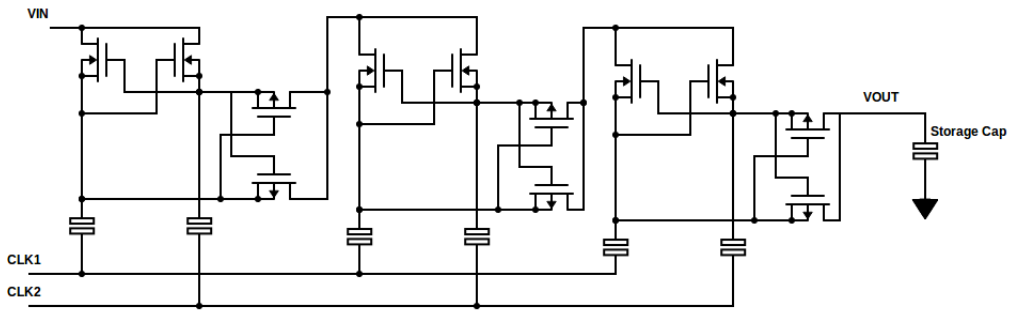

Figure 5.13: Step Up Block.

A three-stage implementation was chosen to achieve adequate voltage levels regarding the technology limitations, discussed later on this chapter. A capacitor was added as a load to the step up block so as to maintain the high voltage level achieved during working mode (power up), reducing the time to reach the desired gate voltage when in power failure. In this manner there is enough voltage saved and ready to be used when the unit power goes down without any packet loss.

Charge pumps can be seen as DC-DC voltage converters that employ switching devices in order to control the voltage connection to a capacitor, which function is to store and transfer the energy. The capacitors are charged when connected to a voltage source through the NMOS switches, and then pump this voltage to the following stage when the PMOS switches are on[36].The PMOS pair handles the charge transfer between stages, turning on/off at a certain clock phase, allowing unidirectional charge flow.

In normal applications, the output voltage of each stage is greater than the one of the previous stage by VDD (neglecting body effect and parasitics), which corresponds to VIN and the amplitude of the clock signal. This is true when the latter is equal to the input voltage value. This behavior can be observed in figure 5.14, where the power supply is 400 mV and the clock signals are ideal out-of-phase pulses of 400mV amplitude.

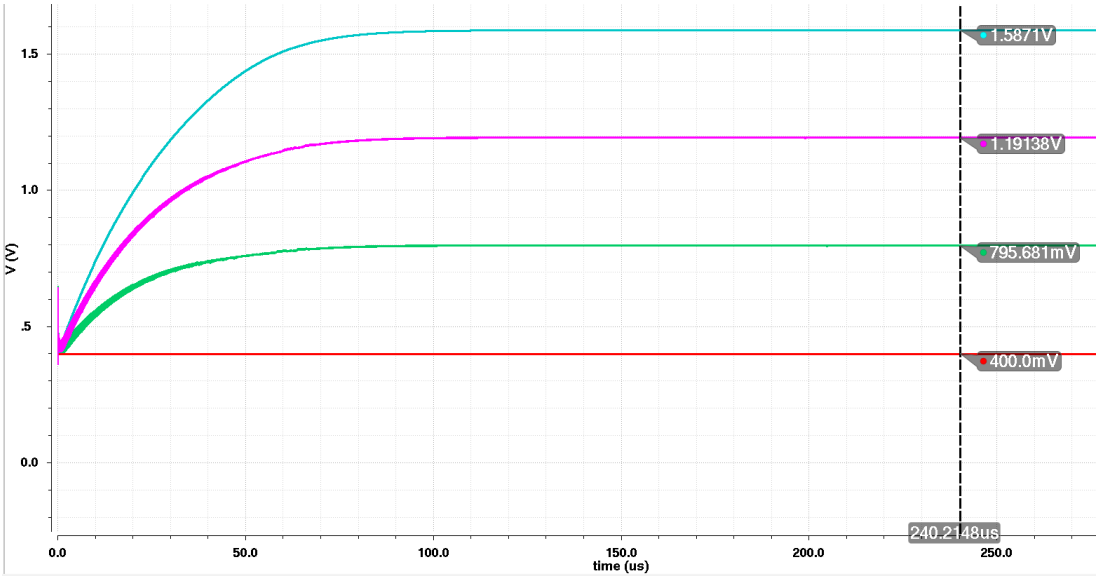

Figure 5.14: Normal Charge Pump Behavior - VDD: 400 mV.

The image above presents the input and output levels of each stage of a three-stage charge pump. As expected, the gain provided by each stage is close to VDD, suffering a slight decrease due to parasitics and body effect.

This ideal gain behavior does not apply for this application. In this case, the amplitude of the clock signal is much higher than the input voltage, which means that each charge pump stage provides a gain higher than the supply voltage. Thus, it is possible to achieve quite high output voltages, even though the input supply is considered low.

5.3.2 Other Alternatives

The voltage multiplier configuration is an option which does not require clock signals. In addition to it, it employs less devices per stage than most of architectures. However, as the number of implemented stages increases, the gain per stage decreases. It can be inferred that this type of design is only robust for certain applications and under a limited number of stages. Also, the voltage drop across the diodes becomes significant for low power applications, which is why it is not suitable for this project[34].

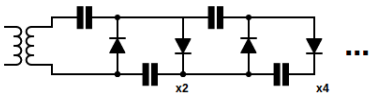

Figure 5.15: Voltage Multiplier.

The most popular version of a charge pump is known as Dickson's charge pump, illustrated in figure 5.16.

When CLK1 is high and CLK2 is low, a capacitor is connected across the supply, charging it to that same voltage. In the following cycle, the circuit is reconfigured so that the capacitor is in series with the supply to the load. Ignoring leakage effects, this provides double the supply voltage to the load (the sum of the original supply and the voltage across the capacitor).

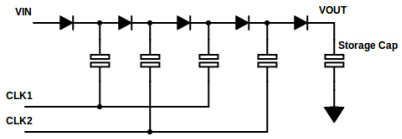

Figure 5.16: Dickson Charge Pump.

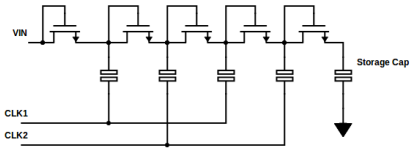

Figure 5.17: Dickson Charge Pump Using MOSFETS.

This architecture, however, presents significantly reduction of gain at low voltages. This is attributed to the voltage difference between source and bulk terminals of the NMOS, figure 5.17, which is elevated in the later stages due to the increase in voltage at the pumping nodes. As a result, the threshold voltage of the transistor becomes larger and more significant as the number of stages increases, reducing the efficiency of the design. In other words, the pumping efficiency is lowered by the body effect as the number of cascaded stages rises, and it is even more noticeable at low supply voltages[35].

Since the harvester block provides a low output voltage so as to not not deeply affect the behavior of the data transmission signals, the previous drawback applies to the current situation and the Dickson charge pump is therefore not suitable for this application. Hence, we employ the cascaded NMOS cross-connected cells, evoked previously.

5.3.3 Clock Signals

To drive the capacitors on each stage, two-phase non-overlapping clock signals are required. The source nodes of the NMOS are therefore out of phase. Several architectures of clock generators were considered and simulated.

- Ring Oscillator

  The ring oscillator is composed by a odd number of inverters in series. The output of the last inverter is fed back to the input of the first. Each inverter produces the logical NOT of its input. This produces a chain of logicals '1' and '0' . The change from one logical level to the other does not happen instantaneously, there is a delay between them. The delay is a function of the transistors parameters (W, L, μCox) and the power supply. The clock frequency is $f = \frac{1}{nT}$, with n being the number of inverters and T the propagation delay[37].

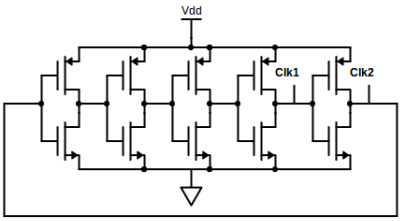

Figure 5.18: Ring Oscillator.

It offers a good performance for the 10 mbps signals because of the higher voltage amplitude levels in comparison with the 100 mbps. The employment of this architecture is then advisable only for 10Base-T systems, which would also require a full wave voltage doubler to act as harvester. This harvester provides high enough supply for the oscillator to perform properly, but still not enough to deliver satisfactory results for the 100Base-TX system.

As mentioned before, the transmitting methods for these two modes are quite different, making it difficult to define a single architecture that would provide robust results for both cases. For instance, if the oscillator is designed based on the 100 mbps signal specifications, it would be over-sized when a 10 mbps signal is transmitted. In result, the output voltage of the step up circuit would become excessive and exceed the transistor voltage limitations.

Figure 5.19 presents the resulted clock signals for the 100Base-TX case in bypass mode. It is possible to observe that the signal levels are not strong and they overlap, which does not provide an efficient performance for the charge pump.

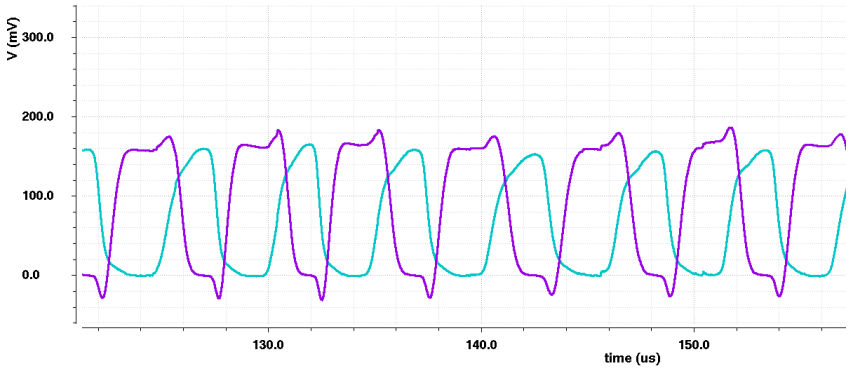

Figure 5.19: Ring Oscillator Clock Signals.

- Class D Oscillator

  Class D is a type of LC oscillator. It is suitable for low power supplies. The circuit is composed by a LC tank and two MOSFETS. It simplifies the complexity of the circuit with relation to class B/C oscillators[38].

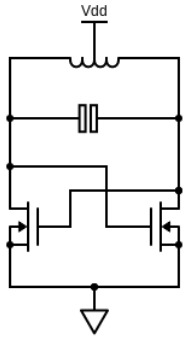

Figure 5.20: Class D Oscillator.

The amplitude of the oscillation is three times the input voltage and the oscillation frequency is given by the LC relation:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

This configuration was simulated for different cases and was proven to provide two completely complementary clock signals even for the worst case scenario. An extracted view of the resulted clock signals in bypass mode is found in figure 5.21. It could be used in addition to the half diode bridge harvester. However, it introduces inductors to the circuit which considerably increase chip area and complexity. An alternative would be to use off chip inductors which would elevate the cost of the solution.

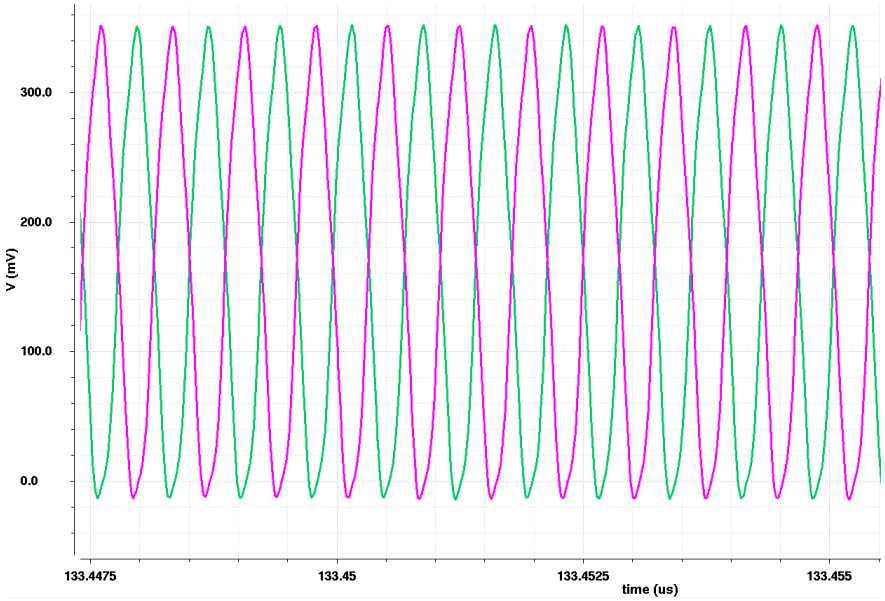

Figure 5.21: Class D Oscillator Clock Signals.

- Ethernet Signals as Clock

  The nature of the Ethernet data transmission signals make them suitable for being used as a clock for the step up block. The signals in each differential pair are complementary as explained more in detail in chapter 3, therefore complying with the required signal type for the circuit block in question.

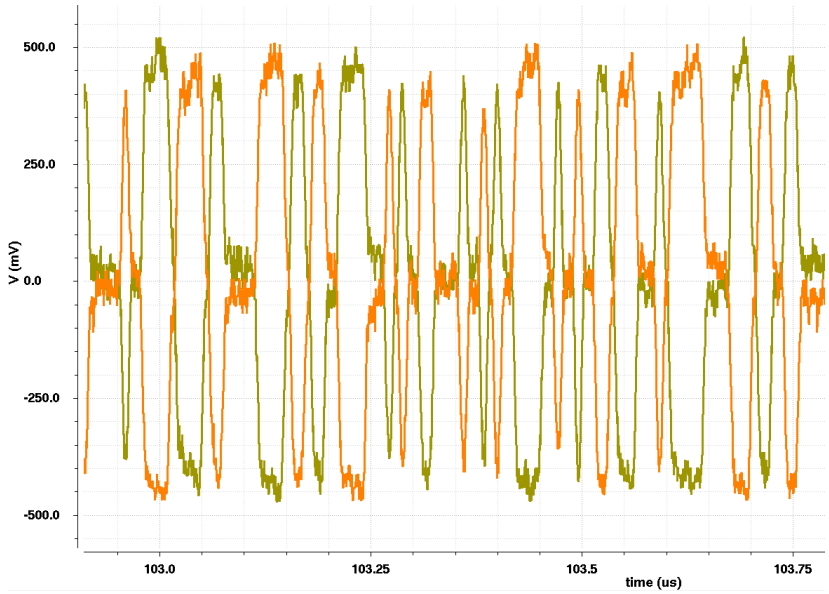

Figure 5.22: Ethernet Transmission Lines As Clock Signals.

As previously mentioned, 100Base-TX signaling method presents a continuous signal either in busy or idle mode, therefore this solutions does not represent an issue for this specific media system.

The selected option was to use the Ethernet signals as clock. This is a robust solution for the 100Base-TX environment and it simplifies the complexity of the design, as well as reducing chip area and therefore manufacturing cost. However, it is not suitable for 10 mbps signals.

It is worth stressing that 10 mbps signals introduce difficulties regarding the clock signals but also for the harvester. The performance of the harvester is dependent on how frequent the units communicate. If long periods on idle mode are in place, oscillators will present difficulties to produce continuous clock signals because of the decreasing input voltage. Thus, the functionality of the ASIC would be compromised regardless the origin of the clock signals.

5.4 Control

A control block is implemented between the charge pump and the gates of the bypass switches. Their purpose is to either connect the gates to

ground (transistors in bypass switches blocked in working mode) or to the output of the step up (transistors in bypass switches conducting in failure mode).

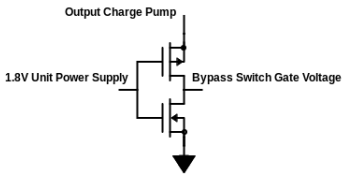

Figure 5.23: Control For The Bypass Switches.

In power failure, the power supplies provided by the unit become grounded. Therefore the supply itself is used as a control signal for this block, triggering the bypass mode operation. The same applies for the gate voltages of the unit switches and the decoupling transistors, all controlled by unit voltage supplies. In this manner, as soon as the unit goes into failure mode, the switches coming from or into the unit are blocked, isolating the unit from the network.

5.5 Process Technology

It must be stressed that the CMOS technology to be selected to fabricate this solution needs to be able to handle the voltage levels required to turn on the transistors. This study was carried out using the 65 nm technology. This is not the best suitable alternative due to the limited maximum voltage allowed across the transistors terminals.

Two solutions are proposed in order cope with this constraint:

- Using 65 nm technology while employing a combination of capacitors and resistors connected in a specific way;
- Implementing a larger technology.

In 65 nm process, a maximum supply voltage of 2.5 V using thick oxide transistors is allowed. In conducting mode, the resistance of the bypass switches is inversely proportional to the control voltage, therefore a higher voltage is interesting to reduce the size of the transistors while maintaining the same resistance.

The maximum peak-to-peak voltage per line in the 100 mbps case is 1.25 V, thus the maximum amplitude is ± 625 mV. Considering that for the

current case the threshold voltage Vth is around 490 mV, 1.2 V of gate voltage would be enough to close the switch but a higher gate voltage is desirable to reduce the amplitude loss in the signal.

A gate voltage of 2 to 2.3 V has been proven to pass the signal with acceptable losses for all cable lengths tested (up to 100 m total), resulting though in a voltage difference between terminals that would exceed 2.5 V. Since the signals are alternative, with a high enough frequency this would not be an issue. 31.25M Hz is considered to be quite low, therefore we should not exceed this limit. For simulation purposes the design was not modified, but if it were to be fabricated in this technology, the following solution would be employed (which was previously evoked in the first item of the list above):

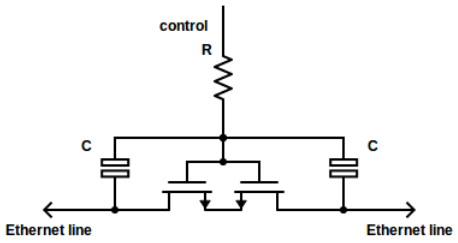

Figure 5.24: Solution to Overcome Voltage Limitations Across the Oxide.

This solution consists in adding a big resistor between the applied control voltage and the gates of the transistors and capacitors between their gates and drains. This system allows the gate voltage to move with the signals, therefore a quite low voltage can be applied.

The main advantage is that it does not require a high gate voltage. Consequently, depending on the level of the harvested energy, a step up block would become unnecessary during failure mode. This solution is not area nor cost effective though, requiring quite large capacitors in order to keep the same performance levels. For instance, each stage of the step up presents two capacitors in the hundreds of femto range, while the capacitors needed for this solution need to be in the hundreds of nano range.

At this point, we observe some difficulties so as to block the signals when the unit is working, due to the capacitors in series which would short the two signal lines. If employed, this solution would require an extra design block in order to tackle this issue.

The use of a larger technology is recommended to allow higher supplies and reduce the cost of the ASIC.

Chapter 6
Layout

The layout design is the final step into the characterization of the circuit. It provides information on the area usage required, parasitics and more precise simulation results.

6.1 Floor Plan

The layout cell view for the design can be seen in figure 6.1.

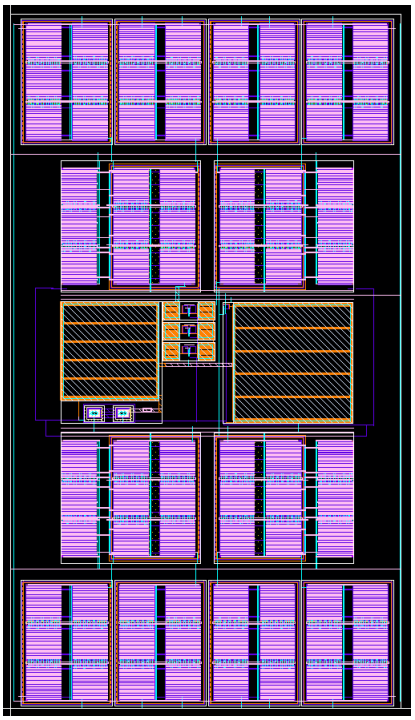

Figure 6.1: Layout View.

Wide transistors are employed in both bypass and unit switches. In order to improve the distribution of the blocks, the transistors are split into multiple fingers. By doing so, there is more flexibility regarding their placement, as well as the shape of the cell.

The design as seen above presents the following dimensions, 259 x 461 μm^2, which results in a total silicon area of 1.19x10^5 μm^2.

Figure 6.2 illustrates the arrangement of the blocks and the axis of symmetry which were taken into account for an efficient area usage.

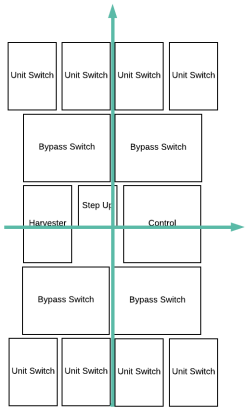

Figure 6.2: Layout Distribution - Axis of Symmetry.

6.2 Routing

There are four different set-up connections when it comes to connecting the inputs and outputs* to the ASIC:

	Application	
Case	Harvester Input	Charge Pump Clock Signal
1	Input	Input
2	Input	Output
3	Output	Input
4	Output	Output

Table 6.1: Possible Pin Connections.

*Signals are classified as input or output from the bypass circuit's point of view.

All these combinations were tested during the pre-layout phase. The results are presented in the next section.

Regarding the layout implementation, there are two alternatives as to how to connect the application blocks in respect to the signals. Assuming we do not know the direction of the data transmission, the harvester and the clock signals can be either of the same type (both from input or output pair signals) or different (one from an input pair and the other from an output pair). Simulation analysis provided similar results. So as to maintain a symmetrical approach, we have selected the first alternative, exploring same type signals.

6.3 Pads

This Ethernet bypass switch circuit has 19 pins. 16 Ethernet signal terminals and 3 voltage supplies.

Figure 6.3 illustrates the complete layout for the chip.

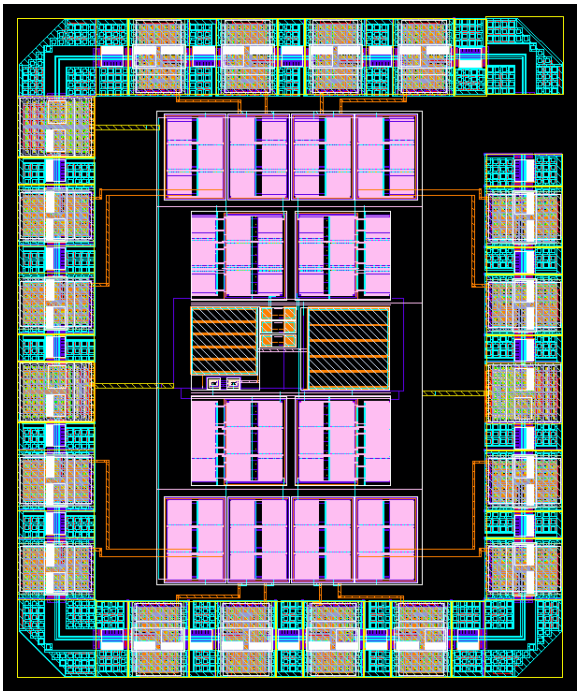

Figure 6.3: Complete Layout View.

The total dimensions of the chip are 531 x 642 μm^2, which results in a total area of 3.4x10^5 μm^2.

Chapter 7
Simulations

The same test bench environment was used for both pre and post-layout simulations. The results are presented below.

7.1 Test Bench

This test bench was designed so as to recreate in the most accurate way the environment to which the ASIC would be subjected to.

It is composed of five main blocks:

- 1. Sources: 1.8 and 3.3 V voltage sources and data signal sources representing the transmitting signals coming from the units when in working mode (1.2 V per line).
- 2. Signals' connections in working mode.
- 3. Signals' connections in power failure
- 4. Termination lines: to avoid signal reflection.
- 5. Connectors: transformers and data signal sources representing the attenuated signal arriving at a receiving unit.

The relays used to establish the signals' connections are controlled by a square signal. The parameters have been set in a way that the working mode is active for 80 μs and the rest of the simulation is in failure mode. This approach in set so as to observe the switching of the signals when there is a change in the operation mode. We wish to observe how much voltage is lost and how long it takes to recharge the capacitors.

Node	Working Mode (Power ON)	Failure Mode (Power OFF)
Tap	1.8 V	Ground
Output Unit Switch	Data signal source TX (1.2 V per line)	Termination Line
Power Supplies	Voltage Sources	Ground

Table 7.1: Node Connections.

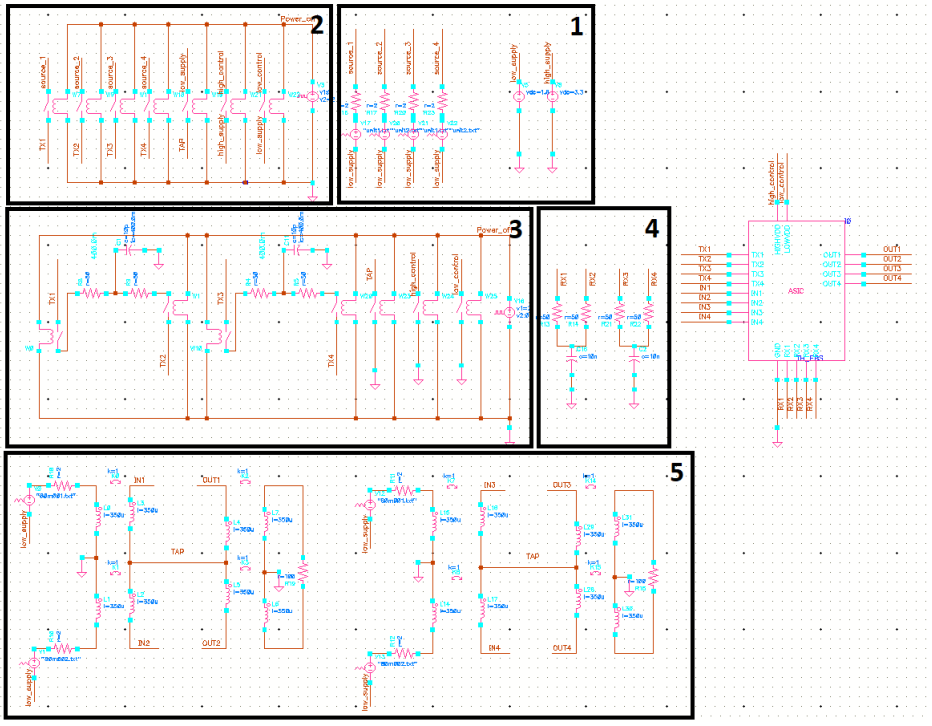

Figure 7.1: Virtuoso Test Bench.

7.2 Pre-Layout Results

The simulation results presented in this section were achieved through verification tests using the schematic view of the circuit.

All measurements were acquired by modeling normal failure conditions, which means that the automation servers were fully functional for some time before failing.

These verifications were set to 300 μs, employing ideal capacitors and the actual signals extracted from the units through the oscilloscope.

All results are presented in relation to the total cable length, which consists on the total wire distance between two active units in series.

Table 7.2 presents the equivalent resistance values to the switches. In addition to it, a comparison is drawn between these values and the measurements obtained during the experiments with discrete components.

Total Cable Length	100 m	80 m	60 m	40 m	20 m
Resistance Bypass Switch	1.27 Ω	1.07 Ω	1.11 Ω	1.18 Ω	0.84 Ω
Resistance Unit Switches (Input + Output)	2.1 Ω	2.11 Ω	2.11 Ω	2.12 Ω	2.13 Ω
Total ASIC Resistance	3.37 Ω	3.18 Ω	3.22 Ω	3.3 Ω	2.97 Ω
Maximum Accepted Resistance (±5 Ω)	30 Ω	80 Ω	115 Ω	145 Ω	165 Ω
Percentage Used by the ASIC	11.2 %	3.9 %	2.8 %	2.3 %	1.8 %

Table 7.2: Effective Resistance.

We can infer that the introduced resistance by the ASIC is well within the limits.

The following results have taken the upcoming measurements into account:

- Output voltage of the harvester block.
- Bypass switch gate voltage: the value in the tables is the maximum voltage level for that test case.
- Time to achieve a stable voltage level at the step up output when the unit is is working mode.
- Time to achieve a stable gate voltage when the unit is in failure mode: this parameter is pertinent even though the capacitors charge during working mode because there is a voltage drop during the change in mode of operation, thus the capacitors are no longer fully charged. This value is determined by the time it takes the system to reach its maximum output, in other words it measures how long it takes to stabilize the output voltage. It is worth mentioning that the gate

voltage is already high enough to pass the full signals after 13 to 20 μs for all cases.

- Transmission signal amplitude loss per line through bypass switches: average value in all four signal lines.
- Transmission signal amplitude loss per line through unit switches: average value in all four signal lines.
- Transmission signal average peak-to-peak amplitude coming out of the ASIC ;

As previously mentioned, there are four different set-up connections regarding the input and output signals. The results from the simulations of these case-studies are presented below.

■ Case number 1: Harvester and clock terminals both connected to input pairs.

Total cable length	100 m	80 m	60 m	40 m	20 m
Output Voltage Harvester	82 mV	135 mV	191 mV	227 mV	376 mV
Gate Voltage	1.55 V	1.8 V	1.98 V	2.14 V	2.5 V
Time To Charge (working mode)	81 μs	37 μs	25 μs	20 μs	15 μs
Time To Charge (failure mode)	184 μs	104 μs	63 μs	68 μs	27 μs
Voltage Loss Through Bypass Switch	14 mV	16 mV	13 mV	19 mV	12 mV
Voltage Loss Through Unit Switch	32 mV	35 mV	35 mV	37 mV	26 mV
Amplitude Output ASIC ($\pm$ 20 mV)	580 mV	670 mV	785 mV	911 mV	1100 mV

Table 7.3: Harvester $\rightarrow$ INP, Clock $\rightarrow$ INP.

- Case number 2: Harvester terminals connected to an input pair and clock terminals connected to an output pair.

Total cable length	100 m	80 m	60 m	40 m	20 m
Output Voltage Harvester	100 mV	145 mV	188 mV	208 mV	386 mV
Gate Voltage	1.56 V	1.79 V	2.03 V	2.13 V	2.5 V
Time To Charge (working mode)	16 μs	14 μs	13 μs	15 μs	14 μs
Time To Charge (failure mode)	67 μs	59 μs	47 μs	28 μs	30 μs
Voltage Loss Through Bypass Switch	13 mV	15.5 mV	13 mV	13.5 mV	17 mV
Voltage Loss Through Unit Switch	28 mV	29 mV	27 mV	29 mV	30 mV
Amplitude Output ASIC ($\pm$ 20 mV)	630 mV	680 mV	810 mV	920 mV	990 mV

Table 7.4: Harvester $\rightarrow$ INP, Clock $\rightarrow$ OUT.

- Case number 3: Harvester terminals connected to an output pair and clock terminals connected to an input pair.

Total cable length	100 m	80 m	60 m	40 m	20 m
Output Voltage Harvester	770 mV	635 mV	601 mV	480 mV	380 mV
Gate Voltage	2.29 V	2.32 V	2.36 V	2.4 V	2.48 V
Time To Charge (working mode)	78 μs	33 μs	24 μs	16 μs	13 μs
Time To Charge (failure mode)	100 μs	44 μs	34 μs	21 μs	17 μs
Voltage Loss Through Bypass Switch	15 mV	12 mV	11 mV	13 mV	23 mV
Voltage Loss Through Unit Switch	30 mV	26 mV	28 mV	32 mV	24 mV
Amplitude Output ASIC ($\pm$ 20 mV)	650 mV	685 mV	800 mV	910 mV	1010 mV

Table 7.5: Harvester $\rightarrow$ OUT, Clock $\rightarrow$ INP.

- Case number 4: Harvester and clock terminals both connected to output pairs.

Total cable length	100 m	80 m	60 m	40 m	20 m
Output Voltage Harvester	715 mV	570 mV	490 mV	370 mV	360 mV
Gate Voltage	2.18 V	2.24 V	2.27 V	2.28 V	2.46 V
Time To Charge (working mode)	13.7 μs	13 μs	13 μs	14 μs	14 μs
Time To Charge (failure mode)	101 μs	44 μs	33 μs	22 μs	24 μs
Voltage Loss Through Bypass Switch	13 mV	14 mV	10 mV	14 mV	15 mV
Voltage Loss Through Unit Switch	26 mV	27 mV	26 mV	26 mV	30 mV
Amplitude Output ASIC ($\pm$ 20 mV)	640 mV	685 mV	740 mV	885 mV	1010 mV

Table 7.6: Harvester $\rightarrow$ OUT, Clock $\rightarrow$ OUT.

7.3 Post-Layout Results

The simulation results presented in this section were achieved through tests using the layout view of the circuit.

Total cable length	100 m	80 m	60 m	40 m	20 m
Output Voltage Harvester	92 mV	140 mV	190 m	225 mV	390 mV
Gate Voltage	1.53 V	1.76 V	1.95 V	2.09 V	2.48 V
Time To Charge (working mode)	79 μs	36 μs	25μs	19 μs	14 μs
Time To Charge (failure mode)	155 μs	99 μs	85 μs	36 μs	26 μs
Voltage loss Through Bypass Switch	16 mV	14 mV	12 mV	18 mV	20 mV
Voltage Loss Through Unit Switch	26 mV	31 mV	33 mV	35 mV	24 mV
Amplitude Output ASIC ($\pm$ 20 mV)	600 mV	670 mV	760 mV	880 mV	1000 mV

Table 7.7: Harvester $\rightarrow$ INP, Clock $\rightarrow$ INP.

To perform such experiments the layout cell view has to be extracted in order to account for the parasitics. The measurements were conducted in the same manner as in the pre-layout section, using the same test bench.

As explained in chapter 6, the input terminals of the harvester and step up blocks were connected in a way that both input signal pairs were used. Therefore, we can only compare the post-layout results with the first case of the pre-layout measurements. However, depending on the direction of the transmission signals in the real application, there would also be the option of using both output signal pairs. Here, "input" and "output" labels are determined from the ASIC's point of view. The input signals are the ones being bypassed while the output signals are the resulted data that has traversed the failed unit.

It can be inferred that both simulations present quite similar results, which means that the added parasitics do not have an important effect on the performance of the circuit.

7.3.1 Power Consumption

The power consumed by the ASIC was computed by calculating the power difference between input and output terminals.

$$P = \int_0^T V(t)I(t)dt$$

$$P = P_{in} - P_{out} = \int_0^T \sum_{n=1}^{m} Vin_n(t)Iin_n(t)dt - \int_0^T \sum_{n=1}^{m} Vout_n(t)Iout_n(t)dt$$

Through these equations we wish to determine the power consumption of our design.

The results presented below were calculated independently for each mode of operation of the unit, in other words working and bypassing modes. During each operation, the step up block presents two different phases: charging and steady state.

Total Cable Length	Step Up Phase	Unit Mode of Operation	
		Working	Bypassing
20 m	Charging	18.45 mW	23.34 mW
	Steady state	17.27 mW	8.25 mW
40 m	Charging	17.26 mW	3.13 mW
	Steady state	16.81 mW	819.6 μW
60 m	Charging	17.12 mW	2.56 mW
	Steady state	16.72 mW	792.3 μW
80 m	Charging	16.98 mW	835.6 μW
	Steady state	16.53 mW	633.2 μW
100 m	Charging	16.57 mW	648.2 μW
	Steady state	16.23 mW	281.9 μW

Table 7.8: Total Power Consumption.

The consumption from the unit power supply remains practically constant regardless of the length of the wires used. The reason for an increment in the total power consumption for shorter distances is that more energy is harvested from the Ethernet communication. The amplitude of the signals is larger and that allows the Schottky diodes to conduct more current into the storage capacitor.

It can be noticed that once the unit fails and switches to bypass mode the power consumed is lower, which is attributed to the fact that enough energy to charge the storage capacitors was harvested before the failure.

The AS-P server currently consumes 10 W. Adding the Ethernet bypass switch ASIC to this unit would result in an 0.19% increase in power consumption during working mode, which is negligible.

Chapter 8

Overall Specifications

A list summarizing the fundamental aspects to be taken into account when designing such a circuit is presented below.

- Maximum cable length between two units: 50 meters.
- Maximum ASIC effective resistance: 30 Ω.
- Maximum affordable amplitude loss : 150 mVp-p.
- Tolerable amount (N) of failed units in series dependent on cable length. Both parameters are related by: $C_{length} = \frac{100}{N+1}$.
- High output voltage levels have been reached with different harvester architectures. However, high levels are not needed since we have a step up block, therefore it becomes unnecessary to push the limits of harvesting into affecting communication.
- A start up power device is not needed. The initialization issue can be solved by setting a different operational mode for a specific register in the PHY transceiver.
- During first installation: units and cables need to be placed before powering up the system.
- No extra protection requirements are imperative besides the isolation provided by the transformers. Since the latter passed the back-to-back test connections, the circuit can be placed inside the unit.

Table 8.1: Asserted Performance Conditions.

*Resistance and amplitude loss values for a maximum cable length between two units of 50 meters.

The main results achieved by experimenting with the ASIC in different set-up cases is presented in the following table.

- Robust solution guaranteed for 100Base-TX mode.
- ASIC equivalent resistance introduced in series with the transmission line is 3.3 Ω.
- Resulted signal loss lower than 100 mVp-p.
- 19 pins: 16 for Ethernet signals and 3 for voltage supplies (3.3 V, 1.8 V and GND).
- Total design area: 1.19x10^{-3} cm^2 (pads not included).
- Total chip area: 3.41x10^{-3} cm^2 (pads included).
- Total power consumption:
  - Worst case (20 meters): 18.5 mW in working mode/ 24 mW in bypass mode;
  - Best case (100 meters): 16.5 mW in working mode/ 300 μW in bypass mode

Table 8.2: Ethernet Bypass Switch Characterization.

Chapter 9
Design Improvements

This chapter is dedicated to the proposal of possible improvements regarding the design previously characterized. The former sections are independent from the following propositions.

9.1 Negative Voltage Supply

The purpose of adding a negative voltage generator to the existing architecture is to provide a more robust design. The goal is to ensure that the switches will block the signals properly and reduce leakage when the transistors are turned off. This situation only arises in some specific cases.

In order to turn off these switches, the voltage between gate and source terminals should never be higher than the transistor's threshold voltage. For this specific design, the threshold voltage is 490 mV.

When the unit is in working mode, the center tap of the transformers is connected to 1.8 V, ensuring that the Ethernet signals are centered around this voltage. In this manner, the signals are never negative and it is therefore enough to connect the gate voltage of the bypass switches to 0 V to ensure that the transistors will not conduct current when they are turned off.

When the unit is in bypass mode the center tap of the transformers is connected to 0 V, which shifts the level of the Ethernet signal, presenting negative values. As a result, a negative supply is needed to ensure a proper blockage of the signals when the unit switches are turned off. This only represents an issue if the amplitude of the signal is higher than the threshold voltage. Among the different case studies with 100Mbit/s signals, this is only true for the 20-meter-total cable length case.

The negative voltage is generated by a cascaded PMOS cross-connected cell with serial NMOS switches, which schematic view of a single stage can be found in figure 9.1.

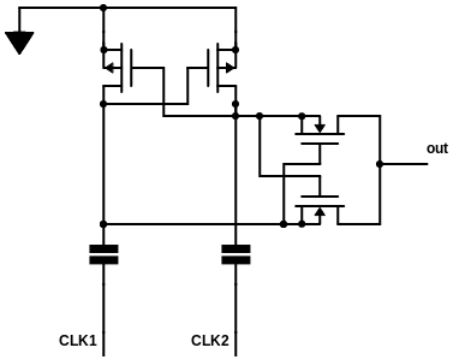

Figure 9.1: One Stage PMOS Cross-Connected Charge Pump.

This charge pump architecture is the same type of structure implemented for the step up block, described in chapter 5. The difference between these two cells is the inversion of the transistor types and the input voltage.

Here, the input of the charge pump is connected to ground while the clock signals are the same as in the step up circuit. Three stages in series were employed to reach an output voltage more negative than the lowest level a 100 Mbit/s signal can present.

In order to simulate this proposition, the schematic view presented on chapter 5 was modified. Both bypass and unit switches' configurations were maintained. The only difference is that in bypass mode (power failure), the gate of the unit switches is now connected to a negative supply instead of being connected to GND. This test was also performed using the Ethernet signals acquired with the oscilloscope.

Figure 9.2 presents the Ethernet signals as well as the control voltages for bypass mode. The simulation shows the case for 20-meter-total cable length. A case where the amplitude of the signal is approximately 600 mV. It is shown that the control voltage of -800 mV allows an efficient blocking of the signal through the unit switch.

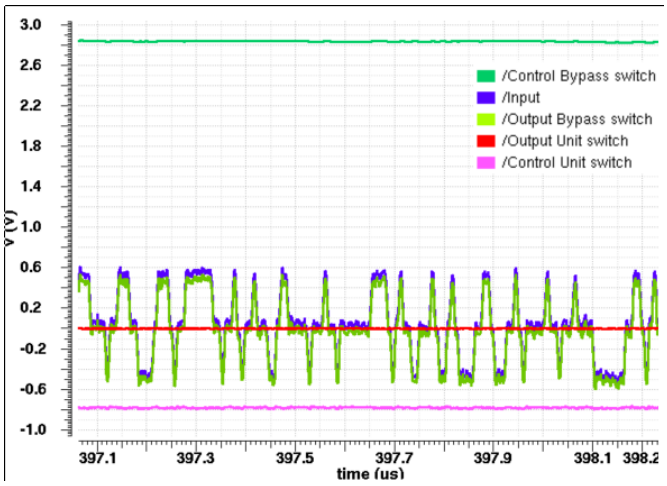

Figure 9.2: Ethernet Signals.

Control

A new control architecture needs to be implemented to connect the gates of the transistors to the voltage levels required for each mode. In power failure, the power supplies provided by the unit become grounded. Therefore the supply itself can be used as a control signal for this block.

This architecture that needs to be implemented has the same structure as the the control design previously presented. The latter defined the connections of the bypass switch gate voltage while this new one controls the connections of the unit switch gate voltage.

There are two possible states:

- Working mode: the unit switches are turned on and the bypass switches are turned off. The gates of the unit switches and the decoupling transistors are connected to the unit power supply of 3.3 V and 1.8 V, respectively, while the gates of the bypass switches are connected to ground.

- Bypass mode: the bypass switches are turned on and the unit switches are turned off. The gates of the bypass switches are then connected to the output of the positive step up block while the gates of the unit switches and the decoupling transistors are connected to the output of the negative step up block, previously referred to as negative supply generator.

9.2 Switches

This section introduces a proposal to reduce the total silicon area. The solution consists on changing the bidirectional NMOS switch configuration by a single NMOS. It becomes possible if the negative supply generator is included in the design. The unit and bypass switches cases are addressed separately. This alternative has not been tested for every case scenario and it is not present in the previously proposed design.

9.2.1 Unit Switch

The bidirectional switches employed for the unit switches could be replaced by a single NMOS transistor as a consequence of the availability of a negative supply. The bulk terminal of these transistors would then be connected to the negative supply, ensuring that the bulk diode remains reversed bias. This configuration allows the switch to block properly the current when the transistor is turned off.

This solution would reduce the number of transistors used for the unit switches by half. Considering that unit switches are the most numerous device in the design, the reduction in area is considerable.

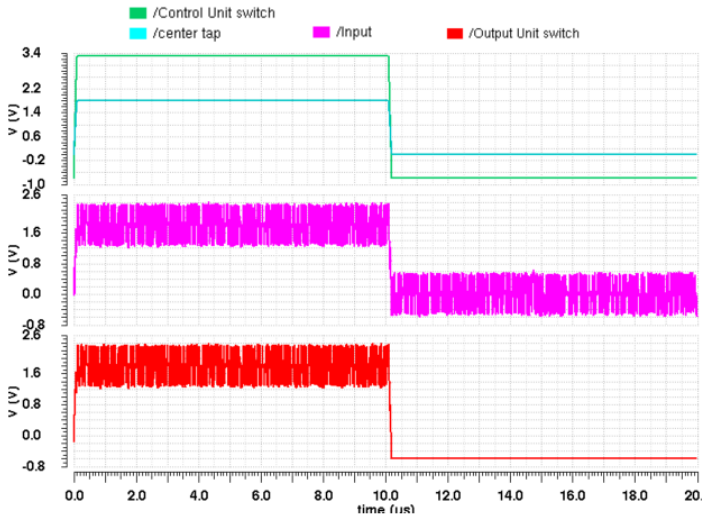

Figure 9.3: Signals Through Single MOSFET Unit Switch.

Figure 9.3 presents some simulation results for this particular case. The test bench consisted on the stand alone switch, the Ethernet signals and the corresponding biases. During the first 10 us the MOSFET is on, allowing

the signal to pass, modeling the working mode of the unit. During the last 10 us the MOSFET is OFF, blocking the signal, modeling the bypassing mode of the unit.

The Ethernet signals used correspond to the 20-meter-total cable length case. The bulk is biased to -800 mV. The gate terminal is biased to 3.3 V for working mode and -800 mV during bypass mode. The signal reference level is 1.8 V during working mode.

9.2.2 Bypass Switch

The same modification mentioned above could be applied to the configuration of the bypass switches. In other words, the bidirectional architecture could be replaced by a single NMOS transistor with the bulk connected to the negative bias.

In this case, the switch would be controlled by GND in working mode and by the output of the positive step up in bypass mode.

It is worth mentioning that although this implementation results in less area usage, it does not provide the possibility of addressing the cross-talk phenomenon. As mentioned previously, an extra transistor was added to the bidirectional switch configuration as a safety measure, which would not be possible in this case.

On these terms, if this alternative design is carried out, an extensive study and model of the existing cross-talk in the circuit would be required so as to determine if the configuration is suitable for this application.

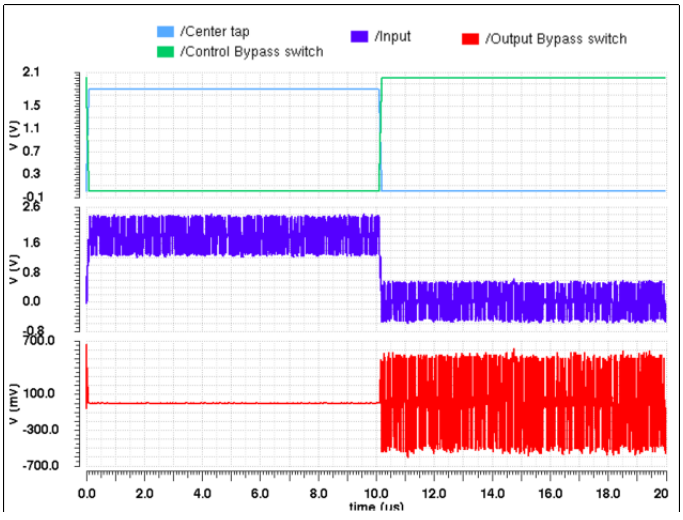

Figure 9.4: Signals Through Single MOSFET Bypass Switch.

Figure 9.4 presents the simulation results for the bypass switch case. The test bench consisted in the stand alone switch, the Ethernet signals and the corresponding biases. During the first 10 us the MOSFET is OFF, correspondent to the working unit mode. During the last 10 us the MOSFET is ON, modeling the bypassing mode of the unit.

The Ethernet signals used correspond to the 20-meter-total cable length case. The bulk is biased to -800 mV. The gate terminal is biased to 0 V for working mode and 2 V during bypass mode. The signal reference level is 1.8 V during working mode.

Chapter 10
Future Work

The validity of an Ethernet bypass switch in the ASIC form has been achieved. The theoretical information regarding the limitations were gathered for future reference and robust results have been delivered during the simulations. Thus, this thesis' goal has been reached.

The next step into the analysis of this solution is a practical experiment. This can be done by producing a SMT circuit so as to test further the circuit's behavior when inserted into an actual application environment. This verification would provide detailed information about response time and performance.

The proposals presented in the Design Improvements chapter can be explored further in order to improve the design. Simulations for every case scenario with schematics and layout are needed to ensure that they meet all the requirements.

It is worth stressing that even though this research was based on one specific type of automation server, this solution is meant to be employed in any Ethernet-friendly environment. In other words, the implementation of the circuit is dependent on the application device, more precisely if is in accordance with the Ethernet standard or not.

Chapter 11
Conclusion

In order to correctly design the Ethernet bypass switch circuit, as well as understand the application environment in which it would be inserted, a research period was required. An analysis of the Ethernet standard protocol, with an emphasis in the physical layer, was performed. This study was fundamental to determine the requirements to be met to complete such a project.

The concept alone was uncertain and had to be investigated. Once this step was attained, it had to be proven that the idea could be implemented as an integrated circuit. The proposed device is then an ASIC composed of solid state switches powered up by energy harvesting.

Difficulties were faced through the process of designing a single architecture able to provide satisfactory results for both media systems in study, 10 and 100 mbps. These complications are attributed to the fact that these two systems present very different transmitting methods, which directly affects the performance of the circuit. This led to the conception of two possible architectures, one specifically for each case. Although both possibilities are mentioned, the main focus of this work is to prioritize real case situations, therefore only the circuit for the 100 mbps is explored in depth since it is more broadly employed.

The ASIC's characterization was presented in detail with the schematic and layout views. Simulation results were also included in order to provide a more comprehensive description of the circuit's behavior and performance.

Pre and post-layout results are within the specifications set during the research phase, both in terms of resistance added in series to the communication lines and in the amplitude loss. We can infer that the aim of the thesis was accomplished successfully, consequently a novel solution to solve the exposed problem is proven viable.

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Appendix A

Appendix

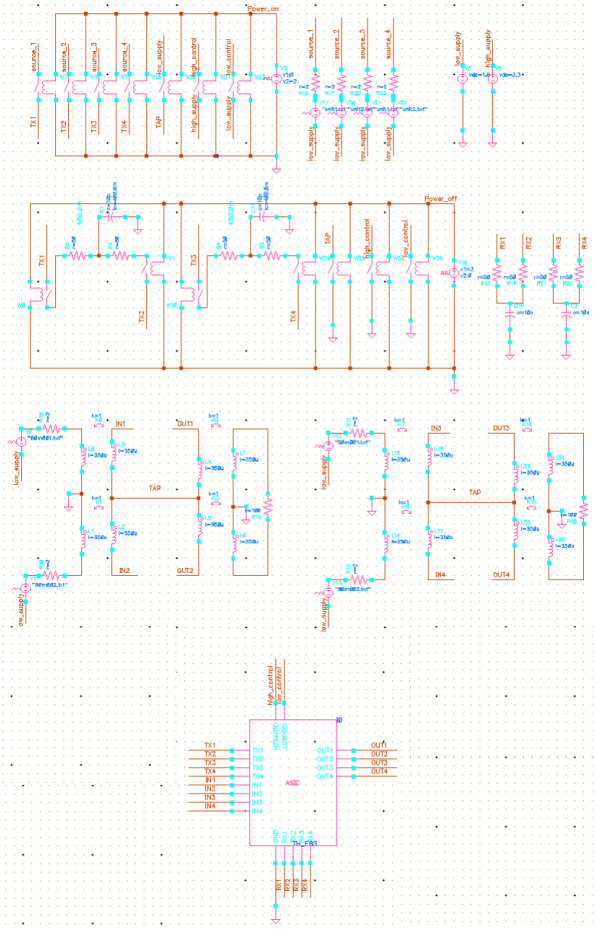

Figure A.1: Virtuoso Test Bench.

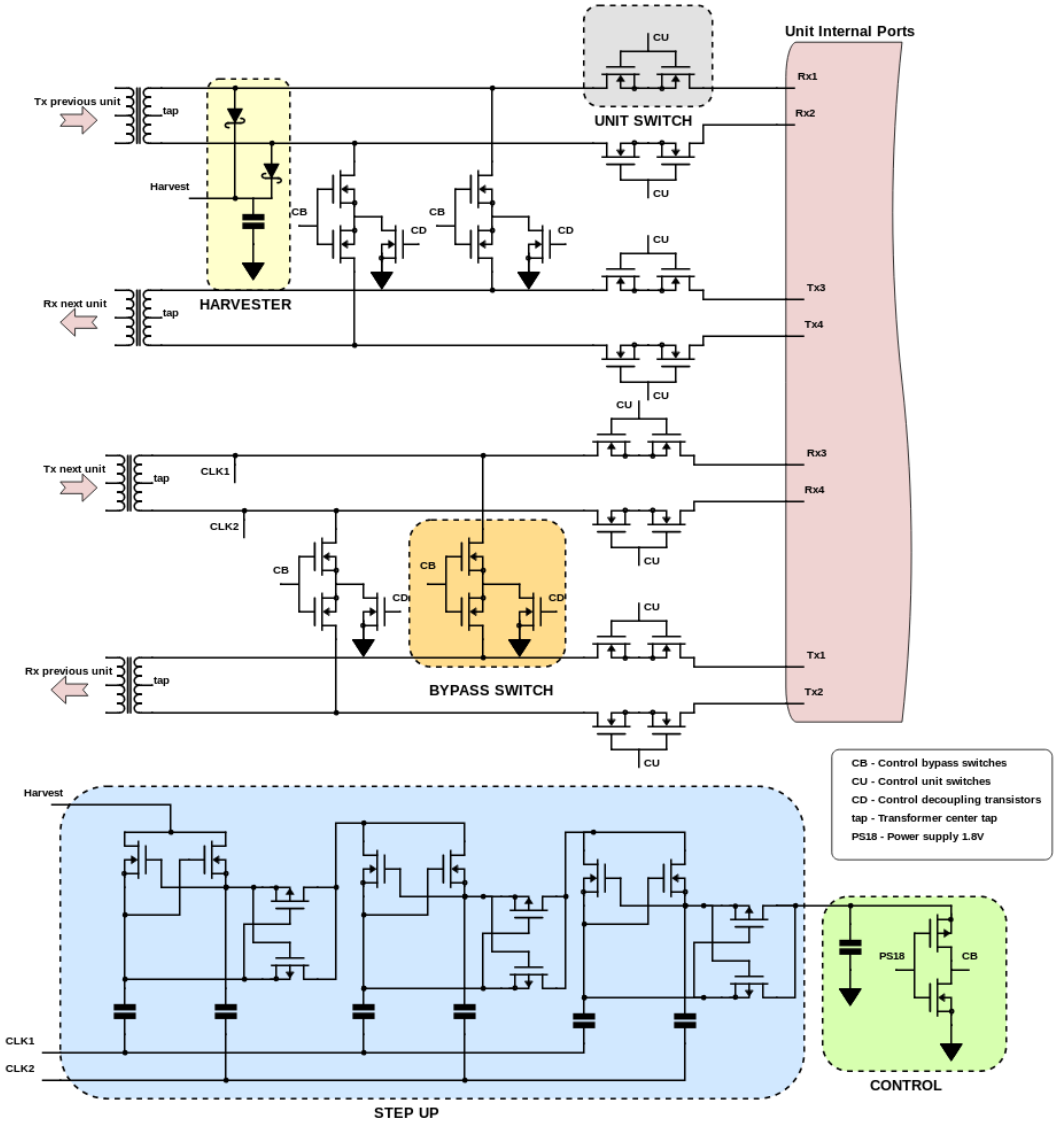

Figure A.2: Complete Schematic of the Ethernet Bypass Switch Circuit Proposed - No Design Improvements Included.

A.1 Simulation Plots

Signal plots for a 40-meter total cable length: working mode [0:50μs], bypass mode [50μs:300μs].

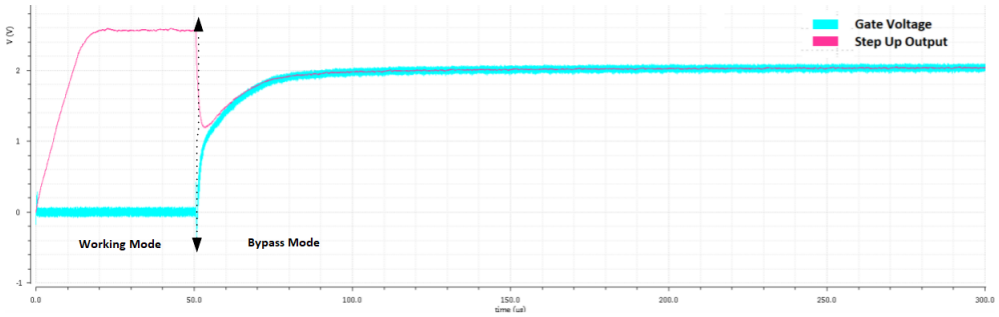

Figure A.3: Gate Voltage and Step Up Output Voltage.

In figure A.4 we can observe the change in the reference level of the signal. The tap node is connected to 1.8 V in working mode and to ground in bypass mode.

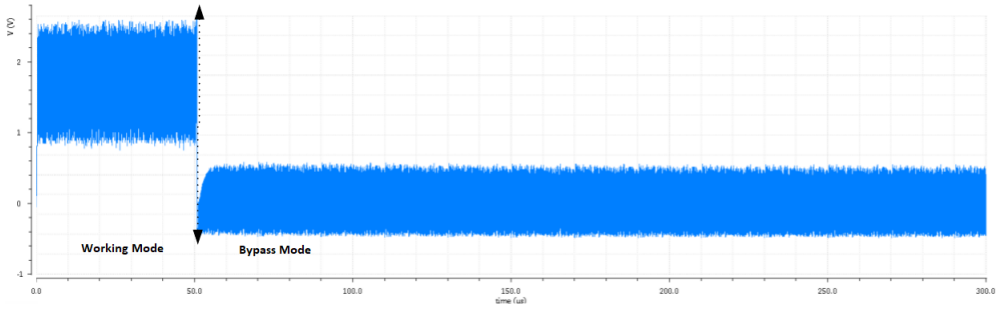

Figure A.4: Example of One Output Transmission Line.

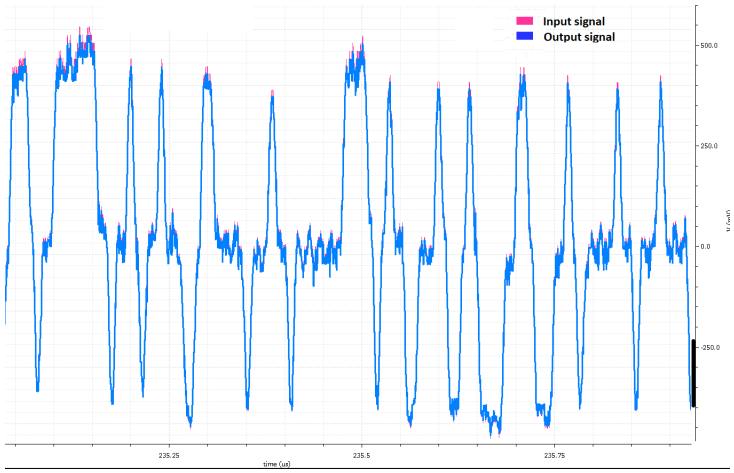

Figure A.5: Input and Output Transmission Line Through Bypass Switch.

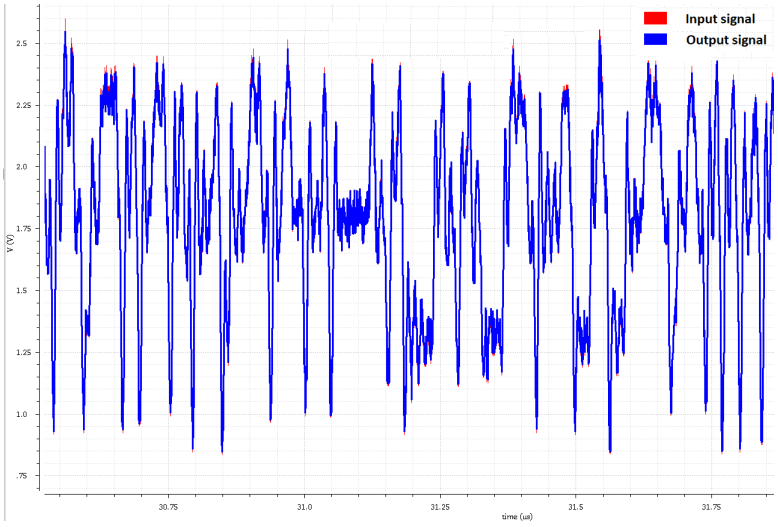

Figure A.6: Input and Output Transmission Line Through Unit Switch.

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