Capacitance Optimization and Ballistic Modeling of Nanowire Transistors

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June 15, 2018

Printed in Sweden
Tryckeriet i E-huset, Lund

Abstract

Downscaling of Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs) has contributed to increased microchip device density and to improve the functionality of the electronic circuits. The dimensions of state of art MOSFET is down to a few nanometers. It has been demonstrated that smaller MOSFETs are faster and more energy-efficient. However, with continued device scaling the performance of ICs starts to deteriorate making it important to implement new technology solutions. Nanowire transistors have in recent years been introduce to face some of semiconductor challenges, such as short-channel effects and performance degradation. The geometry of the nanowires allows the gate contact to be wrapped all-around the nanowire which offers an excellent electrostatic integrity.

However, the performance of nanowire MOSFETs is restricted due to parasitic capacitances and resistances between the metal contacts and semiconductor nanowires. The presence of parasitic capacitances and resistances in devices introduces time delay, which is the time required for charging and discharging the capacitances. Insulating interlayers with high relative permittivity contribute to higher capacitances, and thereby increased time delay. There are amount of materials with low relative permittivity that are suitable to replace the conventionally used spacer material, SiO_2. The high κ-value of SiO_2 is believed to contribute to higher parasitic capacitances, and performance degradation.

Integration of Hydrogen silsesquioxane (HSQ) as an interlayer dielectric in multilevel interconnects has received much attention in semiconductor fabrication. To investigate the possibility of using HSQ as insulating material in nanowire transistors, the properties and the relative permittivity of this material should be explored. Measurement of HSQ κ-value has not been done before and this value has only been speculated. Therefore, a parallel-plate capacitor structure with a varying HSQ-thickness, obtained by using Electron Beam Lithography (EBL), has been manufactured to study the properties of HSQ. Furthermore, the thickness of HSQ has been estimated and CV - characteristics has been considered to measure the κ-value of this material. Experimental measurements on the manufactured structure showed that HSQ is durable as a spacer material, and it has the capability to be used as interlayer dielectric in nanowire transistors. Additionally, the calculated relative permittivity, κ, of HSQ was approximately 3.00 ± 0.40.

Furthermore, this thesis is about investigating the performance of ballistic 1-D MOSFETs at high frequencies, explaining the operational principles of these devices, calculating RF figures of merit, and extracting high frequency transistor metrics, f_T and f_{max}. The simulation in this thesis is based on parameter optimization to find the optimal parameters that give minimized parasitic capacitances and thereby improved transistor performance. To achieve these purposes, 3D-structures have been modeled using COMSOL Multiphysics. The numerical calculations on the modeled 3D nanowire transistor structures demonstrate

a transition frequency $f_T \approx 480$ GHz and maximum frequency $f_{max} \approx 1.60$ THz.

Populärvetenskaplig Sammanfattning

Teknologiutvecklingen inom halvledarindustrin och integrerade krestsar har inom de senaste åren skett i en mycket hög takt, vilket också har medfört en förbättring av transistornas prestanda. Transistorn är grundläggande biståndsdel i elektroniska kretsar med huvudsaklig uppgift att styra strömmar och fungerar på så sätt som ett elektriskt relä. Transistorn består av tre elektroder, som kallas source, drain och gate. Genom att applicera en elektrisk spänning över gate-elektroden, kan resistansen hos kanalen mellan source och drain kontrolleras. På det sättet styrs strömmen genom den elektriska kretsen. Användningsområden för transistorer sträcker sig från förstärkning av elektriska signaler till att bygga logiska kretsar som används för att utföra många, komplexa lösningar.

Nedskalning av transistorer till storleksordning av tiotals nanometer har under de senaste 40 åren bidragit till ökad prestanda av integrerade kretsar. Idag är det möjligt att integrera fler transistorer, upp till miljarder, på ett och samma chip.

Transistorn baserad på halvledarmaterialet kisel, har varit den dominerande inom industrin. Kisel är ett halvledarmaterial som under flera decennier har varit en enastående kandidat till både digitala och analoga applikationer. Kisel är dock ganska ofördelaktig som en elektisk ledare. De fysikaliska begränsningarna hos det materialet har blivit ett hinder inför en fortsatt nedskalning av transistorer och en fortsatt förbättring av transistorns prestanda. Av denna anledning, utforskas det alltjämt konkurrerande tekniker för att överträffa de existerande kiselbaserade kretslösningarna och för att utveckla nya tekniska lösningar.

Forskning och utveckling av transistor baserad på alternativa material och utformningar kan gynna utmaningar vid ytterligare miniatyrisering av transistorer. Ett av alternativen är användande av III-V sammansatta halvledare, främst indiumarsenid InAs eller indiumgalliumarsenid InGaAs. Dessa material har förbättrade egenskaper och kan leda till utveckling av snabba transistor. Detta beror på att elektronerna i dessa material har en hög hastighet i jämförelse med kisel, vilket på sikt bidrar till en transistor med betydligt lägre energiförbrukning.

Användning av III-V halvledare har öppnat nya dörrar för att utveckla nya typer av transistorer som är baserade på nanotrådar. Strömflödet genom kanalen kan bättre kontrolleras eftersom dess cylindriska geometri tillåter gate-kontakten, som lätt kan lindras runt tråden, att ha mer precis kontroll över kanalen. Prestandan av den typen av transistor förväntas ligga i terahertz-området, tack vare kombinationen av dessa innovationer. Trots förbättrad tansistorprestanda, står de nya teknikerna inför nya utmaningar. Därför bör nya lösningar utredas för att kunna uppnå ett optimerat resultat.

I det här projektet har fysikaliska och ballistiska simuleringar av nanotrådstransistor utförs med syftet att uppskatta prestandan och studera kapacitansernas inverkan. Detta har genomförts genom att variera dimensionerna av den modellerade 3D transistorstrukturen.

Dessutom omfattar projektet tillverkning av en platt kondensator som sedan utvärderas. Detta görs i syfte att undersöka möjligheten att ersätta det traditionella isolerande materialet mellan metal elektroderna med andra material som har lägre dielektrik konstant, som till exempel HSQ. På det viset kan man minska påverkan av parasitiska kapacitanser som annars påverkar transistorprestandan negativt.

Acknowledgements

"***Everybody is a genius. But if you judge a fish by its ability to climb a tree, it will live its whole life believing that it is stupid.***"

Albert Einstein

This thesis would not have been possible without the contributions of many people.

Firstly, with all my heart I will thank my family, and specially my mother, for the unconditionally love and endless support. Thank you from the deepest of my heart for being an endless source of inspiration, not giving up on me and always pushing me to achieve my goals and dreams.

I would like to express my gratitude to my supervisors Erik and Adam for their great support and guidance. I would also like to take the opportunity to thank Markus Hellenbrand, together with all members of the nanoelectronics group and lab staff at Lund Nano Lab, who without the work would not be possible.

My sincere gratitude is also dedicated professor Lars-Erik Wernersson for being a great inspiration through my time as a student at Lunds University.

Abbreviations

Al_2O_3	Aluminum oxide
Ar	Argon
CMOS	Complementary metal-oxide-semiconductor
DOS	Density of states
FET	Field-effect transistor
GAA	Gate-all-around
HfO_2	Hafnium dioxide
HCl	Hydrochloric acid
HSQ	Hydrogen Silsesquioxane
ILD	Interlayer dielectric
InAs	Indium arsenide
InGaAs	Indium gallium arsenide
ITRS	International technology roadmap for semiconductors
MOSFET	Metal-oxide-semiconductor field effect transistor
N_2	Nitrogen
NW	Nanowire
QCL	Quantum capacitance limit
RC	Interconnect delay
RF	Radio frequency
Si	Silicon
SiO_2	Silicon dioxide
Ti	Titanium
TMAH	Tetramethylammonium hydroxide

UV	Ultraviolet lithography
W	Tungsten

Physical constants

ε_0	vacuum permittivity	$8.854*10^{-12}$ F/m
k_B	Boltzmann's constant	$8.617*^{-5}$ eV/K
q	elementary charge	$1.602*10^{-19}$ C

Symbols

A	area	m^2
C_{ox}	intrinsic oxide capacitance	F/m^2
C_{gd}	gate-drain capacitance	F/m^2
C_{gs}	gate-source capacitance	F/m^2
C_L	load capacitance	F/m^2
C_{gs}	quantum capacitance	F/m^2
D_{it}	density of interface traps	m^{-3}
E_c	conduction band energy	eV
E_F	Fermi level	eV
f_t	cut-off frequency	Hz
f_{max}	maximum oscillation frequency	Hz
g_d	output conductance	S
g_m	transconductance	S
I_{ds}	drain-source current	A
I_{on}	on-state current	A
L_g	gate length	m
m^*	effective electron mass	kg
N_d	donor doping concentration	m^{-3}
n_{1D}	1-D carrier density	m^{-3}
Q	quantum charge	C
V_{ds}	drain-source voltage	V
V_{gs}	gate-source voltage	V
V_t	threshold voltage	V
R_{nm}	nanowire resistance	Ωm
R_d	drain resistance	Ωm
R_g	gate resistance	Ωm
R_c	access resistance	Ωm
R_s	source resistance	Ωm
ε_r	relative permittivity	-

κ	relative permittivity	-
μ_e	electron mobility	$\mathrm{cm^2V^{-1}s^{-1}}$

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CHAPTER 1

Introduction

Moore's law states that the number of transistors in a dense integrated circuit (IC) will roughly be doubled every two years via geometrical downscaling [1]. Downscaling of transistors has been the most popular approach since it allows for increasing the packing density of metal-oxide-semiconductor (MOS) transistors. Nonetheless, continued device scaling contributes to an increase in dissipated power, limiting the performance of the integrated circuits [1]. Scaling of silicon transistors has reached its limits. Therefore, it is important to turn attention to other materials and technologies to address these problems, and to achieve enhanced circuit performance [2].

Over the past few decades, improved performance of the planar MOSFET transistors has mainly been achieved by reducing the size of transistors to increase the packaging density. This has been achieved by implementing more transistors, up to milliard, onto a small chip. Continued downscaling of transistors gives rise to some unwanted issues which for example can be related to short channel effects (SCEs) and signal delay [1].

III-V based field-effect transistors are among the promising candidates to enhance transistor performance, and to extend the International Technology Roadmap for Semiconductors (ITRS) [3]. InAs and InGaAs have been among the most interesting semiconductor materials in research, due to the enhanced electron transport properties; high electron velocity and injection velocity [5, 6]. By combining silicon innovations with other novel innovations such as nanotechnology and integrating them onto the silicon platform, downscaling of transistors is expected to continue and with an improved performance. In the last decade, good progress has been made in exploring nanowire-based transistors. The cylindrical gate geometry of nanowires results in an improved electrostatic control and decreased current leakage [4].

Device scaling and increased device packing density require a larger number of interconnects, to connect the devices together in the integrated circuit. This results in an increase in wiring density. The main disadvantage of having a large interconnect wiring density is increased signal delay, resistance-capacitance time delay, RC, and power dissipation [57]. Although feature size downscaling provides an improved device speed, the interconnect delay can constitute a major fraction of the total delay. This will result in devices with limited performance [7, 8].

Fabrication process of the multilevel interconnections includes spin coating of thin oxide films. The conventionally used insulating material has been based on silicon-based polymer solutions, such as SiO_2 [36]. An improved microprocessor performance can be

achieved by for example reducing the circuit signal delay. This is achieved by replacing the traditionally used insulator films with materials of a lower relative permittivity (low-κ materials). One of the current leading low-κ materials is hydrogen silsesquioxane (HSQ). Due to the excellent planarization properties and gap-filling capability of this material, it has been extensively used in semiconductor fabrication [9].

The purpose of this thesis is to investigate the properties of HSQ and to estimate the κ-value of this material. The expected value of HSQ is 3.00-9.00. Furthermore, the thesis intends to study the performance of nanowire transistors by numerical calculation and modeling of 3D structures. The insulating material between the metal contacts of these vertical transistors is assumed to have κ-value between 2.00 and 3.00, for the best optimized structure. First-principles calculations constitute a valuable tool to achieve a greater understanding of the behavior of nanowire transistors without requiring empirical data. An exact measurement of HSQ κ-value has not been done before, and there is a relatively little measurement data available. To study the possibility of replacing the conventionally used insulating material in nanowire transistors with HSQ, the simulation performed in this thesis is particularly interesting. Performance improvement will be based on parameter and material optimization.

The remainder of this thesis is structured as follows. In Chapter 2 - Transistor Theory, two types of transistors are introduced and some important operational principles are explained. In Chapter 3 - Ballistic 1-D Transistors, analytical theory behind the performance of 1-D MOSFETs is considered. In Chapter 4 - RF-Transistors, numerical calculation of RF metrics of nanowire transistors is performed. Moreover, issues associated with these devices are explained, and how this thesis intends to solve them based on parameter optimization is discussed. In Chapter 5 - Manufacturing Process, properties of HSQ are investigated and the κ-value of this material is calculated based on thickness-measurement and CV - characteristics. In Chapter 6 - Result and Analysis, the results obtained from the simulation part and from the experiment part are presented and discussed. In Chapter 7 - Conclusions and outlook, a summary of the thesis is given together with suggested future improvements.

CHAPTER 2

Transistor Theory

This chapter introduces the theory of two types of transistors and explains some important concepts associated with these devices.

2.1 Planar MOSFET

Metal oxide semiconductor field-effect transistor is the most common type of transistor. It can be used as a switch and also to amplify signals in electronic devices. Being the most common transistor, MOSFET has been used in both analog and digital circuits. In the last decades, MOSFET has developed quickly and nowadays it is the most important device for advanced integrated circuits. This is due to the unique features of this transistor, mainly low-power consumption and high manufacturing yield [10].

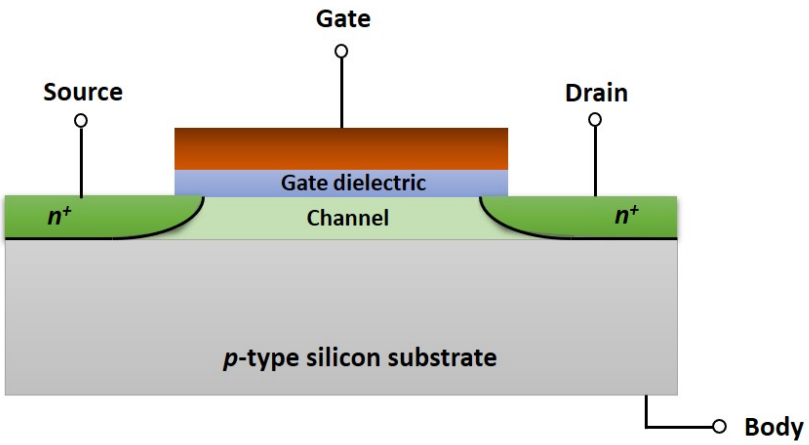


Figure 2.1: A schematic overview of a planar n-type MOSFET, with highly doped source and drain regions.

Traditionally, MOSFET is composed of a MOS capacitor and two pn - junctions placed adjacent to the MOS capacitor, as illustrated in Fig.2.1. This transistor comprises four different terminals, source (S), gate (G), drain (D) and body (B). The active region of MOSFET is called channel, along which the charge carries; electrons or holes, flow from the source to the drain. MOSFET works by electronically changing width of the channel,

which is controlled by the gate terminal. An extremely thin insulating layer of gate oxide separates the gate contact from the channel. Besides, this layer provides a good insulation by preventing current leakage through the channel [11].

The operation regimes; namely accumulation, depletion and inversion, describe the state of the charge carriers in the channel under different bias conditions. During accumulation, the majority carrier charges, electrons in n-type transistors and holes in p-type transistors, are induced at the interface between the semiconductor and the oxide. In the depletion region, the majority carrier charges are *depleted* or greatly reduced. By applying a gate bias above a certain threshold voltage V_T, new minority charge carries start to generate, creating an inversion charge layer at the semiconductor-oxide interface. When the number of minority carriers at the surface is greater than the majority carriers, inversion mode is obtained [11].

The current through the channel, I_{DS}, is controlled by source and drain terminals situated at the two ends of the channel. The amount of charges in the channel depends on the height of the energy barrier between the channel and source/drain contact. For n-type transistors, the current is small or approximately zero if the applied gate voltage is below the threshold voltage, as shown in Fig.2.2 (a). While having a gate voltage above the threshold voltage makes it possible for the electrons to pass from the source to the drain through the channel, as illustrated in Fig.2.2 (b) [12].

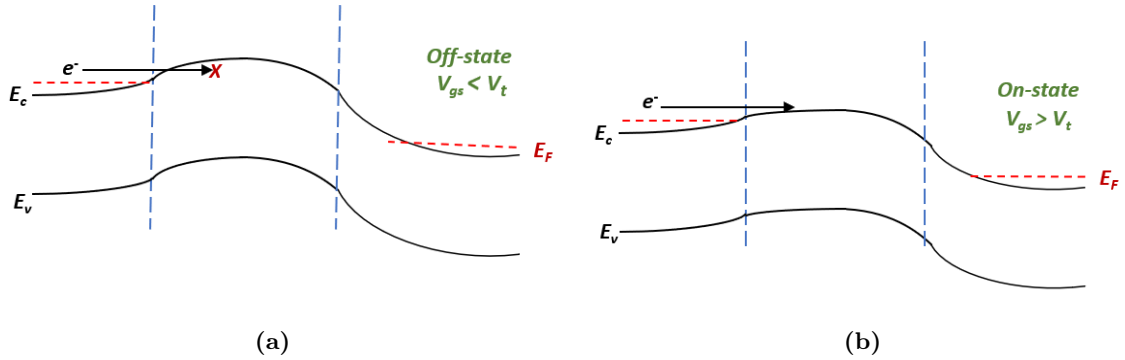


Figure 2.2: MOSFET band simulation. (a) Off-state, the thermionic emission of electrons is blocked by the potential barrier, no conducting channel is created as $V_{gs} < V_t$. (b) On-state, MOSFET operates above threshold voltage which results in electrons flow across the channel.

MOSFETs offer low leakage current, mainly due to the insulating gate oxide film at the MOS interface [43]. Having a low off-state leakage is one of the most efficient approach to maintain higher energy-efficiency in digital circuit. The oxide insulator plays an important role in controlling the performance of MOSFETs by blocking the flow of the current through the gate contact. The gate oxide capacitance per unit area [F/m^2] is given by

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{2.1}$$

where ε_0 is the vacuum permittivity, ε_r relative permittivity of the gate oxide and d is dielectric insulator thickness. According to this expression, the gate capacitance is

increased as the thickness of the gate dielectric film is reduced. Having a very thin dielectric film might result in some issues. Thin films give rise to increased gate-leakage current, which is related to quantum mechanical tunneling through thin layers [13]. Therefore, improved transistor performance can be achieved by, for example, replacing SiO_2 with high-κ oxides such as HfO_2 or Al_2O_3. The main advantage of applying these materials is the good ability to preserve the electrostatics coupling to the gate. In addition, gate leakage and tunneling effects are circumvented by keeping the oxide film thickness constant or relativity thick ($\sim$ nm). Doing so, a capacitance equal to that for devices with thiner gate oxide is obtained [14].

2.2 Vertical MOSFET

Nanometer-scale devices, that are based on quantum or single-electron, are becoming the most promising devices for future electronics generation [15]. The performance advantages of vertical MOSFETs in comparison to their planar contender is making them a viable option to extend the International Technology Roadmap for Semiconductors.

Transistor downscaling has forced the researchers to find new technology solutions to change the gate structure from planar configuration to a more complex 3D structure. This technology makes it possible to avoid undesirable problems inherent in minimization, such as short channel effects and high off-state leakage [16].

The cylindrical geometry of nanowire offers an excellent electrostatics control over the channel, as for example in gate-all-around configuration. The channel is extended in the vertical dimension and the gate electrode is wrapped all-around the nanowire. This contributes to an increased electrostatics, and hence an improved performance. Furthermore, this technology allows for further scaling of the gate length, L_g, due to the excellent electrostatics of this configuration.

Moreover, the vertical geometry offers a unique possibility for more easily relaxation between different crystal planes (lattice constant), resulting in a greater opportunity to create compounds of different materials, so called heterojunctions [56]. Introduction of high mobility III-V channel materials in a transistor structure is making it possible to achieve an enhanced device performance and reduced power dissipation [18]. Besides, the vertical geometry allows for small footprint, decoupled from the gate-length [19].

2.2.1 Transistor Structure

A cross-sectional layout of a vertical nanowire MOSFET structure is illustrated in Fig.2.3. The structure of the vertical nanowire FETs is typically constructed as an array of nanowires arranged perpendicularly to the substrate. The number of nanowires per array is ranged from a single nanowire up to a few hundred, depending on the desired transistor performance. A high-κ oxide is implemented on the III-V nanowire to increase the electrostatic coupling to the gate [20].

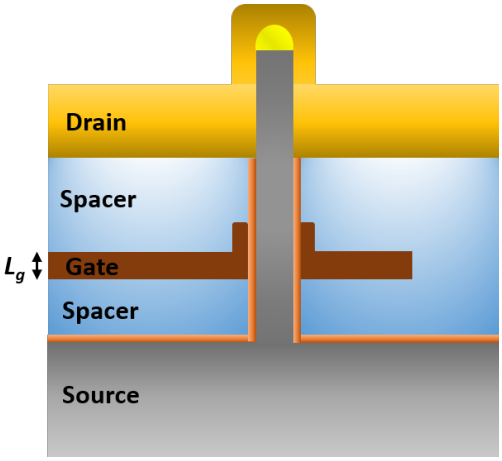


Figure 2.3: A cross-sectional layout of a nanowire transistor, with the gate electrode warped around the wire. A high-κ oxide material covers the entire nanowires, shown here in orange. Source and drain contacts are arranged at the bottom and the top of the nanowire, respectively. L_g corresponds to the gate length. The structure is embedded in an insulating material, shown in blue.

The width of the gate in gate-all-around configuration is defined as the circumference of a single nanowire. To improve the drive current, the number of nanowire per array can be changed, and therefore there is no need of scaling the wire diameter to increase gate width.

The metal contacts in the gate-all-around architecture - gate, source and drain - are vertically stacked on top of each other. The contacts are separated by a spacer insulator material. Ideally, the spacer material should have a low relative perimittivity in order to prevent electronic cross-talk and large parasitic capacitances. Furthermore, the spacer material should be mechanically and thermally stable to withstand further processing, and to increase the ability of controlling the thickness of the deposited film.

2.3 Dielectric Materials

Dielectrics or electrically insulated materials are defined as non-conductors of electricity or as materials with high resistance. This is associated with the large band gap offered by these materials, for example, 1.12 eV for Si compared to 8-9 eV for SiO_2 [21]. Studying the dielectric properties of various materials used in semiconductor fabrication is needed to achieve a greater understanding of the desired circuit performance.

Relative permittivity, ε or κ, is an important property used to measure the ability of the material to be polarized in an external electric field. The capacitance, which is the ability of the material to hold charge, depends on the permittivity of the material, as expressed in equation (2.1). In some materials, such as polymers, the permittivity is defined as a function of frequency, $\varepsilon(\omega)$ [58].

There are two types of dielectrics, categorized based on material permittivity. Dielectrics with low permittivity, low-κ, are defined as materials with low ability to polarize. Low-κ materials are good insulators and provide an excellent insulation between conduc-

tors. Therefore, these materials are used in multilevel ICs when coupling between dense metal layers is suppressed [7]. For this reason, these materials can be used as interlayer dielectrics (ILDs) between two metal interconnections, source-gate or gate-drain in vertical FETs. The high non-conduction properties of these materials have made them prominent in preventing the passage of electric current through the insulating layer [22].

The second type of dielectrics is high-κ materials, which have a high permittivity and good ability to polarize and hold charge. For further improvement of transistors, the thickness of SiO_2 should be small which contributes to severe leakage problems. To tackle these challenges, SiO_2 can be replaced with high-κ materials. The high κ-value of these materials allows for use of a thicker gate oxide, while obtaining a capacitance equal to that of devices with thinner insulating material, as states in equation (2.1).

One example of spacer materials that has been used as interlayer dielectric is organic spacer material. However, using organic materials has difficulties regarding thickness scaling as well as thermal stability. Organic photoresists, such as S1813 or BCB, or inorganic films, such as SiO_2, Si_2N_4 or HSQ are typically used as spacer materials. This is due to the improved mechanical stability of these materials, and their ability to withstand higher temperatures. Air spacer can be considered as the best spacer due to its low relative permittivity, close to 1. Although, using air as spacer material can result in mechanically unstable structure.

Silicon dioxide, SiO_2, has been the most common material to be used as insulating material. Nonetheless, one of the major problems of using SiO_2 is the high κ-value of this material. According to equation (2.1), high κ results in a high parasitic capacitance. Therefore, it is important to find other insulating materials with a lower κ-value. Hydrogen Silsesquioxance is a low-κ material that has been utilized for planarization in integrated circuits. The good properties of this material, make it a good candidate to be used as a spacer material between the metal contacts in vertical nanowire transistors.

Replacing the SiO_2 with materials of a different κ-value is a complicated technology. The properties of the material should be comparable to those of SiO_2. Stability under thermal conditions, low thermal expansion and diffusion coefficients are examples of some material requirements that should be considered [7].

2.3.1 Hydrogen SilsesQuioxane

Hydrogen silsesquioxane ($H_8Si_8O_{12}$) is indicated as polyhedral oligomeric silsesquioxane, and is commercially available in solution as FOX, Flowable Oxide. HSQ ranges as one of the simplest member of the family of spherosiloxanes oligomers. There is a ratio between the two structures of HSQ, so called cage and cross-linked structure [23], illustrated in Fig.2.4 , where the cage structure is dominated.

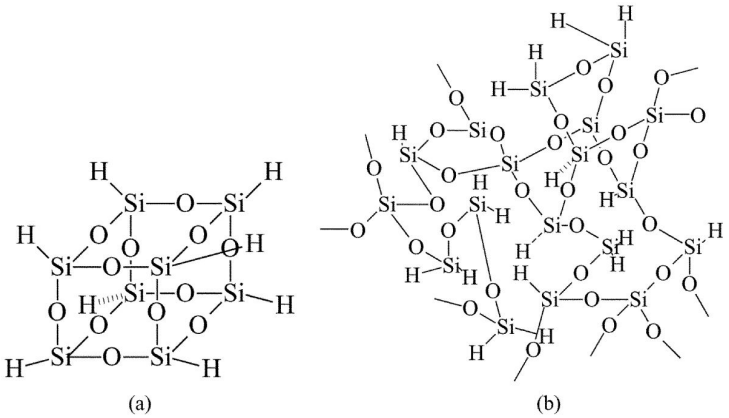


Figure 2.4: The two common structures of HSQ. (a) The monomer or cage structure for an eight-corner oligomer (b) Cross-linked or network form, with some intermediate species involved. The picture is taken from [59].

The non-networked or caged HSQ structure consists of bonding arrangement with Si=H groups. Si atoms sit at the cubic structure corners, forming bridges between three oxygen atoms. Combination of structures with 8 corner oligomer and others with up to 16 corners has been synthesized. The ratio between the two states or structures of HSQ is not constant and changes depending on different fabrication processes [24, 25].

Upon electron-beam irradiation and after treatment of HSQ by heating, silicon hydrogen (Si=H) bonds, which are weaker than SiO bonds, break and additional bonds between the monomer cages are formed. This results in converting the cage structure into a network structure. The physical properties of the network structure are similar to those of SiO_2. The cross-linking, required for negative tone pattering, is generated consequently. Due to the presence of absorbed moisture in the film, Si=H bonds convert into silanol (Si-OH) groups that subsequently form Si-O-Si bridges at the corner, as shown in 2.4 (b) [26]. The unstable silanol groups condense easily, leading to structure breakage and converting the caged molecule into a linear network [27].

HSQ is a low-κ material with low viscosity, providing an excellent gap-filling capability and planarization properties [28]. Furthermore, HSQ is durable and can withstand high processing temperatures. For these reasons, integration of HSQ as an interlayer dielectric in multilevel interconnects has received much attention in semiconductor fabrication [29]. After spin-coating of HSQ on the substrate and thermal heating, it transforms into silicon dioxide, as previously mentioned. The curing temperature is a crucial step through the development procedure of HSQ, since it determines the final HSQ-thickness. Furthermore, it has been demonstrated that the final thickness of HSQ can also be obtained by electron exposure dose in electron-beam lithography (EBL) [30].

2.4 RC Interconnects Delay Time

Over the past few decades, performance improvement of microelectronic integrated circuits (ICs) has been achieved by reducing the size of device features, from 1 μm to a few nanometers. This has resulted in making the ICs faster and with an operational frequency

in GHz-range. With continued downscaling of integrated circuits, the performance of these circuit is starting to deteriorate. Performance degradation is mainly due to the increased signal delay originates from the dense interconnect wiring between transistors [31].

The switching speed of MOSFETs is expected to increase as the device dimensions shrink. This results in decreasing the transit time of the carrier across the channel. The intrinsic gate delay is not the only contributory factor in controlling the effective speed of the device, but also the signal propagation through the metal interconnects.

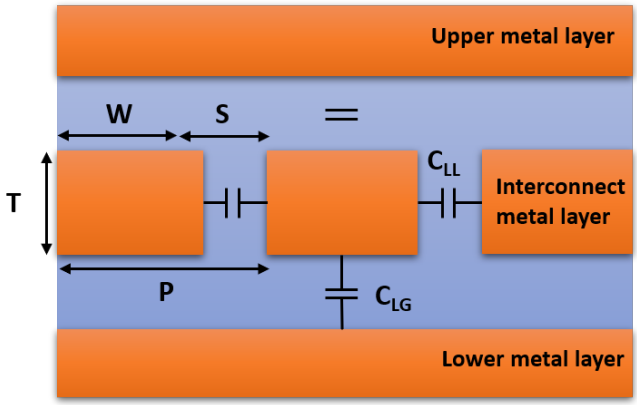


Figure 2.5: A schematic view of an interconnect element, capacitance, embedded in a dielectric material (in blue). This schematic overview includes three lines of length T that run in parallel with each other. The capacitance C_{LL} couples two lines to each other.Capacitance C_{LG} represents the line-to-ground capacitance.

A model of an interconnect circuit is illustrated in Fig.2.5. W represents the line width, T is the line or wire thickness, S is the spacing between two lines or so called interconnect length, and P represents the line pitch. C_{LL} and C_{LG} refer to the contribution of the capacitances from line-to-line and from line-to-ground, respectively. The former mentioned affects both the wiring delay and crosstalk noise, while the second one exclusively affects wiring delay [54].

Resistance-capacitance time delay, RC, is an important figure of merit to characterize the interconnection delay. This time delay can be represented as a series of wires (resistances) and insulating layers between the wires (capacitances). Device downscaling is realized by shrinking the size of transistors to bring the transistors in the device closer together. This can consequently contribute to an increase in the RC interconnect delay time. RC is expressed by equation (2.2) [33].

$$RC = 2\rho\kappa\varepsilon_0\left(\frac{4L^2}{P^2} + \frac{L^2}{T^2}\right) \tag{2.2}$$

C is the total interconnect capacitance which is given as $C = C_{LG} + 2C_{LL}$, while ρ represents the metal resistivity and κ is the relative permittivity. According to this equation, the time delay increases quadratically with decreased feature size.

The ongoing development in device processing requires shrinking of device dimensions, thus the usage of multiple metal interconnections becomes more common in manufacturing semiconductor devices. However, this design approach limits the performance of high-speed

logic chips. That is due to increased time delay originated from the dense interconnects [34].

The signal through the metal interconnects has the ability to limit the improvement of device performance. This effect becomes more prominent as the dimensions shrink to a few nanometers. Reduced RC delay time can be obtained by replacing the current interlayer dielectric film, silicon dioxide, with low-κ materials. Hydrogen silsesquioxane is among the most promising candidates of porous materials to be used as dielectric interlayer at 14 nm technology.

CHAPTER 3

Ballistic 1D Transistors

Miniaturization of transistors enabled a success in fabricating devices and circuits with high operation frequency. As the demand on high frequency electronics increased, and as the silicon transistor scaling is now reaching its limits, the attention is turning to improve the performance of non-Si electronic materials and non-planar structures [47].

A great progress in studying carbon nanotubes (CNT), semiconductor nanowires and III-V materials has been obtained [48]. III-V materials can be used as channel in for example nanowire transistors, replacing the traditionally used material, silicon. The high electron mobility and injection velocity of these materials together with the improved electrostatics of nanowire-based transistors allow for further gate scaling and better transistor performance [31, 35].

Nanowire transistors can be integrated into CMOS logic. The high-performance and low-power of such logic transistor applications should frequently be benchmarked against the existing Si logic transistor [36].

A theory to characterize ballistic 1-D MOSFETs has been developed by M. Lundstrom and others [37]. The objective of this chapter is to understand the analytical theory behind ballistic 1-D MOSFETs.

3.1 Theory of Ballistic 1-D MOSFETs

Ballistic MOSFET can be illustrated as two thermal equilibrium electron reservoirs. The first reservoir is due to source-injection, while the second one is due to drain-injection under low drain bias [36]. These electron reservoirs are separated by an energy barrier whose height is modulated by the gate voltage, V_{gs} [38].

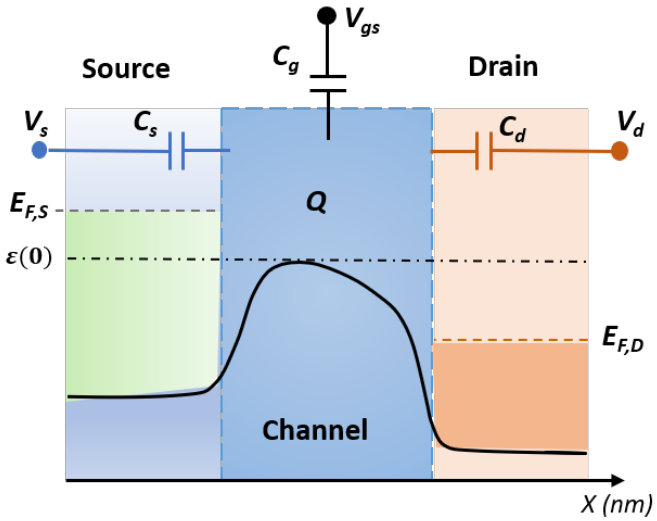


Figure 3.1: Conduction band diagram of a MOSFET. The transistor is modeled as a structure consisting of three capacitors with a channel charge of Q.

As it is depicted in Fig.3.1, the Fermi level at the source side is defined as $E_{F,S}$ and at the drain side as $E_{F,D} = E_{F,S} - qV_{DS}$. The height of the energy barrier between the source and the channel is modulated by the gate voltage, while the drain bias has a small effect. Reducing the height of the barrier results in an increased current flow, since this is directly controlled by carriers injection across the barrier.

Assuming occupation of only one sub-band, the total current induced as the carriers inject from each side into the other can be described as $I_{DS} = I^+ - I^-$, where

$$I^+ = \frac{q^2 k_B T}{\pi\hbar} F_0(\eta_F), \tag{3.1}$$

$$I^- = \frac{q^2 k_B T}{\pi\hbar} F_0(\eta_F - U_D) \tag{3.2}$$

k_B is Boltzmann's constant, T represents the temperature, $\eta_F = \frac{E_F - \varepsilon(0)}{k_B T}$, which measures the location of Fermi level with respect to the conduction band edge, also so called reduced Fermi energy. $U_D = \frac{qV_d}{k_B T}$ and F_0 is the zeroth order Fermi-Dirac integral.

The potential at the top of the barrier is determined from the solution of Poissons equation for three-capacitor system. This system represents the effect of the three terminals; gate, drain and source, on the potential of the barrier. An equivalent system is illustrated in Fig.3.1. The potential at the top of the barrier is defined as

$$-\varepsilon(0) = \frac{C_g}{C_\Sigma} qV_g + \frac{C_d}{C_\Sigma} qV_d + \frac{C_s}{C_\Sigma} qV_s - \frac{Q}{C_\Sigma} q \tag{3.3}$$

where the bias-induced charges or so called local density of states at the top of the barrier, Q, are included. C_Σ is the sum of the parallel coupled capacitances, C_g, C_s and C_d. C_g is

the intrinsic gate capacitance, and is defined as a sum of the parallel coupled capacitances, C_{ox} and C_Q.

$$C_g \approx \frac{C_{ox}C_Q}{C_{ox}+C_Q} \tag{3.4}$$

C_{ox} is the gate oxide capacitance, that is determined by the geometry of the considered device. C_Q represents the quantum or semiconductor capacitance. C_g can also be defined as the total gate capacitance (per unit gate length), C_{gg}.

Ballistic 1D Current

The operation regimes of all transistors can be divided into two categories; the charge controlled or classical limit (CL) and the band controlled or quantum capacitance limit (QCL). The simulations and numerical calculations in this thesis are mainly performed in the QCL regime. This regime is achievable by 1-D nanowire MOSFETS due to their unique scaling potential regarding oxide thickness, body thickness, and channel length.

Under certain assumptions, calculation of the current in the cylindrical nanowire can be simplified. By considering three regions of operation, three equations of I_{DS} can therefore be derived. For simplicity, the following considerations have been taken into account:

- High degenerate condition, meaning $\eta_F \gg 1 \Rightarrow F_0(\eta_F) \Rightarrow \eta_F$
- Studying the scaling behavior of the transistor in quantum-capacitance limit (QCL), where $C_{ox} \gg C_Q \Rightarrow C_g \approx C_Q$. In the QCL, the potential inside the channel is determined by the gate potential suppressing the short channel effects [49].
- Considering operation in the active region of the transistor, above threshold voltage, where $E_{F,D} < \varepsilon(0) < E_{F,S}$. This menas that the channel is occupied only by carriers from the source reservoir, leading to $I^- = 0$. I_{DS} is independent of V_{ds} and it increases linearly with the applied bias voltage, V_{gs}.
- Assuming electrostatically well-designed transistor with $C_g = C_{geo} \gg C_d$, C_s. According to that, equation (3.3) can be rewritten as $\varepsilon(0) = -qV_{gs}$.

Following these considerations, I_{DS} can be defined as

$$I_{DS} = \frac{2q^2}{h}\eta_F \approx \frac{2q^2k_BT}{h}(E_F - \varepsilon(0)) = \frac{2q^2}{h}(E_F + qV_{gs}) \tag{3.5}$$

q is the elementary charge and h is Planck's constant. The equation is expressed for one sub-band.

3.2 Quantum Capacitance

The potential within the channel is determined by the gate voltage in the quantum capacitance limit (QCL). This is assumed since nanowire transistors are expected to operate in

the quantum limit as they are downscaled into a few sub-bands regime. Equation (3.4) is approximated to $C_{gg} \approx C_Q$ in the quantum limit, as $C_{gg} \gg C_Q$. Quantum (or semiconductor) capacitance is gate-voltage-dependent, and is evaluated from

$$C_Q = \frac{\partial Q_g}{\partial V_{gs}} = \frac{\partial}{\partial V_{gs}}(L_g N_{1D} F_{-1/2}(\eta_F(V_{gs}))) \tag{3.6}$$

where $N_{1D} = \frac{\sqrt{2m^* k_B T/\pi}}{\hbar}$, is the one-dimensional effective density of states, Q_g is the charge carriers in the channel, and $F_{-1/2}(\eta_F)$ is the Fermi-Dirac integral of order -1/2.

$$F_{-1/2}(\eta_F) = \frac{1}{\sqrt{\pi}} \int_0^\infty \frac{\varepsilon(0)^{-1/2}}{1 + e^{\varepsilon - \eta_F}} d\varepsilon \tag{3.7}$$

m^* is the effective mass of the semiconductor. The index of Fermi-Dirac integral indicates the dimension of the semiconductor. Accordingly, an index equals to -1/2 corresponds to one dimensional semiconductor.

Fermi-Dirac integrals have the property that [47]

$$\frac{dF_j}{d\eta_F} = F_{j-1} \tag{3.8}$$

Equation (3.6) can therefore be given by

$$C_Q = \frac{N_{1D}}{2k_B T} F_{-3/2}(\eta_F) \tag{3.9}$$

3.3 Ballistic Transconductance

Transconductance, g_m, is an important performance metric in RF applications as it expresses the efficiency of the gate voltage to modulate the energy barrier of the channel. g_m is defined as partial derivative of the drain current with respect to gate voltage

$$g_m = \frac{\partial I_{DS}}{\partial V_{gs}} \tag{3.10}$$

In the active device region, and in the quantum capacitance limit, $C_{ox} \gg C_Q$, g_m is obtained by derivation of equation (3.5). Following the assumptions listed in section 3.1 gives

$$g_m = \frac{2q^2}{h} \tag{3.11}$$

The channel transconductance is, indeed, independent of the gate bias as equation (3.11) states [39].

Fully ballistic transistor are assumed. However, truly ballistic devices are difficult to achieve in reality due to scattering in the channel. Modeling quasi-ballistic devices, devices with some amount of scattering, is therefore preferred to obtain an accurate analysis of device performance.

CHAPTER 4

RF-Transistors

The objective of this chapter is to explore the radio frequency (RF) performance of nanowire transistors. An optimized vertical FET layout is first considered and finite-element modeling software, COMSOL Multiphysics, is used. Performing this simulation is important to emphasize the impact of parasitic capacitances and resistances on transistor performance. RF figures of merit; h_{21}, U, MAG and MSG, are defined by deriving explicit expressions using admittance (Y) parameters. To estimate these parameters two-port network is considered during the calculation. The two most important metrics for transistors are unity current gain frequency, f_T, and maximum power gain frequency, f_{max}. These are determined from the hybrid-π small-signal model. Ideally, these frequencies should be large in order to achieve RF applications with high operational frequency.

4.1 Simulation details

4.1.1 Device Structure

Fig.4.1 (a) illustrates a cross-sectional layout of a nanowire FET structure. A model similar to this structure has been modeled using COMSOL Multiphysics. This structure consists of two rows of semiconductor arranged in a triangular fashion as shown in Fig.4.1 (b), forming transistor unit cell of width of $2(r_{nw} + t_{nw}) + w_s$. The distance between two nanowires is represented by w_s, as illustrated in Fig.4.1 (a) and Fig.4.2. According to [35, 39], the triangular arrangement of nanowires allows for less complicated fabrication methods, Moreover, this configuration results in lower gate resistance in comparison to hexagonal patterns.

The extrinsic and intrinsic capacitances are also included in the structure, together with the specific contact resistance, R_c, and the nanowire resistances, R_{nw}.

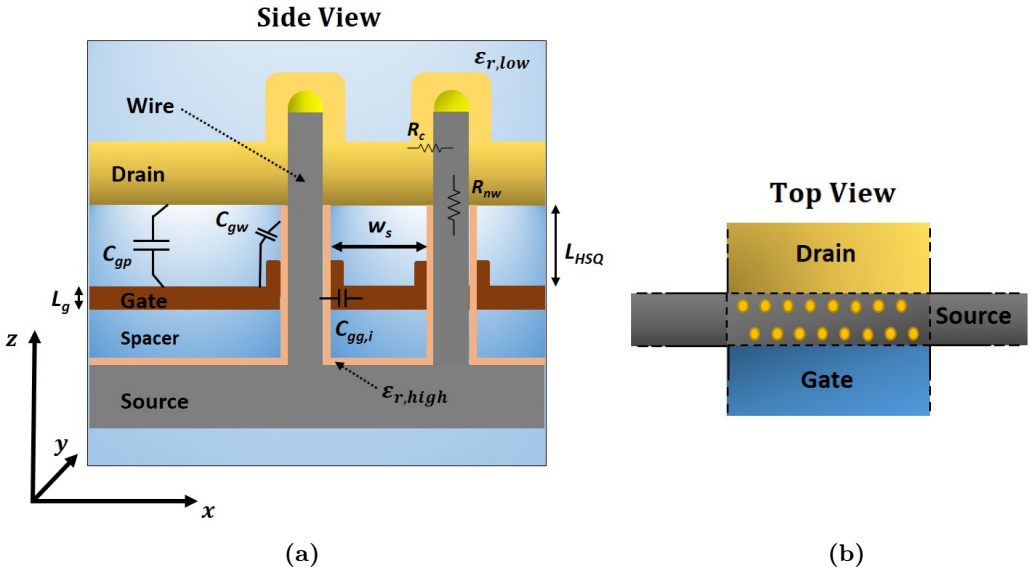


Figure 4.1: A schematic side view illustration of the modeled nanowire FET structure including the extrinsic capacitances (C_{gp} and C_{gw}), intrinsic gate capacitance, $C_{gg,i}$, contact resistance, R_c, and the nanowire resistance, R_{nw}. The entire structure is embedded in low-κ material, where L_{HSQ} is the distance between two metal contacts. (b) A Top view of a 2D device structure, illustrating the electrode configuration, as well as the triangular arrangement of the nanowire array.

The nanowires are assumed to be heavily doped and here to be considered as metallic leads. The nanowires are covered with high-κ oxide, $\varepsilon_{r,high} \approx 20.0$, and with an oxide thickness of t_{ox}. The relatively thick high-κ oxide films solve the gate leakage issues by preserving the electrostatics. The gate-contact is symmetrically arranged in the center of the nanowire. L_{HSQ} depicts the equal separation distance between the gate-source and gate-drain. Source and drain contacts are patterned along the nanowires. The device is embedded in a large box of a low-κ material with a relative permittivity of $\varepsilon_{r,low} \approx 3.00$. This means that the spacer material has same κ-value as that for embedding material.

4.1.2 Numerical Modeling

3D finite element method (FEM) solver (COMSOL Multiphysics) is used to obtain quantitative values of the extrinsic capacitances of the modeled transistor unit cell illustrated in Fig.4.2. To obtain a deeper understanding of how the transistor structure is best optimized, three structures have been modeled during this thesis. The obtained results from the numerical calculation of parasitic capacitances, $C_{gs,p}$ and $C_{gd,p}$, and intrinsic gate capacitance, $C_{gg,i}$, are normalized to one nanowire. Sections (3.2) and (4.2.2) provide further explanation of the origin of these capacitances.

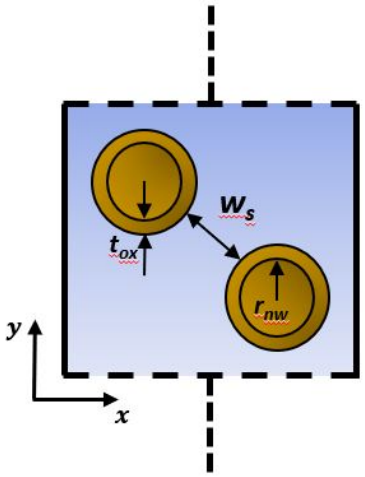


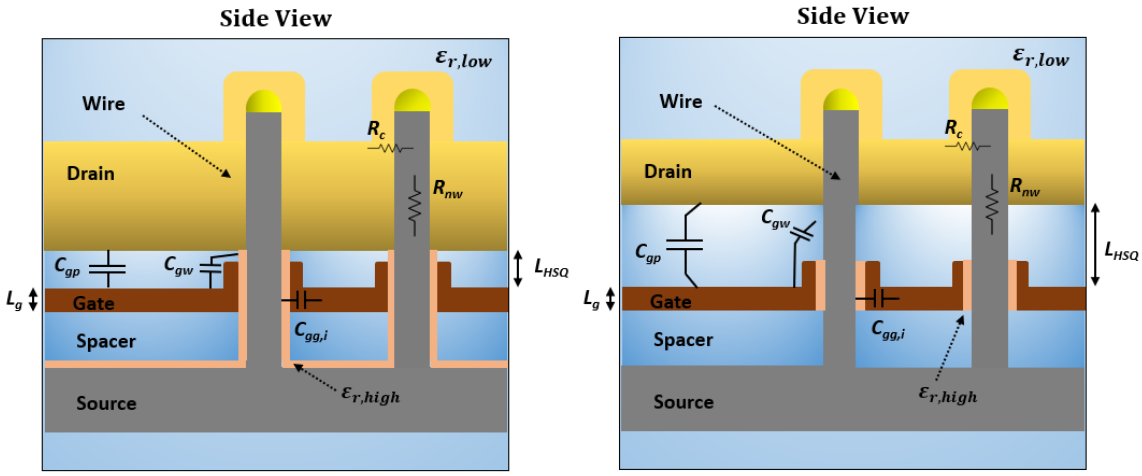
Figure 4.2: The transistor unit cell used during the simulation, with the details of wire geometry are included. r_{nw} is wire radius, t_{ox} is the nanowire thickness, and w_s is the distance between two wires. Periodic boundary condition at the unit cell boundaries in y-direction is considered.

The first model is a symmetric 3D structure, where the source-gate distance and the gate-drain distance are equal. The total capacitance of the structure is evaluated and the effect of varying the κ-value of the embedded material is studied. The result is demonstrated for a single nanowire. The correlation between parasitic capacitance and relative permittivity is explicitly understood when considering plate parallel capacitor equation, expressed as

$$C = \frac{\kappa \varepsilon_0 A}{d_{HSQ}} \tag{4.1}$$

ε_0 is the vacuum permittivity, d_{HSQ} represents the thickness of HSQ layer, and A is the area of the plate capacitor. According to this equation, the capacitance is linearly depended on the relative permittivity, ε_r. Minimized parasitic capacitance is achieved by having a spacer material with low ε_r.

The second structure, shown in Fig.4.3 (a), is modeled to study how the contacts overlap capacitance, C_{gp}, changes as the gate-drain distance, L_{HSQ}, is varied between 30 nm to 130 nm. In the third 3D structure, the high-κ coating material around the nanowires is removed and only remained around the gate surrounded segments of the nanowires, as shown in Fig.4.3 (b). This structure was considered to study the possibility of minimizing the capacitance, C_{gw}, by replacing the high-κ coating film with a low-κ material.



(a) (b)

Figure 4.3: A schematic side view of two additional models of the nanowire FET. (a) The drain contact thickness is varied in order to investigate how the overlap capacitance changes as the distance L_{HSQ} is varying between 30 to 130 nm. (b) The high-κ oxide film is only covering the gated segment of the nanowire.

In these simulations, the terminal input is represented by the gate metal, with a voltage of $V_0 = 1$ V. The cylindrical nanowires and source/drain metals are modeled as metallic elements with a surface potential of 0 V. The nanowires are coated with a high-κ dielectric ($\varepsilon_{r,high} = 20$), of thickness $t_{ox} = 5$ nm.

The structures are embedded in a large enough bounding box to neglect any considerable effect of the capacitances at the contact edges, which might complicate the capacitance calculation. In order to calculate the parasitic capacitances in the transistor unit cell, periodic boundary condition at the unit cell boundaries in y-direction is considered, as illustrated in Fig.4.2. For those models, symmetric structure around z-axis is assumed, meaning that the total calculated source-gate and gate-drain parasitic capacitances are equal.

To calculate the intrinsic gate capacitance, $C_{gg,i}$, section (3.2) is to be considered. According to [34], intrinsic gate capacitance, $C_{gg,i}$, is decreased with wire radius. A wire radius of $r_{nw} = 5$ nm was used in these simulations. However, a radius ranged between 5 - 20 nm has been studied in [31] Fig.2, where a radius of 5 nm showed less possible intrinsic gate capacitance.

4.2 Numerical Calculation of RF Metrics

To calculate the RF metrics of nanowire transistors, a small-signal model circuit is first to be considered. Equations necessary to calculate the electrical elements of this circuit are explained in this section.

4.2.1 Small-Signal Model

The small-signal model of nanowire FETs is represented by using a similar scheme to that of traditional three-terminal MOSFET at an arbitrary frequency. This mainly depends on the fact that the gate metal is insulated from the channel by the high-κ coating material [34]. The circuit model consists of elements that are related to the physical behavior of nanowire transistors. Neglecting the effect of body bias, the traditional two-port small-signal hybrid-π model, shown in Fig.4.4, is used to study the RF performance of 1-D MOSFETs.

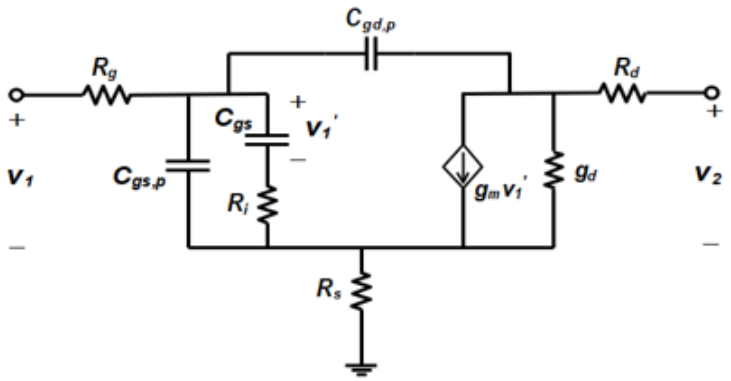


Figure 4.4: A small signal hybrid-π circuit model with the passive elements of a three-terminal FET. Intrinsic and extrinsic capacitances and resistances are included.

The transconductance, g_m, and output conductance, g_d, are included in the small-signal model together with R_g, R_s and R_d to model the resistances of the effective gate, source and drain, respectively. In general, keeping the output conductance minimized is desired to acquire a large intrinsic voltage gain, $A_v = g_m/g_d$. The output conductance is defined as the partial derivative of drain current with respect to source-drain voltage, $g_d = \frac{\partial I_{DS}}{\partial V_{ds}}$. Nanowire FETs are suitable for high values of power gain due to the enhanced electrostatics. Therefore, nanowire FETs are expected to show a lower g_d. For this reason, g_d can be approximated as

$$g_d \approx \frac{g_m}{5} \tag{4.2}$$

which is a typical value that is used when dealing with nanowire FETs.

The resistive element or the channel resistance, R_i is also included in the small-signal model. The nanowire FET structure is assumed to operate in non quasi-static condition, which means that a phase-lag RC, due to scattering, is introduced. The channel resistance

is defined as

$$R_i = \frac{1}{1.4 g_m} \tag{4.3}$$

4.2.2 Device Capacitances

The capacitances C_{gs}, C_{sd} and C_{gd} model the charging currents or how the number of charge carriers changes with the applied voltage at different contacts. These capacitances include both the intrinsic and extrinsic capacitances of the device.

The intrinsic gate capacitance, $C_{gg,i}$, is expressed as $C_{gg,i} = C_{gd,i} + C_{gs,i}$, and is scaled approximately linearly with the gate length, given $C_{gg,i} \sim L_g C_G^{'}$. The effect of the gate capacitance is reduced by decreasing the gate length [31]. $C_G^{'}$ is modeled as the sum of the parallel coupled capacitances C_{ox}, C_Q and C_C. C_{ox} is the oxide capacitance, C_Q represents the quantum capacitance, and C_C is the centroid or band bending capacitance.

C_{geo} represents the gate oxide capacitance for cylindrical geometry, and is defined as [31]

$$C_{geo} = \frac{2\pi\epsilon_0\epsilon_{ox}}{\ln(\frac{r_w + t_{ox}}{r_w})} \tag{4.4}$$

To predict the AC behavior of the device it is important to take the effect of parasitic capacitances associated with the device into account. These capacitances have a large influence on the operation speed of the digital circuit. By using a simple approximation, the values of the parasitic capacitances can be determined.

As illustrated in Fig.4.1 (a), the parasitic gate capacitance along the nanowire can be divided into C_{gw} and C_{gp}. C_{gp} is the parasitic capacitance originates from the fringing electric field between the gate electrode and the source/drain reservoir, while C_{gw} is due to the fringing electric field between the gate electrode and the nanowire source/drain lead [34]. Assuming symmetric structure, the total source and drain parasitic capacitances can be defined as $C_{gs,p} = C_{gd,p} = C_{gw} + C_{gp}$. The parasitic capacitances depend on the device geometry where the nanowire spacing is the key parameter in reducing these capacitances. The electric field between the gate electrode and drain/source electrode is more efficiently screened in dense nanowire arrays. Therefore, dense arrays are superior in minimizing both C_{gw} and C_{gp} [31, 53].

4.2.3 Device Resistances

The performance of any electronic device, especially the energy efficiency and operational frequency in MOSFETs, is further degraded due to the effect of extrinsic resistances. In this thesis, standard transmission line method (TLM) for vertical geometry is demonstrated to characterize the specific contact resistance between the metal contact and the semiconductor nanowire [41].

HSQ - thickness is systemically varied to estimate the nanowire resistance. The total resistance of the nanowire FETs is modeled as two series elements. These include nanowire resistance R_{nw} and contact resistance, R_c, between the nanowire and metal contact (source/drain). These resistances are depicted in Fig.4.5.

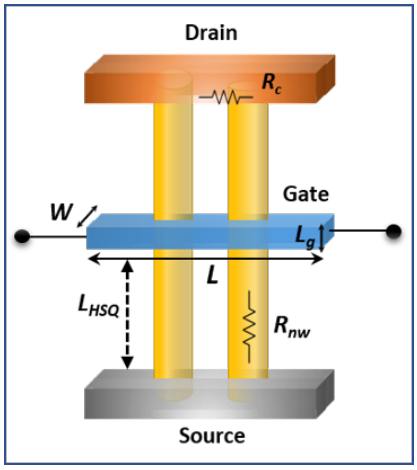


Figure 4.5: A schematic view of a 3D nanowire FET structure with resistances included. The length and width of the gate contact is equal. A similar structure has been modeled in COMSOL to determine the sheet gate resistance.

Due to the cylindrical geometry of the nanowire, equation (4.5) is used to calculate the uniform resistivity of the nanowires.

$$R_{nw} = \frac{\rho_s L_{HSQ}}{\pi r_{nw}^2} \tag{4.5}$$

L_{HSQ} is the distance between the gate and source/drain contacts, which is equal in symmetric structures. ρ_s is the resistivity of the semiconductor, given by

$$\rho_s = \frac{1}{\sigma_n} = \frac{1}{q\mu_n n} \tag{4.6}$$

σ_n is the electron mobility, μ_n is electron conductivity and n is the electron concentration. The contact resistance can be modeled as distributed resistive network, and is defined by equation (4.7).

$$R_c = \frac{\rho_s L_{nw}}{\pi r_{nw}^2} coth(\frac{L_{nw} - L_{HSQ}}{L_T}) \tag{4.7}$$

$$L_T = \sqrt{\frac{r_{nw}\rho_c}{\rho_s}} \tag{4.8}$$

$$\rho_c = \frac{2L_T^2 \rho_s}{r_{nw}} \tag{4.9}$$

L_{nw} is the total length of the nanowire, and L_T is the metal-semiconductor transfer length, given by equation (4.8). ρ_c is the specific contact resistivity and is calculated from equation (4.9) [41].

At low frequencies, the input resistance, or so called R_g, corresponds to one third of the total end-to-end gate metal resistance. Generally, R_g is an intrinsic resistance, since it is more likely linked to the manufacturing process. R_g is a critical parameter that thoroughly

impacts the switching performance and power conversion efficiency of the device. Equation (4.10) is used to determine the value of this resistance.

$$R_g \approx \frac{1}{3}\frac{W}{L}R_{SHG} \tag{4.10}$$

W and L represent the width and the length of the considered gate contact, respectively.

To determine the value of R_g, the gate metal resistance or the sheet gate resistance R_{SHG} is determined by numerical calculation, considering the model shown in Fig.4.5. This cross-sectional layout illustrates a gate electrode, with W/L ratio of 1.

4.2.4 Nanowire FET Scaling

As previously mentioned, a transistor is more likely to be suitable for RF applications if it displays high f_T and f_{max}. Scaling the gate length contributes to a minimized intrinsic gate capacitance, since the last mentioned scaled linearly with the gate length, as explained in section (4.2.2).

In order to understand the relation between scaling of the gate length and an improved transconductance, g_m, equation (4.11) could be considered. This equation is mainly extracted for devices with a relative long gate length, and operate in the diffusive limit.

$$g_m = \frac{WC_g\mu_n(V_{gs} - V_T)}{L_g} \tag{4.11}$$

W is the width of the contact, μ_n is the electron mobility, and $V_{gs} - V_T$ represents the voltage overdrive. For devices with short gate length, the transconductance is therefore expected to be large.

Scaling the gate length is not possible without simultaneously scaling the oxide thickness, t_{ox}, and nanowire radius, r_{nw}, in order to avoid short channel effects [55]. To achieve a good short-channel control, it is preferable to have a gate length of

$$L_g \approx 2.2(t_{ox} + r_{nw}) \tag{4.12}$$

This means that a wire radius between 5 and 22 nm corresponds to a gate length between 22 and 55 nm.

4.3 Review of RF Metrics

The performance metrics of nanowire FETs at high operational frequency are demonstrated in this section. To examine the transistor response under an AC input, Y-and Z-parameters corresponding to the circuit elements in Fig.4.4 are derived.

4.3.1 Two-port Parameters

The admittance parameters, Y-parameters, of the modeled nanowire FET structures, can be calculated using a set of equations in a matrix form. The following matrix, 4.13, is determined using Kirchhoff current law (KCL) to express the current-voltage dependency

in the electric circuit shown in Fig.4.4. By first setting $R_g = 0$ and $R_d = R_s = 0$, this matrix is obtained.

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} \frac{j\omega C_{gs}}{1+j\omega C_{gs} R_i} + j\omega(C_{gs,p} + C_{gd,p}) & -j\omega C_{gd,p} \\ \frac{g_m}{1+j\omega C_{gs} R_i} - j\omega C_{gd,p} & g_d + j\omega C_{gd,p} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{4.13}$$

Y-parameters of this matrix are given by

$$Y_2 = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$$

where

$$Y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0}, Y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0} Y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0}, Y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0} \tag{4.14}$$

To include the effect of resistances, the small-signal circuit in Fig.4.4 can be described as a series connection of three two-port networks, as illustrated in Fig.4.6. This is obtained by first converting Y - parameters, to Z - parameters.

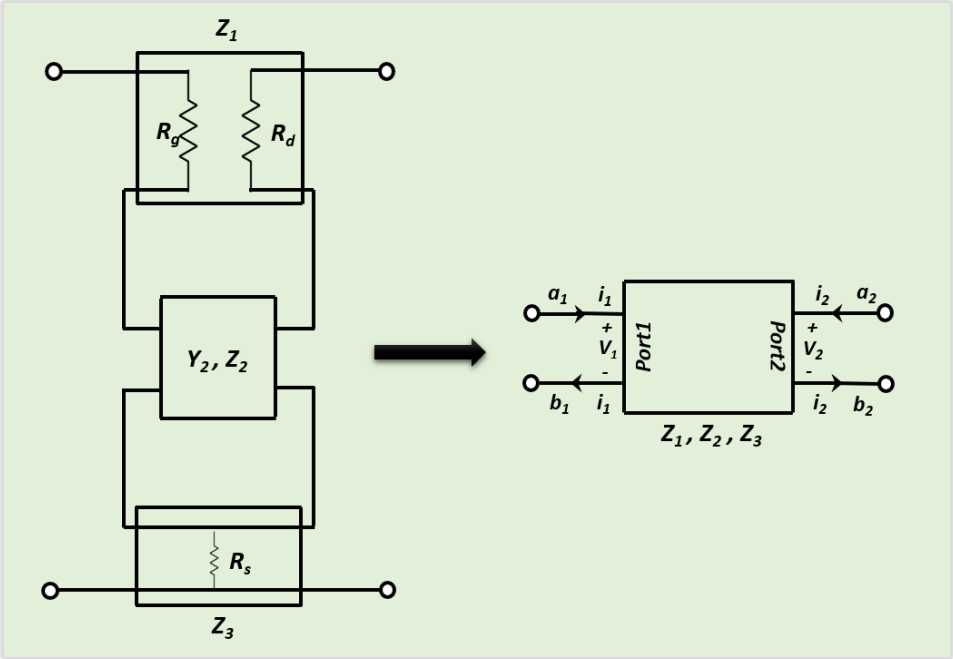


Figure 4.6: Schematic overview of the two-port Y - and Z - parameters, which corresponds to the small-signal model illustrated in Fig.4.4. A series connection of three two-port networks is shown. The figure also includes an additional two-port network, to the right, to represent the sum of the Z-parameters. The incoming and reflected power waves are given by a and b, and the associated currents and voltages are depicted.

In this simulation, Y - parameters of matrix (4.13) are converted into Z - parameters to simplify the calculation. The corresponding matrix, Z_1 - parameters, to define the resistances R_d and R_g, is basically expressed as

$$Z_1 = \begin{bmatrix} R_g & 0 \\ 0 & R_d \end{bmatrix}$$

Using the same deriving method as before, Z_3 - parameters representing the resistance R_s are defined as follows

$$Z_3 = \begin{bmatrix} R_s & R_s \\ R_s & R_s \end{bmatrix}$$

The sum of these parameters can be written as $Z = Z_1 + Z_2 + Z_3$. These parameters are later converted into Y - parameters, since RF metrics are easily described in term of Y - parameters.

4.3.2 RF Metrics

For RF applications, the most important figures of merit to be considered are the current gain h_{21}, and the power gain (MAG, MSG, U).

The current gain, h_{21} is defined as $h_{21} = \frac{Y_{21}}{Y_{11}}$. The so called transition frequency, f_T, is determined from extracting $|h_{21}|^2$ linearly at high frequencies, with a slope of -20 dB/decade in Bode plot. f_T can also be determined using the transitional hybrid-π model, Fig.4.4, and be expressed as

$$f_T = \frac{1}{2\pi}\left(\frac{C_{gg,i}}{g_m} + (R_s + R_d)\left[C_{gg,t}\frac{g_d}{g_m} + C_{gd,t}\right]\right)^{-1} \tag{4.15}$$

$C_{gg,t}$ is the total gate capacitance included both intrinsic and parasitic gate capacitances, while $C_{gd,t}$ is the total gate-drain capacitance.

The maximum available gain of the transistor, MAG, corresponds to the capability of the transistor to amplify the power from source impedance of the electric network, Z_S, to the load, Z_L. The corresponding value of MAG is given by equation (4.16).

$$MAG = \frac{y_{21}}{y_{12}}\left(k - \sqrt{k^2 - 1}\right) \tag{4.16}$$

k is the stability factor

$$k = \frac{2Re(y_{11})Re(y_{22}) - Re(y_{12}y_{21})}{|y_{12}y_{21}|} \tag{4.17}$$

If $k > 1$, the transistor is called unconditionally stable. The transistor is potentially unstable if $k < 1$, leading to a definition of a new figure of merit, the so called maximum stable gain, MSG. Setting $k = 1$ in equation (4.16) gives

$$MSG = \frac{y_{21}}{y_{12}} \tag{4.18}$$

The maximum frequency, f_{max}, is defined as the frequency at which the power gain is unity. This frequency can either be set by MAG or MSG, depending on the characteristic of the transistor.

For transistors with a passive feedback or the so called unilateral transistors, the maximum power gain is defined by Mason's unilateral power gain, U

$$U = \frac{|y_{21} - y_{12}|^2}{4(Re(y_{11}Re(y_{22}))) - Re(y_{12})Re(y_{21})} \tag{4.19}$$

f_{max} is extracted at $U = 1$, and also at $MAG/MSG = 1$ [39]. f_{max} of the hybrid-π model can be expressed as

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_g C_{gd}[1 + \frac{2\pi f_T}{C_{gd}}]\Psi}} \tag{4.20}$$

with

$$\Psi = (R_s + R_d)\frac{(C_{gs} + C_{gd})^2 g_d^2}{g_m^2} + (R_s + R_d)\frac{(C_{gs} + C_{gd})C_{gd}g_d}{g_m} + \frac{(C_{gs} + C_{gd})^2 g_d}{g_m^2} \tag{4.21}$$

CHAPTER 5

Manufacturing Process

In this chapter, manufacturing steps of creating a plate capacitor structure will be described. The purpose of manufacturing this capacitor structure is to determine an exact value of the relative permittivity, κ, of HSQ, and to study the properties of this material. The fabrication steps are combined with theory needed to provide a greater understanding of fabrication and measurement procedures.

5.1 Background

To reduce the parasitic capacitances, the spacer material should have a low dielectric constant, as it states in equation (5.1). The most promising candidate is HSQ, due to its properties, as mentioned before. Introducing of HSQ in the fabrication process of, for example, InAs nanowire FET, can eliminate the need of performing reactive ion etching that is traditionally used to reduce the thickness of organic spacer layers [33].

In order to investigate the properties of HSQ, it is of significant importance to investigate the dependency of HSQ-thickness and the relative permittivity, κ, on electron exposure dose. In this chapter, the relations thickness-exposure dose and κ- exposure dose are investigated. Impedance measurement was performed to estimate the capacitance of the manufactured structure, as explained in section (5.4). κ-value of HSQ is calculated by considering simple plate parallel capacitor equation, given by

$$\kappa = \frac{C d_{HSQ}}{\varepsilon_0 A} \tag{5.1}$$

ε_0 is vacuum permittivity, d_{HSQ} represents the thickness of HSQ layer, and A is the area of the plate capacitor. The thickness of HSQ layer can be set by the electron exposure dose, where high exposure dose results in a thicker layer.

Three samples were finalized during this thesis. Sample A is fabricated on 1 x 1 cm Si substrate with a 200-nm-thick InAs buffer layer. Samples B and C are fabricated by replacing the InAs buffer layer with a 100-nm-thick tungsten, W, layer. The buffer layer of highly doped InAs or W layer serves as a source contact in vertical transistors, and it plays an important role in improving the contact between the semiconductor nanowires and the metal contacts. Replacement of InAs buffer layer was mainly performed to study the relation between κ and the exposure dose at low EBL doses. The presence of trenches in

the buffer layer, to suppress propagation of threading defects, can generate current leakage in thin insulator layers.

Fig.5.1 shows a schematic overview of the desired structure that was manufactured by following some processing steps, such as EBL, UV - lithography, evaporation, lift-off and other processes explained in details later. The fabricated structure consists of a matrix of components with varied area. This structure can be considered as a parallel plate capacitor, where the highly doped InAs buffer layer or W layer serves as the bottom metal contact. The evaporated metal layers serves as the top contact of the plate capacitor.

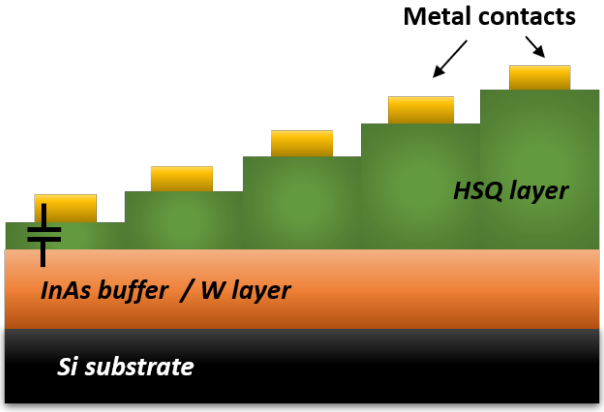


Figure 5.1: A schematic layout of the desired structure with varying thickness of HSQ. The thickness is controlled by the electron exposure dose in EBL. The metal contacts consist of a layer of Ti and Au, deposited by metal evaporation.

5.2 Experiment Details

The samples were prebaked for 1 min at 200^{o}C before spin coating of FOX 15 (HSQ). They are then baked for 2 min at the same temperature after HSQ deposition to remove excessive solvent. A spin speed of 3000rpm for 1 min was used to obtain a maximum layer thickness of approximately 400 nm. Heating treatment of HSQ is important to convert the cage structure into a network structure. This is obtained by maximizing the density of Si-H bonds and minimizing the Si-OH bonds density.

The samples were then exposed with a varied exposure dose in order to define the desired patterns. Electron beam lithography (EBL) system, Voyager, was used to create the patterns. The exposed patterns are squares with sides of 400 x 400 μm, written in matrix consists of 6 columns and 8 rows. The exposure doses are varied between 200 to 600 μC/cm^2 and different exposure steps are tested. To enhance the contrast of the patterns and to remove the unexposed HSQ resist, HSQ was developed in concentrated tetramethylammonium hydroxide solution (TMAH 25 %) for 60s following by water rinsing. The thickness of HSQ for the different components in the matrix was determined by profilometer.

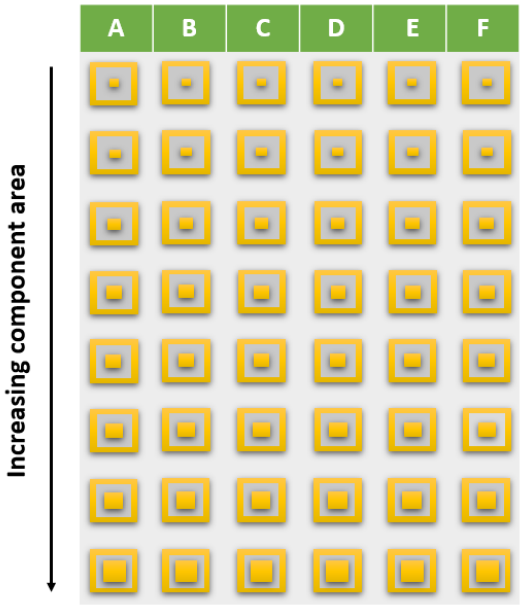


Figure 5.2: A schematic overview of the lithography hard mask used during this thesis. The mask is necessary to defined the pattern of the metal contacts. The area of the components is varied along the y-axis.

UV - photolithography, a process that transfers geometric shapes from a mask into a thin film of radiation sensitive material, was used to define the pattern of the metal contacts. This was achieved by using a lithography mask similar to the one shown in Fig.5.2. The area of the components increase along the y-axis. The main purpose of increasing the area was to explicitly study the correlation between the capacitance per area and electron exposure dose. As it has been discussed in chapters 3 and 4, the capacitance of parallel plate capacitor should increase with area. That means a constant ratio C/A should be observed for components of different area.

$$\frac{C}{A} = \frac{\kappa\varepsilon_0}{d_{HSQ}} \tag{5.2}$$

Before performing the UV - exposure, a radiation sensitive polymeric material or resist was applied by spin-coating at 6000rpm for 1 min. The spinning is necessary to achieve a uniform distribution of resist thickness. The resist used during this step is a negative resist called ma-N 440. The negative-tone resist becomes less soluble upon exposure. Before and after ma-N 440 resist deposition, the samples were heated for 3 min at 95^{o}C to ensure a straight warm distribution and to improve resist adhesion to the substrate.

The process of pattern transfer was accomplished through a photolithographic exposure equipment, $Soft-UV Mask Aligner$. Before ultraviolet-exposure for 35s, the sample was aligned with respect to the mask. After the UV-exposure, the resist was developed by immersion in a developer solvent to remove the unexposed resist. A dry etching, so called oxygen plasma ashing, was used to remove organic matters from the samples. During plasma ashing all residues of the photoresist after development are removed in form of

volatiles of carbon oxides and water vapor. This process is done by using O_2 gas in a Faraday cage to ensure more effective reaction and electron distribution. To remove the native oxide that could have grown at the surface of the sample, wet etching was performed in HCl:H_2O 1:1 for 1 min, followed by water rinsing.

Metal evaporation was performed to deposit the metal contact layers. The evaporation was done in a vacuum chamber, and the metals to be evaporated were placed in boats that were heated up to above the melting temperature of the metal. During evaporation, a metal film consists of 8 nm titanium (Ti), and 200 nm gold (Au) was deposited onto the sampele. Lift-off process was done as the last step to define the metal contact after metal evaporation.

5.3 HSQ-thickness

The thickness of the deposited HSQ layer is measured using profilometer. A so called contact (stylus) profilometer was used in order to measure the profile of the layer surface. This profilometer consists of a sample holder and a detect. A probe is used to detect the surface by direct physical contact, and the samples are scanned in z-dimension to obtain height information. A another method to estimate the thickness is to compare the color of HSQ layer with a reference sample, for example similar to the one shown in Fig-5.3. This method gives approximate thickness values, therefore profilometer is preferred to obtain a correct thickness measurement. The measured thickness is then plotted as a function of varying energy dose, see section (6.2.1)

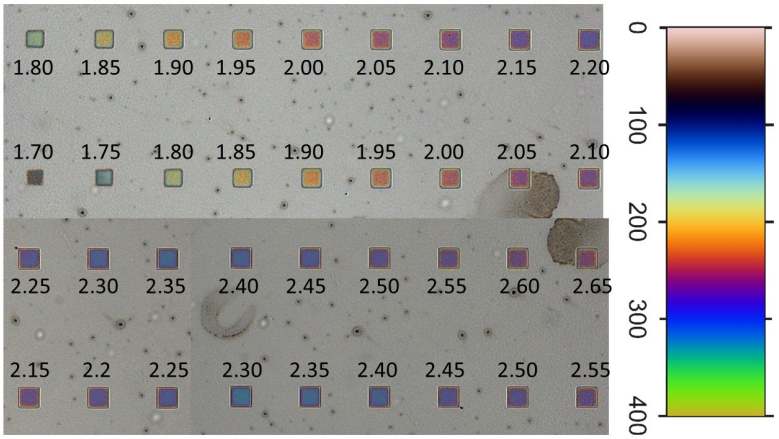


Figure 5.3: Reference sample with components exposed with different energy doses. The exposure dose varies from 1.80 to 2.55, with an exposure step of 0.05. The colorbar indicates the thickness of the deposited layer.

5.4 Cf - Characteristics

To calculate the κ-value of HSQ, the capacitance of the manufactured structure should be determined. Cf-characteristics was performed by using a probe station and impedance analyser in order to measure the impedance of the designed structure. These structures

are easily modeled as a capacitor, C, in series with a resistor, R, at a given frequency. The resistances of the structure are represented by the metal contacts, while the capacitances corresponds to the insulating layer, HSQ in this case, between the metal contacts.

The measured impedance consists of real part, R, and imaginary part, $X_C(\omega)$, as expressed in equation (5.3).

$$Z = R + X_C(\omega) = R + \frac{1}{j\omega C} \tag{5.3}$$

The capacitance is estimated by extracting the imaginary part, $X_C(w)$, and is expressed as

$$C = -\frac{1}{\omega X_C(\omega)} \tag{5.4}$$

ω is the angular frequency and is defined as $\omega = 2\pi f$, where f represents the frequency. From equation 5.3, it observed that $X_C(\omega)$ is frequency dependent. The measured capacitance is expected to be independent of frequency, since an increase in frequency will contribute to an equivalent increase in $X_C(\omega)$ which results in constant capacitance at the given frequency range.

Current leakage is believed to occur in structures with relatively thin dielectric layer. Another contributor to the current leakage in plate capacitors is the undesired imperfection in the dielectric layer. These imperfections result in a non perfect insulator dielectric layer, that allows a leakage current to flow and consequently discharges the capacitor. The impedance would be better modeled as a capacitance in parallel with a leakage resistor, R_L, as it is illustrated in Fig.5.4 and given by equation (5.5).

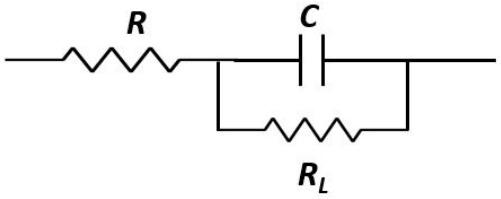


Figure 5.4: The figure shows a capacitance parallel coupled to a resistance R_L associated with current leakage. The sum of these elements is in series with device resistance, R.

$$Z = R + \frac{R_L}{1 + j\omega R_L C} \tag{5.5}$$

In this case, the imaginary part can be expressed as

$$X(\omega) = -\frac{\omega R_L^2 C}{1 + (\omega R_L C)^2} \tag{5.6}$$

It is difficult to predict the behavior or the dependency of the capacitance on the frequency in this case. However, it can be observed that the large denominator of equation (5.6) will result in small capacitance.

5.5 Durability of HSQ

To investigate the durability of HSQ and to study if it has the properties required to be considered as a good dielectric interlayer, two experimental measurements have been performed.

The durability of HSQ was studied by annealing one of the fabricated samples in a rapid thermal annealing (RTA) system in N_2 environment at 350^oC for 1 h. The thickness of HSQ and the capacitance of this sample were measured before and after annealing, in order to explore the capability of HSQ to withstands higher processing temperatures.

The second experiment was to investigate how the thickness and κ-value of HSQ will be affected upon double EBL exposure. In order to perform this measurement, the energy dose of EBL during the first exposure is varied along the x-axis of Fig.5.2, where the area of the components are equal. The thickness was then measured for two rows of components, since the thickness is expected to be equal for all same area components. This measurement was performed on a sample with tungsten layer. The deposited HSQ was exposed in EBL and developed in TMAH before the measurement. No metal evaporation was performed before the second exposure. The correlation of the measured thickness and energy dose was evaluated after the first exposure.

During the second exposure, the energy dose was varied along y-axis instead. The area of the components increases downwards, as shown in Fig.5.2. Thickness measurement was performed before metal evaporation of metal layers. The relation between thickness, with a specific first exposure dose, and energy dose was considered. The purpose of that is to examine if HSQ maintains a thickness that is independent of the exposure dose. Furthermore, the κ-value of HSQ after the second EBL exposure was calculated. It was interesting to investigate if high energy doses could result in HSQ with larger κ-value than that of SiO_2.

CHAPTER 6

Results and Analysis

In this chapter the results obtained from the simulation part and the experimental part are presented and discussed.

6.1 Simulation Result

The simulation and numerical calculation of the capacitances are obtained without considering the affect of frequency on the calculated capacitances. Direct current, DC, is therefore to be considered during this simulation. The calculated capacitances are normalized to a single nanowire.

6.1.1 Numerical Modeling

The parasitic capacitances of three different models have been calculated. The simulation is based on geometry optimization and on changing the κ-value of the insulating material. The modeled 3D nanowire structures consist of nanowire with $L_{nw} = 260$ nm, $r_{nw} = 5$ nm, and $L_{HSQ} = 130$ nm. The permittivity of the embedded material is chosen to be 3.00, which corresponds to the expected κ-value of HSQ. Periodic boundary condition in the transistor unit cell, Fig.4.2, was considered in order to estimate the capacitances of the structures. The obtained result is normalized to one wire.

In the beginning, it was interesting to study how the parasitic capacitances of the modeled 3D structures depends on the κ or ε_r of the spacer material. Fig.6.1 (a) shows the sum of numerically calculated parasitic capacitances, $C_{gs,p}$ and $C_{gp,p}$, as a function of the relative permittivity, $\varepsilon_{r,low}$, that is varied between 2.00 and 9.00. The result, shown in blue, is obtained for the symmetrical structure, Fig.4.3. The capacitance is linearly dependent on ε_r, and a minimized capacitance is obtained for small ε_r. In order to minimize the parasitic capacitances it is preferable to keep the relative permittivity of the insulating material as low as possible. This behavior is identical to the one considered by equation (5.1).

The result obtained for the third model, the coating material around the nanowires is removed, shown in red in Fig.6.1 (a). Replacing the high-κ oxide coating material with a low-κ material could reduce the parasitic capacitances, mainly due to reduced C_{gw}, while preserving the good electrostatic coupling to the gate.

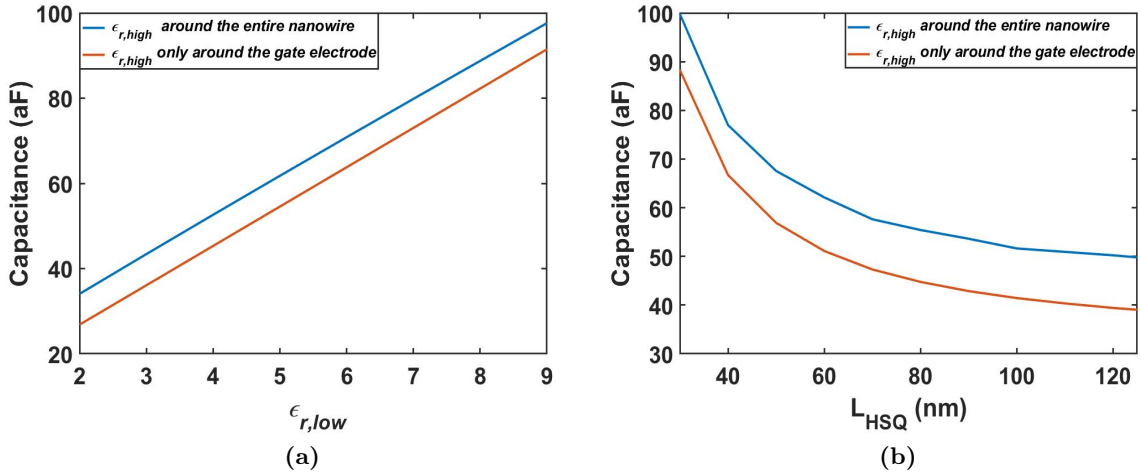


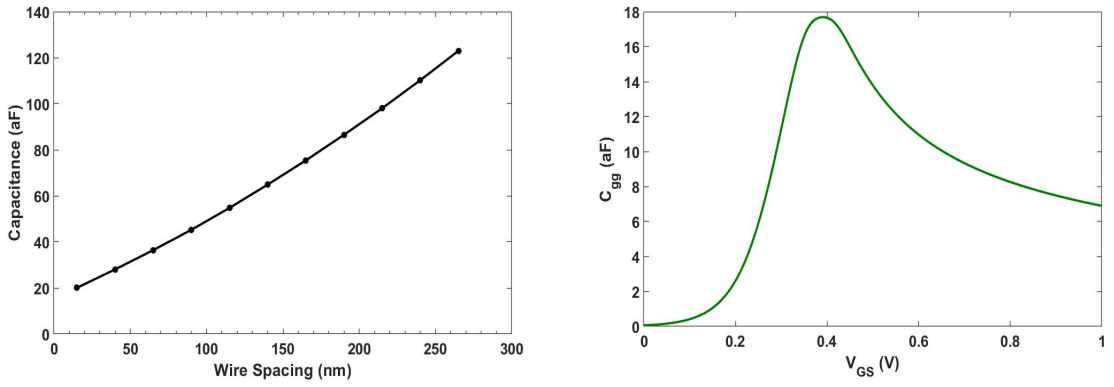
Figure 6.1: (a) The numerically calculated parasitic capacitances as a function of the dielectric constant of the embedded material. Wire spacing is 15 nm. The blue curve shows the correlation when high-κ is surrounding the entire nanowire, while the red curve shows the correlation where only the gate electrode surrounded segments of the nanowire are coated. (b) The correlation between the capacitances as a function of spacer distance L_{HSQ}.

Fig.6.1 (b), shows the result achieved from the second simulation. The distance, L_{HSQ}, is varied to study the possibility of minimizing contacts overlap capacitance, C_{gp}. From this simulation, an optimal distance to achieve a minimized capacitance could be determined. L_{HSQ} is varied between 30 to 130 nm. The result obtained from the simulation of the structure with high-κ coating material around the entire nanowires, Fig.4.3 (b), is shown in blue in Fig.6.1 (b). The capacitance is rapidly decreased with increased spacer distance, to then plateaus at a specific value. The correlation between capacitance and contact distance is equivalent to that of simple parallel plate capacitor as given in equation (5.1).

In conclusion, the spacer distance between the gate and drain/source should be large in order to decrease the parasitic capacitances, $C_{gp,p}$ and $C_{gs,p}$. Furthermore, it is preferred to only cover the gate surrounded segments of the nanowire with high-κ oxide film. This in order to further minimizing the parasitic capacitances and improve transistor performance.

6.1.2 Intrinsic and Extrinsic Capacitances

Fig.6.2 (a) shows the numerically calculated parasitic capacitances as a function of a varied wire spacing. The wire spacing is varied between 10 nm and 260 nm. The obtained capacitances are normalized to 1 nanowire. The simulation was performed for a structure with nanowires of length $L_{nw} = 260$ nm, radius $r_{nw} = 5$ nm, and oxide thickness $t_{ox} = 5$ nm. The corresponding gate length, L_g, is scaled according to $L_g = 2.2(t_{ox} + r_{nw})$ in order to suppress any short channel effects [31], as explained in section (4.2.4).



(a) (b)

Figure 6.2: (a) Total parasitic capacitances, $C_{gd,p}$ and $C_{gs,p}$, as a function of the wire spacing. The result is shown for one nanowire. (b) The calculated quantum capacitance as a function of the applied voltage varied between 0V to 1V.

As further shown in Fig.6.2 (a), improved device performance is obtained if the wire spacing is kept as small as possible. This demonstrates that the parasitic capacitances are minimized in case of dense nanowire arrays. The dense array improves the $C_{gg,i}/C_p$ ratio by screening the effect of the electric field between the gate electrode and source/drain electrode. This will result in minimized total drain/source parasitic capacitances.

Fig.6.2(b), shows the calculated quantum capacitance, according to equation (3.6) and (3.9). The result is hold for InAs nanowire with $m^* = 0.023m_0$. The quantum capacitance plateaus at approximately 7 aF. C_Q is proportional to the 1-D density of states at the Fermi level. The density of states goes to infinity at the band edge of 1-D devices. Accordingly, a rise in C_Q near the band edge could be observed [40], as shown in Fig.6.2 (b). This calculation is performed at room temperature, $T = 300$ K. Quantum capacitance is dominated in quantum capacitance limit, $C_{ox} \gg C_Q$. According to equation (3.4) the intrinsic gate capacitance can be expressed as $C_{gg} \approx C_Q$.

Reducing the parasitic capacitances is one of the important technology solutions used to optimize transistor performance. By comparing Fig.6.1 (a) with Fig.6.2 (b), it can be noticed that the parasitic capacitances is approximately two times larger than the quantum capacitance. Hence, the former mentioned should be minimized during simulation and fabrication of nanowire FETs to further improve device performance.

6.1.3 Extrinsic Resistances

The standard transmission line method (TLM) is used to determine the contact resistance between the nanowire and the metal contact. First, ρ_s is determined for InAs nanowire with high electron doping of $N_d = 5 \times 10^{19}$ cm^{-3}. This gives an electron mobility of around 10^3 [cm^2 V^{-1} s^{-1}] [41]. Inserting these values in equation (4.6) gives ρ_s of 1.25 $\Omega\mu$m. Fig.6.3 shows the calculated nanowire resistance as a function of varied contact separation thickness, L_{HSQ}.

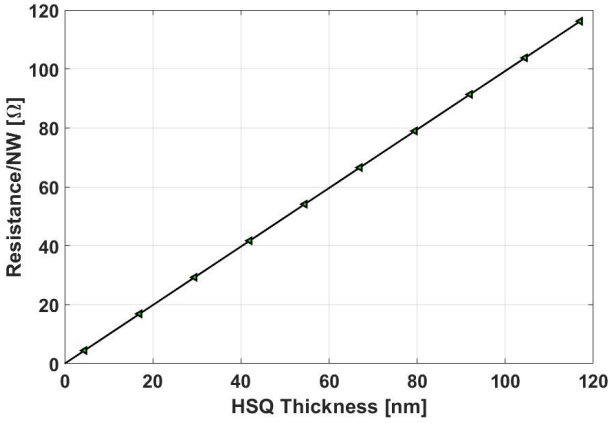


Figure 6.3: Nanowire resistance as a function of varied gate-drain distance for a nanowire with a radius of 5 nm. The resistance is normalized with the number of wires in the array.

The specific contact resistivity, ρ_c, is determined according to [42] (Fig.3 (b)), and estimated to approximately 1.0 $\Omega\mu\text{m}^2$. From this, the transfer length, L_T, is calculated using equation (4.8), and is determined to be about 126.6 nm. Taking these calculations into account, the specific contact resistance is calculated to be around $R_c = 126\ \Omega$, according to equation (4.7). The total extrinsic resistance of the source contact is equal to that of the drain contact, due to symmetry, giving $R_s = R_d \approx 244\ \Omega$, for a nanowire of height $L_{nw} \approx 260$ nm.

6.1.4 Simulation Characteristics

The important figures of merit of RF applications were calculated. The result from this simulation is shown in Fig.6.4. Current gain h_{21}, and the power gain metrics MAG, MSG, and U are included together with the stability factor k. As mentioned in section 4.3, the two important metrics for transistors, the unity current gain frequency f_T and the maximum power gain frequency f_{max} are determined at $h_{21} = 0$ dB and $U = 0$ dB, respectively. Accordingly, $f_T \approx 477.5$ GHz and $f_{max} \approx 1592$ GHz. These results are shown for an *intrinsic* $g_m = 3.53\ \text{mS}/\mu\text{m}$ and for $L_g \approx 22$ nm. The highest reported values of f_T and f_{max} for InP based high electron mobility transistors (HEMT) are 710 GHz [51], and 1.5 THz [52] for $L_g = 32$ nm.

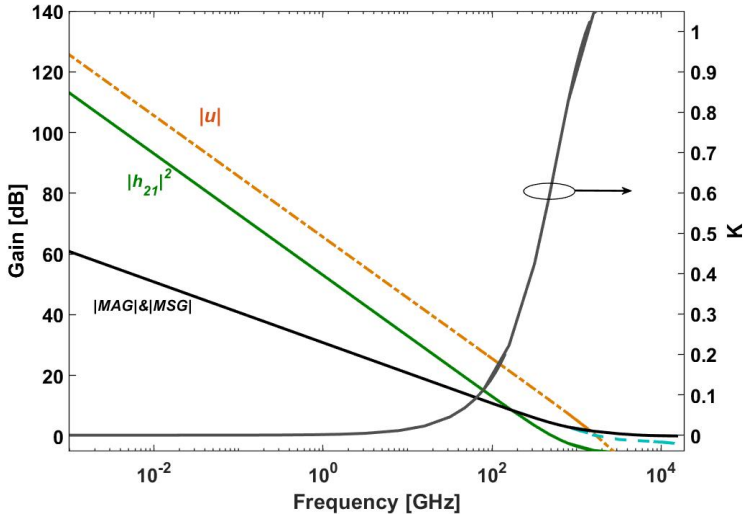


Figure 6.4: RF metrics, including the current and power gain in dB, as a function of frequency for the modeled nanowire FET, with L_g of 22 nm. The simulation and the numerical calculation were performed using software Maple.

Calculating of RF figures of merit was obtained by considering some simplifying assumptions. For example, it has been assumed that the intrinsic gate capacitance, $C_{gg,i}$, is included within the intrinsic gate-source capacitance, as shown in Fig.4.4.

Having a low-κ insulating materials can also contribute to a higher f_T, as illustrated in Fig.6.5. This is due to the minimized parasitic capacitances as explained earlier. For this reason, replacing SiO_2 with low-κ material can be regarded as a great alternative to improve transistor performance.

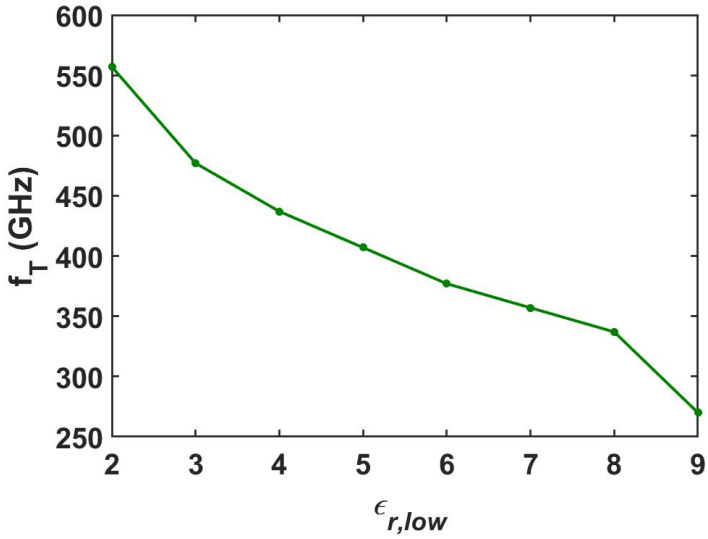


Figure 6.5: The calculated f_T as a function of the dielectric constant, $\varepsilon_{r,low}$, varied between 2.00 and 9.00.

6.2 Experiment Result

After performing the manufacturing steps desired to create the plate capacitor structure, microscopic images of some components were taken. Two of the finished components are shown in Fig.6.6. The electron exposure dose is lower in the component to the left than the one to the right. This can be indicated by the color of HSQ layer, shown here in pink and green. The brown layer corresponds to Si substrate, while the top and bottom metal contacts of the plate capacitor are shown here in yellow.

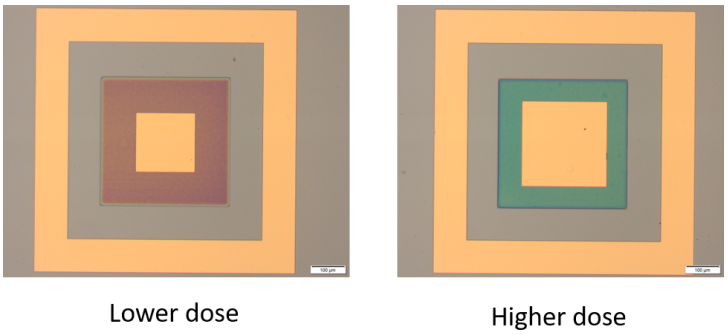


Figure 6.6: A microscope image of two of the finished devices. The square pattern, shown here in pink and green, was defined by EBL after HSQ deposition. The metal contacts were defined using UV-photolithography. (a) A component with lower exposure dose and smaller area (b) Another component with a higher exposure dose and larger area.

6.2.1 Measurement of HSQ-thickness

The results of measured the HSQ-thickness of the designed parallel plate capacitors are shown in Fig.6.7. These results are shown for components of different area. The thickness of HSQ for the both sample A and B varied from approximately 50 nm up to 400 nm, depending on the electron exposure dose. The exposure dose of sample A varies from 200 to 250 μC/cm^2, giving a HSQ-thickness that is varied from 240-315 nm up to approximately 400 nm.

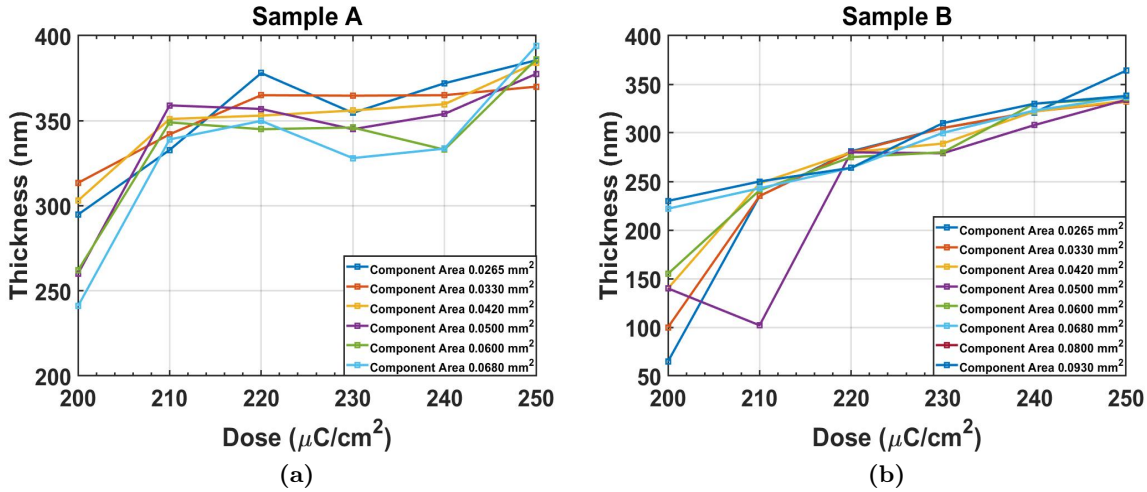


Figure 6.7: An overview of the thickness measurement for the designed samples A and B. (a) and (b) show the correlation between the measured HSQ-thickness and the exposure dose for sample A and sample B, respectively.

Fig.6.8 shows the extracted standard deviation for both sample A and B. In sample A, a small distribution, ≤ 10, at exposure doses between 210 and 230 μC/cm^2 is observed. A similar result is observed for sample B, with a small distribution at exposure doses between 220 and 240 μC/cm^2. The distribution is larger for sample B than A at exposure doses less than 220 μC/cm^2. This inaccuracy in measurement might be due to an uneven HSQ distribution during spin coating. This might be the main reason behind the observed fluctuations in thickness, since the errors are particularly pronounced at the edges of the samples.

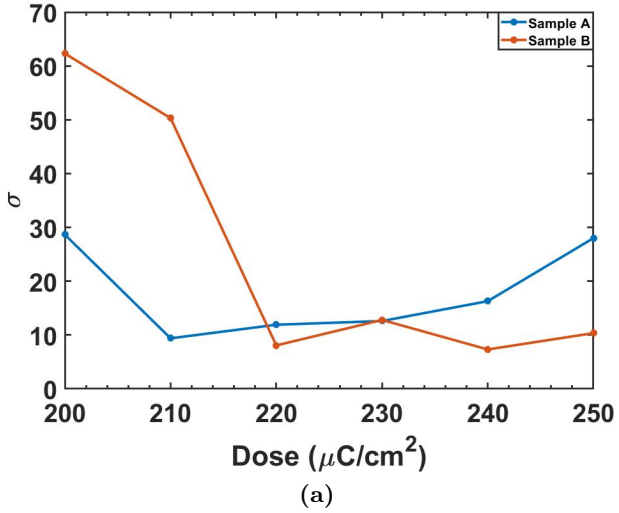


Figure 6.8: The extracted standard derivation for both sample A and B, to determine the distribution in the measurement

In sample B, where InAs buffer layer was replaced by a tungsten metal layer, the thickness is ranged from 50-225 nm up to around 350 nm. For both samples, the thickness increases rather rapidly in the beginning and then saturates at a specific thickness, the maximum thickness, where the HSQ becomes independent of the exposure dose.

HSQ - thickness measured for components of different area should be constant and independent of increased component area. Therefore, no distribution in thickness measurement at a specific exposure dose is expected. The thickness should only depend on the exposure dose. However, fluctuations during thickness measurement is observed to be large at exposure dose = 200 μC/cm^2. The values are less distributed at higher exposure doses.

6.2.2 Cf - Measurement

Cf-characteristics was considered in order to measure the impedance of the designed samples. The capacitance is extracted from the imaginary part of the measured impedance, as explained in section (5.4). The capacitances of the components in the samples were extracted as a function of frequency that is varied from 10 kHz to 10 MHz. The measurement results for both samples A and C are shown in Fig.6.9 (a) and (b), respectively.

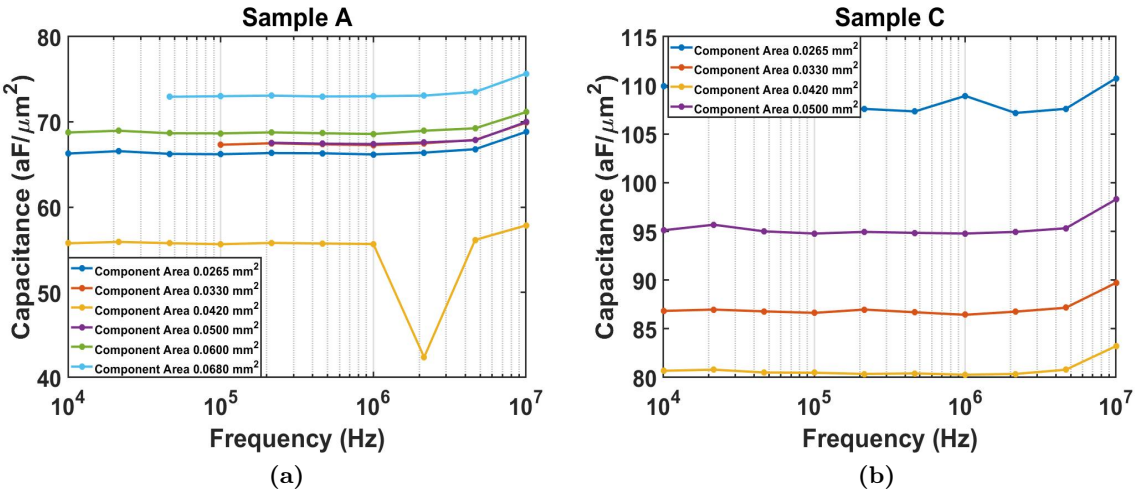


Figure 6.9: Cf characteristics at frequency ranged from 10 kHz to 10 MHz. (a) The measurement result for sample A (b) The measurement result obtained for sample C.

It is interesting to notice that at a given frequency range, the capacitance of the components is essentially unaffected by the frequency. This result was expected according to section (5.4). As further shown in Fig.6.9, the capacitance increases with component area, which is in consistent with the expected behavior when taking equation (5.1) into consideration. The low capacitance at frequency 2.0 MHz can be observed for the component with area 0.0420 mm^2, shown in orange. Besides, a small increase in capacitance can be noticed at frequencies approximately 10 MHz. These exceptions might have occurred due to measurement error.

6.2.3 Measurement of κ-value

To calculate the κ-value of HSQ and to investigate how it depends on the exposure dose, Cf- characteristics was first considered at a given frequency range. To calculate the κ-value of HSQ, equation (5.1) was used. The obtained results for the three samples are illustrated in Fig.6.10 at frequency $f = 70$ kHz.

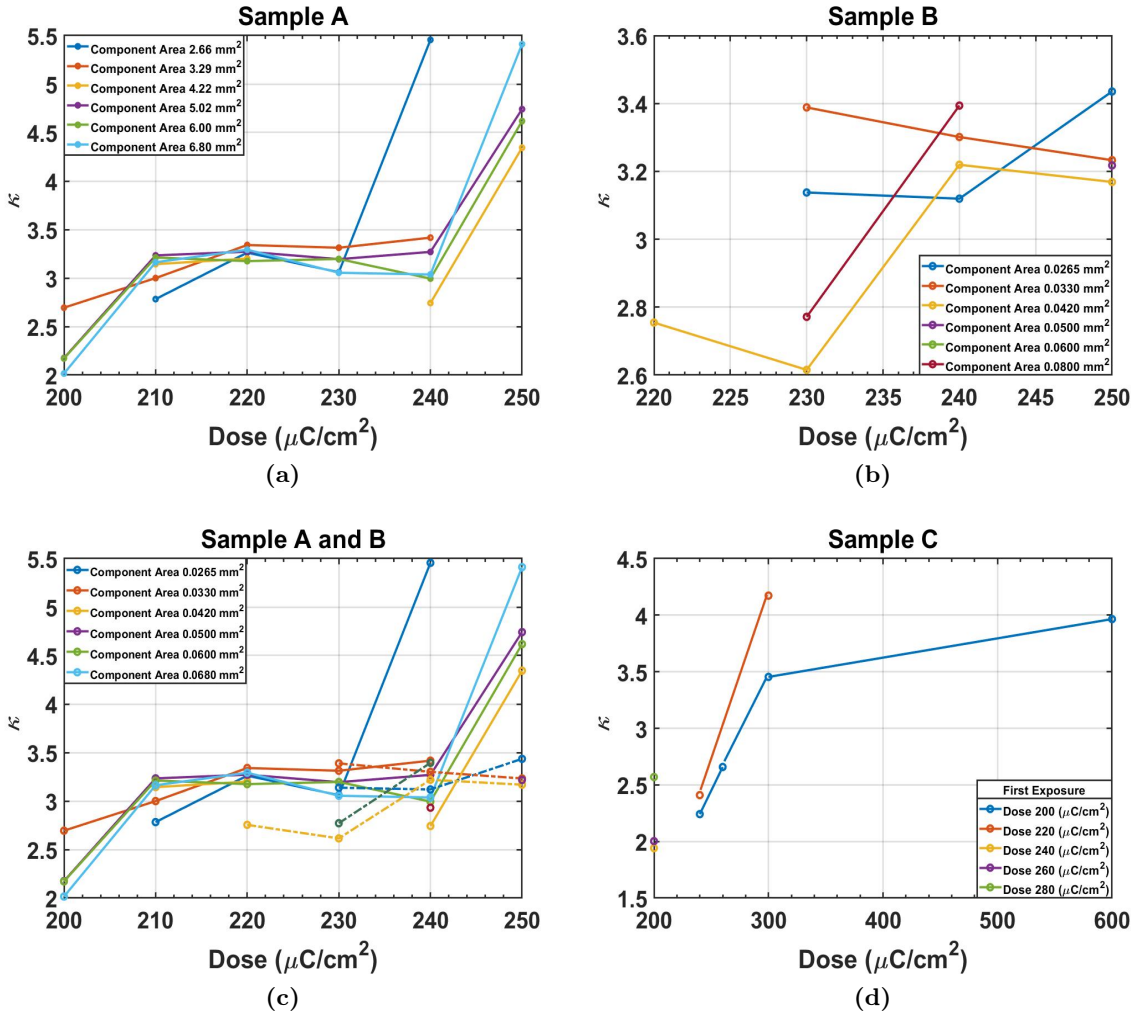


Figure 6.10: Overview of κ-value measurement at frequency of 70 kHz. (a)-(b) Show the correlation between the calculated dielectric constant of HSQ for the all components in samples A and B. (c) The results for both sample A and B, represented by solid lines and dotted lines respectively. (d) The measurement result for sample C, where the exposure dose during the second exposure varied downwards as illustrated in Fig.5.2.

According to equation (5.1), the κ-value depends on the thickness of HSQ and should increase as the thickness increases. It should then saturate as HSQ reaches its maximum thickness at higher energy doses. Fig.6.10 (a) shows the measured result for sample A,

where κ increases from 2.0-2.6, and plateaus at 3.25. However, the expected dependency does not maintain for exposure doses higher than 240 μC/cm^2, as κ seems to increase further beyond the saturation value. The deviation in the result might due to the presence of dust particles at the edges of the sample or an uneven HSQ-thickness distribution. Having these issues can affect measurement sensitivity and result in unexpected values.

Including the results obtained for both samples A and B, Fig.6.10, shows that the κ-value of HSQ is 3.00 $\pm$ 0.40.

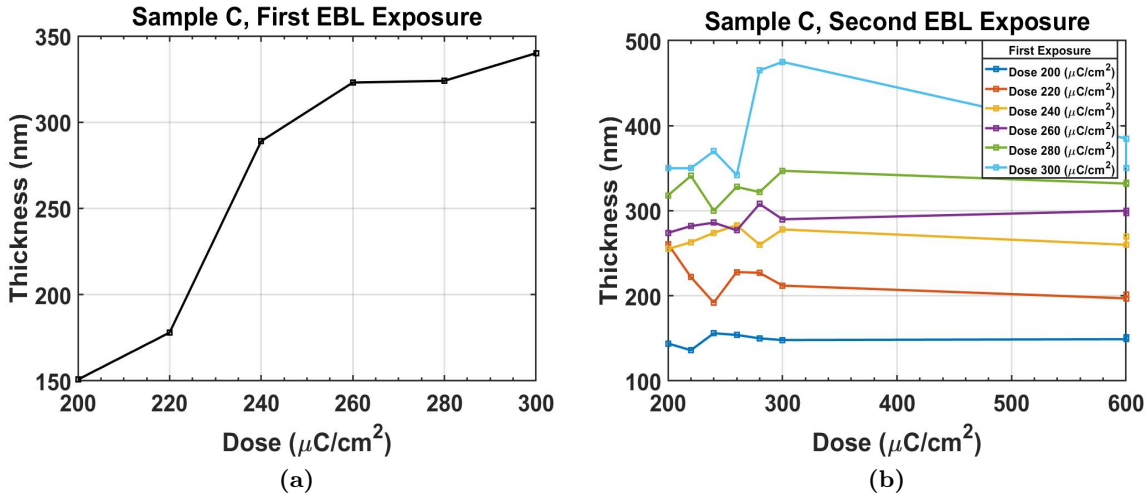
Same result is achieved for sample C as for sample B, at lower exposure doses than 300 μC/cm^2. For very high doses $\sim$ 600 μC/cm^2, the κ-value of HSQ films increases up to 3.9, which is equal to that of SiO_2. It is believed that the κ-value of HSQ could not be larger than 3.9. HSQ is expected to have properties similar to those of SiO_2 as the network structure of HSQ is formed upon heating or EBL exposure. However, the result is based on few measured data points, making it difficult to conclude the behavior of HSQ at very high exposure doses.

6.2.4 Measurement of HSQ Durability

To investigate the durability of HSQ, two experiment were performed and the obtained results are presented in this section.

The first experiment was to anneal sample A in RTA system to investigate if HSQ withstands higher processing temperatures. Measurements of the thickness and κ-value of sample A were identical to those obtained before annealing. This means that HSQ withstands further fabrication processing, and is durable as insulating material.

The purpose of performing the second experiment was to investigate the properties of HSQ upon double EBL exposure. Sample C was designed to perform this investigation. The measurement result of the thickness-dose relation after first EBL exposure is shown in Fig.6.11 (a). The thickness seems to increase linearly, from 150 nm, and plateaus at thickness of 340 nm. During first EBL exposure, the thickness is expected to increase with higher energy doses and then saturates as HSQ becomes independent of electron exposure dose, according to equation (5.1). The result from the second EBL exposure is shown in Fig.6.11 (b).



(a) (b)

Figure 6.11: An overview of the thickness measurement for sample C, outlining the correlation of capacitances and exposure dose, after first (a) and second (b) EBL exposure.

As it is illustrated, HSQ-thickness is roughly independent of the exposure dose after the second exposure. This means that HSQ is stable and durable as a dielectric layer, and can therefore be used as a spacer material in vertical transistors.

The capacitance increases with area, which means that the ratio C/A should be constant. According to equation 5.2, this will result in constant κ/d_{HSQ}. The thickness after the second EBL exposure is therefore expected to be independent of the energy dose, when the energy dose is varied with increased component area. Having insulating material with thickness that is independent of the processing temperature, or energy dose, could be considered as a proof of material durability. HSQ showed a great ability to withstands high processing temperature, and therefore can be considered as a good insulating material.

However, the result shows some fluctuations at low exposure doses. This might depend on measurement errors or dust particles introduced on the surface of the samples before HSQ deposition. The result of thickness measurement with first exposure dose of 300 μC/cm^2, showed in light blue in Fig.6.11 (b), differs from the other curves. The thickness increases from 350 nm to approximately 450 nm, and then plateaus at 350 nm. The surface of the tungsten layer, deposited on the top of the Si substrate, might have been unevenly deposited during spinning. This might have resulted in the large variation in the thickness observed at exposure dose 300 μC/cm^2.

CHAPTER 7

Conclusion and Outlook

Nanowire-based transistors, with their outstanding performance and physical properties, have become the most promising candidates for high speed nanoelectronic circuits. Introducing nanowire transistors into the electric circuits has solved some of scaling challenges faced by semiconductor industry. The inherently 3-dimensional structure, enhanced electrostatics, and better integration possibilities are some of nanowire transistors properties that allow for further scaling and lead to device operation at high frequency.

However, nanowire transistors have also faced some performance challenges, associated with the architecture and design of the vertical structures. The effect of the contact resistances at the interface between the nanowire and the metal contact, and also the large series resistance in the ungated segments have been among the major device performance challenges. Thin spacer layers has been utilized to reduce the effect of series resistances. However, this approach has contributed to a further increase in parasitic capacitances due to the increased overlap between the metal contacts of the transistor.

Therefore, new interlayer dielectric (ILD) materials with low relative permittivity ($\kappa < 3.9$) are required to be integrated in electronic circuits to minimize the resistance-capacitance (RC) delays. HSQ is one of the most promising candidates be used as insulating spacer material. The good properties of this material allow for integrating of HSQ in semiconductor fabrication.

To determine the κ-value of HSQ, simple plate capacitor structure, consists of HSQ layer between two metal contacts, was manufactured. The measurement result showed that the κ-value is approximately 3.00 ± 0.40. This demonstrates the low-κ properties of HSQ. The low κ-value of this material can contribute to minimized parasitic capacitances. Furthermore, the durability and capability of HSQ to withstand further fabrication processes have been proved. The experimental measurement on HSQ showed that HSQ could be considered as a good insulating interlayer. Replacing the conventionally used insulating material, SiO_2, with HSQ is expected to improve the performance of nanowire transistors.

Additionally, the parasitic capacitances in nanowire-based vertical transistors have been investigated and calculated. Moreover, equations of RF figures of merit were derived, and the most important metrics for transistors have been extracted. It has been shown that the parasitic capacitances are minimized as the separation between the nanowire is decreased. Dense nanowire arrays contributes to increased screening of the electric field between the wires. Minimized parasitics capacitances have been achieved in the modeled structure in which the high-κ coating material around the nanowire has been removed. The minimized

capacitance originates from the reduced parasitic capacitance between the gate contact and nanowire lead, C_{gw}.

Short channel effects and quantum mechanical effects, such as tunneling and band bending, should have been considered to obtain more accurate calculation. Moreover, the contribution of oxide capacitance to the total capacitance should have been regarded. Calculations at non-degenerate conditions and not only for degenerate conditions should have included to obtain a greater understanding of operation in real devices.

Implementation of HSQ as a spacer material between the metal electrodes in nanowire transistor might be of interest as a follow-up. This is essential to be able to perform calculations and performance investigation required to compare with the numerically obtained results. However, a successful integration of low-κ material is difficult to achieve and the material should fulfill some requirements to be suitable for potential applications.

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