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Detection and location of HVDC commutation faults from PMU data

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Master thesis

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Abstract:
Commutation Failures in LCC HVDC converters is a topic that is normally addressed from the component perspective, looking at converters' internal signals. How these commutation failures affect the outer AC network is not deeply understood yet. This thesis will provide proof of how commutation failures causes abnormal behavior in the AC network, and how PMU data can be used in order to distinguish commutation failure from AC faults. In order to do so, simulations have been carried out in PSCAD and MATLAB-Simulink. The spreading of commutation failures in a bigger network, in this case NORDIC32, has also been studied using DigSilent-PowerFactory.

Keywords:
HVDC-links, HVDC converters, Commutation failures, Phasor measurement units (PMUs), Electric power systems, Wide Area Measurement systems (WAMS), Standard IEEEC 37.118, Single-line to ground faults, Three-Phase faults, Fault detection and location, Nordic 32, DigSilent-PowerFactory, PSCAD, MATLAB-Simulink, Symmetrical components.

If I have seen further it is by standing on the shoulders of giants.

Sir Isaac Newton,1676

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Preface

After an event in the Nordic system, it was recently realised that HVDC converter commutation failures are not visible to TSO control room. Therefore, it is highly interesting to understand how these failures spread along the AC network.

The main aim of the thesis was, firstly, to develop an algorithm for detecting and locating commutation failures using PMU data, but after the first simulations in MATLAB-Simulink, an unrecognizable behaviour in the AC current was found, which no one could explain at the first glance. To understand that behaviour became the main focus of the thesis. Simulations were carried out in PSCAD in order to address the validity of the previous simulations, finding the same unknown behaviour. For that reason, the aim of the thesis changed, being the algorithm less interesting and prioritizing the understanding about the reasons why the system reacts in that way when commutation failures happen and how can PMU data be used for characterizing that behaviour.

After some time and discussions, it was found that the reason of that behaviour is the configuration of the transformers in the HVDC-link. Therefore, new simulations were carried out in order to prove what was a hypothesis so far. Once the interaction between the HVDC and the AC system while commutation failures was understood, an HVDC was simulated in a complex network in order to understand how these faults spread, but without focusing on the development of an algorithm but only qualitatively, due to time limitations.

List of abbreviations

AC – Alternating current

CCA – Current control amplifier

CFC – Converter firing control

CMU – Current measurement unit

CMU-Current measurement unit

DC – Direct current

EC – European commission

EU– European Union

FACTS controllers – Flexible AC Transmission System controllers

GPS – Global Positioning System

HVDC – High voltage direct current

PC – Power control unit

PDC – Phasor Data Concentrator

PLL – Phase-locked loop

PMU – Phasor measurement Unit

PV – Photovoltaics

RES – Renewable energy sources

ROCOF – Rate of Change of Frequency

SCADA – Supervisory Control and Data Acquisition

SLG fault– Single line to ground fault

SVC – Static VAR compensator

VDCOL – Voltage dependent current order limiter

WAMS – Wide area monitoring system

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1. Introduction

The purpose of this introductory chapter is to define the topic of the research and what it seeks to achieve. Apart from that, a short background and an explanation of the methodology and limitations found during the process are included.

1.1 Background

Due to human action, climate change and its consequences arise [1][2]. Population and energy consumption increases globally as well as pollution does. Therefore, humankind must find new ways of generate, manage and transform energy. Most authors and institutions state that electricity will have a dominant role in the future's energy system, so the electric power system must be upgraded in order to meet the future needs [1][2][3][4]

Among other objectives regarding social or economic issues, the European Commission (EC) has developed the "20/20/20" energy targets for mitigating climate change [3]. Recently, these targets have been updated for 2030 [4], which basically consist in achieve the following objectives:

- At least 40% cuts in greenhouse gas emissions (from 1990 levels)
- At least 27% share for renewable energy
- At least 27% improvement in energy efficiency

The framework seeks to achieve a low-carbon economy that ensures affordable energy for all consumers, reduces the dependence on energy imports and consequently provide environmental and health benefits

In order to achieve these goals, the use of renewable energies emerge as one of the cleaner, and currently cost-effective, measures that would lead to shift towards a sustainable future. Thus, the developing of Smart Grids, given that helps to increase renewables' penetration and increases energy efficiency, are a key point in the EC agenda [4].

Apart from environmental reasons, the high share of renewables and an increase on energy efficiency would lead Europe to become more energy independent. In this case, the energy supply will not depend on imports but will be generated in-situ.

Studies as [5] concluded that a 100% renewable system based on wind, solar and hydropower is feasible at a reasonable price, being electricity and hydrogen the unique energy carriers used. This research has been revised and criticized in [6], that states that the previous work has been based on invalid modelling tools, modeling errors and inadequately supported assumptions. More recent studies as [6] agrees that 80% penetration of renewables can be achieves at a reasonable cost, but the last 20% remaining is difficult and expensive to achieve. Based on [6] conclusions, a broader portfolio of energy sources, including nuclear, bioenergy and Carbon Capture and Storage technologies (CCS) can truly help to decarbonize the energy system in a realistic way. In any case, the integration of renewables will reduce the dependency on other countries, even though to become 100 % independent is not realistic at all at a cheap price.

Due to the variability inherent in renewable energy sources, as solar and wind energy, transmission grids will suffer bigger challenges as the share of RES increases. Highly controllable networks are needed in order to sustain stability. To upgrade the current network integrating power electronics and communications is crucial for being able to tackle future problems caused by generation-load unbalance in an energy system with high penetration of renewables.

The evolution of power electronics as HVDC connections, FACTS controllers, Phasor measurement units (PMU) and the decrease in Renewable energy sources (RES) prices are creating the perfect landscape for countries in order to renew their power networks. Wide-area measurement systems (WAMS) based on PMU's, whose reporting time is much faster than the usual SCADA system, allows the grid operators to see detailed dynamics of the system in real-time. Also, as the measurements are synchronized, grid operators can analyze the stability problem much better thanks to more accurate angle difference measurements. [20]

High-Voltage Direct-Current transmission can be more advantageous than traditional AC transmission in many situations. These systems are a suitable and more efficient option for subsea connections, connection of asynchronous systems and long-distance bulk power transmission, apart from specific projects [11]. That is another reason why HVDC-links are an important technology for integrating renewables, such as off-shore wind farms and solar-PV units. The main advantages are its lower energy loss, the capacity to interconnect asynchronous systems and high control capability that enhances network stability [7]. HVDC technology has, when suited, technical, economic and environmental advantages.

Therefore, both PMUs and HVDC will play a role in the managing of integrate renewable energy sources. The interaction of both systems with the rest of the transmission system under unbalanced situations still not deeply explored in some fields.

In the Nordic countries, many spread PMUs are already installed along their networks. The aim so far is to deeply understand electromechanical oscillations between countries. As can be read in [8], the subsequent action is that the damping control of SVC and HVDC devices will be based on PMU data.

After an event in the Nordic system, it was recently realised that HVDC converter commutation failures are not visible to TSO control room. This is unfortunate as the faults may excite power system dynamics. While the SCADA system is generally too slow for detecting commutation faults, using phasor measurement units (PMUs), due to its faster reporting rate, dynamics events of the system can be detected.

That's why a deeper understanding about how PMU's and HVDC-links interact, specifically how HVDC commutation failures are monitored by Phasor Measurement Units (PMUs), is needed. Therefore, this project aims to broaden the knowledge on this topic.

In the present days, algorithms to detect and locate faults based on PMU measurements have been developed already [9], [10] and [38]. On the contrary, location of HVDC commutation failures using PMU measurements has not been treated in literature. Commutation failures is an issue that is almost always analyzed from a "device perspective". AC events that can lead to a commutation failure in a HVDC converter have been studied [11]. On the contrary, how commutation faults affect the exterior network is not deeply understood yet.

1.2 Objectives

The main objective of this Master Thesis is to understand if commutation failures in HVDC converters can be characterized from PMU data.

Commutation faults are normally studied using waveform-simulation in software like PSCAD/EMTDC or MATLAB-Simulink [12], where electromagnetic transients (EMT) are simulated. On the contrary, dynamic phenomena in large systems are normally studied using phasor-simulation in software like PSS/E or DigSilent-PowerFactory.

A first step to combine these two perspectives and include commutation faults in phasor-simulation has been taken in [13]. The cited work focuses on the voltage dip that an AC disturbance creates along a big network. These voltages are compared with the critical voltage dip that lead to a commutation fault in a supposedly installed HVDC converter. How these commutation faults affect the AC system is not studied.

In the first part of the thesis, a model which include a single HVDC link and a PMU has been simulated with the aim to understand how PMUs behaves when a commutation faults happen. The simulation of commutation faults in the CIGRÉ standard benchmark HVDC converter have been carried out both in MATLAB-Simulink, PSCAD and PowerFactory (EMT). The simulations include different types of faults and fault impedances and provide AC signals and PMU signals.

The results are interpreted in order to identify characteristics in PMU data that make it possible to distinguish commutation faults from other disturbances. It is also important to highlight the differences between the simulation programs when simulating the behavior of the system. Physical reasons are given for explaining the behavior found in the AC side of the converter when commutation faults happen.

After understanding the implications of commutation faults in the outer AC network, analyze how these faults spread along a bigger network is highly interesting. In the CIGRÉ HVDC benchmark angle dynamics are excluded as the two AC systems are represented by voltage sources with fixed phase angles. Therefore, a simulation that includes the whole electromechanical dynamics of the system is needed.

The last aim is to point out the main differences in behavior when the HVDC converter is installed and when it’s not in order to define characteristics that could be used in detection and location algorithms based on PMU data in future work.

1.3 Methodology

With the aim of achieving these objectives, the following methodology has been followed:

After going through the theoretical documentation, several simulations have been carried out in MATLAB-Simulink, PSCAD. At first, the models used are based on the Benchmark models [27], [28], based on [15] and include a HVDC-link in a simplified network with AC sources at both ends and without focus on angle dynamics but the electromagnetic behavior of the system.

To start with, the PMU Model available in the MATLAB-Simulink library [29] has been upgraded, including the possibility of computing also negative and zero sequence, and simulated. Its performance is checked with the standard IEEEC 37.118 [21]. Then, a Single-line to Ground (SLG) fault and a Three-Phase fault along a transmission line model are simulated, the output is sent to the PMU model and the results are analyzed. That has been done in order to be able to highlight the main differences in behavior when the HVDC converter is installed.

After that, the CIGRÉ standard benchmark HVDC model has been simulated using MATLAB-Simulink and PSCAD, focusing on commutation faults. In the first step, the model is simulated under normal operating conditions. After the analysis of the results and the model, several AC faults, with associated commutation failures, are simulated in a modified model which includes more measurement points. The model's outputs are sent to the PMU model and both group of signals are analyzed and compared with the ones obtained from the transmission model. The result of the analysis aims to characterize commutation faults in the AC side of the HVDC model seen from a PMU perspective.

The next step is to simulate the inverter side of the converter, focusing on the delta configuration of the transformer, when a SLG fault happens and leads to a commutation fault. This has been done in order to corroborate the hypothesis that the delta configuration is the reason why the current behaves in a strange way in the AC side of the converter after commutation faults.

The results in the different simulators are analyzed and the main differences highlighted. The reasons of these discrepancies are also provided.

For the second part of the Thesis, a larger model (based on Nordic 32) is simulated in Digsilent-PowerFactory. In this case, the generators' angles are not fixed, as in the previous simulations, and the system is therefore more complex. Before simulating the HVDC converter in a bigger network, a simplified HVDC model is simulated in Digsilent-PowerFactory in order to understand the main differences in the behavior when compared to the MATLAB-Simulink and PSCAD simulations.

Then, the HVDC benchmark model available in Digsilent-PowerFactory is connected to external nodes within the Nordic 32 Network. The new model is tested under normal operation and when SLG faults are applied in the inverter bus where the converter is installed. Five PMUs are installed spread along the network. The PMUs computes frequency and positive and zero sequence of both current and voltage measurements. The computation of the frequency has been done based on PLLs. Three-phase simulations have been done as well, regarding the same principle.

Later on, the information is organized and presented in this report.

1.4 Limitations

Due to time horizon and regarding the scope of the Thesis, the following limitation have arisen.

The HVDC model used is based on the MATLAB-Simulink library example, which is sufficient regarding the scope of the project but could be more detailed, in any case, the model is built based on the CIGRÉ benchmark model [27]. The same happens with the PSCAD model [28], that is based on the library example provided in the software, and the model in DigSilent-PowerFactory [35]. This can be considered a limitation, as the model can be built with more detailed, but also strengthen the truthfulness of the simulation results, as the models are trusted.

In a similar way, the PMU block used for simulations is based on the MATLAB-Simulink library as well. The PMU model computes the positive sequence magnitude, angle and frequency variation of the phasors but also negative and zero sequence, which is not included in the default model. This has been done using sequence analyzers models, which are less accurate than the PMU model itself, as for the sequence analyzer the frequency is given as an input but it's not directly calculated.

Besides, must be said that no physical experiment has been done and all the results come from simulations.

Regarding the second part of the thesis, it would have been interesting to perform more simulations, varying the location of the PMUs and the converter connection point. But due to time restriction it hasn´t been possible.

A further analysis on this topic would be highly interesting. A deeper understanding regarding how commutation faults spread along a network and the reasons behind that behavior can be considered as the natural next step. The conclusions of this study can be used for developing a detection and location algorithm for commutations faults but it hasn't been implemented.

Lastly, it must be pointed out that no comparison with real data has been done. Definitely, this is something that must be done in future studies.

1.5 Thesis structure

In this subsection, the outline of the rest of the thesis is exposed. First, after the introduction, an extended background chapter regarding HVDC and commutation faults, sequence components for transformer banks, PMUs and methods that use PMU data for location of events come next.

The next chapter describe the simulators and models used during the whole process of the thesis. Focusing on the differences between the HVDC benchmark model of the three different simulators.

The rest of the thesis can be divided in two parts. The first part focuses on the interaction between HVDC converters and PMU´s, using a simple network for that purpose. Several simulations are carried out in PSCAD and MATLAB-Simulink in order to explain how commutation faults are managed by PMUs. First, simulations of a transmission line where PMU are installed is also included in order to understand the differences in behavior when the HVDC link is simulated.

After simulating the transmission line, the HVDC Benchmark model is simulated in MATLAB-Simulink and PSCAD. The simulations include SLG fault, Two-Phase fault, Two-Phase to ground, Three-Phase fault and converter failure.

In order to explain the reasons why the AC current behaves as it does when ground is involved in the fault, a system equivalent during commutation fault is simulated. The model focuses on the configuration of the transformer included in the HVDC model.

The second part focuses on how commutation fault spread along a big network and analyzes how PMU data can be used for detect and locate these faults. Therefore, the next chapter analyzes simulation results from Digsilent-PowerFactory. First, the simulation results of the HVDC benchmark model is included.

In order to summarize and point out important conclusions, a final discussion and conclusion chapters close the research. The discussion aims to conclude the findings from the first part of the thesis, while opening a new discussion regarding the results from the Digsilent-PowerFactory simulations.

The last part of the thesis includes the reference list and annexes.

2. Theoretical background

In this section, the basis of HVDC converters and PMU are defined, including a deep theoretical explanation of commutation faults. The focus is on Line Commuted Converters (LCC), or current based transmission, which is the technology that has been installed mainly in the past years. This technology dominates the existing HVDC installations and commutation failures are intrinsic to it. Other systems, as the newer Voltage Source Converters (VSC), are not considered in this study. These are highly interesting and have several advantages as the ability of exchange active and reactive power independently [17] but have very different behaviour during faults.

Apart from that, due to abnormal operation of the system when commutation faults happen, a theoretical explanation regarding symmetrical components in transformers is also included. This is needed as transformers have a decisive importance in the behaviour of the AC current that will be shown later on.

In this section, the theoretical basis of the electromechanical-wave propagation phenomena and fault detection and location methods based on it are also explained. These methods use PMU data, mostly angle differences and frequency variation in order to determine the location of a fault based on time-of-arrival of the electromechanical waves. Already developed methods are able to detect different kind of faults, but so far, none of them focus on commutation faults.

2.1 HVDC converters and commutation faults

A High Voltage Direct Current connection (HVDC-link) consists basically of a rectifier station, a DC-line, and an inverter station. Each station includes transformers and filter banks.

There exist a CIGRÉ HVDC benchmark model since 1991, proposed in [14], [15]. The model represents a 500-kV,1000-MW HVDC link. The converters are based on thyristors (12-pulse configuration with two six-pulse valves in series), transformers, harmonic filters, shunt capacitors and DC smoothing reactors. The model is connected to weak AC systems (Short circuit ratio 2.5 at 50hz). The simplified model can be seen in the Figure 1. The simulation of the system in MATLAB-Simulink has been done before in [12]

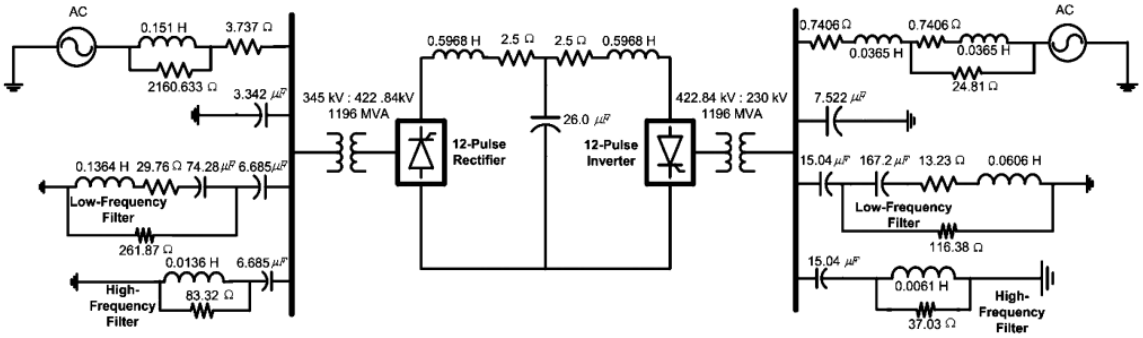

Figure 1. Single-line diagram of the CIGRÉ benchmark HVDC system [15].

LCC converters consume reactive power during normal operation, and that reactive power is supplied by shunt capacitors and other sources. The DC current is smoother thanks to the DC reactor [7]

HVDC transmission systems can be implemented using different configurations. This study will focus on 12-Pulse monopolar systems as in [15]. This configuration is widely used for undersea power transmissions [7]. A schema of the configuration cited can be seen in Figure 2.

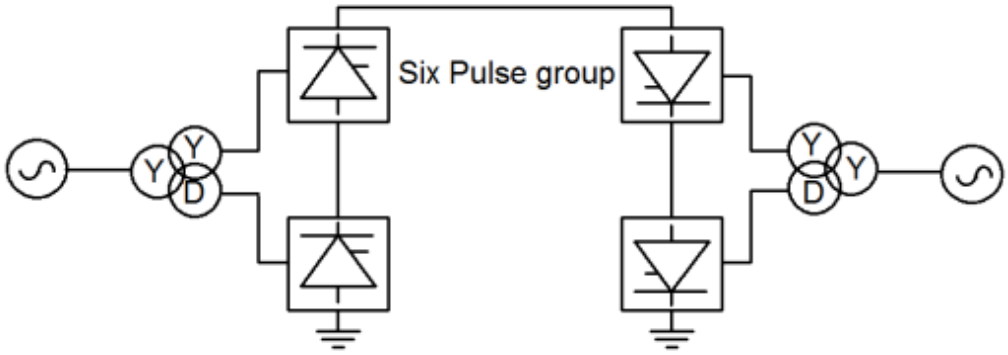

Figure 2. 12-Pulse Monopolar HVDC [7].

The working principle of the LCC converters is based on the Graetz bridge, which configuration can be seen in Figure 3. In the schema, the voltage sources of the AC network, thyristor valves, L, representing the commutation inductance, and L_d, that represents the smoothing reactor, are included.

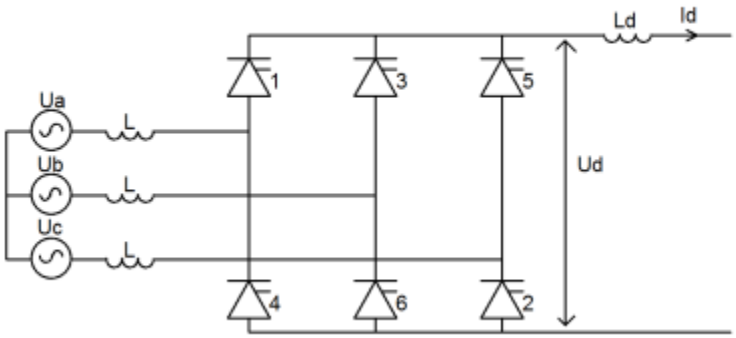

Figure 3. Basic 6-pulse converter [7].

When a valve, for example valve 1, is fired while it is also forward biased (its anode voltage is positive with respect to the cathode), conducts. When U_{ba} is in its negative cycle, valve 3 experiences a negative voltage across it (reverse biased) and cannot conduct current even when a firing pulse is provided. Valve three will conduct only when it is forward biased and also fired during that interval, in the same moment, valve 1 will have negative voltage across its terminals and stops to conduct.

The duration between receiving the forward voltage and start of conduction is usually expressed in angular measure and is referred to as firing or delay angle, α [7].

Theoretically, the delay angle ranges from 0° to 180°. In case the delay angle is between 0° to 90°, the converter operates in the rectifier mode. On the other hand, when the delay angle is between 90° to 180°, the converter operates in inverter mode. In practice there is a minimum delay angle of about 5o for rectifier and from 110° to 165° for the inverter [7].

When one of the thyristor valves stops conducting and another in the same row starts to conduct, it is called commutation. This duration of commutation is referred to as overlap time or angle of overlap, μ [7]. Consider the schema in Figure 4. When valve 1 and 2 are conducting and the direct current needs to be commutated from valve 1 to valve 3, that can only happen when the difference Ub - Ua is positive, this voltage difference is referred to as commutating voltage [7]

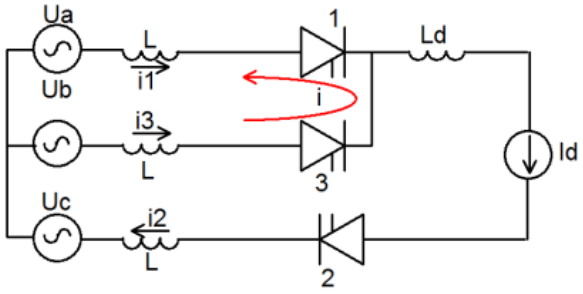

Figure 4. Equivalent circuit for commutation process [7]

Exactly during the commutation process, the converter bridge can be represented by the circuit in Figure 4. Valves 1 and 3 are both conducting during a short period of time, defined previously as overlap time, μ. As it can be seen in Figure 5, the commutation process is finished when the commutation current has increased and is equal to the direct current I_d. Being A (See figure 5) the inverter commutation margin. A reverse voltage is needed to be applied across the thyristor valve during some time in order to remove stored charge during the conduction process [7]

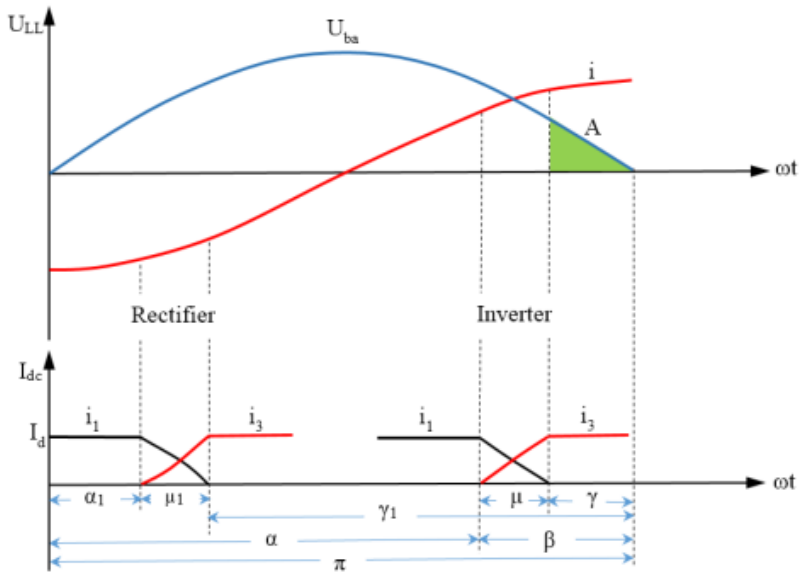

Figure 5. Commutation and angle relationships [7]

As described in [7], in the rectifier, valve 3 is fired at α_1 and the commutation of current from valve 1 to valve 3 takes μ_1.

The remaining time associated to γ_1, is more than sufficient for successful commutation. That is why commutation failures rarely occur in the rectifier [7]. In the inverter, valve 3 is fired at α and the commutation of current from valve 1 to valve 3 takes μ. The remaining voltage-time area A (commutation area) can be greatly reduced in the event of disturbances in the AC network. That is one of the reasons because AC faults applied on the inverter side are more likely to cause commutation failures [16]. When an AC fault happen, U_{ba} is reduced, therefore part of the commutation area will be used for the commutation. Gamma (γ) is called extinction angle or commutation margin and represents the time between when valve 1 is extinguished and when the commutation voltage goes through its zero crossing. In case the commutation has not completed when U_{ba} crosses zero, the commutation failure is a fact.

During steady state operation, the relationship between these angles is as shown in Equation 1.

$$\alpha + \mu + \gamma = 180^o \quad (1)$$

Abnormal operation situations, as commutation failure events, must be taken into special account. These events are likely to happen when AC disturbances occurs, even more likely when these disturbances are located in the inverter side of the converter [16]. More specifically, are caused due to voltage magnitude reduction or/and phase shift that leads to an insufficient remaining voltage-time area after a firing. Commutation faults can also be caused by an increase in the direct current or a hardware malfunction in the firing control [7]. In conclusion, the most severe cause of commutation failures are unsymmetrical faults in the inverter side, as it leads to both voltage drop and phase shift (No phase shift if symmetrical fault). The converter needs to operate with a commutation margin, γ, big enough for decreasing the chance of commutation fault without generating too many losses for that reason. Furthermore, commutation failure can be avoided by temporarily increasing the commutation margin just before a planned switching action [7].

The normal firing sequence of the thyristor valves in the rectifier/ Inverted, as in Figure 6, is altered and therefore the power transmission is interrupted for a short period of time, fact that generates stress in the converter valves and shorten their lifespan [11].

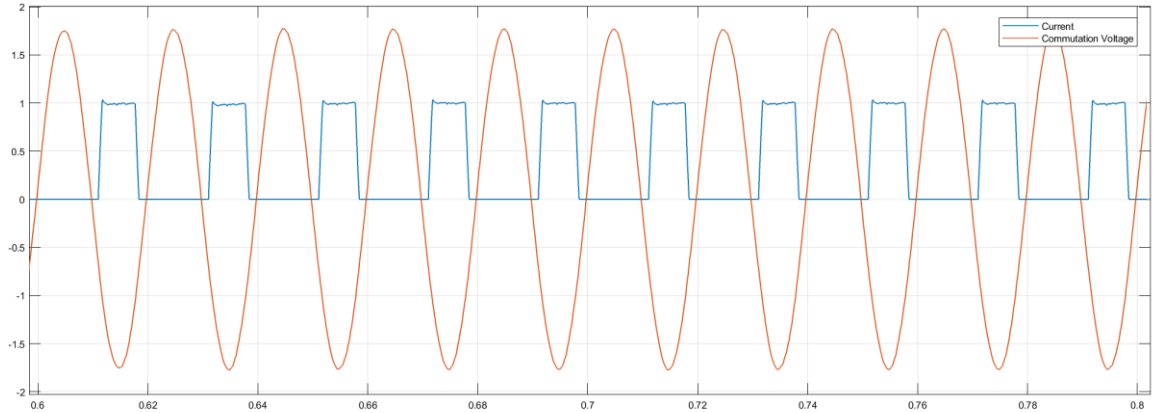

Figure 6. Normal commutation. Commutation voltage (Orange) and current through valve 1 (Blue) in Simulink model

It can be considered as the failure to complete commutation before the commutating voltage reverses, allowing a sufficient margin for de-ionization. As it can be seen in Figure 7, valve 1 is not extinguished before the voltage reverses. Valve 3 extinguishes before arriving to the steady current due to external perturbations and Valve 1 will continue conducting.

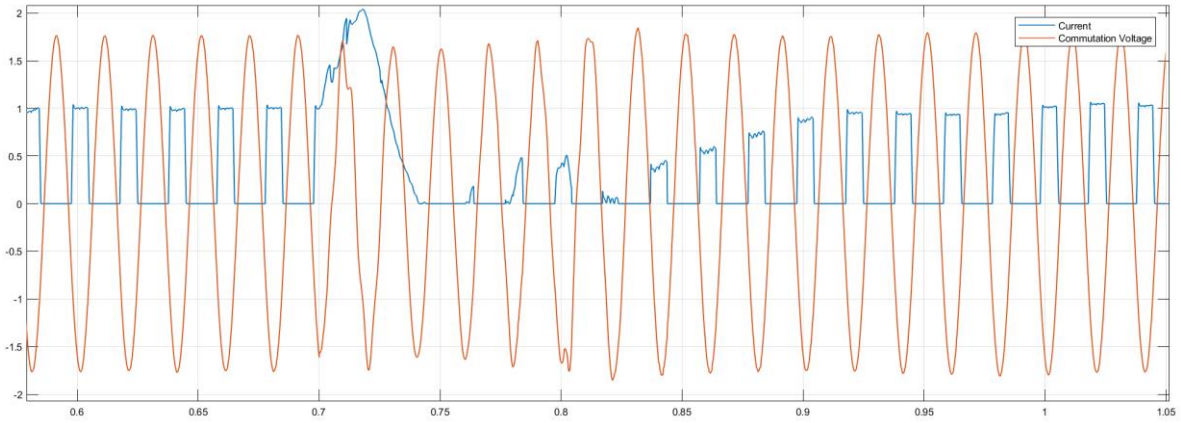

Figure 7. Commutation failure. Commutation voltage (Orange) and current through valve 1 (Blue) in Simulink model

In Figure 8, it can be seen the same signals, but in this case the commutation failure has happened in a different valve. In any case, the power through the converter still interrupted.

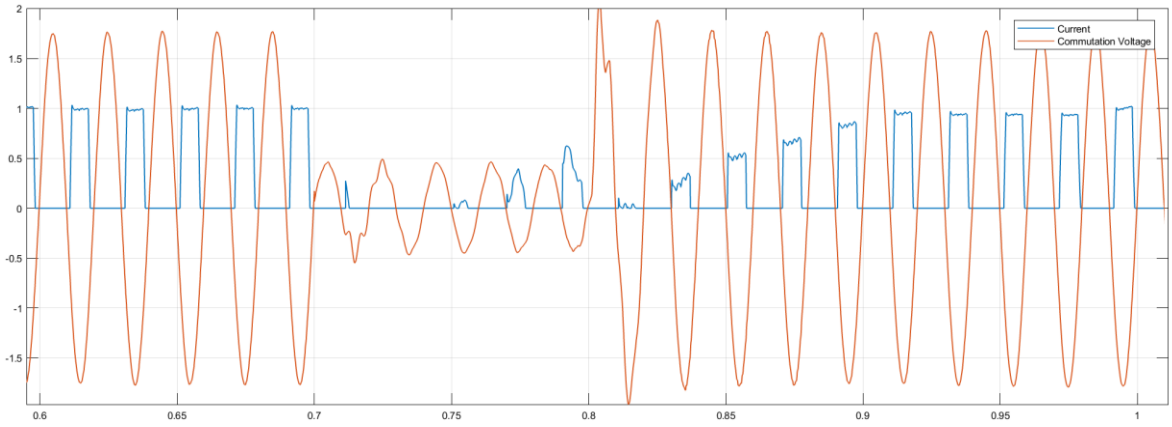

Figure 8. Interrupted commutation. Commutation voltage (Orange) and current through valve 1 (Blue) in Simulink model.

The HVDC converter include several control systems that aims to fulfill the following requirements [7]:

- No steady state error in the ordered current.
- Fast response of the control system to any AC or DC system disturbance.
- Fast reduction of over voltages and short circuit currents across and through the converter valves respectively.
- Stable system operation whenever transients occur on either the AC networks or the DC link.
- Minimize the occurrence of standing commutation failures during faults and ensure prompt restart of the HVDC system without the development of commutation failure.
- Operation with minimum reactive power consumption.

The basic converter control structure can be seen in Figure 9 and consist of several subsystems: power control unit (PC), voltage dependent current order limiter (VDCOL), which task is to assure stability, current control amplifier (CCA) that outputs an order for the firing angle. converter firing control (CFC), that generates the valve control pulses and a current measurement unit (CMU).

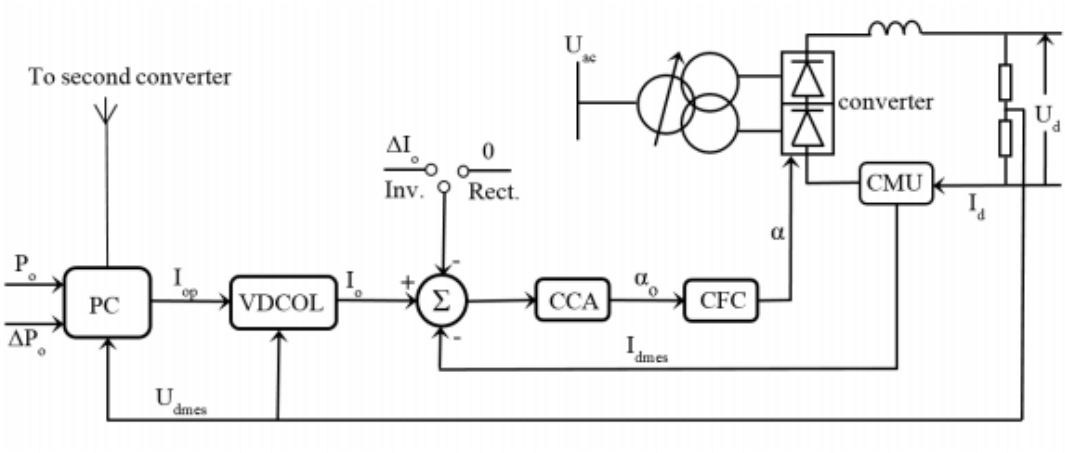

Figure 9. Basic converter control system. Source [7]

Conceptually, a power order, Po, is received by the power control unit (PC) from the HVDC master control. PC produces a current order, I_{op}. This current order is then sent to the VDCOL, where is reduced to maintain stability during transient disturbances [7]. The output, I_o, is a current order but limited by the DC voltage. That signal is compared with I_{dmes}, from the current measurement unit (CMU). Depending on the difference, the converter firing control CFC generate the firing pulses for the converter valves.

The converter also includes a specific control system to prevent commutation faults and reduce their impact. The name of the control is CFPrev and consist on a predictor that actuates when there is risk of commutation fault, and a detector that prevent further commutation faults when one has already happened. The control system decreases the maximum delay angle limit in order to increase the commutation margin during and after the fault [7].

It is also important to mention the contribution of the Low AC Voltage detection control system. The LACVD detects AC faults and turn off the DC Fault protection that should not detect a DC fault even if the DC line voltage dips, as the dip is due to an AC fault [7].

The response of the system to DC and AC faults as well as the influence of the AC system strength on this interaction has been studied by Kundur [11].

2.2 Sequence connections for transformer banks used in HVDC links

In practice, a common configuration for HVDC converters is the one that provide 12-pulse signals. For achieving that, two bridges are connected in parallel, from the AC perspective, and in series on the dc side. As can be seen in Figure 10, two banks of transformers, one Y-Y and the other Y-Delta, are used to connect the bridges. The Wye winding located on the network side is usually grounded, as it is also in the models used later on. Due to this configuration, the three-phase voltages supplied at the bridges are displaced 30°, producing a more sinusoidal signal. In addition, fifth and seventh harmonics are effectively reduced [11]. The transformers also provide galvanic isolation.

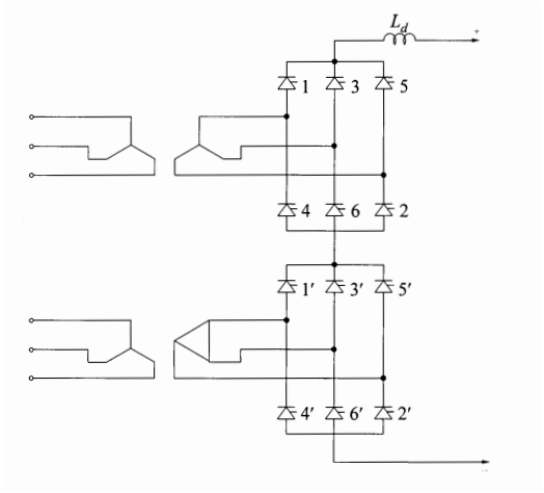

Figure 10. 12-Pulse configuration for HVDC converters [11].

It has been genuinely spotted that the configuration of transformers used in HVDC-links plays a key role in the behaviour that the AC current has when a commutation failure happens in the converter. Therefore, an explanation of how transformer behaves during unbalance operation is needed in order to clarify the causes of the behaviour found in the AC current.

As commutation fault are generated mostly by unbalance faults at the inverter side of the transformer [16], the positive, negative and zero sequence networks for a three-winding transformer, as used in the HVDC-link models, is provided in Figure 11.

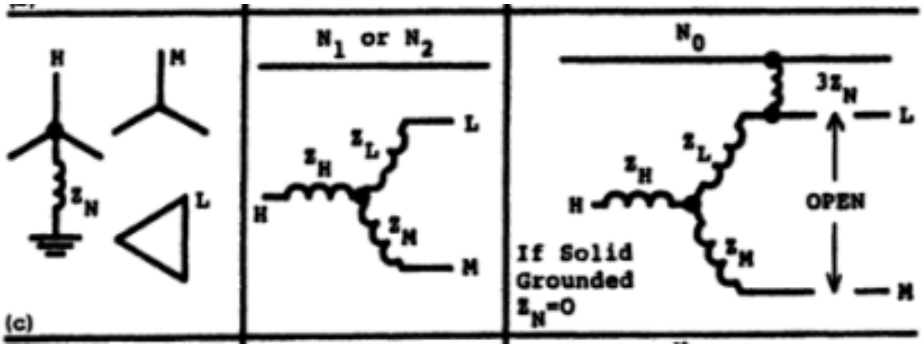

Figure 11. Sequence models for a Three-winding transformer with grounded wye, delta and wye configuration. On the left, the transformer configuration. In the center positive and negative sequence with the neutral above. On the right, zero sequence network with the neutral above [18]

2.3 Phasor Measurement Units

A Phasor Measurement Unit (PMU) is an electronic measurement device that presumably will have an important role in the future power grid [19]. Using a common time source for synchronization, generally a GPS, computes, a phasor associated with a three-phase voltage or current signals. Normally computes at least the positive-sequence phasor associated but can also compute the negative and zero sequence as well.

As different PMU are synchronized with the same GPS signals, the measurement from locations that are spatially far away, can be compared, and their angle dynamics analyzed. This is the innovative factor that PMUs introduce in comparison with the current monitoring system. Also, the reporting rate of the PMU is much higher (between 1 and 60 samples per second) and allows grid operators to analyze the system's dynamics more accurately. Wide Area Measurements (WAMS) are composed of Phasor Measurement Units (PMUs), high-speed communication channels and Phasor Data Concentrators (PDCs) [20].

The internal structure and the method for computing the phasor may vary between commercial models [20]. The output of a PMU is known as a synchrophasor and all information related can be found in the IEEE 37118 standard [21]. It defines synchrophasor, the synchronization and performance requirements and how to assess its compliance under both static and dynamic conditions.

The current uses of PMU are real-time monitoring and off-line analysis. In the future the idea is that this could be used for control and protection purposes as well, features that still under study but have been implemented for specific purposes [10].

An example of a commercial model is the RES670 - Phasor measurement unit by ABB (See Figure 8). The device is used for real-time monitoring and wide area monitoring, protection and control. The RES670 computes phasors from AC measurements. The device provides up to 32 analog phasors in two different data streams. The phasors can represent a single-phase phasor or positive, negative and zero sequence phasors. The device can be synchronized with the Global Positioning System (GPS) or IRIG-B. The measurements fulfill the IEEE C37.118.1-2014 requirements. Regarding communications follows IEC 61850-8-1, IEC 61850-9-2 and DNP3.0. [22]

Figure 12. ABB RES670 Phasor measurement unit

The device can be easily integrated in a substation and also include several protection and control functionalities.

2.4 Fault detection and location methods based on sparse PMU measurements

Previous studies as [37], [39] focused on electromechanical perturbations generated by load or generation changes, generator outages and line flow perturbations.

New research as [8], [9] use PMU data for detection and location of faults. As well as [23], [24] and [26] that use PMUs, integrated in a Wide Area Measurement System (WAMS) for monitoring the power grid. All those uses of PMU data are mainly based on electromechanical wave propagation principles and uses time delays for detection and location of faults within the system as well.

As mentioned in [23], Researchers found delays detecting frequency variations at observation points that were located far from the event location compared to closer observation points [38]. This is because the electromechanical wave propagates with a finite propagation speed, ranging from 200 to 1200 miles per second depending on grid characteristics, but, in any case, much slower than the speed of light [39].

Using that fact, event locators has been developed based upon the Time Difference of Arrival (TDOA or TOA depending on bibliography) of the electromechanical waves and triangulation schemes [9], [23], [26]. Different events can be distinguished as they cause different generation-load profiles that is reflected in frequency, and voltages, magnitude and angle [23]. In any of the cases, commutation failures or more specifically, AC faults together with commutation failure associated, have not been included.

3. Modelling tools and simulation models

3.1 Simulation tools

3.1.1 PSCAD/EMTDC and PSB/Simulink

In the first part of the thesis, an HVDC-link model is simulated using two different software; PSCAD/EMTDC and MATLAB-Simulink. Therefore, it is important to highlight their main differences and common features. The main idea is to compare both simulation outputs and determine if represent the same physical principles.

PSCAD/EMTDC is a simulation software used for simulating power systems and its controls. The main use of the software is time domain analysis of transients. The program uses a graphical user interface for drawing electrical circuits and equipment models. Both electromagnetic and electromechanical physical aspects are considered in the differential equations used. In order to solve these equations, nodal analysis and fixed integration time trapezoidal integration are the techniques used. [12]

MATLAB/Simulink is a multidisciplinary simulation software used in a wide variety of fields. The program includes a design tool called nowadays Simscape Power Systems, previously System Blockset (PSB), specifically developed for modelling and simulating power systems. The blockset includes components and devices used in electrical power networks and describe both electromagnetic and electromechanical physical behaviours. In this case, the system equations are solved using state-variable analysis using either fixed or variable integration time-step. [12]

It can be roughly said that PSCAD allows the user to define a more detailed model. Already built component models are really precise and include more parameters and components than MATLAB-Simulink. On the other hand, MATLAB-Simulink is more flexible and can be used for more purposes that only power systems. Another fact interesting to point out is that PSCAD/EMTDC has only waveform representation of voltages and currents, while MATLAB/Simulink has either that option or phasor-based representation Apart from that, MATLAB-Simulink offers the possibility of using different integration algorithms and is very intuitive for the user. Usually PSCAD/EMTDS is used as an industry standard for HVDC simulations while MATLAB is considered a multi-purpose simulator and widely used in academia. In PSCAD, there is also a feature that allow the execution of the model in RSCAD/RTDS, permitting Hardware-in-the-loop simulations.

3.1.2 Digsilent-Power Factory

Digsilent-Power factory is computer aided engineering tool for the analysis of transmission, distribution, and industrial electrical power systems. The software uses single-line diagrams for power system modelling but can also include controls and dynamic models. Power Factory uses both graphical environment and code, fact that make it flexible and intuitive. The software can be used for real time simulations and testing features are available but the most widely used functions are load-flow calculation, short-circuit calculation, harmonic analysis, protection coordination, stability calculation, and modal analysis [31].

Simulations can be carried out under the RMS mode, when focusing on system stability, or EMT, when the electromagnetic transients are critically important. The RMS simulation is phasor-based while the EMT represents the full waveform signals, similar as simulation tools explained before.

3.2 Network models

First of all, how the different simulators and models interacts is explained in this section. Simulations has been carried out in different software as MATLAB-Simulink, PSCAD and PowerFactory. The results of the simulations have been sent to MATLAB workspace for plotting purposes. After simulation of the CIGRÉ HVDC benchmark, both in MATLAB-Simulink and PSCAD, the waveform signals are sent to the PMU model, developed in MATLAB-Simulink, as an input. The PMU model provide the sequence phasors related to the input signals and send them to MATLAB workspace again for plotting.

3.2.1 CIGRÉ HVDC benchmark

Finally, the HVDC Cigré benchmark model is simulated in MATLAB-Simulink, PSCAD and DigSilent-PowerFactory. The models used are based on the ones available in the software libraries [27][28][35]. The parameters have been kept unchanged, and differ from one simulation software to another, but in both cases are coherent with the rest of the system (Components' rated values) and the benchmark. Therefore, the signals must be compared qualitatively, focusing on the shape of the signals and behaviours found, but not comparing the magnitudes itself.

3.2.1.1 MATLAB-Simulink

The 12-pulse HVDC benchmark model in MATLAB-Simulink can be seen in figure 13. The model follows the benchmark defined in [15]. For the implementation of the model, the three-phase three-winding transformer has been built using three single phase three-winding transformers. As can be seen in the default configuration. The model is prepared for fault simulations, that are turned off by default. The generators are considered fixed and with 60hz and 50hz for rectifier and inverter respectively as operational frequencies by default. The rectifier side generator has been reconfigured for working at 50hz, as the filters and transformer.

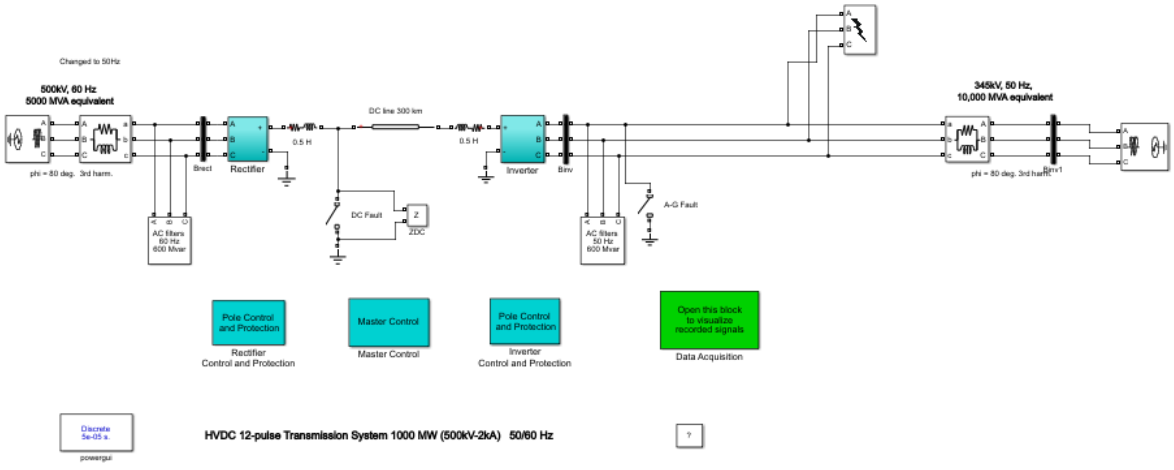

Figure 13. HVDC benchmark model in MATLAB-Simulink [29]

When comparing with the rest of the models, the model available in MATLAB-Simulink is pretty accurate. One of the comments that can be said are that when defining the bridges, PSCAD has more options and parameters available to modify. The control systems can be seen in the Annex A (Figure 69).

3.2.1.2 PSCAD

In the same way, the model used in PSCAD can be seen in Figure 14.

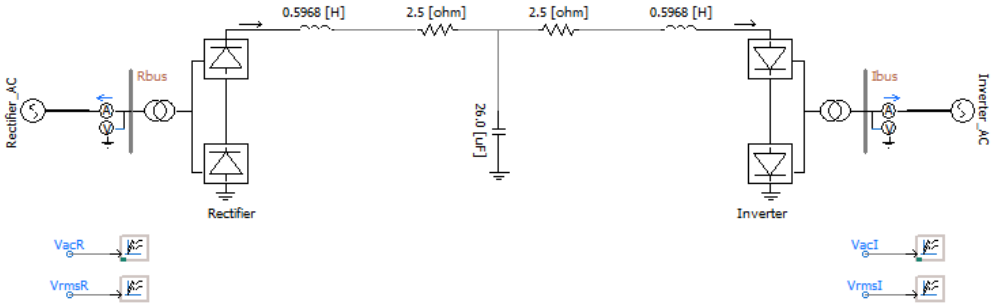

Figure 14. HVDC model in PSCAD [30].

A more detailed schema of the inverter side can be seen in Figure 15. It can be seen how the transformers are defined taking into account their winding configuration and grounding in detail.

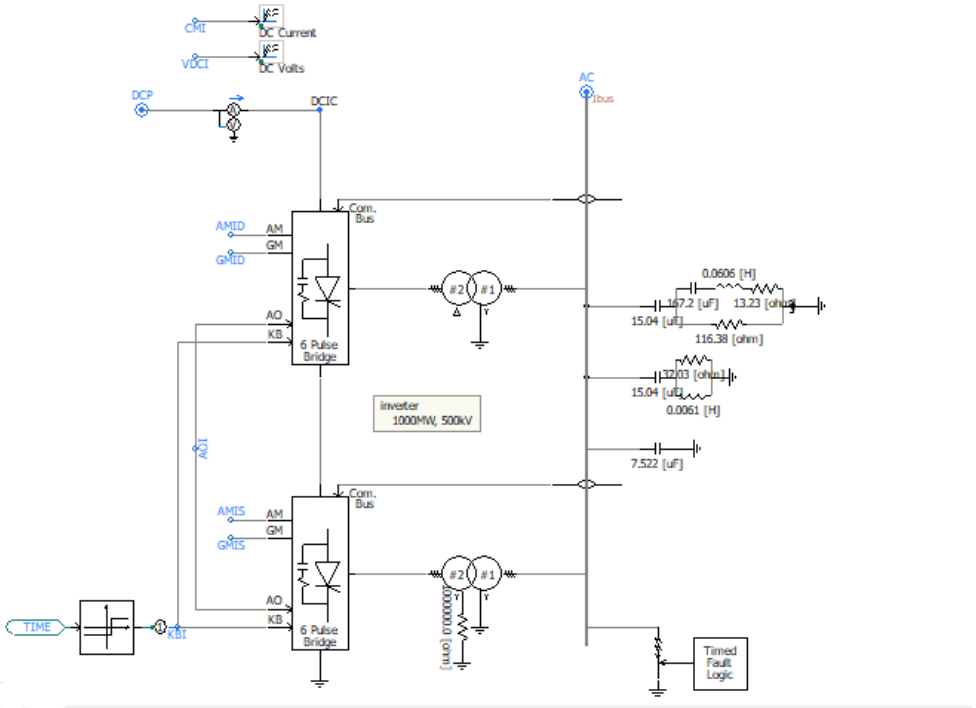

Figure 15. HVDC model in PSCAD. Inverter details [30].

The control loops can be seen in the Annex (Figure 68).

3.2.1.3 DigSilent-PowerFactory

Finally, the HVDC model used for the DigSilent-PowerFactory can be seen in Figure 16.

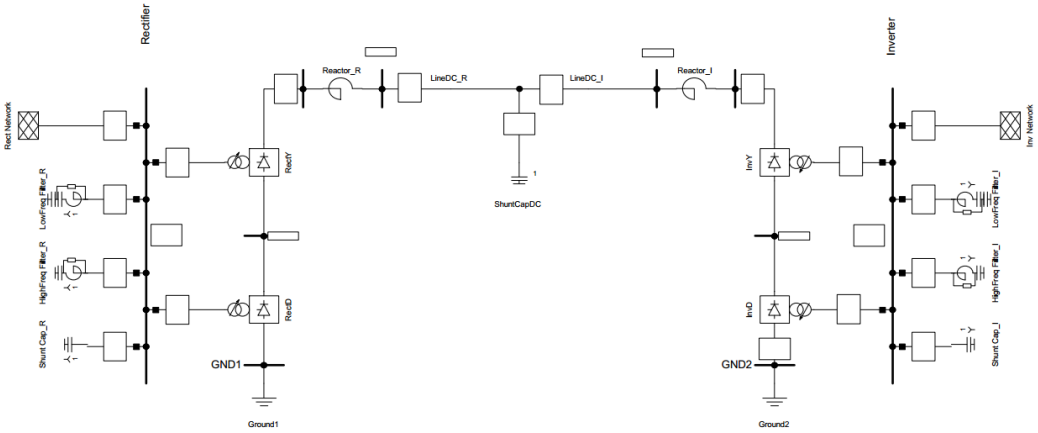

Figure 16. HVDC model in Digsilent-PowerFactory. [35]:

In this case, the delta transformer is only defined by its characteristic phase shift of thirty degrees, but not more parameters are considered [35]. Therefore, the sequence networks that are dependent on the configuration of the windings are not defined. This fact makes the author consider this model the less accurate.

In the model, apart from the single line diagrams, control loops and interactions between models are also defined. First, a composite frame is built. The frame defines the relation between different elements of the system, using only graphical representations. In Figure 17 can be seen the composite frame of the HVDC controls. With the inverter loop on the bottom part and the rectifier loop above.

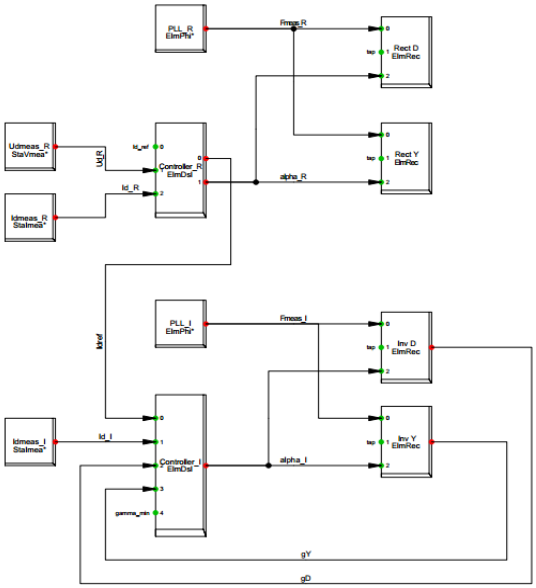

Figure 17. HVDC model in Digsilent-PowerFactory. HVDC controls (Composite frame) [35]

Later on, the inverter and rectifier controls are individually defined using a composite model, that is linked to the previously created composite frame. The rectifier controls can be seen in Figure 18 and the inverter controls in Figure 19 respectively.

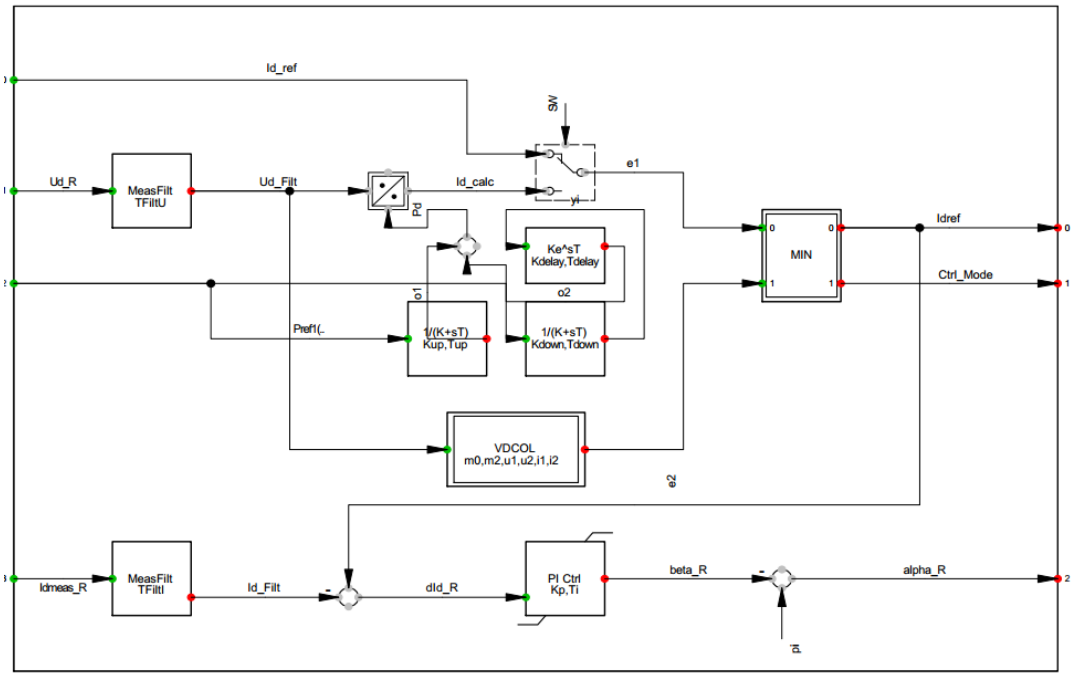

Figure 18. HVDC model in Digsilent-PowerFactory. Rectifier controls (Composite model) [35]

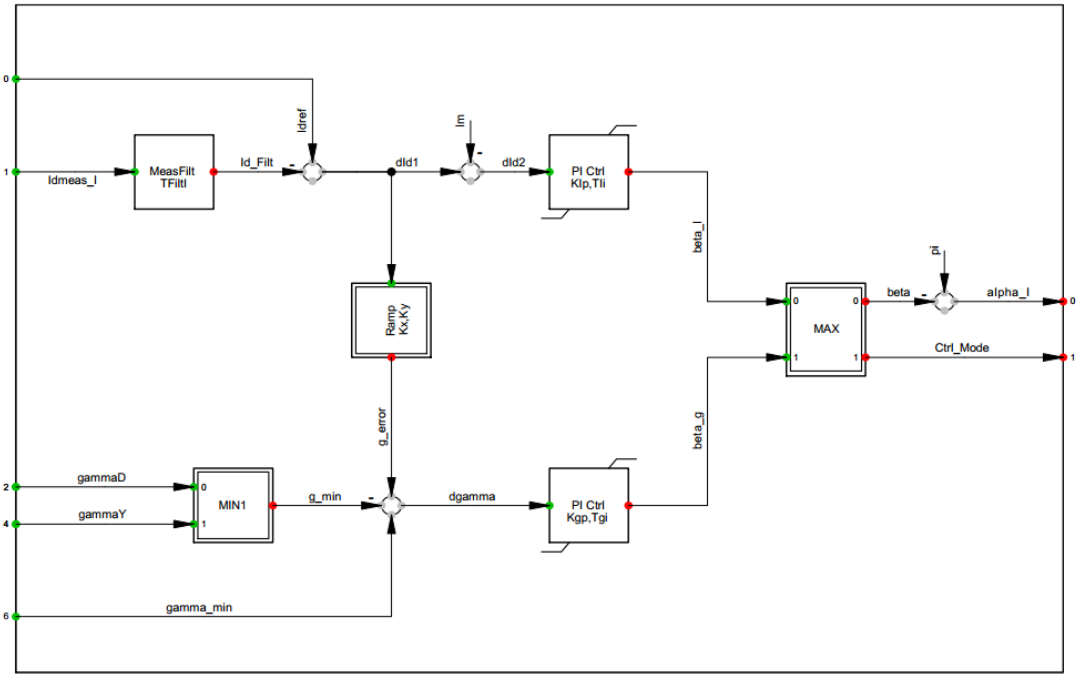

Figure 19. HVDC model in Digsilent-PowerFactory. Inverter controls (Composite model) [35]

3.2.2 Nordic 32

In the base model [32], the system was divided in the following six areas: External (400kV grid), North (400kV grid), Central (400kV grid), Southwest (400kV grid), North (130/220kV grid), Central (130kV grid). The model contained in total: 32 nodes, 23 synchronous generators, 52 lines, 17 transformers, 11 shunt impedances and 22 loads. The model has been used for transient stability studies.

From the original version, nodes 1011,1012,1013 and 1014 were arbitrarily removed in order to have enough nodes available for installing the HVDC. As the number of nodes is limited in PowerFactory when using the student license. The HVDC converter has been simulated when installed in two different places, Node 4042 and Node 4063, where the inverter of the converter has been located. Apart from that, basic PMU models, based on PLLs, have been installed in nodes 4045 (PMU 1), 4051 (PMU 2), 4062 (PMU 3), 4063 (PMU 4) and 4042 (PMU 5). A schematic model of the system can be seen in Figure 20.

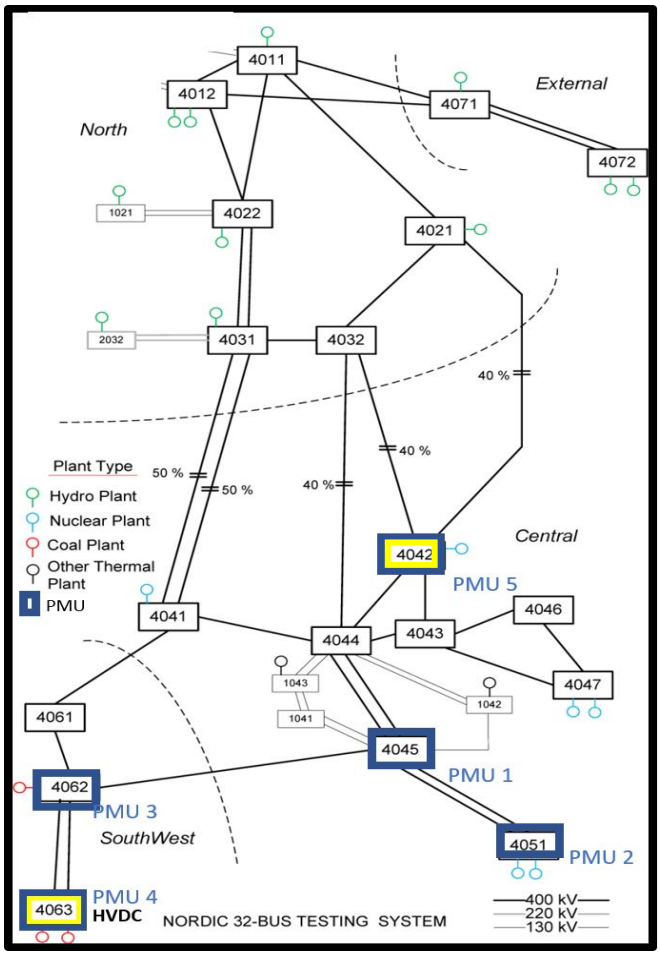

Figure 20. Modified Nordic32 network including alternate locations of HVDC converters operating in inverter mode

The original version of the network model can be seen in Annex (Figure 70). It is basically the same but with the nodes previously mentioned not removed and no PMUs or HVDC installed

3.3 PMU model

The PMU model available in the MATLAB-Simulink [29] library is based in PLL's and computes the positive-sequence component of a three-phase signal containing a series of events in the input signal as unbalances, harmonics and frequency modulation. Two sequence analyzers [30] have been incorporated to the model in order to compute also negative and zero sequence phasors, the Simulink model can be seen in Figure 21. Several parameters can be tuned, as the nominal frequency of the signals (50/60), the sampling rate (64/48/24 points per cycle) and the reporting rate.

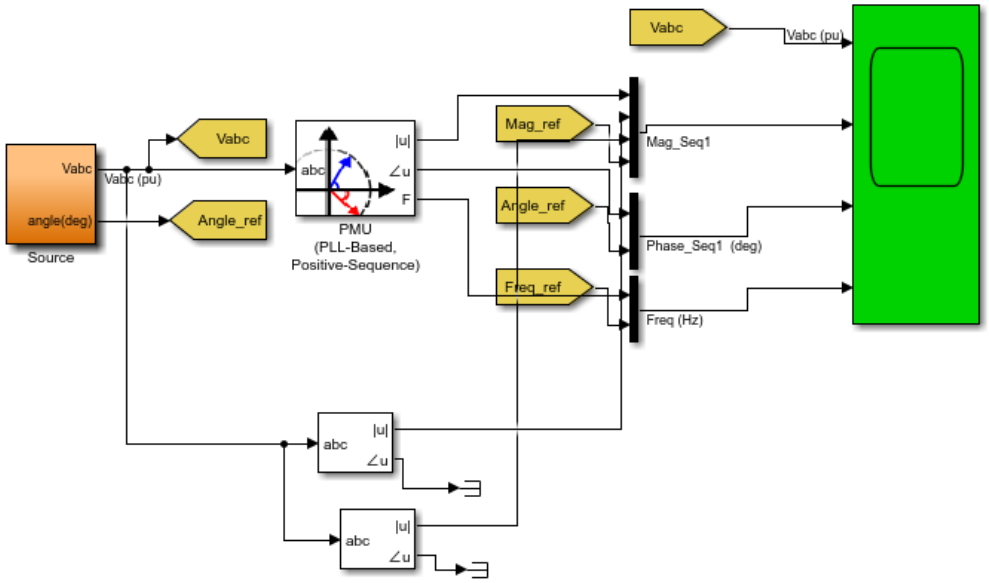

Figure 21. Model for testing the PMU block, based on [29]

In Figure 21, a block diagram that represents the PMU modified model is shown. The model uses the Fourier transform and fulfill the requirements of the standard IEEE Std C37.118.1-2011 [21]. As said in the manual, under subsynchronous conditions, the phasor estimation may present erroneous results [29]. By default, the model only computes the positive sequence phasor of the signal, additionally, sequence analyzers have been installed in order to also compute negative and zero sequence. How the PMU block works can be seen in Figure 22.

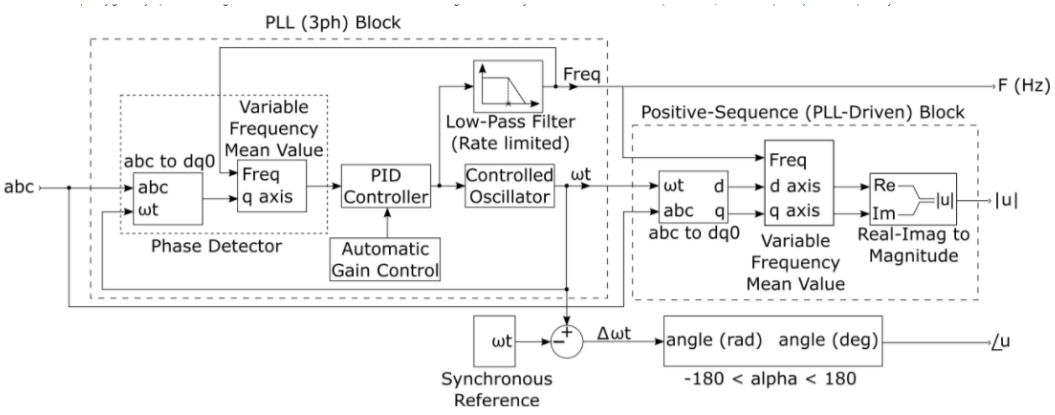

Figure 22. PMU model in detail [29].

For the sequence analyser, frequency is not input but a parameter of the model, and its conceptual architecture can be seen in Figure 23. It can be seen that it's based on Fourier transformations as well.

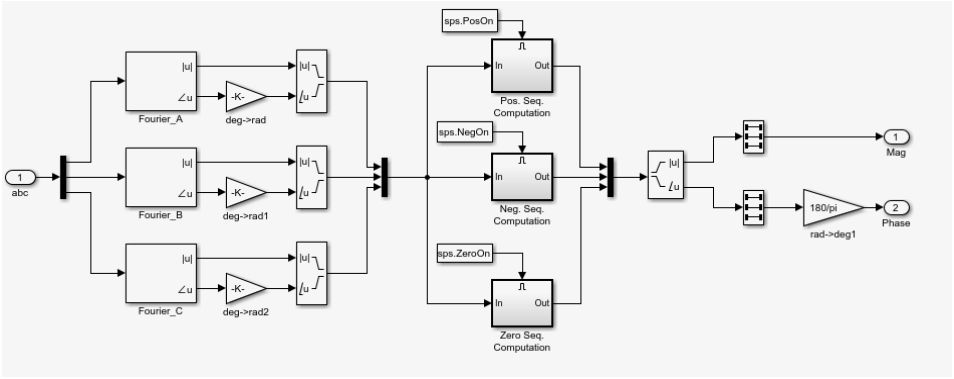

Figure 23. Sequence analyzer model in Simulink [30].

In the Figure 24, it can be seen the input test signal above and the output from the PMU below. Including the positive, negative and zero sequences magnitude, phase and frequency changes during the simulation time. More specifically, the programmable voltage source, that is used as test signal generator, at t=0 has Positive-sequence voltage = 1 pu and phase 0 deg. Between 0.2 s <t< 0.4 s the Positive-sequence voltage falls to 0 pu. In t > 0.5 a sinusoidal frequency modulation (58/62 Hz Freq = 1 Hz) is applied. During the interval 1 s<t< 1.5 s unbalanced condition (0.4 pu of negative-sequence and 0.3 pu of zero-sequence, no harmonics) are added. In t=1.75 s a phase shift of -90 deg is introduced. Lastly, in t > 2 harmonics without unbalance (20% 3rd + 30% 4th) are added (See figure 24).

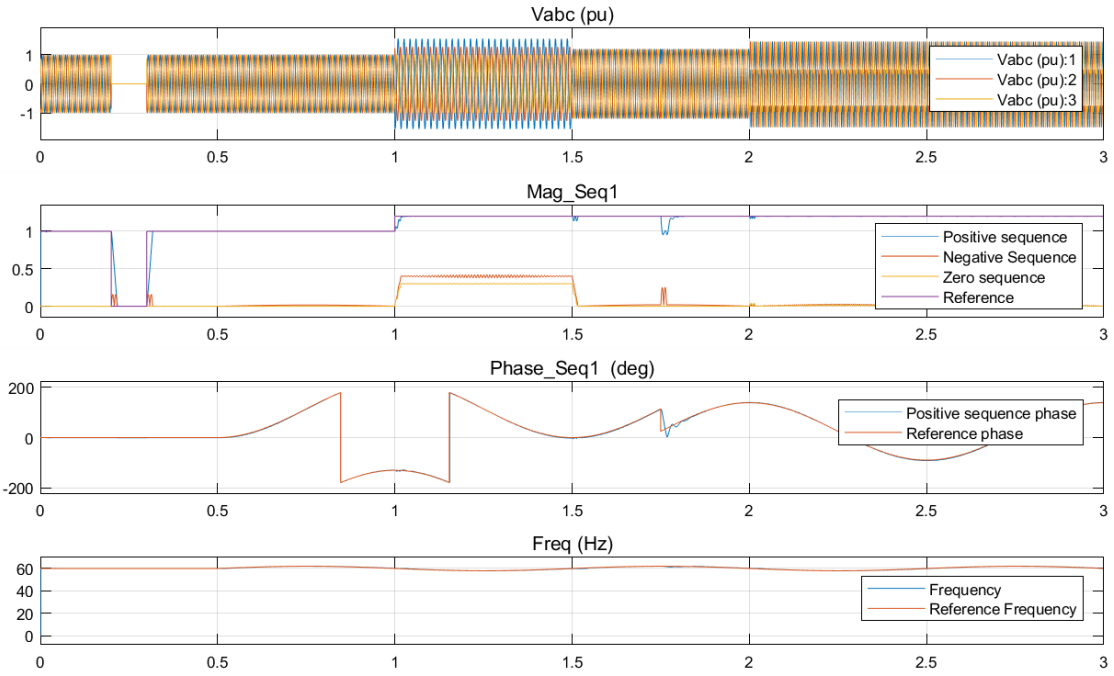

Figure 24. PMU benchmark model simulation with test signal. At t=0 has Positive-sequence voltage = 1 pu and phase 0 deg. Between 0.2 s <t< 0.4 s the Positive-sequence voltage falls to 0 p.u. In t > 0.5 a sinusoidal frequency modulation (58/62 Hz Freq = 1 Hz) is applied. During the interval 1 s<t< 1.5 s unbalance (20% 3rd + 30% 4th) are added. First graph shows the AC voltage, the second one the PMU output and then phase of the positive sequence phasor and frequency respectively.

Finally, compare the reference signals (orange) and the PMU signals (blue for positive sequence) of frequency, magnitude and phase. The simulated events include phase shifts, the addition of harmonics and the injection of negative and zero sequence components. The results vary when the reporting rate factor and sampling rate changes, but the default values have been used [29]. The results of the model simulation are satisfactory.

4. Commutation faults in CIGRÉ HVDC benchmark model

This chapter includes the simulation results of HVDC systems installed in a simple network.

First, SLG and Three-Phase faults along a transmission line model are simulated, the output is sent to the PMU model and the results are analyzed. Therefore, the results show both the AC profiles and the PMU output when the faults occur. These simulations have been done in order to understand how that faults appear in the PMU output and, later on, be able to distinguish between AC faults and commutation failures.

Later on, a model that include a HVDC-link and a PMU is simulated under several conditions. First, the HVDC converter is simulated under normal operating conditions. Then, several SLG faults are simulated along the system and their impact on the commutation process is shown. Two-phase, two-phase to ground and three-phase faults are also applied. The simulation of an internal failure in a converter bridge, where the whole bridge is disconnected, has also been carried out.

After simulating the HVDC-link, a model that ideally simulate the behavior of part of the system when commutation faults happen is built. This model includes a voltage source, line, filters and transformer (Wye grounded – Delta) as if it was the HVDC-link. But, instead of the inverter, circuit breakers are installed. When the circuit breakers open the circuit, the behavior of the system represents a blocked HVDC converter because of commutation failures. The role of the transformer configuration is key in order to understand the behavior of the AC signals when a commutation failure happens.

The main aim of the chapter is to understand the behavior of the AC system when commutation faults happen in the HVDC converter and the physical reasons behind its behavior. The PMU signals represents the AC measurements and therefore also the different behavior found.

To compare the simulation outputs when using MATLAB-Simulink and PSCAD is also highly interesting. Therefore, the simulations have been replicated in PSCAD in order to assess how similar the results are. After the simulation in PSCAD, the signals are also sent to the PMU model and its output is analyzed.

4.1 Faults in a transmission line with a PMU installed

The aim of this simulation is to characterize SLG and three-phase fault without a HVDC converter in order to be able to compare the behaviour when the HVDC converter is installed later. This comparison will be made both using the AC signals and the output from the PMU. The model used in MATLAB-Simulink can be seen in Figure 25. The transmission line is modelled as a parallel RL branch with R=6.205 ohms and L=12.9e-3 H. The fault is applied using the Three-Phase fault block available in the library.

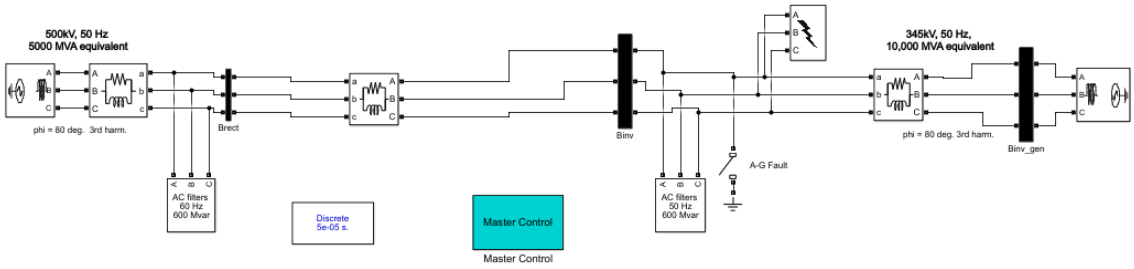

Figure 25. Transmission system model

First, a SLG fault is applied in the middle bus (Bus 2 or Binv) at t=0.7 s and cleared at t=0.8s. Please notice that in this case there are neither inverted or rectifier installed, but later on the line will be substituted by a complete HVDC-link. Only the signals as seen from the bus2 are shown in this section. Figure 26 shows the AC current and voltage at Bus 2 and the PMU signals related to the AC measurements.

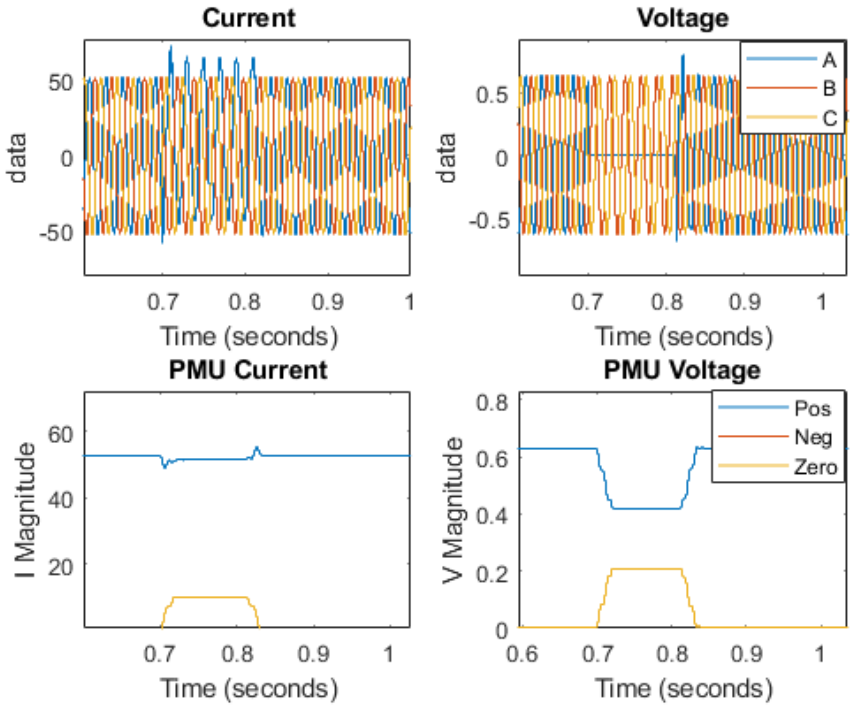

Figure 26. SLG fault in transmission model in MATLAB-Simulink. Fault applied at t=0.7 and self-cleared at t=0.8 in bus2. Positive, negative and zero sequence Current(left) and Voltage (Right).

Based on these simulations, when treating the waveforms using a PMU, a dip in the voltage positive-sequence magnitude can be seen in figure 26. This dip is as maximum 1/3 of the total (1 p.u) as one line is completely out of service for a while. The current positive sequence magnitude also suffers disturbances but in the shape of a dip-and-peak. Disturbances in angle and frequency are restored after the clearance of the fault. Due to the nature of the SLG fault, zero sequence components are not null.

The next case is similar to the previous one. But, in this case, a Three-phase fault is applied in the middle bus at t=0.4 s and seen from the same location. The fault is cleared at t=4.1 s.

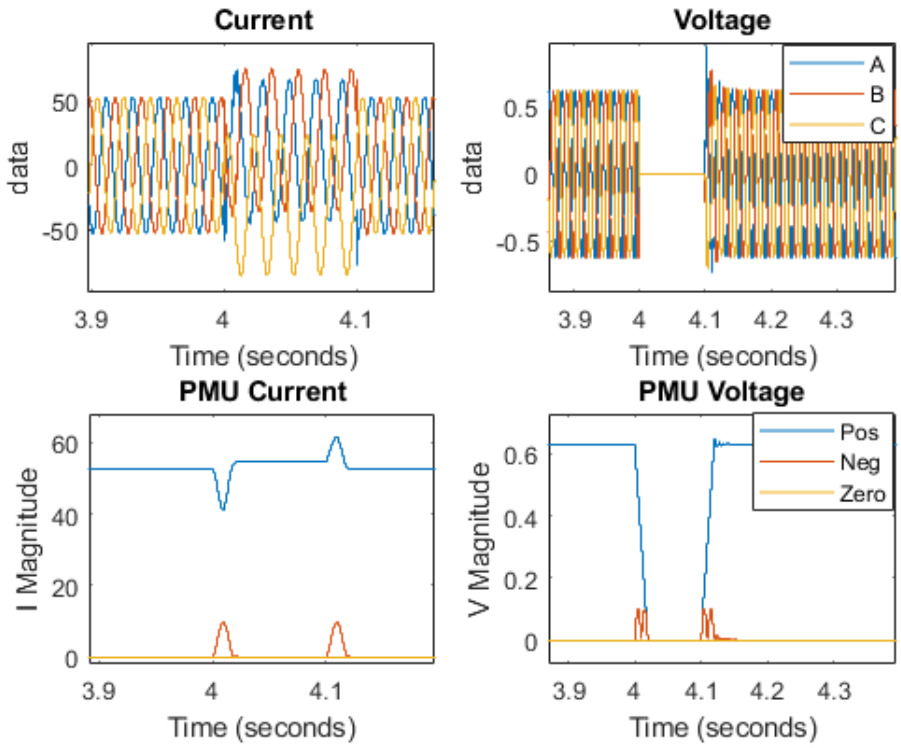

Figure 27. Three-phase fault in transmission model. Fault applied at t=0.7 and self-cleared at t=0.8 in bus2.

As shown in Figure 27, the voltages of all lines became zero during the fault, as expected. The current is also disturbed and increases in magnitude. Another point to highlight is that the phase difference between the three phases (A, B and C) remains constant during all simulation, as in the previous simulation. The positive-sequence voltage magnitude goes completely to zero, fact that differentiate the results from the previous simulation.

The positive-sequence current phasor magnitude suffers a small dip and then a peak when the fault occurs. In this case negative sequence current arise during the starting and clearance of the fault, being the zero-sequence current non-existing, as ground is not involved in this fault.

4.2 Faults in a HVDC link with PMUs installed

Finally, the simulation results of the CIGRÉ HVDC Benchmark model in both MATLAB-Simulink and PSCAD can be found in this chapter. First, the chapter focuses on SLG faults applied on the inverter side of the transformer under different fault resistance conditions. Later on, Two-phase, two-phase to ground and three-phase faults are also applied. An internal failure in a converter bridge has also been simulated disconnecting the bridge from the rest of the network using breakers. The signals are seen from the inverter side. That is because faults on the inverter side are more likely to be the cause of the commutation failure [16] and therefore these signals will be compared to the signals in the inverter side of the HVDC link. The model used has been presented in the previous section and it can be seen in figure 13.

4.2.1. SLG Fault applied at the inverter bus

It is highly interesting to study the effect of SLG faults near converters as this kind of fault is the most common causing commutation failures [16]. The behaviour of the AC current after these failures is still unknown and this chapter seeks to broad the understanding on this topic.

The models used have been shown in section 3.2.1.1 and 3.2.1.2. After the simulation, the results were sent to the PMU model, that it can also be seen in section 3.3, obtaining sequence phasor signals.

The first SLG fault is applied on the inverter side of the converter at t=0.7s and it's cleared at t=0.8 s. In this case the fault resistance is R=0.01 Ohms. Figure 28 shows the AC current and voltage signals as well as the output of the PMU for those measurements.

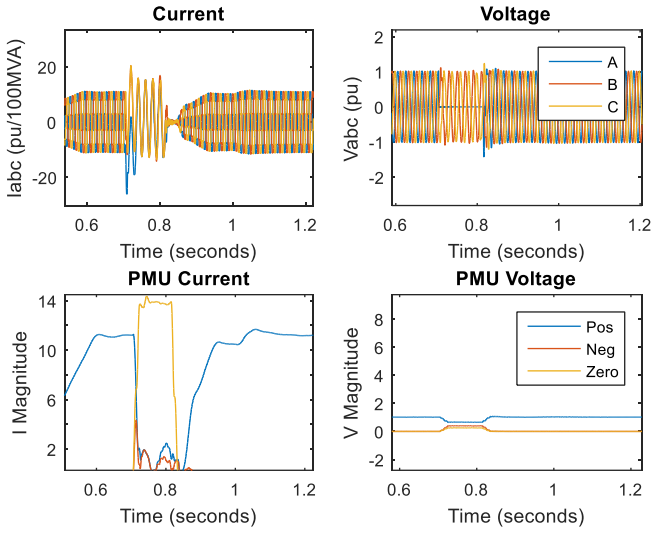

Figure 28. SLG fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s in MATLAB-Simulink. Fault resistance R=0.01 Ohms. AC current and voltage and PMU outputs.

In Figure 29, a detailed plot shows the AC current behaviour, in which all phases lose their phase difference during the faulted time. Positive sequence current goes to zero as zero sequence current has a peak. Regarding voltages, Positive sequence voltage has a dip of 1/3 of its initial value and both zero and negative sequences are not null during the faulted period.

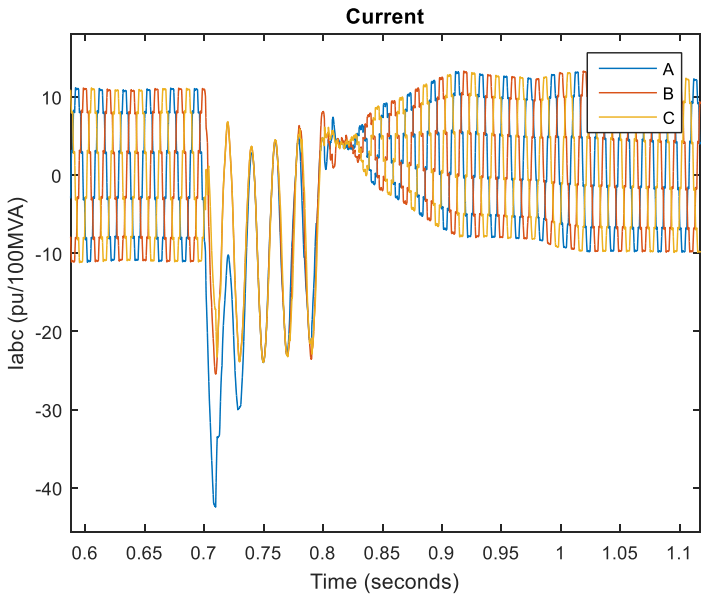

Figure 29. SLG fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s. Fault resistance R=0.01 Ohms. AC current detail.

In Figure 30, the AC current outputs and the PMU signals related to them of both MATLAB-Simulink and PSCAD are shown. When comparing the results, the same behaviour can be spotted in both graphs, being the MATLAB-Simulink result more clean, due to a more simplified model.

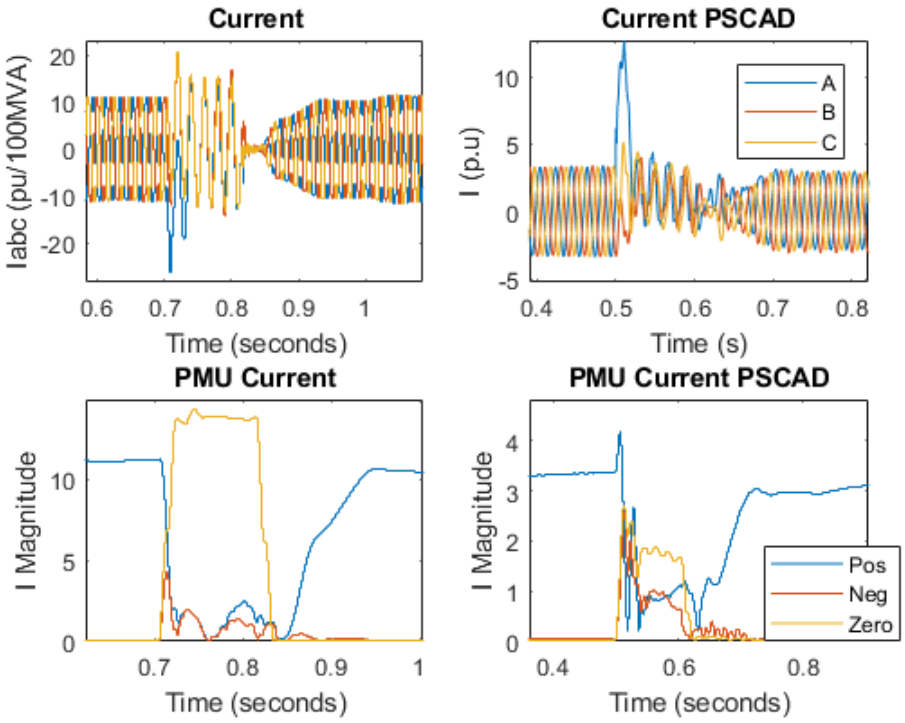

Figure 30. SLG fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s in MATLAB-Simulink and applied at t=0.5 s and cleared at t=0.6 s in PSCAD. Fault resistance R=0.01 Ohms. AC current and PMU output in MATLAB-Simulink (Left) and PSCAD (Right).

The following graphs represents the simulation results when the fault resistance is R=10 Ohms (See Figure 31). The comparison between the simulation in MATLAB-Simulink and PSCAD can be seen in Figure 32.

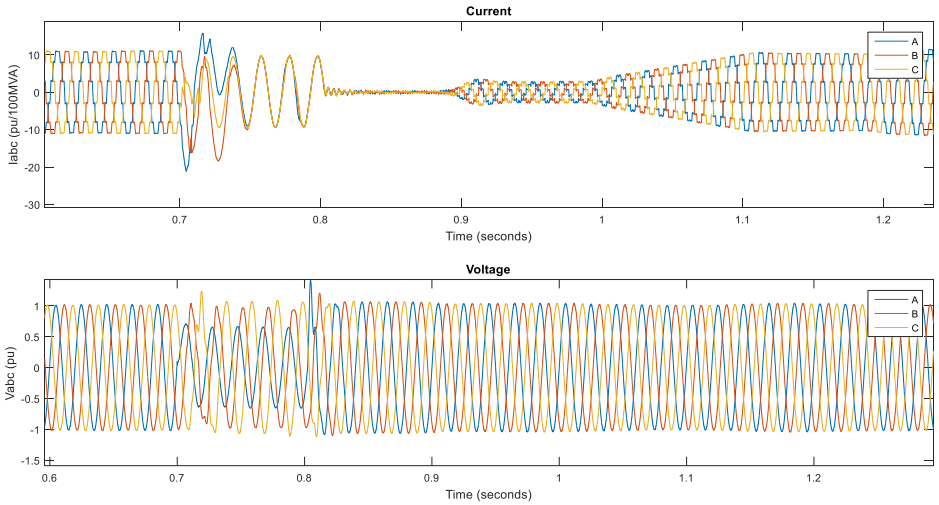

Figure 31. SLG fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s in MATLAB-Simulink. Fault resistance R=10 Ohms. AC current (above) and voltage (Below).

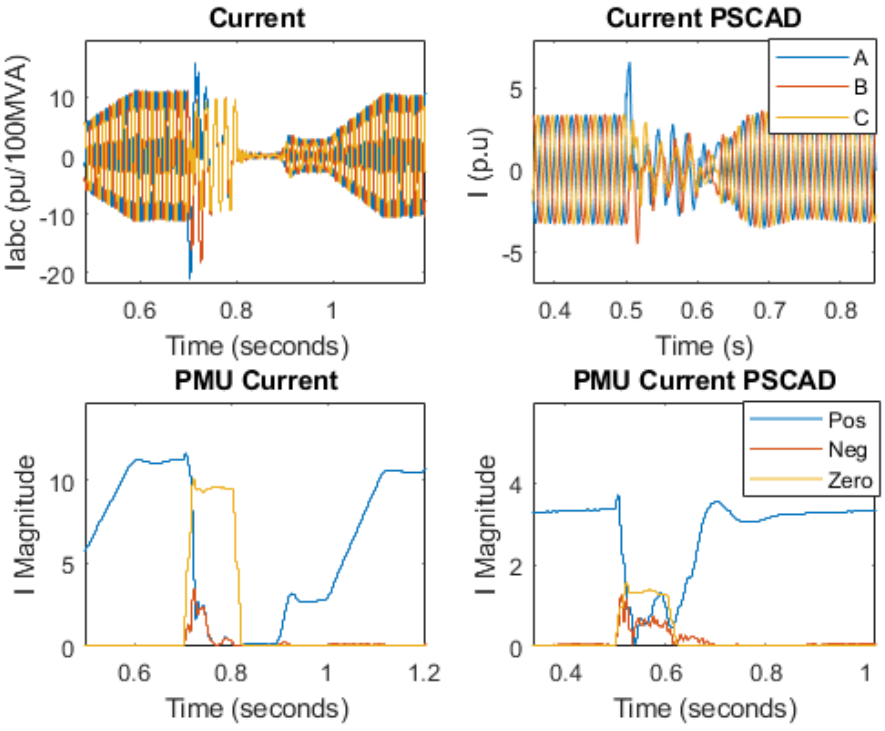

Figure 32. SLG fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s in MATLAB-Simulink and applied at t=0.5 s and cleared at t=0.6 s in PSCAD. Fault resistance R=10 Ohms. AC current and PMU output in MATLAB-Simulink (Left) and PSCAD (Right).

The behavior of the current signals is similar to the one found with fault resistance close to zero.

The following graphs in Figure 33 represent the simulation results when the fault resistance is R=50 Ohms.

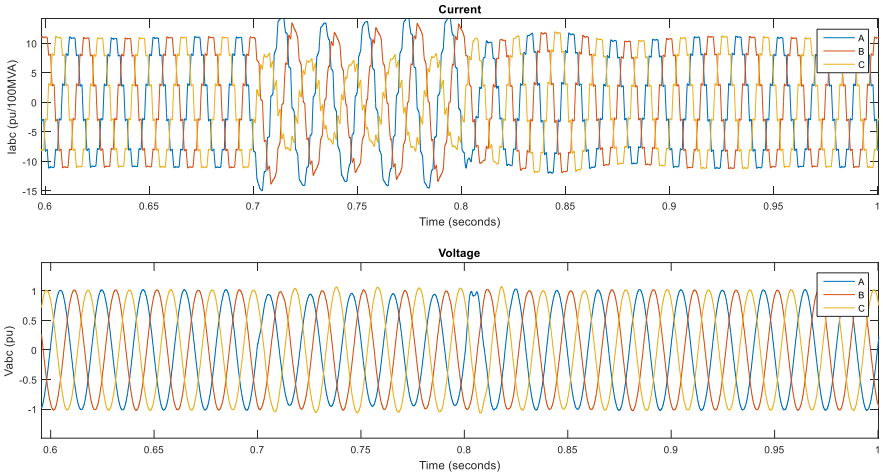

Figure 33. SLG fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s. Fault resistance R=50 Ohms. AC current and voltage.

In the same way as before, the comparison between the simulation in MATLAB-Simulink and PSCAD can be seen in Figure 34. In this case, the commutation failure only happens in the PSCAD simulation. As it can be seen the positive sequence does not go to zero in this case when the simulation is performed in MATLAB-Simulink.

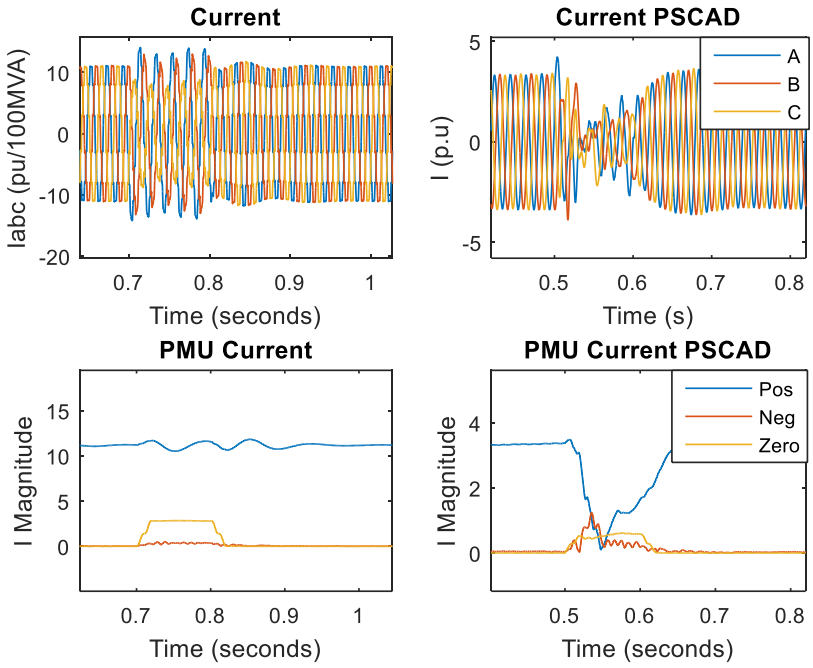

Figure 34. SLG fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s in MATLAB-Simulink and applied at t=0.5 s and cleared at t=0.6 s in PSCAD. Fault resistance R=50 Ohms. AC current and PMU output in MATLAB-Simulink (Left) and PSCAD (Right).

In the same way, the following graphs in Figure 35 represents the simulation results when the fault resistance is R=100 Ohms. In this case the dip in voltage caused by the AC fault is not enough for leading to commutation failures in any of the simulations.

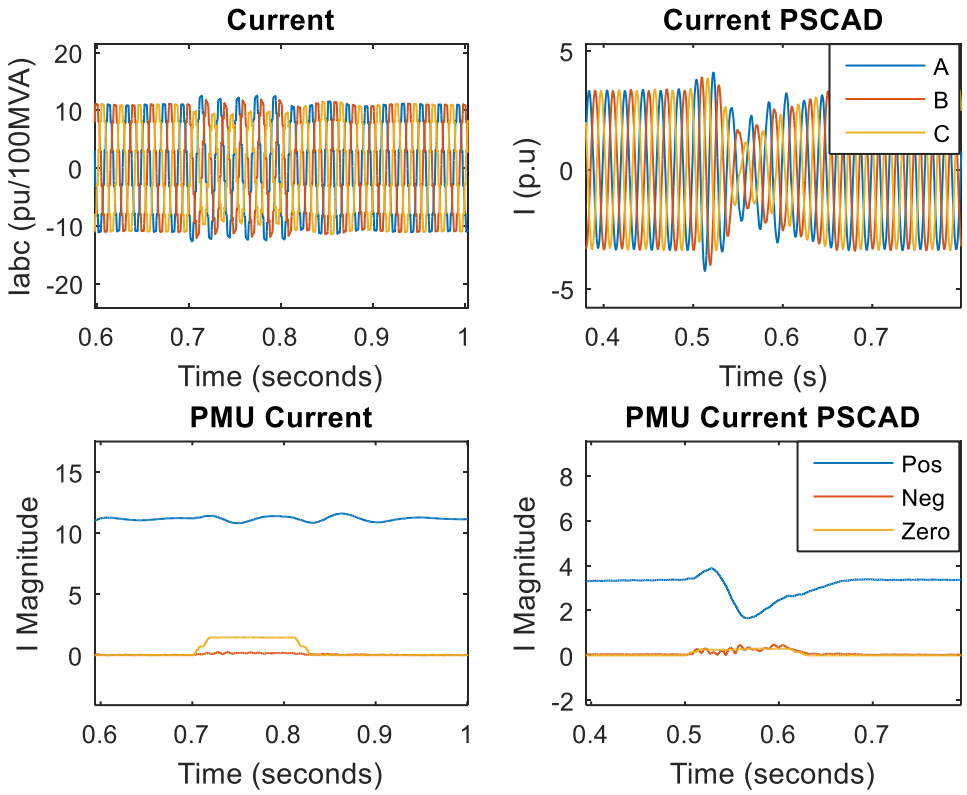

Figure 35. SLG fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s in MATLAB-Simulink and applied at t=0.5 s and cleared at t=0.6 s in PSCAD. Fault resistance R=100 Ohms. AC current and PMU output in MATLAB-Simulink (Left) and PSCAD (Right).

4.2.2 Two-phase to ground fault applied at the inverter bus

Even though SLG faults are the most interesting and common faults to study, Two-Phase to ground faults have also been studied. Only the case when the fault resistance is close to zero is shown, as it represents the most critical situation. The Figure 36 shows the AC signals of current and voltage in the simulation carried out in MATLAB-Simulink as well as the PMU output related with those signals. In this case, the behaviour found in the AC current is found as well, the voltage signals differ in a way that all three sequence voltages are equal during the faulted time.

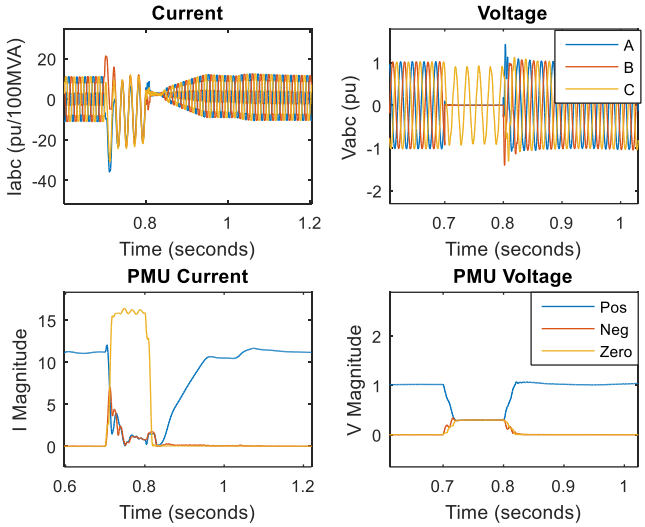

Figure 36. Two-Phase to ground fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s. Fault resistance R=0.01 Ohms. AC current and voltage and PMU outputs.

In Figure 37, The comparison between the output of the MATLAB-Simulink and PSCAD simulation is shown.

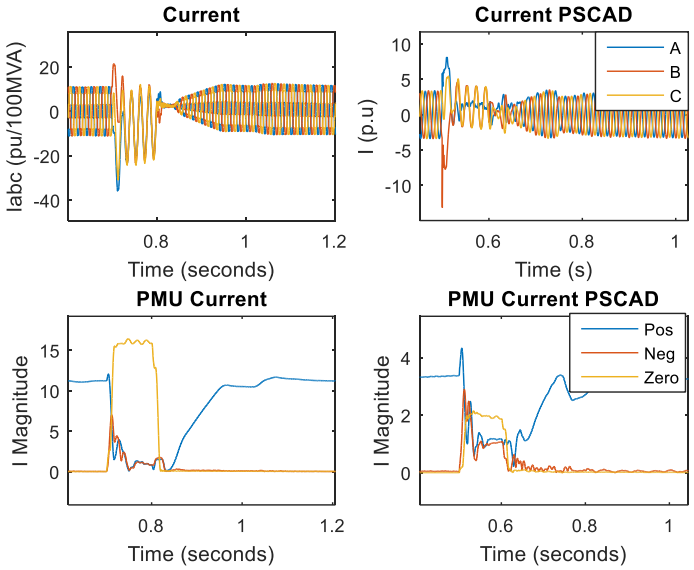

Figure 37. Two-Phase to ground fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s in MATLAB-Simulink and applied at t=0.5 s and cleared at t=0.6 s in PSCAD. Fault resistance R=100 Ohms. AC current and PMU output in MATLAB-Simulink (Left) and PSCAD (Right).

4.2.3 Two-phase fault applied at the inverter bus

In this case, as it can be seen in Figure 38, the zero sequence of both current and voltage is not involved because to the fault is between two phases and grounding is not included. Anyways, as commutation failures happen, the positive sequence current is blocked as in the previous simulations.

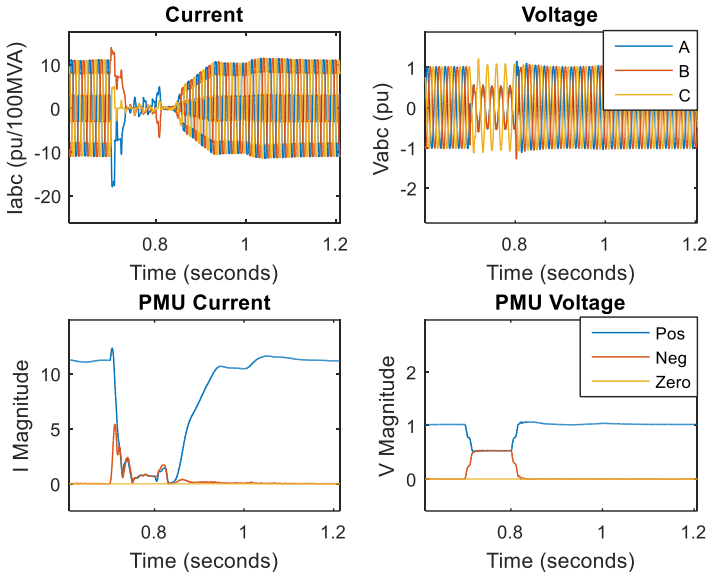

Figure 38. Two-Phase fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s. Fault resistance R=0.01 Ohms. AC current and voltage and PMU outputs.

In Figure 39, The comparison between the output of the MATLAB-Simulink and PSCAD simulation is shown. Both simulators represent the same behaviour, despite the small differences.

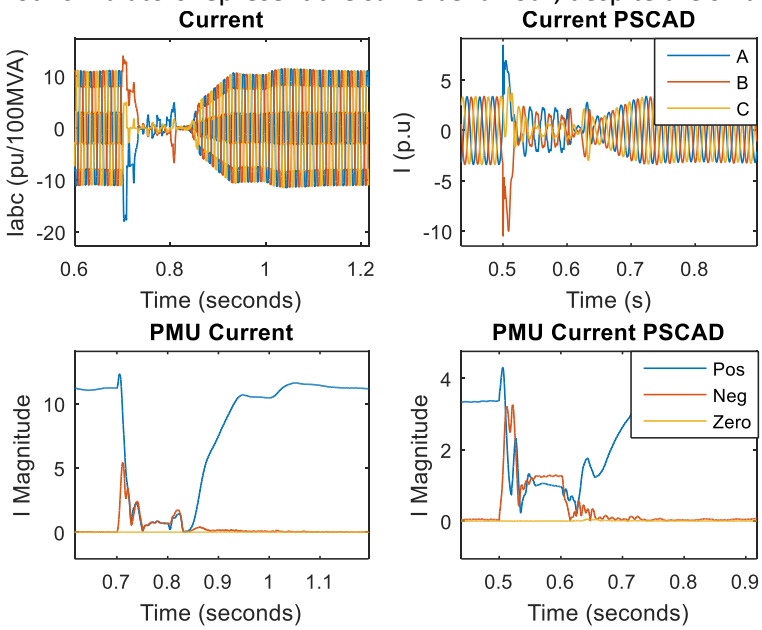

Figure 39. Two-phase fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s in MATLAB-Simulink and applied at t=0.5 s and cleared at t=0.6 s in PSCAD. Fault resistance R=100 Ohms. AC current and PMU output in MATLAB-Simulink (Left) and PSCAD (Right).

4.2.4 Three-phase fault applied at the inverter bus

The last case of AC fault studied is the Three-Phase fault. As shown in Figure 40, zero sequence is not involved but, as before, the positive sequence current is blocked due to the commutation failure. In Figure 41, The comparison between the output of the MATLAB-Simulink and PSCAD simulation is shown. Both simulators represent the same behaviour, despite the small differences.

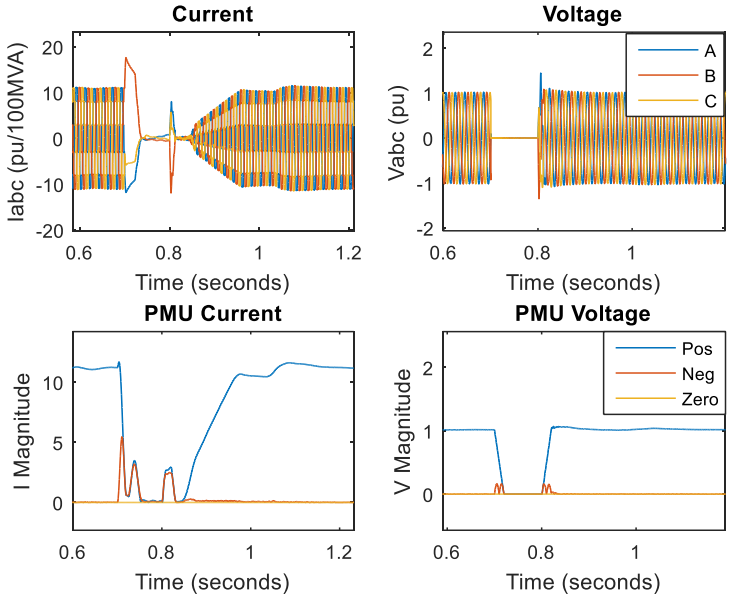

Figure 40. Three-Phase fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s. Fault resistance R=0.01 Ohms. AC current and voltage and PMU outputs.

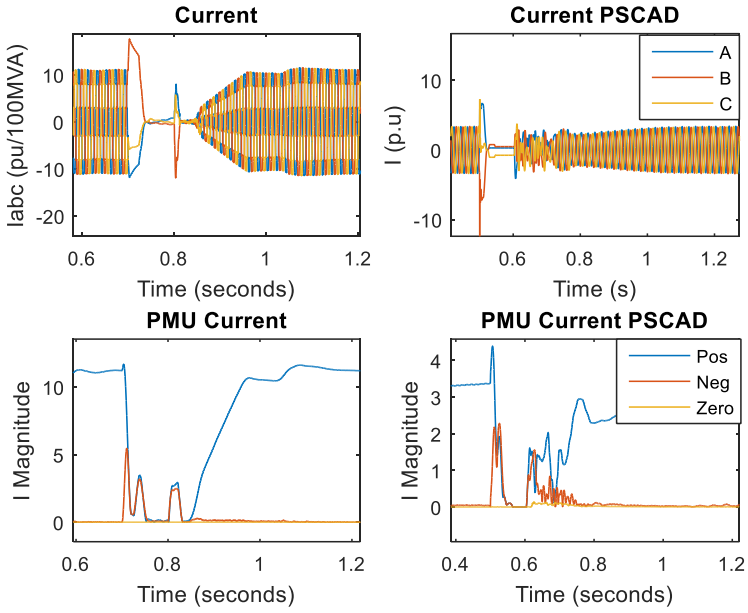

Figure 41. Three-Phase fault applied on the inverter side of the HVDC converter at t=0.7s and cleared at t=0.8 s in MATLAB-Simulink and applied at t=0.5 s and cleared at t=0.6 s in PSCAD. Fault resistance R=0.01 Ohms. AC current and PMU output in MATLAB-Simulink (Left) and PSCAD (Right).

4.2.5 Converter failure

A case in which a whole inverter bridge is turned off, simulating an internal malfunction of the converter, has also been simulated. In this case, only in MATLAB-Simulink. Figure 42 shows the AC current and voltage signals as well as PMU outputs related. This has been simulated disconnecting the bridge connections using circuit breakers and a timer.

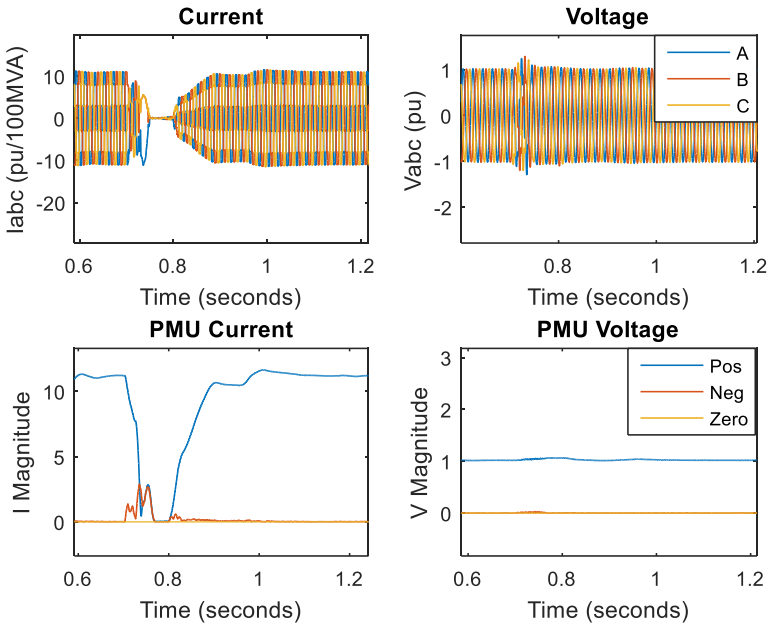

Figure 42. HVDC converter failure simulation at t=0.7s and cleared at t=0.8 s. AC current and voltage and PMU outputs.

The behaviour is similar to a Three-Phase fault regarding current but differs on the voltage signals, as in this case the positive sequence voltage still close to its reference value. The positive sequence current goes to zero as the current flow is blocked, while negative sequence exists during the trigger of the fault.

4.3 System equivalent during commutation failure

This section seeks to explain the reasons behind the behaviour found in the previous section. During commutation failure, the converter is modelled as an open circuit. This is due to the fact that when a commutation fault happens, the power and current flow through the converter is blocked, and therefore the positive and negative sequence are blocked as well. A schematic model of how the system can be represented during a commutation failure is proposed in Figure 43.

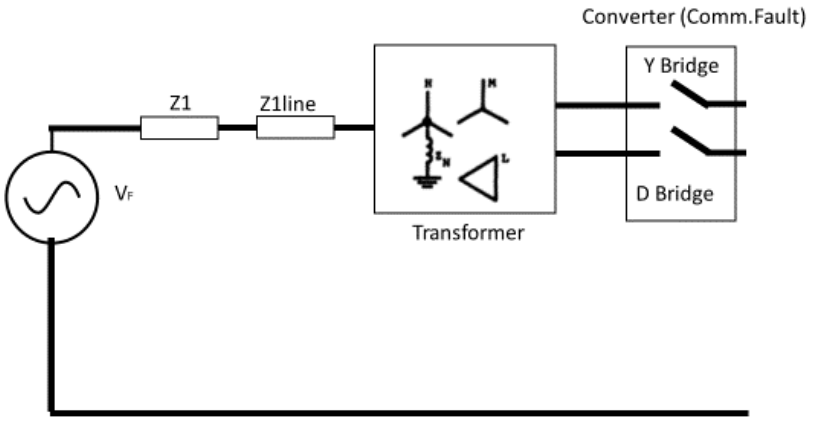

Figure 43. Schematic single-line diagram model of the inverter side when commutation failures happen

Below, the sequence networks and their interconnections when SLG, two-phase, two-phase to ground and three-phase faults are applied are shown in a schematic way. In the diagrams the fault resistance has been considered zero. In all cases, the PMU measures the current into the H terminal of the transformer.

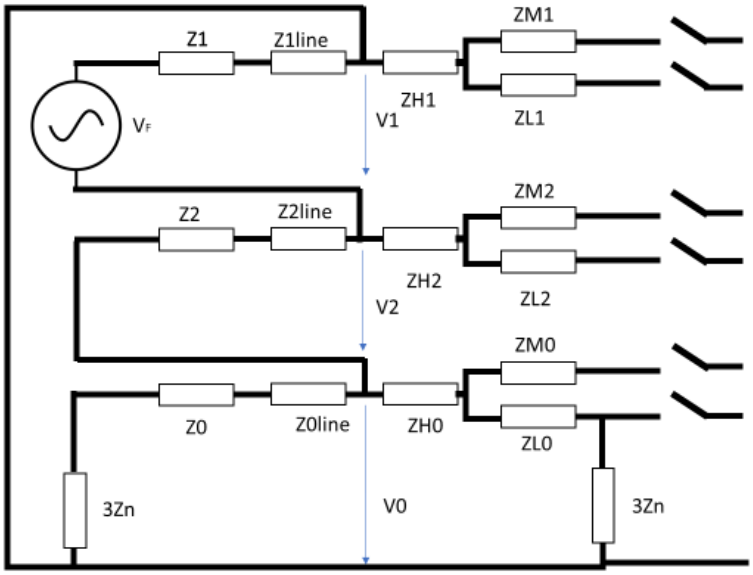

Figure 44. SLG fault at the inverter side during commutation failure. Sequence network with zero fault resistance.

Figure 44 shows how the sequence networks are connected when an SLG fault occurs at the grounded-wye side of the transformer. This represents a SLG fault at the inverter side of the converter. In this case, all three networks connected in series at the fault location. Therefore, as it can be seen, zero sequence currents flow through the circuit thanks to the grounding of the Wye winding of the transformer (The one located on the AC side). The characteristics correspond with the ones found after simulating the system, as shown in Table 1.

Figure 45 shows the system schema when a two-`phase fault is applied at the grounded-wye side of the transformer. In this case, positive and negative sequence connected in parallel at the H terminal of the transformer while zero sequence is isolated and therefore non-existing. In the same way, these characteristics are the same as found after the simulations in the subsection 4.2.

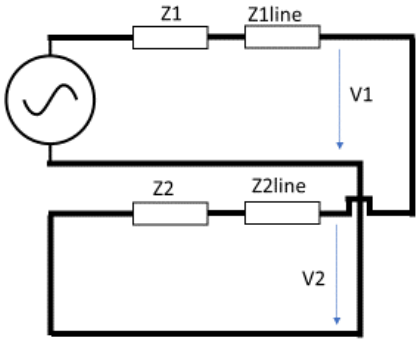

Figure 45. Two-phase fault at the inverter side during commutation failure. Sequence network with zero fault resistance.

In the same way, Figure 46 represents the system when a two-phase to ground fault is applied at the grounded-wye side of the transformer. As in previous examples, this model is only valid during commutation failure. In this case, the three networks are connected in parallel at the fault location. Which is the H terminal of the transformer. For that reason, all sequence voltages are equal and the zero-sequence current exists.

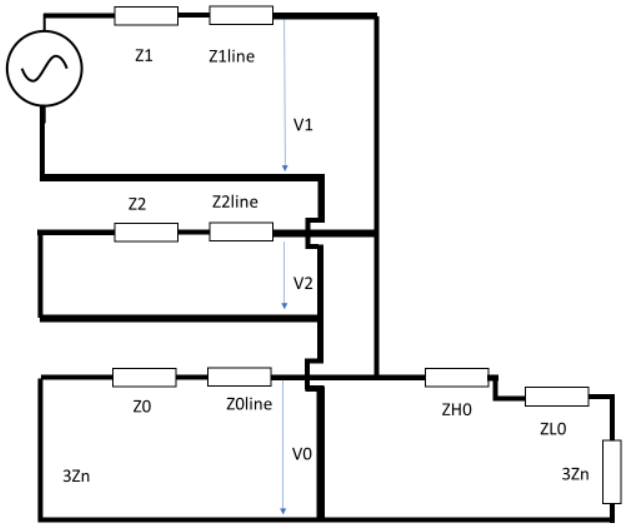

Figure 46. Two-phase to ground fault at the inverter side during commutation failure. Sequence network with zero fault resistance.

The last case can be seen in Figure 47. It shows the system under a three-phase fault located at the grounded-wye side of the transformer. In this case, the three networks disconnected, therefore only positive sequence may exist. As is the only one with a voltage source.

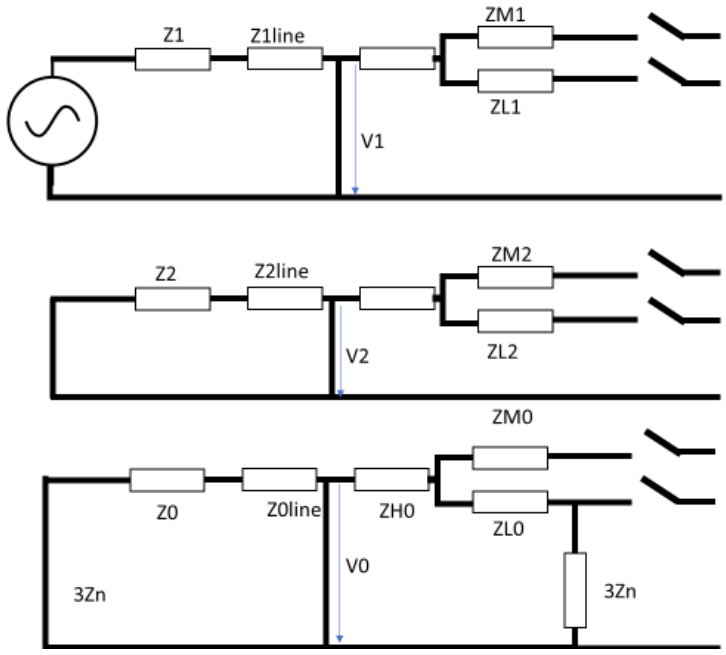

Figure 47. Three-Phase fault at the inverter side during commutation failure. Sequence network with zero fault resistance.

As explained in the background, the configuration of transformers used in HVDC link plays a key role in the behaviour that the AC current has when a commutation fault happens in the converter. The sequence diagrams above suggest that, during CF, the inverter can be replaced by an open-circuit, being the HVDC-link represented only by the transformer alone.

Therefore, a model that behaves as the system while commutation failures happen has been simulated when a SLG fault is applied at the grounded-wye side of the transformer. The model can be seen in Figure 48. At the same instant (t=0.7) the fault is applied as well as the breakers connected at the delta side of the transformer open. This is a way of simulating the blockage of the valves when commutation failures happen.

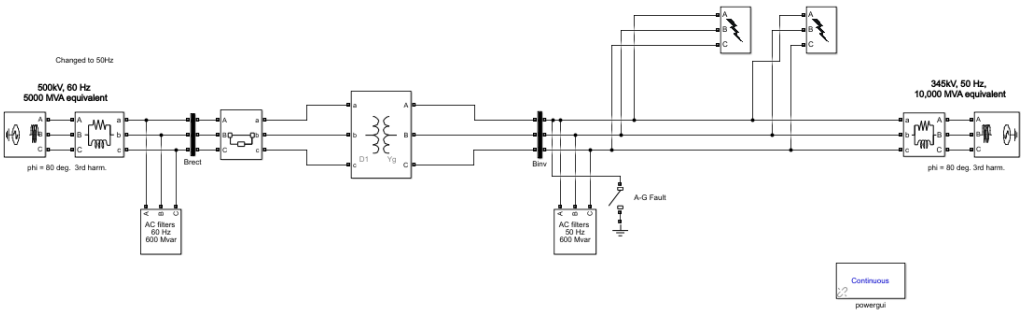

Figure 48. System equivalent during commutation failure modelled in MATLAB-Simulink

In figure 49 it can be seen the AC current and the output of a PMU installed in the grounded-wye side. As positive and negative sequences are blocked, only zero-sequence current exists during the fault. In the AC side this can be seen as a loss of phase difference between the three current phases (A, B, C). This behavior corresponds with the simulation results when the HVDC converter is installed, and their reasons where unknown until now. The zero-sequence network associated with the grounded-wye delta transformer is the reason of this behavior.

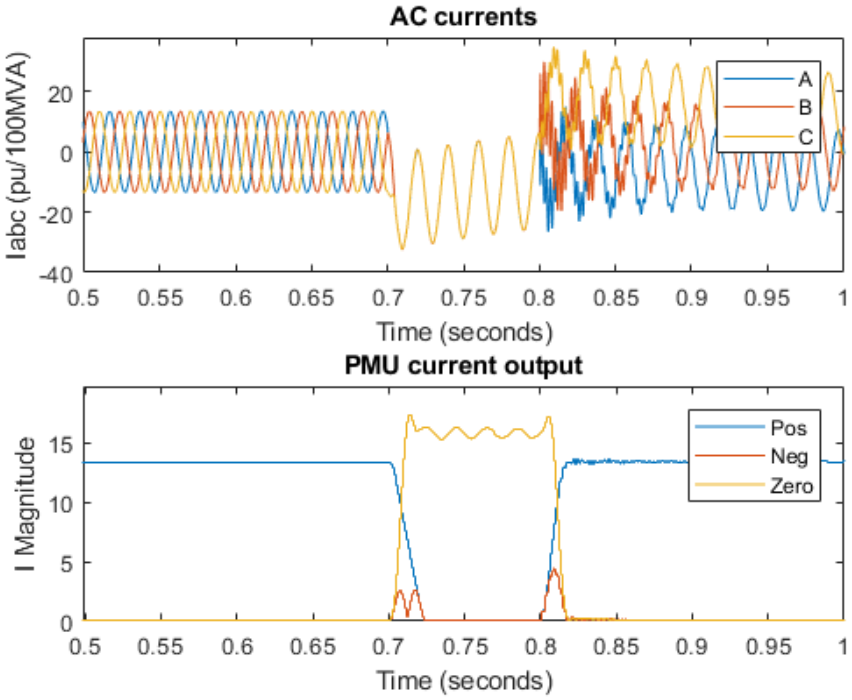

Figure 49. SLG fault simulated in the delta transformer model. Fault applied on the inverter side at t=0.7 s and self-cleared at t=0.8 in MATLAB-Simulink

4.4 Summary HVDC-link simulations

A summary of the characteristics found in the different faults after the simulations can be seen in Table 1, where the qualitative behaviour of sequence currents and voltages is organized. Negative sequence current and voltages are not explicitly included in the table, due to main importance of positive and zero sequences.

Table 1. Summary of characteristics in PMU for the different faults simulated.

FAULT TYPE:	**SLG**	**2 PHASE**	**2 PHASE TO GROUND**	**3 PHASE**	**BRIDGE FAILURE**
Positive-sequence Current	Zero	Zero	Zero	Zero	Zero
Zero-sequence Current	Peak	Zero	Peak	Zero	Zero
Positive-sequence Voltage	Dip	Dip. Equal to negative-sequence	Dip. Equal to Negative and zero sequence	Zero	No changes
Zero-sequence Voltage	Peak	Zero	Dip. Equal to Negative and positive sequence	Zero	Zero

When comparing the table summary with section 4.3, all characteristics are coherent and therefore the behavior can be explained using the simplified diagrams in the previous chapter. When comparing with section 4.1, when the inverter is not installed yet, the signals differs both in current and voltage, which makes simpler to differentiate from a system with HVDC. These traits, can be use in the future in order to build a fault detection and location algorithm, that will be able to distinguish between different AC faults causing commutation failures. The main characteristic that can be used for distinguish between commutation failures, and AC faults is the magnitude of the positive sequence current phasor, that become zero when the current through the converter is blocked due to a commutation failure.

5. Commutation failure detection and location in Nordic32 network

This section includes the simulation results obtained in DigSilent-PowerFactory. First of all, the HVDC Benchmark model available in the library of the software [35] is simulated in order to understand the differences in behavior with the previous results obtained.

Secondly, using the modified Nordic32 model (based on [32]), a SLG is simulated in the Buses 4042 and 4062, and a Three-Phase fault in 4042, where later on an HVDC converter will be connected. More specifically, the inverter of the converter will be connected to these buses while the rectifier side is connected to an infinite bus representing a different AC system. After that, the aim is to understand how the fault spread along the network using the measurement of five PMUs installed in nodes 4045 (PMU 1), 4051 (PMU 2), 4062 (PMU 3), 4063 (PMU 4) and 4042 (PMU 5), as shown in Figure 20.

It must be said that this section is not conclusive, but open new path of research. Due to time limitations, the results shouldn't be considered as definitive. More work is needed in order to understand how commutation failures spread in a bigger network. Only frequency signals are provided in this section, the rest of signals can be found in the Annex.

5.1 HVDC simulation in Digsilent-PowerFactory

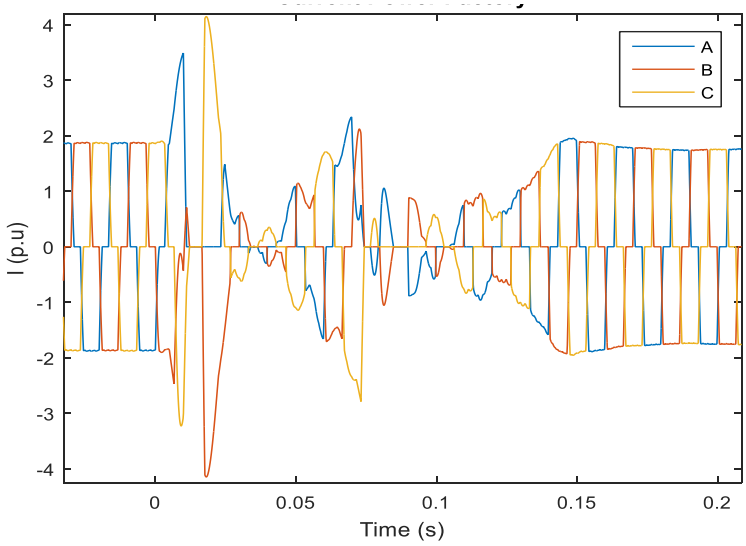

Figure 50. AC currents in the HVDC benchmark model simulation in DigSilent-PowerFactory. SLG fault applied on the inverter side of the transformer at t=0s and cleared (Self-extinguish) at t=0.1s.

A SLG fault has been applied on the inverter side of the transformer at t=0s and cleared at t=0.1s. When the voltage dip in the AC bus is sufficiently deep, commutation failure occurs. But the behavior found in the AC current during previous simulations is not found, as it can be seen in Figure 50. As commented in section 3.2, that is because the transformer model used in the HVDC Benchmark model available does not consider the internal configuration of the windings, but only if the AC signals are displaced in phase. Therefore, the software does not consider the different sequence network available for each type of transformer winding configuration. The simulation was done applying a SLG fault in order to compare the behavior found in the zero-sequence current in previous simulations.

5.2 Simulation of faults in the Nordic32 network using PowerFactory

In this section, the simulations results obtained in DigSilent-PowerFactory when a SLG fault and a Three-Phase are applied on the BUS 4063 and BUS 4042 are shown. In the Nordic32 model used there are PMU installed in the buses specified previously, but there is no HVDC converter installed yet. The PMUs provide frequency, positive sequence voltage and current and zero sequence voltage and current magnitude. As methods mentioned in Section 2.4, frequency signals are used for location of faults, while characteristics of the shape in all other magnitudes can be used for determining which kind of fault happened.

It must be pointed out, that after the SLG simulations, another behavior has been found, different from the derived from the commutations failures in previous sections. The 100 Hz component in the frequency signals during fault as well as the 50 Hz component in the voltage and current is due the fact that the unbalance generated by the SLG fault leads to a negative sequence current on the nearby generator that is translated into a negative-sequence braking torque that is seen as a pulsating torque with twice the synchronous frequency of the system (50 Hz). This behavior is explained with detail in [36]. When applying Three-phase faults, the negative torque does not exist as the fault is balanced and therefore, the 100Hz component in frequency disappears. Please notice that the 100 Hz behavior is related to electro-mechanical dynamics, and therefore cannot be reproduced with the CIGRÉ benchmark model previously simulated, as frequency was fixed.

5.2.1 SLG fault on bus 4063- No converter installed

First, the SLG fault is applied on Bus 4063, where PMU number 4 is installed. The fault happens at t=0.5 s and is self-cleared at t=0.6 s. Due to the unbalance nature of the SLG fault, zero-sequence current and voltages arise during fault (See Annex B).

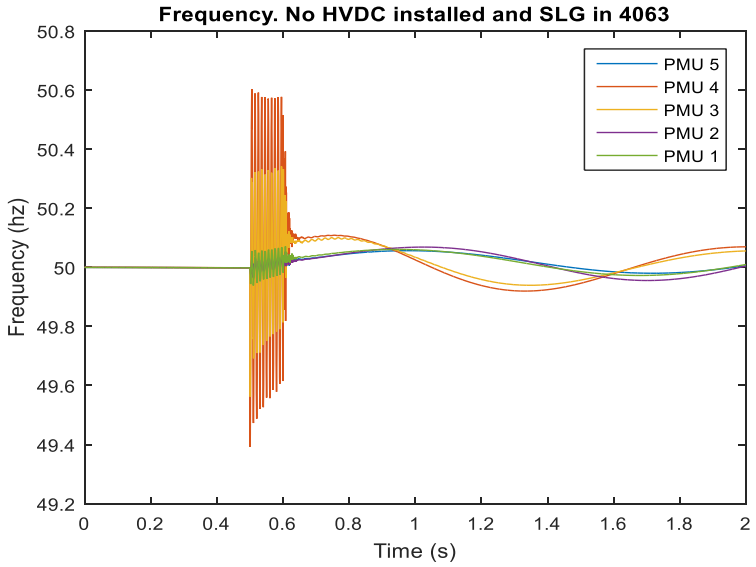

Figure 51. SLG fault on Bus4063 at t=0.5 s and self-cleared at t=0.6 s. No HVDC installed. Frequency signal

As it can be seen in Figure 51, the magnitude of the frequency disturbance is bigger the closer to the converter the measurement is done. In figure 52, it can be seen with detail the 100 Hz component of the signal during fault.

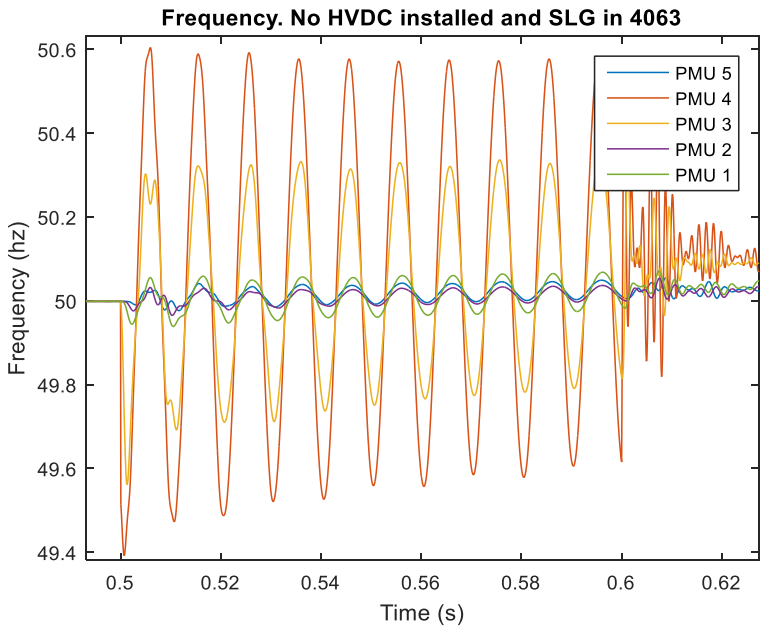

Figure 52.SLG fault on Bus4063 at t=0.5 s and self-cleared at t=0.6 s. No HVDC installed. Frequency signal detail (100 Hz component)

Some delays, apparently originated according to the principles of the electromechanical wave propagation can be seen in Figure 53. The frequency disturbance is felt on this order: PMU 4, PMU 3, PMU 1, PMU 2 and PMU 5. Which is coherent with the spatial layout of the network.

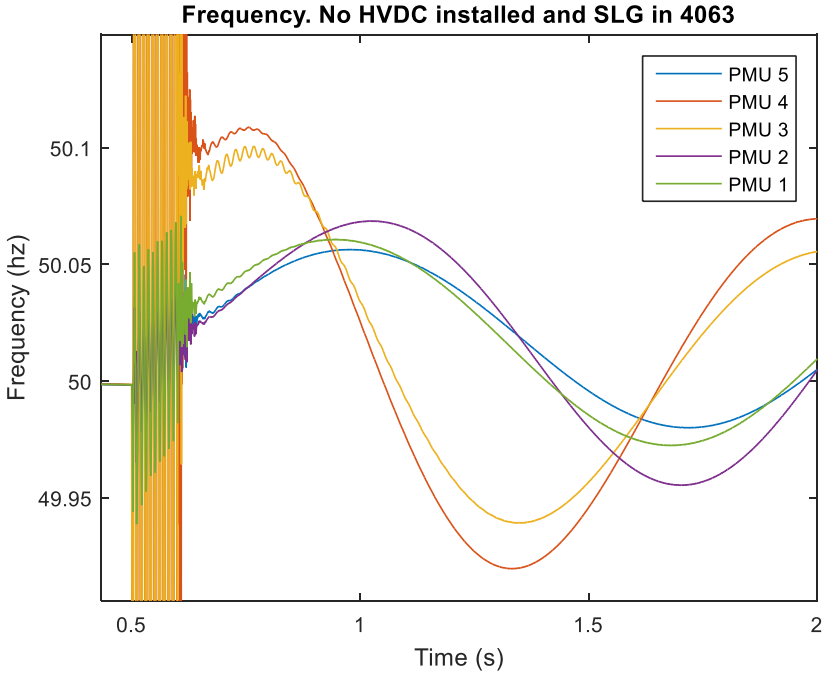

Figure 53. SLG fault on Bus4063 at t=0.5 s and self-cleared at t=0.6 s. No HVDC installed. Frequency signal detail (delay)

5.2.2 SLG fault on bus 4042- No converter installed

In this part, the SLG fault is applied on Bus 4042 instead, where PMU number 5 is installed. Same as before, the fault is triggered at t=0.5 s and self-cleared at t=0.6 s. The frequency signals provided by the PMU can be seen in Figure 54. In figure 55, it can be seen with detail the 100 Hz component of the signal during fault.

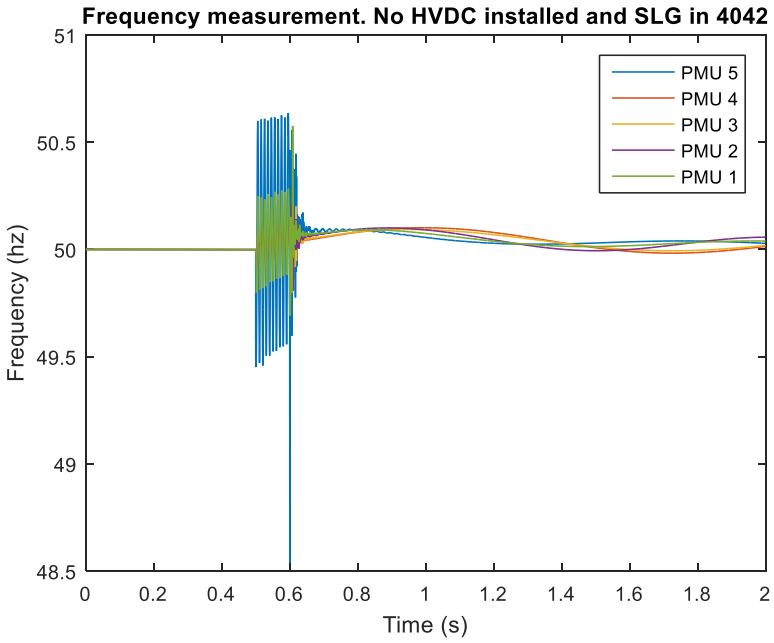

Figure 54. SLG fault on Bus 4042 at t=0.5 s and cleared at t=0.6 s. No HVDC installed. Frequency signal.

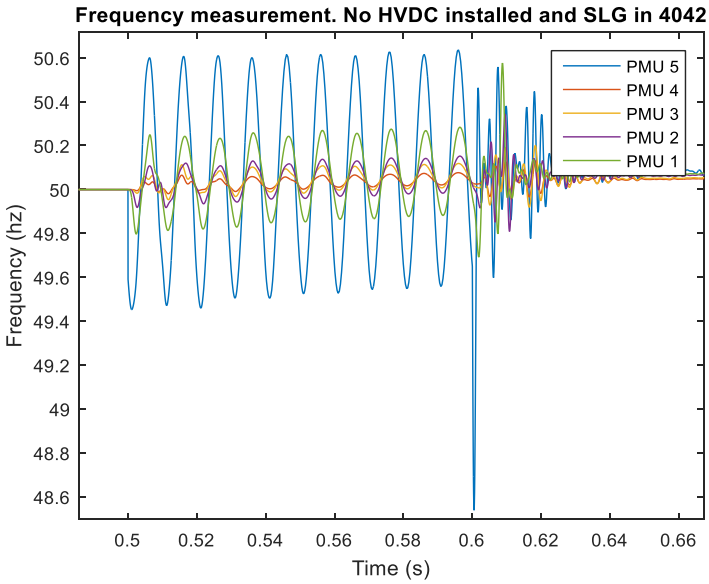

Figure 55. SLG fault on Bus 4042 at t=0.5 s and cleared at t=0.6 s. No HVDC installed. Frequency signal detail (100 Hz component)

Some delays, similar to the ones found in the previous simulation can be seen in Figure 56. In this case, the perturbation is felt first in PMU 5, where the fault is located and later on PMU 1, PMU 2. PMU 3 and PMU 4 respectively.

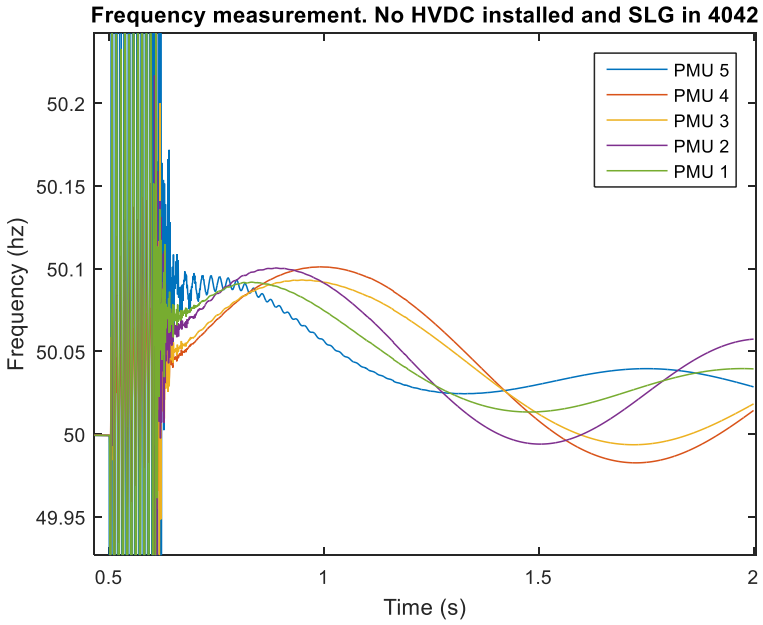

Figure 56. SLG fault on Bus 4042 at t=0.5 s and cleared at t=0.6 s. No HVDC installed. Frequency signal detail (Delay)

5.2.3 Three-Phase fault on bus 4042- No converter installed

In this subsection, a Three-Phase fault is applied at bus 4042, with no HVDC installed. In this case, as it can be seen in Figure 57, the signal does not have the 100 Hz component found before. Zero-sequence voltage and current do not exist in this case, as fault is balanced and ground is not involved

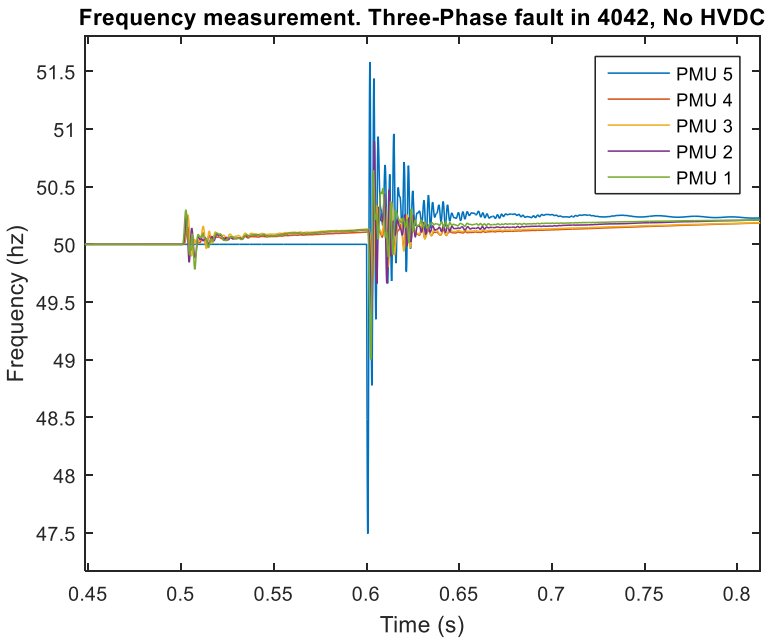

Figure 57. Three-Phase fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. No HVDC installed. Frequency signals

In the same way as in previous simulations, delays can be seen in Figure 58. It is less clear in this picture, but the order is the same as previously: PMU 5, PMU 1, PMU 2, PMU 3 and PMU 4. The order can be found looking at the peak point o the point where the profile crosses certain level.

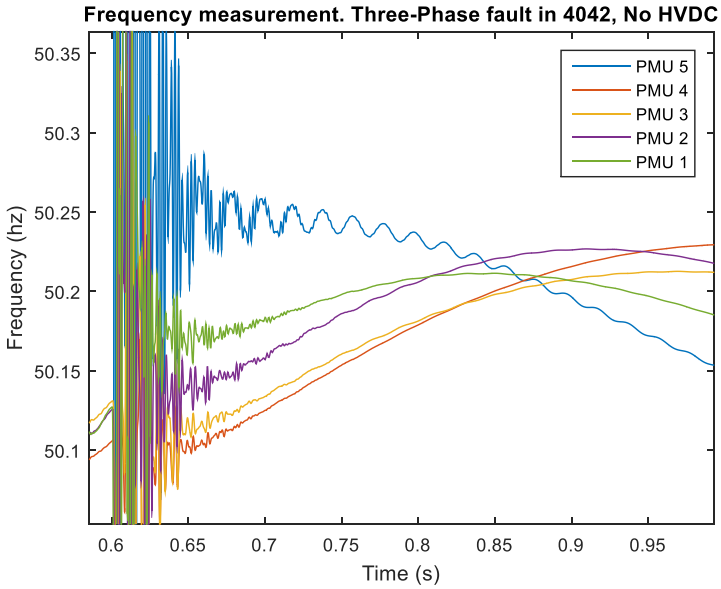

Figure 58. Three-Phase fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. No HVDC installed. Frequency signal detail

5.3 Simulation of commutation failures caused by SLG and Three-phase faults in externally connected HVDC converters along the Nordic32 network using Digsilent-PowerFactory

This section includes the simulation results obtained in Digsilent-PowerFactory when externally connected HVDC converters along the Nordic32 network suffer commutation failures. More specifically, the HVDC-link has one converter installed in an external node of the Nordic32 while the other converter is installed in a different AC system, in this case modeled as an infinite bus. When installing an HVDC in the Nordic32 network model, it is necessary to remove a few nodes in order to fulfill the maximum node requirement of the software. The nodes removed has been Buses 1011,1012,1013 and 1014, as are strongly connected and can be considered as pretty isolated dynamically from the rest. A different choice can be argued.

The commutation faults are caused by a SLG and Three-Phase faults applied (in different simulations) on the inverter bus where the converter is connected. The fault is applied at t=0.5 s and self-cleared at t=0.6 s in each case. The Fault resistance has been considered zero. As it can be seen in figure 59, the power through the converter became zero during the fault and a short time after its clearance.

As in the previous subsection, the focusing is on the frequency signals and the rest of measurements can be found in the Annex B.

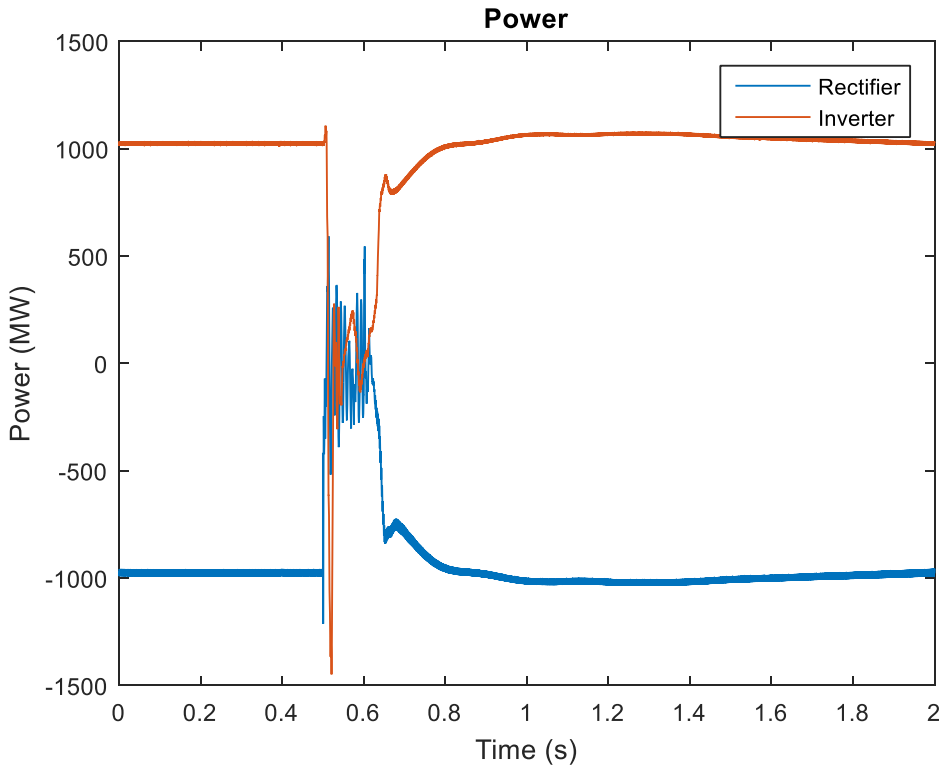

Figure 59. Power profile through the converter when commutation failure. SLG fault applied on the inverter side at t=0.5 s and self-cleared at t=0.6 s

5.3.1 HVDC externally installed at bus 4063- SLG fault inverter

First, as in the previous subsection simulation, the SLG fault is applied on Bus 4063. In this case, the inverter side of an HVDC converter is also connected to cited bus. The frequency signals can be seen in Figure 60. The signals still containing the 100 Hz component, but also become noisy (alternating at high frequency) when close to the converter, as in this case PMU 4 and PMU 3, as it can be seen in Figure 61. The recovery part (right after t=0.6 s) is a bit different regarding shape when comparing with the simulation without the HVDC. This fact can be used for detecting that a commutation failure has happened but need to be studied deeper in order to assure that always happen and that follows a pattern. For that is suggested to perform similar simulations but with the fault located in much more different points.

These signals would be better for analysis after a filter treatment. Due to time limitations this still open to further investigations. As the behavior of the frequency measurement nearby the converter station is not accurate.

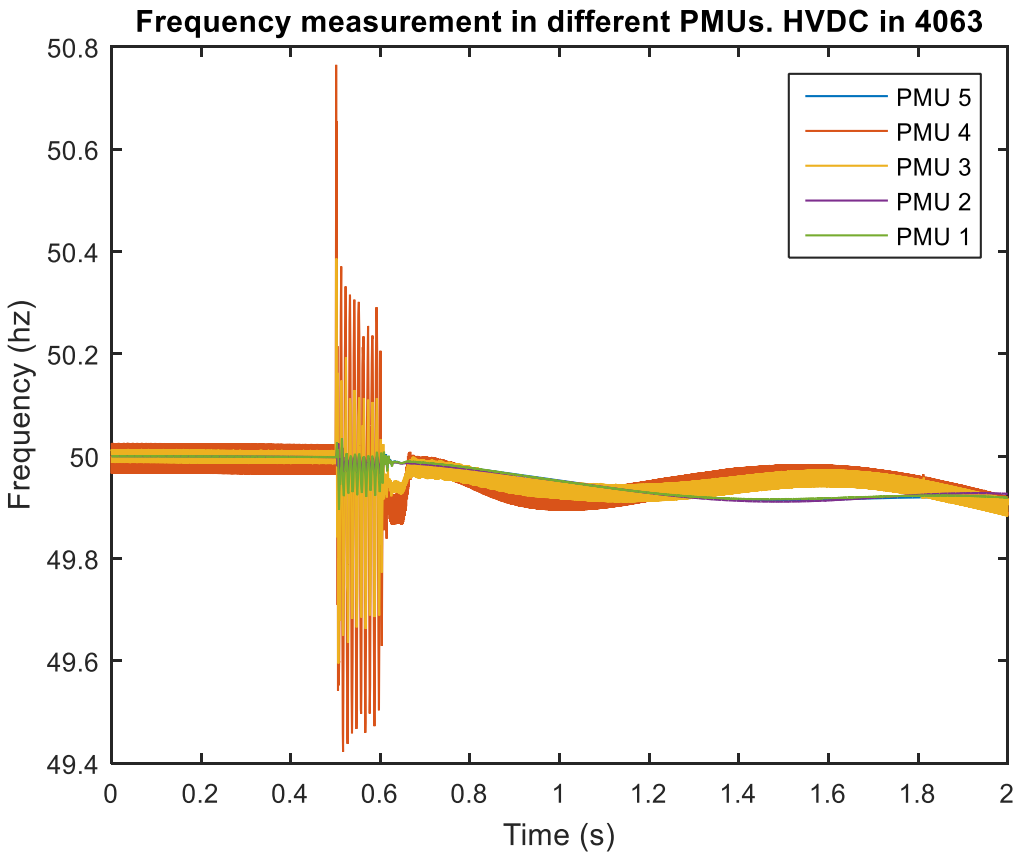

Figure 60. SLG fault on Bus 4063 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Frequency signals

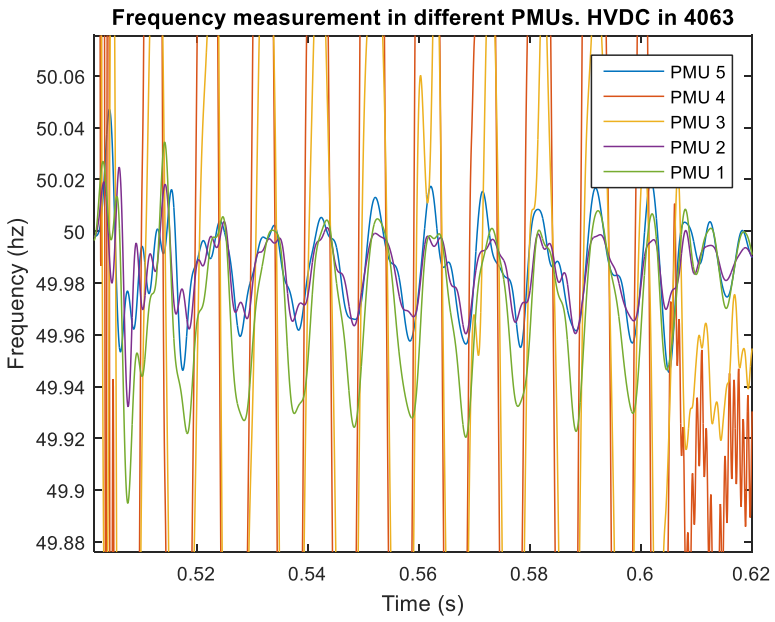

Figure 61. SLG fault on Bus 4063 at t=0.5 s and cleared at t=0.6 s. HVDC installed on Bus 4063. Frequency signals detail

The delays still existing, but there are less clear to see as the frequency output from PMU close to the fault appear noisy. In any case the sequence of the disturbance is in this case: PMU 4, PMU 3, PMU 1, PMU 2 and PMU 5. As in the simulations without the HVDC. But it is clearly much more difficult and unsure to determine (See Figure 62).

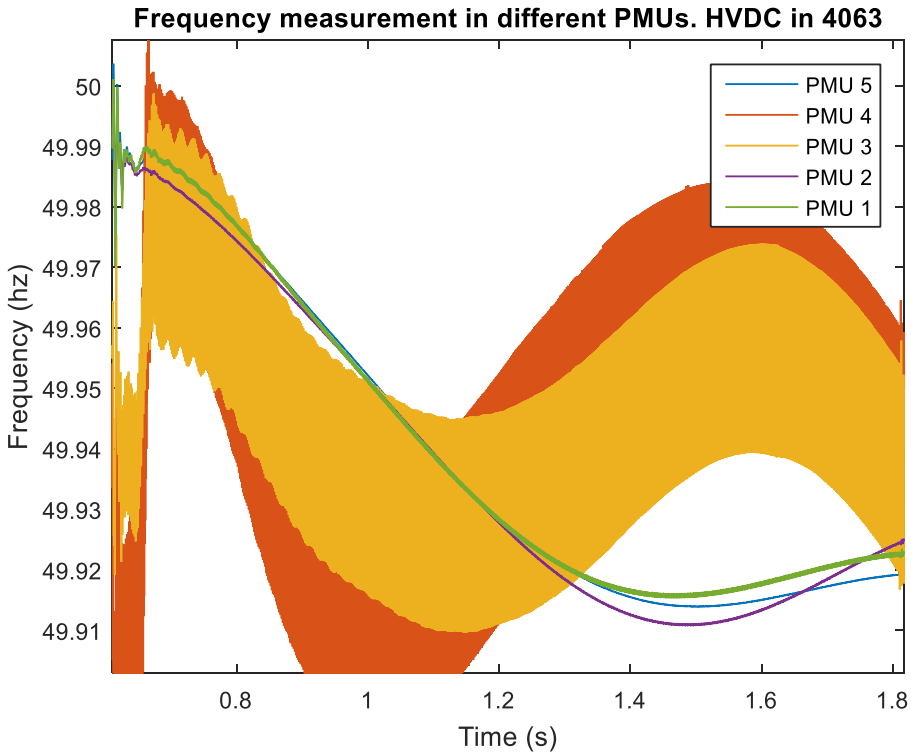

Figure 62. SLG fault on Bus 4063 at t=0.5 s and cleared at t=0.6 s. HVDC installed on Bus 4063. Frequency signals detail

5.3.2 HVDC externally installed at bus 4042- SLG fault inverter

In this case, the SLG fault is applied on Bus 4042. The frequency signals can be seen in Figure 63. The signals still containing the 100 Hz component, but also become noisy (alternating at high frequency) when close to the converter, as in PMU 5. This can be seen in detail in Figure 64. The recovery part (right after t=0.6 s) is a bit different regarding shape when comparing with the simulation without the HVDC as well as in the first case. Figure 65 shows the delays in detail. In this case, the disturbance is first felt at PMU 5 and later spreads to PMU 1, PMU 2, PMU 3 and PMU4, in that order.

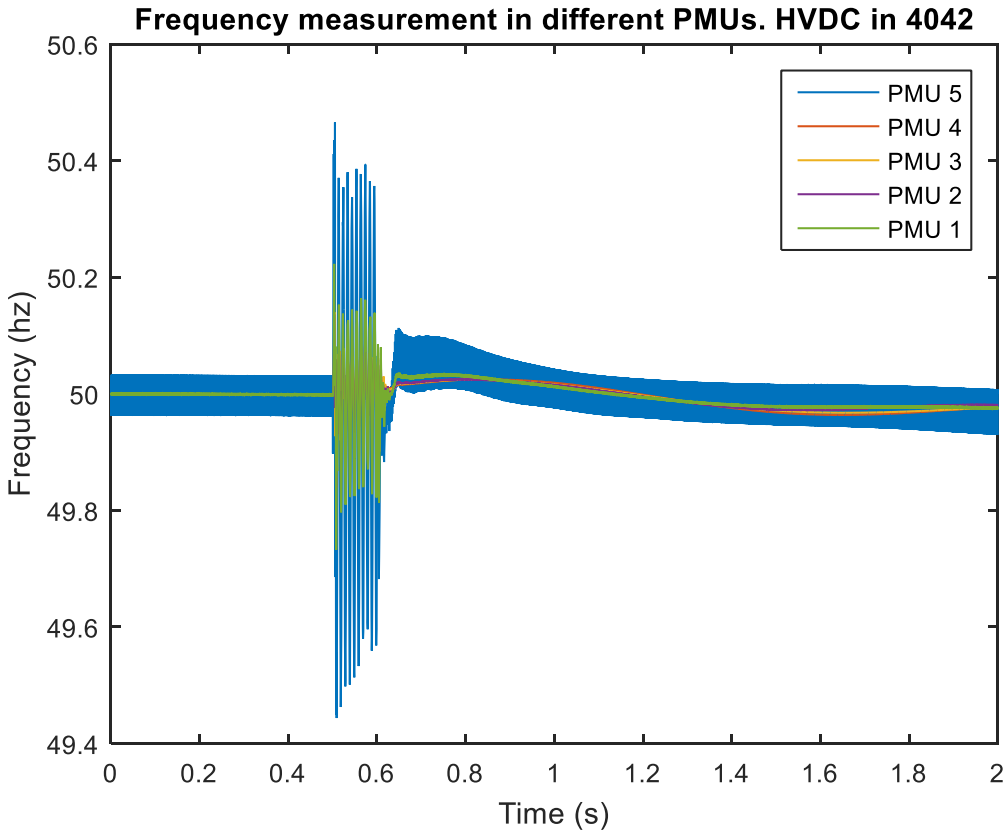

Figure 63. SLG fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Frequency signals

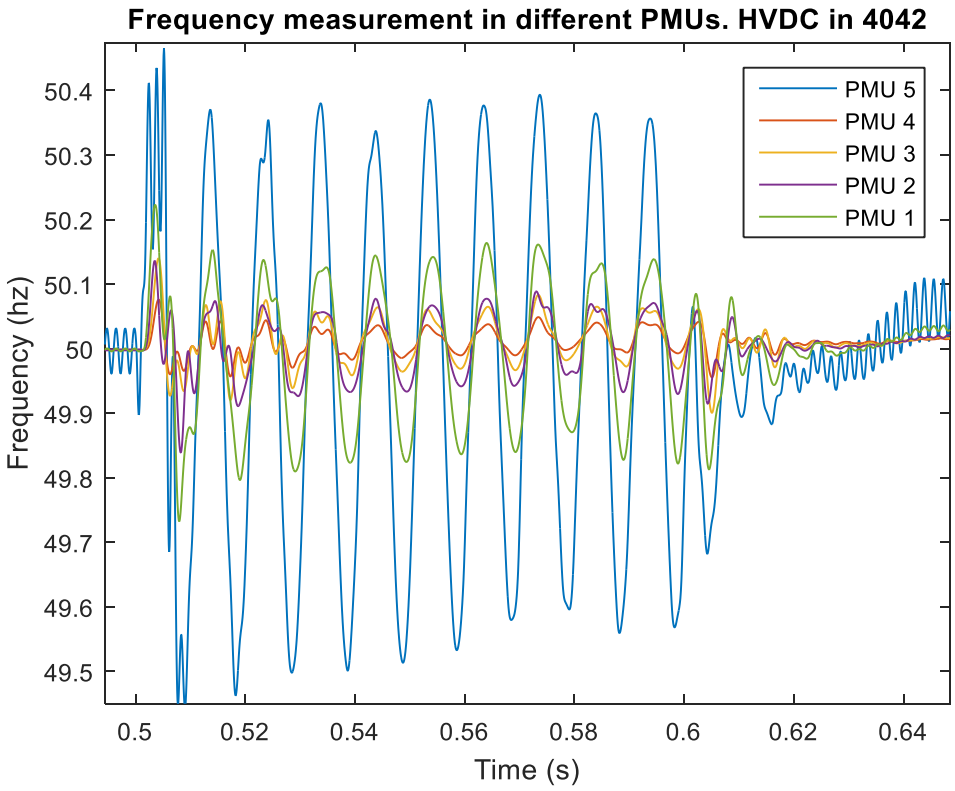

Figure 64. SLG fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Frequency signals detail (100 Hz component)

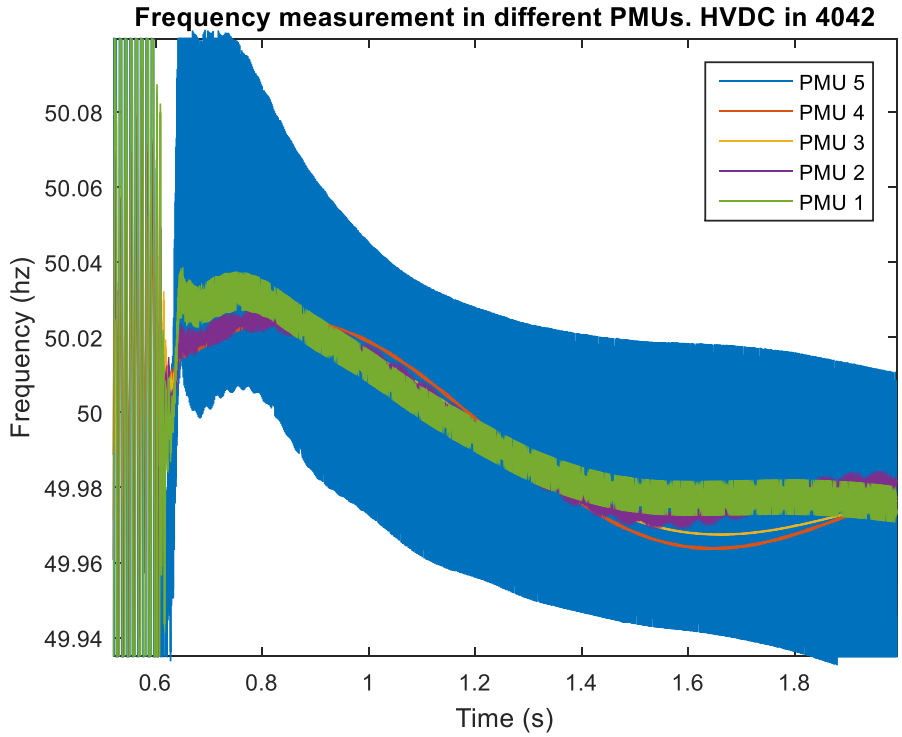

Figure 65. SLG fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Frequency signals detail (Delays)

5.3.3 HVDC externally installed at bus 4042- 3-Phase fault inverter

The result of the simulation when a Three-Phase fault is applied on Bus 4042 can be seen in figure 66. There is no 100 Hz component, as expected, and the profile of the signals differs a bit from the simulation without the HVDC in the recovery from the fault. A detail of the delays can be seen in Figure 67, where the PMUs felt the disturbance in this order: PMU 5, PMU 1, PMU 2, PMU 3 and PMU 4.

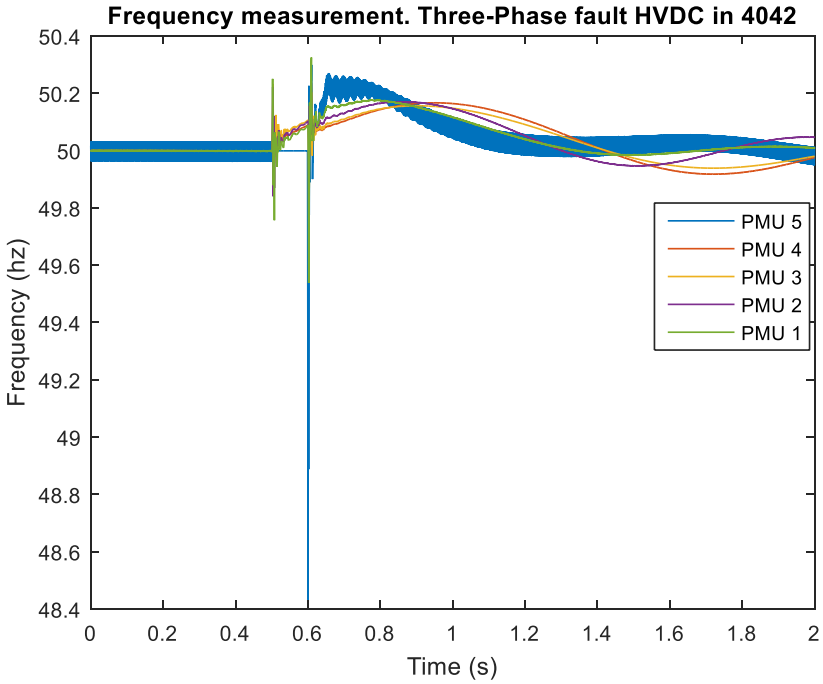

Figure 66. Three-Phase fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Frequency signal.

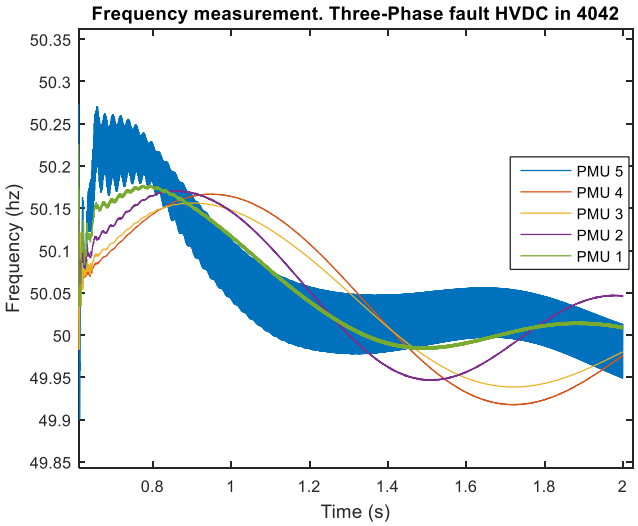

Figure 67. Three-Phase fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Frequency signals detail (Delays)

5.4 Nordic 32 simulations' summary

First of all, it must be said that the HVDC model available in Digsilent-PowerFactory is not accurate enough, as it does not respond as the models simulated in section 4. Therefore, the behavior found in that section cannot be seen in the Digsilent-PowerFactory simulations.

Electromechanically, the model that include the HVDC converter and the one without it behave in a similar way, but also have important differences as the recovery profile after fault and the noisy frequency measurement when the converter station is included in the model.

As said before, the rest of the simulation results can be found in Annex B, where current, voltage and internal signals can be compared.

6. Discussion and implications

6.1 Commutation failure in PMU data

In conclusion, after this research, the output of a PMU when a commutation fault in a HVDC converter near the unit happens, is known now. In all cases, when the commutation fault occurs, regardless its origin, the power through the converter is zero during a short period of time.

When an SLG fault on the inverter side of the transformer is the cause of the commutation failure, as explained in the model in section 4.3, the converter stops switching and it behaves as an open circuit. The positive and negative sequence currents have no path and go to zero. Only zero sequence current can flow into the transformer. The positive voltage phasor output magnitude suffers a dip of 1/3 as maximum, as one phase is temporarily disconnected. The zero-sequence current has a peak as well as the zero-sequence voltage.

When the commutation failure is generated because of a Three-Phase fault in the AC side, the magnitude of the current phasor goes to zero, as, in the same way as before, when the converter stops switching can be considered as an open circuit. In this case, the zero-sequence current as well as zero sequence voltage are zero as the grounding is not included in this case.

In case the commutation failure is caused by a Two-Phase fault, the zero-sequence current as well as zero-sequence voltage are zero, as the grounding is not connected. Positive and negative sequence voltages are equal during fault.

When the commutation failure has been caused by a Two-Phase to ground fault at the inverter, the magnitude of the positive sequence current phasor goes to zero as in all cases. Having also in this case a zero-sequence current peak due to the same reasoning as with SLG. In this case, zero-sequence voltage is equal to negative and positive sequence. The reason is because the sequence networks are interconnected in parallel on the fault location.

In any case, the hypothesis that the behavior is highly influenced by the transformer configuration, as well as that a commutation failure blocks the positive and negative sequence current, has been proved by simulations.

When using the equivalent circuits during commutation faults, the results obtained from simulations are coherent with the circuits proposed. Therefore, the transformer configuration and sequence networks associated are a decisive reason for the behavior found in the AC current signals.

The first trait that can be use is the fact that the positive sequence current become zero when a commutation failure happens. The magnitude of the rest of parameters, as negative and zero sequence currents and voltages can be used in order to determine the nature of the AC fault that lead to the commutation failure.

6.2 Commutation failure detection and location

First of all, contrarily as in the previous section, the simulations results found in the second part of the Thesis haven´t been neither conclusive nor definitive. It can be considered as a first approach and more work needs to be done in this field.

When analyzing signals from Digsilent-PowerFactory, delays can be seen and are coherent with electrical and spatial distances in the network. But these delays are pretty fast, so shouldn´t be considered caused by electromechanical wave propagation principles without prove. This fact suggest that a further study must be carried out. The distribution of generation and inertia in the Swedish grid may be a reason of this behavior but needs to be assessed properly.

The disturbances on the signals are bigger when the PMU are close by the fault and also the reaction fades away when measuring in a further point of the network.

The main differences between the simulations with and without the HVDC installed are basically three. The first one is that, from a qualitatively perspective, the shape of the signals changes. This can be used for detection purposes, but haven´t been studied deeply because of time limitations. The second and evident difference is that when the HVDC is installed, the signals close to it become noisy in the simulation. This may be due to modelling reasons or filter configuration.

The last difference is that the zero-sequence current magnitude is bigger when the HVDC is installed, in case of SLG fault. This may be due to the nature of the commutation failure or just because of the grounding of the transformer bank included in the HVDC-link. As said before, further studies are needed in order to be sure with the conclusion.

So, after the simulations, it can be concluded that commutation faults can be distinguished from SLG faults looking at the magnitude of the positive and zero-sequence current through PMUs located close by the HVDC-link only. When the PMU is located too far, the behavior fades away and it’s difficult to distinguish the faults.

It must be pointed out as well that the HVDC model available in Power-Factory is less accurate that the ones in MATLAB-Simulink and PSCAD. To perform similar simulations but with a more detailed HVDC model is highly interesting.

As explained before, in all signals derived from SLG faults, a 100 Hz component has been found. Based on [36], the behavior can be explained as in the buses where the fault is applied there is also a generator installed.

7. Conclusions and future work

After analyzing the results, some conclusions arise. Regarding the first part of the thesis, where a HVDC was analyzed in a simple network, the results are conclusive. Now, how the AC network behaves during commutation failure in a close by converter is known. How PMUs monitor that behavior is also known, and the type of fault that caused the commutation failure can be determined, based on the sequence current and voltages' magnitude.

Contrarily, the second part of the thesis, where a HVDC converter was simulated in a complex network (Nordic32), provided interesting results, but not conclusive. Delays that follows the electromechanical principles are found, but the simulation model is not accurate enough as the transformer configuration of the HVDC-link is poorly defined. Signals needs to be analyzed in detail in order to point out differences between the simulation with and without the HVDC connected.

It must be said that to perform similar simulations as in the second part but using a better HVDC model, more measurement points and different fault locations is highly interesting.

Apart from that, that will improve the current results, parts of the findings in the first part can be used for developing algorithms for fault detection and location, as well as control strategies.

To compare the simulation results with real PMU data will be very interesting to verify the conclusions and understand how the network behaves in real life when AC faults cause commutation failures and how PMUs represents that behavior.

To understand if commutation failures can trigger stability problems in the AC network is also important to know in the future.

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9 Annexes

ANNEX A: Network models

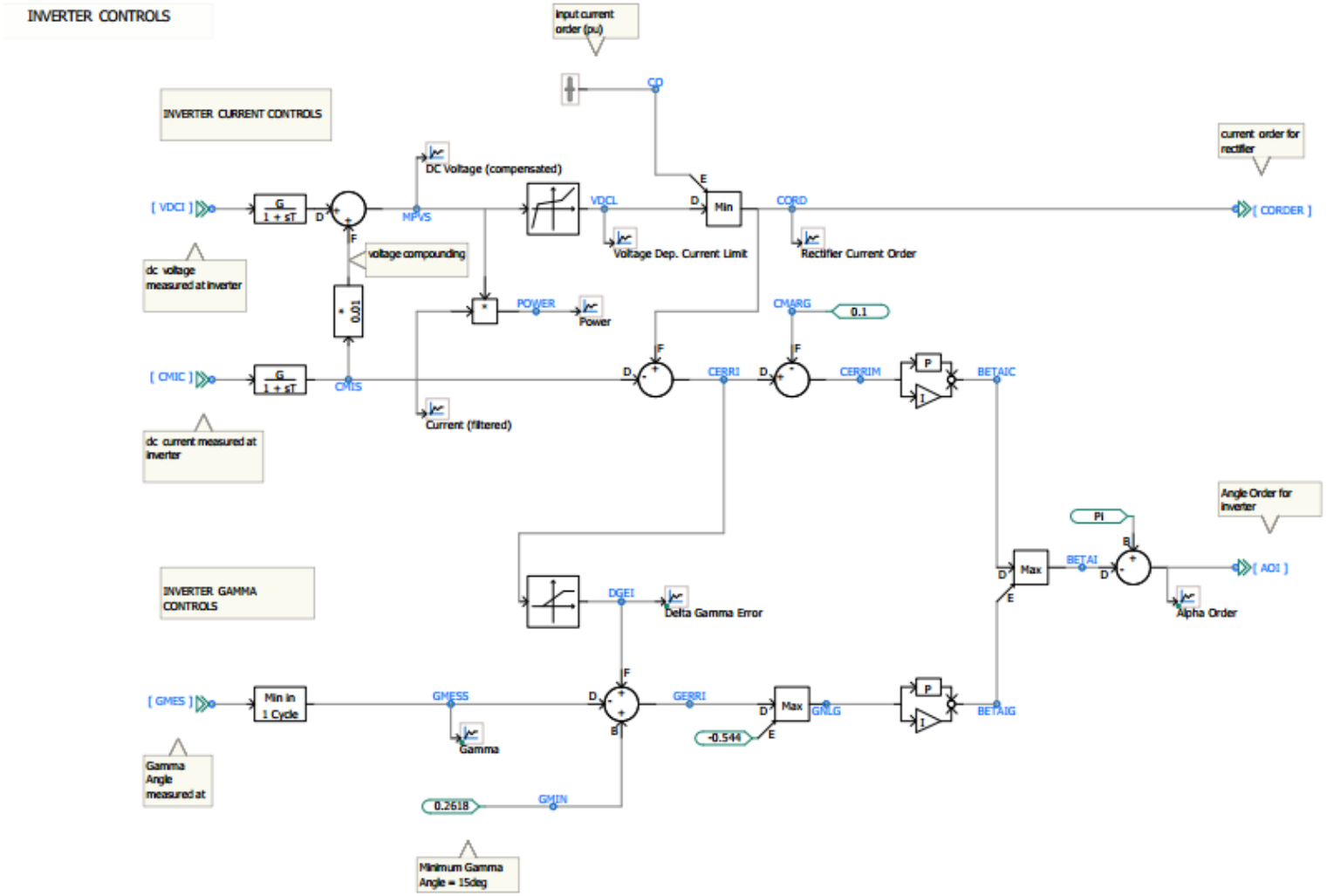

Figure 68. Inverter controls in PSCAD HVDC model.

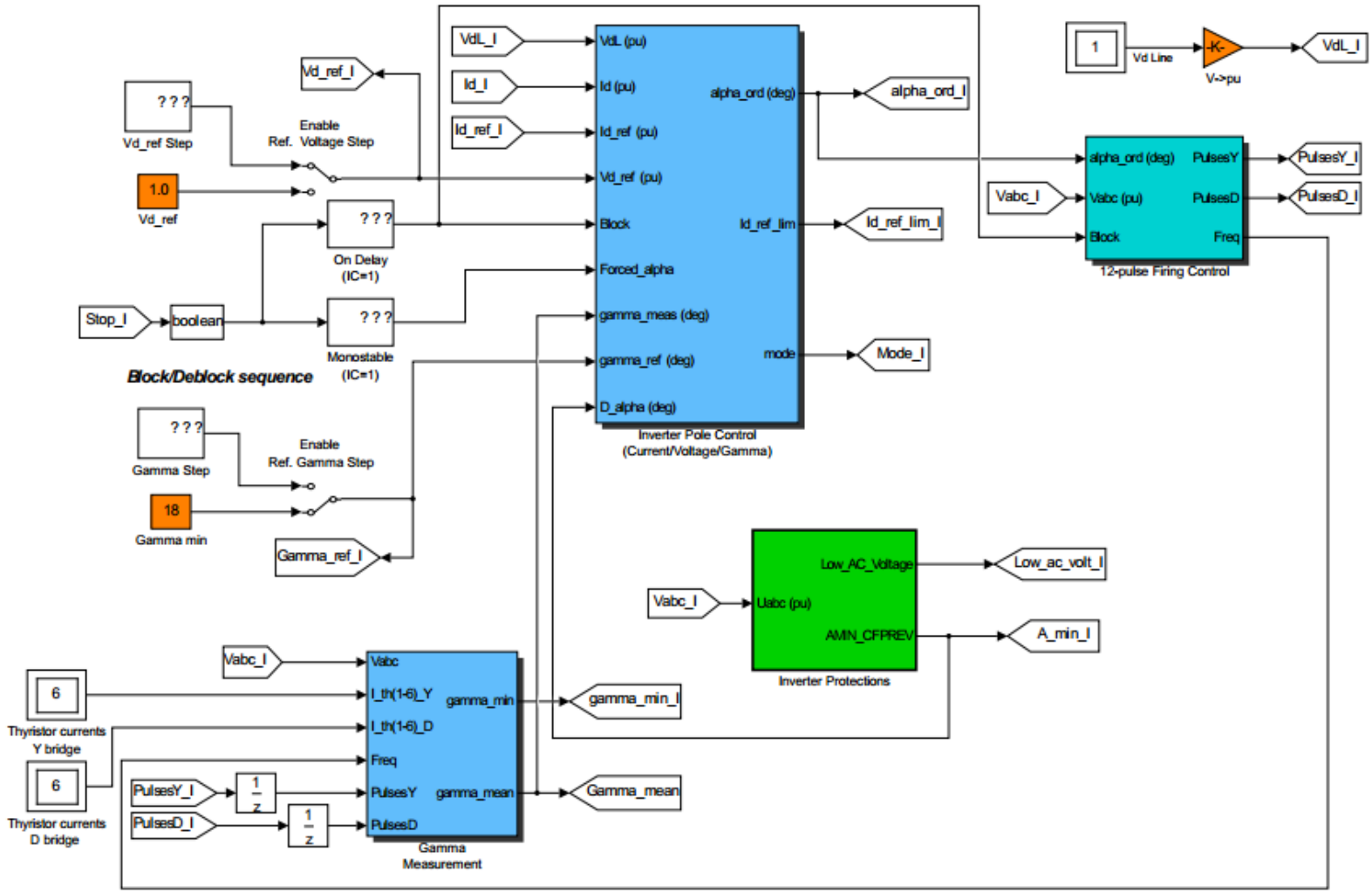

Figure 69. Inverter controls in MATLAB-Simulink HVDC model

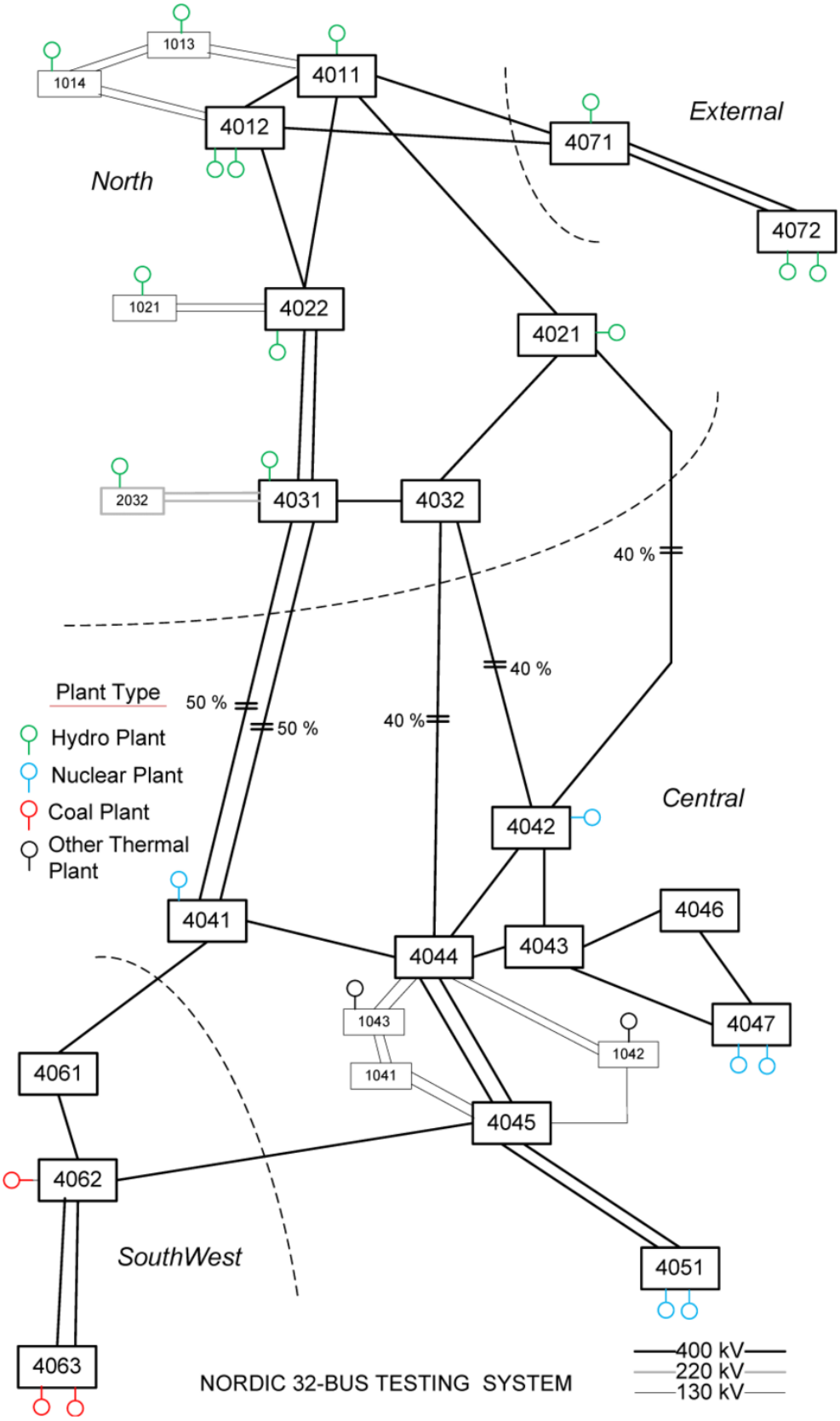

Figure 70. Original Nordic32 model [32].

ANNEX B: Simulation results

SLG fault on bus 4063- No converter installed

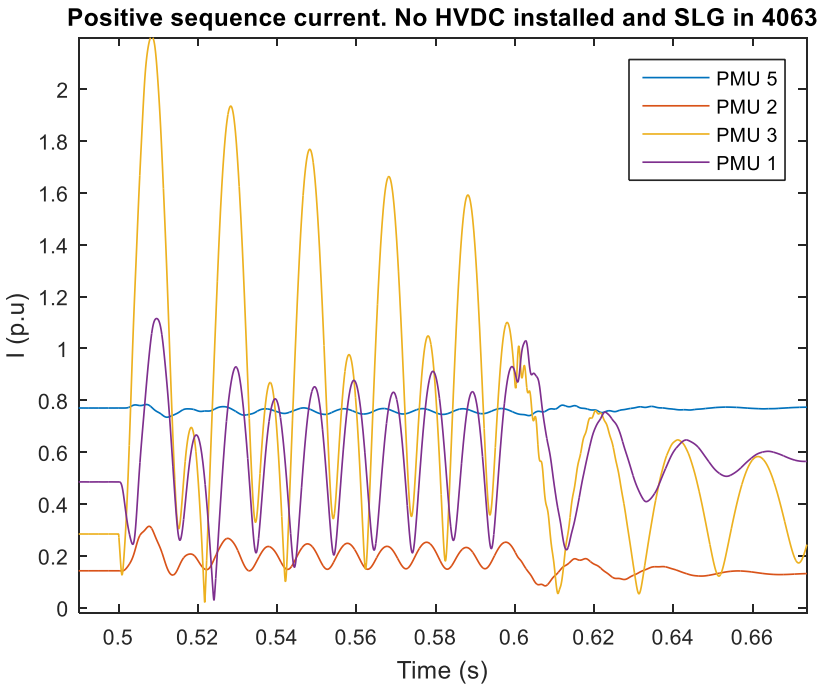

Figure 71. SLG fault on Bus4063 at t=0.5 s and self-cleared at t=0.6 s. No HVDC installed. Positive sequence current.

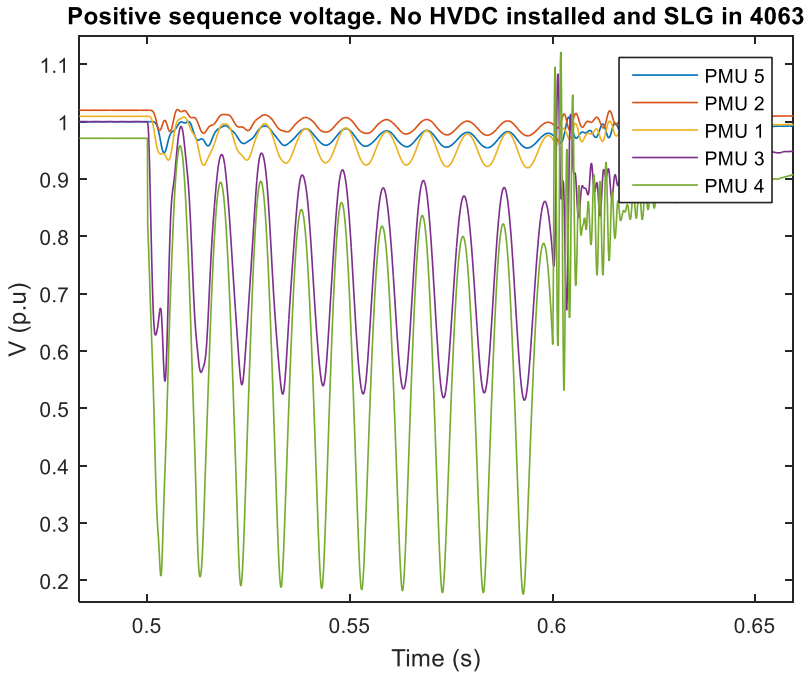

Figure 72. SLG fault on Bus4063 at t=0.5 s and cleared at t=0.6 s. No HVDC installed. Positive sequence voltage.

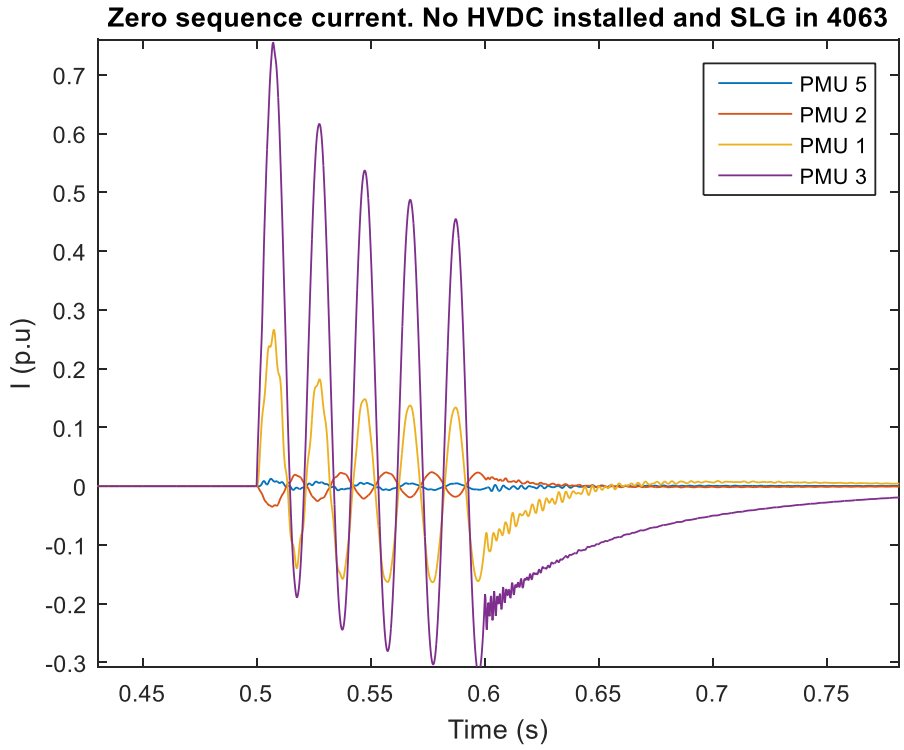

Figure 73. SLG fault on Bus4063 at t=0.5 s and cleared at t=0.6 s. No HVDC installed. Zero sequence current.

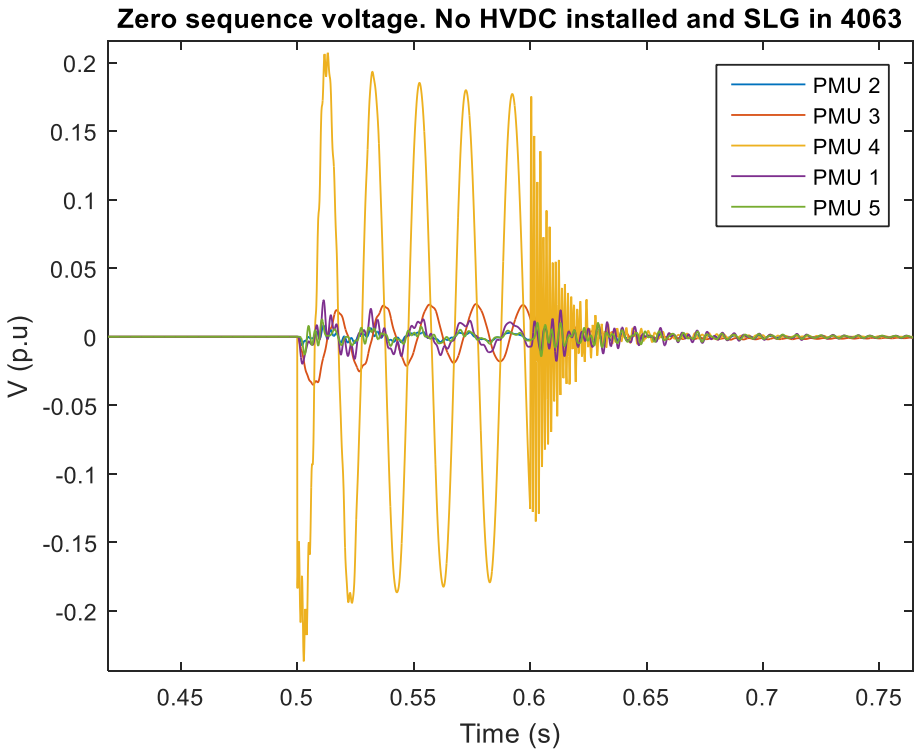

Figure 74. SLG fault on Bus4063 at t=0.5 s and self-cleared at t=0.6 s. No HVDC installed. Zero sequence voltage

SLG fault on bus 4042- No converter installed

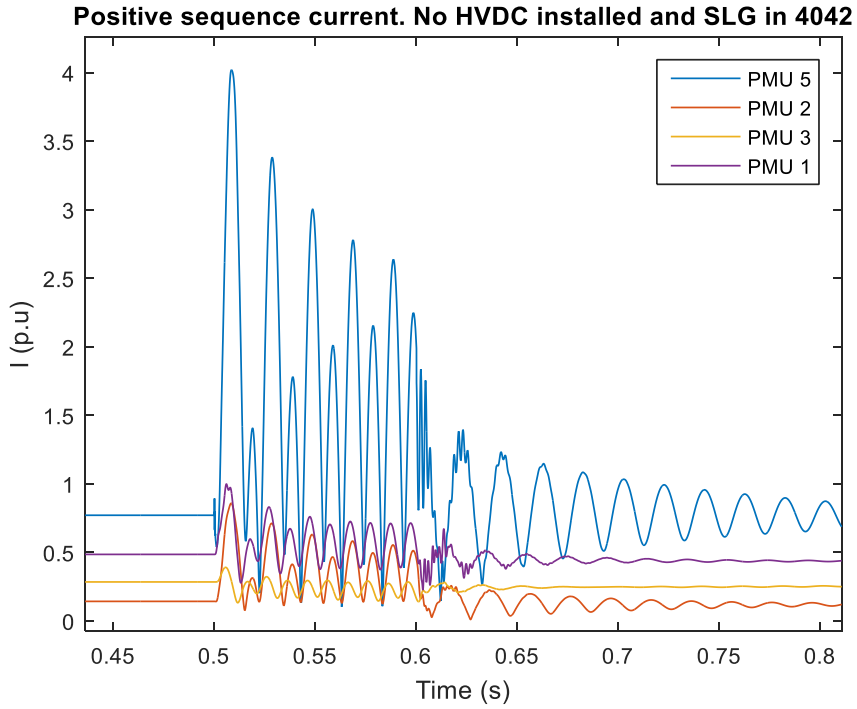

Figure 75. SLG fault on Bus 4042 at t=0.5 s and cleared at t=0.6 s. No HVDC installed. Positive sequence current

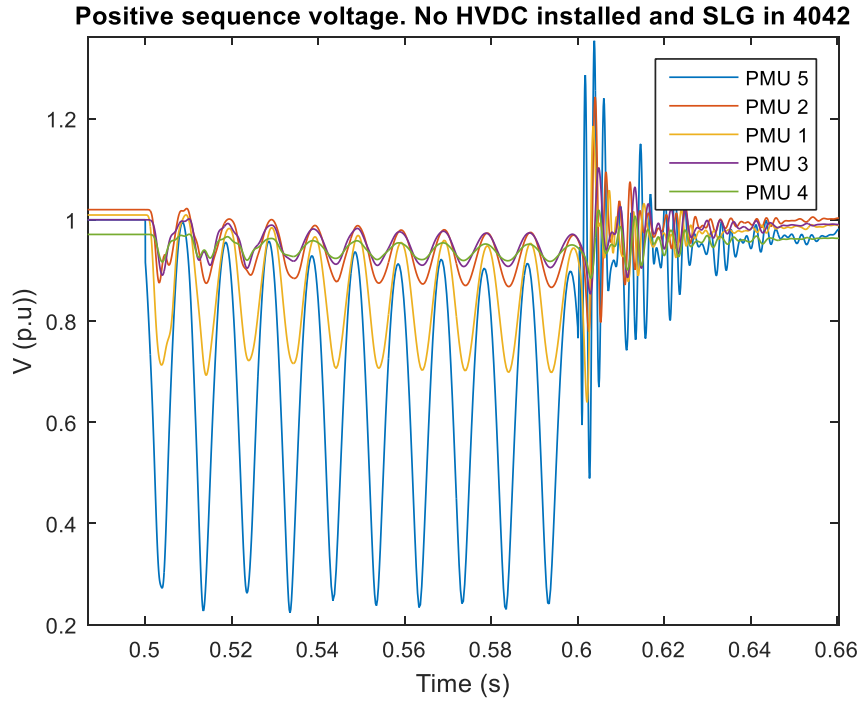

Figure 76. SLG fault on Bus 4042 at t=0.5 s and cleared at t=0.6 s. No HVDC installed. Positive sequence voltage

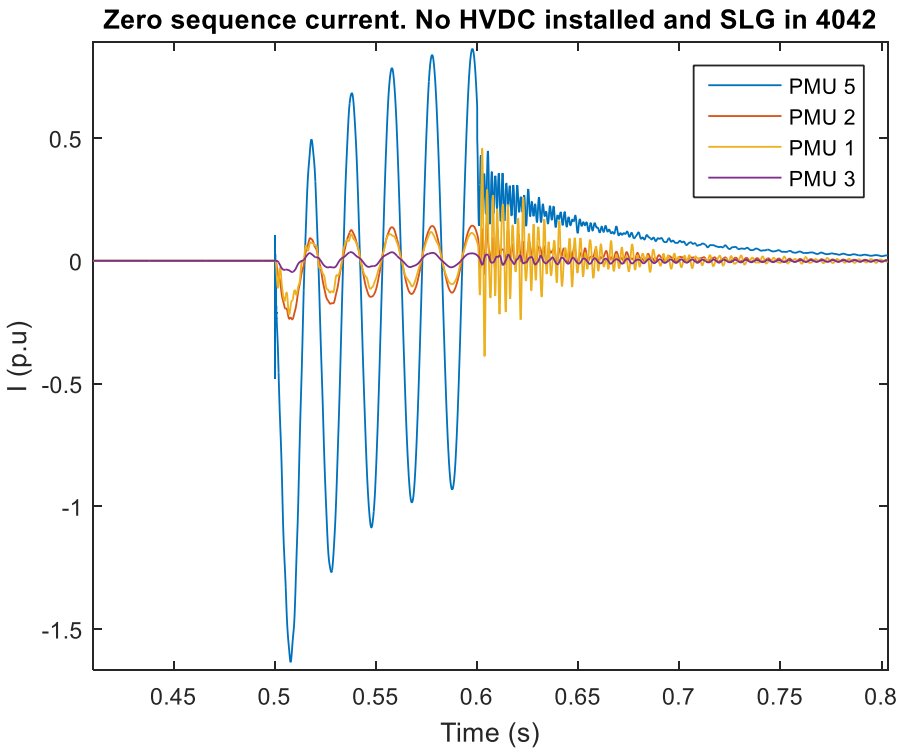

Figure 77. SLG fault on Bus 4042 at t=0.5 s and cleared at t=0.6 s. No HVDC installed. Zero-sequence current

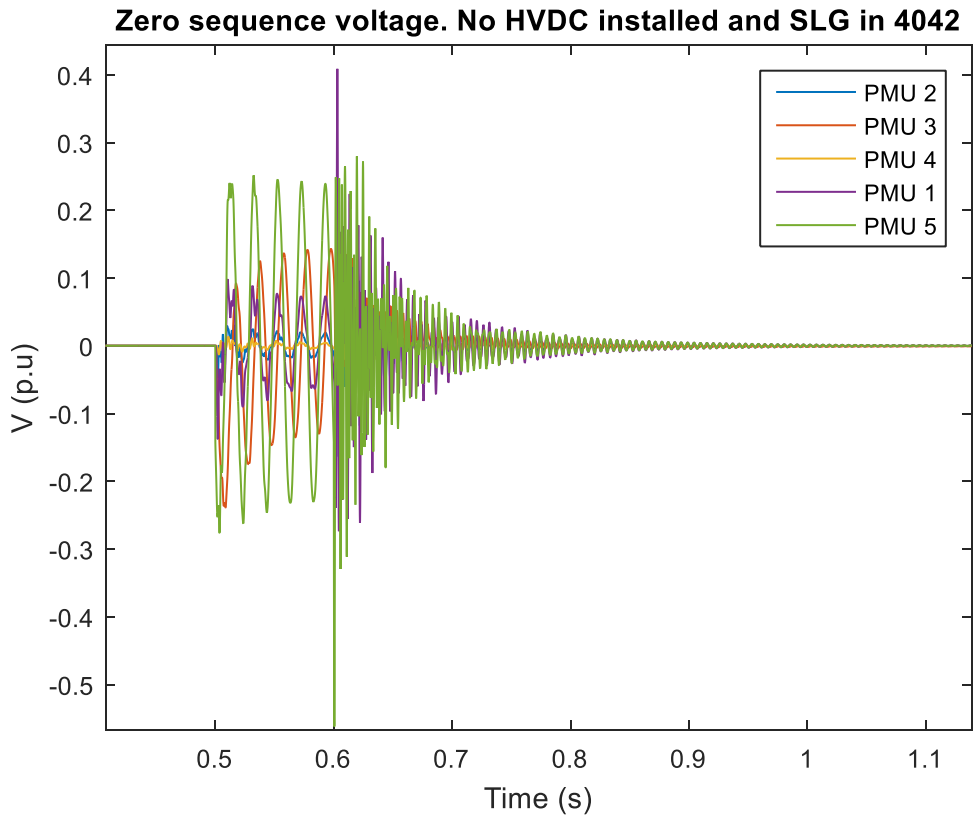

Figure 78 SLG fault on Bus 4042 at t=0.5 s and cleared at t=0.6 s. No HVDC installed. Zero-sequence voltage

Three-Phase fault on bus 4042- No converter installed

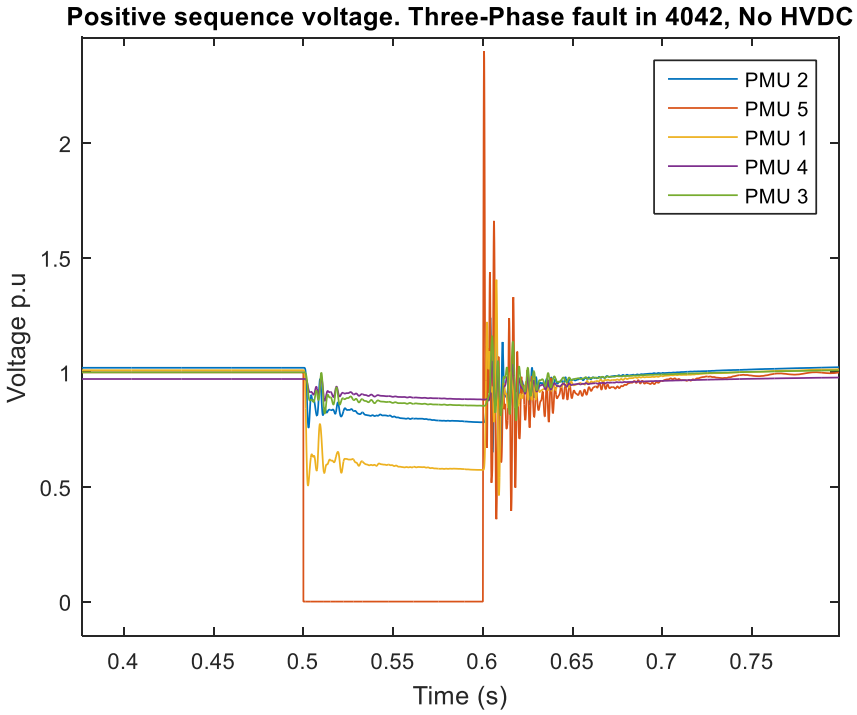

Figure 79. Three.Phase fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. No HVDC installed. Positive-sequence voltage signals

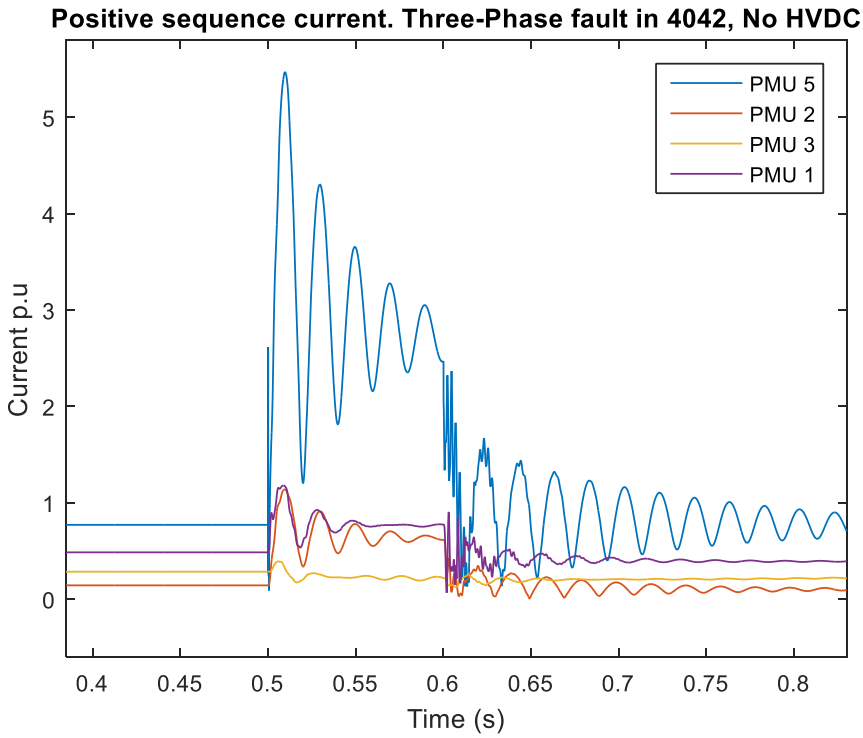

Figure 80. Three.Phase fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. No HVDC installed. Positive-sequence current signals

HVDC externally installed in bus 4063- SLG fault inverter

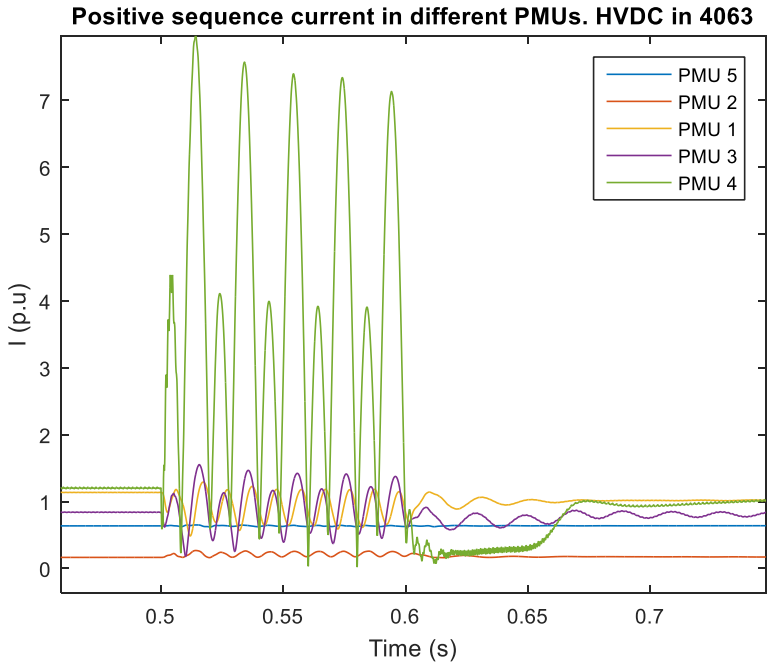

Figure 81. SLG fault on Bus 4063 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Positive sequence current

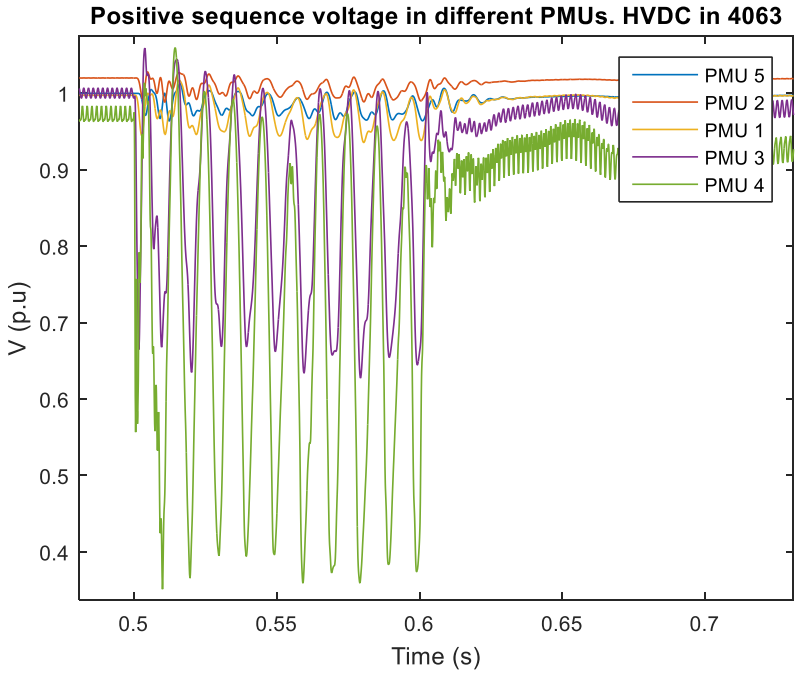

Figure 82. SLG fault on Bus 4063 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Positive sequence voltage

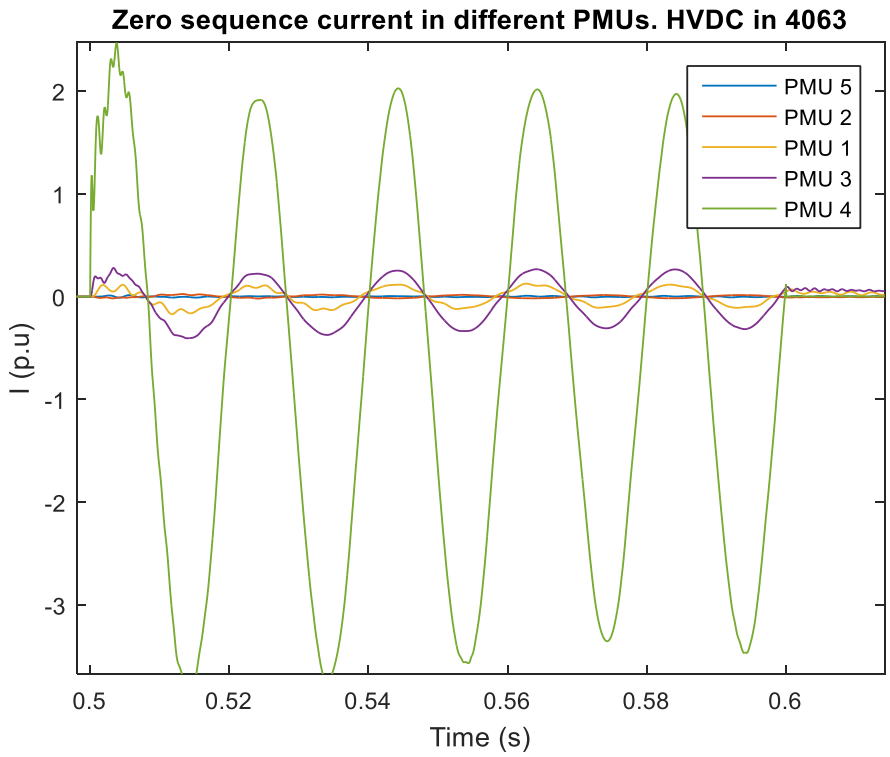

Figure 83. SLG fault on Bus 4063 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Zero sequence current

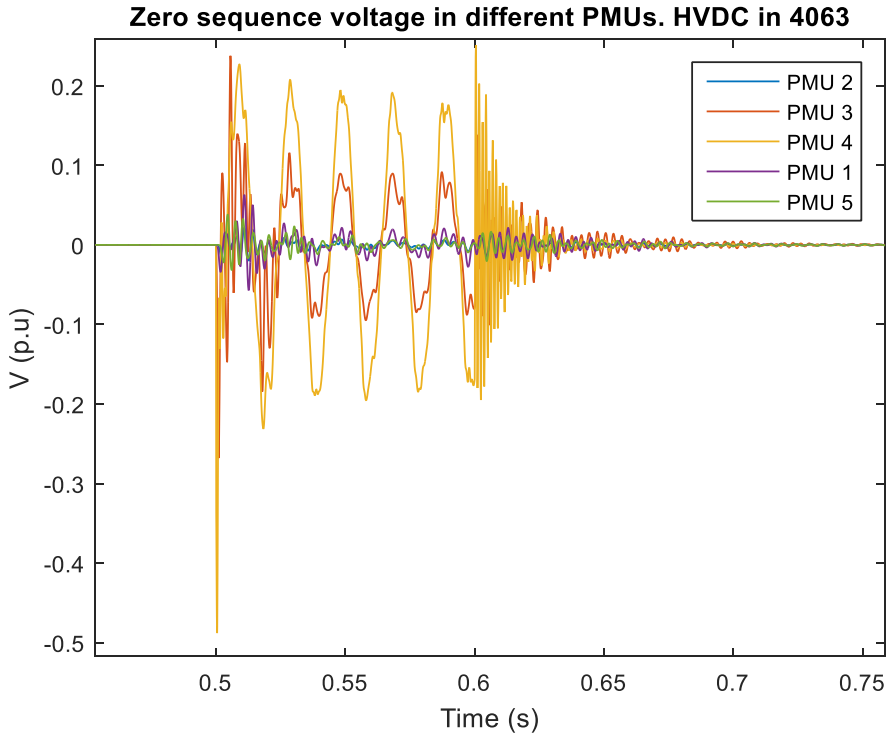

Figure 84. SLG fault on Bus 4063 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Zero sequence voltage

HVDC externally installed in bus 4042- SLG fault inverter

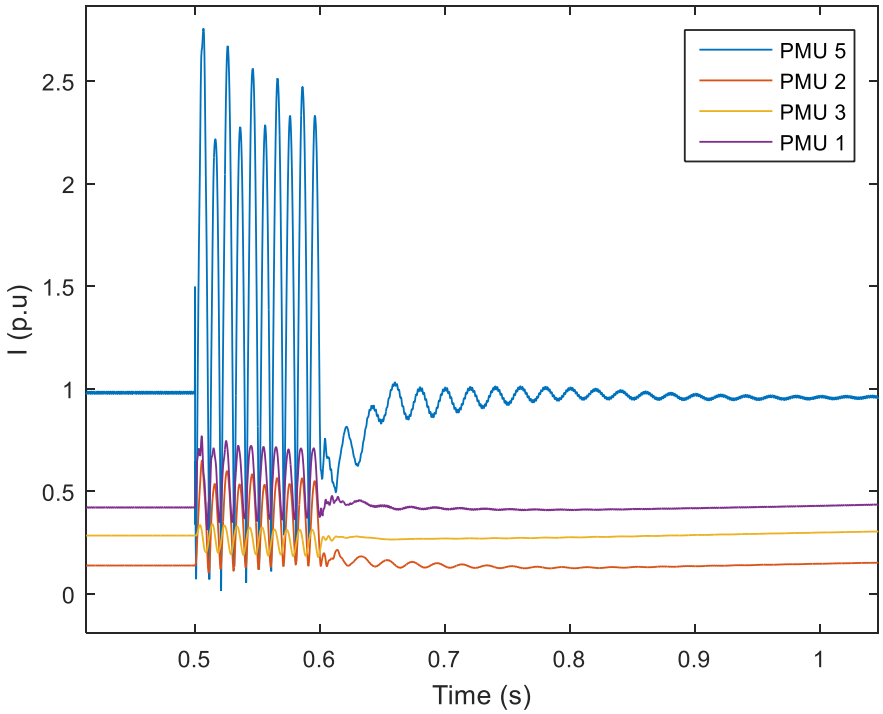

Figure 85. SLG fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Positive sequence current

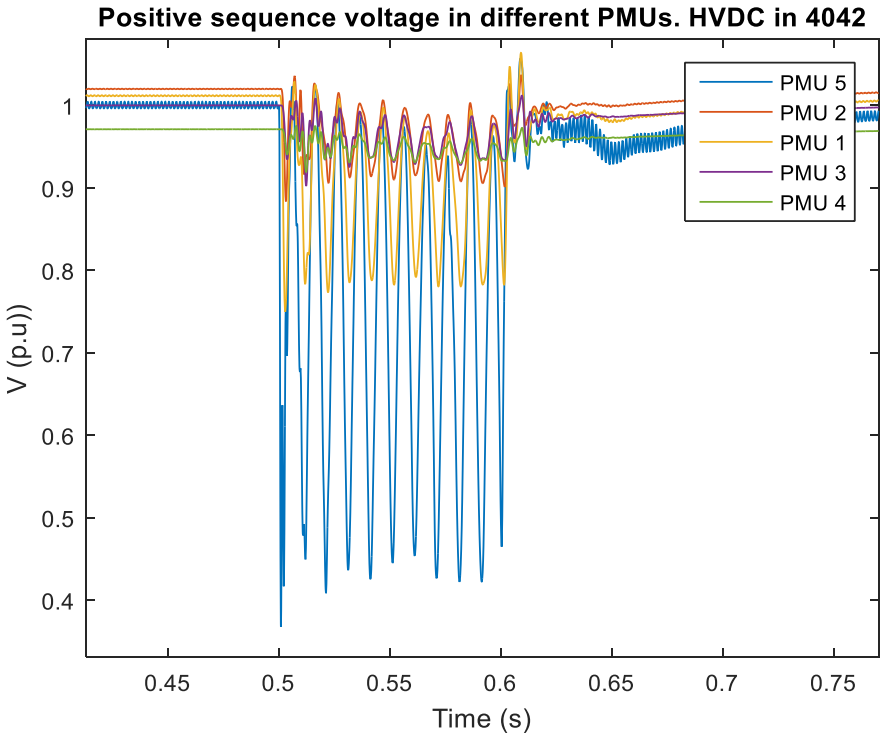

Figure 86. SLG fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Positive sequence voltage

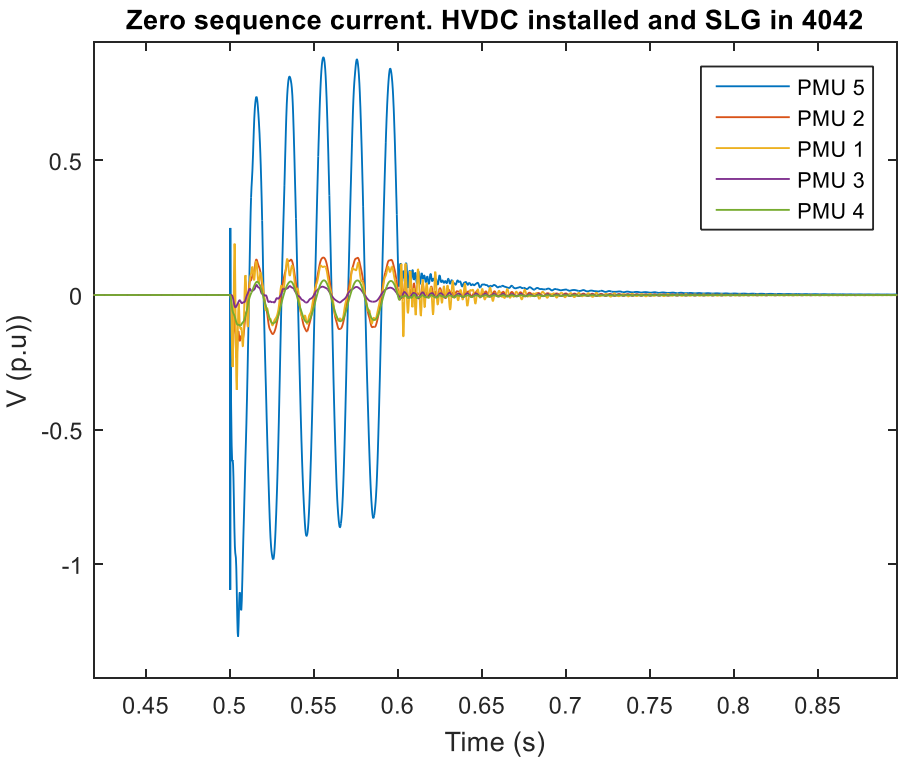

Figure 87. SLG fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Zero- sequence current

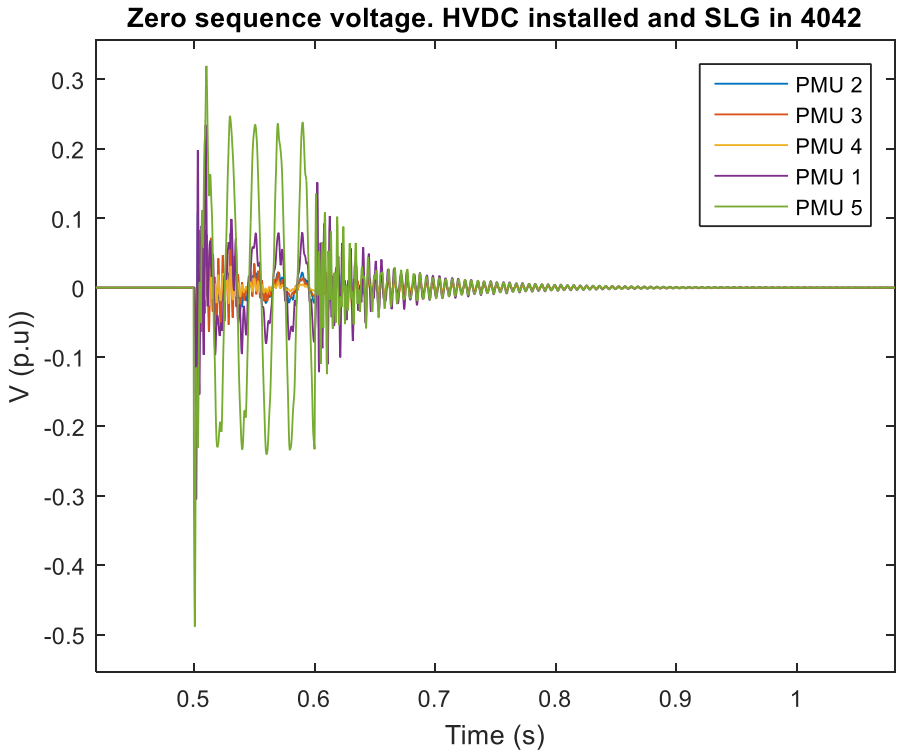

Figure 88. SLG fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Zero-sequence voltage

HVDC externally installed in bus 4042- 3-Phase fault inverter

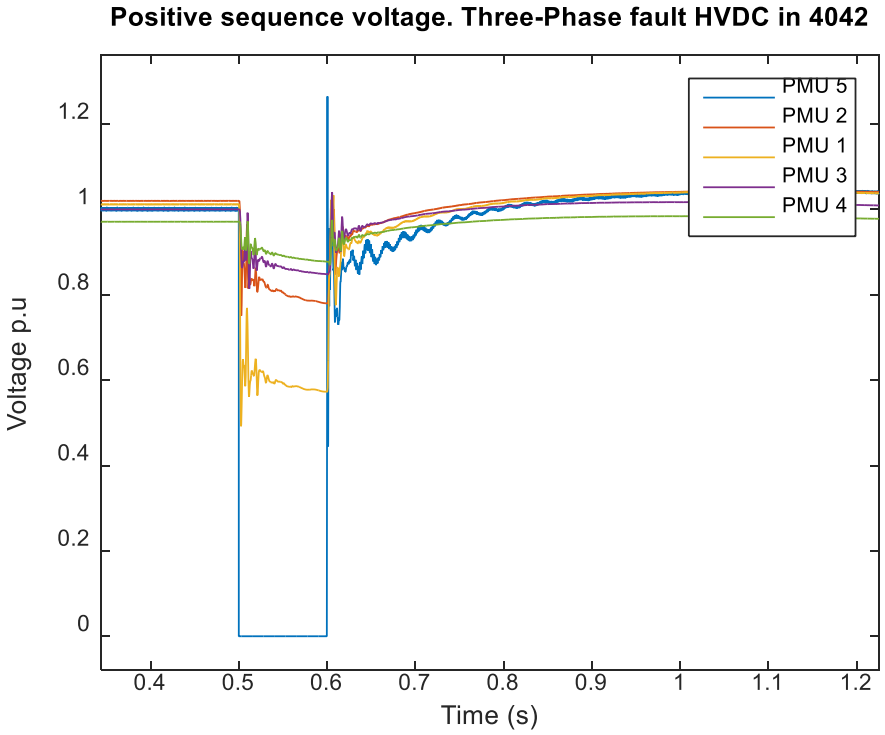

Figure 89. Three-Phase fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Positive-sequence voltage signals.

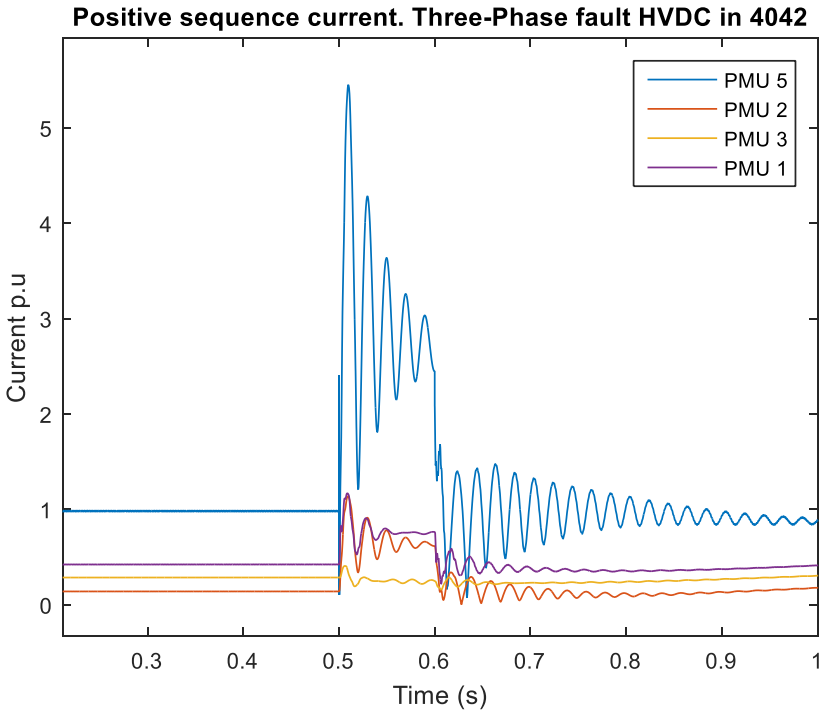

Figure 90. Three-Phase fault on Bus 4042 at t=0.5 s and self-cleared at t=0.6 s. HVDC installed on Bus 4063. Positive-sequence current signals.