Design of a power amplifier for NB-IoT

Master's Thesis

By

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Abstract

An inverse class D power amplifier and a class A power amplifier are designed at schematic level for 20 dBm power class and NB-IoT specification in 65 nm CMOS technology. A suitable switch mode supply modulator is also designed. Three different efficiency enhancement techniques namely EER, Hybrid EER and ET are studied and the suitable transmitters are simulated for each in Cadence Virtuoso. These transmitters are compared with each other on the basis of output power, efficiency, and NB-IoT specifications of EVM and ACPR. The peak efficiency achieved by the supply modulator is 90%. The peak output power that can be achieved by ET, EER and hybrid EER is 24 dBm with efficiency of 37%, 28 dBm with an efficiency of 66% and 28 dBm with an efficiency of 66% respectively. It is also observed that, the low modulation bandwidth and relaxed specifications of NB-IoT standard, make EER architecture more tolerant to the delay mismatch between the envelope and phase path as compared to the other standards like 802.11a (Wi-Fi). With a delay of T/13, where T is the symbol duration, EER achieves a maximum power of 26 dBm while staying within limit of EVM and ACPR specified by NB-IoT. Thus, according to the analysis conducted in the report, EER with inverse class D amplifier proves to be the most promising architecture for NB-IoT specifications as compared to ET and hybrid EER architectures.

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Rajeshwari Yogi

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List of acronyms

ACPR	Adjacent Channel Power Ratio
BPSK	Binary Phase Shift Keying
CMOS	Complementary Metal Oxide Semiconductor
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
EVM	Error Vector Magnitude
GSM	Global System for Mobile
LoRa	Long Range
LPWAN	Low Power Wide Area Network
LTE	Long Term Evolution
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NB-IoT	Narrow Band Internet of Things
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SMPS	Switched Mode Power Supply
SoC	System on Chip
UE	User Equipment
UTRA	Universal Terrestrial Radio Access
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	Wireless Local Area Network

Popular Science Summary

The rapid growth in connected devices promises lucrative business opportunities in the Internet of Things (IoT) segment. Narrow Band IoT (NB-IoT) is a new mobile standard. The services leveraging Low Power Wide Area technologies desire wide coverage along with low power consumption and a large number of connections. As lifetime of 10 years or more is desired in battery operated devices, it makes low power consumption an important requirement for such devices.

The overall power efficiency of a radio circuit is strongly dependent on the power amplifier (PA). Design of the power amplifier also depends on the transmission technique to be used. As a result, the design and implementation of the PA as well as selection of the transmission technique requires detailed attention and efforts to ensure the maximum efficiency and sufficient linearity.

In this project, an inverse class D power amplifier and a class A power amplifier are designed at a schematic level for NB-IoT specifications in 65 nm CMOS technology. These power amplifiers are designed for 20 dBm power class. A switch mode supply modulator is also designed. Since the efficiency is a crucial factor that enables extending battery life of the devices, three different efficiency enhancement techniques: Envelope Elimination and Restoration (EER), hybrid EER and Envelope Tracking (ET) are studied and the transmitters are simulated for each technique. These transmitters are compared with each other on the basis of the output power, efficiency, NB-IoT specifications of EVM and ACPR. According to the analysis conducted in the report, EER with inverse class D amplifier proves to be the most promising architecture for the NB-IoT applications.

1. Introduction

This chapter gives a brief overview of the different concepts being used in the project. It aims at helping the reader to have a better understanding of the thesis project.

1.1. Narrow Band IoT and comparison with different Low Power Wide Area Network technologies

Narrow Band IoT (NB-IoT) [1] is a new mobile standard. It is a Low Power Wide Area Network (LPWAN) technology which is optimized for applications that need low bandwidth and need to send lesser amounts of data infrequently. Some applications [2] of NB-IoT include smart metering, smart city infrastructure, intruder alarms, facility management services etc.

The major characteristics of NB-IoT that makes it suitable for LPWAN applications include:

1. No need of additional infrastructure
2. Improved indoor coverage (+20 dB better coverage than GSM)
3. Longer battery life (approximately 10 years of battery life)
4. Ability to achieve large number of connections (50,000 connections per cell)

NB-IoT can be deployed in 3 different ways [2] as shown in Figure 1:

1. Stand Alone: utilizes an independent resource block
2. In Band: utilizes resource block within the LTE carrier
3. Guard Band: utilizes the unused resources in the guard band of the LTE carrier

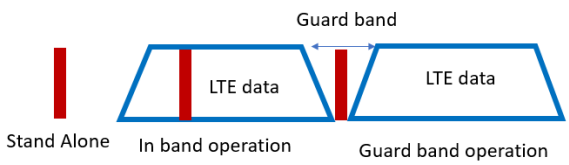

Figure 1 NB-IoT deployment scenarios

As compared to technologies like Long Range Radio (LoRa) [3] and SIGFOX [4] which operate in unlicensed band, as NB-IoT is operated in licensed spectrum, it provides several advantages [1] like improved quality of service, lower deployment costs and lower restriction on power and duty cycle as compared to unlicensed spectrum. The deployment cost is lower as existing cellular networks can be used.

LTE-M [1] and NB-IoT are both cellular protocol standards operating in the licensed spectrum. NB-IoT is optimized for low bandwidth requirements (200 kHz) and stationary devices while LTE-M is optimized for mobile connections and the applications having a higher bandwidth (1.4 MHz) requirement. The latency requirements in NB-IoT are less stringent than LTE-M. Thus, NB-IoT has an application focus where the time delay in sending and receiving information can be allowed whereas, LTE-M has application areas where only a small delay can be tolerated.

1.2. Linear and switch mode power amplifiers

The fundamental trade-off in power amplifiers is between the efficiency and the linearity. All power amplifiers can be broadly classified into 2 major categories – 1) Linear power amplifiers and 2) Switch mode power amplifiers. In a linear PA, the device acts as a transconductor while in a switch mode PA, the device acts as a switch [5]

1.2.1. Linear power amplifiers

The linear power amplifiers have a good linearity but a lower efficiency as compared to the non-linear power amplifiers. The basic circuit diagram of a linear amplifier is shown in the Figure 2 [6]. Here, R_l represent the load, the large inductor (RFC) provides a constant dc current to the drain of the device and the large capacitor (BFC) prevents any dc current flowing to the load.

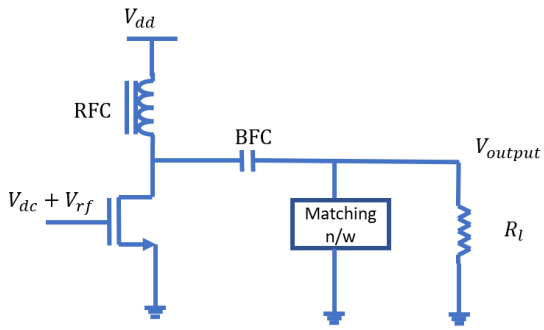

Figure 2 Basic circuit diagram of a linear power amplifier

The linear power amplifiers can be further classified into class A, B, AB or C depending upon the conduction angle. A conduction angle is the portion of input cycle during which the device conducts. It can range from 0° to 360°.The conduction angle varies depending on biasing of the device. Thus, by varying the quiescent point (biasing point), different classes of linear PA can be designed. This is shown in Figure 3 [7], [8] where, I_d represents the drain current, V_{gs} represents the gate-source voltage of the device and V_{th} represents threshold voltage of the device.

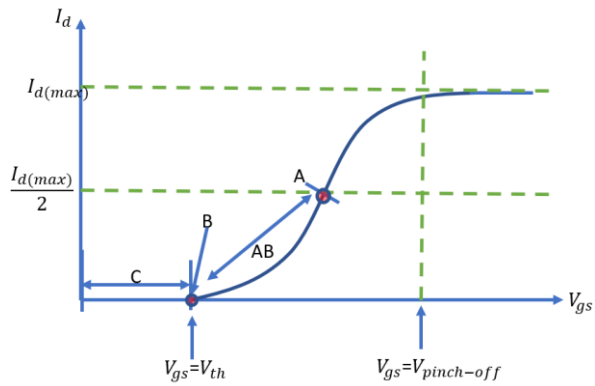

Figure 3 Classification of linear power amplifiers on the basis of quiescent point.

Depending on the conduction angle, drain efficiency of linear amplifiers can be changed. With help of (1), the theoretical efficiencies for all classes of linear power amplifiers can be calculated [6].

$$\eta = \frac{\alpha - \sin(\alpha)}{4(\sin\left(\frac{\alpha}{2}\right) - (\left(\frac{\alpha}{2}\right)\cos\left(\frac{\alpha}{2}\right)))} \quad (1)$$

Where, α is the conduction angle and η is the theoretical efficiency.

The different linear power amplifier classes are briefly described in the following section [6]-[8].

1.2.1.1. Class A Power amplifier

The class A power amplifier is designed by biasing the device at half of the maximum drain current. The conduction angle is 360°. Thus, the device is always conducting even when there is no input signal. As a result, the product of drain voltage and drain current is always positive. This is the main cause of low efficiency in this class of amplifier. On the other hand, a class A PA has the highest linearity as compared to other amplifier classes. By substituting value of $\alpha = 2\pi$ in (1), the theoretical maximum efficiency is found to be 50%.

1.2.1.2. Class B Power Amplifier

In a class B amplifier, the device is biased at the threshold voltage. The conduction angle in this case reduces to 180° as compared to 360° in the case of a class A amplifier. Even though the linearity of class B power amplifiers is lower than class A amplifiers, they are more efficient. Substituting $\alpha = \pi$ in (1) gives theoretical efficiency of 78.5%. An example for a practical peak power added efficiency (PAE) that can be obtained for the frequency range of our interest can be found in [9]. Here a two-stage class B PA is designed in 250 nm CMOS technology to achieve a PAE of 27.4% for peak output power of 29 dBm at 1.9 GHz.

1.2.1.3. Class AB Power Amplifier

This class of amplifiers is a good compromise between the linearity and efficiency. The conduction angle of class AB power amplifiers is between 360° and 180°. As the conduction angle increases, the efficiency decreases but the linearity improves. A 3 GHz fully integrated class AB power amplifier used for WLAN and Mobile WiMAX standards is designed in [10]. It achieves a saturated power of 27.9 dBm and PAE of 12.7%.

1.2.1.4. Class C Power Amplifier

In a class C amplifier, the conduction angle is less than 180°. The linearity is lower than a class B amplifier but, the theoretical maximum efficiency can reach 100% by making the conduction angle close to zero. This can be observed by substituting $\alpha = 0$ in (1). However, making the conduction angle zero, also makes the output power zero [6]. A class C power amplifier for 2.4 GHz is designed in [11] that achieves a peak PAE of 43% for a peak output power of 19.7 dBm.

1.2.2. Switch mode power amplifiers

The switch mode power amplifiers have a good efficiency but lower linearity than linear power amplifiers. The theoretical maximum efficiency that these power amplifiers can reach is 100%. (1) shows that the efficiency of amplifier can be improved by reducing the conduction angle i.e. by reducing the overlapping between the drain current and drain voltage curves. In switch mode amplifiers, the device acts as a switch instead of a transconductor. This ideally makes overlapping between the drain current and drain voltage curves zero, which significantly reduces the power dissipation. This is shown in Figure 4 [12] where, I_d is the drain current and V_d is the drain voltage. Thus, the switch mode amplifiers can reach a theoretical maximum efficiency of 100%. They can be further classified as class D, E, F etc. depending on their configuration.

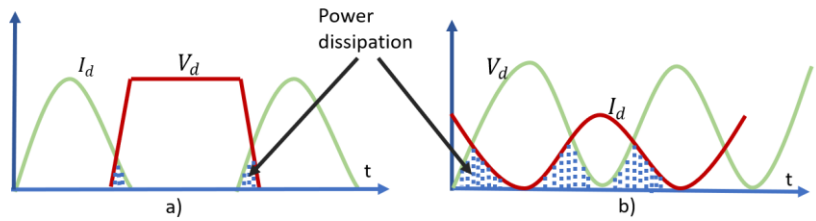

Figure 4 Power dissipation in a) a switch mode PA b) a linear PA

1.2.2.1. Class D power amplifier

Class D power amplifier uses a pMOS and an nMOS device that acts as a switch. Class D amplifier can either be implemented in voltage mode or a current mode (Inverse class D amplifier). Figure 5 shows a voltage mode class D amplifier and a current mode class D amplifier where, V_{DD} represent the supply voltage and R_l is the load resistor [13]. In Figure 5.a, C_0 and L_0 form a part of the resonant circuit

and in Figure 5.b L and C form a part of the resonant circuit. Figure 6 shows their respective drain current (I_d) and drain voltage (V_d) waveforms. Although a class D amplifier can achieve a theoretical efficiency of 100%, it suffers from various losses due to on-resistance, parasitic capacitance, finite switching time etc. An inverse class D amplifier is designed in 65 nm technology in [13] which achieves a peak output power of 21.8 dBm with an efficiency of 44%.

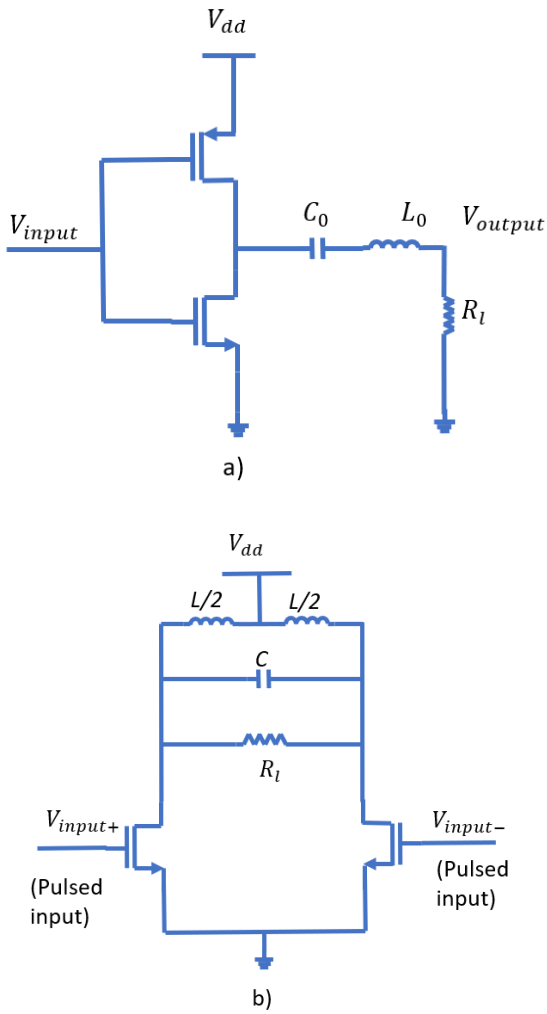

Figure 5 a) Basic class D PA b) Basic class D^{-1} PA [13]

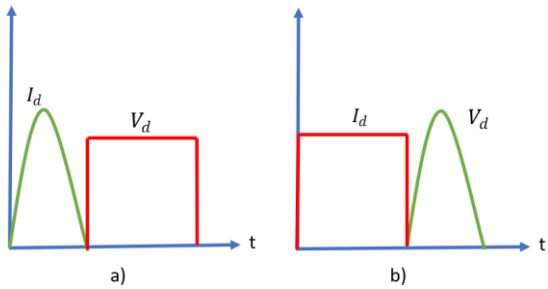

Figure 6 Drain current and Drain voltage for a) class D and b) class D^{-1}

In high frequency (GHz) application, the conventional class D amplifier suffers from some drawbacks [13]:

1. Since the drain capacitors of the transistors do not form part of the resonant circuit, they need to be charged and discharged every cycle which causes unnecessary power dissipation which is directly proportional to the frequency of operation.

2. The conventional class D amplifier uses a pMOS and an nMOS device. The width of a pMOS device needs to be made around 2 or 3 times the width of an nMOS transistor for it to have equal resistance as the nMOS device. This leads to increase in the required area and increase in the input capacitance. Increase in the input capacitance leads to increase in the time required to charge and discharge the input capacitance thus, increasing the switching time of the transistor. Also, increase in the input capacitance causes reduction in ω_T and ω_{max} where, ω_T is the maximum frequency where current gain of the device falls to unity and ω_{max} is the frequency where power gain of the device falls to unity [6]. ω_T and ω_{max} is given as [6]:

$$\omega_T = \frac{g_m}{C_{gs}+C_{gd}} \tag{2}$$

$$\omega_{max} = \frac{1}{2}\left(\sqrt{\frac{\omega_T}{r_g C_{gd}}}\right) \tag{3}$$

Where,

ω_T: frequency at which the current gain falls to unity

g_m: transconductance of the device
C_{gs}: gate-to-source capacitance
C_{gd}: gate-to-drain capacitance
ω_{max}: frequency at which the power gain falls to unity
r_g: gate resistance

In addition to overcoming the above-mentioned drawbacks, the inverse class D amplifier has other advantages [13]-[15]:

1. Inductance of the resonant circuit is absorbed into the balun, which functions as a matching network in addition to differential to single ended conversion of the output.

2. Zero voltage switching (ZVS) is achieved i.e. when the transistor is turned ON, the voltage across it is zero. Thus, the problem of discharging the capacitor every time is removed.

1.2.2.2. Class E amplifier

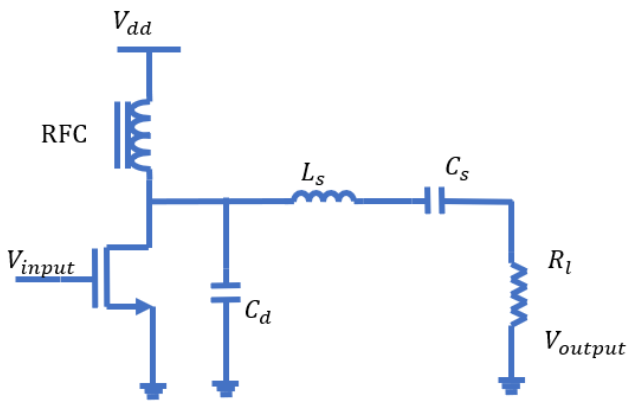

Figure 7 Basic circuit diagram of class E amplifier [5]

A class E amplifier [16] can also achieve a 100% theoretical efficiency, as in the case of a class D amplifier. A basic circuit diagram of class E amplifier is shown in Figure 7 where, V_{dd} is the supply voltage, L_s and C_s for a part of the matching

network and R_l is the load resistor. Single ended class E amplifier uses one active device. The drain-source capacitance associated with the device can be absorbed into the matching network. Class E amplifier achieves zero voltage switching (ZVS). Hence, the parasitic capacitances do not need to be discharged thus, reducing the switching losses. In addition to ZVS, it also achieves first derivative of switch voltage as zero when the switch is turned on [13]. Although class E amplifier can achieve a theoretical maximum efficiency of 100%, it suffers from some disadvantages [13]. Class E amplifier uses a larger number of passive components than class D amplifier. The passive components have finite quality which causes reduction in the practical maximum efficiency. One major disadvantage of a class E power amplifier is the peak drain voltage that can cause stress on the device and damage the long-term reliability of the amplifier. In [17] the design equations for optimum operation of class E power amplifier with a shunt capacitor and a series resonant circuit are derived with help of the steady state drain current and drain voltage equations of the class E amplifier. With help of fourier analysis, [17] shows that the peak drain voltage is given as:

$$V_{peak} = -2\pi\varphi V_{dd} \tag{4}$$

Where,

V_{peak} is the peak drain voltage

V_{dd} is the dc supply voltage

φ is the phase shift given as [17]:

$$\tan(\varphi) = -\frac{2}{\pi} \tag{5}$$

Thus,

$$\varphi = tan^{-1}\left(-\frac{2}{\pi}\right) = -0.5669 \text{ rad.} \tag{6}$$

Substituting the value of φ in (4),

$$V_{peak} = 3.56V_{dd}$$

A class E amplifier designed in [18] achieves a peak output power of 28.5 dBm with an efficiency of 43.6% at 2.4 GHz in a 180 nm CMOS process.

1.2.2.3. Class F amplifier

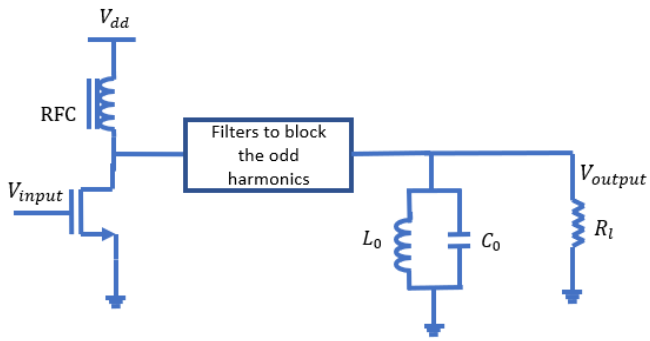

Figure 8 Basic class F power amplifier [5]

The distinguishing feature of the class F power amplifier [6] is the complex matching network. A basic class F power amplifier is shown in Figure 8 where, R_l is the load resistor, V_{dd} is the supply voltage, L_0 and C_0 form a part of the tank circuit that is resonant at the fundamental frequency. The matching network is composed of different LC filters such that the odd harmonics are blocked and as the parallel tank circuit is tuned to be resonant at the fundamental frequency (the desired carrier frequency), it acts as a short circuit for frequencies outside the desired frequency bandwidth. In practice, the class F amplifiers can achieve a better efficiency than the class E amplifiers [6] but, the number of passive components involved in the design as well as the design complexity is much higher than class D and E power amplifiers.

1.3. Envelope Tracking (ET), Envelope Elimination and Restoration (EER) and Hybrid Envelope Elimination and Restoration (Hybrid EER) power amplifier architectures

1.3.1. Envelope Elimination and Restoration

In the Envelope Elimination and Restoration (EER) technique [5], [19]-[21] as the name suggests, the envelope is first "eliminated" from the input signal and is "restored" later in the output. This technique is also known as polar modulation. As input to the PA is a constant amplitude signal, a switch mode PA can be used. This results in high efficiency. Figure 9 shows the basic principle of EER technique.

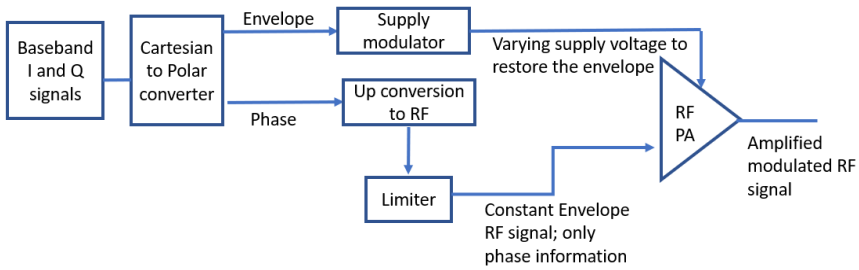

Figure 9 Block diagram demonstrating working principle of EER

In EER, the input signal is first converted to its polar equivalent to separate the amplitude and phase information. The phase signal in then up-converted to the desired carrier frequency before feeding it to the limiter. The limiter forms a constant envelope signal which then forms an input to the switch mode PA. The envelope signal goes to the supply modulator. The supply modulator performs an important function of re-establishing the envelope to the output signal by varying the supply voltage going to the PA in accordance with the envelope information. The PA combines the phase information from the constant envelope input signal with the envelope information from supply modulator to form a modulated output signal. EER thus ensures a high efficiency while maintaining the necessary linearity. Theoretically, it can achieve a 100% efficiency. EER requires an accurate dynamic power supply and an accurate alignment of amplitude and phase information [20], [21]. Since, bandwidth of the phase signal is more than that of the baseband signal, it limits the application of EER technique to narrow band systems. However, [22] shows EER technique efficiently implemented for LTE with channel bandwidth 10 and 20 MHz and for WCDMA.

1.3.2. Envelope Tracking

Envelope Tracking (ET) [5], [19]-[21] is an efficiency boosting technique for linear power amplifiers. The input to the linear amplifiers is a signal with a varying envelope. If the supply voltage is kept fixed, then a lot of power is wasted in heat as shown in Figure 10 below.

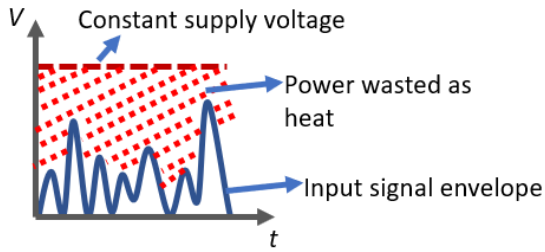

Figure 10 Power wasted in a linear amplifier with fixed supply voltage

Thus, in order to increase the efficiency of a linear amplifier, the supply voltage is varied according to the envelope of the input signal. ET can be of three types [20]:

- Wide band ET: the supply voltage tracks the instantaneous envelope of the modulated input signal.

- Average ET: the supply voltage tracks long term average of the modulated input signal.

- Step ET: the supply voltage is switched to different levels depending upon the envelope power of the modulated input signal.

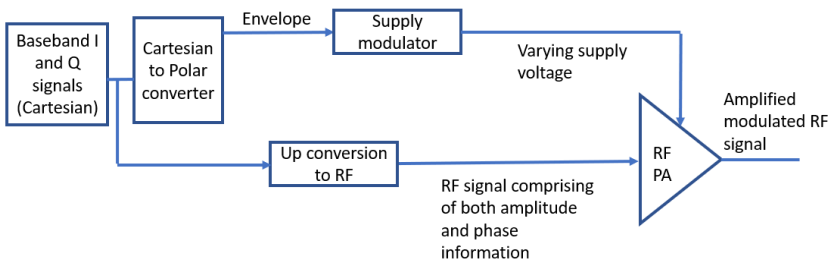

Figure 11 Block diagram demonstrating working principle of ET

Figure 11 shows the basic principle of the ET technique. In case of ET, the efficiency is lower than EER as a linear PA needs to be used. The accuracy requirement of dynamic supply is lower than EER as the input to PA contains both the amplitude and phase information. Less precision is required in time alignment between the supply voltage (envelope) and the RF input signal as an increase in EVM due to time misalignment is less sensitive in ET than in EER [20], [21].

1.3.3. Hybrid Envelope Elimination and Restoration

Hybrid EER [20], [21] is a combination of ET and EER techniques, enabling to utilize the advantages from both techniques. Figure 12 shows the basic principle of hybrid EER technique.

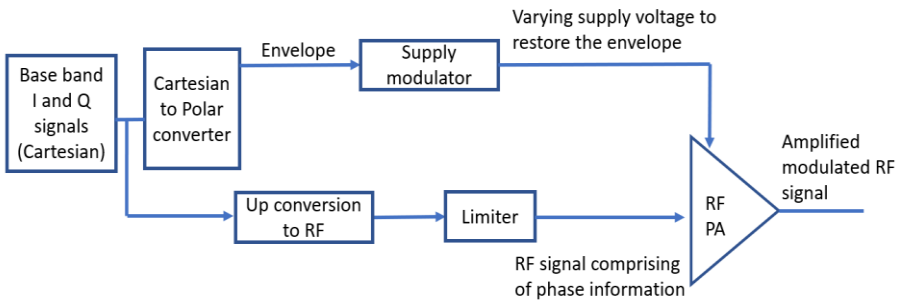

Figure 12 Block diagram demonstrating working principle of Hybrid EER

Hybrid EER uses a switch mode PA, thus achieving a higher efficiency than ET. [20] It also reduces the stringent requirement of time alignment between the phase and the envelope signal which is one of the major disadvantage of EER. The wide band requirement of EER is also eliminated as the phase signal is not used separately. A hybrid class E EER system is designed in [21] which achieves an efficiency of 36% at 19 dBm output power for WLAN 802.11g standard at 2.4 GHz.

2. System Requirements

2.1. General system requirements for the NB-IoT uplink channel

General system requirements for the NB-IoT uplink channel as specified in [23] are follows:

- The maximum channel bandwidth is 200 kHz.
- The minimum output power requirement is -40 dBm.
- The frequency bands that are supported are mentioned in Table 1.

Table 1 Frequency bands for uplink NB-IoT channel

NB-IoT operating frequency band	Frequency range (MHz)
1	1920-1980
3	1710-1785
5	824-849
8	880-915
12	699-716
13	777-787
17	704-716
19	830-845
20	832-862
26	814-849
28	703-748

- In this project, the PA is designed to operate in the encircled frequency band i.e. 1710 MHz-1980 MHz. The higher frequency band was chosen as it is more difficult to design an efficient PA for higher frequencies as compared to the lower frequencies as the switching losses and losses in components like inductor are higher at high frequencies. However, at higher frequencies, integrating the balun becomes easier as lower value of inductance is required thus, reducing the integration area.

- NB-IoT supports two power classes for User Equipment (UE): 20 dBm and 23 dBm. In this project, the PA is designed for the 20 dBm power class. By considering a peak to average power ratio (PAPR) of 6 dB (as in 6 tone case) and an additional 1 dB loss in switch etc. a peak power of 27 dBm is required. If 23 dBm power class is chosen then, a peak power of 30 dBm would be required which is quite difficult to obtain. Thus, the 23 dBm power class is chosen.

- Two subcarrier spacing options of 3.75 kHz and 15 kHz are available. The spacing option of 3.75 kHz helps to achieve deeper coverage at difficult locations where signal strength can be weak [24]

- The possible modulation schemes are π/2 BPSK, π/4 QPSK and QPSK. Figure 13 shows the different modulation schemes. π/2 BPSK is a robust modulation scheme than the higher modulation schemes as it has only two data points which makes the decision making at the receiver easier. Hence, it is generally used in the pilot signals for channel estimation. In QPSK modulation, when moving from the current symbol to the next symbol, any phase change (± 90° and 180°) is allowed as shown in Figure 13.b. But, in the case of π/4 QPSK, the phase change that is allowed when moving from the current symbol to the next symbol is limited only to ±45° and ±135° as shown in Figure 13.c. The phase change of 180° is not allowed which prevents zero crossing and thus, reducing the dynamic range for the amplifier.

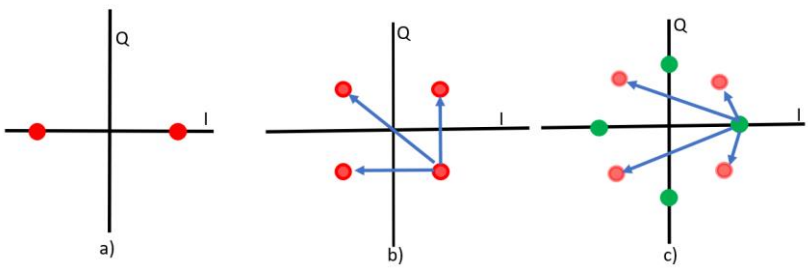

Figure 13 Constellation diagram for a) BPSK b) QPSK c) π/4 QPSK

- NB-IoT supports both single tone and multi tone transmission:
  - Single tone: π/2 BPSK, π/4 QPSK; 3.75 kHz and 15 kHz sub-carrier spacing
  - Multitone: QPSK; 15 kHz sub carrier spacing

- Tones 1, 3, 6, 12 can be used.

2.2. Error Vector Magnitude

Error Vector Magnitude (EVM) [5], [6] is an important measure of performance in the case of a PA. It is a measure of how well a PA can transmit the input information. When the transmitted signal is plotted in an IQ plane then, the received constellation points will differ from the transmitted data points. This may occur due to various factors like finite switching times of devices, quadrature error, phase rotation and non-linearity introduced by a PA etc. Figure 14 shows an error vector [5]. It is the vector between the ideal input constellation points and the ones that are transmitted. Magnitude of this error vector normalized to the signal gives the EVM. NB-IoT has an EVM limit of 17.5% [23].

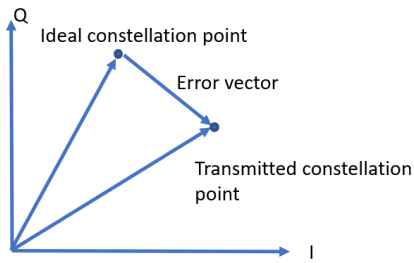

Figure 14 Error Vector for EVM

2.3. Spectral Mask

The out-of-band domain [23] includes all those frequencies that lie immediately outside the wanted or interested frequency range but excluding the spurious emission domain, where the out of band emissions generally dominate. Spurious emission domain [23] is that frequency range which falls beyond the out-of-band domain, where the spurious emissions generally dominate.

The spurious emission domain starts after ΔF_{OOB} = 1.7 MHz from the NB-IoT channel bandwidth. Figure 15 [23] demonstrates the out-of-band and spurious emission domain.

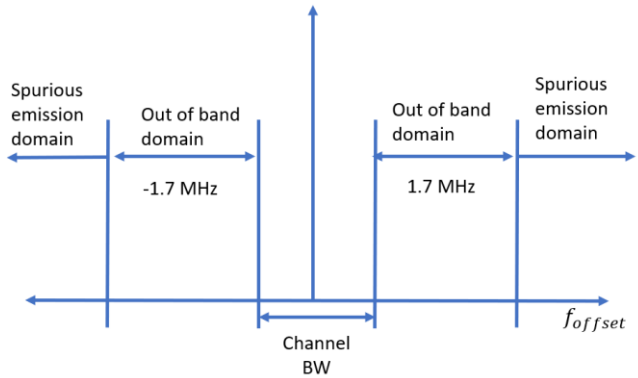

Figure 15 Out of band and spurious emission domain

According to [23], the out-of-band emission limits are as mentioned in Table 2:

Table 2 Out of band emission limits

ΔF_{OOB} (kHz)	Emission Limit (dBm)	Measurement Bandwidth (kHz)
0	26	30
100	-5	30
150	-8	30
300	-29	30
500-1700	-35	30

2.4. Adjacent Channel Power Ratio

Non-linearity in a power amplifier causes power to leak from the intended channel to the adjacent channel. Adjacent channel power ratio (ACPR) [5], [6], [25] is the ratio of the power in the adjacent channel bandwidth at a given frequency offset to the power in the channel of interest. As mentioned in [23], the ACPR requirements for NB-IoT are mentioned in Table 3:

Table 3 ACPR requirement for NB-IoT

Victim systems	GSM	UTRA
ACPR	20 dB	37 dB
Adjacent channel measurement bandwidth	180 kHz	3.84 MHz
Measurement filter	Rectangular	RRC- filter, alpha =0.22
Adjacent channel center frequency offset from the main channel edge	200 kHz	2.5 MHz

2.5. Efficiency

The efficiency is an important measure for a power amplifier. It is significantly important for the power amplifiers being used in NB-IoT applications to have a high efficiency as NB-IoT applications aim at a battery life of more than 10 years.

The drain efficiency [5] is the ratio of RF output power from the PA to the total dc input power.

$$Drain\ efficiency = \frac{P_{output}}{P_{dc}} \quad (7)$$

Power Added Efficiency (PAE) [5], [6] is the ratio of difference between the RF output power and RF input power to the total dc input power

$$PAE = \frac{P_{output} - P_{input}}{P_{dc}} \quad (8)$$

3. Nonlinear amplifier design

3.1. PA architecture

In this project, a power amplifier is designed for both the EER and the hybrid EER architectures. They will be analyzed to determine the more suitable architecture for NB-IoT applications.

3.2. Amplifier class and topology

Among the non-linear amplifier class, class D and class E amplifier are taken into consideration. The class F amplifier is not considered due to its design complexity. The architecture, advantages, disadvantages etc. of class D and class E amplifier are discussed in section 1.2.2. Comparison between class D and class E amplifier is represented in Table 4.

Table 4 Comparison between class D and class E PA

No.	Class D amplifier	Class E amplifier
1	Theoretical efficiency is 100%	Theoretical efficiency is 100%
2	Zero voltage switching can be achieved in inverse class D amplifier.	The switch voltage as well as its first derivative are zero
3	Lesser passive components- lesser area, lesser cost, more reliability	Multiple passive components required
4	Inductor of the resonant tank circuit absorbed into balun	Voltage swing across the devices can be very large (can go up to 3.6 times V_{dd})

Thus, from Table 4, it is observed that a class D amplifier is more beneficial than a class E amplifier and as per discussion in section 1.2.2.1, an inverse class D topology is chosen over the traditional class D amplifier.

3.3. Inverse class D amplifier design calculations

The theoretical equations and background for designing an inverse class D amplifier are reported in [14]. The designing of an inverse class D amplifier involves calculation of various key parameters like the device widths, selecting a proper inductor and capacitor etc. This section describes calculation of these various parameters.

3.3.1. Device Width

The device width is one of the most important parameters in designing the PA. The switch resistance of the device (R_{on}) [14] is given as,

$$R_{on} = \frac{1}{(\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T))} \quad (9)$$

Where,

μ_n and C_{ox} : process parameters

W : width of the device

L: length of the device

V_{GS}: gate-source voltage of device

V_T: threshold voltage

R_{on} is one of the key factors that cause losses in a power amplifier. R_{on} is inversely proportional to the device width as can be seen in (9). Thus, by increasing width of the device, R_{on} can be decreased but this causes increase in the parasitic drain capacitance C_s. Increase in C_s causes distortion in the drain current waveforms which causes more overlap between the drain voltage and drain current which in turn reduces efficiency of the PA [14]. Thus, there is a tradeoff between reducing losses due to R_{on} and C_s. For an inverse class D amplifier at 2.4 GHz, designed in 65 nm technology, it is observed that the efficiency remains almost constant for device widths of 2 mm - 3 mm [14]. Hence as a starting point, a device width of 2.5 mm is chosen which would be refined later.

3.3.2. L and C of the resonant tank circuit

Figure 16 represents the basic circuit diagram of a differential inverse class D amplifier where, V_{DD} is the supply voltage, L and C form the resonant circuit and R_l is the load resistor.

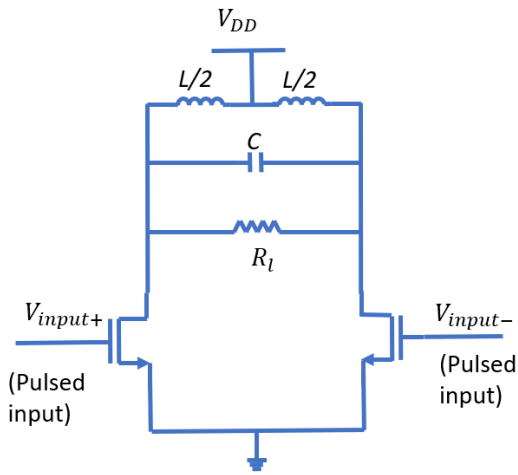

Figure 16 Inverse class D PA [14]

From [14], inductor of the resonant tank circuit (L) is given as:

$$L/2 = \frac{1}{(2.3*\omega_o)^2 * C_s} \quad (10)$$

And,

$$L = \frac{1}{\omega_o{}^2 * (C + \frac{C_s}{2})} \quad (11)$$

C_s is dominated when the device is in the off- state. Thus, by considering the imaginary part of drain current at a given drain voltage and at 1.845 GHz, C_s is calculated to be 1.167 pF.

By substituting the calculated value of C_s in (10)

$L/2$= 1.205 nH

Similarly, by substituting the value of L and C_s in (11),

C = 2.503 pF

Cascode devices are added in order to increase the amount of supply voltage that the device can handle without breaking off and to reduce coupling between the input and the output.

The basic amplifier and the drain current (I_d), drain voltage (V_d) curves are shown in the Figure 17 and Figure 18 respectively.

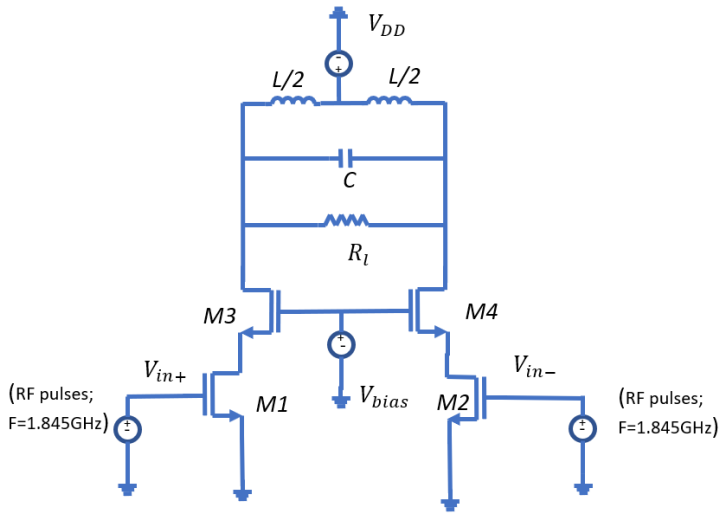

Figure 17 The schematic of simple Inverse class D PA

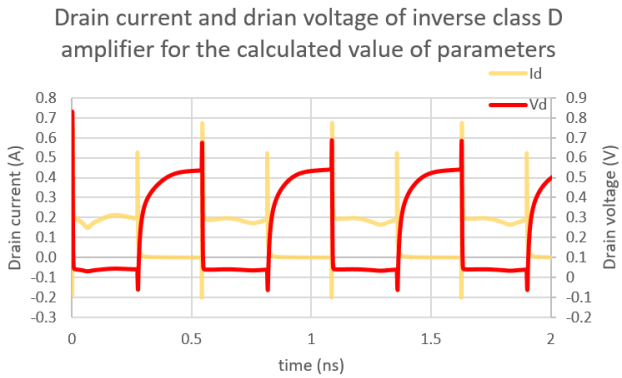

Figure 18 Drain current and drain voltage for the calculated values of inductor, capacitor and device width.

The I_d curve observed in the Figure 18, has high peaks at the beginning and at the end of each pulse. This is because, the input pulses are perfectly square waves with zero as rise and fall time and the width of devices is high, which causes charge and discharge of a high amount of current within relatively very short span of time causing the peaks. Since such high peaks can damage the circuits, they need to be investigated. The investigation on optimizing the PA and reducing the peaks is reported in the following section.

3.4. Optimizing the PA

1. Bias voltage of cascode device

Increasing the bias voltage, increases the drain current that flows through the device and thus, increasing the achievable output power. By varying the bias voltage of cascode device from 1 to 2.5 V, it is observed that a peak efficiency of 79% can be reached at a peak power of 29.6 dBm for bias voltage of 1.8 V. This can be observed in Figure 19. The aim is to have an output power greater than 27 dBm because losses in the balun are not taken into consideration at this point in the simulations. By checking the dc operating points, it is verified that the potential differences for the cascode as well as the main devices are below the breakdown voltages.

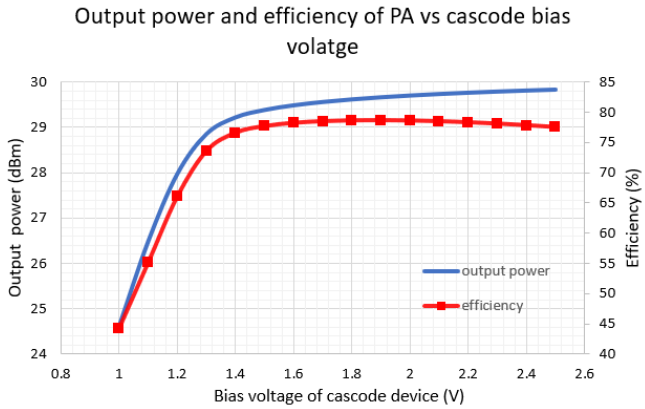

Figure 19 Output power and efficiency of the PA vs bias voltage of the cascode devices

2. Width of the devices

As discussed in the section 3.3.1, increasing the device width reduces the on-resistance of the device but at the same time increases the drain-source capacitance. The output power increases with increasing device width as more current can flow through the device. Hence, determining optimum device width for our required specifications is important.

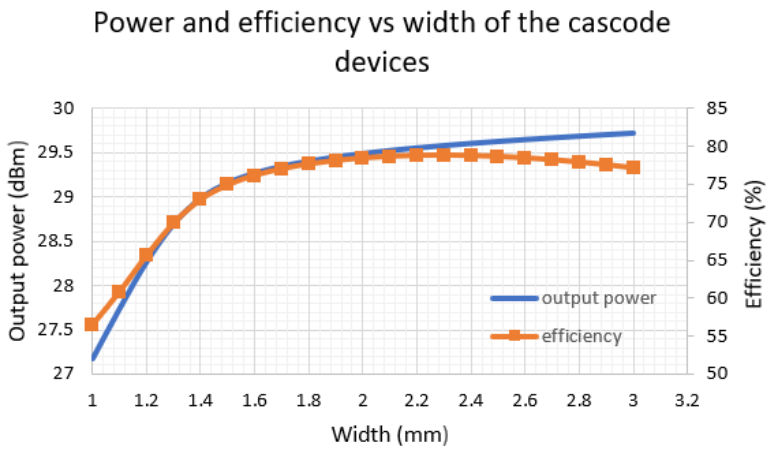

Figure 20 Power and efficiency of the PA vs width of the devices

Figure 20 shows a plot of efficiency and power vs width of cascode device. The efficiency is almost constant after 1.8 mm. It is observed that a peak efficiency of 78% and a power more than 29 dBm can be obtained at 1.8 mm device width. To account for losses in the balun, power of more than 27 dBm is needed.

3. Inductor and Capacitor

Changing the width of devices changes the drain-source capacitance. This alters the resonance frequency. As width of the devices is decreased, the parasitic capacitance associated with the device also decreases. Thus, the capacitor of resonant tank circuit needs to be increased to keep the resonance at 1.84 GHz. The capacitance value is changed to 2.7 pF while the inductor value is kept unchanged at 1.2 nH. Figure 21 shows the resonance curve with peak after changing the capacitance value.

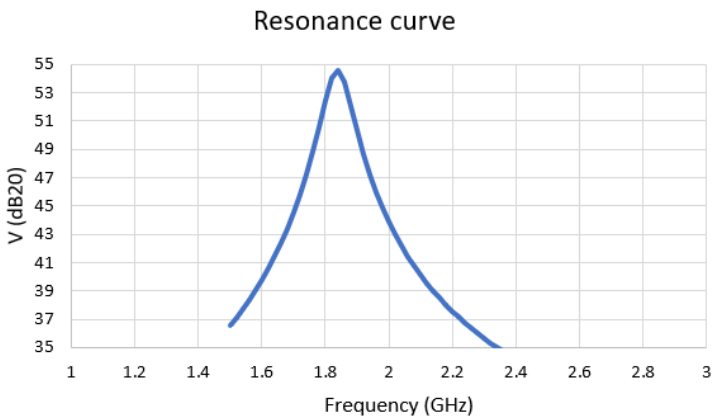

Figure 21 Resonance curve after changing the capacitance value.

4. Designing a class A amplifier

The amplifier is designed for 20 dBm power class. By considering a PAPR of 6 dB and an additional 1 dB loss in switch etc. the amplifier needs to be designed to have a compression point of 27 dBm. The drain current required to provide 27 dBm power is calculated as:

$$I^2R = 27\ dBm \tag{12}$$

= 501.2 mW

= 0.501 W

I^2 = 0.01

$I_{rms} = 0.1\ A$

$I_{peak} = 0.142\ A$

To achieve the required amount of drain current, width of the devices and the basing voltages of the driving devices need to be set optimally. Increasing width of the device increases the drain current but also increases the parasitic capacitances associated with the device leading to reduction in the transition frequency. If the biasing voltage is not set at an appropriate level, it will reduce the voltage headroom and legroom of the amplifier. Figure 22 and Figure 23 shows the drain current, the drain voltage and the input voltage at a few dB below the compression point. As it can be observed, the drain current starts to compress first.

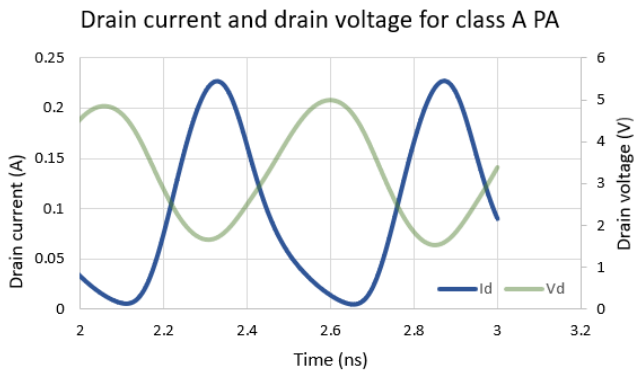

Figure 22 Drain current and drain voltage of cascode device

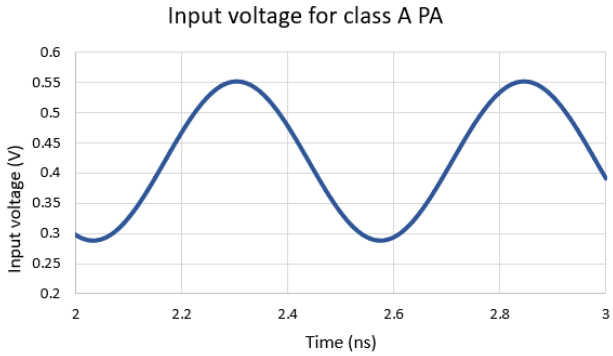

Figure 23 Input voltage signal

Figure 24 shows the compression curve of the designed class A power amplifier. As it can be observed from the figure, a compression point at 26 dBm (output power) is achieved. Figure 25 shows power added efficiency and power gain. The PA has 44% efficiency and 29 dB power gain at the compression point.

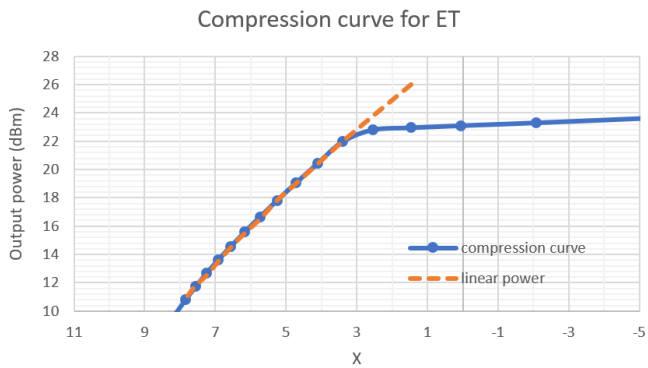

Figure 24 Compression curve for class A PA

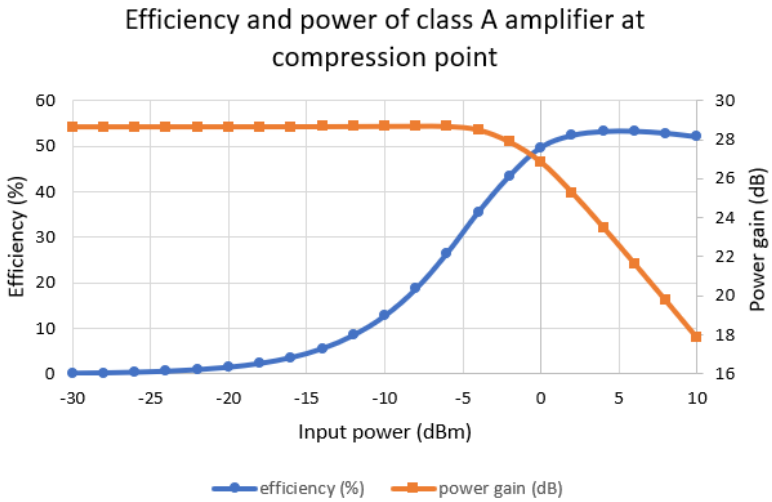

Figure 25 Efficiency and power gain for class A PA at compression point

The inductance and capacitance of resonance tank circuit is adjusted so that a resonance is obtained and 1.845 GHz and S22 of at least -6 dB is obtained at the resonance frequency. Figure 26 shows the S22 curve for class A amplifier.

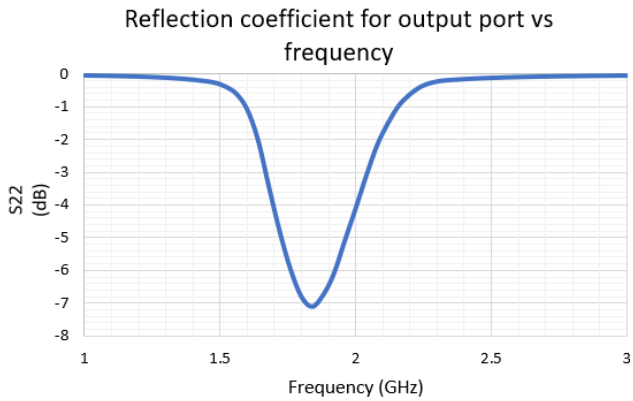

Figure 26 Reflection coefficient of the output port for class A amplifier

5. Balun

The balun is designed as an ideal block to have a loss of 1.3 dB at 1.845 GHz [13]. Inductors of the tank circuit are absorbed into the balun. Apart from converting the differential input to a single ended output, it also functions as a matching network. Figure 27 shows a model of the transformer. Here, *R* is the load resistor, *r_dc* represents the resistance of the coil (dc resistance) and *r_rf* represents the resistive component of the inductor that plays an important role at higher frequencies, *L* is the inductor of the balun and *mind* represents the mutual inductance. Figure 28 shows the schematic and symbol of the transformer used in the simulations.

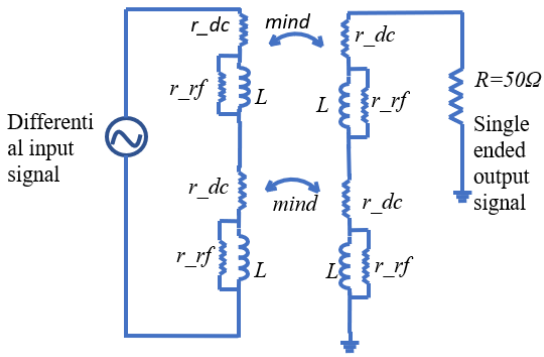

Figure 27 Schematic of the transformer used for determining value of the mutual inductance for the required loss

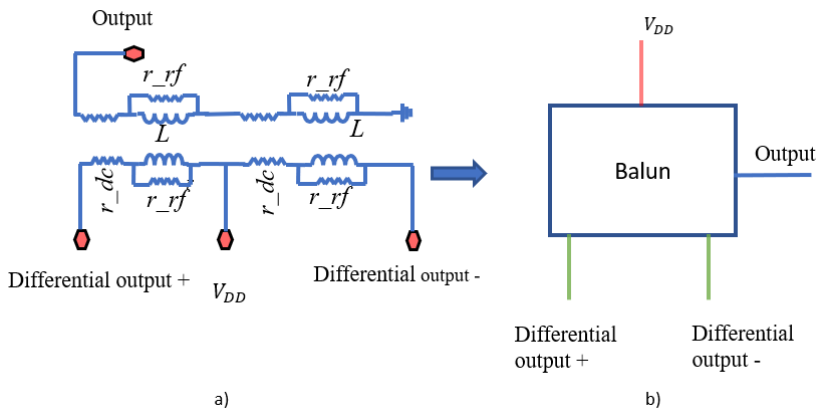

Figure 28 a) The schematic of transformer **b)** symbol used for transformer in further simulations

Value of the mutual inductance is varied for an inductance of 1.2 nH (for inverse class D amplifier) and for an inductance of 200 pH (for class A amplifier) at the desired frequency of 1.84 GHz to obtain the plot shown in Figure 29 and Figure 30.

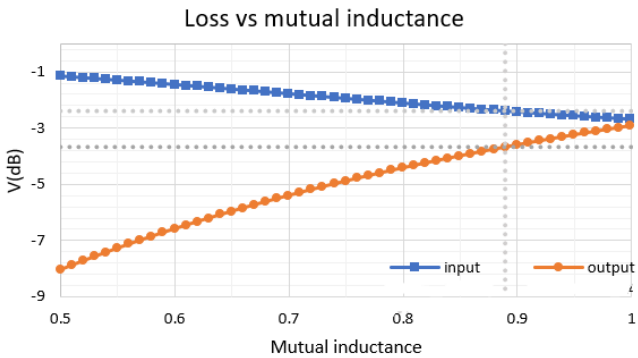

Figure 29 Loss vs mutual inductance for balun of inverse class D amplifier

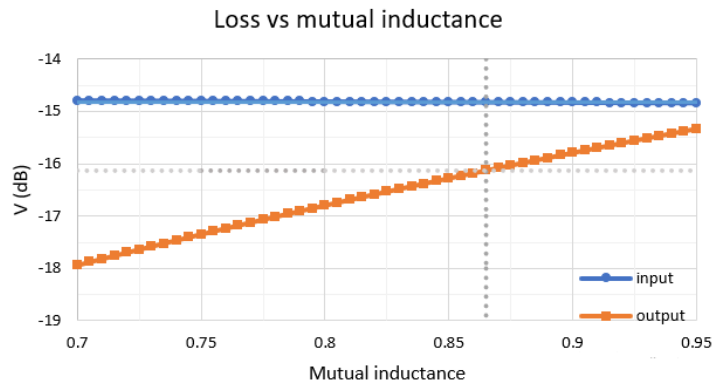

Figure 30 Loss vs mutual inductance for balun of class A amplifier

It can be observed that a loss of 1.3 dB is achieved at a mutual inductance of 0.887 for the balun for inverse class D amplifier whereas a mutual inductance of 0.865 is required for the balun for class A amplifier. Achieving such a high mutual inductance is difficult. The efficient designing of transformer is extremely important because, reduction in the mutual inductance leads to increase in losses caused by the transformer and thus reduces the efficiency of the PA.

Thus, the design of the transformer is critical for achieving a high efficiency. A mutual inductance of 0.9 (approx.) can be achieved with a stacked layout model of the transformer [27]. In the stacked transformer layout, the primary and the secondary of a transformer are implemented on different metal layers. These metal layers need to be perfectly aligned for the best results. It uses both lateral and vertical magnetic fields which enhances the mutual inductance. It also enables to achieve the best area efficiency. However, the major disadvantage of this configuration is a high capacitance and thus a lower self-resonating frequency [26]. This capacitance may be included as a part of the resonant tank circuit but, this requires further analysis as the resonant tank circuit also needs to include the drain-source capacitance of the device and still be resonant at the required frequency. The capacitance can be reduced up to 50-70% by increasing the thickness of the oxide between the spirals, although it reduces the coupling coefficient but the reduction is less than 5% [26].

The value of the mutual inductance is kept constant and the resonant frequency is varied to obtain the plots shown in Figure 31 and Figure 32. As it can be observed from these figures, the loss remains almost constant over a frequency range of 1.5 GHz-3 GHz.

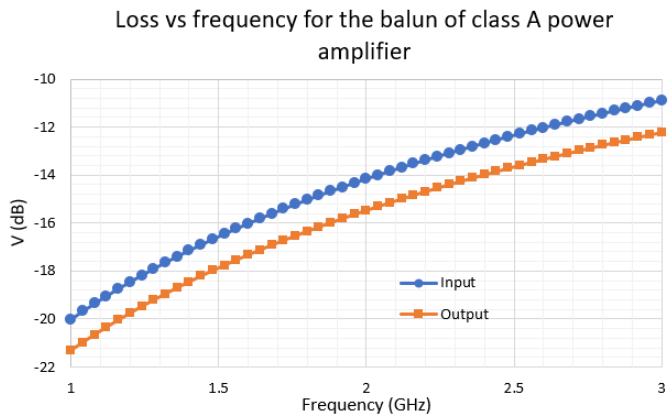

Figure 31 Loss vs frequency for the balun of class A amplifier

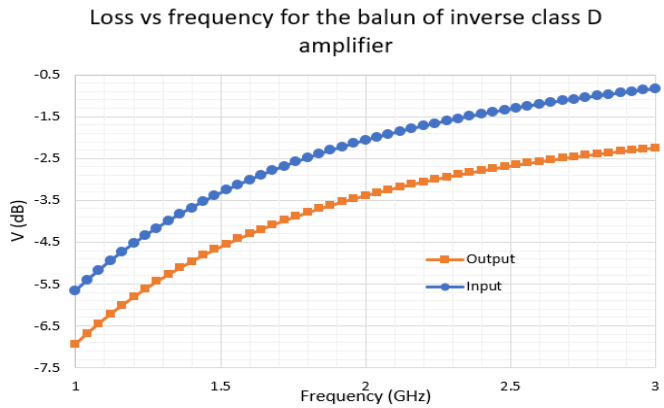

Figure 32 Loss vs frequency for the balun of inverse class D amplifier

6. Driving inverter stages

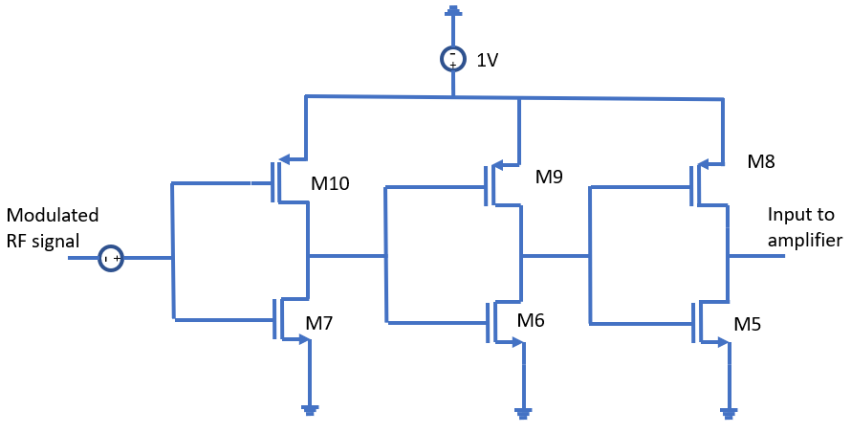

Figure 33 The inverter chain driving Hybrid EER PA

In order to drive a nonlinear PA, a pulsed signal is required as the input to the PA. To achieve this, a chain of inverters is used. Figure 33 shows a chain of inverters. The inverters are biased such that the differential input signals cut each other at mid-point. This helps to deliver a proper differential input to the PA. It is also observed that the efficiency is higher when the inverters are biased such that the differential input signals cut each other at mid-point. This is achieved by having the biasing voltage at approximately half of the supply voltage of inverters. This can be observed in Figure 34.

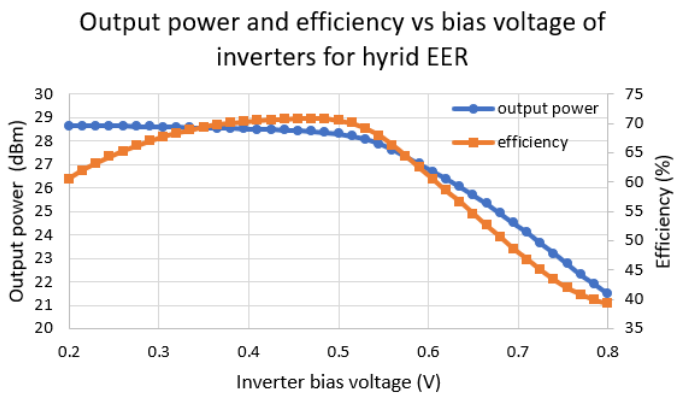

Figure 34 Output power and efficiency of hybrid EER PA vs the bias voltage of inverter stages

The hybrid EER PA requires more inverter stages than EER PA. This is because in case of the hybrid EER, the upconverted cartesian signal forms input to the PA. Thus, when the amplitude of the input I and Q signals is reduced (input power control), the upconverted input signal has a smaller amplitude. When this input signal is passed through the inverter stage, input to the PA is no longer a proper pulsed signal. Hence, more inverter stages were added so that there is sufficient voltage to drive the PA. Whereas in case of the EER PA, the phase signal forms input to the PA. Thus, varying the amplitude of input I and Q signals does not have an effect on amplitude of the phase signal. The number of inverter stages used for hybrid EER and EER is three and two respectively. No inverters are required for the class A power amplifier since it is a linear PA.

7. Supply Modulator

The supply modulator forms an essential part of a nonlinear amplifier system. In the case of a nonlinear amplifier system, the supply modulator is used to re-establish the envelope at the output in order to produce the modulated output signal thus maintaining sufficient linearity. It is also called drain modulation [27]. Supply modulators are also used in case of the linear amplifiers. In this case, their main objective is not to re-establish the envelope but, to vary the supply voltage according to the envelope of the input signal. This reduces power loss thus, increasing efficiency. There are two types of supply modulators: 1) Linear supply modulator and 2) Switch mode supply modulators.

7.1. Linear Regulator

Linear regulators [28], [29] are used to provide the required lower voltage to a given load from a fixed higher value voltage source. A basic linear regulator uses a variable resistor and a feedback loop that controls the value of this variable resistor. The linear resistor is implemented by driving a MOSFET in its linear region. Linear regulators have various advantages [28] like simple design, low voltage ripples as the device is not used in switch mode. The major drawback of linear regulators is the low efficiency. Since, linear regulator basically uses a variable resistor, its efficiency can be written as [28]:

$$\eta = \frac{P_{output}}{P_{input}+P_{loss}} = \frac{V_o I_o}{V_o I_o+(V_i-V_o)I_o} = \frac{V_o}{V_i} \tag{13}$$

Thus, if the difference between the required output voltage and the available input voltage is higher, the efficiency will be very low. However, if this difference is very low, then a high efficiency can be achieved. But, another aspect to be taken into consideration is that since here the MOSFET needs to operate in a linear mode, a certain voltage drop is required for it to function in linear mode. Another limitation of the linear regulator is that it can only be used to as a step-down converter. If a higher output voltage than the available input voltage is required, then a linear regulator cannot be used.

7.2. Switch Mode Power Supply

In a switch mode power supply (SMPS), the device acts as a switch instead of a resistor thus reducing the power loss and increasing the efficiency. SMPS can work as a step-up or a step-down converter.

Figure 35 [30] shows the operating principle of a switch mode power supply. The envelope and triangular pulses form input to the comparator. The output from the comparator is a pulse width modulated signal which is fed to the inverters. The output from the inverter is passed through a low pass filter before feeding it as a supply voltage of the PA.

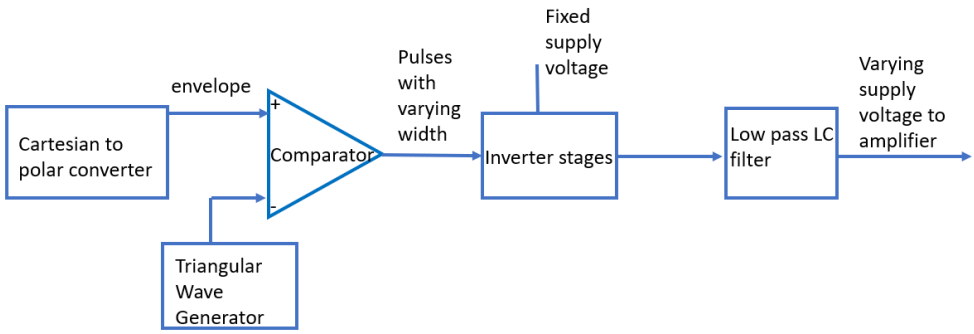

Figure 35 Block diagram demonstrating working principle of a supply modulator

A major disadvantage of this technique is that the transmit spectrum may contain a number of unwanted frequencies as shown in Figure 36 where ω_m represents the modulation frequency (the wanted signal) and ω_s is the switching frequency of the devices. The unwanted spurious frequencies are formed by the combination of switching frequency and the modulation frequency for example: $\omega_m + \omega_s$, $\omega_m - \omega_s$, $\omega_s - 2\omega_m$, $\omega_s + 2\omega_m$ etc.

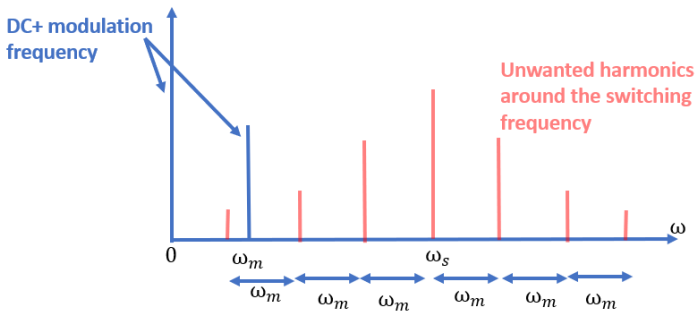

Figure 36 The wanted and spurious frequencies [30]

Thus, a low pass filter needs to be designed so that it filters out all the unwanted frequencies before the signal that goes to the PA. Another aspect that needs to be

taken into consideration is the switching loss. Higher switching frequency causes higher switching loss but, it relaxes the requirements on the filter design as the filter can have a higher cut-off frequency. Having a higher cut off frequency also reduces the delay induced by the filter since, for higher cut-off frequency, smaller inductors and capacitors are sufficient which introduce a lower delay. Thus, balancing between the filter design, switching losses and delay forms a critical trade off in the case of SMPS.

However, in the case of NB-IoT system, the modulation frequency is only 180 kHz. Thus, a lower switching frequency can be selected and the switching losses can be reduced.

In addition to the capacitive switching loss of the supply modulator, there is another important source of loss which is due to ripple current in the inductor of the filter.

From [27],

$$I_{ripple} = \frac{V_{dd} * D(1-D)}{F_{switching} * L} \tag{14}$$

$F_{switching}$: Switching frequency or frequency if triangular wave

D: duty cycle

The product of the mean squared value of this current and the effective series resistance gives conduction loss [27]. The conduction loss decreases with reduction in ripple current.

Thus, increasing the switching frequency increases the switching losses but at the same time decreases losses due to the ripple current. As mentioned earlier, increasing the switching frequency, relaxes the requirement on filter design and reduces the delay caused. Thus, there exists a tradeoff which needs to be taken into consideration in designing the supply modulator.

The schematic of the supply modulator is shown in Figure 37. The amplitude of the triangular signal is adjusted such that it is slightly higher than the strongest envelope signal so that it can cover the exact shape of the envelope signal when it is the strongest and also when it is the weakest. The size of the filter components and the inverters are optimized through a number of iterations to obtain the best possible efficiency at reasonable filter and inverter dimensions. The efficiency of supply modulator for two different switching frequencies is plotted in Figure 38.

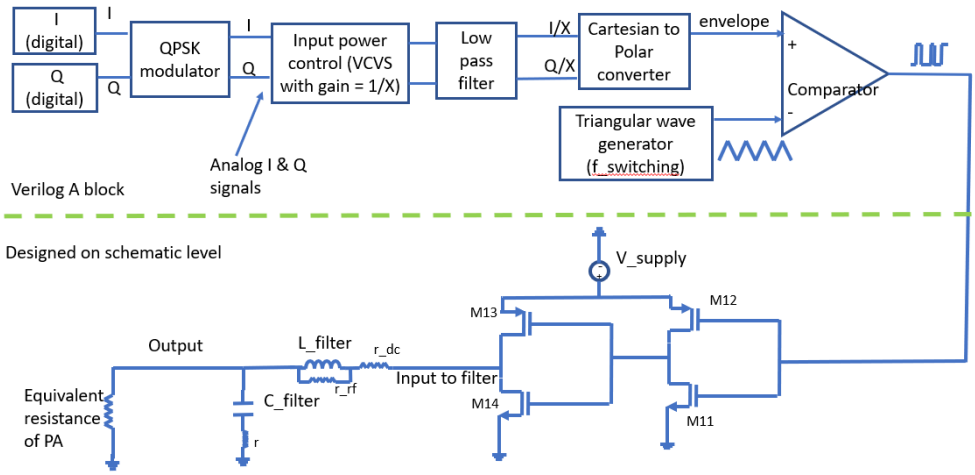

Figure 37 Schematic of the Supply Modulator

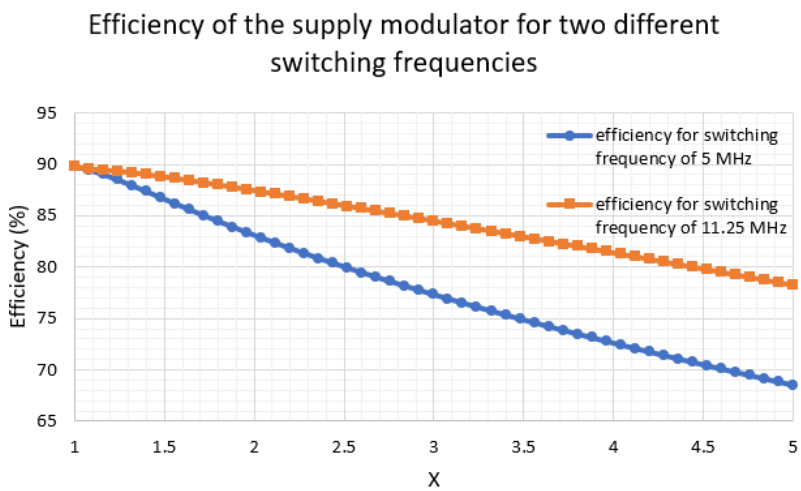

Figure 38 Efficiency of the supply modulator for switching frequency of 5 MHz and 11.25 MHz (where X is the parameter to control the input power)

In Figure 38, the x axis (X) represents a divider for the amplitude of input I and Q signals. Higher the value of X, lower is the strength of the input signal and lower is the strength of the input envelope signal. It can be observed that the switching frequency of 11.25 MHz provides overall higher efficiency. Here, the switching losses are compensated by the lower losses in the filter. However, further increase in the switching frequency causes decrease in efficiency as the switching losses begin to dominate.

The final values of various components are as follows:

-Inductor and capacitor of the filter: 300 nH and 400 nF

- Width of the nMOS in main inverter: 1600 µm

-Width of the nMOS in driving inverter: 500 µm

-Switching frequency: 11.25 MHz

The output from the supply modulator and the envelope signal at input of the supply modulator is shown in Figure 39. It can be observed that the output follows the shape of the envelope but is slightly delayed. This delay is due to large inductor and capacitor used in the filter.

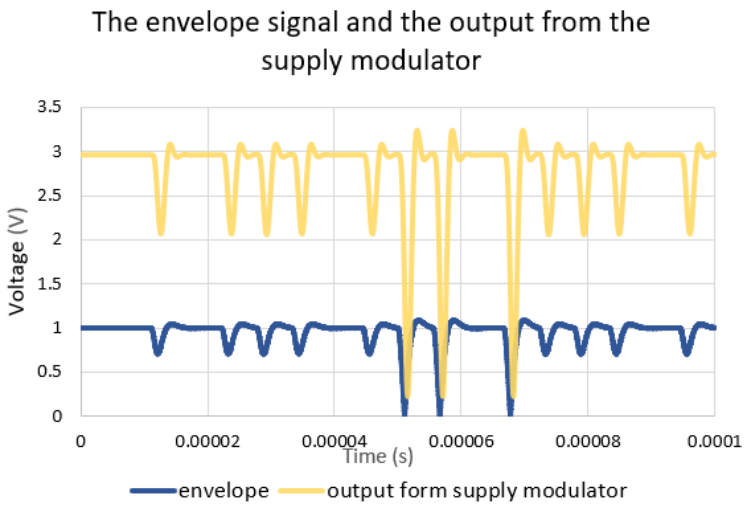

Figure 39 Envelope of the input signal and output from the supply modulator

8. Results

This chapter discusses different results obtained through simulations for ET, EER and hybrid EER amplifiers. Figure 40, Figure 41 and Figure 42 represent the architectures for ET, EER and hybrid EER respectively. The digital I and Q signals are fed to the QPSK modulator which forms a QPSK signal with a symbol period of 5.56 µs. The signal then goes to a low pass filter. The I and Q signal are then fed to the IQ modulator or a phase modulator, depending on the architecture, and to the supply modulator. The IQ modulator performs an up conversion of the baseband signal to 1.845 GHz RF signal. The input power is varied by dividing the amplitude of I and Q signals obtained after the QPSK modulator by a variable (referred as X in the report). The efficiency (for all the three cases) is calculated as ratio of output power to total DC power.

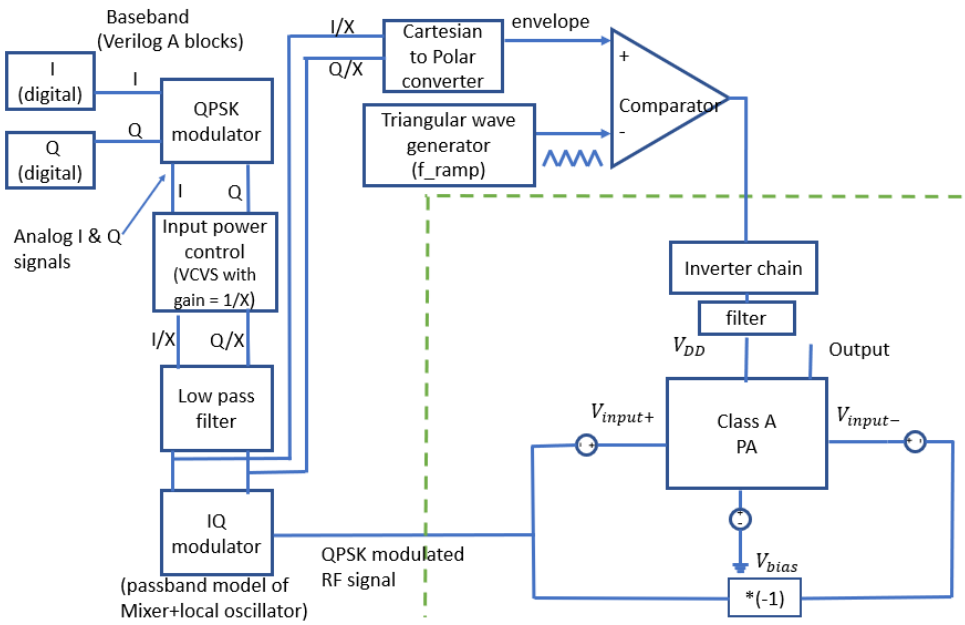

Figure 40 Block diagram of ET

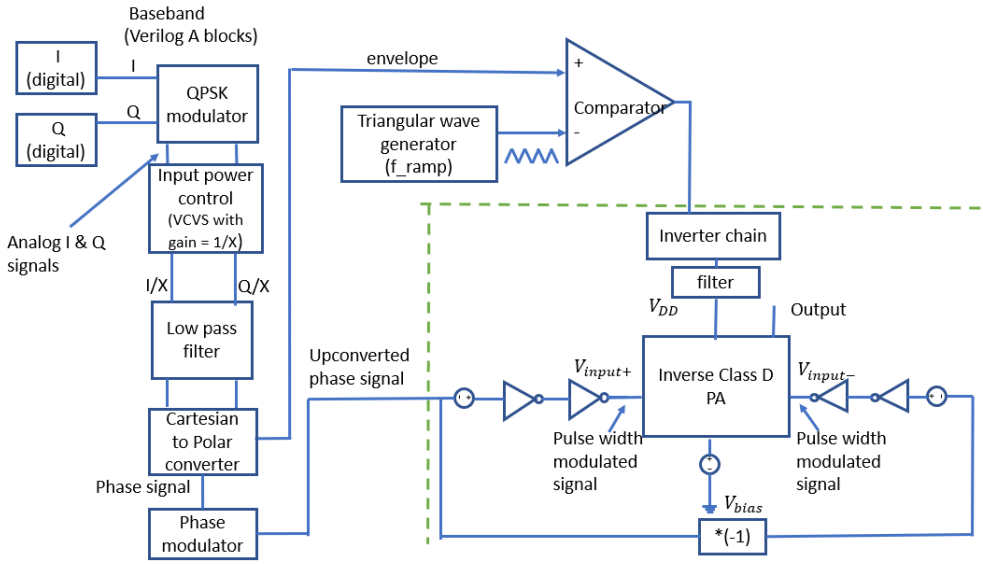

Figure 41 Block diagram of EER

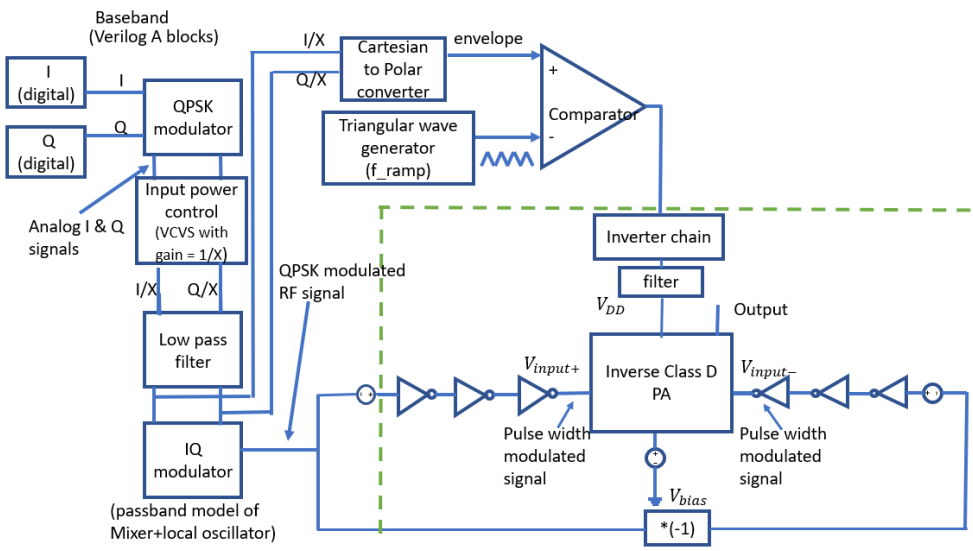

Figure 42 Block diagram of hybrid EER

As mentioned in the earlier sections, ET architecture is used for linear PAs while EER and hybrid EER architectures are used for nonlinear PAs. In this project, ET architecture is implemented with a class A amplifier. As ET uses a linear PA, QPSK

modulated RF signal directly forms an input to the amplifier. Thus, no inverter chain is required in case of the ET.

The inverse class D amplifier is used in the case of EER and hybrid EER architectures. The main difference between hybrid EER and EER is the way input is fed to the PA. In the case of EER, the upconverted phase signal forms an input to the PA while in the case of hybrid EER, the modulated RF signal (phase + amplitude) forms an input to the PA after passing through the inverter stages.

8.1. Drain current and Drain voltage

The drain current and drain voltage curves for EER and hybrid EER are shown in Figure 43 and Figure 44. The characteristics of the drain current and the drain voltage mainly depend on the type of PA rather than the efficiency boosting technique that is being used. As EER and hybrid EER both use inverse class D amplifier, their drain current and drain voltage waveforms are similar. The peak that can be observed in the beginning of each drain current pulse is due to a sudden flow of current when the device conducts. Ideally, there should be zero overlapping between the drain current and the drain voltage of EER and hybrid EER PAs, as they use the inverse class D amplifier. But, it can be observed in Figure 45 that there is some overlapping. This is because the devices are not ideal. They have nonzero switching time and have various parasitic capacitances associated with them. This overlapping between the drain current and drain voltage causes unwanted power loss which leads to decrease in the efficiency.

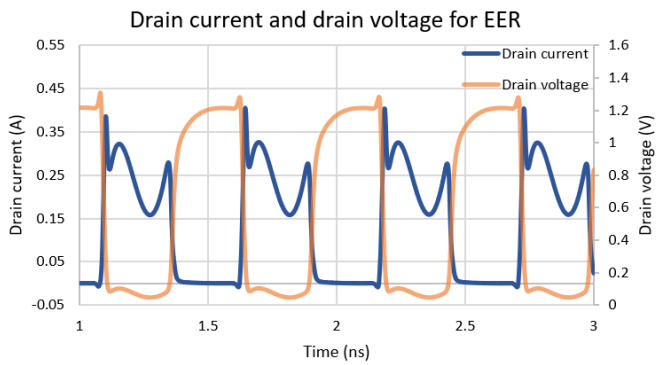

Figure 43 Drain current and drain voltage for EER

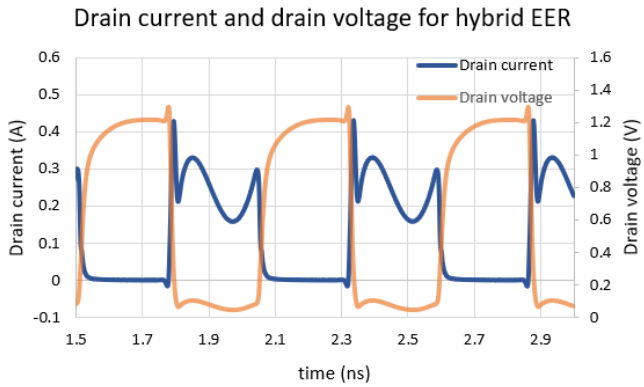

Figure 44 Drain current and drain voltage for hybrid EER

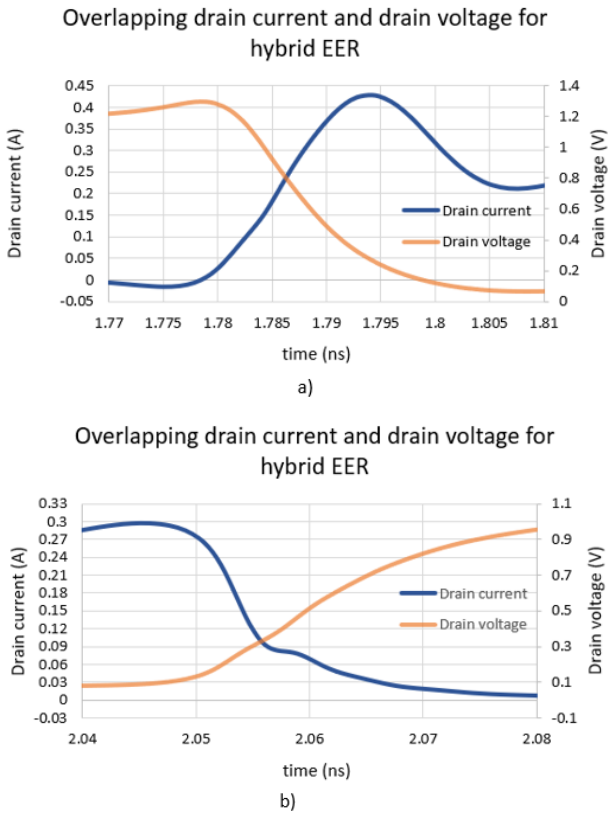

Figure 45 Overlapping between the drain current and the drain voltage for hybrid EER at the a) beginning and b) at the end of the pulse

As ET uses a class A amplifier (conduction angle of 2π), it can be observed that there is a significant overlapping between the drain current and the drain voltage. This is a major cause of low efficiency in case of the ET PA. The drain current and the drain voltage curves for ET represented in Figure 46 are taken when the drain current and the drain voltage are just starting to compress.

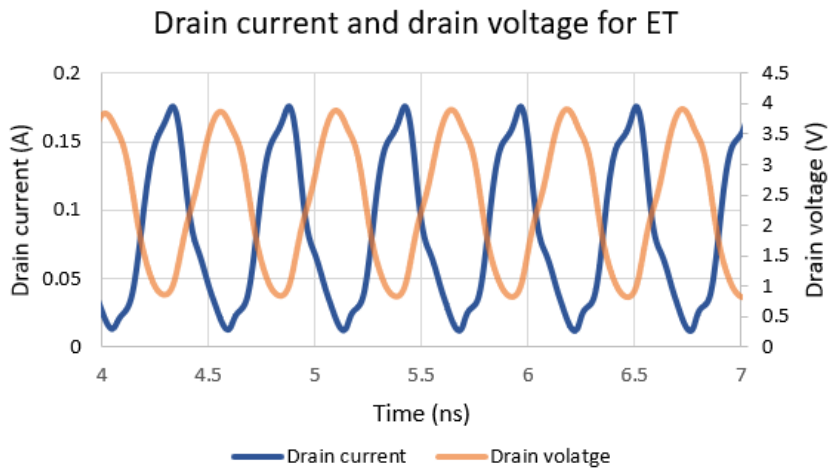

Figure 46 Drain current and drain voltage for ET

8.2. Power and efficiency

8.2.1. Power and efficiency for ET

The compression curve for ET amplifier is shown in Figure 47. The 1 dB compression point obtained is 22.8 dBm (output power). The compression point is lower as compared to standalone class A amplifier because of the losses introduced by the supply modulator.

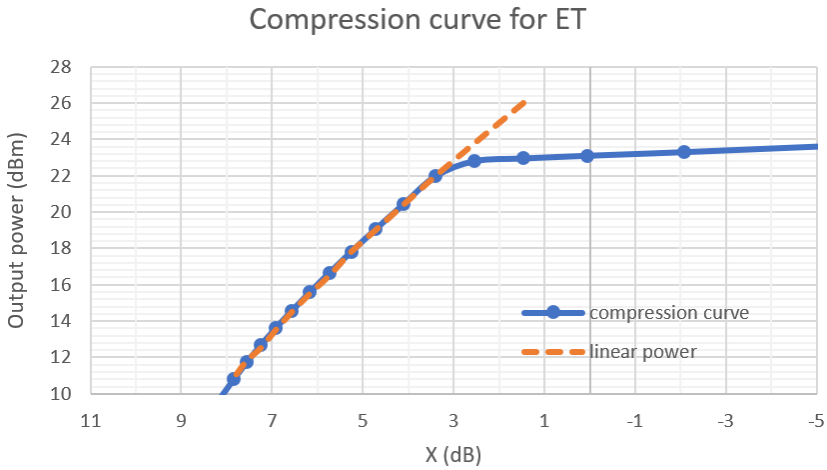

Figure 47 Compression curve for ET amplifier (where X is the parameter for input gain control)

The power and efficiency curves for ET are shown in Figure 48 and Figure 49. A peak efficiency of 37% can be reached at a peak output power of 24 dBm. As it can be observed in Figure 49, there is almost a linear increase in the efficiency with increase in the output power till the saturation state is reached. In addition to having a lower efficiency as compared to EER and hybrid EER, steep slope of the efficiency vs output power curve is another disadvantage of the ET architecture. It can also be observed that there is a steep reduction in efficiency after the compression point. This reduction in efficiency is caused because, the output power remains constant due to saturation while the input power increases, causing the efficiency to decrease.

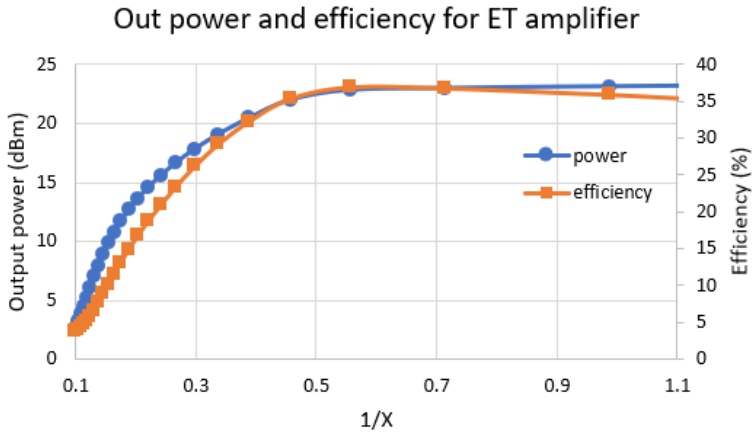

Figure 48 Output power and efficiency for ET amplifier vs 1/X (parameter for input gain control)

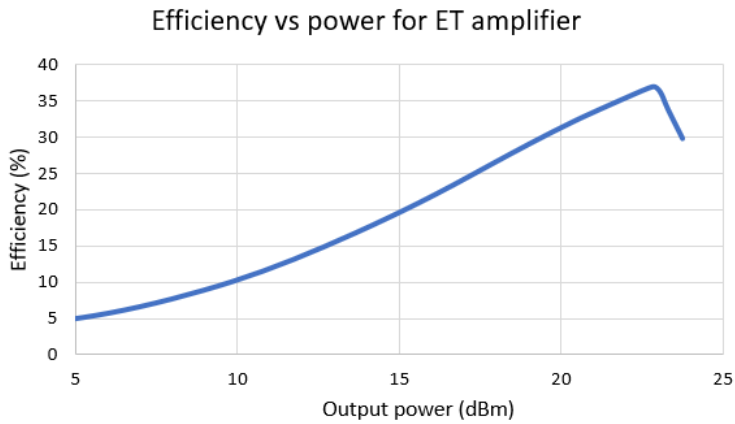

Figure 49 Efficiency vs output power for ET amplifier.

In case of the linear class A amplifier, the supply modulator is not required to re-establish the envelope as in the case of nonlinear amplifiers. As discussed in section 1.3.2, the supply modulator, in the case of ET performs the function of efficiency boosting by varying the supply voltage according to the input envelope in order to reduce power wastage. Thus, as observed in Figure 50, the overall efficiency obtained in ET is higher than for a standalone class A amplifier with a fixed supply.

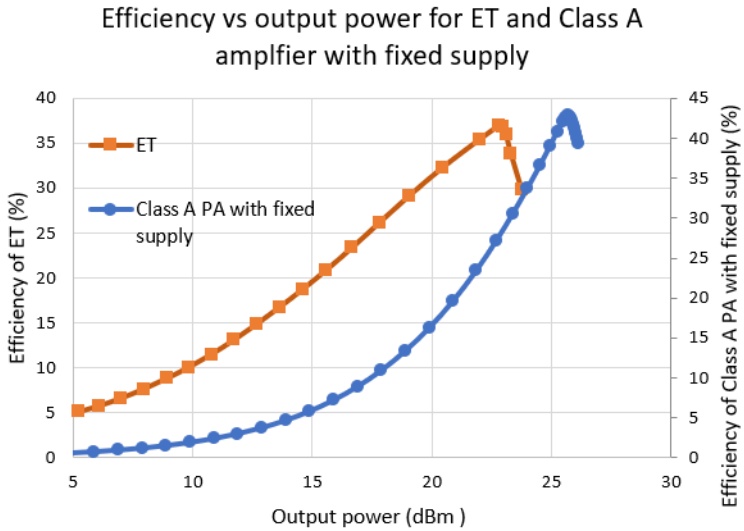

Figure 50 Comparison of efficiency vs output power for ET and a class A amplifier with fixed supply.

Around 15% increase in the efficiency is achieved with ET architecture as compared to the class A amplifier with a fixed supply for the output power in a range of 15 dBm to 22 dBm (approx.) However, the peak achievable output power in ET is reduced to 24 dBm due to the losses associated with the supply modulator that is used in the ET architecture.

8.2.2. Power and efficiency for EER

The power and efficiency curves for EER PA are shown in Figure 51. The PA can achieve a peak power of 28 dBm with a peak efficiency of 67%. EER enables the use of high efficiency nonlinear amplifiers even for the modulated input signals, which helps to achieve a high overall efficiency and thus increase the battery life of the devices. Having a long battery life (10+ years) is one of the main requirements of NB-IoT applications. It can also be observed that the output power curve does not reach saturation in Figure 51. This is because in case of EER, the devices in power amplifier (inverse class D amplifier) act as a switch and the supply voltage is changed according to the changes in the input power. Thus, when the input power is increased, the supply voltage also increases and increase in the supply voltage gives higher output power. However, eventually the output power will saturate as the power supply connected to the supply modulator is fixed.

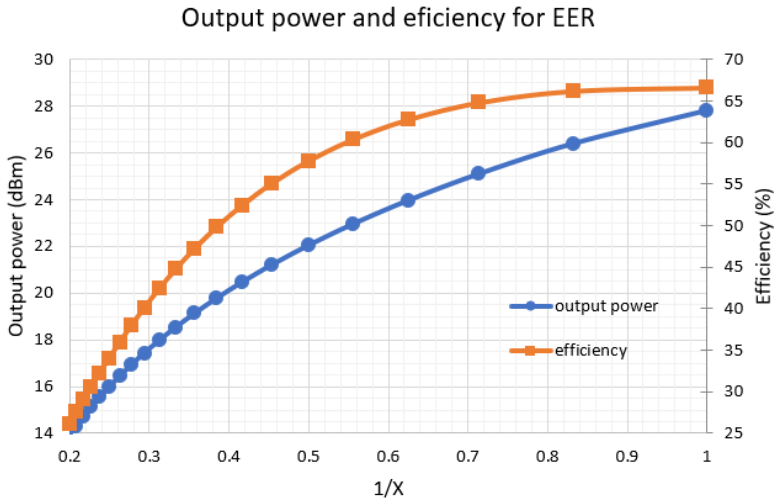

Figure 51 Output power and efficiency for EER PA vs 1/X (parameter for input gain control)

A plot of efficiency vs output power for EER amplifier is shown in Figure 52. The efficiency becomes almost constant for output power above 25 dBm. As the amplifier is designed for 20 dBm output class, it is observed that the PA can handle the required output power and PAPR of 6 dB with good efficiency.

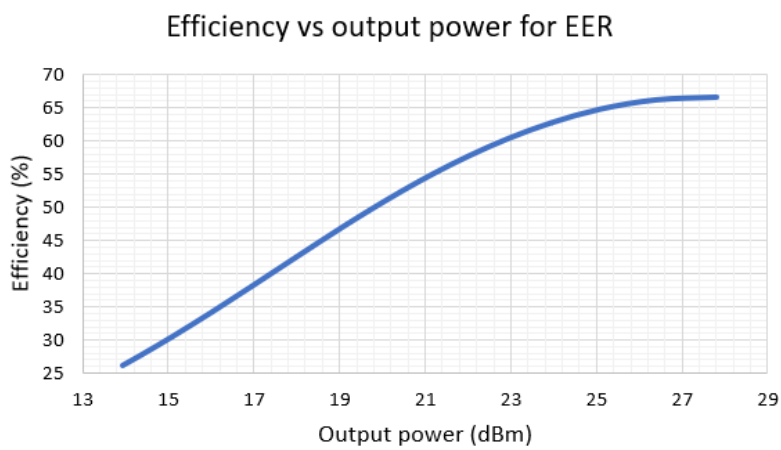

Figure 52 Efficiency vs output power for EER PA

8.2.3. Power and efficiency for Hybrid EER

The output power and efficiency for the hybrid EER power amplifier is shown in Figure 53. The PA can achieve a 28 dBm peak power with a peak efficiency of 66%. The nature of the efficiency and output power curve is similar to the EER power amplifier but, the peak efficiency is slightly lower (0.3%). This is due to the additional inverter stage used in case of the hybrid EER PA.

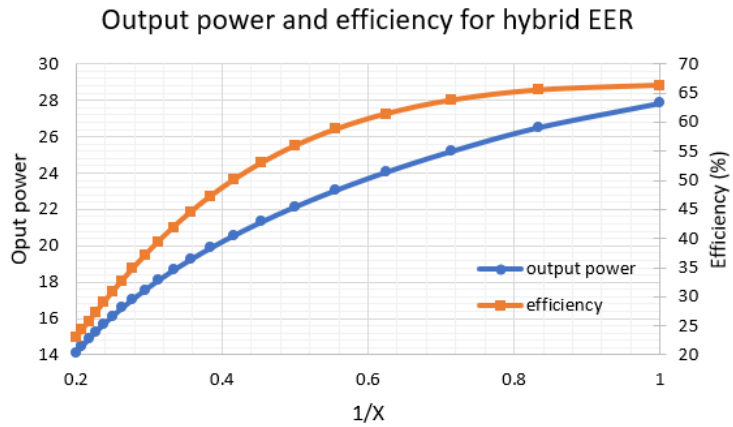

Figure 53 Output power and efficiency for the hybrid EER power amplifier vs 1/X (parameter for input gain control)

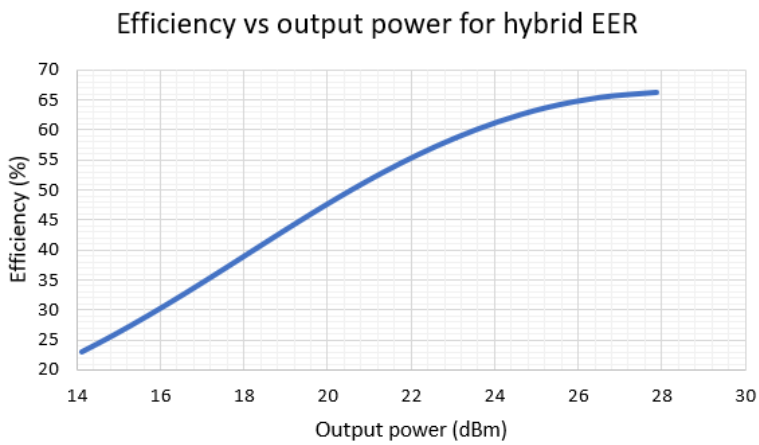

Figure 54 Efficiency vs output power for the hybrid EER power amplifier.

Figure 54 shows efficiency vs power graph the hybrid EER power amplifier. The efficiency is almost constant after 26 dBm. As the amplifier is designed for 20 dBm output power class, it can handle the required output power and a PAPR of 6 dB with good efficiency.

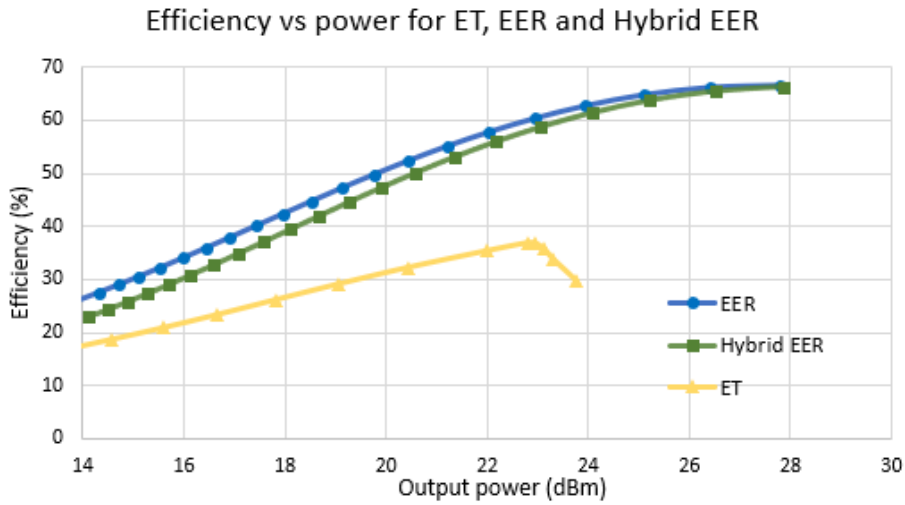

Figure 55 Efficiency vs output power for ET, hybrid EER and EER

Figure 55 shows a plot of efficiency vs output power for all the three architectures. The use of inverse class D amplifier and lesser number of inverters as compared to hybrid EER, enables the EER power amplifier to achieve best efficiency characteristic among the three architectures.

8.3. EVM, ACPR and dynamic range

This section shows the maximum and minimum output power that can be achieved by using the power amplifiers while satisfying the NB-IoT requirements of EVM and ACPR. EVM and ACPR are simulated using the 'envlp' analysis available in Spectre of the Cadence Virtuoso tool. The bandwidth for the main channel and for the adjacent channels (victim systems) is set using the ACPR wizard. The dynamic range is calculated as the difference between the maximum and the minimum output power that can be achieved without violating the NB-IoT specifications of EVM and ACPR. In general, the dynamic range of an inverse class D power amplifier is lower as compared to a class A power amplifier. This is because, it is difficult to

completely turn off the inverse class D power amplifier due to large size of the devices and capacitive leakage.

8.3.1. Hybrid EER architecture

The amplifier can deliver a peak power of 28 dBm with efficiency of 66%. However, it violates the ACPR specification at such a high output power. Table 5 shows that the highest and the lowest output power that can be achieved while staying within the EVM and ACPR specifications for NB-IoT is 25 dBm and 1.3 dBm respectively. Thus, the dynamic range that can be achieved with hybrid EER PA is 23.7 dB

Table 5 EVM and ACPR for hybrid EER

Output power	EVM (%) Specification: 17	ACPR (dBc)			
		Victim system: GSM Specification: -20		Victim system: UTRA Specification: -37	
		Low	high	low	High
25 dBm	6.7	-20.01	-21	-45.8	-44.9
1.3 dBm	14.3	-20.98	-22.8	-40.3	-40.2

8.3.2. EER architecture

The EER amplifier can deliver a peak power of 28 dBm with efficiency of 66%. However, it violates the ACPR specification at such a high output power.

Table 6 shows the highest and the lowest output power that can be achieved with the EER architecture, while staying within the EVM and ACPR specifications for NB-IoT is 26 dBm and 2 dBm respectively. Thus, the dynamic range that can be achieved with EER PA is 24.4 dB

Table 6 EVM and ACPR for EER

Output power	EVM (%) Specification: 17	ACPR (dBc)			
		Victim system: GSM Specification: -20		Victim system: UTRA Specification: -37	
		Low	high	low	High
26.4 dBm	5.5	-25.1	-21.7	-41.4	-41.2
2 dBm	16.1	-21.7	-25.6	-42.3	-41.6

The major advantage of hybrid EER architecture over the EER architecture is the reduced effect of delay mismatch between the envelope and phase signals. In case of 802.11a standard (Wi-Fi standard), the maximum allowed delay is 2 ns i.e. 4% of the symbol time (50 ns) [31]. For EER architecture designed in this project, the delay introduced by the supply modulator in the envelope path is 430 ns i.e. 7.7% of the symbol time. But, from the results obtained it is observed that, the linearity performance of EER is similar to the hybrid EER. Thus, it can be concluded that for NB-IoT specifications, the delay mismatch in case of EER does not have significant impact. This is because NB-IoT has low modulation bandwidth (180 kHz) and a relaxed requirement on EVM and ACPR

8.3.3. ET architecture

The amplifier can deliver a 24 dBm peak power with an efficiency of 37%. However, it violates the ACPR specification at such a high output power.

Table 7 shows the highest and the lowest output power that can be achieved while staying within the EVM and ACPR specifications for NB-IoT is 23 dBm and -40 dBm respectively. As mentioned earlier, the supply voltage is varied according to the input power. Thus, while determining the lowest possible output power, the supply voltage is kept constant at 1V to prevent the devices from turning off and the input power is lowered. The dynamic range that can be achieved with ET PA is 63 dB.

Table 7 EVM and ACPR for ET

Output power	EVM (%) Specification: 17%	ACPR (dBc)			
		Victim system: GSM Specification: -20 dBc		Victim system: UTRA Specification: -37 dBc	
		Low	high	low	High
23 dBm	3.5	-24.6	-21.7	-46.7	-45.4
-40 dBm	4.9	-22.65	-20.64	-45.18	-45.85

8.4. Output matching

The resonant tank circuit performs the function of a matching network in addition to conversion of the signals from differential to single ended. To have an efficient power amplifier, it is extremely important to have a proper matching network so that, the losses due to reflection are minimized and the maximum output power is transferred to the load. The output voltage curve showing resonance at 1.84 GHz and the S22 curve for all the three architectures is shown in Figure 56, Figure 57 and Figure 58. The minimum S22 requirement of -6 dB is full filled by all the three architectures.

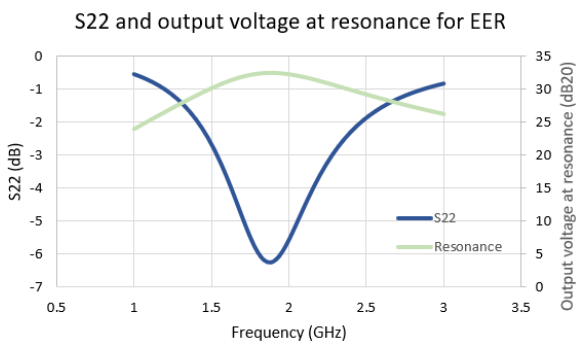

Figure 56 S22 and output voltage at resonance for EER

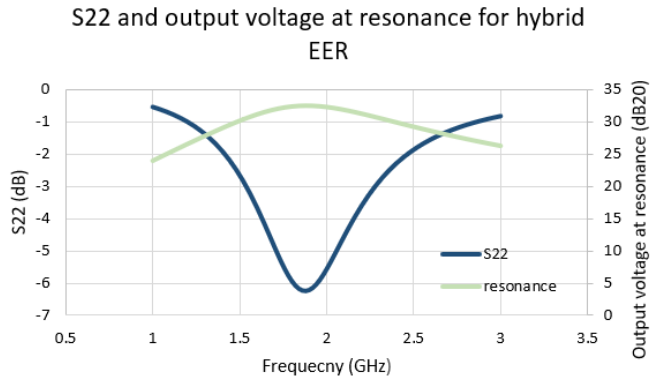

Figure 57 S22 and output voltage at resonance for hybrid EER

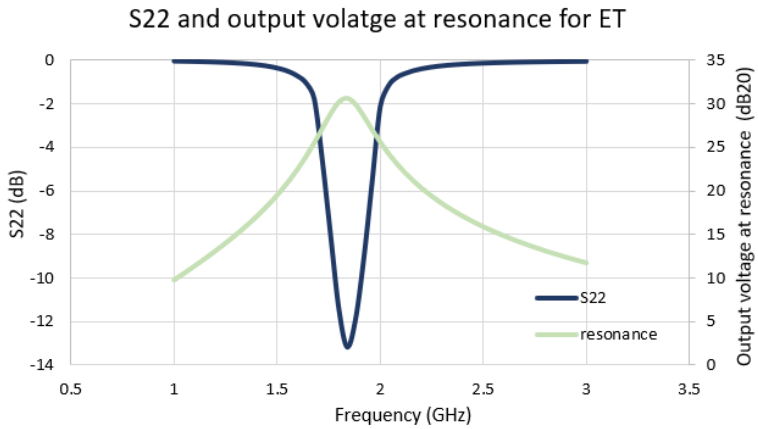

Figure 58 S22 and output voltage at resonance for ET

9. Conclusion

The rapid growth in connected devices promise lucrative business opportunities in the Internet of Things (IoT) segment. Narrow Band IoT (NB-IoT) is a new emerging mobile standard for IoT applications. For battery operated devices, a lifetime of 10 years or more is desired. It makes low power consumption an important requirement for such devices. The overall power efficiency of a radio circuit is strongly dependent on the power amplifier. Design of the power amplifier also depends on the transmission technique to be used. As a result, the design and implementation of the PA as well as selection of the transmission technique requires detailed attention and efforts to ensure the maximum efficiency and sufficient linearity.

In the project, an inverse class D power amplifier and a class A power amplifier are designed and implemented on schematic level in 65 nm CMOS technology for 20 dBm power class and NB-IoT specifications. A switch mode supply modulator is also designed. The peak efficiency achieved by the supply modulator is 90%. Three different efficiency enhancement techniques – ET, EER and hybrid EER are studied and suitable transmitters are simulated. The peak output power that can be achieved by ET, EER and hybrid EER is 24 dBm with efficiency of 37%, 28 dBm with an efficiency of 67% and 28 dBm with an efficiency of 66% respectively.

As compared to the class A power amplifiers with a fixed supply, implementing ET architecture improved the efficiency of class A PA by almost 15% as observed in Figure 50. Thus, it is advisable to implement ET architecture if a linear PA is being used instead of using the PA with a fixed supply. ET achieves a dynamic range of 63 dB, which is the highest dynamic range among all the three architectures. The lowest required output power according to NB-IoT specifications is -40 dBm and only ET transmitter can satisfy the EVM and ACPR requirements at such a low output power. However, as ET uses a linear PA, the overall efficiency of ET power amplifiers is much lower than EER and hybrid EER architectures. The major advantage of hybrid EER architecture over the EER architecture is the reduced effect of delay mismatch between the envelope and phase signals. But, from the results obtained it is observed that the linearity performance of EER is similar to the hybrid EER. Thus, it can be concluded that for NB-IoT specifications, the delay mismatch in case of EER does not have significant impact. This is because NB-IoT has low modulation bandwidth (180 kHz) and a relaxed requirement on EVM and ACPR

ET, Hybrid EER and EER architectures have some advantages and some disadvantages. Although only ET can achieve the lowest specified output power among the three architectures, it can deliver a maximum usable 23 dBm output power. Thus, it cannot handle the 6-tone uplink signal which has a PAPR of 6 dB and it has lower efficiency as compared to the other two architectures. EER transmitter has a slightly better performance than hybrid EER transmitter. Thus, in

order to have an efficient transmitter to enable the battery-operated devices to have a battery life of more than 10 years, EER with inverse class D amplifier is proposed to be the most suitable architecture.

10. References

1. O. Liberg, M. Sundberg, Y.-P. Eric Wang, J. Bergman, J. Sachs, "Cellular Internet of Things: Technologies, Standards and Performance", Academic Press an imprint of Elsevier, ISBN: 978-0-12-812458-1, 2017
2. HUAWEI, NB-IoT - Enabling New Business Opportunities, White paper
3. LoRa Alliance Technical Marketing Workgroup 1.0, LoRaWAN™, What is it?, A Technical Overview of LoRa and LoRaWAN™ , White paper, November 2015
4. Sigfox, About Sigfox, 2018, Available at: https://makers.sigfox.com/
5. Sreshtha, R. (2010). "*RF POWER AMPLIFIER TECHNIQUES FOR SPECTRAL EFFICIENCY AND SOFTWARE-DEFINED RADIO"* (Doctoral dissertation). Univeresity of Twente, Enschede, Netherlands. ISBN: 9789036530767
6. T. Lee, "*THE DESING OF CMOS RADIO FREQUENCY INTEGRATED CIRCUITS* ",The press syndicate of the university of Cambridge, ISBN: 0-521-83539-9, 2004
7. Doudorov, G.(2003). *Evaluation of Si-LDMOS transistor for RF power amplifier in2-6 GHz frequency range* (Master's thesis). Linköping University, Linköping, Sweden. ISRN: LITH-ISY-EX-3435-2003
8. Worku, F.Y. (2011). *Bias Circuit for RF Power Amplifier* (Master's thesis). Chalmers University of Technology, Gothenburg, Sweden. Retrieved from http://publications.lib.chalmers.se/records/fulltext/155399.pdf
9. P.Asbeck, and C. Fallesen, "A 29 dBm 1.9 GHz class B power amplifier in a digital CMOS process" in the proceedings of *ICECS 2000. 7th IEEE International Conference on Electronics, Circuits and Systems*, ISBN: 0-7803-6542-9, pp. 474-477, Jounieh, Lebanon, Lebanon, December 2000
10. Y. Ng, L. Leung, K. Leung, " A 3 GHz fully-integrated CMOS Class AB power amplifier" in the proceedings of 2009 52nd IEEE International Midwest Symposium on Circuits and Systems. ISBN: 978-1-4244-4479-3, pp. 995-998, Cancun, Mexico.
11. S. Cao, Y. Liu, W. Lu, "A 2.4 GHz highly linear class C power amplifier in 0.18 μm CMOS technology" in the proceedings of *2007 7th International*

Conference on ASIC, ISBN: 978-1-4244-1131-3, pp. 427-430, Guilin, China, October 2007.

12. K. Oishi, E. Yoshida, Y. Sakai, H. Takauchi, Y. Kawano, N. Shirai, H. Kano, M. Kudo, T. Murakami, T. Tamura, S. Kawai, K. Suto, H. Yamazaki, T. Mori, " A 1.95 GHz Fully Integrated Envelope Elimination and Restoration CMOS Power Amplifier Using Time Alignment Technique for WCDMA and LTE", *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2915-2924, December 2014.

13. D. Chowdhury, L. Ye, E. Alon, A. Niknejad, "An Efficient Mixed-Signal 2.4-GHz Polar Power Amplifier in 65-nm CMOS Technology", *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1796 – 1809, August 2011.

14. D. Chowdhury, S.Thyagarajan, L. Ye, E. Alon, A. Niknejad, " A Fully-Integrated Efficient CMOS Inverse Class-D Power Amplifier for Digital Polar Transmitters ", *IEEE Journal of Solid State Circuits*, vol. 47, no. 5, pp 1113 - 1122, May 2012

15. H. Kobayashi, J. Hinrichs, P. Asbeck, "Current mode class D power amplifier for high frequency RF applications" *IEEE Transactions on Microwave Theory and Techniques*, vol. 29, no. 12, pp. 2480 – 2485, December 2001.

16. N. Sokal, A. Sokal, "Class E- A New Class of High Efficiency Tuned Single-Ended Switching Power Amplifiers" *IEEE Journal of Solid State Circuits*, vol. 10, no. 10, pp. 168-176, June 1975

17. F. Raab, "Idealized operation of the class E tunes power amplifier" *IEEE transactions on Circuits and Systems*, vol. 24, no. 12, pp. 725-735, December 1977

18. A. Ghorbani, M. Ghaznavi-Ghoushchi, "A 35.6 dB, 43.3% PAE class E differential power amplifier in 2.4GHz with cross coupling neutralization for IoT applications" in the proceedings of 2016 24th Iranian Conference on Electrical Engineering, ISBN: 978-1-4673-8789-7, pp. 490-495, Shiraz, Iran, May 2016

19. Ellie Cijvat (2010). CMOS Integrated Switched-Mode Transmitters for Wireless Communication, Advances in Solid State Circuit Technologies, Paul K Chu (Ed.), ISBN: 978-953-307-086-5, InTech, Available from: http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/cmos-integrated-switched-mode-transmitters-for-wireless-communication

20. Wang, F. (2006) *High Efficiency Linear Envelope Tracking and Envelope Elimination and Restoration Power Amplifier for WLAN OFDM Applications* (Doctoral dissertation). University of California, San Diego

21. F. Wang, D. Kimball, J. Popp, A. Yang, D. Lie, P. Asbeck, L. Larson, "An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4086-8099, December 2006

22. K. Oishi, E. Yoshida, Y. Sakai, H. Takauchi, Y. Kawano, N. Shirai, H. Kano, M. Kudo, T. Murakami, T. Tamura, S. Kawai, K. Suto, H. Yamazaki, T. Mori, "A 1.95 GHz Fully Integrated Envelope Elimination and Restoration CMOS Power Amplifier Using Time Alignment Technique for WCDMA and LTE", *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2915-2924, December 2014

23. Technical Report for BS and UE radio transmission and reception (Release 13), 3GPP TR 36.802V13.0.0 (2016-06) http://www.3gpp.org/

24. S. Shin, NB-IoT System Modeling: Simple Doesn't Mean Easy, Keysight Technologies White paper.

25. P. Kenington, 2000, "*High-Linearity RF Amplifier Design",* Boston, London, Artech House, ISBN: 1-58053-143-1

26. W. Chen. 2007."*The VLSI Handbook*", CRC Press, ISBN: 978-0-8493-4199-1,

27. Stauth, J.T, Sanders, S.R, "*Dynamic Power Supply Design for High Efficiency Wireless Transmitters"* (Master's thesis), 2006. University of California, Berkely. Retrieved from https://www2.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-72.pdf

28. H. Zhang, Basic Concepts of Linear Regulator and Switching Mode Power Supplies, LINEAR TECHNOLOGY Application note 140, October 2013.

29. Y. Li, "*A NMOS Linear Voltage Regulator for Automotive Applications*" (Master's thesis), DELFT University of Technology, Delft, Netherlands. 2012 disadvantages of switching power supplies

30. Milosevic, D. (2009). High- efficiency linear RF power amplification: a class-E based EER study case Eindhoven: Technische Universiteit Eindhoven DOI: 10.6100/IR656555

31. J. Bercher, C. Berland, "Envelope/Phase delays correction in an EER radio architecture" in the proceedings of 2006 13th IEEE International

Conference on Electronics, Circuits and Systems, ISBN: 1-4244-0394-4, pp. 443-446, Nice, France, December 2006