EBL Patterned ITO Contacts for Single Nanowire Devices

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Abstract

Nanowires have attracted interest as fundamental building blocks for electronic and optoelectronic devices as well as for fundamental research. Photonic studies of single nanowire devices typically involve patterning of metal electrodes for electronic access, yet plasmonic effects between the metal contacts and the light source may perturb experimental measurements. An alternative to conventional metallic contact materials is transparent conductive oxides (TCOs), such as indium tin oxide (ITO). ITO is a well-studied TCO often used as transparent top contact for optoelectronic devices, including nanowire array devices. Contacting single nanowires requires high-resolution patterning of the ITO electrodes, which has never been reported using EBL. Here, we demonstrate a simple method for patterning sub–100nm wide ITO lines with EBL and lift-off. We contacted single InAs nanowires and demonstrated ohmic ITO contacts and measured for the first time a specific contact resistivity of $(3.94 \pm 2.79) \times 10^{-5}\,\Omega\mathrm{cm}^2$, which to the best of our knowledge is the lowest specific contact resistivity between ITO and any semiconductor. Although ITO properties were improved by annealing, the ITO contact resistance increased which was hypothesized to be caused by oxygen diffusing from ITO to the InAs during the heat treatment. The contact resistivity of 3.5 nm/5.5 nm/100 nm Ni/Au/ITO contacts to InAs nanowires was generally higher than that of pure ITO contacts at $10^{-4}\,\Omega\mathrm{cm}^2$. Annealing indicated that contact resistivity of these contacts could be improved, but no definitive conclusion could be drawn from the statistical analysis.

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Acronyms

$(NH_4)_2S_x$ Ammonium polysulfide.

In_2O_3 Indium oxide.

SnO_2 Tin oxide.

1D One Dimensional.

2D Two Dimensional.

DC Direct Current.

DOS Density of states.

EBL Electron Beam Lithography.

GaAs Gallium Arsenide.

HC Hot Carrier.

HCSC Hot Carrier Solar Cell.

InAs Indium Arsenide.

InP Indium Phosphide.

ITO Indium Tin Oxide.

IV Current Voltage.

LED Light Emitting Diode.

LNL Lund Nano Lab.

MESFET Metal Semiconductor Field Effect Transistor.

NW Nanowire.

RF Radio Frequency.

RT Room Temperature.

RTA Rapid Thermal Annealing.

SC Solar Cell.

SMU Source Measure Unit.

TCO Transparent Conductive Oxide.

TLM Transmission Line Model.

Symbols

A^* Richardson effective constant.

A Area.

χ Electron affinity.

e Elementary charge.

E_C Conduction band energy.

E_F Fermi-level.

E_{Fm} Metal Fermi-level.

E_{Fs} Semiconductor Fermi-level.

ε_s Semiconductor permittivity.

$E_{\mathbf{vac}}$ Vacuum energy.

$\mathbf{F}$ Force.

J Current density.

J_s Reverse current density.

k Boltzmann constant.

L Contact width.

l Length.

L_T Transfer length.

μ Charge carrier mobility.

n Negative charge carrier concentration.

N_D Concentration of donor dopants.

P_c Chamber pressure.

Φ_B Schottky barrier energy.

Φ_m Metal work function.

Φ_s Semiconductor work function.

P_s Source material vapor pressure.

q Charge.

R_C Contact resistance.

$R_{\mathbf{dep}}$ Deposition rate.

ρ Resistivity.

ρ_C Specific contact resistivity.

$R_{\mathbf{horizontal}}$ Horizontal resistance.

$\rho_{\mathbf{NW}}$ Semiconductor resistivity.

R_L Line resistance.

$r_{\mathbf{NW}}$ Nanowire radius.

R_S Sheet resistance.

$R_{\mathbf{vertical}}$ Vertical resistance.

T Temperature.

t Thickness.

V Bias.

$V_{\mathbf{acc}}$ Acceleration voltage.

V_{bi} Built-in voltage.

W Width.

W_{sc} Space charge region width.

1 Introduction

This section presents the outline for the thesis and provides a background for relevant subjects and key concepts as well as motivation of the work and overall scope of the thesis.

1.1 Background

Nanowires (NWs) are nanoscale structures characterized by high aspect ratios: widths are typically in the range of ten to a few hundred nanometers and heights range from hundreds of nanometers to several micrometers. Several properties make NWs attractive in research, and for improving existing and realizing novel electronic devices. Their minute sizes may confine the charge carriers in all physical dimensions but one, leaving them free to move only along the axis of the wires and effectively lowering the Density of states (DOS) of the electrons to one dimension (1D). Low-dimensional semiconductor systems with 1D and 2D DOS are intensively researched in semiconductor physics and have found many applications in opto-electronic technologies, for example in lasers, LEDs, transistors, sensors and solar cells (SC) [1].

The dimensions of NWs are advantageous in other aspects, too. The strive for more efficient solar cells and LEDs has led researchers to explore exotic material systems such as InAs, GaAs and InP which are considerably more expensive than the currently dominating workhorse material Si. In contrast to conventional planar semiconductor geometries, the small footprint of NWs can drastically reduce expensive material consumption and possibly make such implementations economically viable [2, 3, 4, 5]. Further, materials of different lattice constants can be combined in ways that would not be possible in conventional planar layered technologies as the NWs can relax interfacial strain between lattice-mismatched materials radially: strain induced dislocations are pushed outwards towards the surface of the NWs where they are annihilated [6, 7]. The ability to combine different semiconductors to create so-called heterostructures is crucial for fabricating many solid-state devices [1, 8, 9].

The beneficial properties of NWs lend themselves especially well to SCs, where a lot of effort has been put into making them more efficient and to a

lower cost [10, 11, 12, 13]. These SCs are conventional in the sense that they use *pn*-junctions to extract carriers excited by light and therefore suffer from fundamental efficiency limits; they can convert only parts of the incident solar spectrum to useful energy [14]. The reason is that the incoming photons from the sun either have too low energy to excite charge carriers above the bandgap or they have enough energy to excite the carriers, but with some excess kinetic energy that will quickly be lost in collisions with the surrounding lattice atoms, dissipating that energy as heat in a thermalization process.

A promising SC device concept aiming at increasing solar power conversion efficiencies are hot carrier solar cells (HCSC). HCSCs extract "hot" carriers (HC), i.e. carriers with excess kinetic energy, before they thermalize. Two fundamental physical phenomena can be utilized to realize this: HCs can be extracted before losing energy to phonons to increase the open-circuit voltage or the HCs can through inelastic collisions excite more carriers through impact ionization to increase the short-circuit current. The effects are mutually exclusive, i.e. only one of them can be utilized at a time, but their implications are tremendous: HCSCs can theoretically reach a solar energy conversion of 66% [15], by far surpassing the theoretical limit of 31% in conventional SCs [14].

1.2 Motivation

Ongoing research at Solid State Physics, Lund University by Steven Limpert et al. aims at unveiling the physics behind HC transport mechanisms in single NW HCSC devices and related photonic NW structures [16]. Some measurements have proven difficult as the Ni/Au electrodes conventionally used to contact the single NW samples exhibit plasmonic resonances in the metal-photon interaction, which interferes with the physical effects being investigated. To overcome these issues, it was proposed to use a non-metal contact material, namely Indium Tin Oxide (ITO). ITO is a transparent conductive oxide (TCO) which makes it attractive for photovoltaic applications: it has a high transmittance in the visible light spectrum and can simultaneously conduct a current with relatively low resistance [17, 18]. As such, it could make an excellent alternative contact material for sensitive photonic measurements on single NWs. Further, ITO could simultaneously act as a waveguide to selectively couple in light into the NW via optical modes for

wavelengths otherwise not accessible due to the minuscule diameter of the wire.

Lund Nano Lab (LNL) has capabilities for ITO sputtering deposition which is used in several photonic research projects [19]. In such projects, ITO is normally deposited at the end of the device fabrication as a coherent top electrode layer that extends over arrays of NWs. This is often in combination with a spacer layer that minimizes the area and hence sheet resistance of the TCO electrode on the device [10].

To contact and measure single NW devices, the ITO contacts must be patterned to high-resolution, nanoscaled contacts which poses some challenges. Fabrication of conventional Ni/Au contacts involves electron beam lithography (EBL) patterning of a resist followed by thermal evaporation of the metal and resist lift-off. Unlike thermal evaporation, sputtering is a non-directional deposition technique which may complicate lift-off of the resist, as the ITO layer risks becoming coherently deposited over the entire resist layer [20]. Although patterning and lift-off of microscale ITO contacts has been shown previously [21, 22, 23], EBL defined ITO contacts with dimensions of hundreds of nanometers have not been fabricated previously to the best of my knowledge.

1.3 Scope of the thesis

In this project, a processing strategy for fabricating high resolution ITO contacts to single InAs NWs has been devised using the state-of-the-art equipment present in LNL. The processed and contacted devices have been investigated using present measurement setups to determine the electrical contact quality and have been compared to Ni/Au contacts on single NWs. The processing has been optimized to achieve a robust fabrication process and as low resistive ITO contacts as possible. The main quality factor for electrical contacts is the *specific contact resistivity* (see Sec. 2.2.2 and 2.2.3) and a lot of effort has been put into investigating this quantity for ITO contacts on InAs NWs, which, to the best of my knowledge, has not been investigated previously. The specific contact resistivity between a contact and a device material is important for assessing the contact resistance a certain contact would give rise to. Generally, it is desirable to minimize the parasitic contact resistance for optimal device properties. Thermal annealing has been

investigated as a method to improve the contact resistivity for ITO contacts and Ni/Au/ITO contacts. An initial goal of the work was to compare the performance of NW devices utilizing ITO contacts to devices utilizing metal contacts in optical measurements, but had to be the subject of further experimental investigations due to time constraints.

2 Theory

This section expands on the concepts in Sec. 1 and gives a theoretical basis for the methods and physics relevant for results and discussion. As the main material utilized in the thesis is ITO, it deserves a subsection of its own where general properties are thoroughly explained. The remaining parts of Sec. 2 are dedicated to electrical contacts and how to measure their properties, and semiconductor processing techniques utilized in this work.

2.1 Indium tin oxide

ITO is arguably the most important and studied TCO. TCOs have found natural applications as transparent contacts in optoelectronic devices such as LEDs [24, 25], photodetectors [26, 27] and photovoltaics [17, 28] where good transparency is required to avoid optical losses in the emission or absorption of light. Although metals in general make far better contacts to such devices, they are often not suitable due to being notoriously opaque and thereby detrimental to optical properties.

ITO owes its popularity to its excellent transparency in the visible wavelength region ($\geq 90\%$) and low electrical resistivity in the order of $10^{-4}\,\Omega\,\mathrm{cm}$ [17, 18]. ITO is formed by doping indium oxide (In_2O_3) with tin (Sn), usually by sintering In_2O_3 and SnO_2 powders; common ratios are $90\,\mathrm{wt}\%$ In_2O_3 and $10\,\mathrm{wt}\%$ SnO_2 [29]. By itself, In_2O_3 is a wide-gap oxide with a bandgap of $3.5 - 4.3\mathrm{eV}$, making it transparent in the visible and near-infrared electromagnetic spectrum [18]. Sn atoms replace In atoms in the ITO lattice and act as n-type dopants. Together with n-type oxygen vacancies supplying two electrons each, ITO is a degenerately doped semiconductor with the Fermi-level (E_F) above the conduction band edge (E_C): carrier concentrations are in the order of $10^{20}\,\mathrm{cm}^{-3}$ to $10^{21}\,\mathrm{cm}^{-3}$ [17, 18, 30], enabling low electrical resistivity desired for contact material purposes. Electrical and optical properties of ITO are however interdependent in that the best electrical properties are achieved at some expense of the optical transmission [17].

ITO can be deposited in a number of ways, including sputtering [31], electron beam evaporation [32], chemical vapor deposition [33] and the sol-gel method [34]. ITO film properties vary strongly with the deposition method [17].

The most common method used is direct current (DC) and radio frequency (RF) sputtering due to potentially high deposition rates and industrial scale feasibility [30, 31]. Sputtering is the ITO deposition technique utilized in this project and details of the general sputtering deposition method are found in Section 2.3.2 while some specific notations of ITO sputtering are mentioned here.

For optimal film properties, ITO is sputtered onto a heated substrate ($\geq$200 °C) but such conditions may not be suitable for some applications such as photovoltaics, as elevated temperatures can damage the devices [31, 35, 36]. Heating is neither compatible with lift-off patterning utilized in this work as the resist polymer may melt and distort the contact patterns. Room Temperature (RT) sputtering may on the other hand suffer from poor ITO crystallinity due to limited adatom mobility during deposition and consequently poor conductivity and optical transmittance [30, 31].

The crystallinity can be promoted by post-deposition annealing, such as Rapid Thermal Annealing (RTA). The annealing step has several effects on the material properties. First, the crystallinity is improved as crystalline grains grow. This reduces the amount of grain boundary surface that act as carrier life-time reducing scattering sites, so carrier mobility is enhanced. Increased crystallinity moreover improves optical transmittivity. Second, annealing activates (ionizes) Sn dopants, which increases the amount of charge carriers, thereby reducing resistivity [30]. This effect is not unambiguously beneficial however, as the increase of Sn^+ ions increase the effect of impurity scattering [36].

Care must be taken when choosing annealing conditions such as ambient composition and temperature. Ref. [36] reported that 150 °C annealing for 2h gave different results for different atmospheres. While a H_2:Ar atmosphere drastically lowered resistivity by increasing carrier concentration, annealing in O_2 and air increased the resistivity of the sputtered films compared to the non-annealed samples. This is because the n-type oxygen vacancies in the ITO are annihilated during annealing in oxygen rich environments, while more oxygen vacancies are created upon annealing in a reducing environment such as H_2:Ar [36]. For RTA in vacuum, Ref. [30] showed that resistivity can be greatly lowered with increasing annealing temperature up to 600 °C as both mobility *and* carrier concentrations increase simultaneously. Wang et al. studied the influence of different atmospheres during ITO annealing at 200 °C

for 30 min [37]. While annealing in Ar and air improved transmittance of the films, the N_2 and forming gas (5% H_2:N_2) atmospheres resulted in lower resistivities and higher carrier mobilities in the ITO films. An interesting result of their study was that carrier concentrations *increased* after annealing in ambient conditions, more so than for N_2 and forming gas. Unfortunately, the authors do not discuss this observation. Although the ITO was deposited via electron beam evaporation, the improved electrical properties of the N_2 and forming gas annealed ITO films should be transferable to RF sputtered ITO. For ITO deposited on InAs NWs, temperatures should generally be kept below 300 °C to maintain structural integrity of the wires.

Last, the optical and electrical properties of ITO are highly related to deposited film thickness. Generally speaking, electrical properties are improved for thicker ITO films at the expense of lower transmission in the infrared and near-infrared regions [38]. As is evident from Eq. 6 in Sec. 2.2, sheet resistance R_S decreases with film thickness as $1/x$. Resistivity decreases too, but the decrease evens out after a thickness of 300 nm to 400 nm. This can be attributed to both the mobility and the carrier density increase in thicker films. The authors in Ref. [38] attributed this to larger grain sizes in thicker ITO films resulting in fewer scattering centers at grain boundaries.

2.2 Contacts and resistances

A good electrical contact should provide electronic access to the device by enabling charge transfer with as little resistance as possible. For devices on the nanoscale such as NW devices, this must be achieved at very small dimensions. This subsection provides a theoretical background of contacts and contact interfaces as well as some metrics used to assess performance and compare results of different contacts. The material system studied in this thesis, ITO and InAs (NWs), has been emphasized.

2.2.1 Schottky contacts and ohmic contacts

Consider a metal-n-semiconductor junction. Generally, the metal work function Φ_m, i.e. the energy required to promote an electron from the metal Fermi level E_{Fm} to the vacuum energy E_{vac}, differs from the semiconductor

work function Φ_s, which in this example is taken to be smaller. In thermal equilibrium, the Fermi levels E_{Fm} and E_{Fs} align, creating the bandstructure seen in Fig. 1.

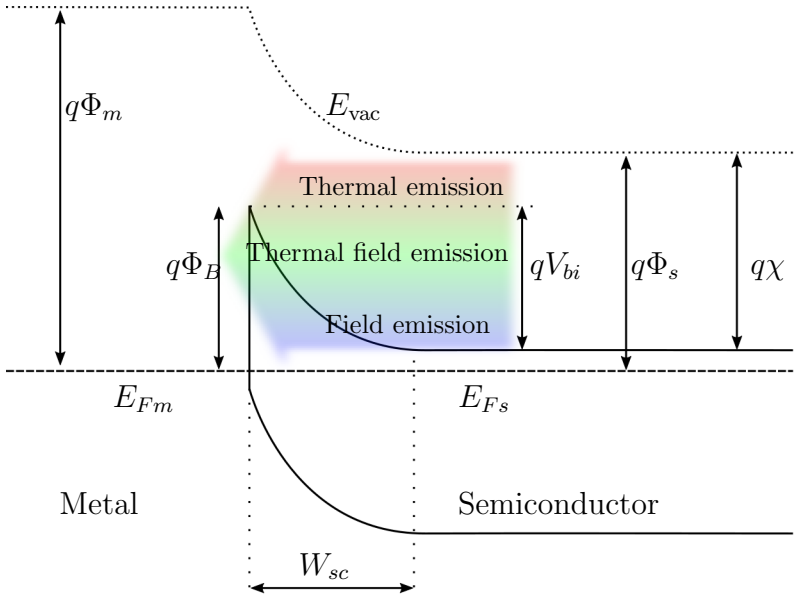

Figure 1: Schematic figure of the metal-semiconductor Schottky barrier junction and the current injection mechanisms.

On the semiconductor side, there are immobile positive charges near the junction left behind by electrons that have diffused to the metal and thermalized to E_{Fm}. The electric field between the semiconductor space charge region of width W_{sc} and the electrons in the metal creates an electric field that causes a built-in voltage of $qV_{bi} = q(\Phi_m - \Phi_s)$ that prevents more electrons from diffusing to the metal. W_{sc} and V_{bi} are related by Eq. 1 (from [39]):

$$W_{sc} = \sqrt{2\varepsilon_s V_{bi}/qN_D} \tag{1}$$

Where ε_s is the semiconductor permittivity and N_D is the dopant concentration. Electrons on the metal side are hindered from diffusing into the semiconductor by a potential barrier known as the Schottky barrier, the height of which surmounts to

$$q\Phi_B = q(\Phi_m - \chi) \tag{2}$$

where χ is the semiconductor electron affinity. The Schottky barrier is important when $q\Phi_B \gg kT$, i.e. much greater than the thermal energy of the electrons. Interfacial defects such as dangling bonds cause mid-gap states that in practice shifts the true barrier height from the ideal value in Eq. 2 [39]. This is especially the case for InAs that is known to have a high density of surface states [40].

There are three mechanisms for injecting electrons from the semiconductor to the metal: *thermionic emission*, *thermionic field emission* and *field emission* [41]. Electrons in the semiconductor with a thermal energy exceeding V_{bi} can diffuse into the metal unhindered. In thermal equilibrium, this current is matched by an opposite flow of electrons from the metal into the semiconductor yielding zero net current. A forward bias of V lowers V_{bi} by VeV. An exponentially larger number of electrons now have enough energy to pass the potential barrier and the diffusive current characteristics can according to [39] be described by

$$J = J_s(e^{qV/kT} - 1), \tag{3}$$

$$J_s = A^* T^2 e^{-q\Phi_B/kT} \tag{4}$$

where V is the applied bias, k is Boltzmann's constant, T is temperature and A^* is the effective Richardson constant which depends on the semiconductor material via its effective electron mass. A reverse bias will *not* significantly reduce the Schottky barrier $q\Phi_B$ that the electrons in the metal must overcome to be injected into the semiconductor; the reverse current J_s remains constant with V. The IV characteristics of a Schottky junction are therefore diode-like.

Thermionic field emission and field emission are tunnelling mechanisms where electrons can tunnel directly through the potential barrier into the metal. Their contributions to the current relative to thermionic emission are proportional to$\sqrt{N_D}$: high semiconductor doping levels reduce the barrier width and enhance the tunnelling probabilities [41, 42]. This is reflected in Eq. 1 where $W_{sc} \propto 1/\sqrt{N_D}$.

While Schottky contacts can be utilized to realize MESFETs and highly sensitive NW sensors [43], they introduce high contact resistances that can be detrimental for many semiconductor devices. In contrast, *ohmic contacts* have negligible contact resistances so that current can flow with a small voltage drop over the contact interface compared to the semiconductor device [39]. Ohmic contacts do not necessarily imply linear Current Voltage (IV) characteristics: the space charge region associated with every metal-semiconductor interface eventually make IV characteristics nonlinear for large enough biases [41].

2.2.2 Resistances

Resistances play an important role in electrical devices. It is both an inherent property of the particular material and a consequence of geometry and material combination. If you know the resistance each part of a device will contribute with, one can design the device to avoid parasitic resistances and improve the device functionality. The goal of this section and Sec. 2.2.3 is to introduce resistance concepts that are particularly important for ITO contact lines and ITO contact interfaces, namely *sheet resistance*, *contact resistance* and *specific contact resistivity*, as well as methods used to measure these quantities.

Resistance can be interpreted as the opposition to current flow. It is related to intrinsic material properties and the material dimensions by

$$R = \rho \frac{l}{A} \tag{5}$$

where ρ is the material resistivity, l is the length and A is the area of the cross-section through which current flows. A convenient way to assess resistance of a contact line of some length l and width W is to decompose A in Eq. 5 to the thickness t times the width W such that

$$R = \rho \frac{l}{tW} = R_S \frac{l}{W} \tag{6}$$

where we have introduced the *sheet resistance* $R_S = \rho/t$. Now, if $l = W$ in Eq. 6 the total resistance R of the contact line equals R_S. If we know

the contact dimensions (l and W) and measure some resistance R, we can rearrange Eq. 6 to get R_S. Any rectangular contact can be divided into a number of squares with the same sheet resistance: adding them together gives the total contact line resistance. Knowing the sheet resistance of a contact material is thus valuable from an engineering perspective as it allows us to foresee the total resistance a contact of some length and width would contribute.

The resistivity ρ in Eq. 5 is an intrinsic material property. Using the Drude model, it is expressed as

$$\rho = \frac{1}{ne\mu} \tag{7}$$

where n is the (electron) carrier concentration, e is the elementary charge and μ is the carrier mobility, a measure of how fast charge carriers can move through the material [1].

In Sec. 2.2.1 the concepts of Schottky and ohmic contacts were introduced. We define contact resistance R_C as

$$R_C \equiv \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \tag{8}$$

as an important figure of merit for ohmic contacts [39]. R_C is the interfacial resistance between the contact and device. A related parameter is the specific contact resistivity ρ_C

$$\rho_C = R_C A \tag{9}$$

where A is the area of the of the contact-semiconductor interface. ρ_C is expressed in units of Ωcm^2 and is convenient for different contact geometries, such as planar contacts overlapping cylindrical NWs, as it is independent of the contact overlap area. Due to a phenomenom known as current crowding where current is mostly conducted through the edges of a contact, Eq. 9 cannot be used directly for planar contacts on cylindrical NWs to assess ρ_C. In the following section, equations that are specially adapted to this geometry are introduced.

2.2.3 Resistance measurements

A common way to measure R_C and ρ_C is to model the contact-semiconductor interface as a transmission line model (TLM) and to conduct TLM measurements. In Ref. [44], R_C for a cylindrical NW was derived as

$$R_C = \frac{\rho_{\mathrm{NW}} L_T}{\pi r_{\mathrm{NW}}^2} \coth(L/L_T) \tag{10}$$

where ρ_{NW} is the semiconductor NW resistivity, L is the length of the contact overlap on the NW (contact width), $L_T = \sqrt{r_{\mathrm{NW}} \rho_C / 2\rho_{\mathrm{NW}}}$ is the so-called transfer length and r_{NW} is the NW radius. We see that R_C and ρ_C are related by L_T in Eq. 10. If the contact is "long" such that $L > 3L_T$ Eq. 10 takes on the simpler form

$$R_C = \frac{\rho_{\mathrm{NW}} L_T}{\pi r_{\mathrm{NW}}^2} = \frac{\rho_C}{2\pi r_{\mathrm{NW}} L_T} \tag{11}$$

Eq. 10 and 11 assume that the NW is cylindrical and that the contact surrounds the entire NW. Further, it is assumed that the deposition of the contact does not change the NW material properties. The equations also assume that the contact is in direct physical contact with the NW throughout its length L [44]. If R_C of a device has been measured, Eq. 10 can be solved numerically for ρ_C using e.g. Python or MATLAB.

TLM measurements can be carried out with several single NW device designs. Three designs labeled Design 1, 2 and 3 are depicted in Fig. 2. While all designs were implemented and tested for ITO contacts on InAs NWs to measure R_C and ρ_C, Design 3 was the only method that provided sufficiently reliable results. For this reason, only details on measurement techniques for Design 3 are presented here. The interested reader is referred to Ref. [44] for details on measurements utilizing the other device designs.

Measurements on devices according to Design 3 (Fig. 2 C) employ a conventional four-point probe measurement where a current I_{14} is sourced between contacts one and four. The voltage drop V_{23} between contacts two and three, i.e. the inner contacts, is measured and, as the same current I_{14} runs between contacts two and three, the resistance between these contacts is

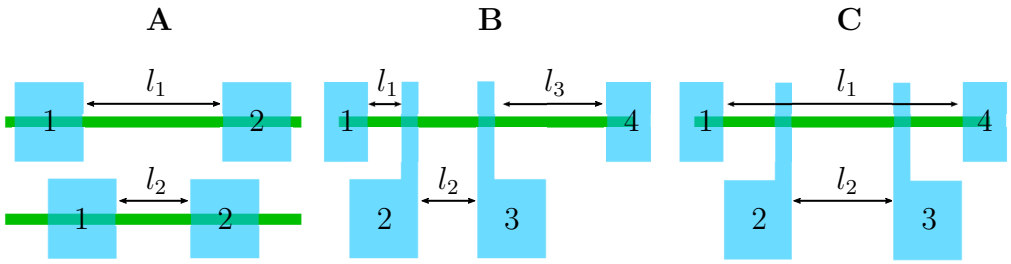

Figure 2: Three different TLM designs for measuring contact resistance between contacts (teal) and NWs (green): (A) Design 1, (B) Design 2 and (C) Design 3. Adapted from Ref. [44].

$$R_{23} = \frac{V_{23}}{I_{14}} = \rho_{\mathrm{NW}} \frac{l_2}{\pi r_{\mathrm{NW}}^2} \tag{12}$$

from which the NW resistivity ρ_{NW} can be extracted, given that l_2 and the NW radius r_{NW} are known. The measurement thereby avoids measuring contact resistance between the NW and the contacts. Due to the Fermi level pinning of InAs NWs causing conduction to primarily occur at the NW surface, Eq. 12 likely overestimates the resistivity of the InAs NWs [45].

In Fig. 2 C, l_2 is taken as the inner distance between the two inner probes, assuming that contacts 2 and 3 are infinitely small point contacts. In the non-ideal case when contacts 2 and 3 have a finite width, we shall take l_2 as the distance between half the widths of the contacts. When voltage is measured between contacts 2 and 3, the voltmeter is assumed to have an infinite input impedance. This is in practice a valid assumption using standard commercial measurement equipment [44]. The measurement of R_{23} is crucial in the following steps to extract R_C.

The resistance between the outer contacts one and four, R_{14}, is then measured by measuring the potential drop across them, such that $R_{14} = V_{14}/I_{14}$. R_{14} is equal to the total resistance of the entire NW and the contact resistances between contact 1 and the NW and contact 4 and the NW:

$$R_{14} = 2R_C + \rho_{\mathrm{NW}} \frac{l_1}{\pi r_{\mathrm{NW}}^2} = 2R_C + R_{23} \frac{l_1}{l_2} \tag{13}$$

After this two-point measurement, we can rearrange 13 to solve for R_C:

$$R_C = \Big(R_{14} - R_{23}\frac{l_1}{l_2}\Big)/2 \tag{14}$$

Having performed the four-point and two-point resistance measurements, we can use Eq. 14 to attain a value of R_C for a particular device. Knowing R_C, ρ_C can then be calculated by solving Eq. 10 or Eq. 11 for ρ_C.

There is however an issue with Eq. 13 as it assumes that the resistance of the contact lines is negligible, which often is the case for many metallic contact lines. For contact lines of ITO however, Eq. 13 should be modified to include the contact line resistance as ITO can have relatively high sheet resistance [46, 47]. Because the ITO contact lines can extend quite a bit before they contact the NWs, the resistance contribution from the contact lines R_L can be significant. Therefore, we modify Eq. 13 to include the contribution of the ITO contact lines:

$$R_{14} = 2R_C + R_{23}\frac{l_1}{l_2} + 2R_L \tag{15}$$

Rearranging Eq. 15 to solve for R_C, we obtain:

$$R_C = \Big(R_{14} - R_{23}\frac{l_1}{l_2} - 2R_L\Big)/2 \tag{16}$$

Again, with an experimental value of R_C, we can now solve Eq. 10 or Eq. 11 for a more correct value of ρ_C.

How can we obtain a value for R_L? As stated in Sec. 2.2.2, any rectangular contact line of dimensions $W \times l$ can be divided into a number of squares where each $W \times W$ square contributes with the sheet resistance R_S (Eq. 6). Hence, if the sheet resistance of the contact line material, e.g. ITO, is known, R_L can be expressed as $R_L = R_S \times$ #squares. This is schematically demonstrated in Fig. 3.

R_S can in turn be measured for "bulk" ITO (i.e. thin ITO layers sputtered on a macroscopic substrate) utilizing the van der Pauw method, as described in detail in Sec. 2.2.4. For patterned ITO lines, R_S can be measured by

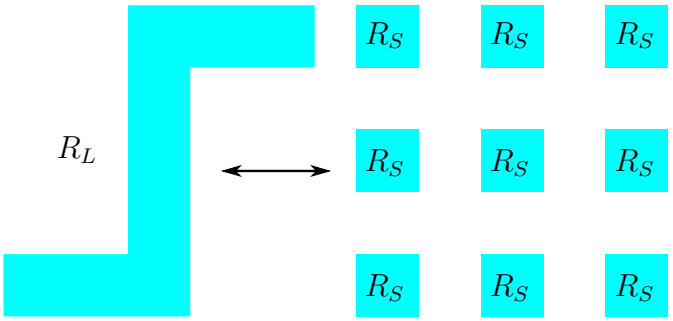

Figure 3: A rectangular contact line of dimensions $W \times l$ and resistance R_L can be divided into a number of $W \times W$ squares with a sheet resistance R_S

measuring the total resistance R of a single ITO line in a two-point measurement. If the width W and length l of the ITO line is known, Eq. 6 can be rearranged to $R_S = RW/l$.

The resistances present in a four-point probe device (schematically shown in Fig. 2 C) are explicitly shown in a circuit diagram in Fig 4.

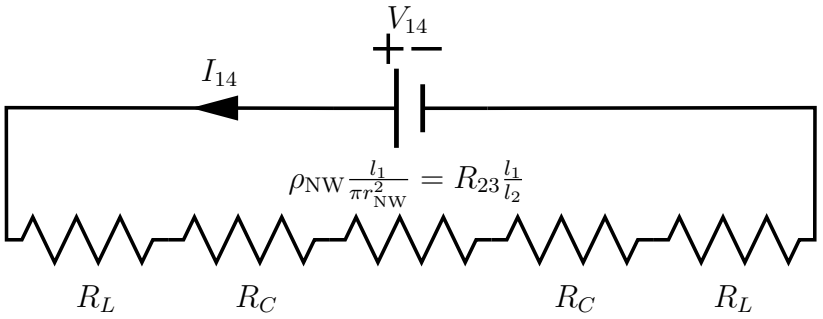

Figure 4: Equivalent circuit diagram depicting the resistances being measured in a four-point probe device measurement.

R_C and ρ_C should be as low as possible for ohmic contacts to have ideal device properties. High contact resistances can for instance be detrimental to the fill factor for NW solar cells [48]. ρ_C is generally negligible for many metal-semiconductor interfaces [49]. In Ref. [50] the authors measured $\rho_C = 5.1 \times 10^{-4}\,\Omega\mathrm{cm}^2$ between ITO and planar n-GaN; in Ref [48] the authors measured $\rho_C = 1.41\,\Omega\mathrm{cm}^2$ for ITO to n-GaAs NWs and $\rho_C = 0.13\,\Omega\mathrm{cm}^2$ for

an annealed ITO-In contact to the same NWs.

The most common way to achieve ohmic contacts to semiconductors is to have a region of high doping at the metal-semiconductor interface. This reduces W_{sc} (Eq. 1) so that any Schottky barrier will be virtually transparent to electrons impinging from the metal and the semiconductor and tunneling can dominate the conduction. This can be achieved by doping the surface layer of the semiconductor by ion implantation, shallow diffusion doping, or by alloy regrowth of the contact or in-diffusion of a dopant contained in the contact. In alloy regrowth, the surface of the semiconductor is dissolved in the contact material (metal) during heating. When it cools, the regrown semiconductor will contain a high concentration of metal, acting effectively as a highly doped interface. In-diffusion is similar in that the contact is heated, but dopant atoms from the metal instead diffuse into the semiconductor [41]. Both of these processes could theoretically occur during annealing of ITO contacts on NWs, which may be another benefit of annealing ITO contacts.

2.2.4 van der Pauw measurements

As originally devised by van der Pauw in 1958 [51], the van der Pauw method is routinely used in research and industry to characterize electrical properties of flat semiconductor samples. In this thesis, the van der Pauw method has been used to measure the bulk value of R_S of samples of sputtered ITO and sputtered Ni/Au/ITO layers. The measurement setup requires four contacts at the corners of the sample (Fig. 5) which makes it convenient to use the same sample for subsequent Hall measurements that have been used to measure carrier concentration and mobility of sputtered ITO layers.

The contacts are numbered 1 to 4 as shown in Fig. 5. The measurement procedure uses two characteristic sample resistances: R_{vertical} and $R_{\text{horizontal}}$. To calculate R_{vertical}, a current $I_{4,3}$ is run through contacts 4 and 3, and the voltage drop $V_{1,2}$ between contacts 1 and 2 is measured. From this measurement we calculate $R_{4,3} = V_{1,2}/I_{4,3}$. These measurements are repeated by sourcing a current $I_{1,2}$ through contacts 1 and 2 and measuring the voltage drop $V_{4,3}$ over contacts 4 and 3 so that $R_{1,2} = V_{4,3}/I_{1,2}$. The two resistances are combined to give R_{vertical}:

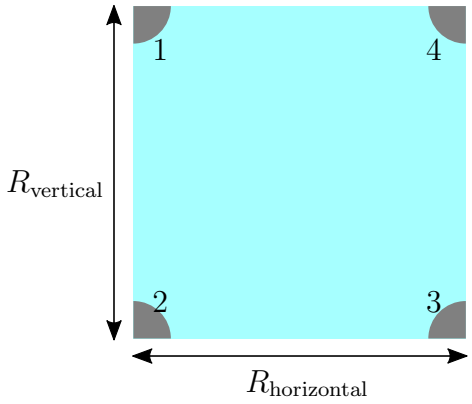

Figure 5: Schematic sample layout for van der Pauw measurements.

$$R_{\text{vertical}} = (R_{1,2} + R_{4,3})/2 \tag{17}$$

By the identical procedure for the other pairs of contacts, $R_{\text{horizontal}}$ is calculated to:

$$R_{\text{horizontal}} = (R_{1,4} + R_{2,3})/2 \tag{18}$$

The sheet resistance R_S of the sample can now be obtained by solving the van der Pauw equation ([51]):

$$e^{-\pi R_{\text{vertical}}/R_S} + e^{-\pi R_{\text{horizontal}}/R_S} = 1 \tag{19}$$

Eq. 19 can be solved for R_S numerically, for example in MATLAB or Python.

2.3 Semiconductor processing

Compared to the physical dimensions NW devices, single dust particles barely resolvable by the human eye are giants. Normal indoor environments contain large quantities of airborne dust particles and any one of them landing on a sample chip may short circuit or physically damage the devices. Semiconductor processing is therefore performed in a clean room, in which the

controlled environment severely limits the amount and size of airborne particles by diluting the lab atmosphere with filtered air several times per hour. The processing steps in this thesis were performed in Lund Nano Lab (LNL) which has a ISO 5 and ISO 7 cleanliness area. ISO 5 is a higher cleanliness standard than ISO 7: $10^5\,\mathrm{m}^{-3}$ particles of size $\geq 0.1\,\mu\mathrm{m}$ or fewer may be present in an ISO 5 clean room. Further details can be found in ISO 14644-1:2015.

A basic device consists of a single NW contacted by two or four contacts on a device chip which can hold up to 24 devices, depending on the number of contacts used per device. The goal of processing is to transfer InAs NWs to a device chip and contact them with a contacting material (ITO or metal) to measure NW and contact characteristics. A finished device chip is referred to simply as a sample. The processing sequence comprises a number of distinct sequential steps and tools to produce a sample. This section provides a basic theoretical background for a selection of the most important semiconductor processing techniques utilized in this thesis. The processing steps are schematically shown in Fig. 6.

2.3.1 Electron beam lithography

EBL is a crucial tool in nano engineering, as it allows writing arbitrary, high-resolution patterns in resists without the need of an expensive mask. In contrast to its industrial relative, the optical lithography tool, EBL has a rather low throughput. Nonetheless, it is a ubiquitous tool in most micro and nano fabrication labs.

Basically, the EBL tool is a modified SEM; imaging the sample is in fact crucial for the sample alignment procedure prior to exposure. It is therefore instructive to consider the layout of a SEM to understand how EBL works (Fig. 7 A).

Electrons are extracted from the electron gun, either by heating a low work function material (thermionic emission) or biasing a sharp tip (field emission). The electron gun ideally provides the system with a current of high brightness (high current density per solid angle) where the electrons are monochromatic (have a low energy spread). Field emission guns are superior in these aspects and are normally preferred. By heating the field emission gun (called Schot-

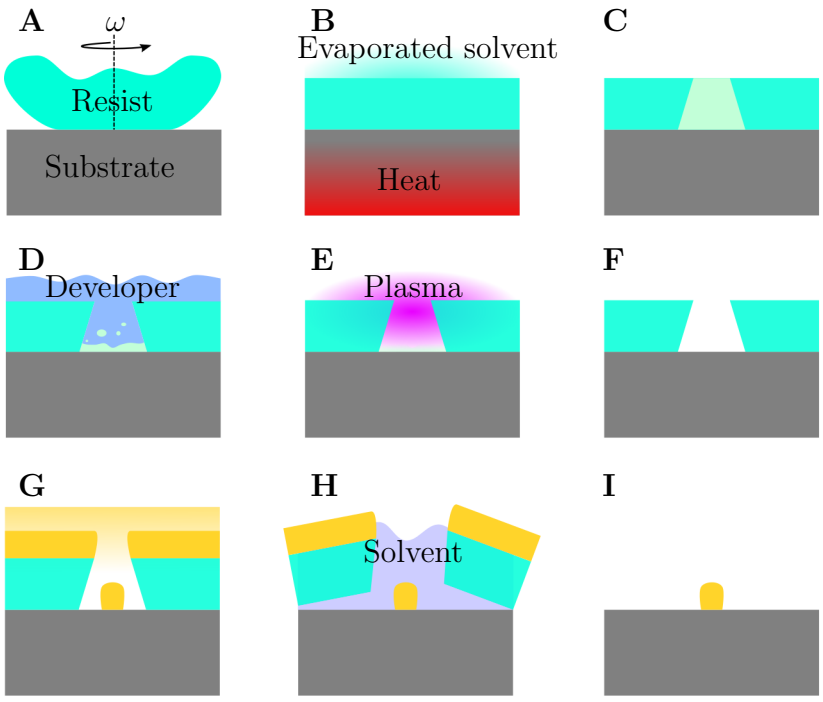

Figure 6: Schematic overview of the processing steps. (A) A resist is spun on the device chip (sample) and (B) then baked to evaporate solvent and harden the polymer. (C) A pattern is exposed in EBL and (D) the exposed parts are developed in a liquid solvent followed by (E) plasma ashing to remove residual developed polymer, (F) exposing the sample substrate. (G) Material is deposited over the entire sample. (H) After lift-off, (I) a patterned material has successfully been transferred to the sample.

tky field emission gun), vacuum constraints may be lowered as adsorbants on the gun that affect the current stability are effectively evaporated.

Following extraction, the electrons are accelerated with an acceleration voltage (V_{acc}) toward the sample. Condenser lenses utilize magnetic fields to merge the electron flow into a beam that is scanned over the sample using scanning poles. Prior to these, off-axis electrons are filtered with an aperture to increase monochromaticity of the beam at the expense of a lower current. The beam is converged into a nano-sized spot by the objective lens, which is arguably the most important lens in the system; the resolution is never better than the size of the beam spot. Any aberrations and astigmatism

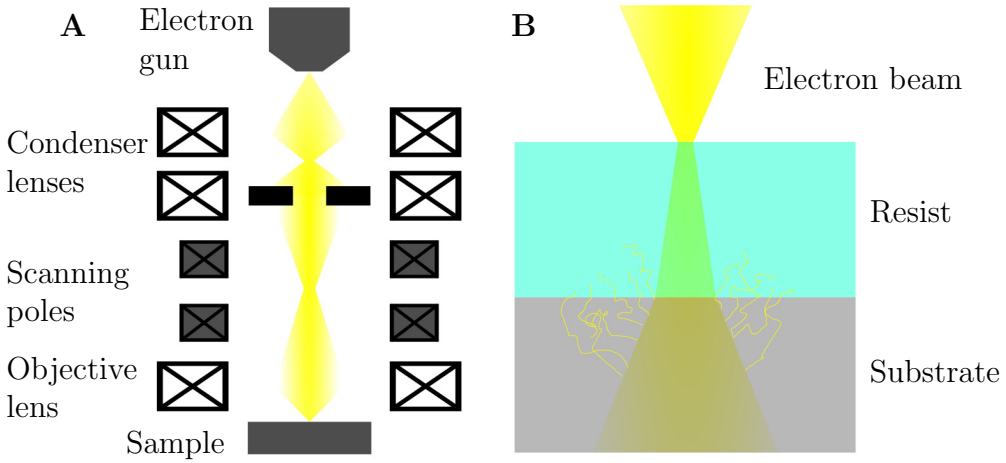

Figure 7: (A) Schematic drawing of SEM and (B) interaction between sample and electron beam.

(difference in focus along x and y axis) are corrected in the objective lens to achieve optimal focus and resolution. The size of the spot is limited by the electron optics and repulsive force between the electrons, the latter of which is more noticeable for higher currents and lover acceleration voltages, as more electrons must be converged to the same physical location [52].

The final pattern resolution is only partly given by the system. Upon entering the sample, the electrons undergo a series of collisions with the resist and substrate atoms. Most of the collisions are low-energy, elastic collisions between electrons and the resist and substrate nuclei. This causes the electrons to be deflected at low angles (forward scatter), broadening the beam [52]. The forward scattering limits the resolution of the pattern as the beam size becomes larger in the resist. The amount of deflection in the resist is related to the energy of the beam, and so a high acceleration voltage yields not only a small spot size, but also less forward scattering, improving the resolution. Lower acceleration voltages can however be much preferred, as the so-called undercut created in the resist is beneficiary for subsequent lift-off [20], as discussed further in Sec. 2.3.2 and 2.3.3.

The angle of deflection is higher for materials with higher atomic number, and so the beam broadens more when it reaches the more dense substrate. Some electrons are deflected many times at high angles such that they reemerge in the resist (Fig. 7 B). These electrons may expose the resist several microns

away from the intended site, causing a resolution limiting phenomenon known as the *proximity effect*, which is particularly important to consider for dense patterns [52].

The other type of electron-sample collisions are inelastic collisions that occur when the impinging primary electrons transfer energy to the sample electrons, resulting in bond breaking in the resist (chain scissons) and emission of secondary electrons from resist and substrate atoms. Secondary electron energies are much lower than the electron beam energy, giving them a much shorter range in the resist, but they cause the majority of the exposure and ultimately limit the resolution. Energy transferred from primary or secondary electrons to the resist causes physico-chemical reactions resulting in a higher or lower solubility of the exposed patterns for positive and negative resists, respectively. A common positive resist is poly-methyl methacrylate (PMMA), which has been used in this work. The energy provided by the electrons breaks the high molecular weight polymer chains into shorter, more soluble fragments. Many of such chain scissions are required for significant solubility change, why the electron beam exposure dose, defined as charge per unit area ($\mu C\,cm^{-2}$), is an important factor in the EBL process. A higher dose pushes the distribution of polymer fragment sizes toward smaller fragments and hence the solubility increases [52]. Further, a higher dose will also increase the undercut in the resist after development [20] (Fig. 8).

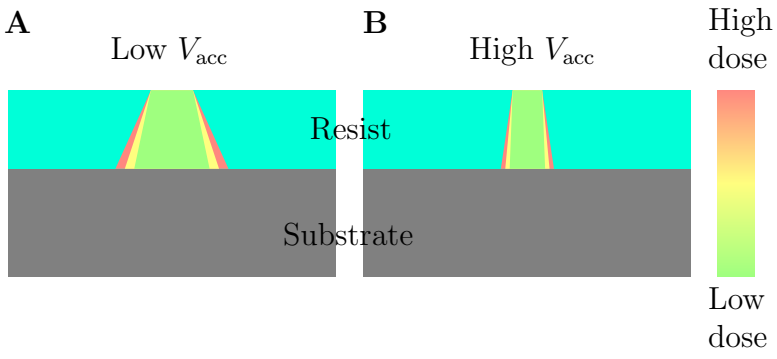

Figure 8: (A) Schematic resist profile for different doses at low V_{acc} and (B) at high V_{acc}.

2.3.2 Material deposition

Semiconductor devices utilize many types of thin film materials, which can be deposited with several fundamentally different methods. Metals and ITO are deposited using methods in the physical-vapor deposition (PVD) category. In PVD, atoms from the deposition material are ejected by some mean in vacuum and condensed on the sample. Common PVD methods are thermal evaporation, e-beam evaporation, plasma spray deposition and sputtering [20, 39].

Thermal evaporation and sputtering that have been used in this thesis differ in the way atoms are ejected from the deposition material. In thermal evaporation, a large current heats up a "boat" that the deposition material sits in. At a high enough temperature, the deposition material melts and vaporizes, ejecting atomic species in a directional beam normal to the boat (upwards). The sample sits at a distance r above the boat and the atomic species from the beam condense all over the sample, covering it in the desired material. The rate of deposition R_{dep} can be expressed by Knudsen's cosine law:

$$R_{\text{dep}} \propto \frac{\cos\theta\cos\phi}{r^2}(P_s(T) - P_c) \tag{20}$$

where θ is the angle of the sample to the normal axis of evaporation source, ϕ is the orientation of the sample surface relative to the orientation of the evaporation source, $P_s(T)$ is the (temperature dependent) source material vapor pressure and P_c is the chamber pressure. If the sample is oriented normal to the evaporated material, $\cos\phi$ reduces to 1, but it is clear that the deposition rate is non-uniform due to $\cos\theta$, especially for larger samples [20].

Thermal evaporation has some drawbacks: notably, it is not well suited for alloy materials that have different vapor pressures $P_s(T)$ in Eq. 20 and thus different deposition rates. Additionally, the quality of the deposited film is among the lowest of thin film deposition techniques [20]. Still, the simplicity of the method makes it suitable in research and for depositing materials with a relatively low melting point such as metals.

Dielectrics such as ITO usually have much higher melting points and require different means to eject atoms from the material; here sputtering has been used. In sputtering, energy is supplied by a plasma with cations that acceler-

ate towards the deposition material, called target. Momentum transfer from plasma ions ejects atomic species from the target in all directions; many of them deposit on the rotating sample that sits normal to the target (Fig. 9) [39].

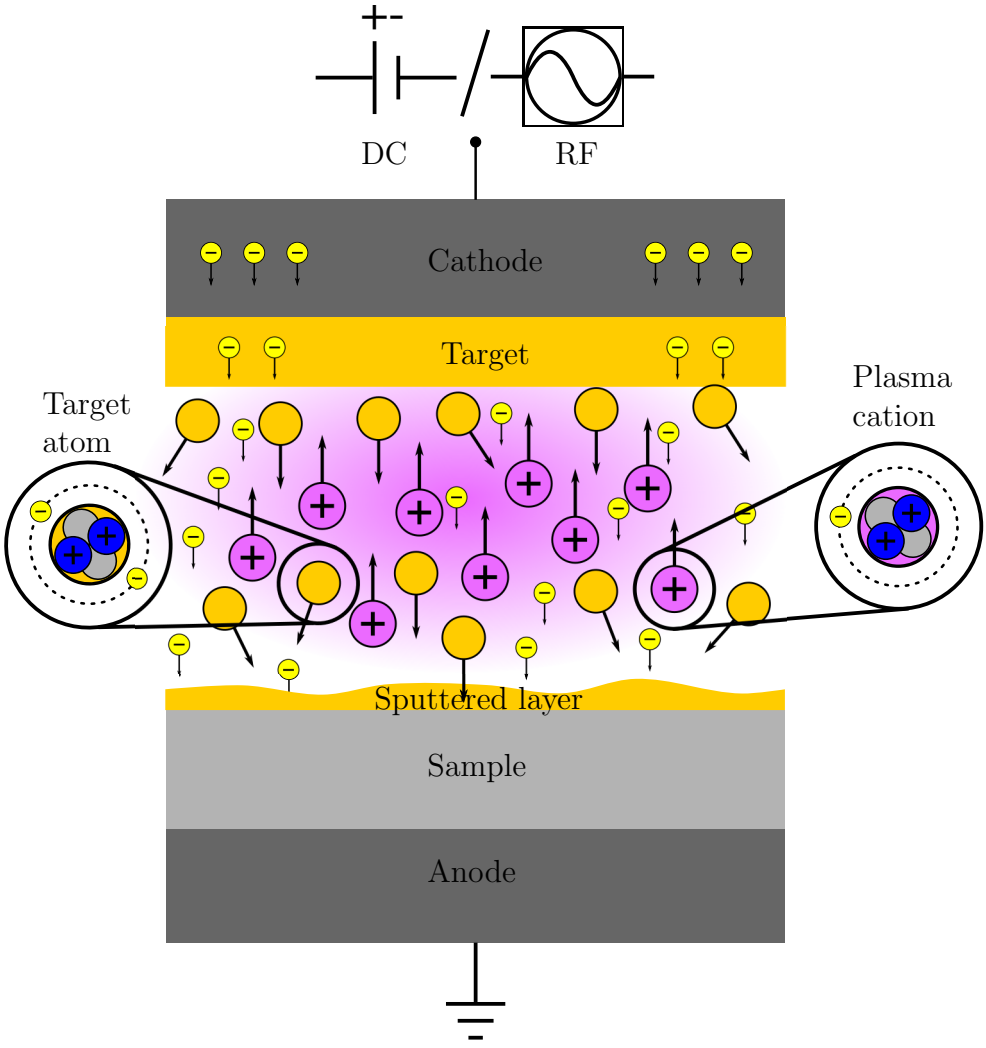

Figure 9: Schematic image of the sputtering deposition process.

ITO can be deposited by both DC and RF sputtering. Here, DC sputtering has been used for metals and RF sputtering for ITO. The difference between the systems is how the bias is applied. In DC sputtering, a negative bias is

applied to the cathode where the (metallic) target is. Electrons in the target gain enough energy to leave it and accelerate toward the anode. On their way, they collide with and ionize Ar gas atoms. The emitted electrons are accelerated and may also ionize more Ar atoms. At a high enough power and Ar pressure this ignites the Ar gas into a plasma, and the positive Ar ions in turn accelerate toward the cathode where the target sits (Fig. 9).

DC sputtering requires conductive, usually metallic targets. RF sputtering on the other hand has the ability to sputter *both* metallic and dielectric targets. In RF sputtering, a time-varying MHz potential applied to the cathode induces another time-varying potential on the opposite side of the target. Again, the plasma is ignited by stray electrons. During positive half-cycles of the RF bias, electrons accumulate on the target surface as they are much lighter than the Ar cations. Eventually, the target surface becomes negatively charged such that electrons are repelled from it and no net charge arrives at the target. Ar cations accelerate towards the target and transfer their momentum to target atoms that are sputtered in all directions [39]. An improved version of the RF sputtering system is the RF magnetron cathode setup. Here, a magnetic field is applied perpendicular to the electric field that is oriented normal to the cathode. The magnetic field causes the electrons to travel in a spiral instead of in a straight line, increasing chance of Ar ionization, plasma density, and hence deposition rate [20].

A critical condition to consider in PVD is the directionality of the deposition material vapor. High aspect ratio patterns in the resist suffer from the risk of becoming sealed before enough material is deposited onto the substrate if the deposited atoms impinge from random directions (Fig. 10 B). In the subsequent lift-off step, the resist including its sidewalls is entirely covered by the deposited material and solvent cannot reach the resist. This leads to patterns with higher side walls and usually poor pattern resolution or lift-off may not be feasible at all [20, 53]. Strategies to improve the directionality of the vapor is to increase the distance between deposition material and the sample and/or collimate the vapor beam. In both cases, only atoms arriving at an angle close to the sample normal will reach the sample [39]. Evaporation has an inherently higher directionality during deposition; the atoms tend to flow in a straight line, whereas atoms are ejected at all angles from the target during sputtering. In the sputterer reactor, the pressure is higher due to the presence of the plasma, and collisions between sputtered atoms and plasma particles further increases the non-directionality [54].

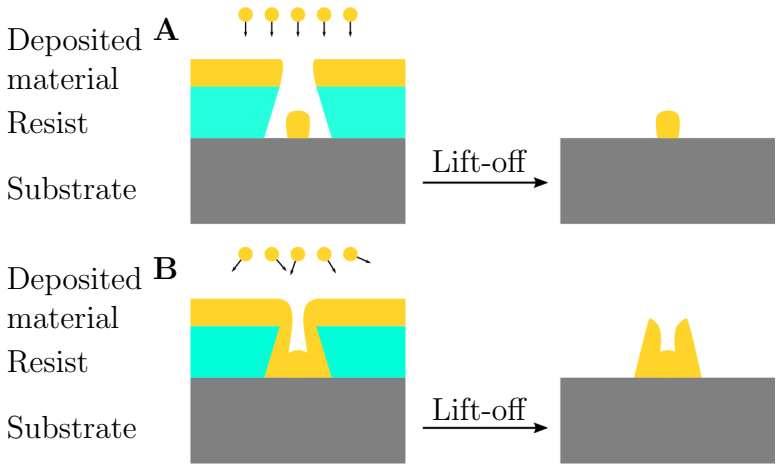

Figure 10: (A) Material coverage of patterned resist and after lift-off for directional deposition and (B) non-directional deposition.

In this project, thermal evaporation has been utilized to deposit 20 nm/100 nm Ni/Au layers; magnetron sputtering has been utilized to deposit 3.5 nm/5.5 nm Ni/Au layers (DC sputtering) and 100 nm to 150 nm ITO layers (RF sputtering). While sputtering is superior in terms of material quality and vacuum constraints, the ease, speed and directionality of thermal evaporation justifies its use for the thicker Ni/Au metal layers.

2.3.3 Lift-off

The final processing step that completes the pattern transfer is lift-off. In lift-off, the sample, now covered in the deposited material, is immersed into a liquid solvent that dissolves the remaining, non-exposed resist and thereby washes away unwanted material, ideally leaving behind the high resolution material patterns. Acetone is the solvent of choice for many resists, including PMMA, because it is cheap and easy to work with. The resist dissolving can be sped up by carefully heating the acetone.

For a successful lift-off, it is imperative that the solvent can access as much resist as possible. A discontinuity in the deposited material ensures this. The discontinuity can be realized in several ways. The importance of directionality of the deposition method has already been discussed. The slanted

side-walls of the patterned resist (Fig. 10), realized by broadening of the electron beam are, despite being a resolution limiting factor, actually beneficial for lift-off: the so-called *undercut* aides discontinuity in the deposited thin film, especially for directional deposition. In non-directional deposition, the sidewalls eventually become covered in material as Fig. 10 B demonstrates, but for thin deposited layers (or thick resists), there may still be an effective discontinuation of the deposited material. Thus, strategies for effective lift-off is to have a thick resist (or conversely a thin deposited layer), a large undercut and/or directional deposition. Moreover, by using a lower acceleration voltage in the EBL patterning step, the beam broadens more in the resist, enabling a larger undercut, at the expense of lower pattern resolution. A higher electron dose will also help to accomplish a good undercut while maintaining the same resolution at the very top of the pattern where the beam hits the resist (Fig. 8) [20].

3 Materials and methods

This section describes in detail the methodology including equipment used to fabricate, measure and investigate devices.

3.1 Nanowire device fabrication

The strategy to transfer a nanoscale contact pattern to single NW devices on a substrate is schematically outlined in Fig. 6 A—I. A number of different NW devices were fabricated to assess the contact quality of metal and ITO contacts. We call a chip with devices a sample where a device consists of an InAs NW with two our four electrodes that electrically connect the device to Au pads on a Si/200 nm SiO_2 chip with 24 100 µm×100 µm fields. Micrographs of a device chip and a field is seen in Fig. 11.

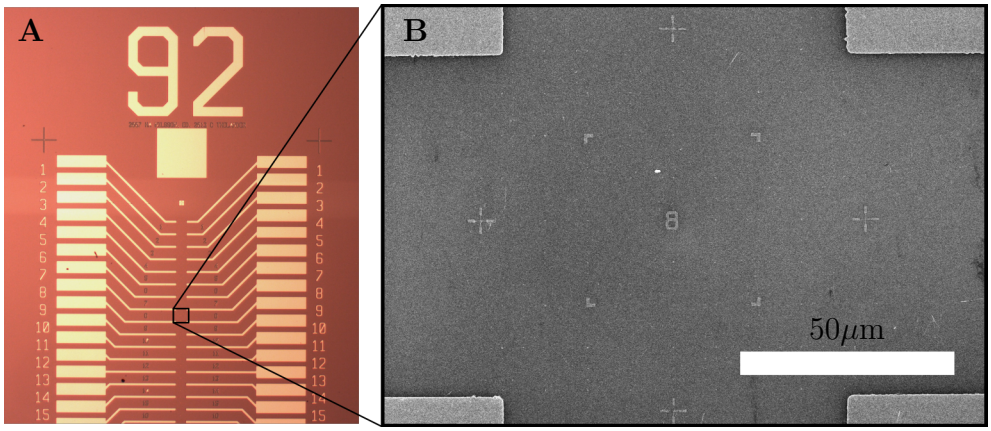

Figure 11: (A) Optical micrograph of a 24 pad measurement chip used to contact devices, showing the 15 first fields and (B) a SEM micrograph of a field where Au contact pads are seen in the corners.

The first step in the fabrication was to transfer NWs from a growth substrate to the measurement chip. The InAs NWs utilized here were grown via chemical beam epitaxy (CBE) in LNL by Sören Jeppesen et al., see Refs. [55, 56] for details. The measurement chip was first cleaned for five minutes in an ultrasonic acetone bath (40 ml; Sigma-Aldrich), rinsed in IPA (20 ml; Sigma-Aldrich) for 20s, blow dried with a N_2 gun and plasma ashed for 30s

in an O_2 plasma to remove organic residues. Transferring the NWs to the measurement chip was accomplished by carefully scraping the growth substrate with a piece of clean room paper: NWs would break off of the growth substrate and stick to the piece of paper. When the paper was tapped on the measurement chip, some NWs stuck on the paper would adhere to the measurement chip by van der Waals forces. An Axioplan optical microscope (Zeiss) operated in dark field mode was used to confirm the presence of wires in the fields on the measurement chip.

In order to design contacts for the EBL software, the exact location of the NWs on the chip had to be known. Each field on the chip had its own xy coordinate system, which can be seen as the small dots in Fig. 12 B. The origin (0, 0) is at the very center of the field, here hidden by the 3 in Fig. 12 A. The shortest vertical and horizontal distance between two adjacent dots is 2.5 µm, and a larger marking is found at every 10 µm. A real example of assigning coordinates to the grid dots is seen in Fig. 12 B. By this system, the exact location of the NWs in the coordinate system was easily acquired by imaging suitable NWs on each field of the measurement chip. A Hitachi SU8010 SEM operated at 20kV V_{acc} and a current of 10 µA was used for this purpose. The SEM micrographs are fed into a custom LabVIEW program by Claes Thelander. The program was used to assign coordinates to the NWs with the help of the dot grid and then generated the desired contact patterns that would be used in the EBL software. Note that one NW per field could be contacted, consequently it was sufficient to locate and assign coordinates to one NW per field.

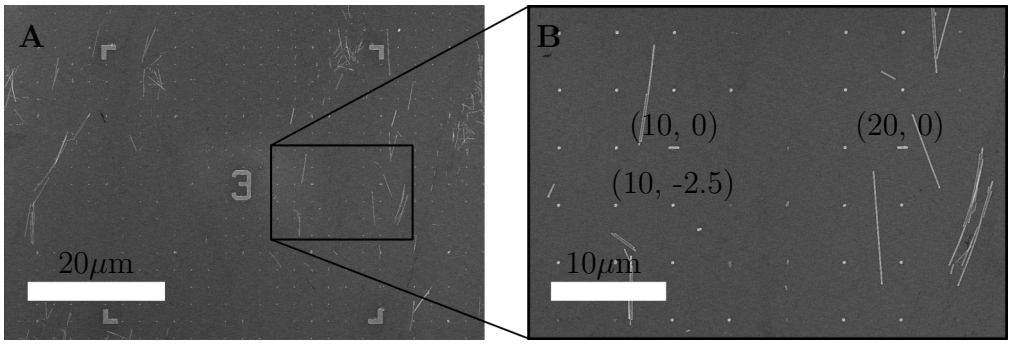

Figure 12: SEM micrographs to locate NW positions on the measurement chip.

After the chip has been imaged in the SEM, the chip was spin coated with a PMMA 950K A5 resist. 950K indicates that the average polymer chain has a molecular weight of 950×10^3g/mol and A5 means that the polymer concentration in the solvent A (anisole) is 5%. A higher polymer concentration will for a given spin speed result in thicker resist layers. The A5 resist is popular among many groups at LNL and was chosen because optimized processing schemes were present for it.

The chip, vacuum fastened to the spinner, was covered in liquid resist solution. Three different spin speeds were tested to optimize the lift-off process and pattern resolution. These were 3000, 4000 and 5000rpm for 60s, generally with an acceleration of 1500rpm/s. After spinning, the chip was immediately transferred to a hotplate and baked at 180 °C for five minutes to evaporate solvent and harden the resist (Fig. 6 B). Polymer residues on the back of the chip were carefully scraped away to ensure that the chip was as flat as possible — this was very important to ensure an even exposure in the EBL.

In the EBL exposure step (Fig. 6 C), the chip was mounted on the chip holder and inserted into a load lock before being inserted into the evacuated EBL chamber. The system used was an EBL Raith 150 system with a thermionic field emission gun. V_{acc} was set to 20kV which gave a decent trade-off between pattern resolution and undercut. To increase resolution further, the aperture size was set to 10 µm to reduce the beam current.

After EBL exposure, the sample was developed by stirring it in a 1 : 3 MIBK:IPA solution (20 ml) for 90s to remove the exposed resist patterns (Fig. 6 D) and then rinsed in pure IPA (20 ml) for 20 seconds and blow dried with a N_2 gun. The procedure was completed by ashing polymer fragment residues in the developed patterns for 30s in O_2 plasma at 5mbar pressure (Fig. 6 E) in a Plasma-Preen System II 862 system (Plamatic System Inc.). Before material deposition, the oxide layer present on the surface of any III-V NW had to be etched away to achieve a good electrical connection to the contact material. Ammonium polysulfide ($(NH_4)_2S_x$) based processes have been successfully implemented for etching oxides and passivating the surfaces of InAs NWs [57] and were used in this work. The chip was inserted into a 40 °C solution of 100 µl to 150 µl diluted 20% $(NH_4)_2S_x$(Sigma-Aldrich) and 10 ml to 20 ml deionized water for two minutes.

Immediately after surface passivation, the sample was transferred to the deposition systems for material deposition (Fig. 6 G). The deposition systems

used in the thesis were a low-pressure AVAC evaporator for depositing Ni/Au (20 nm/80 nm) and an AJA Orion 5 sputterer with three RF-magnetron sources and two DC sources for depositing ITO or Ni/Au/ITO. Pumping down the evaporator chamber required 2—3 hours as the system lacked a load lock. Appropriate settings for the thickness monitor were set depending on the material to be evaporated. Evaporation was initiated by increasing the current through one material boat at a time until the sufficient material deposition occurred. When enough material had been deposited, evaporation was interrupted by inserting an aperture and ramping down the current.

The sputterer had a load lock that only required 10 to 15 minutes to pump down. DC magnetron cathodes were used to sputter Ni/Au and an RF magnetron cathode was used to sputter ITO. After setting the thickness monitor to the desired material, Ar was pre-flown at 9 sccm/min for 2 minutes to rid the chamber of pollutants. Then, the Ar flow was lowered to 3 sccm/min and the DC/RF cathode power was set to 50W to ignite the plasma. After plasma ignition, Ar flow was increased to 4 sccm/min (ITO) or 9 sccm/min (Ni and Au). Cathode power was ramped for 90 seconds to 150W and 75W for Ni and Au respectively, while it was kept at 50W for ITO. The targets were pre-cleaned (sputtered) for five minutes (ITO and Ni) or 30 seconds (Au) before opening the shutters to initiate material deposition onto the sample. During deposition, plasma pressure was about 1.2mTorr for ITO and 2.4mTorr for Ni and Au. The deposition rates varied greatly between the materials: for ITO, it was about 0.3—0.4Å/s; Ni and Au had about one order of magnitude higher deposition rates. In all cases, R_{dep} was significantly lower than evaporation. 100 nm to 150 nm thick layers of ITO were deposited, requiring 40—60 minutes deposition time. The very thin layers of 3.5 nm/5.5 nm Ni/Au required only a few seconds of deposition however, which made precise thicknesses hard to achieve.

After deposition, the sample was removed from the deposition system, and its edges were carefully scraped with a scalpel to remove the material covered resist on all four sides. This increased the chance of a successful lift-off as the solvent now had a larger area to dissolve the resist from. In the lift-off step (Fig. 6 H), the sample was immersed in an acetone beaker (20 ml) heated to 50 °C for 15 minutes. The sample was then transferred to a fresh acetone beaker (40 ml) at room temperature, where the sample was sprayed in the acetone with a pipette to remove remaining resist. Finally, the sample was rinsed in an IPA beaker (20 ml) to remove the acetone and blow dried with

a N_2 gun.

3.2 Process optimization: dose testing

As thoroughly described in Sec. 2.3.1, a large number of processing parameters influence the final material pattern resolution in EBL patterning. The simplest and in some ways most important parameter that can be changed is the electron dose during the EBL exposure step; the electron dose affects mainly the size distribution of resist polymer fragments and thereby the undercut (Fig. 8). As argued in Sec. 2.3.2 and 2.3.3, a large undercut is crucial especially for non-directional deposition such as sputtering to achieve a good lift-off. However, a large undercut may lower the pattern resolution in sputtering as the entire base of the resist pattern is covered in material. This means that e.g. contact lines will be much wider than what was originally designed, which may be detrimental for small devices such as NWs. To correct for this, the processing procedure described in Sec. 3.1 was performed for chips without NWs, where straight lines of varying width were patterned with different electron doses. After deposition and lift-off, the lines were inspected in the SEM. This is called dose testing and it serves two purposes. First, we can use the data to construct calibration curves for the doses. For instance, this may show that for a dose of $300\,\mu C\,cm^{-2}$ a designed line width of 200 nm may give 300 nm wide lines. For designs where accurate resolution is important, such information is crucial. Second, the dose testing may show where lift-off is not possible. For example, dose testing may show the smallest achievable resolution for some dose or at which dose the process does not work altogether.

Here, dose testing was performed at two different resist thicknesses corresponding to resist spinner speeds of 3000 and 4000rpm. Lines with designed widths of 40 nm to 320 nm where patterned in the Raith 150 EBL system with doses between $200\,\mu C\,cm^{-2}$ to $500\,\mu C\,cm^{-2}$ by changing the electron beam exposure time (which was automatically calculated by the software). Deposition and lift-off were performed as described in Sec. 3.1. Dose testing was done for 100 nm and 150 nm ITO thicknesses. The material lines in the micrographs were inspected in the SU8010 Hitachi SEM and the measurements of the lines were done with the software ImageJ.

3.3 Electrical measurements

With the fabrication finished, it was possible to achieve electrical contact to the NW devices via the macroscopic Au contact pads seen in Fig. 11 A. The two measurement setups mainly utilized, Setup A and B, required wire bonding the gold contact pads to a larger chip. The bonder tool (model K&S 4523) used ultrasonic power to melt the tip of a 25 µm in diameter Al wire threaded through a wedge needle. The Al wire sticked to the contact of the bigger chip and the needle was aligned with the sample. Ultrasonic power was used to fasten the metallic thread on the sample contact pad and to cut the thread, completing the wire bond. This established a reliable electrical connection between the larger chip contact pad and the smaller sample contact pad, but sacrificed speed and flexibility in the measurements. This was because only two to four of the 12 to 24 devices on the sample could be wire bonded to the larger chip at a time; after they had been measured, their wire bonds had to be removed before other devices could be wire bonded.

In Setup A a Yokogawa GC200 DC Voltage/Current Source was used to source voltage with high resolution to the samples. Because the output currents were small, in the range of pA to µA, they were amplified by a FEMTO DLPCA-200 Low Noise Current Amplifier with variable gain that converted the current signal to a voltage that was easier to read by the Keysight 34401A $6\frac{1}{2}$ Multimeter. Setup A could only perform two-point probe IV measurements. Four-point probe measurements, Hall measurements and van der Pauw measurements were performed in Setup B that had a Keithley 2602 System Sourcemeter that sourced voltage with high resolution through the outer contacts of four-point devices with SMUs, which means current could be read simultaneously. The voltage drop between the inner probes was measured by a Keithley 6514 System Electrometer that had a input impedance of 200 TΩ. The Keithley 2602 and 6514 were connected to a Keithley 7002 Switch System that could be programmed to do several measurements sequentially on different devices with a MATLAB program by Olof Hultin.

4 Results and discussion

4.1 Dose testing

A selection of SEM micrographs of straight 100 nm thick patterned ITO lines from dose tests for two different spin coating speeds (corresponding to different resist thicknesses) and targeted line widths of 40 nm (top lines) and 80 nm (bottom lines) are shown in Fig. 13. The processing was performed as described in Sec. 2.3 and 3.2 by EBL patterning of PMMA resist spun on empty Si/SiO_2 device chips, sputtering ITO and lift-off. Many more micrographs of different line widths and doses between 200 µC cm^{-2} to 500 µC cm^{-2} were acquired but would be too exhaustive to present here.

Dose testing is rather tedious and repetitive work but gives important insights to the processing. As evident from Fig. 13, EBL patterning of ITO lines does indeed work with the basic processes explained in Sec. 2.3 and Sec 3.2, at least for these resist thicknesses (spin coating speeds). The white high-contrast residues on the edges of the lines in Fig. 13 clearly show that the sidewalls of the resist were covered in sputtered ITO. It is speculated that the ITO on the resist sidewalls adhere too strongly to the ITO lines to be removed in the lift-off step. If the ITO was thicker or the resist thinner, it is possible that lift-off would not be feasible. Indeed, the top lines for 3000rpm and 4000rpm with a target width of 40 nm are completely absent for the 220 µC cm^{-2} dose in Fig. 13, suggesting they were washed away in the lift-off step, perhaps due to strong adhesion to the resist sidewalls.

Fig. 13 also shows that resolution is hampered by the low directionality in sputtering deposition as all the actual line widths strongly deviate from their target widths of 40 nm and 80 nm. The actual measured widths are plotted as a function of the corresponding target widths in Fig. 14 for the 100 nm thick ITO lines.

The overall trend in Fig. 14 is clear: the lower the dose, the thinner ITO lines achievable and the closer to the designed line widths the measured line widths become. This is crucial for designing a certain contact dimension, in that case, Fig. 14 can be used as a calibration curve. We note that most doses yield line widths that deviate significantly from the designed width, which is probably due to the non-directional sputtering that deposits

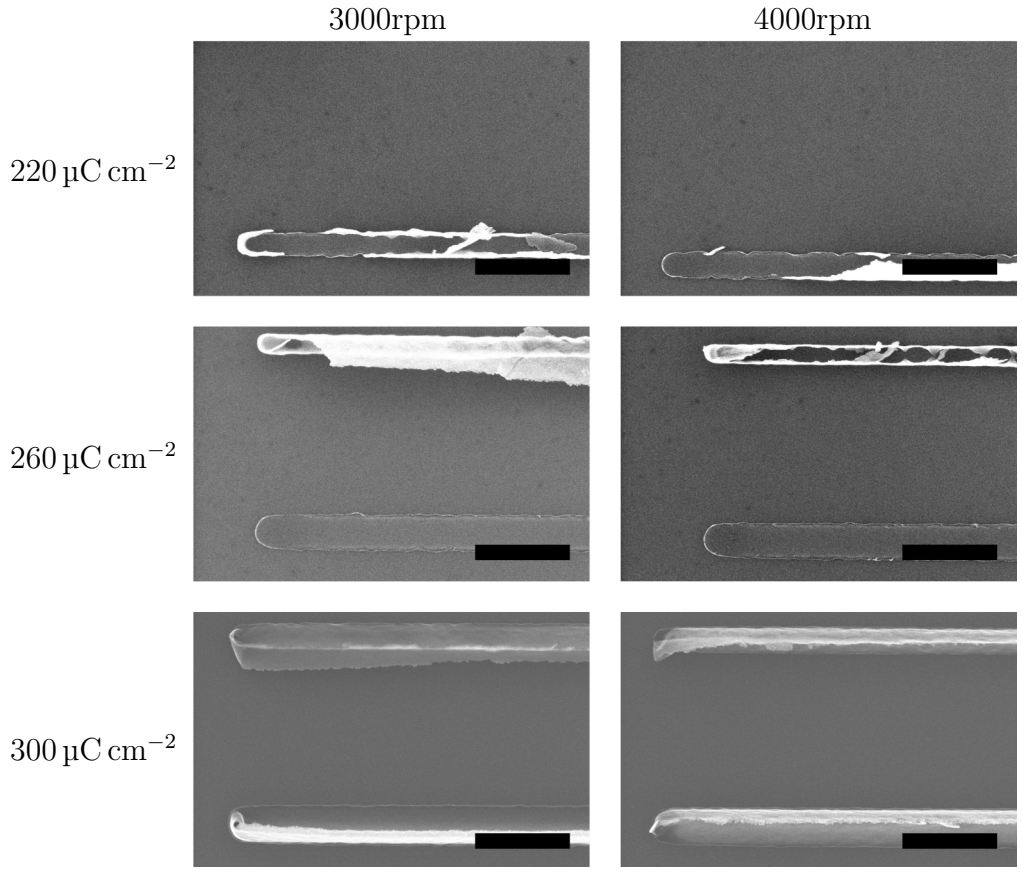

Figure 13: SEM micrographs of straight 100 nm thick ITO lines used for dose testing. Targeted line widths are 40 nm (top line) and 80 nm (bottom line) in all micrographs. Scale bars 500 nm.

material beneath the undercut (Sec. 2.3.1, 2.3.3 and Fig. 10). The lowest doses (220 µC cm^{-2}) cannot pattern the smallest features. This is either 1) because the dose is insufficient to fully expose the resist or 2) because the ITO adheres to the patterned resist so well that it is washed away in the lift-off step due to the high fraction of surface being in contact with the resist instead of the substrate.

100 nm ITO thickness was chosen because it is a common layer thickness for patterned metal contacts to NWs used in this work, that is, NWs with a diameter of 60 nm to 70 nm. However, thicker ITO layers have beneficial

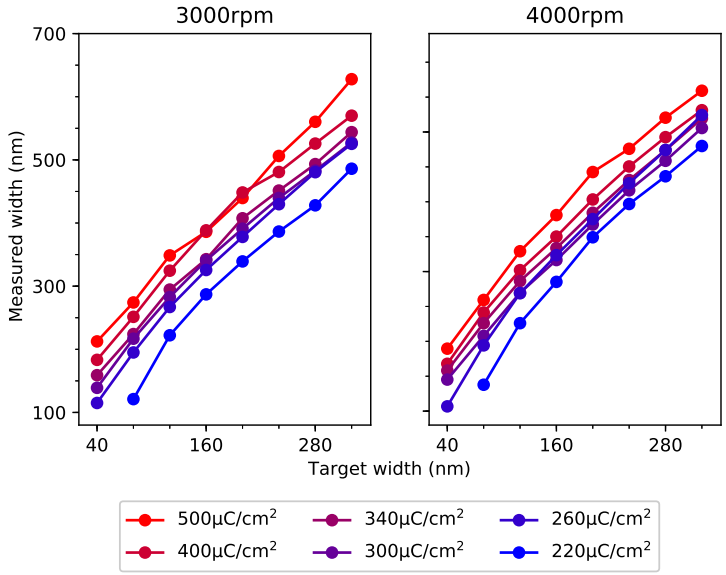

Figure 14: Dose test for 100 nm thick ITO lines.

electrical properties (Sec. 2.1), which is why the dose test performed for 100 nm (Fig. 13 and 14) ITO was repeated for 150 nm thick layers: a selection of the results are shown in Fig. 15.

Fig. 15 shows that lift-off was possible for 150 nm ITO as well, with the same resist thicknesses corresponding to resist spinning at 3000 and 4000rpm. The results of measuring the 150nm ITO lines are shown in Fig. 16.

According to Fig. 16 it seems that a higher line resolution is achievable for 150 nm sputtered ITO. It may be related to fine tuning parameters in the EBL, but shows, for the first time, that sub 100 nm resolution is achievable for patterned ITO. The failure to pattern designed widths thinner than 120 nm at 240 µC cm^{-2} for 3000rpm resist in Fig. 16 could be related to the larger ITO sidewalls seen in Fig. 15: the 3000rpm resist is thicker than the 4000rpm resist, and more of the sidewalls of the ITO lines are in contact with the thicker resist sidewalls. In the lift-off step, the shearing forces from the thicker resist on the thinnest lines are higher than the shearing forces exerted by removing the thinner resist. Consequently, the thinnest ITO lines patterned with the thicker resist may stand a higher risk of being removed altogether

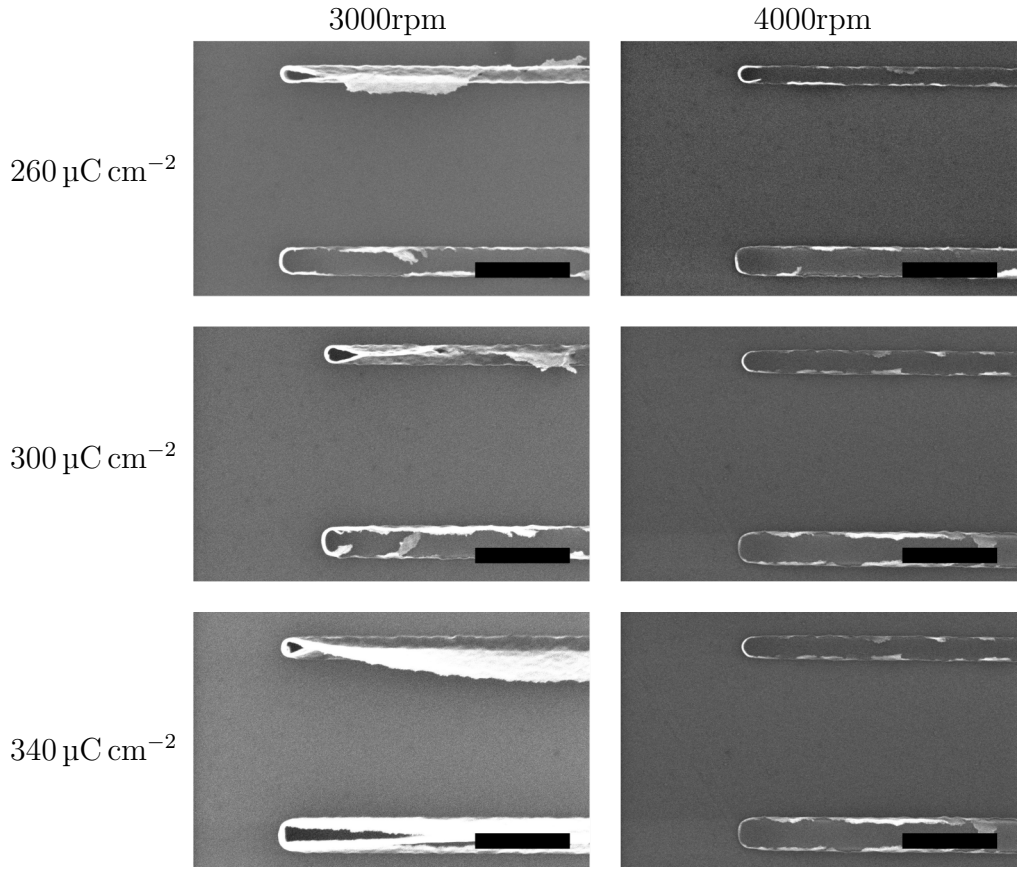

Figure 15: SEM micrographs of straight 150 nm thick ITO lines used for dose testing. Targeted line widths in all images is 40 nm and 80 nm. Scale bars 500 nm.

in the lift-off process than ITO lines patterned with the thinner resist.

After comparing the results in the plots and micrographs shown, a resist thickness corresponding to 4000rpm with an electron dose of 300 µC cm^{-2} was chosen as main parameters for subsequent processing due to its high reliability and quality lines. For the 100 nm thick ITO contacts used to contact NWs in subsequent samples, Fig. 14 was used as a calibration curve to attain desired contact widths.

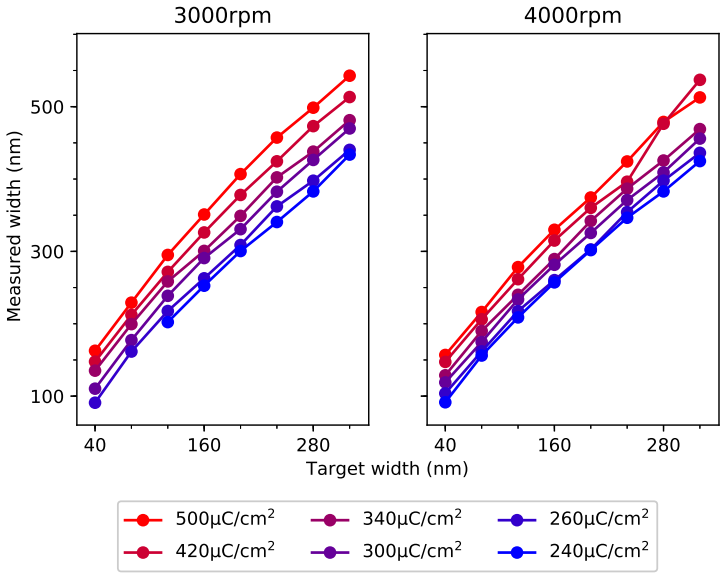

Figure 16: Dose test for 150 nm thick ITO lines.

4.2 Electrical properties of sputtered ITO

Electrical properties of 100 nm thick ITO and 3.5 nm/5.5 nm/100 nm Ni / Au / ITO sputtered on thin glass substrates were investigated by van der Pauw (Sec. 2.2.4) and Hall measurements (see e.g. Ref. [58]). A schematic image of the square sample geometry with the four electrical contacts in the corners is seen in Fig. 5. Van der Pauw measurements were first performed to attain a value of R_S, followed by Hall measurements from which carrier concentrations and mobilities were extracted. Table 1 summarizes the electrical properties of several sputtered samples measured on glass substrates. Note that only R_S and ρ was measured for the Ni/Au/ITO sample as for stacks of materials, there is some ambiguity as to which material's carrier concentration and mobility is being measured.

Table 1 provides valuable information on how well the sputtered materials performed. It shows especially that the sputtered ITO material has a high electrical quality comparable to figures found in literature [17, 18, 31, 59, 60], and that they are improved somewhat by the 30 min annealing scheme in 200 °C N_2. It is expected that a tougher annealing recipe would improve

Table 1: Electrical properties of sputtered glass samples

	A	B	C	D
Material	ITO	ITO	Ni/Au/ITO	Ni/Au/ITO
t (nm)	100	100	3.5/5.5/100	3.5/5.5/100
Annealed	No	Yes	No	Yes
R_S (Ω/square)	64.2	55.3	25.3	20.3
ρ ($\Omega\,$cm)	6.42×10^{-4}	5.53×10^{-4}	2.76×10^{-4}	2.21×10^{-4}
n (cm^{-3})	4.12×10^{20}	4.25×10^{20}	x	x
n_s (cm^{-2})	4.12×10^{15}	4.25×10^{15}	x	x
μ_{Hall} ($\mathrm{cm^2V^{-1}s^{-1}}$)	23.6	26.5	x	x

electrical properties further, but the temperature was intentionally kept low to avoid damage to subsequent samples with InAs NWs. We see for instance in Table 1 a very high carrier concentration on the order of $10^{20}\,\mathrm{cm}^{-3}$ that seems to increase with annealing, just as expected from theory in Sec. 2.1. A high carrier concentration is promising for making good electrical contact to InAs, but simultaneously bring drawbacks in the form of decreased carrier mobility for ITO relative other semiconductor materials and consequently a relatively high sheet resistance. A high R_S is disadvantageous for long, narrow contacts.

The values of R_S in Table 1 are for large samples. It is conceivable that contacts with widths on the micro and nanoscales behave differently. To investigate the influence of line width on the sheet resistance of the ITO contacts, resistance measurements of 100 nm thick ITO EBL patterned lines of varying widths were taken in Setup A. After a resistance R was measured for each patterned ITO line, the actual lengths l and widths W of the ITO lines were measured with the SEM to calculate R_S by rearranging Eq. 6 to $R_S = R \times W/l$, which is plotted for the line widths before and after annealing at 200 °C in N_2 for 30min in Fig. 17.

Fig. 17 shows a strong correlation between ITO line width and sheet resistance R_S. R_S decreases rapidly to a roughly constant value at $90\,\Omega$ with increasing ITO line width. Annealing decreases this value to about $80\,\Omega$. This shows an important drawback of patterned ITO contacts: while narrow contact lines suitable for nanoscaled samples such as NWs are feasible to pattern with EBL, their electrical properties are hampered with decreasing ITO line width. If we consider the resistivity of the contacts $\rho \propto R_S$ (Eq. 6), it is likely that the mobility μ (Eq. 7) is lowered by decreasing the ITO

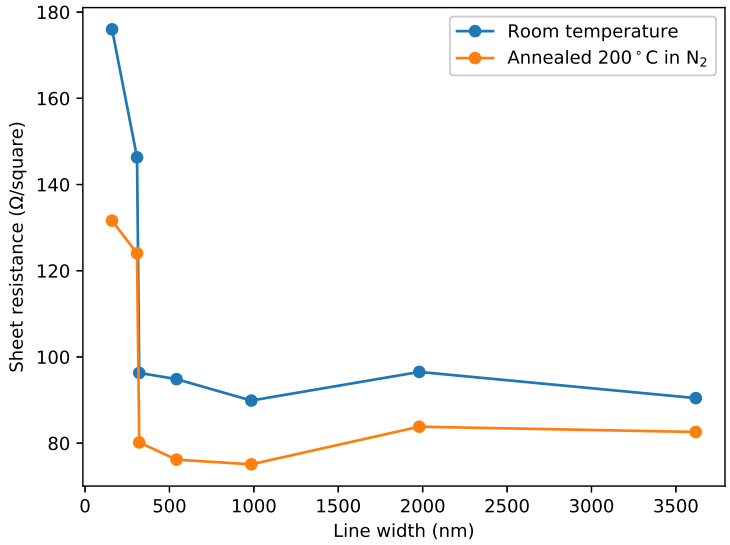

Figure 17: Sheet resistance of patterned ITO lines before and after annealing.

line width. While the carrier concentration n should be invariant to the line dimensions, narrower contacts have a higher surface to volume ratio i.e. more surface where electrons can scatter, which hence may decrease carrier mobility. The patterning of ITO may also affect the grain size distribution in the polycrystalline material. Smaller grain sizes, for instance, would increase the carrier scattering and lower the mobility too.

4.3 TLM measurements of patterned contacts

4.3.1 Sputtered ITO contacts

To assess the electrical contact quality of 100 nm thick ITO contacts on InAs NWs, several transmission line samples based on the three NW device designs described in Sec. 2.2.3 and Fig. 2 were prepared and measured in Setup A and B. The two first TLM designs (Fig. 2 A and B) were found to provide very unreliable results that were hard to interpret. A frequent device failure was also observed for samples utilizing these designs: for instance, single ITO

contacts would often break in devices designed according to Design 2 (Fig. 2 B). An example of a device designed according to Design 2 with a broken contact is shown in Fig. 18.

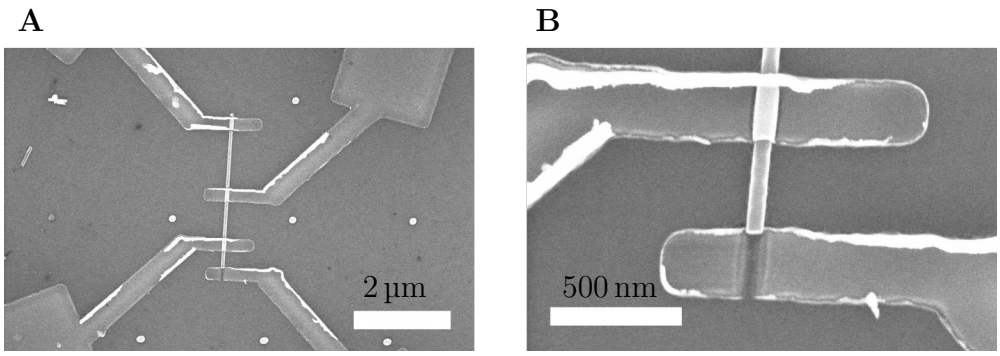

Figure 18: (A) SEM micrograph of a broken device from Sample 3 and (B) a zoomed in SEM micrograph of the broken contact.

Fig. 18 A is an example of what a device looks like in the SEM. The micrograph demonstrates the precision of the EBL patterning: all contacts are perfectly aligned with the InAs NW. A part of the InAs NW has been broken off at the bottom contact. What might be the cause of this? After sputtering, the ITO will be thicker wherever it covers parts of the NW (Fig. 19 A). In the lift-off step, that ITO may stand a higher risk of being removed with the resist. If the ITO adheres strongly enough to the NW, the part of the wire covered by ITO may be ripped off along with the ITO (Fig. 19 B).

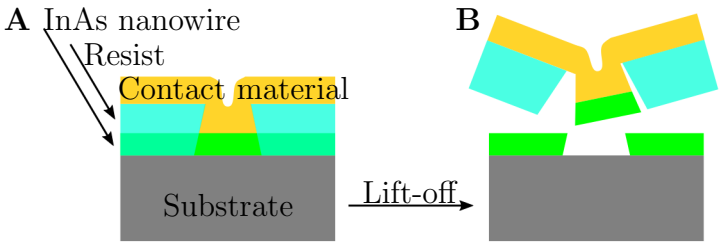

Figure 19: Schematic images showing how a contact and nanowire might break during lift-off.

One positive consequence of contact breakage was that micrographs such as Fig. 18 B allowed for a direct observation of how much of the circumference of

the NW that was covered by the ITO. The information can be used to correct the transfer length L_T in Eq. 10 to obtain a more accurate value of ρ_C. A closer inspection of Fig. 18 B revealed that the ITO covered about 90% of the wire, which is a fortunate consequence of the non-directional sputtering deposition. Directional deposition such as thermal evaporation is expected to cover a significantly smaller part of the NW. In Ref. [44] they estimated that 75% of the NW circumference is covered by evaporated material. Hence, using the derivation of R_C in Ref. [44], we update L_T to $L_T = \sqrt{\frac{r_{\mathrm{NW}}\rho_C}{0.9\times 2\rho_{\mathrm{NW}}}}$, which we can plug into Eq. 10 to numerically solve for a more accurate value of ρ_C.

While alterations of the two first TLM designs may be useful for other NWs to measure ρ_C, they were abandoned in favor of Design 3, which was the four-point probe device design (Fig. 2 C). Two-point probe and four-point probe IV measurements of the four best devices from such a sample (Sample 1) are shown in Fig. 20.

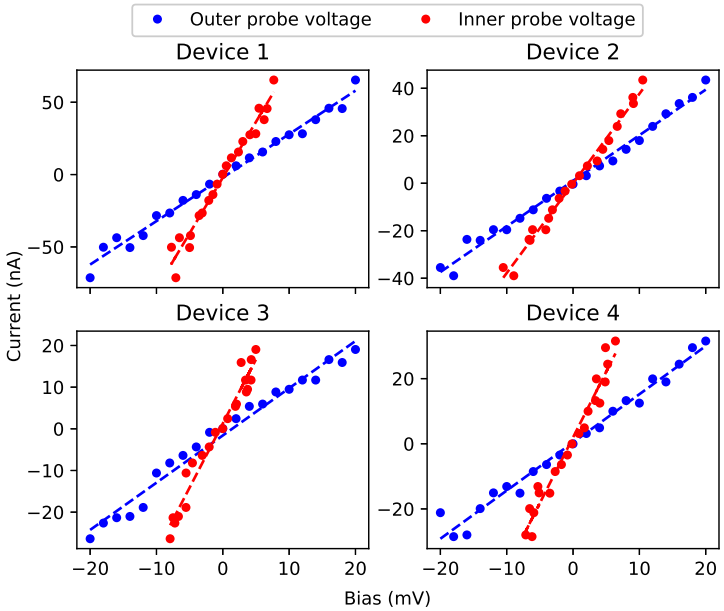

Figure 20: Two-point probe (blue) and four-point probe (red) measurements with linear regressions (dashed lines) of ITO contacts on single InAs NW devices from Sample 1.

In Fig 20, linear fits have been made to extract the resistance R_{23}, i.e. the resistance between the inner contacts 2 and 3, from the four-point data (red dots), and the resistance R_{14}, i.e. all the resistances in the device as seen in Fig. 4, from the two-point data (blue dots). By imaging the devices in the SEM to extract its dimensions, we can use Eq. 16 to attain a value of R_C for each device, which in turn can be used in Eq. 10 to solve for ρ_C.

It was however found that using Eq. 16 directly to extract R_C yielded negative values of R_C. This most likely originated from the design of the two middle contacts in the four-point devices (Fig. 2 C): the contacts were designed relatively wide to make good electric contacts to the NWs, but in doing so, the width L of the inner contacts 2 and 3 were always wider than the transfer length L_T. The problem is that when $L > L_T$ (Fig. 21 B) current will leak through the contacts such that R_{14} is measured to be smaller than it in reality is [44]; large segments of the relatively resistive InAs NWs are practically shorted by the wide ITO contacts. When Eq. 16 is used, R_C becomes negative. This issue was not fully understood until after measurements and analysis of the samples. To compensate for the issue, Eq. 15 was modified to

$$R_{14} = 2R_C + R_{23}\frac{l_1^*}{l_2} + 2R_L \tag{21}$$

which just as before can be solved for R_C:

$$R_C = \left(R_{14} - R_{23}\frac{l_1^*}{l_2} - 2R_L\right)/2 \tag{22}$$

where l_1^* is the length of the NW segments not covered by the ITO contacts. If we call the length of the NW segment between contacts 1 and 2 l_{12}, the length of the segment between contacts 2 and 3 l_{23} and the length of the segment between contacts 3 and 4 l_{34}, l_1^* can be expressed as $l_1^* = l_{12} + l_{23} + l_{34}$ (Fig. 21 D). The difference between l_1 and l_1^* is explicitly shown in Fig 21 C and D.

In contrast to Eq. 16, Eq. 22 overestimates R_C because the non-zero resistive contributions from the shorted NW segments are neglected. This method thereby gives an upper value of ρ_C and has been used in the data analysis

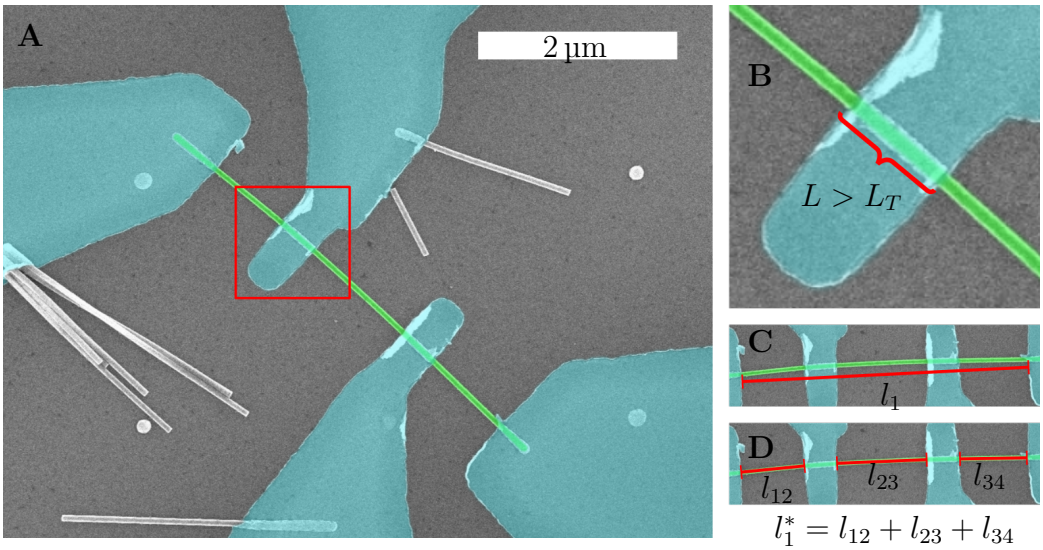

Figure 21: False colored SEM micrographs of a four-point device. (A) A four-point device. (B) The width L of a middle contact. (C), (D) Characteristic lengths l_1 and l_1^* are explicitly shown.

from the measurements on the four-point samples. The resistances in the four-point probe measurements are in more detail shown in Fig. 22.

In contrast to the previous circuit diagram depicting the resistances measured in the four-point probe method (Fig. 4), Fig. 22 decomposes the entire NW resistance into the resistive contribution from each NW segment between each pair of contacts where the NW segments have the lengths l_{12}, l_{23} and l_{34} as well as the NW segments under the middle contacts 2 and 3 of length L. In this picture, there are two resistors in parallel for the NW segments covered by the middle contacts 2 and 3: the NW segments beneath the contacts and the contacts themselves. If the resistive contribution from the contact, $R_{\mathrm{ITO}} + R_C$, is much smaller than the resistance of the NW segment beneath the contact, $\rho_{\mathrm{NW}} \frac{L}{\pi r_{\mathrm{NW}}^2}$, those NW segments will contribute with a much smaller resistance (i.e. $R_{\mathrm{ITO}} + R_C$) than the other NW segments. R_{ITO} is the (relatively small) resistive contribution of the ITO contact itself, in the order of a few times R_S of patterned ITO. For this reason, $l_1^* = l_{12} + l_{23} + l_{34}$ was introduced for Eq. 21. Because the resistance of the middle contact $R_{\mathrm{ITO}} + R_C$ is neglected in Eq. 21, R_C is overestimated when solving Eq. 21 for R_C.

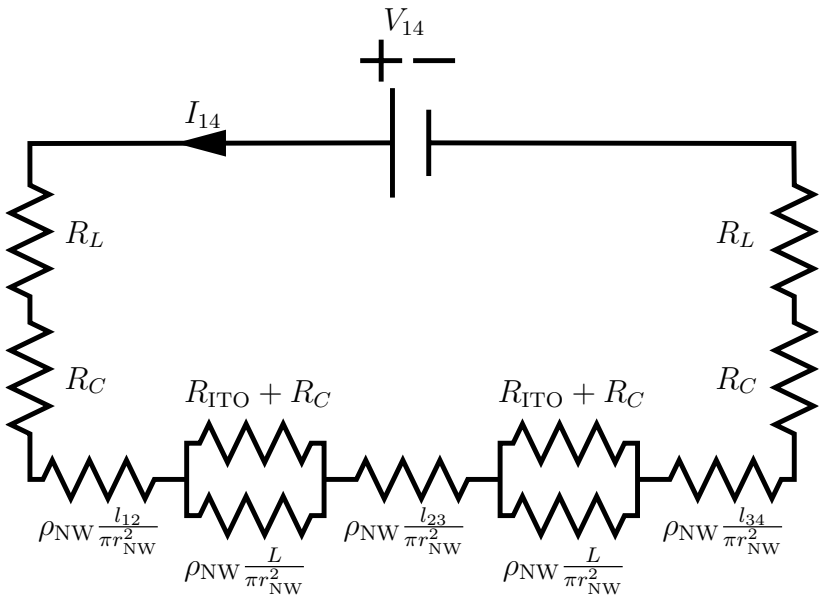

Figure 22: Equivalent circuit diagram depicting the resistances being measured in a four-point probe device measurement.

Extracted values of R_{14}, R_{23}, R_C and ρ_C for Sample 1 are presented in Table 2. 95% confidence intervals have been calculated for the fitted slopes in Fig. 20 from which R_{23} and R_{14} were calculated. With these intervals, lower and upper bounds of R_C for each device were extracted. The upper bounds were calculated by using the upper endpoints in the 95% intervals of R_{14} and the lower endpoints in the 95% intervals of R_{23} in Eq. 22 when calculating R_C. Conversely, the lower bounds of R_C were calculated by using the lower endpoints in the 95% confidence intervals of R_{14} and the upper endpoints in the 95% intervals of R_{23} in Eq. 22 to calculate R_C. The bounds of R_C have in turn been utilized to extract upper and lower bounds of ρ_C using Eq. 10. For the lower bounds of ρ_C, the lower bounds of R_C were used in 10. Because the lower bounds of R_C in turn were calculated using the upper endpoints in the 95% confidence intervals for R_{23}, those upper endpoints for R_{23} were used to extract an upper limit of ρ_{NW} which was used in Eq. 10 (remember, $R_{23} = \rho_{\mathrm{NW}} l_2 / \pi r_{\mathrm{NW}}^2$). Note that because Eq. 10 is nonlinear, the lower and upper bounds of ρ_C are not necessarily symmetric around its "average" value, i.e. the value obtained by using the best fitted values of R_{14} and R_{23} that were used to extract R_C. The confidence intervals of R_{14}

and R_{23}, and the bounds of R_C and ρ_C are shown in parentheses next to the average values (obtained from the best linear fits of R_{14} and R_{23}) in Table 2.

Table 2: Extracted resistances of Sample 1 from Fig. 20

	Device 1	Device 2	Device 3	Device 4
R_{14} (kΩ)	333 (314, 352)	521 (494, 548)	881 (815, 947)	676 (629, 723)
R_{23} (kΩ)	130 (119, 141)	265 (251, 279)	325 (293, 357)	248 (223, 273)
R_C (kΩ)	7.0 (-14.5, 29.5)	57.8 (33.9, 81.7)	134 (71, 197)	150 (108, 192)
ρ_C (Ωcm^2)	4.78×10^{-7} (-, 82.9)$\times 10^{-7}$	2.43×10^{-5} $(0.85, 4.38)\times 10^{-5}$	6.32×10^{-5} $(1.94, 11.3)\times 10^{-5}$	7.77×10^{-5} $(4.74, 10.8)\times 10^{-5}$

Because the lower limit of R_C for Device 1 is negative, no lower limit of ρ_C could be extracted. For this reason, Device 1 is excluded from the subsequent analysis. The average of ρ_C of the remaining devices in Table 2 based on the best linear fits of the IV data in Fig. 20 is $(5.51 \pm 2.25)\times 10^{-5}\,\Omega\text{cm}^2$, with a highest upper bound of $11.3 \times 10^{-5}\,\Omega\text{cm}^2$. To set the results into context, these values are quite good: they are lower than ITO contacts on n-GaAs NWs [48] and similar to ρ_C for ITO on planar n-GaN [50], which suggests a good ITO/InAs contact interface, probably due to the high carrier concentrations that were measured for the sputtered ITO (Table 1) as well as the high electron concentration expected for the InAs NWs. This is promising for realizing ohmic contacts to the InAs wires and ohmic characteristics are indeed supported by the linear shape of the IV curves in Fig. 20. With the exception of Device 1, all devices show positive, narrow ranges of ρ_C as calculated with the 95% confidence intervals of R_{14} and R_{23}. This suggests that the measurements are statistically reliable.

Despite low values of ρ_C, the contact resistances R_C are in the order of 100 kΩ which here is in the same order of magnitude as R_{23}, but probably too high for many applications. The high values of R_C are due to the small electrode area and would be significantly reduced for larger contacts and/or larger samples; the NWs used here are only about 60 nm to 70 nm in diameter.

A concern unveiled in Table 2 is the high value of R_{23}, i.e. the resistance between the inner contacts 2 and 3. For these types of degenerately doped InAs NWs, we should expect a NW resistance between 10 kΩ to 100 kΩ due to carbon n dopant incorporation during growth [55, 56, 61], but none of the

devices showed a NW resistance below 100 kΩ. One concern was that the surface passivation scheme with $(NH_4)_2S_x$ (see Sec. 3.1 and Ref. [61]) did not etch away all of the oxide on the InAs surface. A thin remaining surface oxide could explain the high value of R_{23} observed for Sample 1.

To test this hypothesis, Sample 2 was made with a smaller batch of six devices with ITO contacts that were fabricated just as previous samples, but with a stronger passivation solution of 150 µl $(NH_4)_2S_x$ in 10 ml water, about twice as strong as the previously used solution. The four-point probe measurements of the two best devices are presented in Fig. 23. Table 3 shows extracted resistances from the data including 95% confidence intervals of R_{14} and R_{23} and lower and upper bounds of R_C and ρ_C for each device.

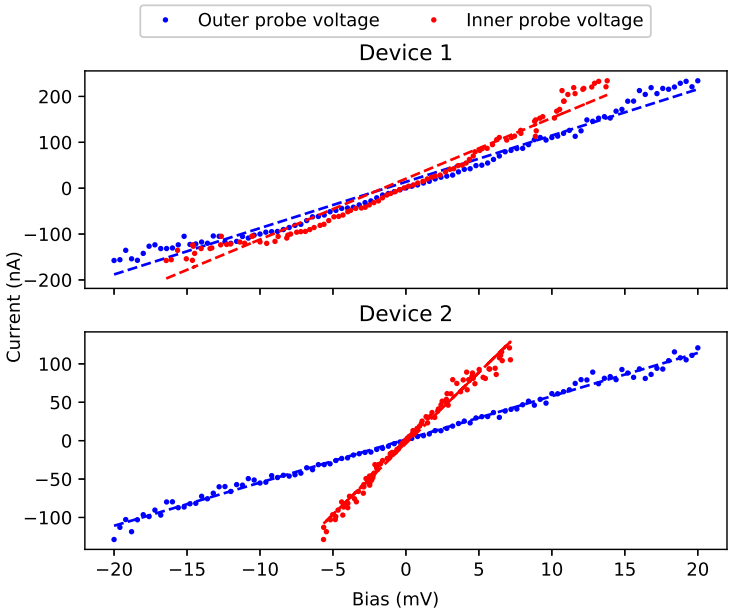

Figure 23: Two-point probe (blue) and four-point probe (red) measurements with linear regressions (dashed lines) of ITO contacts on single InAs NW devices with stronger surface passivation (Sample 2).

The summarized results in Table 3 suggest that increasing the concentration of $(NH_4)_2S_x$ in the passivation step was a reasonable decision as the resistances R_{14} and R_{23} were lower for these devices compared to the previous sample. Contact resistances were lower too; consequently, a record low

Table 3: Extracted resistances of Sample 2 from Fig. 23

	Device 1	Device 2
R_{14} (kΩ)	99.1 (96.2, 102)	178 (175, 181)
R_{23} (kΩ)	75.5 (72.5, 78.5)	54.1 (52.7, 55.5)
R_C (kΩ)	3.8 (0.6, 7.0)	61.3 (59.3, 63.3)
ρ_C (Ωcm^2)	3.10×10^{-7}	3.10×10^{-5}
	$(0.07, 11.0) \times 10^{-7}$	$(2.96, 3.23) \times 10^{-5}$

ITO-on-InAs NW contact resistivity of $3.10 \times 10^{-7}\,\Omega\text{cm}^2$ was reached (Device 1). Within the confidence intervals of R_{14} and R_{23}, R_C of Device 1 lies within a quite wide span so that ρ_C fluctuates between $7 \times 10^{-9}\,\Omega\text{cm}^2$ to $1.1 \times 10^{-6}\,\Omega\text{cm}^2$, i.e. three orders of magnitude. This is due to the slight nonlinearity in the IV curves of Device 1 in Fig. 23, making the estimation of R_{14} and R_{23} less accurate. The lower bound of ρ_C at $7 \times 10^{-9}\,\Omega\text{cm}^2$ for Device 1 is unlikely as it rivals ρ_C of the best metal contacts to InAs NWs; ITO generally has a significantly higher ρ_C to semiconductors than metals do. Device 2 on the other hand had a very narrow range of R_C and ρ_C, closely matching ρ_C of the other devices in the previous samples. The upper bound of ρ_C of $3.25 \times 10^{-5}\,\Omega\text{cm}^2$ is significantly lower than the highest upper bound of the previous set of devices in Sample 1 with a milder surface passivation. Note that these were the two best devices out of five functioning devices: the remaining three were very poor in terms of NW resistance and contact resistance.

Still, the results support that the previous surface passivation step may have been ineffective and perhaps that these InAs NWs had an unusually thick oxide layer. Precaution must however be taken when increasing the concentration of $(NH_4)_2S_x$ as it may etch down the actual InAs too in the passivation step. The sample was therefore examined in the SEM to investigate any signs of overetching, which would show up as tapering of the InAs NW close to the ITO contacts. Micrographs of Device 1 from Sample 2 are shown in Fig 24.

At most, Fig. 24 B shows a very slight tapering of the NW just before the ITO contacts, but it is possible that there is no tapering at all. A large tapering would increase the NW resistance drastically, on the other hand, a small tapering would give visual confirmation of the effectiveness of the surface passivation solution.

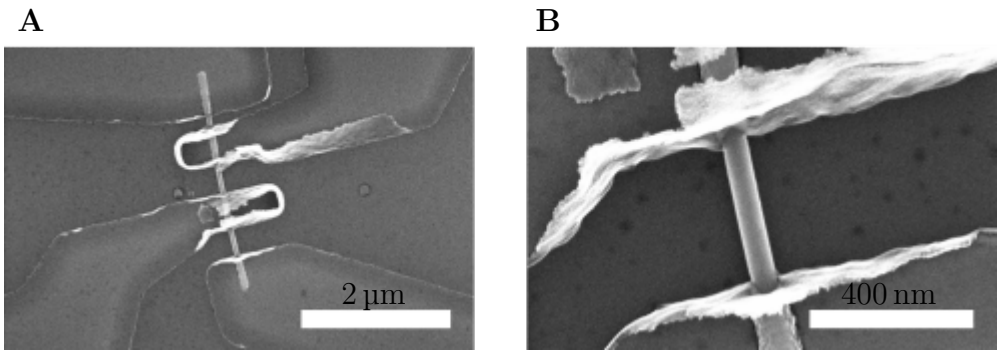

Figure 24: (A) SEM micrograph of Device 1 from Sample 2. (B) Zoomed in micrograph of same device.

The top two contacts of Device 1 in Fig. 24 A are very closely spaced. This creates a large electric field at higher biases that may cause a leakage current between the contacts, which in turn might explain the slightly nonlinear IV curves for Device 1 in Fig. 23. Due to the promising results from Fig 23 shown in Table 3, Sample 2 was annealed using the conventional annealing procedure for 30min at 200 °C in N_2 flow. Unfortunately, Device 1 did not survive the annealing step, and so only the IV characteristics of Device 2 are shown in Fig 25, with the results summarized in Table 4. Note that the annealed value of R_S extracted from Fig. 17 was used to calculate ITO line resistance for Device 2 after annealing.

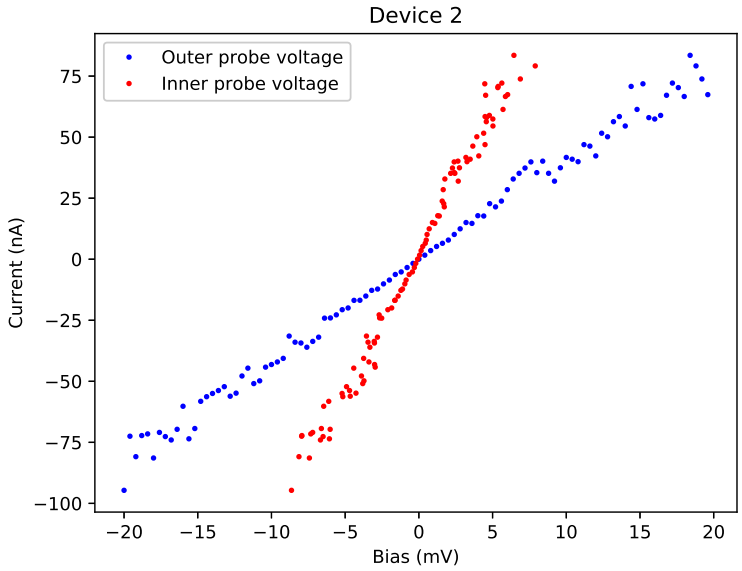

Figure 25: Two-point probe (blue) and four-point probe (red) measurements of Device 2 from Sample 2 with stronger surface passivation. The device was annealed for 30min at 200 °C in N_2.

Table 4: Extracted resistances from Fig. 25

	Device 2
R_{14} (kΩ)	423 (390, 450)
R_{23} (kΩ)	86.9 (75.9, 97.9)
R_C (kΩ)	77.3 (57.0, 97.6)
ρ_C (Ωcm^2)	3.71×10^{-5}
	$(2.40, 5.04) \times 10^{-5}$

Despite that the electrical measurements in Sec. 4.2 indicated that annealing is beneficiary for the electrical properties of sputtered ITO (Table 1), Fig. 25 and Table 4 indicate that these improvements did not translate to the contact properties: R_{23}, R_C and ρ_C all increased in the post-annealing measurements. This means that the annealing may have caused undesired changes in the ITO/InAs interface, which deteriorated the electrical properties. Moreover, the noise in the measurements increased too, which can be seen as the increase

in the width of the confidence intervals for R_{14} and R_{23} and hence the increase in the difference between the upper and lower bounds of R_C and ρ_C.

The slight increase in R_C and decrease in measurement confidence may give a clue to what is happening. In Ref. [50], the authors noted a similar contact quality degradation when they annealed their ITO contacts on n-GaN. In Ref. [62], the authors utilized the high oxygen content of ITO to oxidize a Ni layer on p-GaN. It is plausible that the annealing process have promoted diffusion of oxygen from the oxygen rich ITO into the contact interface and the InAs, causing oxidative reactions of InAs that would be detrimental to the electrical properties.

4.3.2 Sputtered Ni/Au/ITO contacts

To investigate if this side effect of annealing the ITO contacts could be prevented, a small sample of six four-point devices with Ni/Au/ITO contacts were fabricated for Sample 3. The idea was that Ni makes a good contact to InAs and Au protects the Ni from oxidizing, while the ITO acts as a current spreader to further decrease the resistivity and maintain a coherent contact layer. To maintain a high transparency of the contacts, the Ni and Au layers were intentionally made very thin, about 3.5 nm and 5.5 nm respectively. The fabrication utilized the same methods as previous samples, including a high $(NH_4)_2S_x$ concentration in the surface passivation step. The Ni/Au layers were deposited sequentially in the same sputtering step as the ITO which made the process very flexible. The two-point and four-point probe measurements are shown in Fig. 26 with extracted data presented in Table 5.

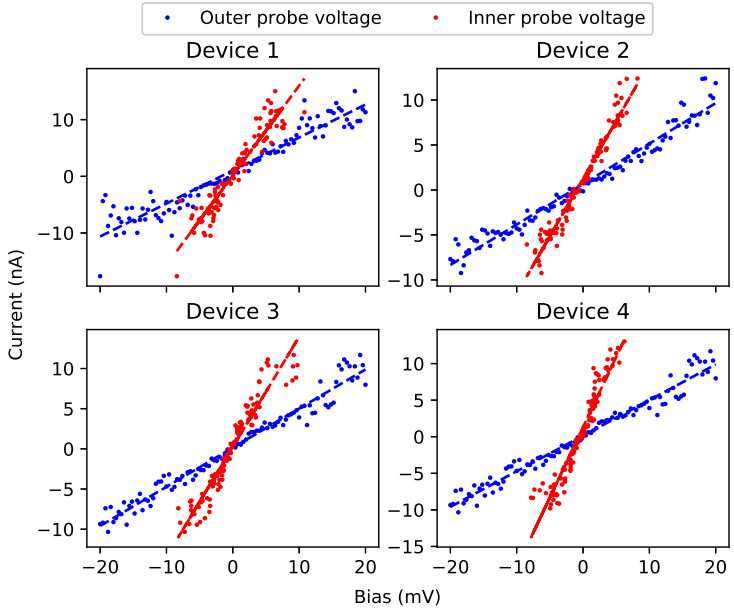

Figure 26: Two-point probe (blue) and four-point probe (red) measurements with linear regressions (dashed lines) of Ni/Au/ITO contacts on single InAs NW devices from Sample 3.

Table 5: Extracted resistances of Sample 3 from Fig. 26

	Device 1	Device 2	Device 3	Device 4
R_{14} (kΩ)	1720 (1616, 1824)	2220 (2140, 2300)	2050 (1980, 2120)	1910 (1840, 1980)
R_{23} (kΩ)	632 (589, 675)	780 (746, 814)	730 (686, 774)	521 (489, 553)
R_C (kΩ)	596 (526, 666)	415 (343, 487)	503 (436, 570)	623 (567, 679)
ρ_C (Ωcm^2)	3.17×10^{-4} $(2.67, 3.67)\times10^{-4}$	2.90×10^{-4} $(2.27, 3.54)\times10^{-4}$	3.63×10^{-4} $(2.97, 4.29)\times10^{-4}$	4.92×10^{-4} $(4.36, 5.48)\times10^{-4}$

The average ρ_C of the four devices in Table 5 is $\rho_C = (3.66 \pm 0.78) \times 10^{-4}\Omega\text{cm}^2$. Not only are the values of ρ_C similar between the devices, the upper and lower bounds of R_C and ρ_C for each device are close too; the highest upper bound of ρ_C is only about 50% higher than the average ρ_C for all the devices. Disappointingly, the strategy to improve the ITO contact interface via a thin Ni/Au layer worked poorly as seen in Fig. 26 and Table

5: R_{14}, R_{23} and contact resistances are significantly higher than for Sample 2, suggesting that the passivation step did not work well and/or perhaps that the ITO oxidizes the Ni layer, i.e. the Au layer did not protect the Ni sufficiently from diffusing oxygen, even under ambient conditions before annealing. Still, the sample was annealed using the conventional annealing procedure to determine the annealing impact on this new contact design.

The results of Device 1 and 4 are presented in Fig. 27 and Table 6.

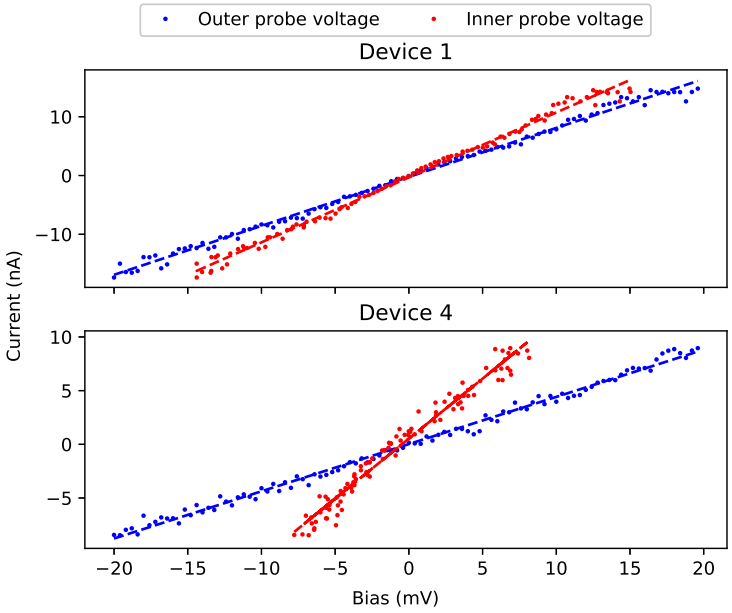

Figure 27: Two-point probe (blue) and four-point probe (red) measurements with linear regressions (dashed lines) of annealed Ni/Au/ITO contacts on single InAs NW devices from Sample 3. The devices were annealed for 30min at 200 °C in N_2.

The results suggest that the Ni/Au/ITO contacts behave quite differently than ITO contacts after the annealing treatment, for which the specific contact resistivity increased as seen for Sample 2. While R_{23} increased some 42% and 72% for device 1 and 4 respectively in Sample 3, perhaps suggesting that the parts of the InAs NWs not covered by the contacts were oxidized in the treatment, ρ_C decreased 54% and 79% for the two devices. This could be due to Ni diffusing into the NW, creating a low resistive Ni/InAs alloy

Table 6: Extracted resistances from Fig. 27

	Device 1	Device 4
R_{14} (kΩ)	1200 (820, 1580)	2270 (1310, 3230)
R_{23} (kΩ)	905 (614, 1200)	895 (509, 1280)
R_C (kΩ)	225 (-88.0, 538)	565 (-161, 1291)
ρ_C (Ωcm^2)	6.42×10^{-5}	3.88×10^{-4}
	(-, 28.1)$\times 10^{-5}$	(-, 8.44)$\times 10^{-4}$

at the interface [63]. However, because of the lowest bounds of R_C and ρ_C are negative for both devices, no definitive conclusion can be drawn for the annealing of the Ni/Au/ITO contacts.

Although the metal/ITO contact design did not work as well as intended it may show promise for heat treatments, both due to improved sheet resistance R_S (Table 1) and contact resistance R_C (Table 6). It could be that the $(NH_4)_2S_x$ surface passivation was still too weak to etch away all the InAs surface oxide, meaning that higher concentrations of $(NH_4)_2S_x$ likely are possible without etching away too much InAs from the wire. Simultaneously, the confidence in the measurements of R_{14} and R_{23} is rather low, leading to fluctuating bounds of R_C and ρ_C for the two devices.

4.3.3 Evaporated Ni/Au contacts

Last, Sample 4 was fabricated with devices utilizing conventional thermally evaporated Ni/Au (20 nm/80 nm) contacts in a four-point probe design as a control sample to be compared to the devices utilizing ITO electrodes. The IV characteristics of the two-point ant four-point probe measurements are shown in Fig. 28.

Unfortunately, the IV curves of the devices behaved very strangely: currents were extremely low, and the four-point resistances were offset. This proves no conclusive results except that the devices probably failed somewhere in the processing although the exact same methodology as previously was used to fabricate them. For this reason, no resistances have been extracted for comparison.

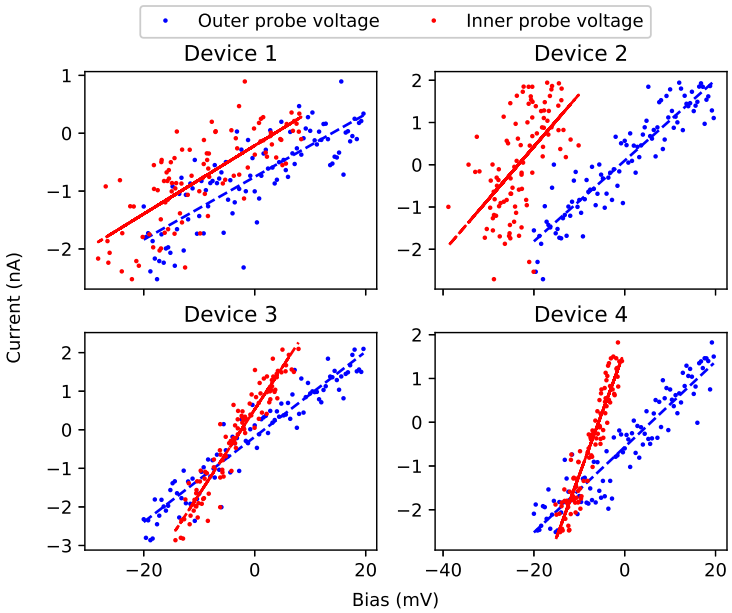

Figure 28: Two-point probe (blue) and four-point probe (red) measurements with linear regressions (dashed lines) of evaporated Ni/Au contacts on single InAs NW devices from Sample 4.

5 Conclusions and outlook

This thesis has investigated the possibility to switch conventional evaporated metal contacts to sputtered ITO contacts for single NW devices. ITO has several attractive properties that potentially makes it more useful for certain types of NW devices. It is highly transparent in visible wavelengths, which not only limits parasitic plasmonic effects present between light and metal contacts but also enables higher light absorption or emission as the device can still absorb or emit light where the ITO overlaps. ITO is a well-studied TCO, but its properties as a nanoscaled contact material for contacting NWs are not well-known; especially, the contact quality between ITO and InAs NWs has previously not been investigated. This work provides a first step towards a better understanding of patterning nanoscaled ITO contacts with emphasis on the ITO/InAs contact interface.

To contact single nanoscaled devices, the contacts need to be patterned to

smaller dimensions than what has previously been done for ITO. This is complicated by the non directional deposition nature of the sputtering process that is the dominant method to deposit high quality ITO. Here, a simple EBL patterning scheme with lift-off was investigated and optimized. The work has shown for the first time not only that EBL patterning with lift-off for ITO indeed is possible, but also that sub 100 nm wide lines can be achieved for 150 nm thick ITO, which, to the best of my knowledge, is the smallest dimensions ITO has been patterned to. Further optimization could likely push the resolution down the nanoscale, but it was shown that this is not always desirable: downscaling the contacts severely increased the sheet resistance R_S, which was attributed to the increase in surface scattering and lower carrier mobility. Knowing R_S is important from an engineering point of view as it allows for assessing the contribution from ITO line resistance during design of the contacts. This is usually not considered for conventional metal contacts, but ITO has intrinsically a much larger resistivity than most metals which may result in a undesirably large voltage drop across the contacts instead of the device. Although a 30 min annealing scheme in 200 °C N_2 improved the sheet resistance somewhat, it is still a concern for ITO contacts, which therefore should be designed to be as wide as possible prior to physically contacting the device.

Three TLM designs were investigated to measure the ITO/InAs specific contact resistance, ρ_C, which is arguably the most important figure for electrical contact quality between two materials. For these NW samples, the conventional four-point probe measurement technique was the most useful. All device designs did however show unreasonably large total resistances, including contact and nanowire resistance. This was somewhat improved by increasing the ITO contact width and thereby contact area. The largest improvements were accomplished by increasing the concentration of the active surface passivation agent $(NH_4)_2S_x$. From the four-point probe measurements, an average specific contact resistivity of $(3.93 \pm 2.79) \times 10^{-5}\,\Omega\text{cm}^2$ with an upper bound of $11.3 \times 10^{-5}\,\Omega\text{cm}^2$ was then extracted, showing promise for ohmic ITO contacts to InAs NWs, likely due to high ITO carrier concentrations as confirmed by Hall measurements.

While annealing improved most relevant material properties for samples with ITO sputtered on glass substrates, as shown by van der Pauw and Hall measurements, the improvements did not translate to the ITO/InAs interface quality as R_C and ρ_C increased post annealing. It was believed that the

annealing promoted oxygen diffusion from ITO to the InAs, causing oxidating reactions at the interface, which increased ρ_C. A different contact stack of 3.5 nm/5.5 nm/100 nm Ni/Au/ITO was tested with the intention to hinder oxygen from diffusing into the InAs while maintaining a relatively high optical transmittivity. Unfortunately, these contacts did not perform as well and an average ρ_C of $(3.66 \pm 0.78) \times 10^{-4}\,\Omega\text{cm}^2$ with an upper bound of $5.48 \times 10^{-4}\,\Omega\text{cm}^2$ was measured. In contrast to the pure ITO contacts, annealing seemed to improve the contact resistivity. This was attributed to Ni diffusing into the InAs NW, creating a low-resistive Ni/InAs alloy. However, because the lower bounds of R_C and ρ_C were negative, no significant conclusions could be drawn from the statistical analysis. Since none of the micrographs of the devices showed tapering of the NW at the contact, an even higher $(NH_4)_2S_x$ concentration could be tested in the surface passivation to ensure that all InAs surface oxide has been removed.

This work has showed initial feasibility of patterning nanoscaled ITO contacts for single NW samples. Additionally, the contacts make ohmic electrical connections to InAs NWs, with low contact resistivity in comparison to ITO on other semiconductor materials. For future work, it would be valuable to test the ITO contacts on new InAs NWs that have been confirmed to have excellent conductivity, as the ones used here were ambiguous in that aspect. Replicating experiments to measure the specific contact resistivity done in this thesis for e.g. InP, GaAs and GaN NWs would be valuable for research on NW devices with ITO electrodes, including NW array devices such as photodetectors and SCs. For improved reliability in the measurements, a new device design for the four-point probe devices could utilize very thin metal contacts for the two middle contacts. This would avoid the issue of short-circuiting large segments of the NW that was believed to be the case for the deliberately wide designed middle ITO contacts. Alternatively, a slight alteration of the four-point measurement could be performed to extract R_C and ρ_C. This would require longer NWs to design wide and, more importantly, four equally wide contacts. After the four point-measurement, a two-point measurement between the middle contacts would eliminate the issue of current being short circuited for the two point measurement between the outer contacts, which would simplify the equations used to extract R_C.

The processing utilized in this work was optimized for depositing 100 nm to 150 nm thick ITO layers. As thicker ITO has improved electrical properties, the devices would likely benefit from optimizing the processing for depositing

thicker ITO layers. Last, the benefits of using ITO as contact material of photonic NWs needs be confirmed by in optical experiments and compared to NW devices with metal contacts.

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