Suitability of Dynamic Latches for Sub-VT Operation

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In the past the major concerns of VLSI designers were the performance and area of electronic devices but right now because of technology scaling in CMOS and also with the substantially growth in portable computing gadgets like smart phones, tablets, laptops, etc the power consumption has become a critical issue. In order to decrease power wasting it is necessary to apply low power techniques in all steps of circuit design.

Minimizing supply voltage is the most effective way to decrease the total power dissipation. Indeed reducing supply voltage to sub-threshold region leads to improve energy efficiency but unfortunately the standard cells that are conventionally being used in the electronic designs not optimized for being used in ultra low voltage design. Up to 70% of total energy in a chip consumed by storage elements and data path components and reducing the power consumption of these elements can lead to save more energy.

This project is going to investigate on different dynamic latches to find the minimum reliable supply voltage for each design and also analyzing these circuits in case of area and performance. The leakage current as a crucial factor in power dissipation, especially when the design is in standby mode, is considered in this project in order to control the total power consumption. Anyhow the main goal of this master thesis is implementing the interested latches at sub-threshold voltage and also these topologies were investigated and compared with each other in many aspects and the desire latch in case of low power dissipation was selected for customization and post layout simulation. Scaling supply voltage results to increase V_{th} variations and this issue directly affects on design reliability. For having more reliable results Monte-Carlo simulation with 10,000 iterations was carried out.

For now only four dynamic latches (Pass transistor, transmission gate, True dingle phase and tri state gate) were investigated and analyzed in case of accuracy, performance and power consumption but in order to work at ultra low power regime it is necessary to develop new full-custom circuit for ULV operation either customize standard cell library and this could be something for future work.