Inductively-Coupled Plasma Etching for Nanoimprint Si-masters

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Abstract

In the last decades, engineers have been pushing semiconductor technology towards fabricating ever smaller devices, and will eventually pass the lower limit of currently commonplace optical lithographic techniques. New techniques have been developed, such as nanoimprint lithography. Stamp fabrication is the key for nanoimprint, and stamps often need to be bought from an external company. In this thesis work, a simple method for stamp fabrication utilising Inductively Coupled Plasma Reactive Ion Etching on samples with Electron Beam Lithography defined patterns in an electron beam sensitive resist, using fluorine based etch chemistry in a Single-step Reactive Ion Etch process, has been developed, allowing for in-house stamp fabrication at Lund Nano Lab using a reactive ion etching process. A process for increasing etch selectivity, called selective infiltration synthesis, was also investigated as a means to improve the fabrication process. This work enables nanoimprint lithography to be a more readily available, and thus more widely used, patterning technique for various research projects within Lund Nano Lab.

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List of Abbreviations

ALD	Atomic Layer Deposition
BCP	Block Co-Polymer
CPU	Central Processing Unit
EBL	Electron Beam Lithography
ICP	Inductively Coupled Plasma
IPS	Intermediate Polymer Stamp
LNL	Lund Nano Lab
NIL	Nanoimprint Lithography
PMMA	Poly-(Methyl Methacrylate)
PS	Polystyrene
PS-b-PMMA	Polystyrene-Poly-(Methyl Methacrylate) block copolymer
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
SCCM	Standard Cubic Centimetre per Minute
SIS	Sequential Infiltration Synthesis
TMA	Tri-methyl Aluminium

1 Introduction

In the current highly digitalised society, processing power is an always important concern.[1] In all manner of different aspects of life, from entertainment, with editing and rendering of movies, to science, with modellings and simulations, more processing power is better, allowing for faster calculations. It is therefore no big surprise that scientists and engineers go to great efforts to develop smaller and faster transistors,[2] the main component of a computers processor.[3]

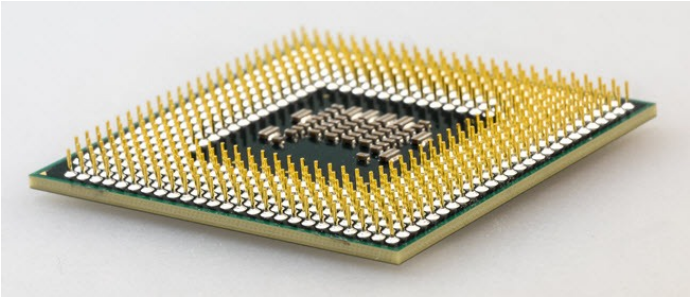

Figure 1: An example of a processor outside of a computer.[4]

Making the transistors smaller allows for more of them being able to be packed in a specified area, giving a higher processing power without increasing the size of the processor. The miniaturisation also often reduces the energy required to power an individual transistor, meaning that doubling the amount of transistors does not automatically translate to a doubling of the power consumption. This development observation has been named after Gordon E. Moore, one of the founders of the electronics company Intel.[5] Moore's law states that the number of transistors on a chip, and thus the processing power, grows exponentially with time. Currently, the rate is cited as a doubling of every two years. The constant improvements to old techniques, coupled with the development of new ones means that the law has held up since its formulation in 1965.

Lately, however, the transistors have been starting to reach the limitations on lower size limit achievable with the commonly used optical lithography technique used for patterning of devices. Therefore, new techniques will be needed to continue the miniaturisation process that retain the high-throughput characteristics of optical lithography.

One of these processes is Nanoimprint Lithography, that uses a stamp with three dimensional features that patterns a soft sacrificial layer. This process has been proven to be able to achieve resolutions below the 10 nm mark,[7] and there are techniques that can be used to make very high resolution stamps with complex features.[8] This would make it a viable candidate to replace optical lithography for the 22 nm transistor node, and continue to carry the fabrication technology even further.[9] The parallel patterning process of NIL, meaning that the entire wafer area is patterned simultaneously, gives the process the high throughput of the commonly used optical lithography, coupled with the higher resolution attainable, comparable to serial patterning techniques such as EBL, while being a cheaper solution, both in terms of equipment and masks/stamps.[10] There is also a possibility to use a roll-to-roll NIL, where the stamp features are on the

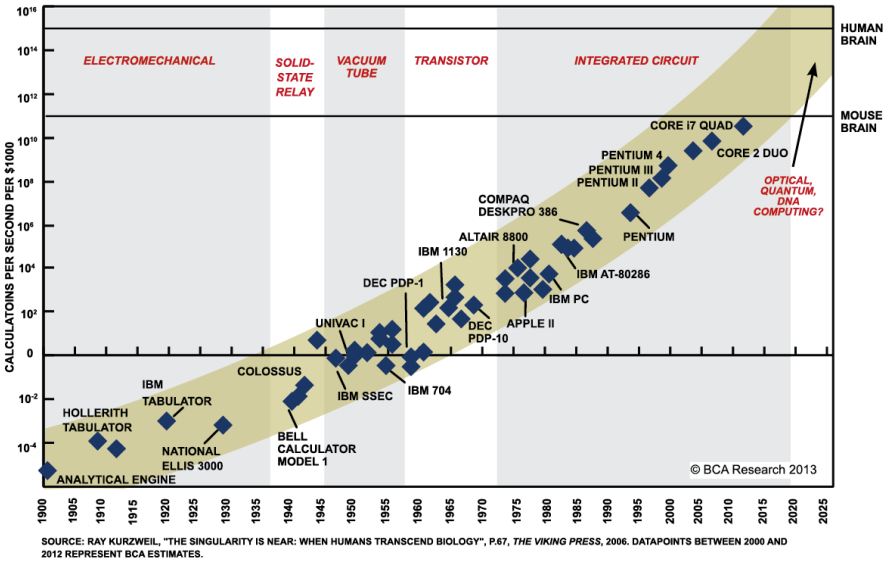

Figure 2: A diagram showing the development of processors from the early 1900s until 2015. The yellow field represents the development speeds according to Moore's observation.[6]

surface of a cylinder, and the substrate is patterned by being pressed through the gap between the patterning cylinder and another roller below. This would make patterning into a continuous process, which would be very favourable in industrial applications.[11,12]

But it is obvious that this development with transistor down-scaling has a clear and definitive lower limit. As dimensions go lower, the amount of atoms are of course reduced. Eventually, devices would become so small that they consist of only a single atom, at which point a size reduction becomes impossible without significantly altering the basic working principle of a transistor. On top of this, each size reduction is harder than the previous, making the complexity and cost of transistor downscaling grow exponentially.[13]

This has led to a shifting of focus from just the cramming of more transistors on to a chip, to integrating the other components onto the same chip as the transistors. These components include things like power control, sensors or RF communications (like WiFi or Bluetooth). These approaches towards downscaling of entire systems has been called More than Moore and System Scaling.[13,14] They don't necessarily have the same scaling characteristics as Moore's Law and transistor scaling, but provide different benefits to the electronics devices it is applied to. One example is combining the optical sensor of a camera with the processor necessary for processing the signal into a complete image onto a single chip, creating a small, energy efficient and potentially very fast camera unit, that could easily be utilised in smartphones.[14]

Integrating all these different components onto the same chip of course requires many more production steps than a transistor-only chip. This bring with it

more lithographic processing, where each one needs to be perfectly lined up with the previous. While this is perfectly doable with optical lithography, this would require many different masks. These masks are often expensive and fragile, and more lithographic steps results in more risk for mask damage during the production of a single wafer. Nanoimprint stamps are less expensive to replace, and, if an intermediate stamp is used, much less likely to break, making the process more favourable for multi step fabrication processes. These other components ar also often much less complex than transistors, which makes NIL a good choice.[12]

Another advantage of NIL in this regard is the 3D nature that the process possesses. While the process was initially developed as an alternative to the 2D lithographic techniques, such as optical lithography or EBL, with essentially binary patterning with either (almost) complete resist displacement of no resist displacement, it is not difficult to create a multilevel stamp, where resist thickness can be specified as anywhere between these two extremes. This gives NIL more freedom in what type of structures that may be produced, such as smooth hemispheres, pyramids or wedge-like ridges, which may prove useful for the More-than-Moore and System Scaling developments.[15]

In common with the masks used in optical lithography, the nanoimprint stamps first needs to be fabricated, which is often performed by a third party. This can cause unnecessary delays and costs in a project when new stamps needs to be made as improvements on previous designs are made. While these professionally made stamps are hard to surpass in quality and accuracy, in the early stages of a project it is often overkill to order one, as the effects of defects on a stamp may well be overshadowed by design flaws. It would thus be preferable if there was a way to make simple stamps useful to get preliminary results that can be used to begin the iterative optimisation process. The ability to more quickly get new stamps would allow for faster development cycles.

It should also be noted that it is not only the electronics industry that can benefit from the development of Nanoimprint Lithography. In the world of medicine and biochemistry, a relatively new concept called Lab-on-a-chip has arisen. The aim here is to create what is functionally a complete laboratory on a single glass or silicon plate. Microscopic channels on the chip lead a fluid sample to analytical "stations", see Figure 3. These stations can do various things, such as particle sorting by size,[16] detection of specific particles or proteins[17] or even copying of DNA strands for analysis of genetic make-up.[18] Advantages of this technique are for example that the biological sample volume needed is very low, thanks to the small size and high sensitivity of the devices, fast results due to the small volume making diffusion, heating and similar processes very quick, and the ability to test multiple things in parallel, further reducing the time between sampling and diagnosis.[20] However, one of the disadvantages is that the fabrication of the devices is difficult and requires special, expensive machines and highly trained staff. This is where Nanoimprint Lithography comes in. Due to the nature of the Nanoimprint stamps, being essentially a collection of trenches and protrusions, it resembles one of these lab-on-a-chip very much. It would thus not be that hard to imagine that the imprinting process could be used to create these chips in a soft material.[21] The high throughput and reusable stamps featured in Nanoimprint Lithography would allow for quick and cheap Lab-on-Chip fabrication.[21,22]

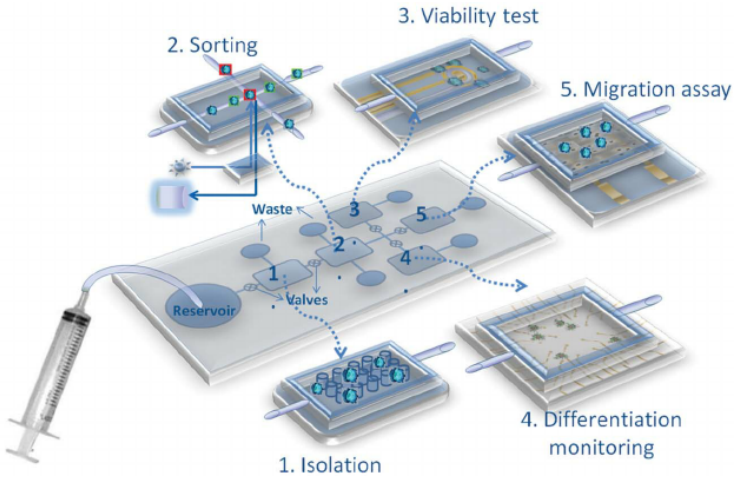

Figure 3: An example of a Lab-on-a-Chip for study of stem cells. There are a number of different modules, that in this example isolate the interesting cells, sorts and tests whether the cells are viable, before finally running the actual tests on the selected cells that you are certain are giving the most representative results. By fitting all these functions o a small chip, the need for a dedicated biological lab is greatly reduced in this specific case.[19]

Nanoimprint Lithography and Lund University has a lot of history together. Lund University started working with Nanoimprint Lithography early on and was among the leading developers for the technique, with many papers published on the subject.[23,24] One of the leading companies producing Nanoimprint equipment, Obducat, has close ties with Lund University and still has their main office in Lund. The specific system present in Lund Nano Lab is shown in Figure 4. Nanoimprint Lithography is thus an important technique for Lund University, both because of history and the potential for development. It is therefore no big surprise that Lund University is participating in a European collaboration project, aimed at making ultra-high resolution NIL more accessible for whoever needs it.[26]

This project aimed at developing a technique to fabricate NIL stamps at Lund Nano Lab, using a reactive ion etching technique on common silicon wafers, preferably using a soft resist mask. The etching has been performed in an Inductively Coupled Plasma Reactive Ion Etcher (Apex SLR from Advanced Vacuum/Plasma-Therm) on Electron Beam Lithography (EBL) defined samples. The etch results has been examined with Scanning Electron Microscopy (SEM) and ellipsometry.

It is possible to fabricate the type of structures present on a stamp surface using various etching techniques. However, there are a few requirements on the properties of the structures, apart from sufficient resolution for the pattern. For example, the walls of trenches and protrusions needs to have a certain profile, see Figure 5, to allow the stamp to be easily removed after the patterning process.

Figure 4: The Obducat nanoimprint lithography system used in Lund Nano Lab.[25]

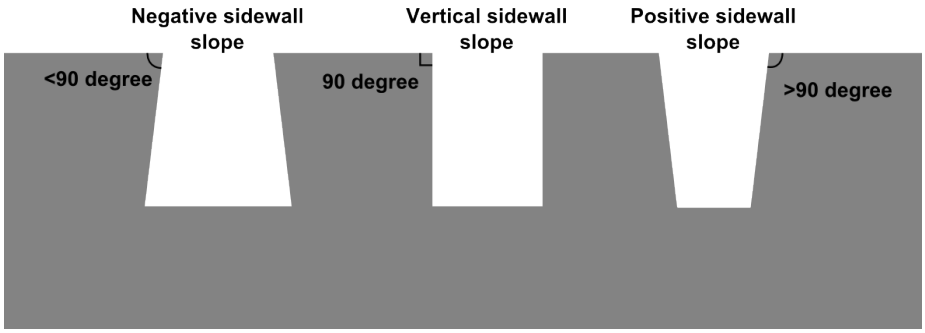

Figure 5: A sketch showing the difference between negative, vertical and positive sidewall angles for etched structures.

It is thus vital to find the proper conditions with regards to the technique used, the etching chemicals and their concentrations as well as other parameters specific to the technique used. The sacrificial layer used for the pattern definition is also often susceptible to the etching to some degree, which can limit the results of etching in terms of depth if not handled properly.

In the end, a recipe was attained which satisfied the requirements of a positive angle of the sidewalls, an etch rate allowing for precise tuning of etch depth and optimisation for structures of different dimensions, and an etch selectivity high enough to allow soft resist masks to be used. This means that NIL is

a more accessible lithographic technique at LNL, as researchers do not need to order stamps from an outside company, reducing both the cost and waiting time for a new stamp when using NIL in a project. The attempts at performing Sequential Infiltration Synthesis (SIS) also provided new information for the further development of the technique, at least regarding the limitations of the process as there were no indication of an improvement in resist stability in the trials performed in this project.

In the report, Chapter 2 gives a background for techniques and devices used in the project, while Chapter 3 describes the experimental details. The results are outlined in Chapter 4 and analysed in Chapter 5. Chapter 6 summarises the project and its results, and proposes directions for further development of NIL at Lund Nano Lab. For reference, the final recipe is presented in Table 7, Appendix A.

2 Theory

2.1 Reactive Ion Etching

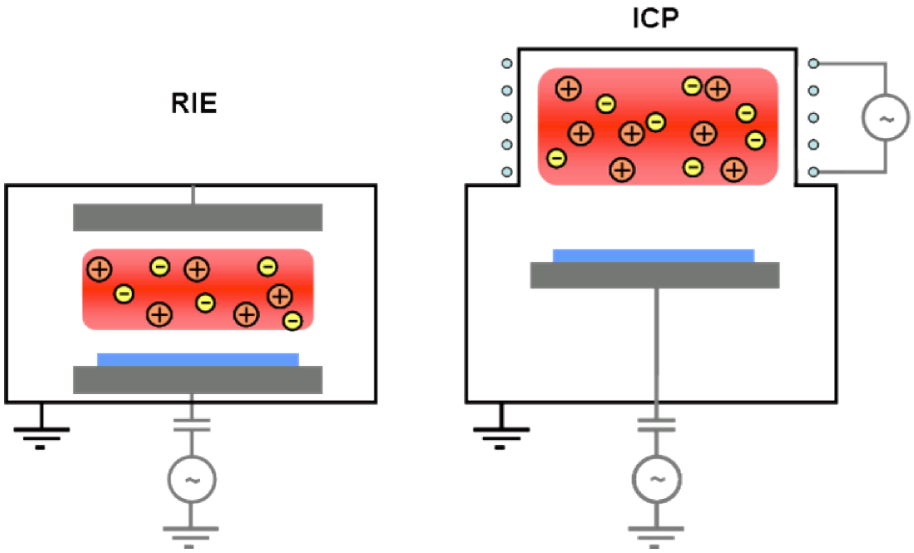

Figure 6: A sketch showing the chamber layout of a conventional Reactive Ion Etching system and an Inductively Coupled Plasma RIE.[27]

Reactive Ion Etching (RIE) is a dry etching technique based on producing chemically reactive ions and radicals by subjecting a gas mixture to a radio frequency (RF) electromagnetic field. A schematic image showing a typical chamber layout is shown in Figure 6 The RF-field will cause the electron cloud of the atom to be pulled in alternating directions, while the heavier, and thus less responsive, nucleus will vibrate less strongly. This will eventually result in an ionisation of the gas molecules. These ionised species will then be accelerated to the surface by the field, where it will react with the surface of the sample, forming volatile compounds that are pumped away.[9,28]

There are a variety of parameters that can be tweaked to achieve the optimal etch conditions for a certain application. The power of the RF-field mentioned previously for example. An increase of the power will lead to more ionisation, and thus a higher plasma density, increasing the etching properties of the process. However, it will also increase the energy with which the ions impact the surface, leading to more pronounced physical etching, or sputtering, effects. This may be undesired, since sputtering rate is dependent on physical etch resistances, such as hardness, instead of chemical resistance. This has an effect on *etch selectivity*, defined as the ratio between etch rate of the substrate and the etch rate of the masking material. It is generally desired to have a high selectivity, where the substate etch faster than the masking layer. However, the etch mask is seldom more resistant to both physical and chemical etching than the substrate. This means that the mask will be eroded by the sputtering at a faster rate than the substrate, which, depending on the severity of this difference, can

limit the maximum depth of the structures etched into the surface.[9,28]

The gas mixture also affects the properties of the etch. To have etching at all, you need a gas which is able to react with the substrate, and form the volatile compounds necessary for the removal. The exact gas required depends on the chemical composition of the material to be etched. For example SF_6 can be used for silicon etching. The flow of this gas will affect the rate of removal of the etched material; a higher flow results in an increase of available etching species and thus an increase in etch rate. However, if only etching gases are used, the etch will be of a more chemical kind, with less directional control (isotropic), meaning that the etch rate will be similar in all directions on the sample, see figure 7. This can result in severe under-etching, where the parts of the substrate covered by the mask may be partially etched away.

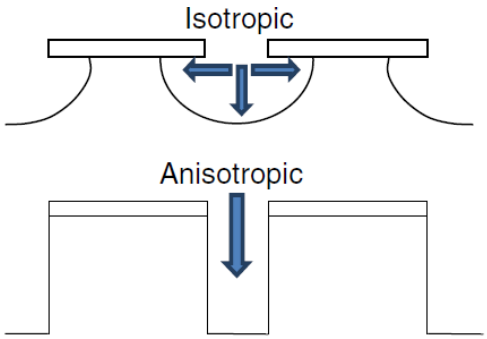

Figure 7: Comparison between isotropic and anisotropic etching.[28]

It is thus possible to include another component in the gas mixture, which forms a protective film on the exposed surfaces. This will slow down the etch speed, but may give a better control on the directionality of the etching. This is a result of the combination of chemical and physical etching. The physical etching is highly anisotropic, and only etches downwards. This means that the protective film deposited on the horizontal surfaces will be etched both chemically and physically, whereas the film on the wall will only be chemically etched, which results in a higher etch rate vertically than horizontally. The ratio between these gases can be tuned to give you the etch profile that you need.[9,28]

2.1.1 Inductively Coupled Plasma RIE

Standard Reactive Ion etchers have the RF electric field applied between the chamber walls and the sample stage. This field both generates ions and accelerates them towards the sample stage. This means that the plasma density is connected to the energy of impinging ions. By adding a coil around the top part of the chamber, it is possible to separate these two processes. Applying a RF energy to the coil will create a switching electromagnetic field inside the chamber, which will induce a current in the gas, that will in turn ionise the gas. This field won't accelerate the ions towards the sample, however, so a RF field between the walls and the sample stage will still be responsible for the ion energy allowing for reactive ion etching. It will however give the possibility to

create a high-density plasma, without increasing the energy of the accelerated ions.[9, 28]

2.1.2 Fluorine-based RIE

Fluorine-based RIE techniques uses gases that form fluorine ions and radicals in a plasma. Commonly used gases include SF_6, CF_4, CHF_3 and C_4F_8. While all of these gases will produce the etching fluorine radicals, the last three also may lead to polymerisation and formation a thin polymer layer on the sample. This can be used to passivate and protect the surface, granting the beneficial effects on anisotropy discussed earlier.[28, 29]

2.2 Lithography

In order to perform any process for limited area surface modification, you need to mask the areas that are to be left unmodified. This is usually achieved with a polymer based layer, often called a resist layer. This layer can then be patterned with a variety of techniques, including, but not limited to, UV-lithography, Electron Beam Lithography (EBL) and Nanoimprint Lithography (NIL). Each have their own advantages and disadvantages; for example, EBL has a high resolution, but is a slow process, since the surface needs to be exposed one pixel at a time in a serial process resulting in a long process time.[9]

2.2.1 Electron Beam Lithography

Electron Beam Lithography (EBL) is a method for patterning a masking layer (resist) that relies on changing the solubility of the masking layer by changing the chemical structure with exposure to a focused beam of electrons. The resist used can be of a positive type, where the exposed area has an increased solubility, or negative type, where the exposed areas instead have reduced solubility. This can be achieved by either breaking or inducing creation of cross-links in a polymeric material.[9]

As mentioned earlier, the resolution of EBL is very good, below 10 nm. The maximal resolution is determined by how small a point the electron beam can be focused into, and can be down towards single nanometres. However, the spot size, and thus the resolution, is limited by imperfections in the magnetic lenses used for focusing the electrons, called aberrations. The main examples are **chromatic** and **spherical** aberration. Chromatic aberration is caused by differences in energy between electrons. As stated earlier, higher energy electrons are more strongly affected by the magnetic lenses, and will thus be focused earlier than lower energy electrons. Because electron guns are imperfect, there will always be a spread in energy of the generated electrons. This effect is reduced by introducing apertures at certain points in the column where it is known that electrons of a certain energy will be focused to a crossover point. This will remove much of the electrons with a different energy, at the cost of a reduced beam current, and thus a lower signal at the surface. Spherical aberration is a result of the fact that electrons are bent more strongly the further from the centre of a lens they pass. The impact this has on the focusing can be reduced by using stigmators that compensate for this effect.[30]

Due to the fact that only such a small area can be exposed at a time, it will

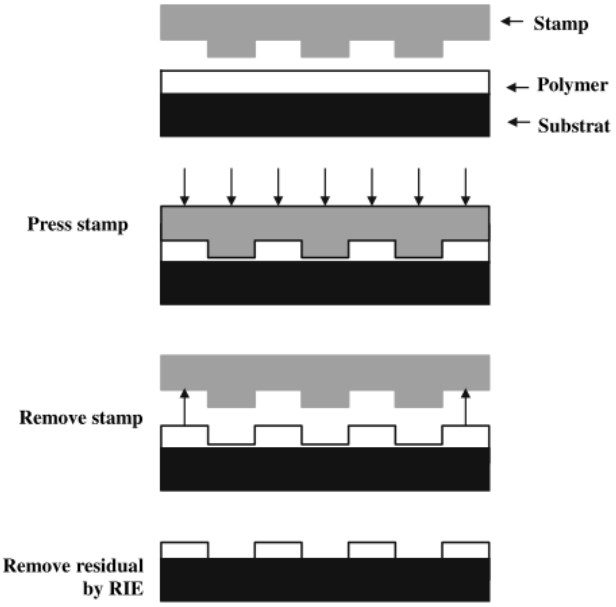

Figure 8: A schematic NIL process.[9]

take a long time to complete the exposure of the entire pattern. The electron beam can be moved over the sample without mechanically moving the sample using deflection coils, meaning that it is easy to ensure that the pixels are spaced evenly, and a good pattern cohesion is obtained. There is a limit to the deflection distance achievable, creating a square on the sample known as a *write field*. If the pattern is larger than one write field, it is necessary to move the sample to the next write field to complete the pattern. This can create problems if the mechanical movement is not properly calibrated, which may result in a misaligned pattern, overlapping write fields or gaps between write fields. This will render the pattern unusable, and requires you to redo the entire process, resulting in even more time used.[9]

2.2.2 Nanoimprint Lithography

Nanoimprint Lithography is a mechanical method of patterning a masking layer. A schematic process is shown in Figure 8. It relies on pressing a stamp with a three-dimensional pattern, representing the pattern needed, into a viscous liquid or semi-solid resist layer. The stamp has both high areas, where the resist will be displaced in order to access the substrate surface, and low areas, where the final resist layer will be thicker, and the substrate surface will be inaccessible. The resist will be displaced by the structured stamp, at which point it can be hardened, such that the pattern remains after removing the stamp. This hardening can be done in several ways, and the two major methods are cooling and induced crosslinking.

- The first method, often called thermal imprinting, entails heating up the resist to a point where flowing is possible. Then the stamp is pressed into

the layer, and the resist is displaced. The sample is then cooled until no longer flowing, and the stamp can be removed.[9]

- In the second method, the resist is already flowing at room temperature, allowing the imprinting to be performed without heating. The resist is instead hardened by inducing crosslinking of the polymers, for example by exposure to UV-radiation. After this hardening, the stamp can be removed, with the imprinted structure remaining.[9]

There often will be a thin residual layer at the bottom of the imprinted structures however, as mechanical pressing is unable to completely displace all of the resist, requiring another process to remove this final layer, such as plasma ashing for a polymer resist.[9]

The resolution of NIL can be made to be comparable to EBL. There are however issues with NIL that EBL doesn't have to deal with. These arise mostly due to problems with the mechanical displacement. To properly transfer the pattern, the resist may need to flow over large areas to reach the lower stamp structures. If the resist is unable to flow quickly enough, these larger areas will have a thicker residual resist layer, possibly preventing the access of the substrate. You also need to be able to remove the stamp without tearing away the resist. This risk can be minimised by modifying the stamp surface to interact unfavourably with the resist, thereby reducing the adhesion of the resist to the stamp. This may not be enough, and very small structures can still be torn off even when handled carefully.[9]

Another common problem is the sensitivity of the stamp. Since direct contact and high pressures are required, it is very possible for the stamp to be destroyed because of hard contaminant particles that end up under the stamp. This risk can be removed with the use of an Intermediate Polymer Stamp (IPS). Here you have a master stamp of a durable material, e.g. silicon or nickel, which you make negative copies of in a flexible polymer sheet, using a thermal imprinting process. This negative intermediate stamp is then used for the actual sample imprinting, after which the intermediate stamp is discarded. With this technique, hard particles will not destroy the stamp, due to the IPS being flexible. Instead, any contaminants on the master stamp will be incorporated into the IPS, as the polymer flows around the particle, encasing it inside the stamp structures. Additionally, these particles will not affect the final imprinted structures.[9]

Contaminants on the imprint target however will not be accommodated in the same way. Here, the advantage with the IPS is that it is flexible and disposable. The polymer sheet will flex around the particle, preventing if from causing cracks in the substrate. The structures in the area under the contaminant will be destroyed, which it why is preferable to place multiple copies of the structure on the master stamp, increasing the chance that at least some of your structures are functional.[9]

2.2.3 Block copolymer lithography

Block copolymers is a group of polymeric materials with the common factor that the polymer chain is built up of two (or more) blocks of different polymers, see the left of Figure 9, as compared with random copolymers, where the different

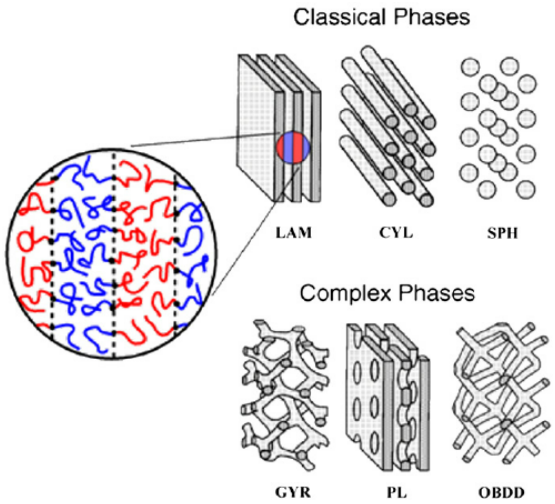

Figure 9: Example sketch of a block copolymer (left) and different structures that the block copolymer can adopt on phase separation (right).[31]

polymers are randomly distributed throughout the chain. Because they are chemically bound to each other, it is possible to combine two polymers that are non-miscible, and get a bulk material where the different polymer blocks phase separate into smaller regions, with each region only containing the blocks of one specific polymer. Block copolymer (BCP) lithography is a lithographic method utilising this self assembly of non-miscible polymers to create distinct regions with differing chemical and physical properties. It is possible to modify the substrate to make surface interaction favourable for one of the polymer blocks. This means that that block will prefer to form a surface there, allowing you to direct the self assembly to form regions of specific polymers. These regions can then be used for further processes that use the different properties of the polymer blocks to modify either one of the areas formed.[29]

2.3 Atomic layer deposition

Atomic Layer Deposition (ALD) is a method for fabrication of films of material with a thickness on the nanometre scale. A large number of materials are possible to deposit in this way, for example hafnium oxide (HfO_2) for transistor gate dielectric, titanium nitride (TiN) and aluminium oxide (Al_2O_3). The process uses precursors, for example in the form of organometallic or halide compounds, to perform reactions selectively at the surface, creating single-atom layers of material.[32]

ALD is a cyclical process. The precursor gas is introduced into a chamber together with the sample. Often, the gas reacts with groups already present on the surface. The chamber is heated, facilitating the reaction of precursor gas adsorbed to the surface. For example, when depositing alumina using tri-methyl aluminium (TMA), see Figure 10, the TMA will react with OH-groups from adsorbed water molecules, forming bonds with two oxygen atoms, while removing two of the methyl groups. The surface is then subjected to water vapour in order

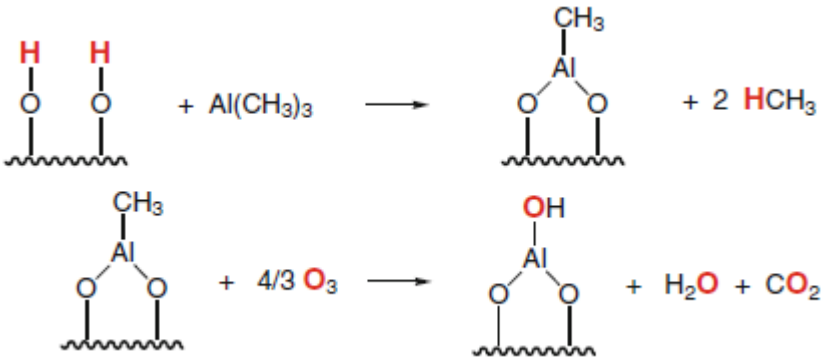

Figure 10: The reaction mechanism that form alumina from tri-methyl aluminium.[32]

to remove the last methyl group and replace it with a OH-group. This sets up the surface for another round of precursor exposure, resulting in a cyclic process where (ideally) one mono-atomic layer of material is deposited each cycle.[32]

Other types of functional groups that can be used to perform ALD include hydrogen, oxygen, fluorine and chlorine.[32]

2.3.1 Sequential Infiltration Synthesis

Sequential Infiltration Synthesis (SIS) utilises the same equipment as an ALD process. The difference is that instead of depositing thin layers on the surface, the aim is to modify (specific areas of) the polymer resist. If done correctly, this will enhance the properties of the resist. One example is infiltration with alumina (Al_2O_3). This will increase the polymer's resistance towards physical dry etching.[33] This can be utilised in block-copolymer lithography, by selecting the constituents in a way that one of the polymers can be infiltrated, while the other polymer can't. The stability of infiltrated polymer will be much higher than the non-infiltrated, making removal of the unwanted areas of the mask easy.[34] A schematic sketch of the process is displayed in Figure 11, where the PMMA (yellow) is infiltrated with alumina (red), while the polystyrene (green) is unaffected apart from the thin layer of Al_2O_3 that is uniformly deposited across the sample. This results in that the polystyrene will be much easier to etch away, eventually being completely removed, exposing the Si underneath.

The process has been demonstrated to work with infiltration of trimethylaluminium into poly-(methyl methacrylate) and ZEP 520a electron beam resist.[33]

2.4 Scanning Electron Microscopy

Scanning Electron Microscopy (SEM) is a microscopy method that uses electrons instead of photons to characterise the surface of a sample. The electrons have a much shorter wavelength than visible light, which gives a higher attainable resolution on the order of nanometres. However, because electrons interact

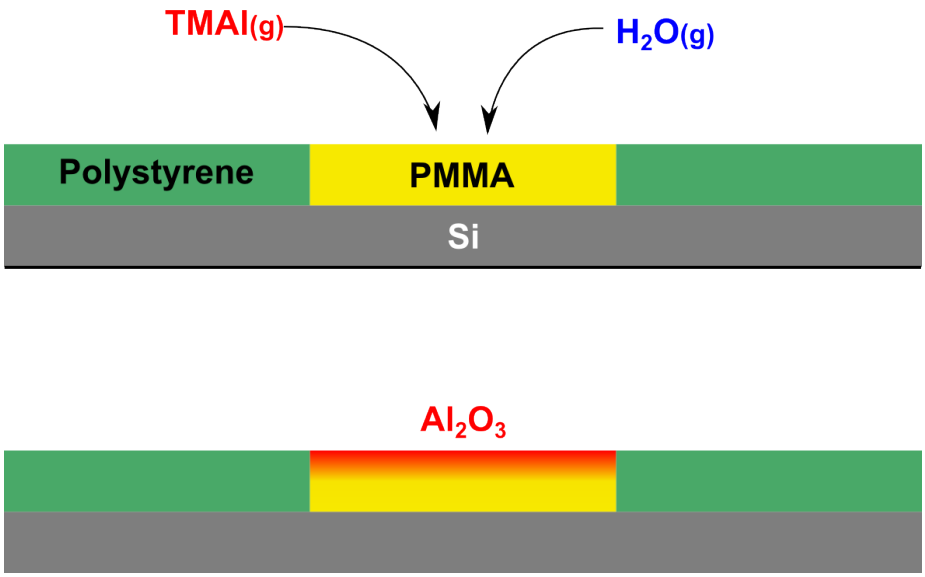

Figure 11: A schematic process sketch of a sequential infiltration synthesis (SIS) of alumina in PMMA in a PS-b-PMMA copolymer. If done correctly, the SIS process may result in infiltration of the whole depth of the polymer.

differently with a material than light, the detection method needs to be different. The primary, or beam, electrons generate a number of secondary electrons from the sample that can be used to characterise the surface, which will give different information on the properties. This also means that it is not possible to study the entire surface at the same time, but instead an image is generated pixel by pixel by scanning an extremely thin beam across the area of interest.[30]

Free electrons can be generated in a few different ways. It is possible to thermally excite electrons from certain materials with low work function, such as LaB_6. Another way is to subject a sharp tip of a metal, commonly tungsten, to a strong electric field. The electric field will be enhanced at the tip, and electrons will be ripped out of the metal. Both of these methods can be used to create a source, called an electron gun, for imaging electrons. The electrons generated by the gun will then be subjected to a high-voltage field, and accelerated through the microscope's column. Voltages applied are on the order of tens of kilovolts for SEM. The inside of the column is kept at vacuum levels, since the electrons would interact and be scattered by any atoms or molecules that it would encounter, making it impossible to focus.[30]

The focusing is done by magnetic lenses. These will focus the electrons into a tight beam and eventually a small spot at the surface of the sample. The focusing effect is stronger if the electrons have a higher energy, which results in a smaller possible spot size with higher accelerating voltage. Due to the image being built up by measurements of each spot individually, a smaller spot size gives a higher resolution for the resulting image.[30]

2.5 Ellipsometry

Ellipsometry is a measuring technique that characterises properties of a thin film by studying changes in polarization of light when reflected on or transmitted through the film. There are a lot of different parameters that can be measured using ellipsometry, such as film thickness, refractive index, surface roughness and composition. Since the measurement is performed using a beam of light, the method does not require any physical contact, as well as not risking causing damage to the possibly sensitive thin film.[35]

A typical setup consists of a light source, followed by a polariser, which together produce a light beam with a selected linear polarisation. This beam then impacts the sample, being either transmitted through or reflected by the thin film. The beam is then passed through an analyser, which consists of another polariser, before hitting a detector that generates a signal. Information gathered by the tool include both the intensity measured and the azimuthal angles of the pre-sample polariser and analyser. This can be used together with known parameters for the sample to give a measurement of layer thickness or other optical parameters.[35]

3 Experimental details

In order to find a process yielding an acceptable etch selectivity between Si and masking material, Si wafers were prepared by Electron Beam Lithography, patterning a layer of 250 nm thick, positive tone AR-P 6200 resist. This provided the resolution required for defining the sub 100 nm features. After developing, the resist thickness was measured using ellipsometry before the samples were etched in an Apex SLR ICP-RIE from Plasma-Therm. The recipe used was changed between etch runs in order to determine the effects of the different etch parameters on etch results. The initial conditions were taken from the results

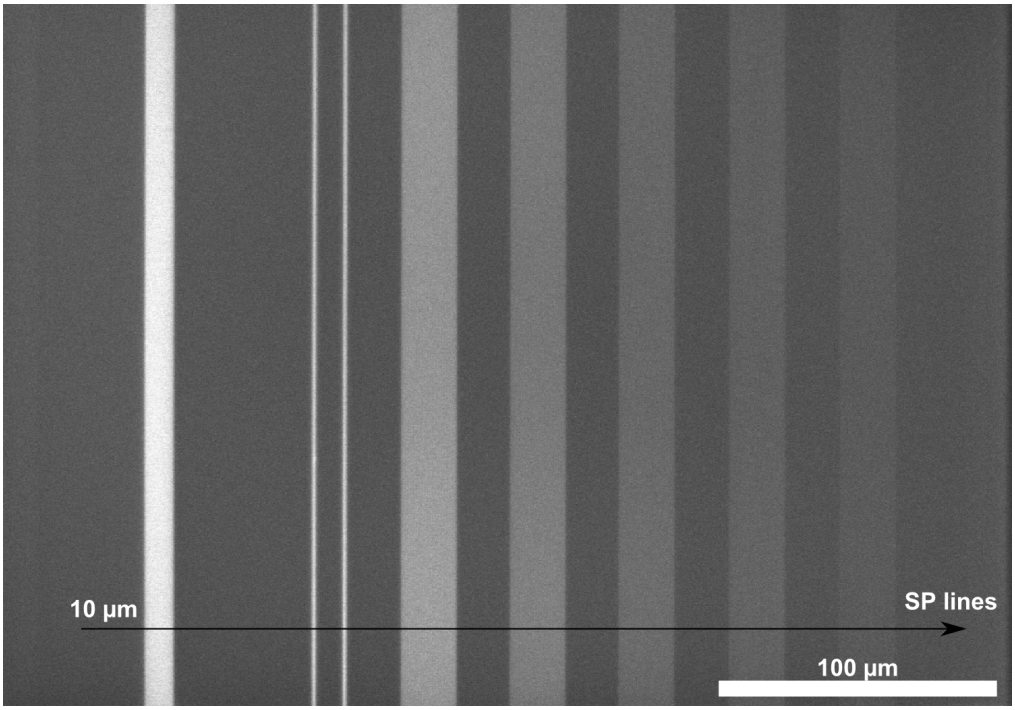

Figure 12: An overview SEM image of a sample coated with AR-P 6200 and EBL-defined lines as described below.

presented by Yung-Jr Hung et al,[36] due to the similarities in the etching systems dimensions and ICP coils, and the promising results shown in the report, with Si to resist etch selectivity of 16 or above. However, since etch systems are always different, it was decided to start with Cr hard-masked samples to ensure that the process works on Si, before moving to a soft polymer resist mask. This is to determine how the soft mask reacts to the etch conditions, and give a value for the etch selectivity. After the etching stage, the resist thickness was once again measured, to determine the amount of resist removed during the etching stage. The samples were cleaved, and the cross-section was examined using a SEM, where the etch depth in Si as well as the sidewall structure was examined.

In conclusion, during this project, a number of different etch masks were used. The specific details of each Si sample is as follows:

- **Si with Cr nanodot hard mask.** A Si wafer was spin-coated with TU-7 polymer resist, and then patterned using an Obducat nanoimprint lithographer to form 200 nm wide circular holes in a polymer resist. Chromium was evaporated onto the sample. The resist was removed, removing all Cr deposited on top of it, only leaving the Cr deposited in the bottom of the holes. The wafer was diced into samples of around 12 by 12 mm.

- **Si with EBL defined lines in AR-P 6200 polymer resist.** A Si wafer was spin-coated with an electron beam sensitive resist, AR-P 6200, with a thickness of around 250 nm. The resist was patterned in a Voyager EBL (Raith GmbH) with a series of lines, see Figure 12, all being 8 mm long, from left to right:

  - One 10 µm wide line.
  - Two 1 µm wide lines, pitch 11 µm.
  - 20 200 nm wide lines, pitch 1 µm.
  - 20 100 nm wide lines, pitch 1 µm.
  - 20 50 nm wide lines, pitch 1 µm.
  - 20 30 nm wide lines, pitch 1 µm.
  - 20 single pixel wide lines, pitch 1 µm.

  The wafer was then diced into smaller samples of around 12 by 15 mm, each sample containing all of the features above, with the longer side being parallel with the lines.

- **Alumina-infiltrated AR-P 6200 on Si.** These samples are identical to the previous sample, except that they were subjected to a SIS treatment. The recipes for the SIS are outlined below.

- **Alumina-infiltrated block copolymer on Si.** These samples consist of a block copolymer, polystyrene-co-poly methyl methacrylate (PS-b-PMMA), coating on a Si wafer. The thickness of the BCP layer was measured to around 45-50 nm. The coated wafers were provided by a research group in Barcelona. The block copolymer was deposited in a random lamellar structure, with no additional patterning performed. The wafers were processed with SIS before being cleaved into samples of around 10 by 10 mm, by scratching a small notch with a diamond pen and snapping the wafer along the crystal lattice.

- **Prototype Si master stamp.** A single 2 inch Si wafer was spin coated with the AR-P 6200 resist, and patterned in the EBL. The pattern consisted of 8 arrays of hexagonal holes. Each array used a different dose level in the EBL, to make sure that at least one array was properly patterned, and the lithography was not the factor that would make or break the result.

3.1 Recipe formulation - Cr mask on Si

Because the etch system that was to be used was newly acquired, there was no recipe available for etching of silicon. Therefore, the first step was to develop

this. The initial conditions was based on a published article,[36] where the etch chamber had similar dimensions and ICP coils, as well as the same gas mixture. These conditions are displayed in Table 1. The total flow of SF_6 and C_4F_8 was kept at 80 sccm for all etch tests. Thus, when talking about the flow relation between SF_6 and C_4F_8, the values will be displayed as (flow of SF_6 in sccm)/(flow of C_4F_8 in sccm). As an example, the relation in Table 1 would be 26/54. The initial experiments were conducted using the CR-masked samples.

Table 1: The initial etch conditions, based on the report by Y. Hung et al.[36]

Flow SF_6	26 sccm
Flow C_4F_8	54 sccm
Flow Ar	20 sccm
ICP power	800 W
RF/platen power	9 W
Process pressure	19 mTorr
Process temperature	20 °C

After etching in a Plasma-Therm APEX SLR ICP-RIE system for 4 minutes, the samples were cleaved and the cross section was examined in a Hitachi Su8010 SEM to measure the etch depth. Etch conditions were altered to get an optimal Si etch rate of 30-50 nm/min. This is where the etch rate is high enough to not require hour-long etching processes, while still keeping the etch depth easily tunable by altering etch times.

3.2 Recipe formulation - soft resist mask on Si

When a suitable Si etch rate was found, the samples were exchanged to the Si masked with AR-P 6200 without any SIS processing. The samples were studied with a Woollam M200VI ellipsometer both before and after etching to determine the difference in thickness of the resist layer. These samples were etched for 3 minutes, in order to reduce the chance of completely removing the polymer resist, which would make it impossible to accurately determine removal rate of resist. Etch depth in the silicon substrate was determined by cleaving the sample across the lines, and studying the cross-section in the SEM. Alterations of the recipe were then made based on this data, with the focus being on the flow of etching SF_6 gas, the passivating C_4F_8 gas and the power supplied to the RF field generator.

3.3 Improving etch selectivity - SIS on AR-P 6200

After the recipe formulation, further techniques to improve the process results were considered. Attempts at infiltrating the resist film with alumina were made, to try to increase the resistance to physical etching. The recipe was based on results from a research group in Barcelona, and designed for use on polystyrene-b-poly(methyl methacrylate). It was also considered lowering the etch temperature. Further infiltration tests were performed on a sample of polystyrene-b-poly(methyl methacrylate).

Table 2: Recipe used for SIS by the Barcelona group.

Temperature	100 °C
N_2 (carrier) flow	20 sccm
Pulse time	30 s
Purge time	60 s
Cycles	10

3.4 Etching of a prototype Si master stamp

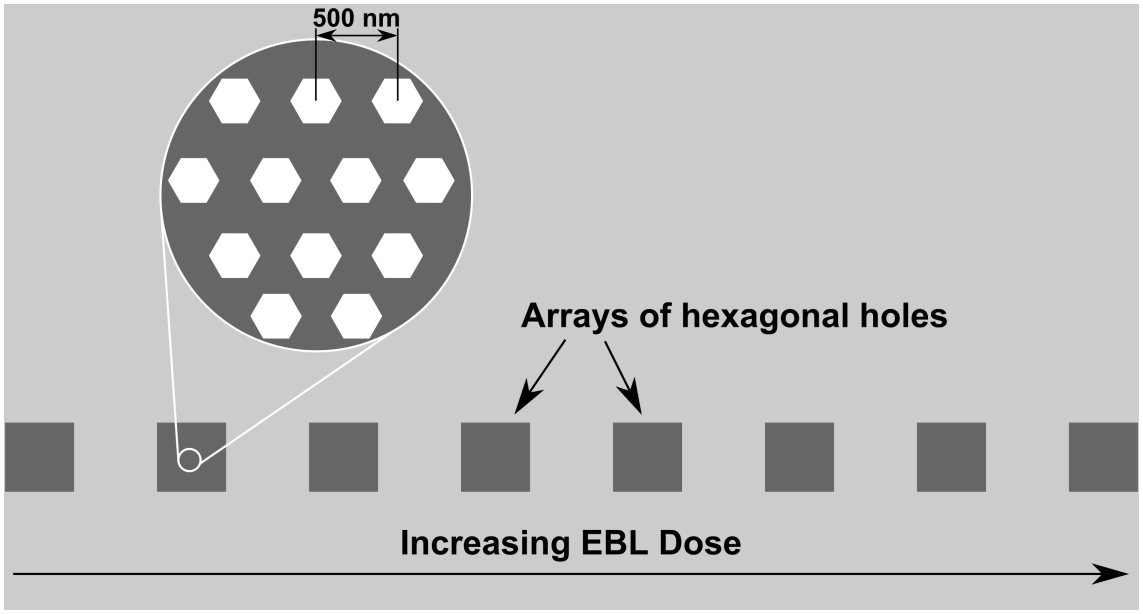

Figure 13: A sketch of the pattern used for the prototype stamp fabrication. Each dark grey box represents an array filled with hexagonal holes, shown in the magnifying circle.

A 2 inch SI wafer was spin-coated with AR-P 6200 resist and patterned with an EBL with structures consisting of arrays of hexagonal holes. The entire wafer was then etched using the best etch recipe achieved. The stamp was then cleaned of the remaining resist, and tested by using it in an imprinting procedure with a polymer intermediate formed by thermal imprint in a plastic sheet. Creation of intermediate stamps using UV-curable Ormostamp resist was also tested. These intermediate stamps were then used to imprint a Si wafer spin-coated with TU7 resist:
The Si wafer was placed in the imprinting tool, and the IPS was placed on top. The stamp was then pressed towards the wafer with a pressure of 20 bar and exposed to four 5 seconds flashes of UV light, while kept at 75 °C. The stamp was then removed from the wafer. The wafer was baked for 120 seconds at 95 °C to remove any remaining solvent from the resist. The resulting imprinted pattern was then examined in optical microscopy to study macroscopic defects, and in SEM to see the structure of the hole arrays.

4 Results

4.1 Recipe formulation - Cr mask on Si

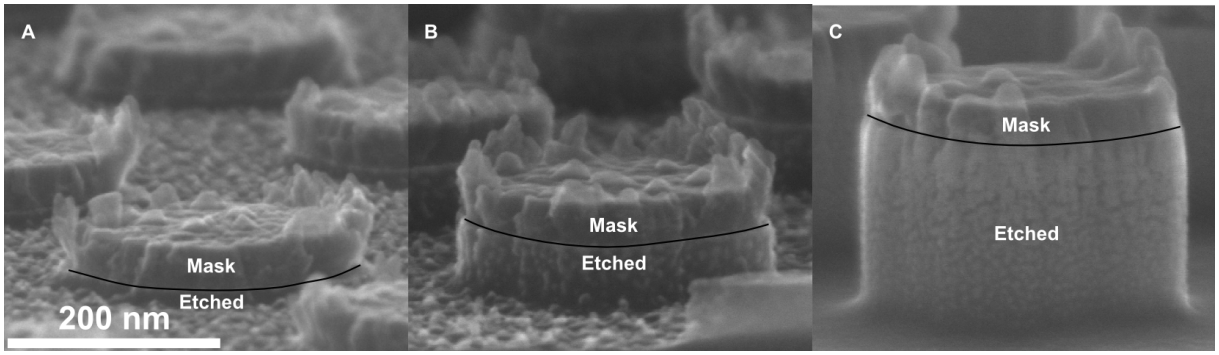

Figure 14: Etch results from primary tests on Cr-masked samples. (A): Initial conditions with RF power of 9 W and flow ratio of 26/54, full recipe outlined in Table 1. (B): RF power increased to 20 W and flow ratio SF_6/C_4F_8 changed to 30/50. (C): RF power increased to 60 W and flow ratio increased to 33/47.

The results from the initial tests on Cr-masked samples are shown in Figure 14. Figure 14A shows the results from the initial recipe shown in Table 1. We can see that the etch is very shallow, with an etch rate of 5.5 nm/min, and the surface is very rough. The roughness was thought to be caused by an ineffective removal of the passivating layer formed by the C_4F_8. To try fixing this, RF power was increased, thus increasing the physical etching caused by ion bombardment, which is the main effect removing the polymer. To attempt to increase the etch rate, a higher flow of etching SF_6, from 26 to 30 sccm, was tested, increasing the chemical etch effect. The results from this test is shown in Figure 14B. We can see that the Si etch rate is improved, this time the etch rate was measured as 8.25 nm/min, but still too low for any useful application, and the roughness is still too high. Thus, the SF_6/C_4F_8 ratio was increased further to 33/47, as well as the RF power to 60 W. This time, the results were looking good, seen in Figure 14C, with a sufficiently high Si etch rate of 50 nm/min. This recipe, shown in Table 3 was then used as a basis for the tests with the soft mask and examination of etch selectivity between Si substrate and polymer resist.

Table 3: The etch recipe giving the best results on Cr masked samples.

Flow SF_6	33 sccm
Flow C_4F_8	47 sccm
Flow Ar	20 sccm
ICP power	800 W
RF/platen power	60 W
Process pressure	19 mTorr
Process temperature	20 °C

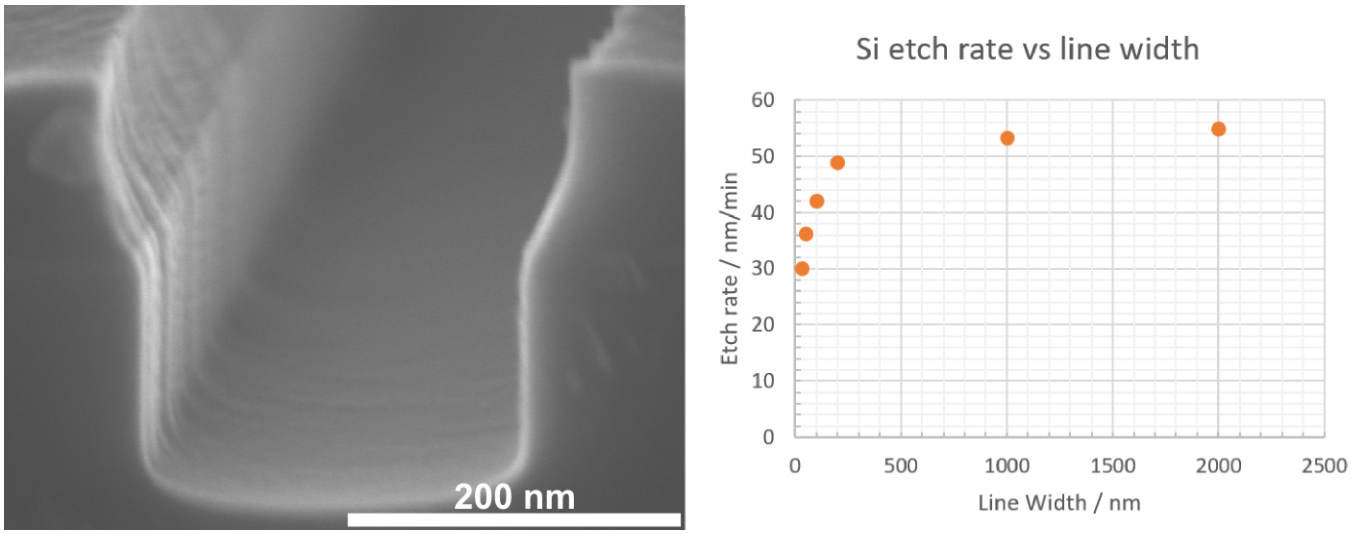

Figure 15: Left: SEM micrograph of a 200 nm wide line in Si on a sample with AR-P 6200 resist etched at the conditions in Table 3. Right: Graph showing the Si etch rate for the lines 30 nm to 10 µm wide. The aperture effect is clearly visible, with a rapid drop-off in etch rate below 200 nm. The 10 µm point has been placed at 2000 nm nm to allow for a greater separation of the 30-100 nm points.

4.2 Recipe formulation - soft resist mask on Si

Now that a recipe that worked well for etching Si had been developed, it was necessary to see how it would affect a soft mask, that may be removed by the etch. Figure 15 shows a micrograph of one 200 nm wide line from a sample etched at the conditions that were found to work well to etch Si, see Table 3. Figure 15 also shows a graph over the Si etch rate for all the lines. We can see that we have an etch rate above 50 nm/min for lines wider than 200 nm, while the etch rate drops off rapidly below 200 nm, eventually reaching 20 nm/min for the 30 nm lines.

The dependence of etch rate as a function of the size of an opening is called the "aperture effect". For a reaction to take place, the reactive species needs to be transported to the surface, and the products of the reaction also needs to be removed. Small openings limit the flow of both of these gases, so that a lower amount of etching gas actually reach the bottom of deep, narrow structures, severely limiting the etch rate. This must be taken into account when choosing processing times for a sample. The resist removal rate, measured via ellipsometry, is equal across the sample, and was found to be 37.3 nm/min for the sample. This gives a Si-to-resist etch selectivity of from 0.81 for the 30 nm lines, to 1.5 for the 10 µm lines. This is a relatively low selectivity, especially compared to the results displayed in the report where we obtained the initial recipe,[36] which reported selectivity up to 16.

Since this recipe seems to work fairly well even for a soft mask, the next step was to study the process window. The most important parameters were identified

as the gas flows, both the ratio of SF_6 and C_4F_8 and the flow of Ar, and the RF power. Three additional values was chosen for further testing each for the flow

Table 4: Parameters for the process window trials. The 30/50 and 40/40 flow ratios are not tested with the 30 W or 90 W RF power values.

RF power	SF_6/C_4F_8 flow ratio
30 W	26/54 sccm
40 W	30/50 sccm
60 W	33/47 sccm
90 W	40/40 sccm

ratio and the RF power, both above and below the current values. The chosen values are displayed in Table 4. Not all of the possible combinations in Table 4 were tested, due to limited time. The trials were divided into **RF power trials** and **flow ratio trials**. The RF power trials included the combinations between

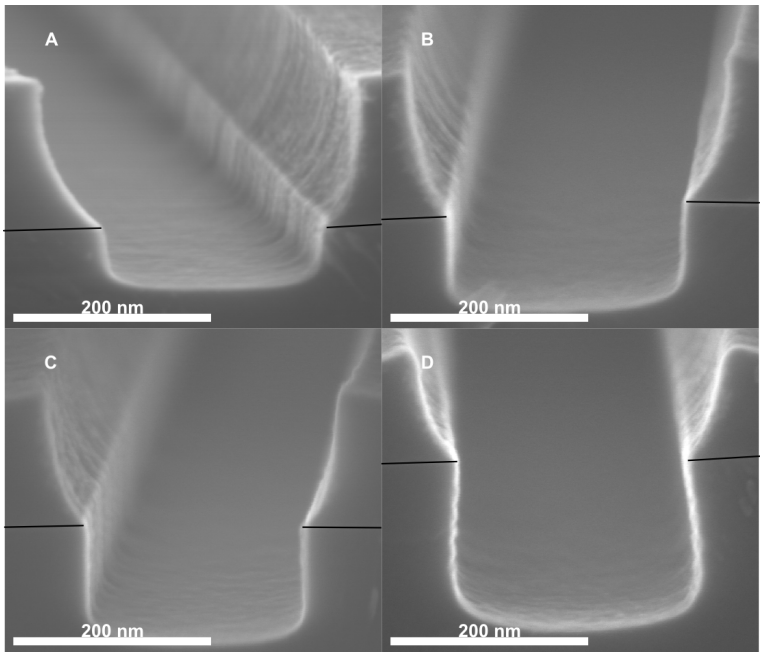

Figure 16: SEM micrographs of the etch results when using RF power of 40 W, while changing the flow ratio. For increased visibility, the resist-silicon interface has been marked with a black line. (A): flow ratio 26/54 (0.48). (B): flow ratio 30/50 (0.60). (C): flow ratio 33/47 (0.70). (D): flow ratio 40/40 (1.0).

flow ratio of 26/54 and 33/47, together with all the RF power values.

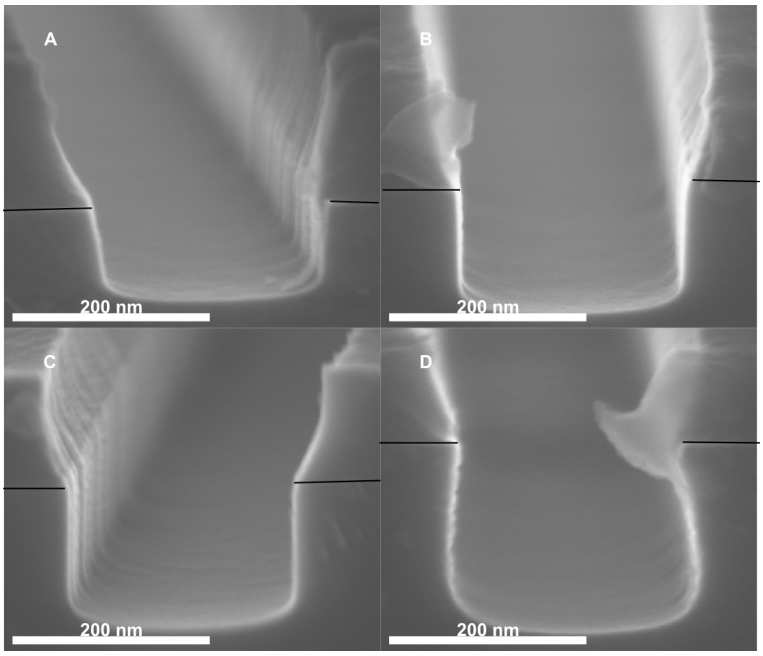

Figure 17: SEM micrographs of the etch results when using RF power of 60 W, while changing the flow ratio. For increased visibility, the resist-silicon interface has been marked with a black line. (A): flow ratio 26/54 (0.48). (B): flow ratio 30/50 (0.60). (C): flow ratio 33/47 (0.70). (D): flow ratio 40/40 (1.0).

The flow ratio trials were the combination between the RF powers of 40 W and 60 W, together with all the flow ratio values.

The result from the flow ratio tests, shown in Figures 17 and 16, showed an increase in etch rate for both the Si and the resist when the amount of SF_6 increased. However, the Si etch rate increased to a greater extent, thus increasing the overall etch selectivity. This can be seen more clearly in Figure 18.

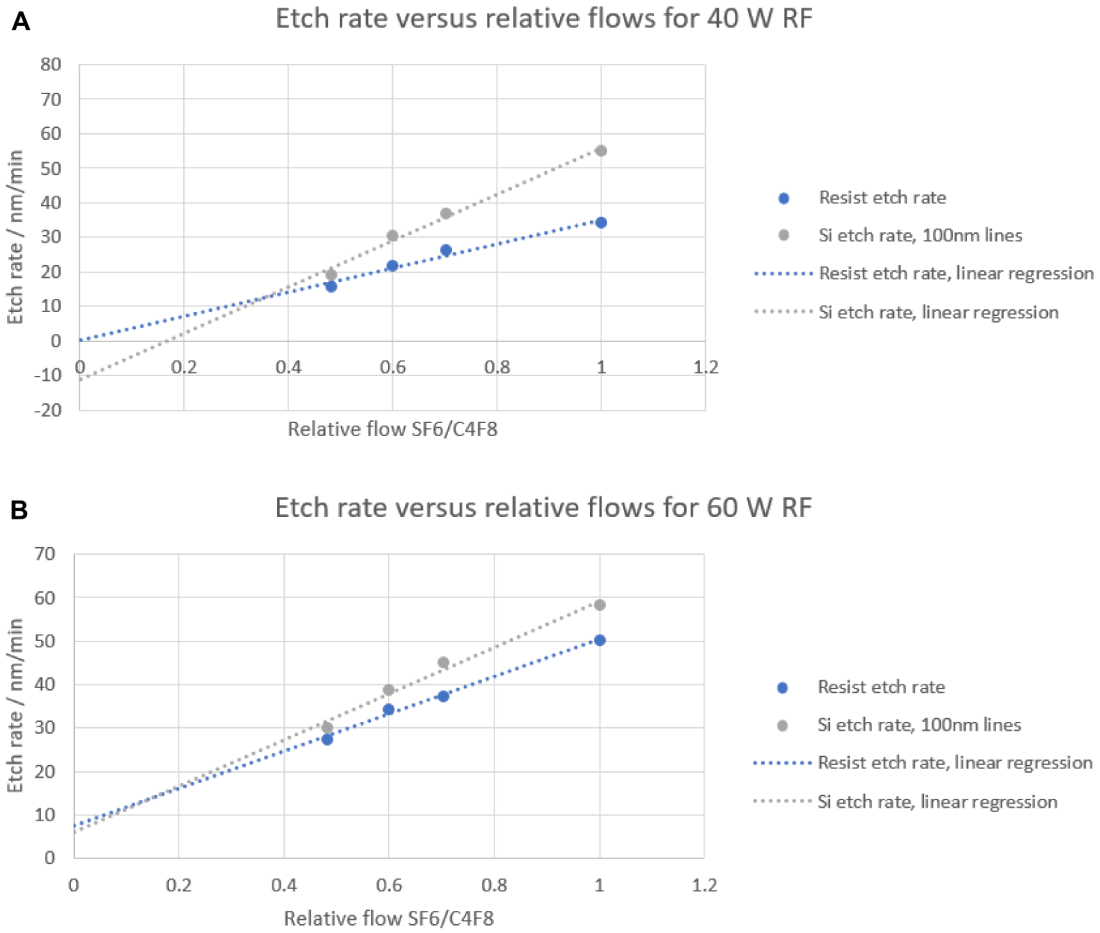

Figure 18: Etch rate of the AR-P 6200 resist and 100 nm lines when varying the flow ratio and keeping the RF power constant. A shows the results for a RF power of 40 W, and B shows the results for a RF power of 60 W.

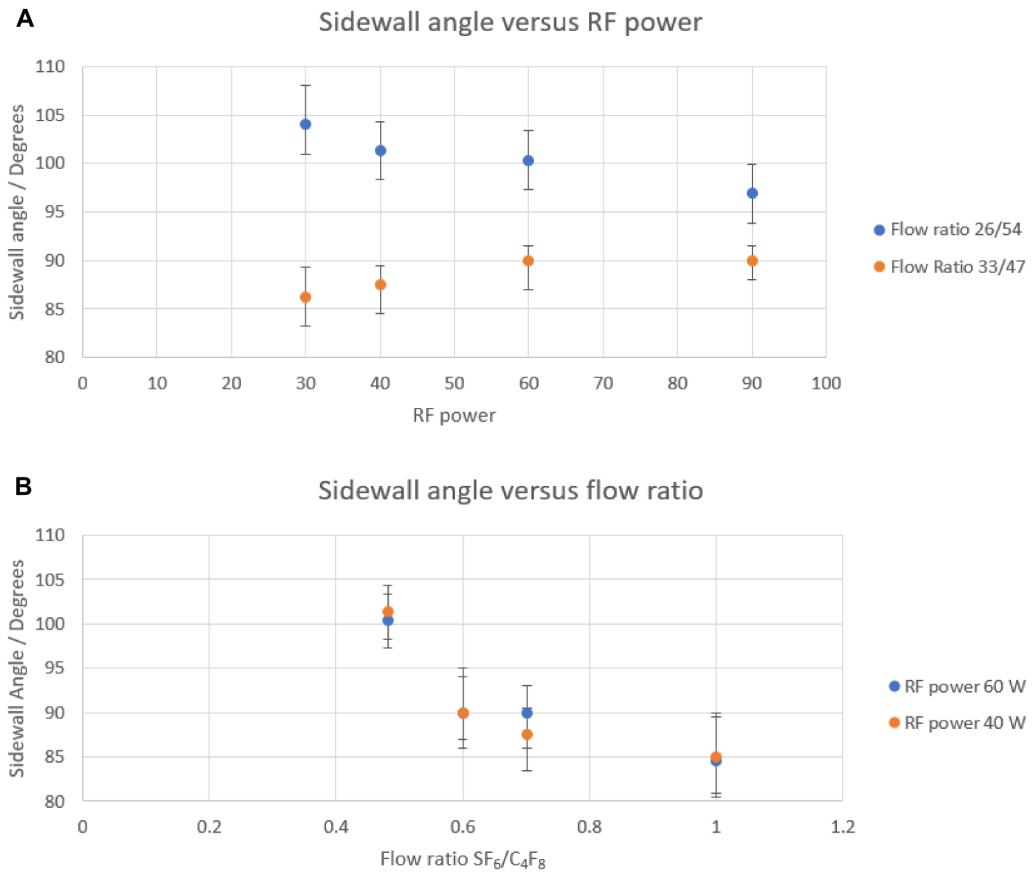

Figure 19: Graphs showing the effects on sidewall angle when changing the parameters in the experiment. A shows the change in angle when altering the RF power, while B shows the effects when changing the flow ratio. Each data point is made up of 4-7 measurements on two or three samples, error bars show highest and lowest values.

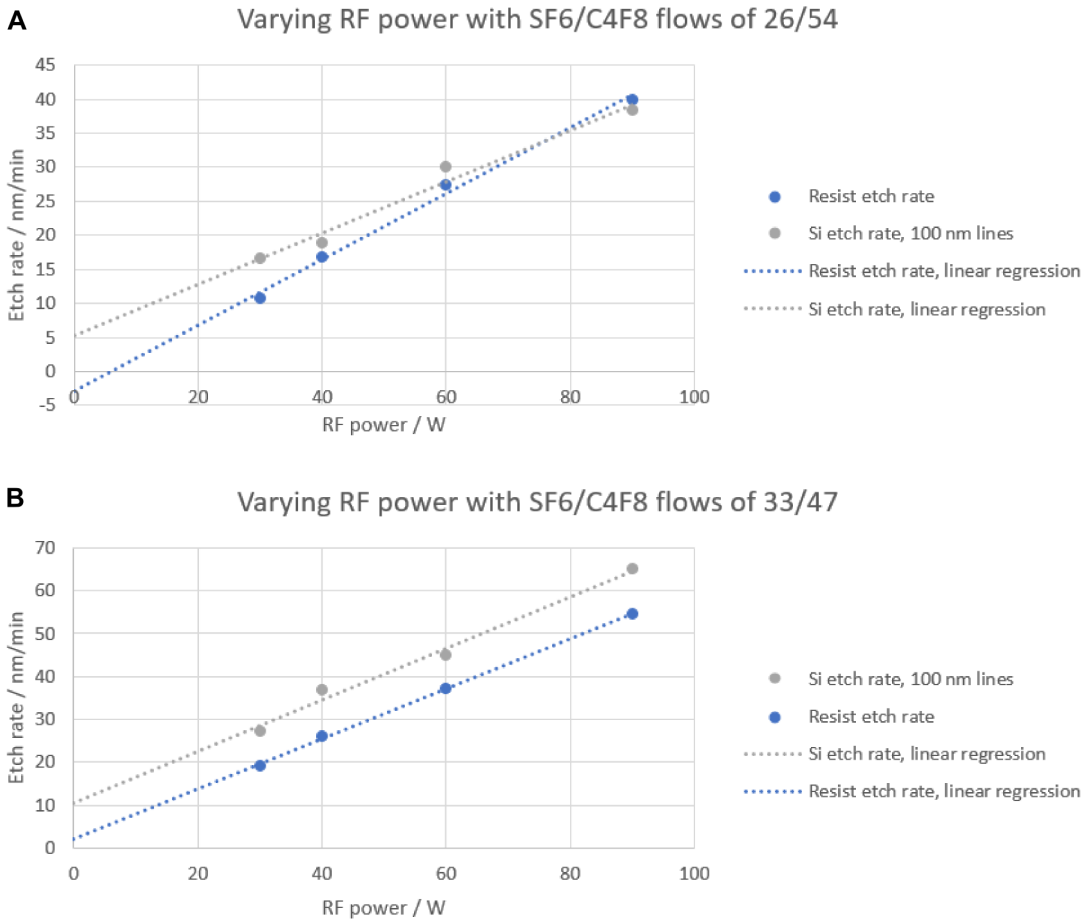

Figure 20: Etch rate of the resist and 100 nm lines when varying the RF power and keeping the flow ratio constant. A shows the results for a flow ratio of 26/54, and B shows the results for a flow ratio of 33/47.

Here we can also get a feel for what happens at a flow of 0 sccm SF_6, by extrapolating with a linear fit. For the series at 40 W, the resist etch rate goes down to 0 nm/min, while the Si etch rate goes below 0. Of course, this does not mean that additional Si would deposit, but it may be a net deposition of fluoropolymer from the C_4F_8 on top of the silicon in the narrower trenches, effectively reducing the depth of these trenches. For the 60 W series, both the Si and resist etch rates end at 6-8 nm/min at 0 sccm SF_6.

A direct impact on the anisotropy was also visible. We can see the graph showing the angles versus flow ratio in Figure 19B. There were no big differences between the 60 W and 40 W series; the same trend was visible. The angle goes from 102 degrees at a flow ratio of 26/54 down to 85 degrees at flow ratio 40/40. In Figure 19, we can see the angles of the sidewalls for the different test conditions performed. The angles were calculated by measuring the deviation from vertical sidewalls. In Figure 19B the relation between sidewall angle and flow ratio is

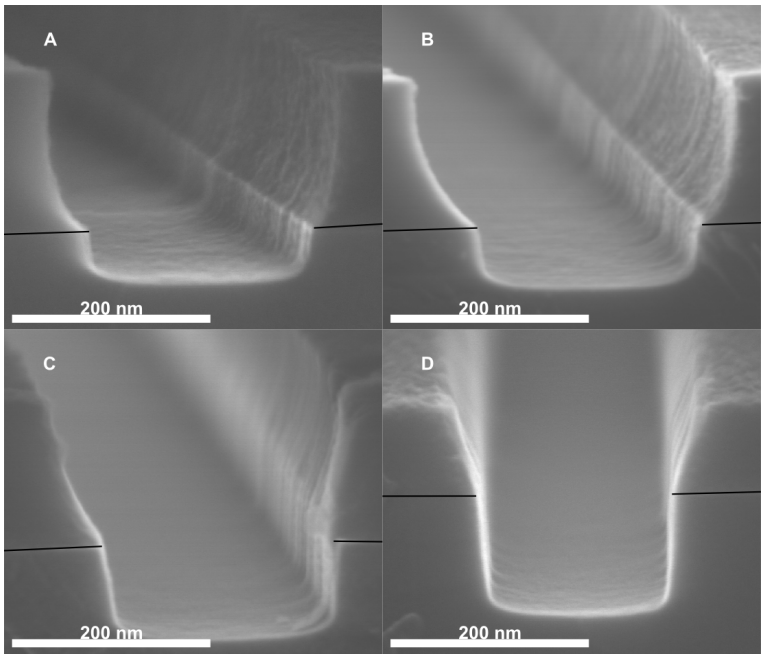

Figure 21: SEM micrographs of the etch results when using SF_6/C_4F_8 flow ratio of 26/54, changing the RF power. For increased visibility, the resist-silicon interface has been marked with a black line. (A): 30 W RF power. (B): 40 W RF power. (C): 60 W RF power. (D): 90 W RF power.

shown. It seems that fully vertical sidewalls occur at around the ratio of 30/50 SF_6/C_4F_8.

The RF tests, shown in Figures 21 and 22, showed that increasing RF power values also increased the etch rates of both Si and resist. Plots showing these changes are shown in Figure 20. This time however, the resist etch rate increased faster, resulting in a lower overall selectivity. There was a small effect on the sidewall profile present for the RF power test. In Figure 19A we can see the effect on sidewall angles from RF power for both the 26/54 flow ratio and the 33/47 test series. The angles for the 26/54 series start at 104 degrees at 30 W RF power. The angle then decreases and reaches 97 degrees at 90 W RF power. For the 33/47 series, the angle instead starts at 86 degrees at 30 W, and increases to 90 degrees at 60 W and above. There is no measurable difference between the 60 W and 90 W samples. When approaching lower values, there was a noticeable increase in Si surface roughness, similar to the results on the Cr-masked samples.

4.3 Improving etch selectivity - SIS on AR-P 6200

Sequential infiltration synthesis of alumina (Al_2O_3) has been reported to increase the stability in plasmas for some resists.[33] A few attempts at infiltrating the AR-P 6200 resist with alumina (Al_2O_3) were made. One with the recipe in Table 2, one with a higher temperature of 115 °C, and one with 15 cycles. After SIS processing there were no colour changes visible for the resist layer, which

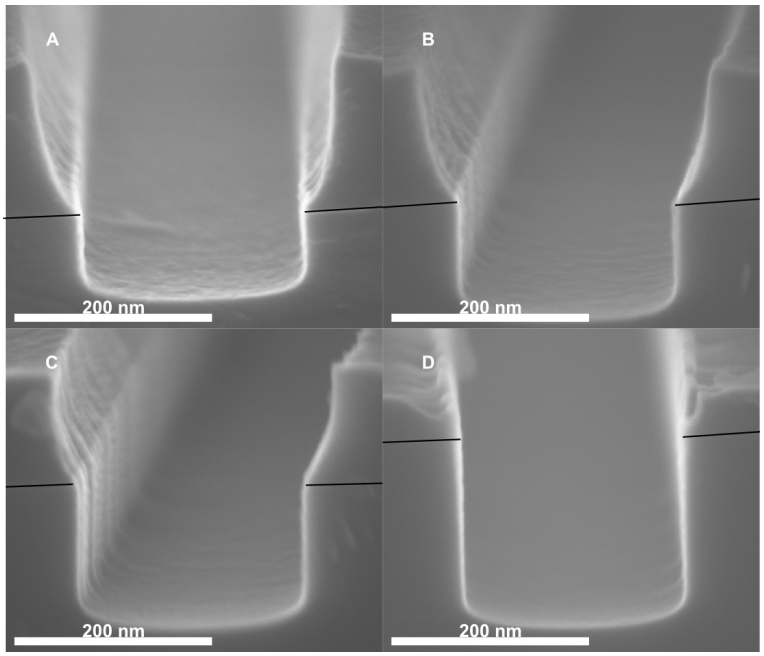

Figure 22: SEM micrographs of the etch results when using SF_6/C_4F_8 flow ratio of 33/47, changing the RF power. For increased visibility, the resist-silicon interface has been marked with a black line. (A): 30 W RF power. (B): 40 W RF power. (C): 60 W RF power. (D): 90 W RF power.

would be an indication that the composition had changed, and the optical properties with it. Measurements taken after subjecting the samples to the etching process showed that the etch rate of both the resist and the Si decreased, consistent with an alumina layer deposition on the surface. The decrease in etch rate was similar for both areas, with around 10 nm/min decrease for both the 10 cycle samples and 15 nm/min for the 15 cycle sample. In conclusion, this means that the selectivity improving effects that was hoped to be achieved with SIS were not present or visible for these trials.

Table 5: Etch rates for the SIS-modified samples.

	No SIS	SIS, 10 cycles 100 °C	SIS, 15 cycles 100 °C	SIS, 10 cycles 115 °C
Si etch rate (micron lines)	31 nm/min	19 nm/min	15 nm/min	19 nm/min
Si etch rate 100 nm lines	26 nm/min	19 nm/min	15 nm/min	20 nm/min
Resist etch rate	25 nm/min	18 nm/min	15 nm/min	18 nm/min

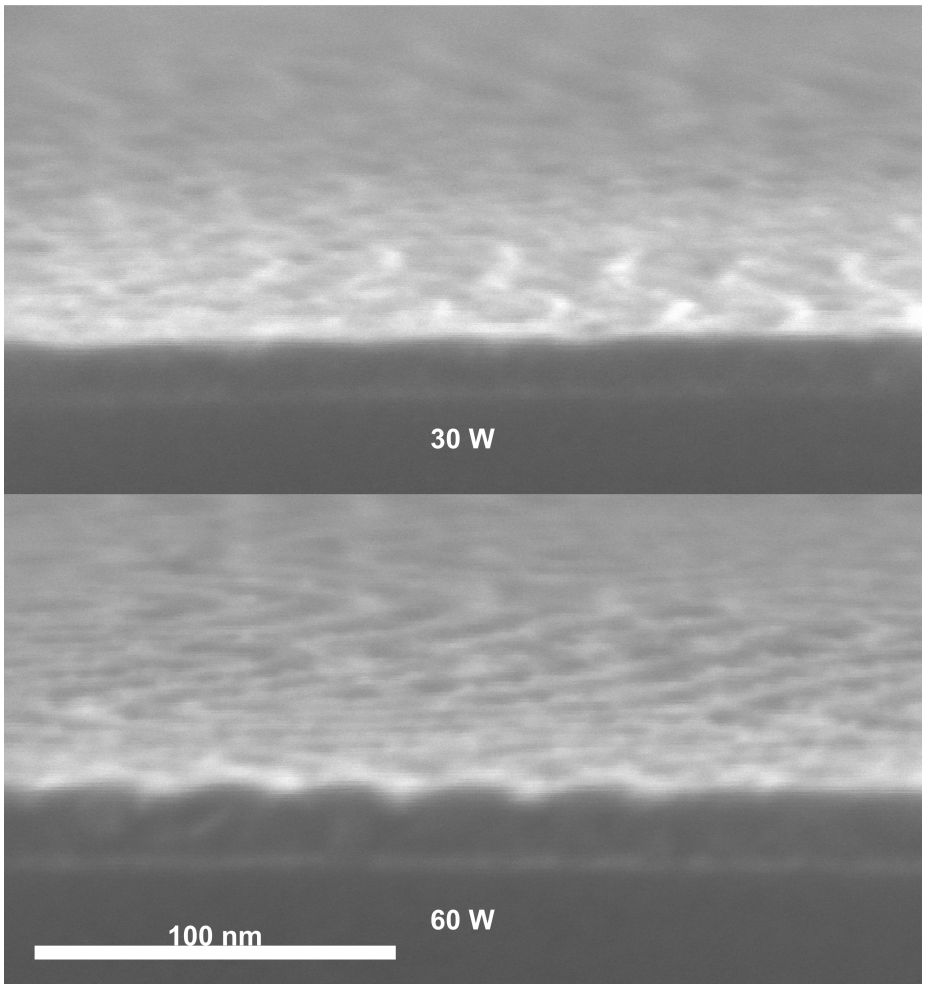

Figure 23: The results from infiltration of PS-b-PMMA mask. Both are using the 26/54 flow ratio, with different RF powers. Top: 30 W, bottom: 60 W. Both were etched for 1 minute 30 seconds.

4.4 SIS on block-copolymer

To see if our recipe for the infiltration process works in situations previously confirmed to work, we tried to use it on a polystyrene-poly methyl methacrylate (PS-b-PMMA) block copolymer. During the SIS process, alumina will be incorporated into the PMMA block only, leaving the PS part intact. RIE of Si under optimal conditions will remove the uninfiltrated areas faster than the alumina infiltrated areas, and give a easily visible structure of trenches in a lamellar ordering, which will be visible in SEM inspection. It may also result in pattern transfer into the Si substrate. Such a process can be used to make NIL stamps with ultra high resolution. A few different etch times were tested, to find the moment just before the infiltrated polymer portion is completely removed, in order to see the maximum achievable Si etch depth with this thickness. However, after testing etching times up to 1 m 30 s, results in Figure

23, the tests were aborted, as the etch rate difference between the supposedly infiltrated and un-infiltrated sections did not seem to differ significantly much to warrant further testing at the time.

4.5 Etching of a prototype Si master stamp

Table 6: The etch recipe which gave the best compromise between an etch rate allowing for easy tuning of etch depth, positive sidewall angles allowing for easier demolding and sufficient etch selectivity between silicon substrate and polymer resist to allow for the etch depth to reach high enough values to allow for stamp structures to be formed. Lower values of RF power may also be used, down to a minimum of 30 W if higher selectivity is required, but this may impact etch rate, especially for small structures.

Flow SF_6	26 sccm
Flow C_4F_8	54 sccm
Flow Ar	20 sccm
ICP power	800 W
RF/platen power	60 W
Process pressure	19 mTorr
Process temperature	20 °C
Measured etch rate	30-33 nm/min
Measured etch selectivity	1.0-1.2
Etch time	7 min

To verify the developed process, a test Si master stamp has been manufactured; A pattern of hexagonal holes was patterned using EBL into an 250 nm thick AR-P 6200 polymer resist. RIE was performed on the wafer using the recipe shown in Table 6. Two different intermediates were fabricated, an Ormostamp casting and an IPS imprinting, that were then used to imprint a wafer coated with a TU7 polymer resist using a UV imprinting process, as detailed in Section 3.4. The results from imprinting with the Ormostamp intermediate stamp can be seen in Figure 24. We can clearly see large defects with uneven resist thickness

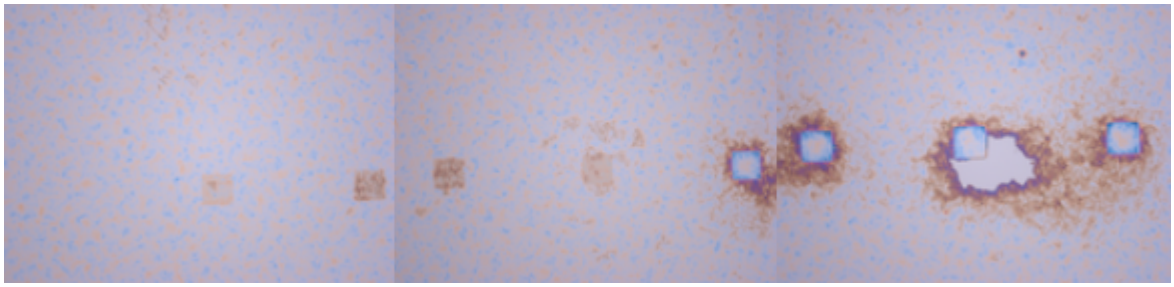

Figure 24: Optical microscopy image of the results from the imprinting with the Ormostamp intermediate stamp. The squares are the arrays of holes. The EBL exposure dose for each square is different, with the highest dose farthest to the left, and the lowest dose farthest to the right.

or even completely removed resist across all of the sample.

On the other hand, the imprinting performed using a IPS stamp did not show any significant defects in the optical microscope, see Figure 25. Thus, this

Figure 25: Optical microscopy image of the results from the imprinting with the IPS intermediate stamp. The squares are the arrays of holes. The EBL exposure dose for each square is different, with the highest dose farthest to the left, and the lowest dose farthest to the right.

sample was also examined in SEM to study the quality of the arrays on an individual basis.

In Figure 26 we can see the micrographs of four arrays of imprinted holes in TU7 resist, each of which with a different EBL exposure dose. We have the area with the lowest dose in Figure 26A, with the next dose level in Figure 26B. In the same fashion, Figures 26C and D shows the areas with the third and fourth lowest dosage respectively. The patterns created at dose levels above the fourth were destroyed by overexposure caused by proximity effects in the EBL. We can see that the holes are all of a different size, with the smallest being for the lowest dose at around 155 nm going through 190 nm for the second and 206 nm for the third dose levels, and the largest being 238 nm for the fourth dose level. We can also see that the imprinting from the fourth area is defective, as the walls of the holes are not horizontal like the other three areas.

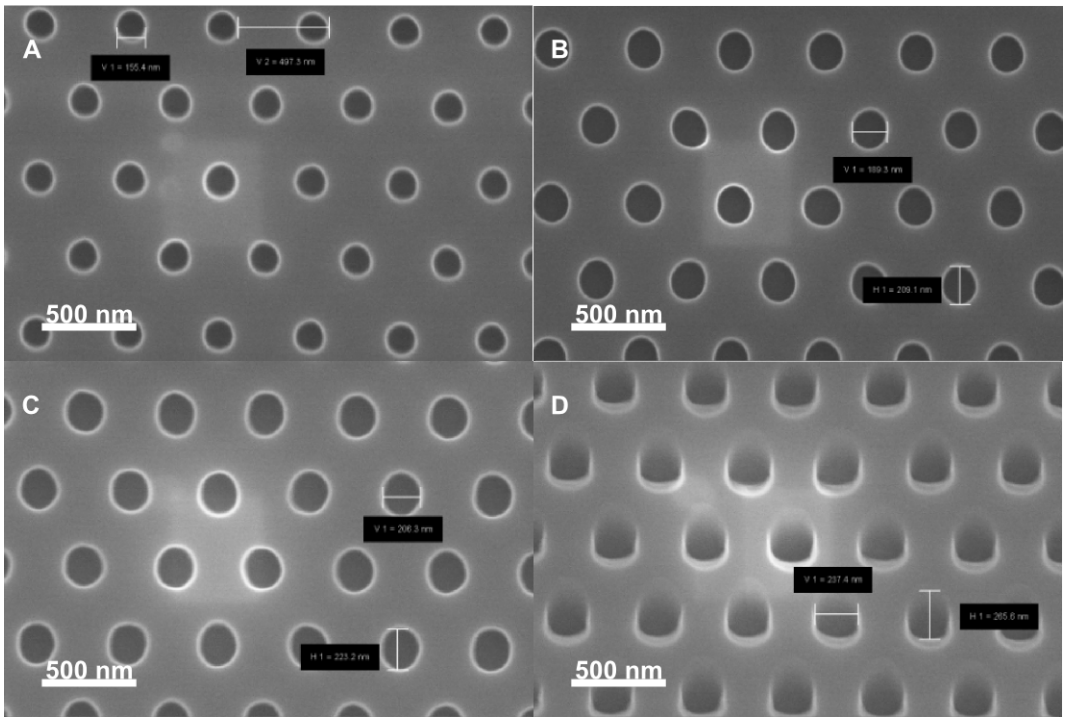

Figure 26: SEM micrograph of the arrays printed using the IPS stamp. The different images shows the results from different EBL exposure doses, with image A being the lowest exposure used, with increasing doses up to image D being the fourth lowest. All other doses above this fourth lowest were unusable due to overexposure in the EBL destroying the pattern.

5 Analysis and Discussion

5.1 Recipe formulation

In general, there are some trends visible for each of the parameters. The RF power showed a direct correlation to selectivity; higher powers resulted in increased etch rates for both Si and polymer resist. However, the increase for the resist was proportionally higher, resulting in an overall decrease of selectivity. We could also observe an increased surface roughness at low RF powers, most likely due to an insufficient removal rate of deposited C_4F_8 locally preventing the SF_6 from etching.

The flow ratio also showed expected results: increased SF_6 flow increased Si etch rate, due to a combination of reduced surface passivation and an increase in etching fluorine plasma. Extrapolation down to 0 sccm SF_6 showed indications that there may be a net deposit of fluoropolymer in the bottom of trenches with a width of 100 nm and lower at lower RF powers, see Figure 18A, while the resist etch rate would be close to 0. For the higher RF power, shown in Figure 18B, the etch rates for both the resist and the Si ended up at 8 nm/min. This difference in etch rate at a 0 sccm SF_6 flow between the two RF powers makes sense, as the increase in RF power leads to a higher effect from ion sputtering, and thus higher etch rates. The increase in resist etch rate is also larger than for the Si, 18 nm/min compared to 8 nm/min, as the resist is much softer than the Si, and thus more vulnerable to the increased ion bombardment.

We could also see an effect on the sidewall angle, Figure 19B, where higher SF_6 ratios gave a more negative slope. This is easily explained, since etching with SF_6 is a purely chemical, and thus isotropic, etch process. The C_4F_8 is introduced to decrease the etching on the sidewalls, moving the entire process to more anisotropic conditions, and it is thus logical that an increase in SF_6/C_4F_8 ratio brings more isotropic characteristics. Vertical sidewalls occur around the ratio 30/50, meaning that for etching nanoimprint stamps, where slightly positive sidewalls is preferred, the ratio should be below this.

There was also an effect on sidewall angle from RF power, as can be seen in Figure 19A, however less pronounced. The effect also seems centred around 90 degrees, or vertical, sidewalls, with higher RF powers giving increased sidewall angles while below 90 degrees, and lowering angles when above 90 degrees. This can be explained by considering the properties of the physical etching by ion sputtering: Increased RF powers gives higher ion energies, and in turn increased etch rate by sputtering, a highly anisotropic process, giving vertical sidewalls. The higher RF powers do not affect the isotropic chemical etch rate as strongly, leading to an overall shift towards anisotropy, and moves the angles closer to 90 degrees. It is therefore not as useful to use for tuning the angles, as it can never take a gas mixture that creates a negative profile and give a recipe for positive sidewalls. For positive sidewalls, it is theoretically possible to use the RF power to fine-tune the angle, but it is more of a band-aid solution, as changing the flow ratio is arguably as easy, and finding the proper flow ratio gives a higher freedom for the other parameters. Also, as discussed earlier, the RF powers effects on resist removal, and thus etch selectivity, are much larger than on the sidewall angle, and therefore should be the primary consideration when choosing the RF power.

The series of experiments using the Cr-masked Si wafers gave the first surprise regarding the etcher setup and its' mechanics. The initial conditions were chosen due to the similar dimensions, chemistry and RF field generators, as well as the favourable results achieved in the study.[36] Their results showed a Si etch rate of 300-400 nm/min with a Si/resist selectivity of around 16 using a $SF_6/C_4F_8/Ar$ plasma mixture. However, the value for the vertical RF field power of 9 W proved wholly insufficient for our setup, and any reasonable etching conditions required at least 20 W, or even 30 W. Even going up to 60 W we only achieved an etch rate of around 50 nm/min, a huge 6 to 8 times lower than the report. While this was favourable in our case, since we wanted a lower etch rate to be able to control the etch depth easier, this huge difference in result between these supposedly very similar systems using the same recipe was concerning.

This difference also proved significant in the next test set, where a soft resist mask was used. These high requirements for RF power generated a substantial DC bias on the surface, upwards of 300 V at 60 W power. This brings with it a high degree of physical etching, which heavily reduces the stability of the polymer resist. The highest selectivity achieved, while still maintaining a usable etch rate and an acceptable surface smoothness, was around 2, with a RF power of 30 W.

5.2 Stamp Fabrication

Two different methods for NIL with an intermediate stamp were tried. The first one used Ormostamp resist to cast a intermediate stamp from the etched master stamp. This attempt did not yield any positive results. The TU7 resist was found to be uneven, or in some areas even completely absent, after imprinting with the Ormostamp intermediate, as can be sen in Figure 24. This is likely caused by the method with which the Ormostamp stamp is created. The Ormostamp resist was deposited as a single droplet, and then squeezed out across the rest of the wafer by a glass plate before being hardened with UV light. There is a risk that the distribution of the resist is not even, and these irregularities will become apparent when the intermediate is used for the actual imprinting process. This is most likely what has happened in this case.

The second process with the IPS stamp worked much better. There were no visible defects on the macro scale, and the resist distribution looks to be even. On the nanoscale, out of the four patterns that were actually usable, and not ruined by proximity effects in the EBL, only one of them showed systematic defects. This one, number 4, showed signs that the pillars in the stamp were bent when they imprinted the pattern. An explanation to this is that the pillars for this array were longer than the depth of the resist layer, and thus bent when they hit the Si substrate. One noteworthy fact is that the holes are larger for the bigger doses. This is caused in the EBL by the proximity effect, that increases the area where the electrons interact with the resist. Most of the dose will be absorbed in the centre of the beam, but some of it will be scattered and absorbed away from the beam impact area. The further away a point is from the beam centre, the lower the chance for the electron to reach it. However, a larger dose means that more electrons are available to be scattered, and that the area where the resist will be fully exposed increases. Thus, a bigger dose results in a larger hole that is accessible for etching. This helps to explain why the area

exposed with dose level four had pillars that were longer than the others, and long enough to go through the TU7 resist layer completely.

For RIE, there is an effect known as the aperture effect. For an area to be etched, it needs to be accessible for the etching radicals, that are accelerated by the RF field inside the etch chamber. The radicals will most likely not go straight down the normal of the substrate, as they will collide with the other molecules present in the etch chamber and be scattered away, similar to the electrons earlier. This means that etching radicals can come from any angle when reaching the surface. Small openings, such as holes or narrow trenches, limits the angles from where the radicals can come, and still reach the bottom. This means that a smaller hole will have fewer etching radicals reaching the bottom of the hole, and thus a lower etching rate. A smaller hole will also limit the rate at which the reaction products, containing the etched away material, can be removed from the surface. This means that the small size creates a bottleneck for the gas flow, further limiting reaction speed, and thus etch rate. When choosing the etching time, it is thus necessary to know the dimensions of the features that needs to be etched, as the etch depth can only be optimised for a specific hole size. In our case, the areas with a lower dose has a smaller hole size, due to the proximity effect mentioned earlier, reducing the etch rate. The etching time chosen for the etching of this test stamp was optimised to allow features of around 200 nm to reach a depth of 250 nm, meaning that larger features than 200 nm will be deeper than that. In this case they were deep enough to cause the pillars on the intermediate stamp to be too tall, causing problems during imprinting. This can therefore not be said to be a problem caused by a bad etching recipe, rather an etch time poorly optimised for all the features present.

However, one thing that needs to be considered is whether the aperture effect makes the process window for useful stamps with sub-300 nm features too small to be usable. For NIL to work best, the stamp features needs to be of the optimal height: short enough for the stamp features not to push through the entire resist layer and bend at the substrate surface, but also tall enough to leave a sufficiently thin residual layer. If a sample only contains features of a single size, for example a mask for deposition of seed particles for nanowire growth, this is not a problem, as the process is easily optimised. If it instead contains a combination of features with different dimensions, even a relatively small size difference gives rise to a large difference in etch rate, as can be seen in Figure 15, where the etch rate drops off rapidly below the 200 nm mark, making the process harder to optimise. Because the widest features will always be the tallest, the etching will need to be optimised for these, resulting in that the smaller features will become more shallow, and gives a larger residual layer after imprinting. The effect can be reduced by minimising the thickness of the masking layer, which is why a thin masking layer and high etch selectivity is preferable over a thick mask and a low etch selectivity.

In the end, the process worked sufficiently well for it to be tested for fabrication of a prototype master stamp. We could fabricate this master stamp that was able to be used for patterning of a TU7 resist layer on a Si wafer using a standard Nanoimprint Lithography process, using an intermediate polymer stamp (IPS). We can therefore conclude that the recipe works for that which it is designed, and produces features of sufficient depth and sidewall angle for

de-moulding of the stamp to be feasible. And based on the trends discovered, this is likely close to the optimal conditions for this type of etching.

5.3 Sequential Infiltration Synthesis

Looking at the results from the SIS processed samples, it was clear that there was no improvement due to alumina infiltration. If we look at the actual numbers, after processing for 10 cycles, the etch rate was reduced by 10 nm/min for micron-wide silicon lines and 7 nm/min for the resist, and for the 15 cycle samples the Si micron-wide line etch rate was reduced by 15 nm/min and the resist etch rate was reduced by 10 nm/min. There was some etch rate reduction, but since the reduction was similar for both Si and resist, it seems that the reduction was due to alumina deposition rather than infiltration. However, when comparing the chemical composition of AR-P 6200 to that of ZEP 520a, which is a resist which SIS is proven to work for, we can see that both consist primarily of a co-polymer of α-methyl styrene and α-chloroacrylate. Since the infiltration is a chemical process, one would assume that it would work for both AR-P 6200 and ZEP 520a, given this compositional similarity. However, there may be a difference in which additives the two resists use, and these may affect the accessibility of the functional groups that are used in the alumina infiltration. Comparing different physical parameters, we can get an indication that there are differences in the overall product formulation. For example, the glass transition temperature for ZEP 520a is listed in the product description as 105 °C, whereas the glass transition temperature of AR-P 6200 is listed as 128 °C. However, it may also be that the SIS recipe is poorly optimised.

The tests on the PS-b-PMMA coated samples showed that the infiltration works to some degree. We could see that there were some structures etched into the BCP layer, that had a structure resembling the lamellar pattern from the resist layer, indicating that there were some selectivity in the infiltration, as expected. There were the same issue regarding the etch selectivity between unmasked (uninfiltrated PS) and masked (supposedly infiltrated PMMA) areas as with the pure AR-P on Si samples, shown by the extremely shallow etch result. There are many possible reasons as to why the effect is so small. For example, the high power that was needed to effectively etch Si gives a high bias voltage. This high voltage gives a significantly higher effect of sputtering, which we have already shown causes significantly worse characteristics for the normal resist. Another consideration is that the amount of cycles were too low to get any considerable amount of alumina into the resist. However, the test where the number of cycles performed on the AR-P showed no indication of increased alumina infiltration, only deposition, making this concern unlikely.

Based on these results, there are no direct conclusions that can be drawn regarding whether the infiltration actually does not work on the AR-P 6200 and the difference is small enough to be unnoticeable, or if it does not work at all. It may just be that the etching process developed is too aggressive for the infiltration to give any benefit.

5.4 The etch selectivity

The final issue that needs to be addressed if the reason why the high RF power was necessary. This is the most confusing problem of the project. We have examples of machines with similar dimensions and technical properties that shows results with higher Si etch rates together with lower resist etch rate, using significantly lower RF powers. Based on the fact that we developed a functioning recipe, with good sidewall angles, and the trends discovered when altering the parameters, this high RF power requirement is likely a feature of the machine. We could see an increase in selectivity when increasing the fraction of etching SF_6 gas, but this ruined the sidewall angle and would have made it impossible to de-mould a stamp. And the RF power was tested at low values, similar to other studies, but showed results with etch rates far below any useful values, coupled with poor surface smoothness. There are of course other parameters that could be tested, but seeing as there was such a big difference between our results and those of the study we based the initial conditions on, the problem, if you want to call it that, most likely lies with the machine rather than the recipe.

One difference between our system and the one used in the reference publication[36] is that our chamber has a few flanges added to allow for other processes to be performed in the chamber. This increase in chamber height changes the volume of the chamber, and thus increases the amount of gas in the chamber. As ions are primarily generated by the ICP coil in the top part of the chamber, this additional gas volume will be closer to the sample stage, and therefore unaffected by the ICP ionisation. This means that the ions generated at the top has to traverse a larger distance of unionised gas, which will give rise to more collisions and scattering. The frequency of scattering event are described by the mean free path, that denotes the average distance between collisions. Scattering events remove most, if not all, of the kinetic energy of the ions, requiring the ion to start accelerating again. If the mean free path of ions in the specified conditions was larger than the original chamber height, this means that on average, ions passed through the unionised gas without losing their kinetic energy. In this case, an increase in chamber height would result in a larger fraction of ions having been scattered at least once on their way from the ICP area to the sample stage, thus giving a lower average kinetic energy when impacting the surface. The chemical aspects of the etching is unaffected by this decrease, as they depend solely on whether the reactive species reach the substrate. This means that the deposition of fluoropolymer by the C_4F_8 is unaffected, but the removal of this is reduced as the main removal process, ion sputtering, is not as efficient. This results in a coverage of the area in this polymer, drastically reducing access for the etching fluorine species, giving an uneven etch. Increasing the RF power will increase the average energy of impinging ions and thus improve the removal rate of deposited fluoropolyer.

However, we also move closer to a conventional RIE system, where ion generation and acceleration are both handled by the vertical RF field. We thus get more ionisation in the areas outside of the ICP area, giving us more sputter ions, while also increasing the mean free path of ions, by reducing the fraction of unionised gas. Both these factors contribute to increase the effect of sputtering for resist removal rapidly, while only moderately increasing the chemical

etching component. This is not necessarily a linear process; the ionisation may very well have a threshold value, where ionisation by the RF field dramatically increases. This would make optimising the parameters for higher selectivity more complex, and require changing other parameters such as process pressure, substrate temperature or total gas flows.

6 Summary of Conclusions

A method for etching Si based nanoimprint master stamps based on ICP-RIE of EBL patterned structures was successfully developed. A test stamp was successfully produced and replicated in an Intermediate Polymer Stamp at Lund Nano Lab. This IPS was then also used to transfer the stamp pattern into a TU7 nanoimprint resist.

Etch selectivity for the Si NIL stamp etch process was at best 1.4 to 1, which is low, but sufficient for the application. A method for infiltration of the AR-P 6200 resist with alumina was tested to see if it would increase selectivity. The results did not show any reduction of the resist etch rate. The same process with infiltration and etching was tested on a resist that has been proven to work for infiltration, but the results were similar to for the AR-P 6200 samples, with low etch rate difference between uninfiltrated and infiltrated areas. Thus, no real conclusions could be drawn regarding the viability of alumina infiltration of AR-P 6200 resist.

The low etch selectivity was attributed to the high demands on the RF power for the etch process. Powers of more than three times those recorded in studies with similar etch systems were necessary. We attribute this to differences in the geometry of the etch chamber giving rise to differences in resonance for RF signals, as well as effects caused by an increased amount of gas that is not ionised by the primary ion source, the ICP coil.

This work opens up a possibility for in-house fabrication of NIL stamps, which should make fabrication of nanostructures at Lund Nano Lab both cheaper and easier. It also gives more knowledge on SIS and the conditions where it does not work, and contributes to the development of the SIS process by giving a bigger picture of the process window.

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Appendix

A Etch Recipes

Table 7: The etch recipe which gave the best compromise between an etch rate allowing for easy tuning of etch depth, positive sidewall angles allowing for easier demolding and sufficient etch selectivity between silicon substrate and polymer resist to allow for the etch depth to reach high enough values to allow for stamp structures to be formed. Lower values of RF power may also be used, down to a minimum of 30 W if higher selectivity is required, but this may impact etch rate, especially for small structures.

Flow SF_6	26 sccm
Flow C_4F_8	54 sccm
Flow Ar	20 sccm
ICP power	800 W
RF/platen power	60 W
Process pressure	19 mTorr
Process temperature	20 °C
Measured etch rate	30-33 nm/min
Measured etch selectivity	1.0-1.2

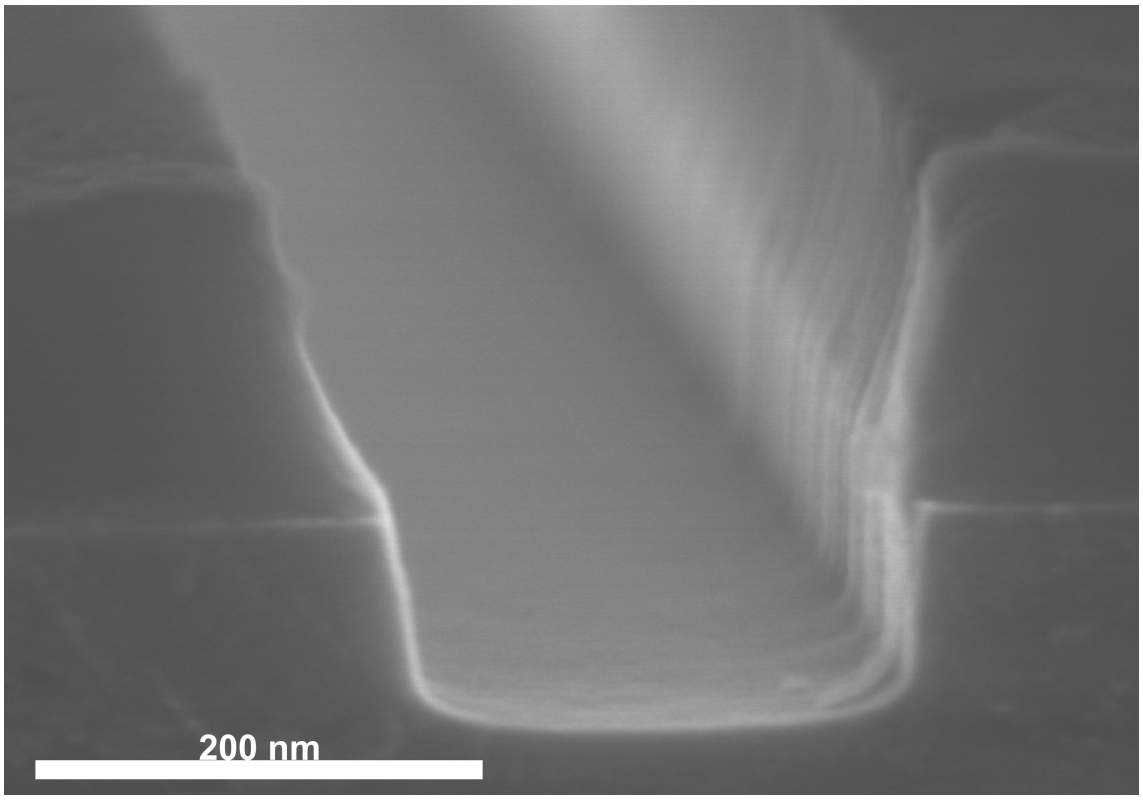

Figure 27: SEM image of a typical result using the developed recipe shown in Table 7.