A 100GHz Millimeter-Wave Voltage-Controlled Oscillators in III-V Nanowire Technology

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Abstract

This paper describes the design of III-V nanowire process inductor-capacitor tank (LC-tank) millimeter wave voltage controlled oscillators. Varactor, transistor and inductor designs are optimized and scaled to achieve the best performance of 100 GHz VCO. An investigation of trade-off between phase noise and tuning range for III-V nanowire varactor at 100 GHz has shown that the gate lengths between 20 and 100 nm result both good quality factor (16) and Cmax/Cmin ratio (1.87) in the III-V nanowire process used for the study. A 100 GHz VCO with a tuning range of 10.77 GHz, FoM(Figure-of-merit) at -183 dBc/Hz, phase noise of -113.883 dBc/Hz at 10-MHz offset and power consumption of 1.59-33.2 mW from a 1-V supply has been designed. This is the iii-v nanowire VCO with the highest fundamental operating frequency currently.

Index Terms ------ iii-v nanowire, millimeter wave, inductor-capacitor tank (LC-tank), nanowire varactor, quality factor, tuning range, FoM(Figure-of-merit), voltage-controlled oscillator(VCO)

Popular Science Summary

Voltage controlled oscillator (VCO) is a signal generator that output signal frequency controlled by the external signal voltage. The core component of VCO is varactor. When the voltage that added on the varactor changed, the output frequency will also changed gradually. The frequency of VCO is linearly related to the control voltage. With the rapid development of electronic technology, the application of VCO is more and more widely. For example, in the radio measuring instrument, it produces sinusoidal signal voltage of various frequency bands. Some electrical equipment is controlled by a contact-less switch that made of the VCO; In electronic clock and electronic watch, oscillation circuit with high frequency stability is used as timing component.

Furthermore, VCO provides actual output signal in PLL(Phase Locked Loop) and its performance directly determines the overall performance of PLL. The phase noise of VCO determines the output phase noise of PLL and the output frequency range of PLL is directly depend on frequency tuning range of VCO. In addition, the output spectrum purity of PLL also depends on the design of VCO and the power consumption of VCO occupied the majority of the entire PLL power consumption. Therefore, the research of VCO design has a significant meaning.

Acknowledgment

I would like to take this opportunity to thank a number of people who have offered invaluable assistance in the preparation of the thesis. I acknowledge with gratitude to Lars Ohlsson Fhager and Stefan Andric, my respective supervisor, who have always been sincere and helpful in guiding and encouraging me. I am deeply grateful of their help in the completion of this thesis. I also wish to express my gratitude to my beloved parents and friends for their loving considerations and great confidence in me all through these years.

CHAPTER 1

1. Introduction

1.1 This thesis

Modern electronic information technology is the basis of integrated circuit chips and constitute the integrated chip device unit are almost composed of silicon CMOS Field Effect transistor (Field Effect Transistors, FET). However, today's CMOS transistor technology is facing an unavoidable fact: it is approaching its physical limit. According to an assessment by the International Technology Roadmap for semiconductors (ITRS), the timeline is roughly a few years until 2020.[1] Under this situation, looking for the new material to replace silicon CMOS is becoming more and more urgent for semiconductor industry. Miniaturization of transistors below 5nm is one of the key issues in the semiconductor industry, as smaller transistors present a variety of challenges and the world is doing some in-depth research on this issue to overcome the challenges of future technological nodes.

At present, the main process used in the realization of millimeter-wave integrated circuit is III-V compound semiconductor technology , such as Gallium arsenide (GaAs) and Indium arsenide (InAs). The transistors produced by this sort of process have higher election mobility and breakdown voltage, high gain and low noise emission, and passive components produced have higher Quality-factor. Compared with III-V compound semiconductors, silicon-based CMOS devices have many disadvantages, such as low substrate resistance and channel electron mobility, low gain, poor noise performance, and low quality factor of passive

components. Compared with GaAs process' higher substrate resistivity , the lower substrate resistivity of standard CMOS process especially in the microwave and millimetre wave frequency band will cause greater loss of the circuit due to substrate coupling effect. Nevertheless, high polysilicon gate resistance value in CMOS process will introduce more noise and affect the gain of device. In millimetre wave applications, the distribution effect of device and the substrate loss effect will cause the system performance reduced greatly, so the traditional circuit design is not feasible anymore. What's more, the coupling effect of interconnection lines and the use of passive components will introduce more noise and reduce the gain. Therefore, the traditional silicon process for millimetre wave circuit is no longer feasible because of the great reduce of system performance.[2][3][4]

This paper implement the III-V nanowire transistors which have been illustrated in article [2] and [3]. Before this work, there are no documents and articles discussing the W-band VCO design that based on III-V nanowire technology. According to International Technology Roadmap for semiconductors (ITRS) in Fig 1, the III-V nanowire transistors will be fabricated and applied for industry around 2030. Therefore, the innovation of this paper is revolutionary.

In recent years, the voltage-controlled oscillator (VCO) around 100GHz in CMOS technology is motivated, [6] and [7] implement a conventional push-push configuration, [5] and[8] adopted a varactorless topology that tuning range achieved by change the supply voltage, [9] described the function of output buffer. At such a high frequency, the main difficulties of VCO design are wide tuning range, low phase noise and low power consumption. Especially, for a traditional millimeter wave VCO, there is a trade-off between phase noise and Q-factor for varactor. For instance, implement minimum length of varactor may achieve the lowest phase noise, but it decreases the tuning range due to

the intrinsic capacitor. Therefore, finding a proper balanced point of tuning range and phase noise is an significant index for high frequency VCO design. Switched varactor is mentioned for increasing the tuning range of VCO design [10]. In CMOS process, NMOS is usually used as RF switch. The switching capacitance composed of RF switches and MIM capacitors is a part of the resonator and its performance will affect the performance of the entire VCO. Firstly, the Q-factor of the switching capacitance will affect the Q -factor of the resonator; secondly, the ratio of the maximum capacitance to the minimum capacitance of the switching array will affect the tuning range of the VCO.

1.2 Thesis organization

The aim of the paper is exploring the limit and performance of III-V nanowire VCO at 100GHz operating frequency. The large and linear tuning range achieved by choosing reasonable dimensions of varactor and transistors. This article is organized as follows: chapter two illustrates the basic information of III-V nanowire n-type(InAs) trasistor. Chapter three illustrates the VCO design philosophy and calculation analysis. Chapter four illustrates the method of simulation in ADS in this paper. Chapter five describes the implementation and measurement results. Finally, the conclusion and future work is summarized in chapter six and chapter seven.

YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14T2	P32M14T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
IDM-Foundry node labeling	i10-i7	i7-i5	i5-i3	i3-i2.1	i2.1-i1.5	i1.5-i1.0	i1.0-I0.7
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA 3DVLSI	VGAA, LGAA 3DVLSI
Logic device mainstream device	finFET	finFET	LGAA	LGAA	LGAA	VGAA	VGAA
DEVICE STRUCTURES							
LOGIC DEVICE GROUND RULES							
MPU/SoC Metal1 ½ Pitch (nm)[1,2]	18.0	14.0	12.0	10.5	7.0	7.0	7.0
MPU/SoC Metal0/1 ½ Pitch (nm)	18.0	14.0	12.0	10.5	7.0	7.0	7.0
Contacted poly half pitch (nm)	27.0	24.0	21.0	18.0	16.0	16.0	16.0
L_g - Physical Gate Length for HP Logic (nm) [3]	20	18	16	14	12	12	12
L_g - Physical Gate Length for LP Logic (nm)	22	20	18	16	14	14	14
Channel overlap ratio - two-sided	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Spacer width (nm)	8	7	6	5	5	5	5
Contact CD (nm) - finFET, LGAA	18	16	14	12	10		
Contact CD (nm) - VGAA						12	12
Device architecture key ground rules							
FinFET Fin Half-pitch (nm)	16.0	14.0					
FinFET Fin Width (nm)	8.0	7.0					
FinFET Fin Height (nm)	45	50					
Footprint drive efficiency - finFET	3.06	3.82					
Lateral GAA lateral half-pitch (nm)			12.0	10.5	9.0		
Lateral GAA vertical half-pitch (nm)			8.0	8.0	8.0		
Lateral GAA (nanosheet) thickness (nm)			5.0	5.0	5.0		
Lateral GAA (nanosheet) minimum width (nm)			7.0	7.0	6.0		
Number of vertically stacked nanosheets			3	4	5		
Device height (nm)			47	63	79		
Footprint drive efficiency - lateral GAA			3.00	4.57	6.11		
Vertical GAA lateral half-pitch (nm)						7.0	7.0
Vertical GAA width (nm)						6.0	6.0
Contact-gate enclosure (nm)						2.0	2.0
Footprint drive efficiency - vertical GAA						1.7	1.7
Defice effective width (nm)	98.0	107.0	72.0	96.0	110.0	24.0	24.0
Device lateral half-pitch (nm)	16.0	14.0	12.0	10.5	9.0	7.0	7.0
Device height (nm)	45.0	50.0	47.0	63.0	79.0	24.0	24.0
Minimum device width (fin, nanosheet) or diameter (nm)	8.0	7.0	7.0	7.0	6.0	6.0	6.0

Fig 1: Device Architecture and Ground Rules

Roadmap for Logic Device Technologies[1]

CHAPTER 2

2.1 III-V nanowire transistor

The semiconductor era began in 1960 with the invention of integrated circuits. In integrated circuits, all active/passive components and their interconnections are integrated on a single silicon wafer, giving them a leading edge in portability, functionality, power consumption and performance. Over the past few decades, the semiconductor industry has grown rapidly under Moore's law. Moore's law is that the number of transistors on a chip roughly doubles every two years. For decades, the industry silicon-based CMOS devices is shrinking the key size, improving the level of integration in order to achieve lower power consumption, faster and cheaper integrated circuit chips. The early development of CMOS is relatively simple, only need to improve the machining accuracy, according to the geometric principle simple device horizontal and vertical size. But after entering the 21st century, in order to extend Moore's Law, new structure and material have been implemented into the industry, such as the start of the 90 nm node with strain Silicon (Strained Silicon) technology, from 45 nm node using high K gate media and metal gate technology, from 22 nm technology node, Fin type transistor structure (FinFET) came into use.[2][3]

According to the ITRS, the nanowire-based transistor will gradually replacing the role of silicon-based transistor.[1] Nanowire is only 6-8 nm in diameter, which means channel is easier controlled by gate as known as short channel effect. Therefore, under the same gate capacitance, nanowire transistors have more potentials on size reduction than traditional silicon-based transistor [3].

In this paper, the MOSFET based on nanowire is achieved

at Lund University and described by Verilog-A. This model is packaged into the Nanoelectronics Student Component Library(NSCL) and is identified design environment for ADS, which is developed by the Nanoelectronic Group at Lund university. Nanowires are made of high mobility III-V semiconductors, indium arsenide (InAs) allows electrons to travel faster and more current than silicon. This device type has the potential to replace or supplement the silicon based MOSFET in digital and analog applications.[4]

2.2 Small-signal analysis of III-V nanowire transistor

The transistor model used for analysis is scaled in 60 nanowire width, 3 fingers and 20 nm for length. In order to extract the necessary data of nanowire transistor, different simulation has been established in Keysight ADS. The transistor is a very non-linear element, but if the operating window is small enough, which means that the transistor bias at some fixed DC voltage with superimposed time-varying signal amplitudes are very small and can be described with linear circuit elements such as resistors, capacitors and so on. In real life, III-V nanowire transistor is very complicated as shown in Fig 2. Different parasitic resistors and capacitors are located at drain, source and gate node. The parasitic resistor and capacitor are the main elements that limiting the performance of the nanowire transistor. Parasitic resistance of active transistor has limitation to the effective voltage on the operating device and parasitic capacitor will limit the performance of the varactor that based on nanowire transistor configuration.

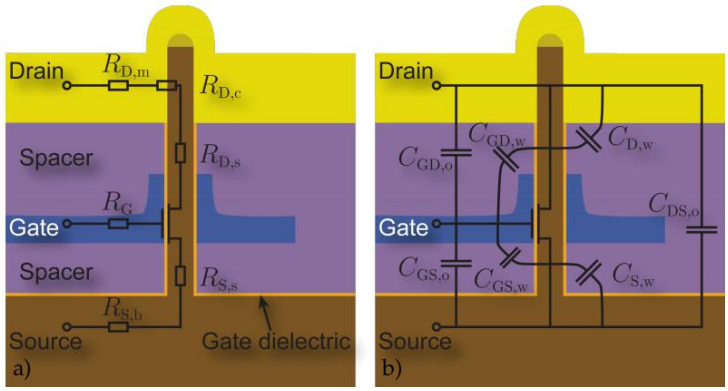

Fig 2: Schematic images of a vertical nanowire MOSFET[11]

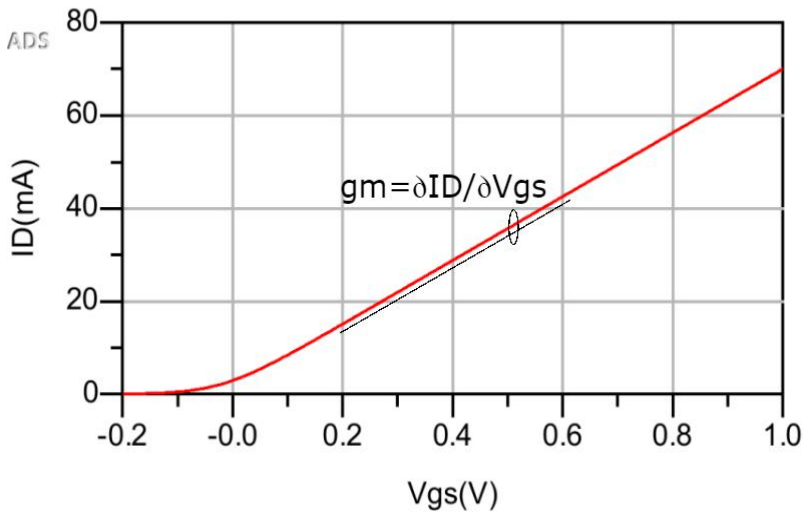

Fig 3: Simulated ID & Vgs characteristic

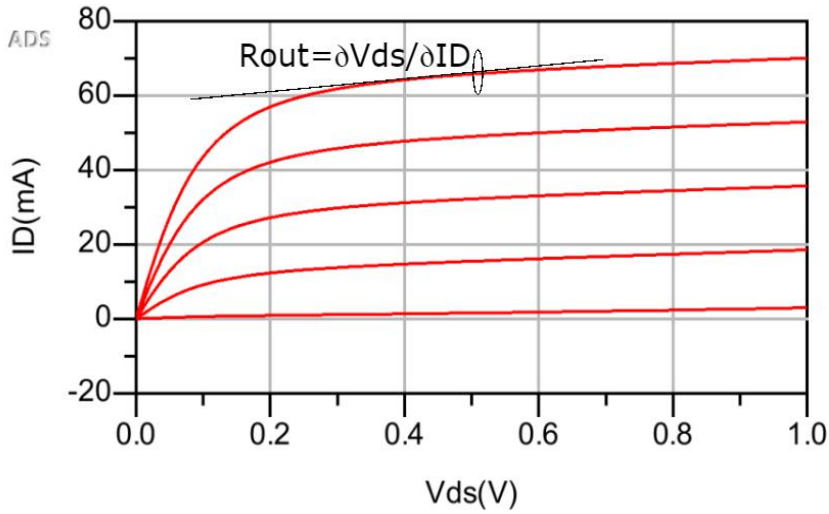

Fig 4: Simulated ID & Vds characteristic

In order to make the analysis of transistor easily and understandable, the only necessary elements of transistor are described in this paper. Transconductance(g_m) is an important metric of transistor, the mathematical expression of gm is expressed by,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{i_d}{v_{gs}}|_{V_{GS},V_{DS}} \quad (1)$$

By this definition, transconductance is the ratio of the change in the output current to the change in the input voltage. High transconductance is advantageous in RF circuits because it allows high low-frequency gain. Simulated Ids/Vgs characteristic is shown in Fig 3 and the slope rate of the curve is g_m of the transistor, which is around 12mS approximately. Furthermore, the sloped rate of a selected curve in Fig 4 can be used for calculating the intrinsic resistor, the the mathematical expression of g_m is expressed by

$$R_{out} = \frac{\partial V_{DS}}{\partial I_D} = \frac{v_{ds}}{i_d}|_{V_{GS},V_{DS}} \quad (2)$$

By this definition, intrinsic resistor is the ratio of the

change in the drain-source voltage(V_{ds}) to the change in the drain-source current(I_{ds}), which is roughly between 200Ω and 220Ω.

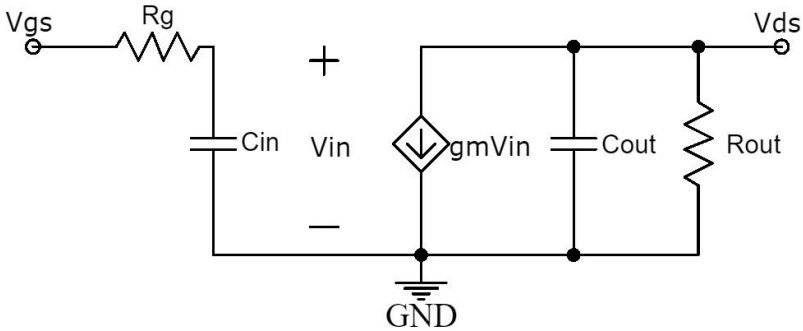

Fig 5: A small signal model of NW-Transistor based on linear circuit element

The detailed analysis of nanowire transistor is not mentioned in this paper due to the limitation of the thesis and in order to make the analysis of III-V nanowire understandable, a simplified small signal model is built and shown in Fig 5. The small signal model contained a gate resistance R_g , an input capacitor C_{in} , output capacitor C_{out} and intrinsic resistor Rout. The sum of the C_{in} and C_{out} is regraded as the total parasitic capacitor of the nanowire transistoor. At high frequencies, gate resistance R_g will affect performance of the transistor.[12]

The parasitic capacitance is a key element of VCO design since it has a huge effect on the tuning range of VCO as well as the Q-factor of the resonator. A good tuning range can be achieved by minimizing the parasitic capacitance that connected to LC tank.From the Fig 6, the left smith chart illustrates the equation that can be used for input capacitor and resistance, which is

$$Z_{in} = r_{in} + \frac{1}{jwC_{in}} \tag{3}$$

The input impedance is expressed by below at 100GHz

$$Z(1,1) = Z_0 * (0.413 - j5.916) = 20.65 - 295.8j$$

Note that Z0 adopts 50 Ω for the load resistance. The input capacitor C_{in} and resistor R_g as shown in Fig 6 can be calculated from Z(1,1), which is 20.65Ω and 42.9fF. The smith chart in the right hand of Fig 6 illustrates the the equation that can be used for output capacitor and resistance, which is

$$\frac{1}{Z_{out}} = \frac{1}{r_{out}} + jwC_{out} \tag{4}$$

The output impedance is expressed by below at 100GHz

$$Z(2,2) = Z_0 * (4.139 - j5.782) = 206.95 - 289.1j \tag{5}$$

The output capacitor C_{out} and resistor R_{out} is shown in Fig 6, the calculation result from Z(2,2) is 610 Ω and 23 fF.

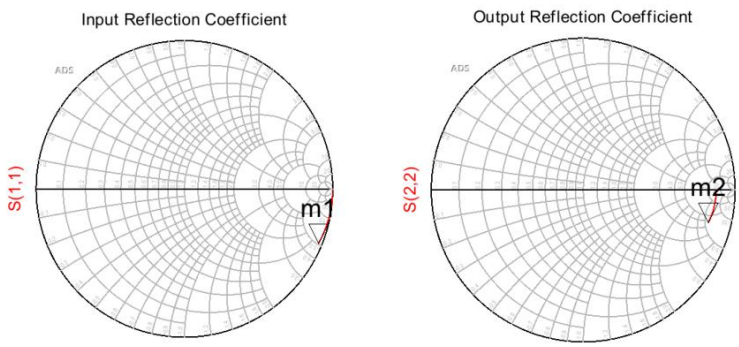

Fig 6: Input&output capacitor and resistance simulation

Chapter 3

Voltage controlled oscillators can be divided into resonator-based oscillators and waveform based oscillators. The oscillator based on resonator is divided into LC oscillator and crystal oscillator. LC oscillator can be divided into cross-coupled VCO and colpitts VCO. Compared to colpitts VCO, cross-coupled topology can provide higher operating frequency and better stability. There are three commonly used cross-coupled VCO structures: single NMOS, single PMOS, NMOS and PMOS current multiplexing. Current multiplexing structures are rarely used under most of current technology since limited by thresholds and output amplitudes. [12]

3.1 Small-signal analysis of VCO

The VCO in this paper employs the NMOS cross-coupled topology similar to [2] for this paper and is shown in Fig 7. It consists of a resonate tank and cross-coupled pair with a NMOS current tail connected to the ground. The small-signal model analysis of VCO is illustrated in this paper. In the LC voltage-controlled oscillator, the concept of negative resistance is usually used to analyze the oscillate condition. A parallel circuit consisting of an ideal inductor L and varactor C resonates at frequency f_0 =100 GHz. Inductor and varactor consist the LC-tank of the VCO, RL and RC are parasitic resistors of inductor and varactor . In order to compensate for the loss of parasitic resistance and capacitance in the resonator, negative resistance -R is formed in the circuit. In real life the negative resistor -R is form into cross-coupled pair. By cross connecting the output to the oscillator, the same negative resistance as the transistor transconductance

(g_m) is produced. [12] If a negative resistance equal to the parasitic resistance is connected in parallel in a resonator, the oscillating circuit will oscillate continuously. The output is generated at the both side of the cross-coupled pair,the differential output is defined in Vd and expressed by

$$v_d = v_p - v_m \tag{6}$$

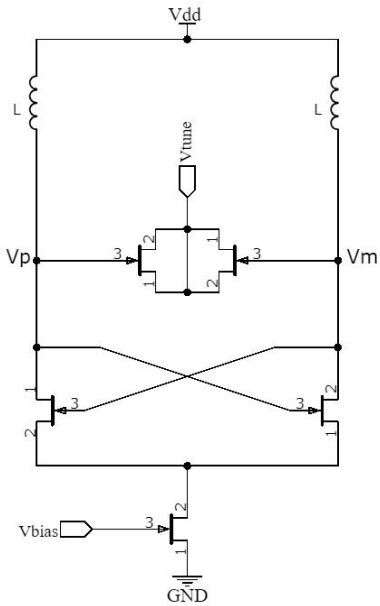

Fig 7: The cross-coupled VCO in this paper

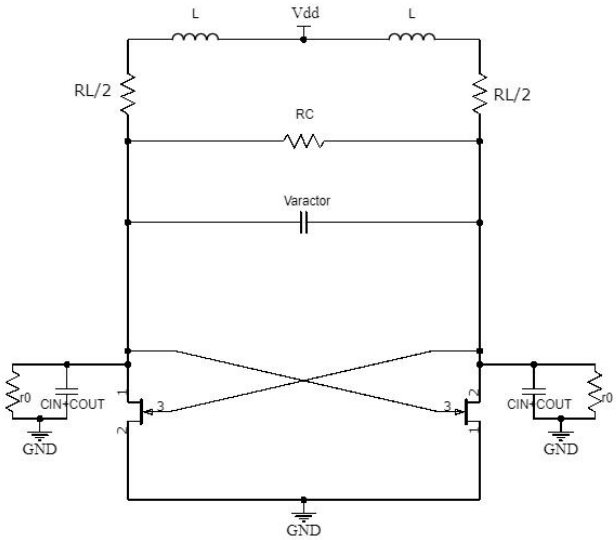

Fig 8: Equivalent capacitor model of VCO core

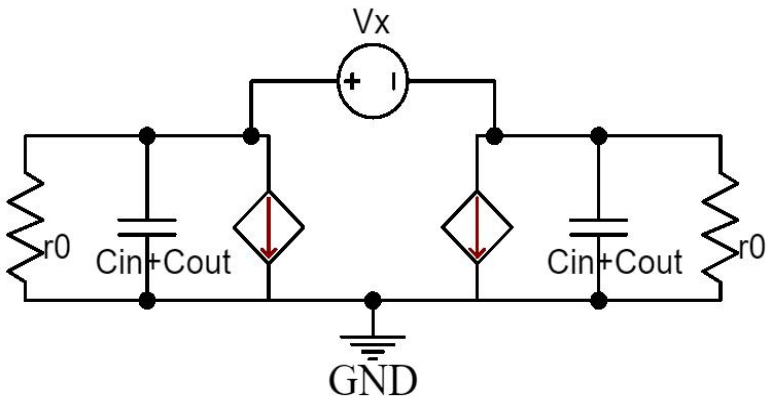

Fig 9: Small signal model of VCO core

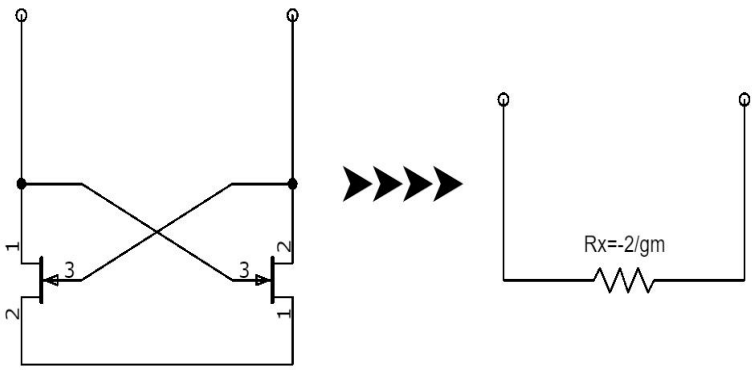

Fig 10: The cross-coupled pair modeled as a negative resistance

According to the small signal model in Fig 9, it is easily get the total impedance of the input, which is

$$Z_0 = r_0 \parallel jwC_0 \tag{7}$$

$$C_0 = C_{in} + C_{out} \tag{8}$$

the effective transistor capacitance at the drain node is actually (Cin+Cout) as shown in Fig 8. If a voltage source Vx applied to the small-signal model then the input impedance can be expressed as

$$Y_x = \frac{I_x}{V_x} = -\frac{g_m}{2}(1 - \frac{1}{g_m r_0}) + \frac{1}{2} jwC_0 \tag{9}$$

So approximately the input impedance can be simplified called Rx as shown in Fig 10, if the cross-coupled pair using the same dimensions,

$$Z_x = \frac{1}{Y_x} \rightarrow R_x = -\frac{2}{g_m} \tag{10}$$

Generally, the condition for determining whether the NMOS VCO oscillate is when the active device is sufficient to compensate for the loss of resistor in LC-tank, a resistor called R_P is adopted in Fig 8, which is the total impedance of the parallel resonator($R_L // R_C$), which is consisted of the impedance of inductor and varactor and that can be simulated by S-parameter analysis in Keysight ADS, gm is the trans-conductance of a nanowire transistor when the loop is opened. Above all the discussion, the general oscillation condition of cross-coupled VCO is expressed by below,

$$(R_p - \frac{2}{g_m}) < 0 \tag{11}$$

3.2 FoM calculation

In recent years, more and more attention has been paid to the performance of VCO since they act an important role of circuit design and radar technology. The performance of VCO is difficult to evaluate since it differs in different aspects, such as tuning range, phase noise , center frequency and power consumption. As a benchmark for comparing VCO performance, FoM (Figure of merit) is widely used in documents.[13]

Usually, the FoM of VCO performance is defined as [14]

$$FoM = L(f_{offset}) - 20\log(\frac{f_0}{f_{offset}}) + 10\log(\frac{P_{DC}}{1mW}) \tag{12}$$

$L(f_{offset})$ is the phase noise in dBc/Hz at offset frequency from the carrier frequency f_0 . P_{DC} is the DC power dissipation in mW. Moreover, the phase noise is defined as the ratio of noise power to signal power in a 1Hz bandwidth,

which is given for a LC oscillator by[8]

$$L(f_{offset}) = 10\log[\frac{2FkT}{P_{sig}}\frac{f_0^2}{4Q^2 f_{offset}^2}] \quad (13)$$

where k is Boltzmann constant, T is the absolute temperature, P_{sig} is the output power, F is device excess noise factor and Q is the quality factor of the resonator. However, this FoM has not physically considered the degradation of the frequency tuning range (FTR) and associated it with circuit parameters. In this paper, a new FoM calculation has been implemented which takes FTR of VCO into account and associates it with circuit parameters.[7] The new FoM is defined as " FoM_L ", whose definition is to consider the degradation amount in the quality factor as follows

$$FoM_L = FoM(f_{center}) - 20\log(1+\frac{FTR}{2}) \quad (14)$$

$$FoM(f_{center}) = L(f_{center}) - 20\log(\frac{f_{center}}{f_{offset}}) + 10\log(\frac{P_{DC}}{1mW}) \quad (15)$$

From above, FTR can be expressed as (fmax+ fmin)/ fcenter. Therefore, when FTR increases, fmin needs to be reduced, thus reducing the average quality factor, resulting in a decrease in VCO performance. Therefore, degradation of the inductance quality factor must be considered when FTR is considered. Alternatively, FoM_T is used to include FTR into the conventional FoM given by [9]:

$$FoM_T = FoM_{peak} - 20\log(\frac{FTR}{0.1}) \quad (16)$$

As seen from equations above, FoM can be improved by increasing tuning range, reducing power consumption and reducing phase noise. When the absolute value of FoM is larger or the negative value is smaller, the performance of

VCO is better.

3.3 LC-Tank Design

In general, at frequencies lower than 10 GHz, the Q-factor of LC-tank is limited by the inductor. But at millimeter-wave frequencies, the Q-factor will not depend on the inductor any more. Since the Q-factor of varactor decreases with frequency, while that of inductor increases with frequency, so the tank is limited by the Q of varactor at millimeter-wave frequencies. The main problem in designing high performance LC-VCO is to design resonant tank with high quality factor. The quality factor of the resonator can be expressed as[13]

$$Q_{\tan k} = \frac{Q_C Q_L}{Q_C + Q_L} \tag{17}$$

Where, Q_C is the quality factor of varactor and Q_L is the quality factor of inductor. The Q_C value of varactor is much higher than the Q_L value of inductor, so the Qtank value of resonator is slightly lower than the Q_L value of inductor. Improving the Q_L value of inductor can obviously improve the phase noise performance of VCO.

3.3.1 Inductor

The inductor model is built and shown in Fig 11, the model includes an inductor, a parasitic resistor(R_L) and capacitor(C_L), which is 1 Ohm and 10 fF. In order to calculate the Q-factor of inductor at a reasonable number, the equation can be approximately expressed by,

$$Q_L = \frac{\omega L}{R_L} \tag{18}$$

ω is angular operating frequency, L is inductance and R_L is equivalent resistance. The Q-factor of the inductor is the ratio of the stored power of the inductor to the loss power consumption. The higher the Q-factor, the lower loss of the inductor, which is directly related to the resistance lost of the inductor. Fig 12 shows the variation of the Q-factor of inductor with frequency. At a frequency of 100 GHz, the quality factor of inductor is 16.6 and the inductance is 30 pH.

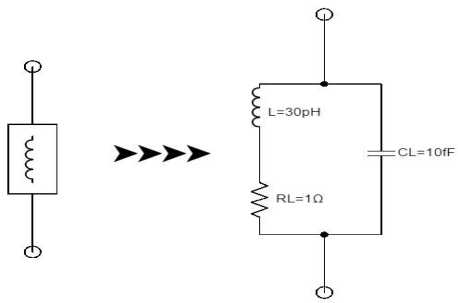

Fig 11: Equivalent inductor model with parasitic resistance and capacitor

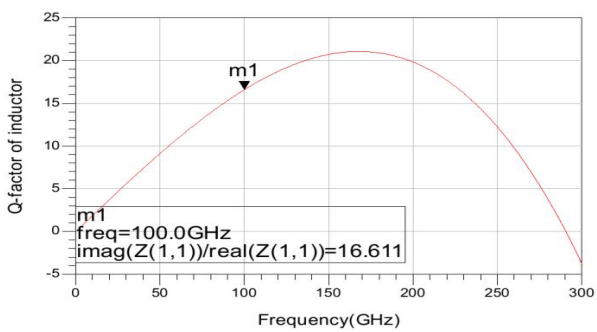

Fig 12: Simulated Q-factor versus frequency of inductor

3.3.2 Varactor

The most common method of varactor design is to use MOSFET-based structure, as shown in Fig 7, two nanowire transistors are placed reversely with the drain and source connected to each other. The varactor is usually in an accumulation region, which means that the surrounding well is doped in the same way as the transistor. But nanowire transistor does not have well, so this is a big difference with silicon based transistor.

In this paper, the varactor is consist of III-V nanowire transistor and the number of nanowire and length can be used for adjusting the Q-factor of resonator. In order to achieve minimum phase noise in LC-VCO, the quality factor (Q) of the resonator must be as high as possible. For the varactor in VCO design, the minimum gate length is not used. Since with the increase of the length, the parasitic capacitor will also increase. The tuning range is related to the parasitic capacitor. Therefore, the length of varactor should be as long as possible but still can be fabricated in reality. The oscillation frequency (f_0) of the VCO is given by below and was designed to be 100 GHz,

$$f_0 = \frac{1}{2\pi\sqrt{LC_{\text{var}}}} \tag{19}$$

C_{var} is varactor capacitance and with the tuning voltage differed, the value of C_{var} will also changed with the tuning voltage. That is the basic theory of voltage-controlled oscillator.

This paper describes three ways for changing the capacitance of varactor: width, length and fingers. The ratio of Cmax over Cmin, which is Cmax/Cmin, is usually a benchmark for evaluating the performance of varactor. The larger Cmax/Cmin, the better performance of VCO. In order

to explore the best performance of the varactor, the width is swept from 10 um to 100 um, length is swept from 20 nm to 100 nm and finger is swept from 1 to 15. Different simulation results have been compared in this paper. Fig 13, Fig 14(a) and (b) illustrates the C/V characteristic, Cmax/Cmin ratio and Q-factor of LC-tank when the length of varactor is a variable value and they are shown below.

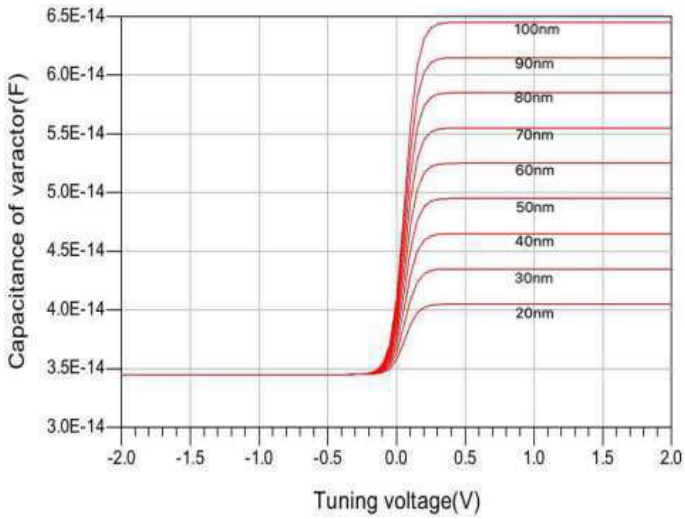

Fig 13: C–V characteristics of the nanowire varactor with different lengths at 30 um width and 15 fingers

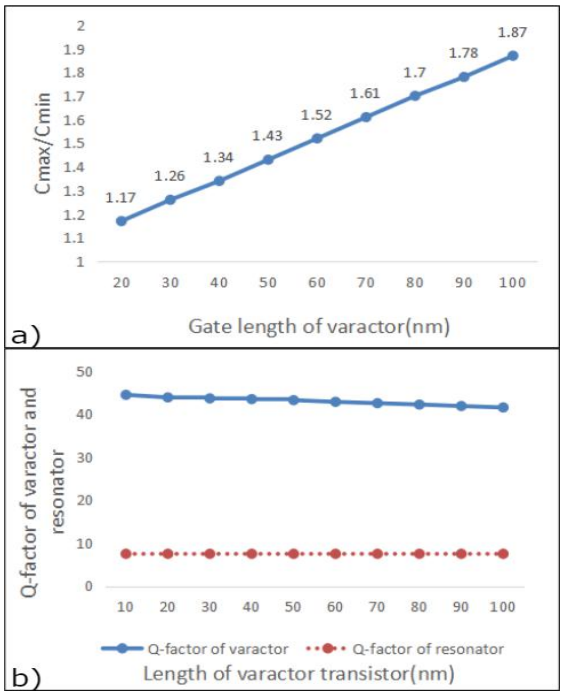

Fig 14(a): Cmax/Cmin ratio as a function measured at 100GHz with varying length at 30 um width and 15 fingers; (b): The relationship between Q-factor and length in varactor at 30 um width and 15 fingers

In order to test these trade-off experimentally in iii-v nanowire based VCO for operating at 100GHz, different gate lengths vary from 10 nm to 20 nm are simulated. Fig 13 shows the varying length from 20 nm to 100 nm and Cmax changed from 41.15 fF to 64.15 fF, which means Cmax/Cmin ratio varying from 1.17 to 1.87 as shown in Fig 14(a). Fig 14(b) shows the measured Q-factor for

varactor and resonator with varying gate lengths. For this varactor, the tuning range is limited at Cmax/Cmin=1.52. In the VCO design, the tuning range is the most important index that needs to explored. In addition, the most effective way improving the tuning range is making varactor larger. There are two methods to change the size of varactor: adjusting widths or lengths. Fig 15(a) and (b) Cmax/Cmin ratio and Q-factor of LC-tank when the width of varactor is a variable value and they are shown below.

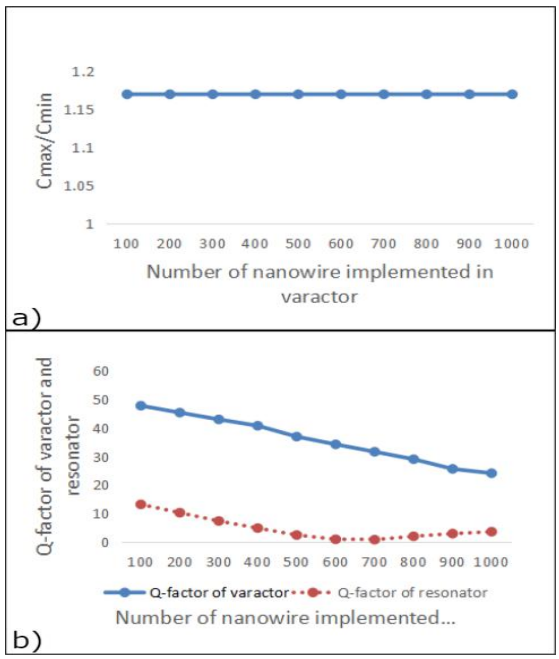

Fig 15(a): Cmax/Cmin ratio as a function measured at 100GHz with varying width at 60 nm length and 15 fingers; (b): The relationship between Q-factor and width in varactorv at 60 nm length and 15 fingers

Fig 15(b) shows the the measured Q-factor for varactor and resonator with varying widths of iii-v nanowire transistor. Note that increase the size of varactor will decrease the Q-factor of varactor, but the length does not have large influence of the Q-factor of resonator even if the Q-factor of varactor changed. The Q-factor of varactor decreased with the increase of the gate length and width as well as tuning ratio increases. It is obvious that different widths do not expand the Cmax/Cmin ratio, which means that width does not have influence of tuning range. Instead, as shown in Fig 14(a), length has an significant effect on Cmax/Cmin ratio. From Fig 15(a), even if the Cmax changed with varying widths, but also the Cmin increased. Since width increasing, the minimum parasitic capacitor will also increase at the same time, that is why the Cmax/Cmin ratio keeps constant at 1.17 in Fig 15(a).

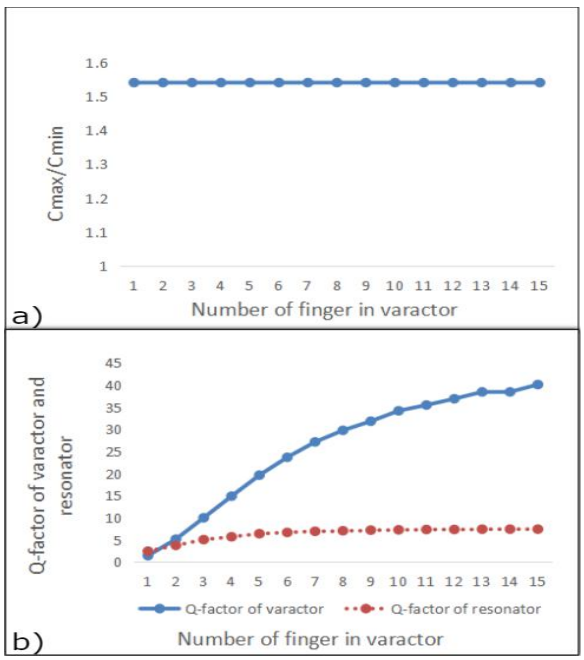

Fig 16(a): Cmax/Cmin ratio as a function

measured at 100GHz with varying width at 60 nm

length and 30 um width; (b): The relationship between Q-factor and finger in varactor at 60 nm length and 30 um width

According to the structure of III-V nanowire transistor, the number of nanowire that located in the finger of NW-transistor presents the different dimensions. For varactor transistors, the number of nanowire is arranged by 300, which means the width of varactor transistor is roughly around 30 um. According to the documents [10] [11] [12], each finger of NW-transistor has 20-30 nanowire that is a best choice for device implement. In addition, the number of finger in the varactor has an infect on the Q-factor of varactor. It is obvious that when the finger reaches 15, which means 20 nanowire per finger of nanowire transistor, the Q-factor of varactor has largest value which is 41.15. Note that the number of finger in varactor does not have influence on Cmax/Cmin since the number of finger does not have any relationship with parasitic capacitor in nanowire transistor as shown in Fig 16(a). As shown in Fig 16(b), with 300 nanowire and length 60 nm, the finger varying from 1 to 15, the Q-factor of varactor increased a lot and Q-factor of resonator kept constant when the finger reaches 10. This proves that the number of nanowire should implemented between 20 to 30 per finger in order to behave the stable performance of NW-transistor.

Depending on the VCO operating frequency, phase noise, power consumption and tuning range all these requirements, such a diagram can be used to select the appropriate varactor structure. In III-V nanowire processes, varactor gate length between 40 nm and 100 nm and number of finger between 10 and 15 has a good tuning range and Q-factor and this paper adopts a varactor with 300 nanowire for the width, 60 nm for the length and with15 fingers.

Chaptor 4

Method of ADS simulation

Keysight ADS is a complex circuit simulator and it takes a lot of time to learn a variety of complex functions. ADS can be performed on a variety of operating systems. The thesis adopts ADS 2019 version and runs on Linux system. ADS mainly focuses on RF and microwave design, so most devices in the library are RF and microwave components. However, There are some design libraries for low frequency effect transistors and BJTs. [15] ADS can perform several different simulations and the simulations that this paper has been used are illustrated in this chapter. Note that the design library , which is Nano-electronic Student Component Library, is provided by Nano-electronic Group of Lund University in Sweden.

4.1 S-Parameter

This analysis method is widely used in engineering and microwave circuit design. In this paper, this analysis is mainly using for calculate the Q-factor of inductor, varactor and resonator at 100 GHz frequency. In additional, S-Parameter analysis can also be used for transistor analysis, for instance, when the frequency is swept from 1GHz to 100 GHz, the I-V characteristic, the maximum gain and C-V characteristic can be simulated.

4.2 Transient Analysis

Transient analysis can predict circuit performance in time domain. For the VCO analysis, it is important set initial condition before the simulation, otherwise the simulation will give the wrong information. The value of initial condition

should be set infinitely close to the supply voltage, for instance, the value is set to 0.999 V since the supply voltage is 1 V in this work. Note that this simulation can take a lot of time and generate a lot of data.

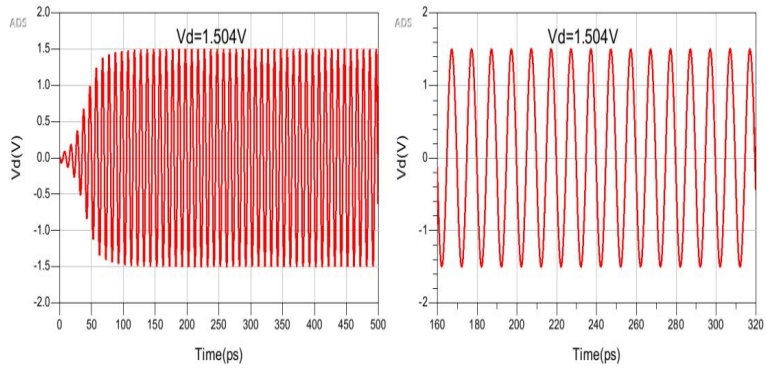

Fig 17: Simulated oscillator transient analysis waveform

Transient analysis is an effective method to check the working state of VCO by evaluating the relationship between output voltage and time, for instance, it is easily calculate the operating frequency from the output waveform. Fig 17 shows the transient analysis of the sinusoidal waveform and the steady-state waveform. The response time of the oscillator is about after 100 ps getting stable oscillation and the transient analysis shows that the peak oscillation voltage is 1.610 V.

4.3 Harmonic balance(HB)

Because the VCO operates at high frequency, harmonic balance is mainly for checking the distortion in the nonlinear system. In the HB simulator, the number of order is set to 12 in order to make the simulation result precise and For the phase noise analysis, a controller called " Noise Cons " must be implemented. This controller allows the simulation of phase noise based on varying temperature, carrier frequency and offset frequency. Note that a device called " OscPort '' is used

for noise simulation [16], but it is not practical for cross-coupled VCO when simulating the phase noise since there is no negative or positive feedback in it. Furthermore, the tuning characteristic can also be achieved by HB simulation.

In Fig 18, simulation shows that the secind harmonic index of the VCO is 14 dBm. Harmonic suppression output at -18.568 dBm. There is about 33 dBm difference between second harmonic index and fourth harmonic index. The additional higher frequency modes of the seventh and eighth harmonic index are -31.225 dBm and -37.956 dBm, respectively.

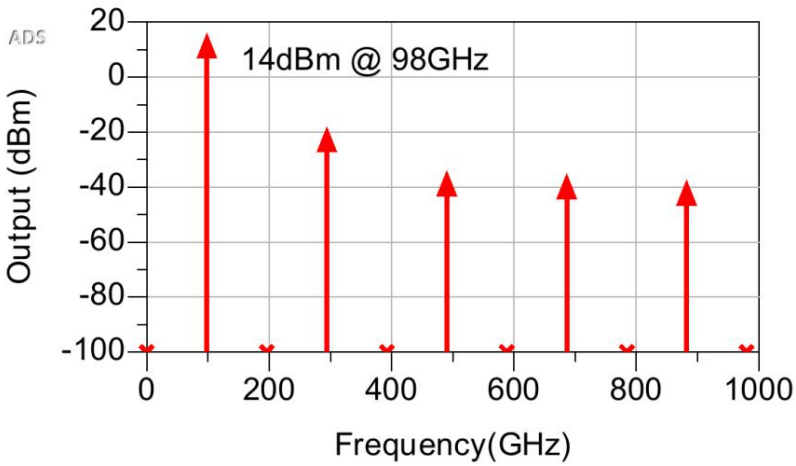

Fig 18: Simulated harmonic index distribution

CHAPTER 5

Experiment Result

As the maximum frequency of NMOS transistors in III-V nanowire technology is higher than 600 GHz, VCO operating near 100 GHz can be realized. By applying the low parasitic and low loss design method discussed in chapter two, VCO operating between 95-105 GHz is realized. The schematic of VCO for testing is shown in Fig 19.

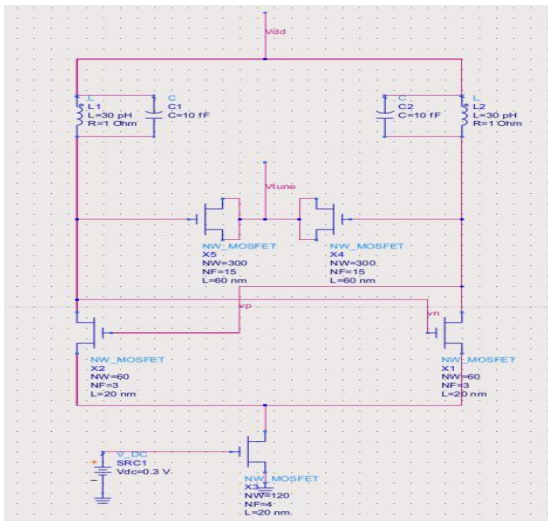

Fig 19: Schematic of VCO core for testing

5.1 Tuning range and phase noise analysis

To explore the frequency limitations of this process, transistor dimensions ranging from 8 um(80 nanowire for width) to 6 um(60 nanowire for width) are used to vary the central frequency of the VCO. For cross-coupled transistors, the number of nanowire is changed from 80 to 60, which means the width of varactor transistor is roughly varied from 8 um to 6 um and the number of fingers is changed from 4 to

1. The maximum measured oscillation frequencies of VCO with a core transistor width of 80, 70 and 60 number of nanowire are 95.8, 99.2, and 106.2GHz, respectively. The values of the varactor and inductor are fixed. For the varactors, the minimum gate length is not implemented. Instead, a varactor that is 30 um x 60 nm with a large tuning ratio (Cmax/Cmin=1.87) is implemented in this paper.

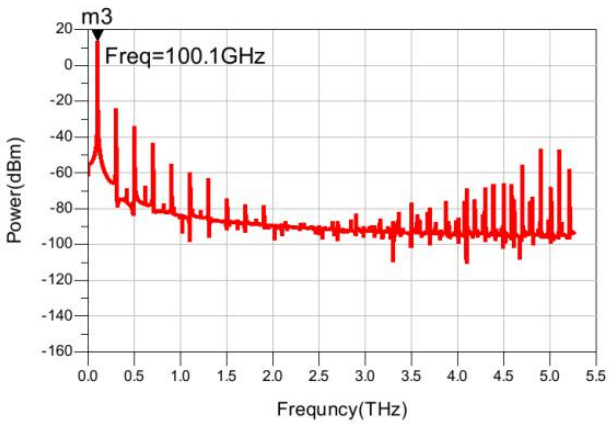

Fig 20: Measured Output spectrum of 100GHz VCO

The 100GHz VCO adopted 6 um wide cross-coupled transistors and began to oscillate at a bias current and supply voltage of 15.6 mA and 1.0 V. Furthermore, for more stable oscillations and larger output power, measurements were made at a higher bias current of 20.2 mA and larger supply voltage at 1.2 V. The measured output spectrum is shown in Fig 20. The measured phase noise is about -112 dBc/Hz at 10-MHz offset from the carrier as shown in Fig 21. Since the transistor capacitance is the main contributor to the LC-tank capacitance and also the transistor capacitance depends on the bias conditions, the tuning range can be increased by adjusting the transistor capacitance. In fact, some authors suggest increasing the tuning range by changing the power supply voltage.[17][18]

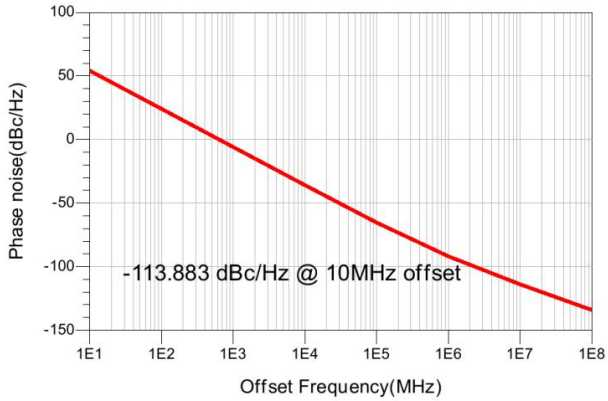

Fig 21: Measured Phase noise of 100GHz VCO

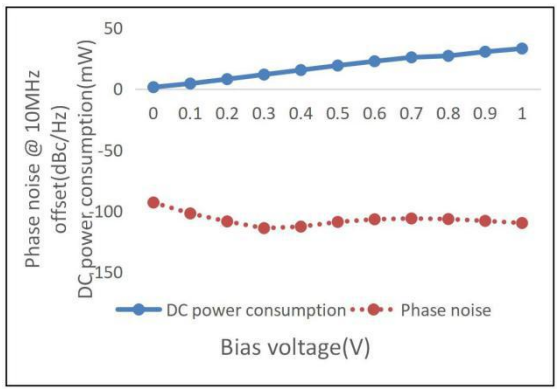

Fig 22: Measured power dissipation and phase noise with different Vbias

However, changing the supply voltage is not practical since this will infect the phase noise of the overall circuit. Fig 22 illustrates the distribution of phase noise and power dissipation with bias voltage varying from 0 to 1 V. As seen from Fig 22, the phase noise reaches -113.883 dBc/hz at 10 MHz offset from carrier under 0.3 V bias voltage, this is the lowest phase noise achieved by this work. The DC power consumption increased from 1.58 mW to 33.2 mW with the bias voltage varying from 0 to 1 V. Note that the length of varactor does not have effect on phase noise since it does not

have influence on the Q-factor of resonator. By adjusting the varactor's bias voltage, the VCO's oscillation frequency is tuned.The phase noise is an important design index of VCO. Minimizing phase noise is the key factor to realize the maximum potential of any communication system. By limiting the current range, the variation of the output power and phase noise in the tuning range can be limited. In this implementation, Vbias is used for fine tuning and varactors for coarse tuning.

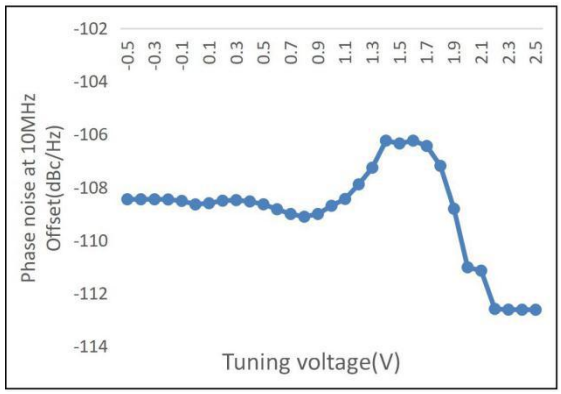

Fig 23: Measured Phase noise with varying tuning range

Varactor tends to be strongly accumulated or depleted, where it causes a smaller VCO gain and this helps to keep the phase noise low as shown in Fig 23. By adjusting the varactor's bias voltage, the VCO's oscillation frequency is tuned.The phase noise is an important design index of VCO. Minimizing phase noise is the key factor to realize the maximum potential of any millimeter-wave platform. Fig 23 illustrates the phase noise distribution with tuning voltage from -0.5 V to 2.5 V. The best phase noise range is achieved when tuning voltage varying from 2 V to 2.5 V. For the whole tuning range 10.77 GHz when Vbias at 0.3 V and supply voltage at 1V, the phase noise varying from -106.457 dBc/Hz to -113.883 dBc/Hz at 10MHz offset from carrier.

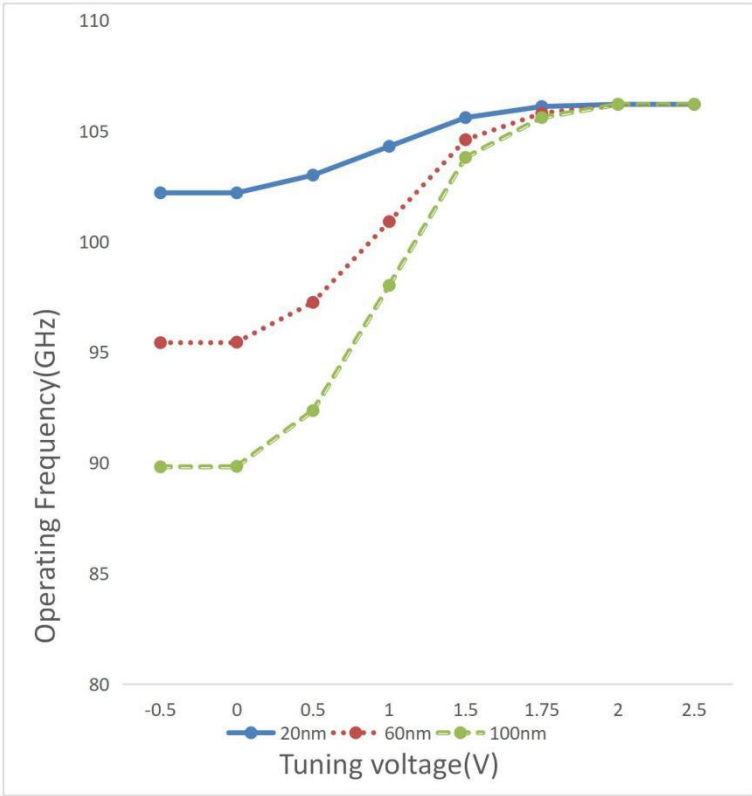

Fig 24: Measured tuning range with varactor length at 20 nm, 60 nm and 100 nm

Fig 24 shows the tuning characteristics of VCO with length at 20 nm, 60 nm and 100 nm. For 20 nm length implemented for varactor, the output frequency can vary from 102.2 GHz to 106.2 GHz. In the same word, by implementing the 60 nm and 100 nm for the length of varactor, the tuning range is 95.89 GHz ~ 106.2 GHz and 89.84 GHz ~ 106.2 GHz. The center frequency is varying from 104.2 GHz to 98.02 GHz.

5.2 Figure-of-merit(FoM) analysis

In chapter three, the definition of the Figure-of-merit(FoM) takes into account the change of Q-factor caused by FTR. FoM and FoMcenter were compared and there was a difference between them. In this chapter, FoM is firstly analyzed theoretically and then each difference is simulated. Since the average Q-factor decreased with the increase of FTR, a good FoM should be kept relatively constant with the increase of FTR. Since the device excess noise factor F that mentioned in chapter three is unknown for iii-v nanowire transistor, so FoM_T is not included in this paper. When the ideal capacitance is used in the simulation, FTR changes with the change of capacitance value. According to the formula of FoM, the DC power consumption has an influence on FoMcenter. The bias voltage varying from 0 to 1 V and length of varactor varying from 20 nm to 100 nm has been simulated to check the changing direction of FoM.

Fig 25(a) and (b) illustrates the FTR and FoM change with different lengths of varactor. According to the definition of FoM in chapter three, there are two mainly elements of VCO that have impact on it: FTR and Power consumption(P_{DC}). From Fig 25(b), the value of FoM is not influenced by the changing of length in varactor, since length is not one of the factor that has impact on phase noise. The FoM kept constant around -181 dBc/Hz and the value of them shows similar result. FTR is changed by the length of varactor where were used in simulation.It can be seen from the Fig 25(b) that the wider the FTR, the worse FoM.

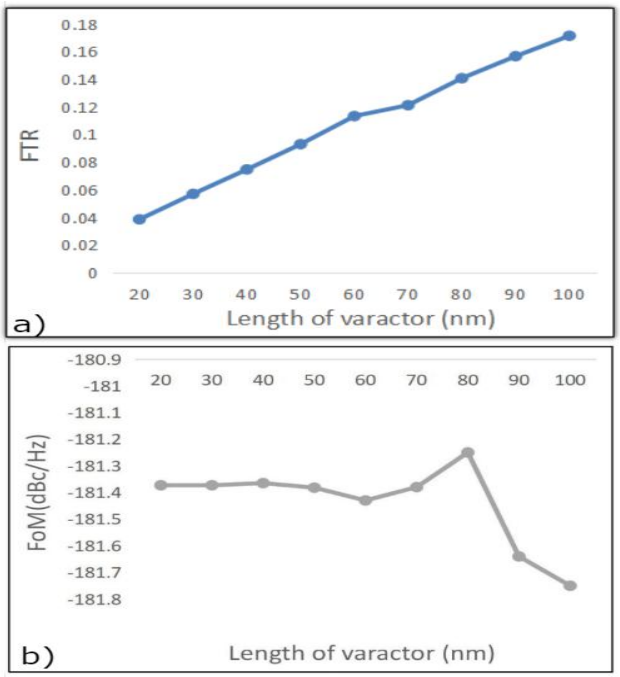

Fig 25(a): Measured FTR with length of varactor varying from 20 to 100 nm; Fig 25(b) Measured FoM with length of varactor varying from 20 nm to 100 nm

From Fig 26(a) and (b), by the changing of the bias voltage, the FTR and FoM also changed. With the bias voltage increased, the DC power consumption will also increase, which will decrease the value of FoM. For the bias voltage between 0 to 0.4 V, the FoM reaches the peak value at 0.3 V, which is around -183 dBc/Hz and after 0.4V the FoM and tends to worse. In order to keep tail-transistor in saturation region, the best bias voltage should be controlled from 0.1 V to 0.5 V since the threshold voltage of III-V nanowire transistor is 0.15 V. Furthermore, as mentioned before, with the number of finger changed in the varactor, the Q-factor increasing with the finger increased, which means that phase noise will become lower.

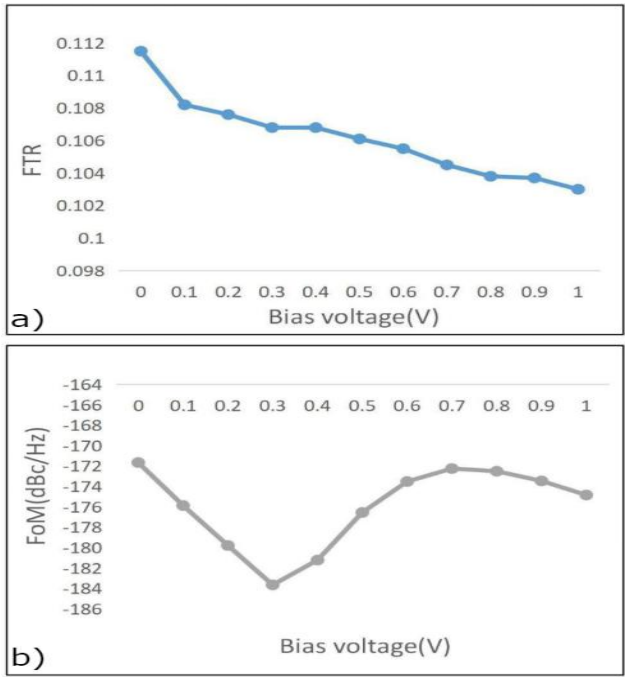

Fig 26(a): Measured FTR with bias voltage varying from 0 to 1 V; (b): Measured FoM with bias voltage varying from 0 to 1 V

Fig 27 illustrates the relationship between FoM & Phase noise and number of finger in varactor when other parameters unchanged. As it mentioned in chapter three, the quality factor of resonator decreased as the number of finger in varactor increased. From Fig 27, the phase noise decreased from -101 dBc/Hz to -113 dBc/Hz, the FoM changing from -171 dBc/Hz to -183 dBc/Hz with number of finger varying from 1 to 15. From Fig 28, the phase noise varying from -109.282 dBc/Hz to -116.842 dBc/Hz when the width changed from 100 nanowire to 1000 nanowire, this means that phase noise of nanowire-based VCO is inversely proportional to the Q-factor based on the discussion in Chaptor three. Therefore, if increasing the Q-factor of the LC-tank, the phase noise will be increased. In general, the higher

Q-factor gives VCO better phase noise, but for the III-V nanowire process is different.

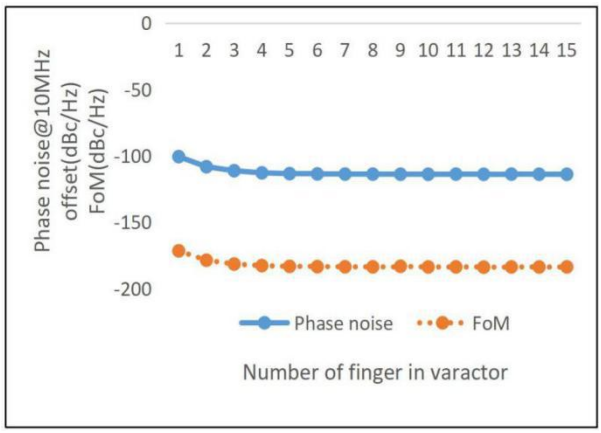

Fig 27: Measured phase noise at 10 MHz offset and FoM with number of finger in varactor varying from 1 to 15

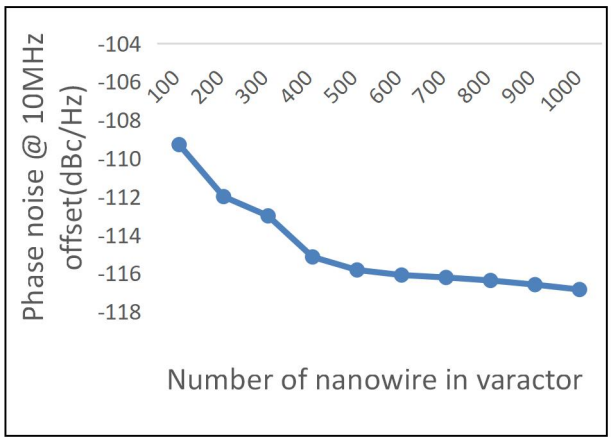

Fig 28: Measured phase noise at 10 MHz offset versus number of nanowire in varactor varying from 100 to 1000

5.3 Comparison with published work

Above all the discussion, by considering the all the design parameters of VCO, the iii-v nanowire vco adopted a cross-coupled differential configuration, 60 nanowire width, 3 fingers and 20 nm length for cross-coupled pair, 300 nanowire width, 60 nm length and 15 fingers for varactor, a 30 pH inductor that Q-factor is 16.61 and 120 nanowire width, 4 fingers and 20 nm length for tail transistor. All transistors are arranged in 20 nanowire per finger, which can behave the best performance of iii-v nanowire transistor. Table 1 illustrates the comparison of VCO that operating around 100GHz based on different technology.

Reference	Frequency(GHz)	Phase noise(dBc/Hz) @10MHz offset	VCO core power consumption(mW)	Tuning range(GHz)	Figure-of-merit(FOM)(dBc/Hz)	Technology
This work	**100**	**-113.883**	**1.59-33.2**	**10.77**	**-183**	**III-V nanowire process**
[1], 2006	98.5	-102.7	7-15	2.58	NA	130nm CMOS
[18], 2008	95.7	-106	9	3.5	-176	65nm CMOS
[19], 2009	102.2	-100.88	7.59	4.1	-172.5	32nm SOI
[20], 2012	103.8	-101.08	12	1.5	-170.6	65nm CMOS
[21], 2013	105	-92.83	54	9.97	-175.48	65nm CMOS
[2], 2012	100	-104.5	3.52-11.9	11.2	-175.5	65nm CMOS
[1], 2006	105.2	-97.5	7.2	0.2	NA	130nm CMOS
[22], 2012	100.6	-104.1	7.2	4.5	--168.25	65nm CMOS

Table 1: Comparison of published high frequency VCO based silicon technology

CHAPTER 6

Conclusion

The main objective of the project is to study, design and simulate a voltage controlled oscillator (VCO) that can be implemented in many RF applications in the range over 100 GHz, such as mobile phone and other millimeter-wave system. In order to achieve the desired wide tunability, linearity, response time, noise performance and cost-effectiveness, a wide range of VCO topologies as well as blocks and tunable components have been illustrated in the background. In this article, a III-V nanowire technology based crossed-coupled differential voltage-controlled oscillator is presented. Table 1 compared the published millimeter-wave fundamental VCOs based on silicon technology with iii-v nanowire process. As the exploration of application in vertical InAs nanowire transistor, the VCO of this paper has behaved much better performance than traditional silicon technology. Tuning range is one of the most important design index for evaluating the performance of VCO. For most of VCO that operating around 100 GHz that have been published, their tuning ranges varying from 0.2-5 GHz. For III-V technology, the VCO can achieve at least 10.77 GHz and even more. To the authors' knowledge, it is the breakthrough of 100 GHz VCO design and it is first time using the III-V nanowire technology into VCO design. In addition, this paper also achieved lower phase noise, which is -113 dBc/Hz and better Figure-of-merit (FoM), which is -183 dBc/Hz. Compared to the VCO based on silicon process, this paper has shown that III-V nanowire technology has competitive performance and should be further explored.

CHAPTER 7

Future work

By implementing the III-V nanowire technology, the power consumption of VCO has been reduced significantly. This work is explored in schematic level and there still a large space that needs to be done. While we have successfully designed a voltage controlled oscillator (VCO) as expected, there are several areas where more researches can be conducted in order to further improve the design. We strongly recommend that one improvement in the future include implementing more improved varactor that may provide a greater space for tuning range. The layout of iii-v nanowire VCO is not included in this paper due to the limitation of the technology. In the following research work, the millimetre-wave VCO that operating extremely high frequency (300 GHz-500 GHz) can be achieved via using improved III-V nanowire transistor model and fabrication of NWFTS can be realized in the future. Furthermore, as an expansion of this thesis, an improved configuration of varactor can be explored for the VCO in future work and it is shown in Fig 16. The capacitors connected to the cross-coupled pair and they should be large enough to block the DC signal from cross-coupled pair. Meanwhile, the function of resistors are using for blocking the AC signal from cross-coupled pair to the ground at voltage source and resistance is usually much large than the impedance of varactor. The voltage source can be used for changing the tuning range by implementing the varying value without requiring the tuning voltage over the supplied voltage or lower the ground. Generally, the tuning voltage is between ground to supplied voltage. For this work, the tuning range is around 5 GHz of

the tuning voltage from 0 to 1 V. By implementing the improved configuration of varactor, the tuning range is increased 10 GHz almost. But the penalty is that the phase noise and Figure-of-merit will be sacrificed at a certain level. This need to be explored in deep in the future work in order to achieve the better performance for III-V nanowire process based VCO.

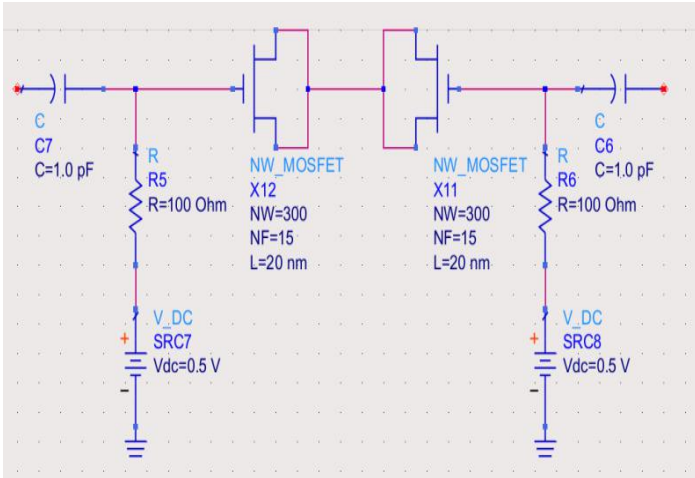

Fig 29: An improved configuration of varactor

Reference

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