LUNDS UNIVERSITET

Ferroelectric Gate-Stack on InAs

PONTUS LITTOW

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Supervised by

PROF. LARS-ERIK WERNERSSON and PROF. ANDERS MIKKELSEN

Nanoelectronics Group
Department of Electrical and Information Technology, LTH
And
Division of Synchrotron Radiation
Department of Physics
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Abstract

Modern electronics are becoming more powerful and energy efficient for every new process generation. A key component in electronics is the transistor, which has made this trend possible. For many years the transistor has simply been scaled down.However, that is not possible any longer. To continue improving the transistor, new structures and materials need to be researched. A promising topic in this field is to use a ferroelectric film to create a negative capacitance FET that could go below the 60 mV/decade limit.

In this thesis, MOSCAPs (Metal-Oxide-Semiconductor capacitors) were fabricated with a $Hf_{0.5}Zr_{0.5}O_2$ oxide and annealed to induce ferroelectricity in the oxide on both Si and InAs substrates. Different sample oxide thicknesses, oxide-deposition temperatures, and annealing temperatures were measured in order to see how they affected their hysteresis curves. I-V measurements, P-E measurements and PUND measurements were used to electrically characterize the samples, and XPS was used to structurally characterize them. The results show clear hysteresis, however, more data need to be gathered to correlate the P-E and PUND measurements, and then to optimize the films further.

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Chapter 1

Introduction

Since the transistor was first created, the way forward has been to just scale down the transistor. This is known as Moore's law, which is an observation that every two years the number of transistors is doubled in an integrated circuit. This trend continued for many years successfully. However, in recent years the scaling down method has not been as successful. Problems arrived and new ideas had to be introduced in order to solve the problems. New geometries and materials were introduced to solve these problems, however, the rate for Moore's law has slowed down. The way forward now has several branches of different ways to continue the transistor evolution. These include: Tunneling Field Effect Transistors (TFETs), 3D integration, III-V materials, negative capacitance FETs, etc. [1]. In Lund university, some of these branches are ongoing research areas in Lund Nano Lab. The negative capacitance FETs (NCFETs) did not gain much traction until it was discovered that hafnium-based oxides could become ferroelectric after annealing [2][3]. Hafnium oxide (HfO_2) is already a common oxide to use as a gate dielectric, which means it has already been integrated in the processing of transistors. With this discovery, more research began on the ferroelectric films and NCFETs around the world at university institutions, [4] also in the industry has research in this area begun [5]. The NCFETs is a so called steep-slope device, meaning the subthreshold swing goes below 60 mV/decade. A normal transistor has a thermionic limit of 60 mV/decade and cannot go lower. This means the NCFET can operate at lower voltages compared to a normal transistor. While the TFETs rely on tunneling between the bands of two materials, the NCFETs look and operate very similar to an ordinary MOSFET. The biggest difference between NCFETs and a MOSFET is that the gate oxide is ferroelectric. The ferroelectric

oxide film provides an amplification of the electric field applied over the channel and can thus go below 60 mV/decade. It is due to this property of the NCFET that the research interest of this area has grown in the past few years. With this type of transistor, the operating voltage can be reduced and thus the transistor is more energy efficient. Since computers and smartphones are so prevalent, and the demand is only increasing, it is important to make electronics more energy efficient. As mentioned, the most important component of this transistor is the oxide. Normally, the oxide is there to prevent current from going from the gate to the channel. The gate controls the channel like a flood gate, raising and lowering the bands to control how much current gets through the channel. This is done by applying a bias at the gate and creating an electrostatic-potential over the channel. At first, SiO_2 was used as a gate dielectric. However, with smaller transistors, leakage current became a problem. The solution to this was to use a high-k dielectric instead, eg. HfO_2. So, the oxide has already been integrated in the Si processing making it ideal for ferroelectric films. Since it was discovered that HfO_2 could become ferroelectric much research into this is made using HfO_2 as a base material. Different dopings have been investigated (Al [6], Si [2], La [7], etc.) and also creating a mixture of HfO_2 and ZrO_2 ($Hf_{0.5}Zr_{0.5}O_2$) [3]. It is this mixture that has been the focus of this thesis work. For $Hf_{0.5}Zr_{0.5}O_2$, the mixture should have a ratio of 1 to 1 of Hf and Zr. In order to accomplish this, an atomic layer deposition (ALD) machine was used which have Hf and Zr as sources. By alternating the pulses of HfO_2 and ZrO_2, the total oxide created should give an oxide with a ratio of 1 to 1 of Hf and Zr. The ALD machine used was the Picosun ALD in the Lund Nano Lab. This work was also run in parallel with another master student, who worked with pure HfO_2 ferroelectric films instead, on another ALD machine in Lund Nano Lab.

Chapter 2

Theory

2.1 Ferroelectric Material

A ferroelectric material is a material which exhibits spontaneous polarization without an electric field and in which the spontaneous polarization can be reversed if an electric field is applied. This spontaneous polarization of the material is not uniform. In ferroelectric material there are regions which have a uniformly oriented polarization, in the same direction, these are called a domains. Two domains next to each other can sometimes have the same direction of the polarization, but switch at different voltages. If these domains are distributed in such a way that, on macroscopic scale, the net polarization is zero, then the material is not ferroelectric. When an electric field is applied, the domains will align in the direction of the electric field. When the field is removed, the material has a polarization now which is called remnant polarization (P_r).

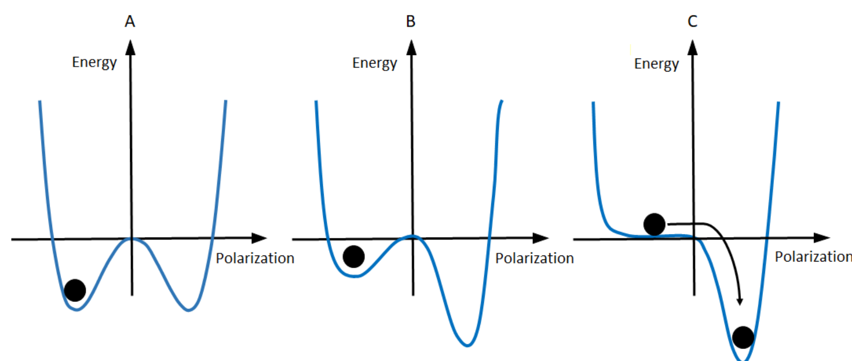

Figure 2.1: Energy vs polarization diagrams, where in A, no electric field is applied; B, a small electric field is applied; and C, the applied voltage is high enough for the ion to move to the other minima. Adapted from [8].

The polarization comes from the ion in the crystal structure of the material having two equilibrium states and can be moved from one state to the other when an electric field is applied. These two states, up or down, can be expressed in an energy versus polarization diagram [9], and is illustrated in Figure 2.1. The curve in this diagram has the shape of a double-well. These two minima in the double-well are the remnant polarization states P_r which have equal and opposite non-zero polarization. Between these two states, there exist a barrier (P=0) which means the two minima states are more energetically favorable than the non-polarization state. If an electric field is applied, then the barrier is lowered and the ion can move to the other state and thus reversing the polarization [8]. This is also seen in the diagram illustrated in Figure 2.1.

2.2 Hysteresis Loop

A P-E curve is the curve of polarization vs. electric field applied of a device at a given frequency. In the case of an ideal capacitor, the P-E curve will be a straight line whose slope is then proportional to the capacitance (as seen in the diagram in Figure 2.2). The current in an ideal capacitor leads the voltage by 90 degrees, which means that the charge is in phase with the voltage [10]. However, in the case of an ideal resistor, current and voltage are in phase, making the P-E curve have an elliptical shape centered on the origin. This can be seen in the diagram in Figure 2.3. Taking an ideal capacitor and ideal resistor and combining the components in parallel will give a P-E curve like the diagram in Figure 2.4. This is essentially a lossy capacitor, where the slope is proportional to the capacitance and the area inside the loop is proportional to the loss tangent of the device. In the case of a ferroelectric material, the resulting P-E curve can be seen in Figure 2.5.

If no electric field has ever been applied on the material, the domains will have spontaneous polarization in different directions. If an electric field is applied arbitrary some of the domains will start to align with the electric field. By increasing the electric field until all of the domains are aligned, polarization saturation can be reached. Subsequently decreasing the electric field to zero will show a nonzero polarization due to many domains still being aligned in the same direction. This is called remnant polarization and is denoted P_r in Figure 2.6 [10]. If a negative electric field is then applied, the polarization will go to zero since the domains were aligned in the opposite direction. The point where the

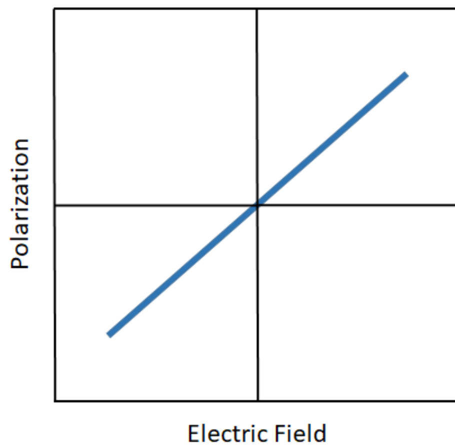

Figure 2.2: P-E curve of a ideal capacitor.

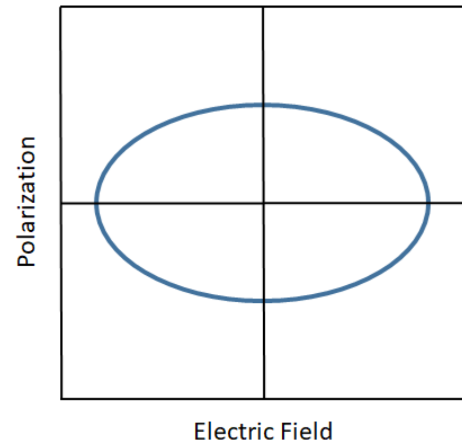

Figure 2.3: P-E curve of a ideal resistor.

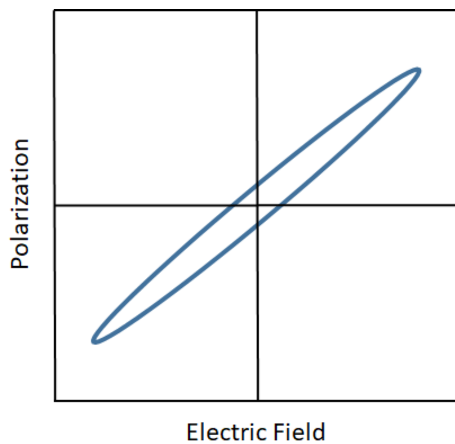

Figure 2.4: P-E curve of a lossy capacitor.

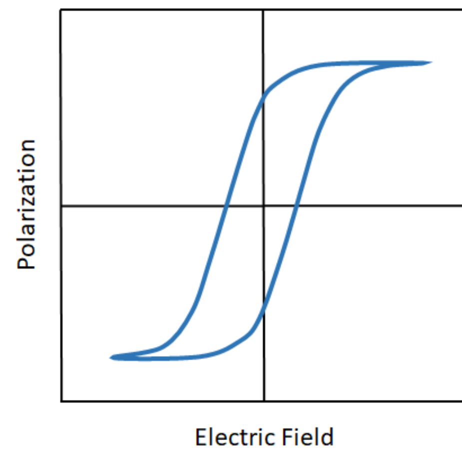

Figure 2.5: P-E curve of a ferroelectric material.

polarization is nonzero with an electric field applied is called a coercive field. Increasing the electric field further aligns domains until polarization saturation is reached, now in the negative direction. Decreasing the electric field back to zero, will result in a remnant polarization here as well. Applying now a positive electric field, causes the polarization to go back to zero as it did before, now for positive bias. This point is also called a coercive field E_c. Continuing to increase the electric field and the polarization comes back to the saturation region. An ideal hysteresis loop is symmetric, meaning the absolute values for the different metrics are the same in both directions of the electric field [10].

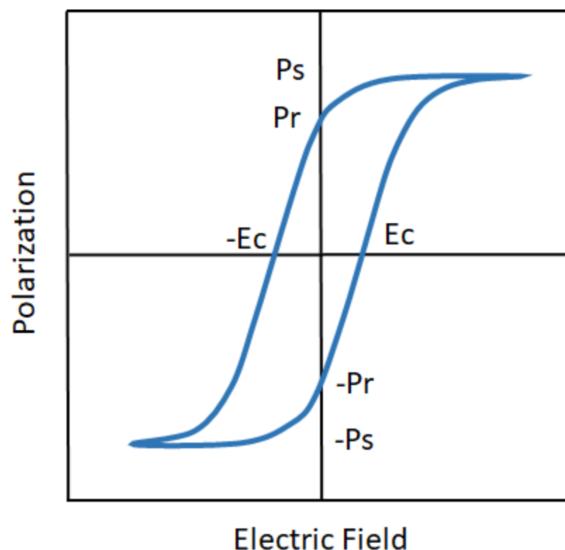

Figure 2.6: Hysteresis curve with important metrics

2.3 Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$

Previous ferroelectric materials that have been used in electronic devices, for instance ferroelectric random access memory, are based on perovskite structural materials. Examples of these type of materials are: $Pb(Zr,Ti)O_3$, $BaTiO_3$ and $SrBi_2Ta_2O_9$. These materials are generally not suited to be integrated on a Si substrate since the interface between the two causes a silicon oxide to be formed [11]. Another problem with these materials are their relatively small band gaps. If these materials would be used in a NCFET, there would be leakage currents and breakdowns. In recent years, it was discovered that HfO_2 doped with Si could become ferroelectric [2]. Since HfO_2 is a a high-k gate dielectric material that is used in the semiconductor industry, it has already been integrated in the Si technology. Another advantage of HfO_2 compared to perovskite materials is that HfO_2-based ferroelectric films have a thickness around 10 nm. Perovskite materials need to be several 100 nm in thickness to become ferroelectric, which is not compatible with modern transistor technology [11]. It was reported that different dopant materials (such as Al, La and Gd [12]) used to dope HfO_2 induced ferroelectric properties. It was also found that alloying HfO_2 and ZrO_2 would result in ferroelectric properties [3]. These two oxides have similar properties because they have similar physical structure and chemical properties. They also have many different polymorphs: monoclinic phase (m-phase), tetragonal phase (t-phase), cubic phase (c-phase) and orthorhombic phase (o-phase). The first three phases are symmetrical but the o-phase is non-symmetrical. It is the o-phase

which gives the hafnia film its ferroelectric properties. The o-phase itself can be divided into several phases: oI-phase (space group Pbca), oII-phase (space group Pnma) and oIII polar-phase (space group $Pca2_1$). The transitions between these different phases depend on temperature and pressure. For example, the transition from the m-phase to the t-phase happens at $1700°C$ at atmospheric pressure. The transition to the oI-phase and oII-phase from the m-phase happens at different pressures, 4 GPa and 14.5 GPa respectively. These conditions are in the case for HfO_2 and ZrO_2. The third orthorhombic phase oIII polar-phase is stable under conditions which include: surface and chemical conditions, as well as different stresses. In the case for Si doped HfO_2, the temperature needed to obtain a ferroelectric film is $800°C$. Comparing this to $Hf_{0.5}Zr_{0.5}O_2$, which can crystallize between $400 - 600°C$ to a ferroelectric phase [11] , means that this oxide has a lower thermal budget. The $Hf_{0.5}Zr_{0.5}O_2$ oxide is thus a more attractive material to use on III-V material due the lower thermal budget. However the $Hf_{0.5}Zr_{0.5}O_2$ oxide can also exhibit anti-ferroelectricity depending on if the oxide has more Zr than Hf. If the oxide has more Hf than Zr, then the oxide will have less polarization. Oxides with the same ratio of Hf and Zr are optimum for a ferroelectric film [13].

2.4 Grains and Film Thickness

While temperature is important for the $Hf_{0.5}Zr_{0.5}O_2$ oxide, the thickness of this oxide is also important. Grains will form in the oxide and are determined by temperature and thickness. These grains are important since the ferroelectric properties of the oxide is dependent on the grain sizes formed. The first critical step is to deposit an amorphous oxide in order to not form any grains that induce m-phase, and instead anneal at a later step inducing crystallization. In order to accomplish this, the deposition temperature needs to be significantly lower than the crystallization temperature. Even deposition close to the crystallization temperature can form m-phase grains. The thickness will, as have said before, affect the polarization. Thicker oxides give lower remnant polarization because more m-phase is formed, which results from larger grain sizes. To have an effective HZO oxide then, the thickness should be less than 20 nm in order to get high ferroelectric polarization[14]. It is also important to cap the oxide with a top contact, which avoids volume expansion and shearing. This in turn reduces formation of the m-phase.

2.5 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a technique to characterize the surface of a material. The method is based on the photoelectric effect, which uses x-ray radiation to excite and release an electron. These electrons are also elastically scattered, meaning the electrons do not lose any energy when they are emitted. The electron is then captured and its kinetic energy is then measured. If the incoming photon has an energy which is equal to that of the work function of the sample, then the outgoing electron has zero kinetic energy and is at rest. This is known as the vacuum level and the electron has no interaction with neighboring particles since it is far away from them, see figure 2.7. The vacuum level is used as zero energy on the resulting spectra. To avoid any energy loss of the ejected electrons (as well as contamination of the material) the sample is placed in ultra-high vacuum ($10^{-8} - 10^{-9} Pa$ [15]). The kinetic energy of the electrons is determined by their binding energy (BE), the energy of the incoming photons, and the work function, which is the energy difference between the valence band and vacuum level. This is expressed in equation 2.1.

$$E_K = hf - (E_B + \phi) \tag{2.1}$$

Where E_K is the kinetic energy, hf is the energy of incoming photon, E_B is the binding energy and ϕ is the work function of the material[16]. BE is the difference between the core shell, energy level where the electron excited from, and the valence band energy level. The binding energy gives information about which element it is since every element on the periodic table has different BE peaks for the same core level. This is because their nuclear charge is different. When the kinetic energy of the electrons is measured, by convention the spectra displays a BE scale to identify the element more easily. Thus equation 2.1 is usually rewritten as:

$$E_B = hf - E_K - \phi \tag{2.2}$$

However, the binding energy of a core level in an atom or molecule is dependent on the surroundings of the atom or molecule. This is due to charge transfers which can leave an atom with positive or negative charges, and leads to shifts in the binding energies of core levels. It is also associated with the coulombic attraction between the electrons in the core, and the nucleus [16]. An example of this is an atom in a high oxidation state having a higher binding energies than the same atom in low oxidation state. This is called a

chemical shift, and can be as large as 10 eV [16]. So, while a peak for every distinct atom could be observed in the sample, this is not always the case because the energy spread of incident radiation will often be larger than these chemical shifts. Since the technique uses x-rays instead of electrons for spectroscopy, the damage to the sample is much smaller than other electron-based spectroscopy techniques. Also, contamination of the sample is much lower. [15].

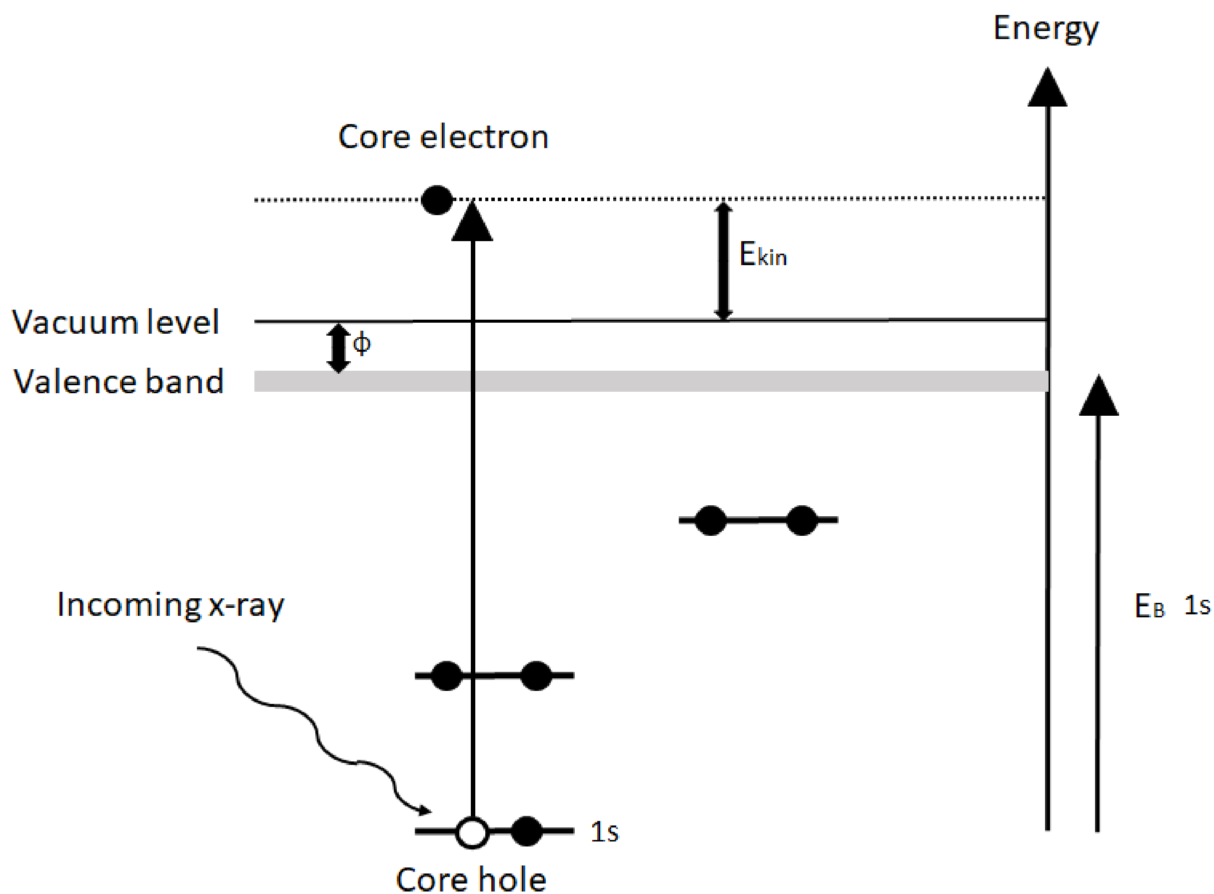

Figure 2.7: Excitation of a core electron by an x-ray. Figure adapted from [16].

Chapter 3

Processing of ferroelectric films

3.1 Silicon Wafer

The fabrication process started with a 2-inch wafer of silicon. The wafers used in this work had low resistance, meaning they were highly p-doped (boron). The crystal orientation of the wafers was (100). The thickness of the wafers was about 0.3 mm and had a resistivity of 0.003 to 0.005 Ωcm. The wafers was then cleaved down into smaller samples; this was done using a diamond tip and scratching along the crystal direction on the back side of the wafer and then applying pressure in order to break it in half.

3.2 InAs Wafer

One of the goals for this project was to put $Hf_{0.5}Zr_{0.5}O_2$ oxide on a III-V material. InAs was then chosen to be used. This InAs wafer was doped (n-doped) in order to make it low resistant. The dopant here was sulphur and the carrier concentration was between 1.67 - 2.48 $10^{18} cm^{-3}$. The crystal orientation was also in the (100) direction, same as the silicon wafers studied. The thickness of the wafer was between 0.504 and 0.517 mm. The resistivity was between 0.000020 and 0.0000108 Ωcm, which is lower than the Si substrate. On top of this wafer, another 100 nm of InAs was grown. This part was purposefully not doped with sulphur. However, there will always be some impurities that will act as dopants. So, this undoped InAs still has an effective carrier concentration of about $10^{16} cm^{-3}$.

Though InAs has a melting temperature of about $942°C$, under atmospheric pressure,

there is a problem of diffusion at temperatures of $500°C$ and above. At these temperatures, In and As can diffuse into the oxide which will create defects. These defects can affect device degradation, by increasing leakage currents and by lowering the reliability of the device [17]. Due to this, the samples which were made with InAs substrate were not annealed above $400°C$. The only samples which were annealed above $400°C$ have been on Si substrates.

3.3 Atomic Layer Deposition

The first step in the fabrication of the ferroelectric films was the deposition of the $Hf_{0.5}Zr_{0.5}O_2$ oxide. This was done in the Picosun Sunale R-100 ALD (atomic layer deposition) machine. This machine does thermal ALD, meaning the oxidation comes from water (H_2O) and not from ozone. The Picosun machine is located inside a glove box which has a nitrogen atmosphere, protecting the oxide and sample from oxygen. The hafnium precursor used is called tetrakis(dimethylamido)hafnium (TDMAHf). For zirconium, tetrakis(ethylmethylamido)zirconium (TEMAZr). The source temperatures were set to $80°C$ for Hf, and $110°C$ for Zr. The oxidation reactant in this reactor is water and the temperature of the source is $26°C$. All settings can be seen in table 3.1. In order to grow the $Hf_{0.5}Zr_{0.5}O_2$ oxide, the pulses are alternated so to create a 1 to 1 ratio of Hf and Zr, this then produces an oxide with the same amount of Hf and Zr in the film. So, first TDMAHf was pulsed in and then purged, followed by H_2O in the same manner. After this, TEMAZr was pulsed in and goes the same way as the Hf pulse. This was also followed by the water pulse and purge. Each pulse of HfO_2 and ZrO_2 creates a monolayer of oxide that diffuses together to create a $Hf_{0.5}Zr_{0.5}O_2$. An illustration of the mono layers can be seen in figure 3.1 The usual rate for growth in ALD is 0.9 Å/cycle for both Hf and Zr [18].

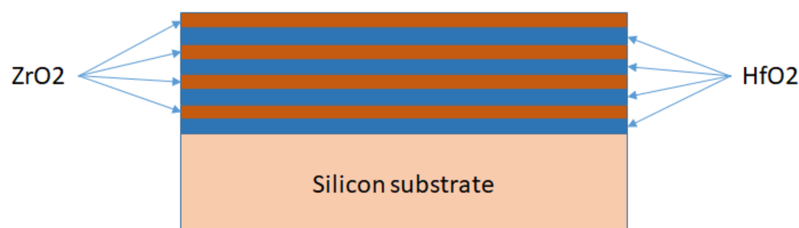

Figure 3.1: Monolayers of HfO_2 and ZrO_2

Settings for precursors in ALD				
Material	Pulse time [s]	Purge time [s]	Temperature [$°C$]	Flow [sccm]
Hf	1.6	5.0	80	80
Zr	1.6	5.0	110	150
H_2O	0.1	10	27	150

Table 3.1: Settings for precursors in ALD

For this thesis work, different thicknesses were grown in the ALD using different reactor temperatures. Every sample had a MOS structure except for one reference sample, which was made with 10 nm TiN on silicon, making it a MIM (metal-insulator-metal) structure. On top of this TiN, $Hf_{0.5}Zr_{0.5}O_2$ was grown as the other samples. All the samples grown in the ALD are shown in table 3.2. After the deposition, the ellipsometer was used to measure the thickness.

Thickness and temperatures of samples grown in ALD		
Substrate	Thickness oxide [nm]	Temperature in chamber [$°C$]
Si	10	200
Si	10	250
Si reference	10	250
Si	12	250
Si	15	250
InAs	15	200

Table 3.2: Thickness and temperatures of samples grown in ALD.

It should be noted that the Picosun ALD machine is not perfect. The machines sample holder can, at maximum, fit a 4 inch wafer. As a test for seeing how the growth of the oxide is on the area of the sample holder, a 4-inch wafer is placed and 40 nm of ZrO_2 was grown. The results can be seen in figure 3.2. The settings for the Zr and H_2O were the same as in table 3.1. As can been seen in the figure, there is a discoloration at the bottom left of the wafer. Figure 3.3 and figure 3.4 show a ellipsometric map of the 4-inch wafer, with the first figure showing the thickness across the wafer, and the second figure showing the MSE (mean square error) along the wafer. The discolored part in the wafer is

located at the bottom of the ellipsometric maps. These two figures show that it was not a uniform deposition across the wafer and that the discolored area appears to have a thicker oxide than the rest of the wafer. These figures show that the location of the sample in the sample holder is important to get the intended thickness of the oxide. Although it was not investigated how this nonuniform deposition arises, one theory is that the sample holder is in the way of the precursor gases which come from the sides of the chamber, and therefore the gases are not uniformly deposited in this area.

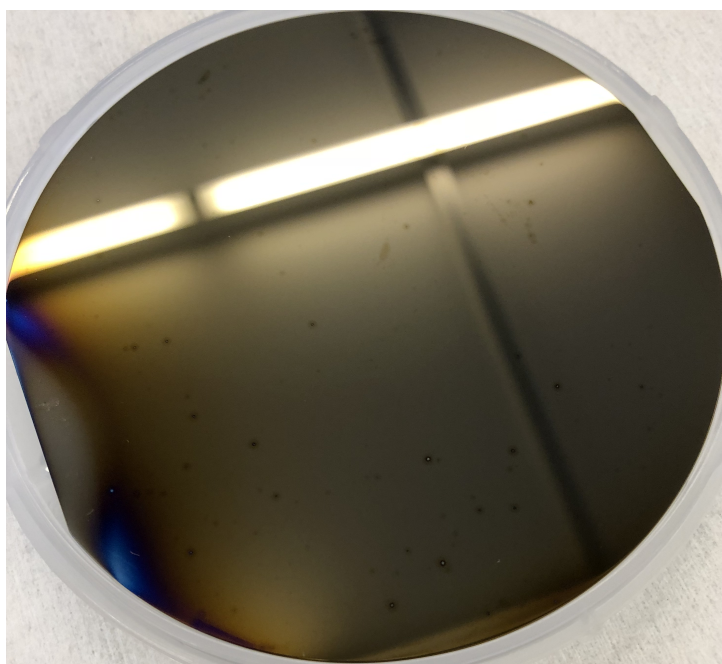

Figure 3.2: 4 inch silicon wafer with 40 nm of ZrO_2 deposited on top by ALD.

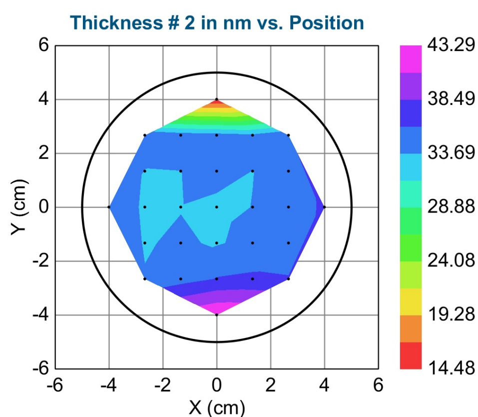

Figure 3.3: Ellipsometer thickness map of the 4 inch wafer in figure 3.2.

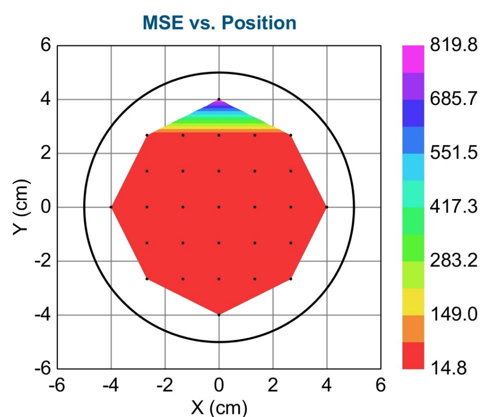

Figure 3.4: Ellipsometer MSE map of the 4 inch wafer in figure 3.2.

3.4 Sputtering

After the deposition of the oxide in the ALD machine, the top contact is defined of the MOS cap. This process is performed in the sputtering machine, AJA Orion 5. Sputtering is a physical vapor deposition (PVD) method to deposit various metals. The target (the material to be deposited) is hit with energetic ions which are generated from a plasma. The plasma is situated in front of the target. This process of bombardment will cause the removal of the target atoms. The target atoms will then condense and form a thin film on the sample surface[19]. To define the top contacts on the sample a shadow mask was used. The shadow mask is a thin metal piece which contains small openings of six different circular sizes. The largest opening has a radius of about 100μm, followed by sizes of 70μm, 60μm, 50μm, 30μm and the smallest size has a radius of about 25μm [20]. These openings defined the top contacts after the sputtering is complete. The metals used in this work were TiN and W. First 10 nm of TiN is sputtered followed by 100 nm of W. After this process, MOS caps with six different areas were formed (see figure 3.5).

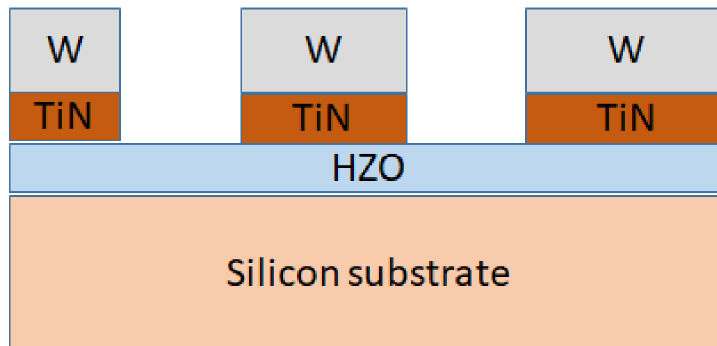

Figure 3.5: A cross section of the MOS stacks after sputtering TiN and W through a shadow mask.

3.5 Rapid Thermal Anneal

After the samples were fabricated, they were split into 4 pieces. This way, after the samples were annealed, 4 different temperatures could be used, one temperature for each piece of the sample. The annealing was done in a RTP 1200-100 machine in Lund nano lab. With rapid thermal annealing (RTA), the sample is quickly heated and then cooled down very quickly. The idea is to heat the sample very quickly to a temperature, stay at

that temperature for some time and then quickly go down in temperature. Unfortunately, the machine misses the target temperature and overshoots the temperature (see the graph in Figure 3.6). In this work, the annealing temperature started at 600°C and moved down in order to find the lower temperatures where the film would still be ferroelectric. This would help conserve the thermal budget in case of integration into a transistor.

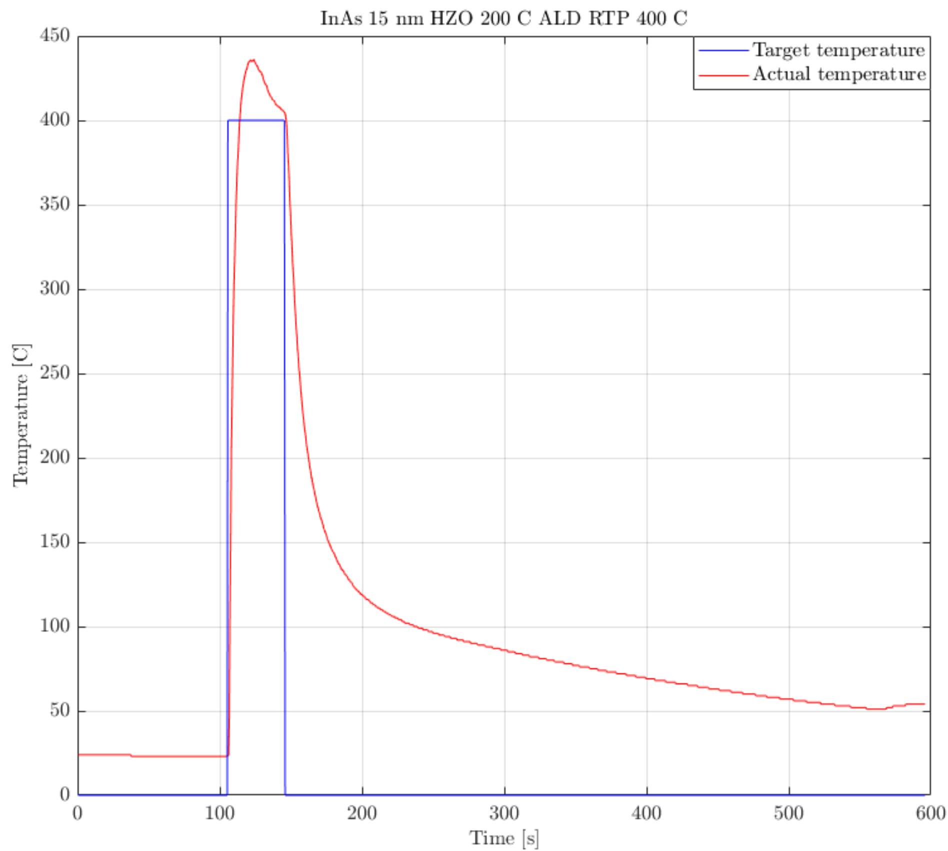

Figure 3.6: Temperature profiles of a RTA run.

Annealing temperatures		
Sample	Deposition temp. [°C] and substrate	Annealing temperature [°C]
10 nm $Hf_{0.5}Zr_{0.5}O_2$	200 °C ALD Si	600, 550, 500, 450
15 nm $Hf_{0.5}Zr_{0.5}O_2$	250 °C ALD Si	500, 450, 400
15 nm $Hf_{0.5}Zr_{0.5}O_2$	200 °C ALD InAs	400, 375, 350

Table 3.3: Annealing temperatures. The annealing time was 40 s for all runs.

Chapter 4

Measurement

4.1 I-V Measurement

The first measurement performed on a sample was a I-V measurement using the Cascade 11000B probe station in Lund Nano Lab. It uses a Keithley 4200A parameter analyzer. Here, a voltage is applied to the top contact and the machine measures the current through the sample. The sample is placed on a chuck which acts as the back contact and ground. To apply a bias, a probe is placed on the top contact. The initial voltage is set and it is swept in steps while the current is measured at each voltage step.

4.2 P-E Measurement

To determine if the $Hf_{0.5}Zr_{0.5}O_2$ is ferroelectric, a Polarization-Electric field (P-E) measurement was done. To do this, first a function generator applies a voltage bias over the sample as an input signal. This bias has the form of a triangle wave. The generated current from the capacitor was measured and then converted in to a voltage by a current to voltage converter, this voltage is the output signal. The output signal is connected to an oscilloscope and compared to the input signal which is also connected to the oscilloscope (as can be seen in the picture in Figure 4.1). The signals are aligned and the voltage for the input signal is increased. The P-E curves can now be extracted from the data. However, already from the oscilloscope it is possible to see if the device is ferroelectric or if it behaves like a regular capacitor. As mentioned before, the input signal is a triangle wave and if this signal is applied on a capacitor then the output signal would be a square

wave. If the out-signal continues to be a square wave even if the voltage is increased, then the device is not ferroelectric. If the oxide is ferroelectric, it would be expected for there to be two peaks and no longer look like a square wave. One peak would be a leakage peak and the other, a ferroelectric peak. With aligned phases, the leakage peak lines up with the highest value of the triangle wave and the ferroelectric peak would then come before the voltage peak.

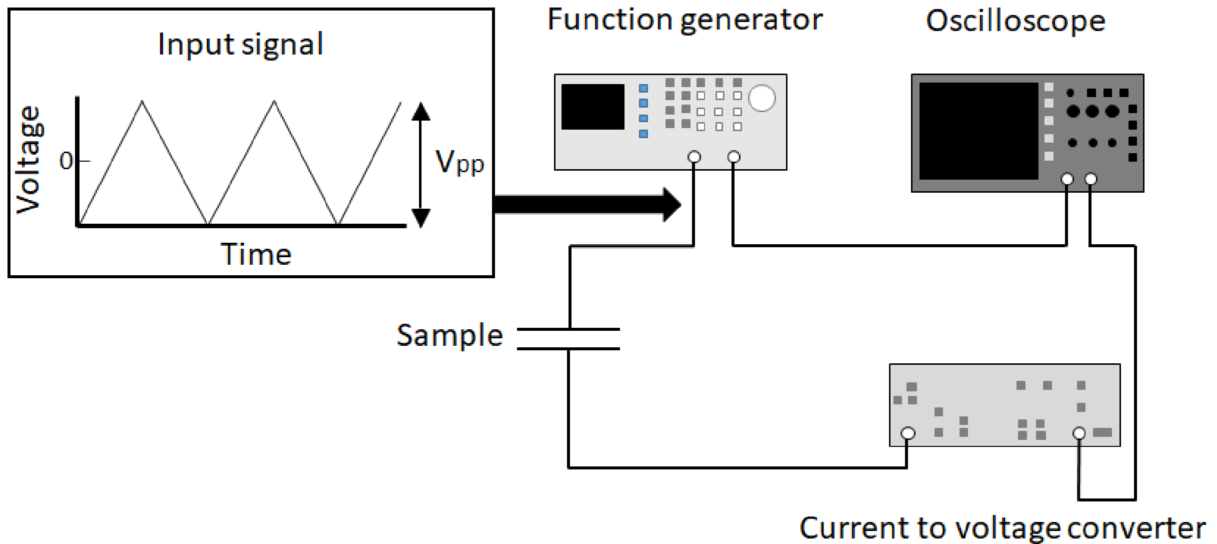

Figure 4.1: Setup of the P-E measurement

After the measurement, the P-E curves can be extracted from the data. First, the electric field is calculated via equation 4.1.

$$E = \frac{V_{pp}}{d} \tag{4.1}$$

Where E is the electric field, V_{pp} is the voltage and d is the thickness of the oxide. The charge can be obtained from the current by integrating over time, as seen in equation 4.2.

$$Q(t) = \int_{t_1}^{t_2} I dt \tag{4.2}$$

By dividing the charge by the area of the device, the dielectric displacement, D, can be calculated as the surface charge density;

$$D(t) = \frac{Q(t)}{A} \tag{4.3}$$

where A is the area. In this case, $A = \pi r^2$, since the top contact is a circle. From

Maxwell's equations, the displacement D can be written as:

$$D(t) = P(t) + \epsilon_0 E(t) \tag{4.4}$$

and if the polarization is proportional to and aligned with the electric field, it can be written as:

$$P(t) = (\epsilon_r - 1) * \epsilon_0 E(t) \tag{4.5}$$

where ϵ_r is the relative permittivity of the dielectric. Since $Hf_{0.5}Zr_{0.5}O_2$ is a high-k dielectric, P(t) will be larger than $\epsilon_0 E(t)$. By neglecting $\epsilon_0 E(t)$ in equation 4.4 due to P(t) being larger, the equation can thus be written as:

$$D(t) = P(t) \tag{4.6}$$

with the displacement being equal to the polarization. Equation 4.3 can therefore be written as:

$$P(t) = \frac{Q(t)}{A} \tag{4.7}$$

4.3 PUND Measurement

In the previous measurement method, the leakage current cannot be separated from the ferroelectric current. To discriminate between these currents PUND measurements were used. In this measurement, two positive voltage signals are applied followed by two negative voltage signals. In the virtual ground measurement, it is one positive, followed by a negative, voltage signal. This means the first positive signal switches the ferroelectric material so there is a ferroelectric peak. The second positive signal then would not switch the ferroelectric material but just the leakage current. This way it would be possible to take current from the second output signal and subtract it from the first. This way the actual amount of current generated from the ferroelectric oxide could be determined. For the negative signals, it would be the same as with the positive signals. The first negative voltage switches the ferroelectric material and the second signal is used to filter out the leakage current. See figure 4.2.

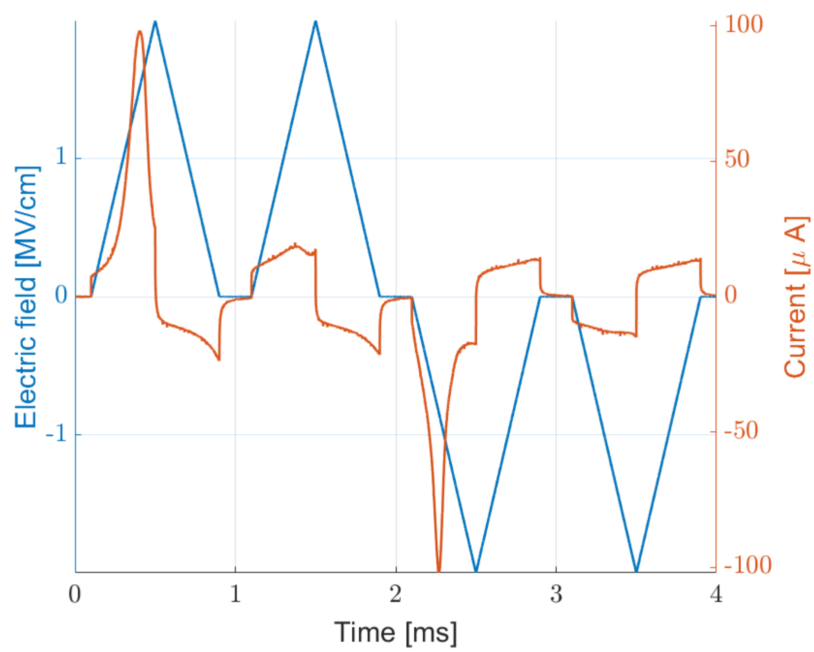

Figure 4.2: Example of a measurement with PUND.

Chapter 5

Results

In this chapter, the results from the experiments are presented. First, the I-V measurements are presented, followed by the P-E measurements, PUND measurements and XPS measurements.

5.1 I-V Measurement Results

In this first section the results from the I-V measurements are presented.

The first I-V measurements were done on 3 samples. All the samples were the same except the oxides. One sample had pure HfO_2, another pure ZrO_2, and the third had $Hf_{0.5}Zr_{0.5}O_2$. All the oxides had the same thickness (10 nm) and were deposited at the same temperature (200 $°C$). The substrates were of the same type, and the same thickness of the top contacts was used. In these measurements the voltage was swept from 0 to 4 V. The results presented in a graph in Figure 5.1.

From the results presented in Figure 5.1, one can note the spread of the HfO_2 and ZrO_2 curves. These results could be due to the deposition of the top contacts not being well defined due to the shadow mask. It could also be the deposition settings in the ALD not being the most optimized for the individual oxide. However, the $Hf_{0.5}Zr_{0.5}O_2$, as can be seen in the figure, is not spread out and well defined.

The second I-V measurement was performed on the $Hf_{0.5}Zr_{0.5}O_2$ sample in the previous measurement. Here, the different areas of the top contact were investigated as a function of voltage (see the results in Figure 5.2). The currents was divided by their areas to normalize the curves. One would expect the currents to be the same; however, the shadow

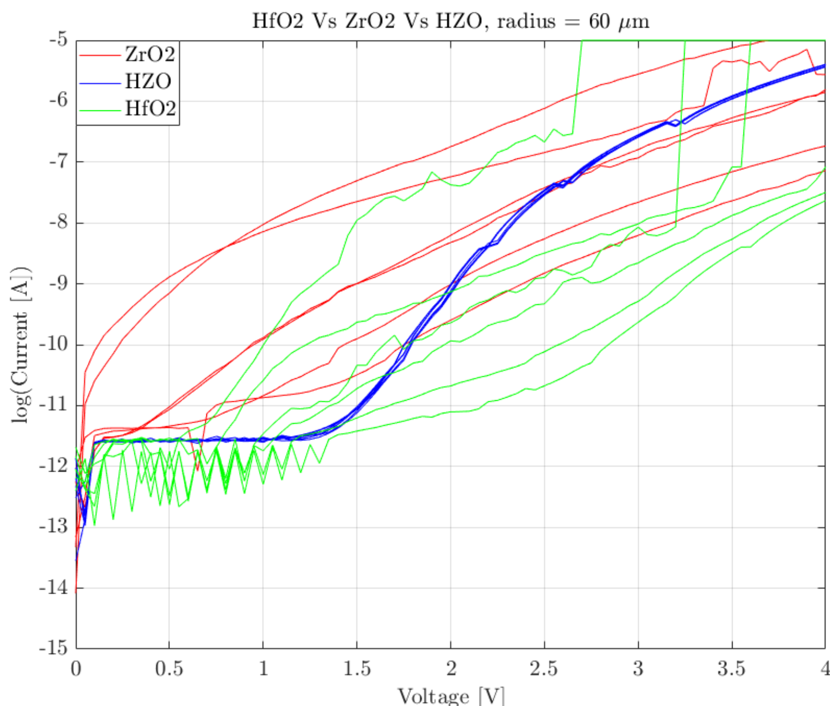

Figure 5.1: I-V measurement of HfO_2, ZrO_2 and $Hf_{0.5}Zr_{0.5}O_2$.

mask can give top contacts with different areas even though they are supposed to have the same area. Since we assume here that they have the same area for the same size when we divide by the area this could lead to the difference we see in the current density.

The next sample measurement shows the influence of deposition temperature on 3 samples. The first sample was the previous sample measured. The second and third samples were deposited at 250 $°C$. However, one of these two samples was the reference sample, which had 10 nm TiN between the oxide and the substrate. The resulting I-V measurement can be seen in figure 5.3. In this figure, we see a clear difference between the currents. The currents for the 200 $°C$ sample is lower as compared to the 250 $°C$ samples. We could thus see that deposition temperature for the sample in the ALD will impact the oxide.

In the next measurement, thickness was investigated for the same deposition temperature. The samples here had 10, 12 and 15 nm thick oxides and the deposition temperature was 250 $°C$. As can be seen in the results presented in figure 5.4, the thicker (15 nm) oxide has lower leakage currents compared to the 10 and 12 nm samples. This is expected, since thicker oxides usually reduce leakage currents. However, for integration into a transistor, the oxide cannot be this thick.

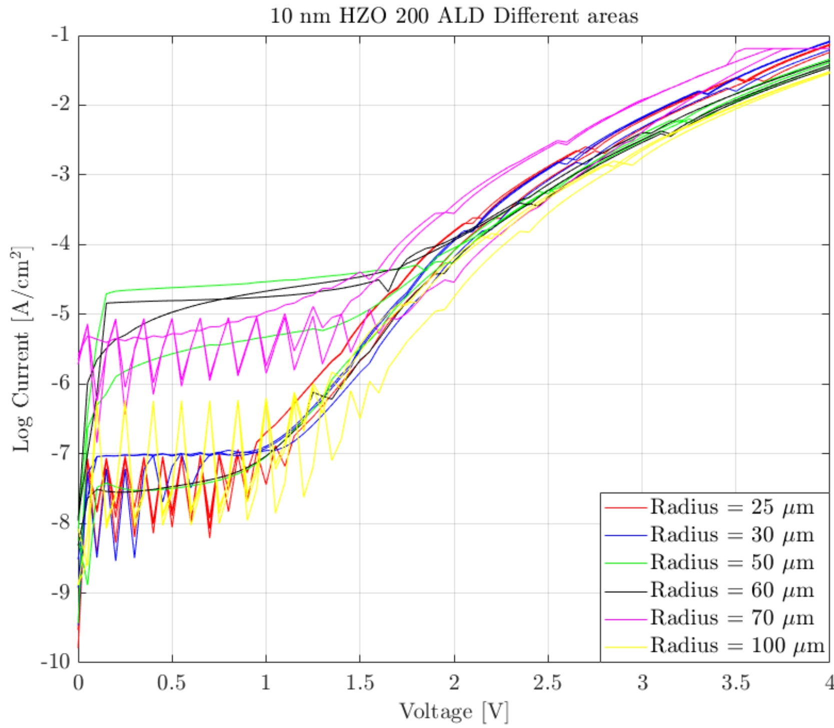

Figure 5.2: Current density (current divided by area) as a function of voltage.

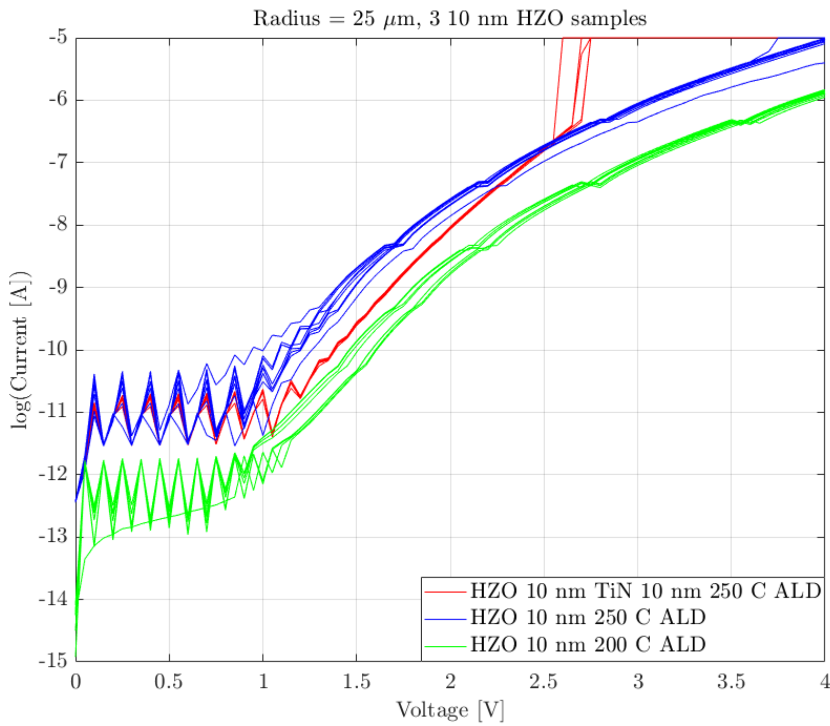

Figure 5.3: I-V measurements with the same thickness of $Hf_{0.5}Zr_{0.5}O_2$, but at different deposition temperatures.

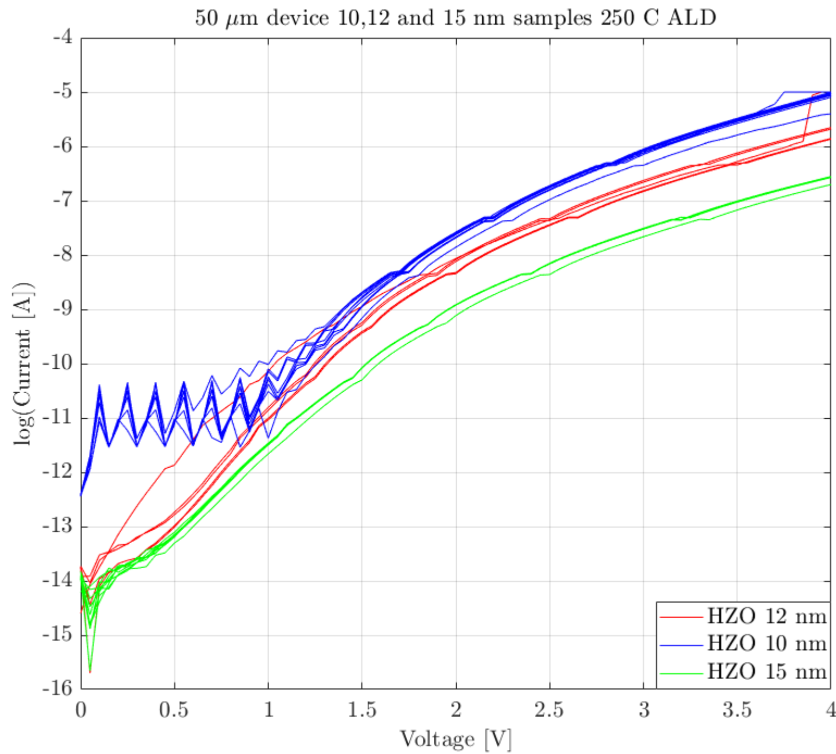

Figure 5.4: I-V measurements of samples with the same deposition temperature but different thicknesses of $Hf_{0.5}Zr_{0.5}O_2$

.

With the previous results in mind, the InAs sample was fabricated to have the lowest leakage current based on the parameters that have been used in this work. From the previous results, figure 5.3 shows that the sample deposited at 200 $°C$ has lower leakage current than the sample deposited at 250 $°C$. A thicker oxide helps to reduce leakage current. Thus, these parameters were applied to the InAs sample. In figure 5.5, the results from I-V measurement of the InAs sample are presented.

So far, all the I-V measurements were performed with a positive bias applied at the top contact. In figure 5.6, the difference between a positive bias and negative bias applied to the top contact are presented. It shows that the MOS cap is not symmetrical and at higher voltages the direction of the bias will influence on how much leakage current there is. This is important to remember when the P-E measurement is analyzed, since both a positive and a negative bias are applied.

Taking all the data from these samples and plotting them in the same graph gives figure 5.7. In this figure, one can see that, the InAs sample had the lowest leakage current.

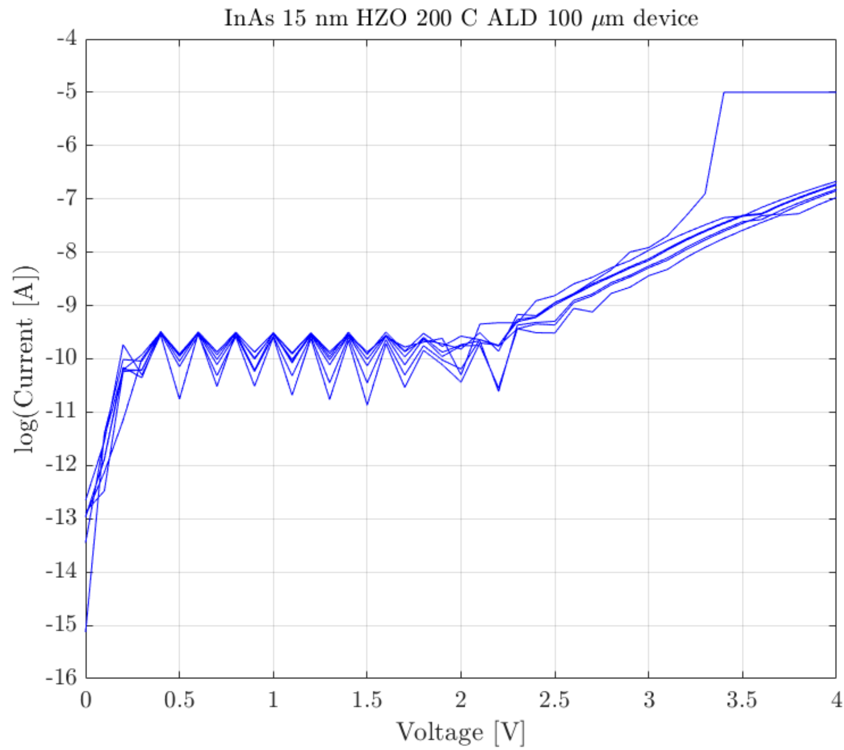

Figure 5.5: I-V measurements of the InAs sample

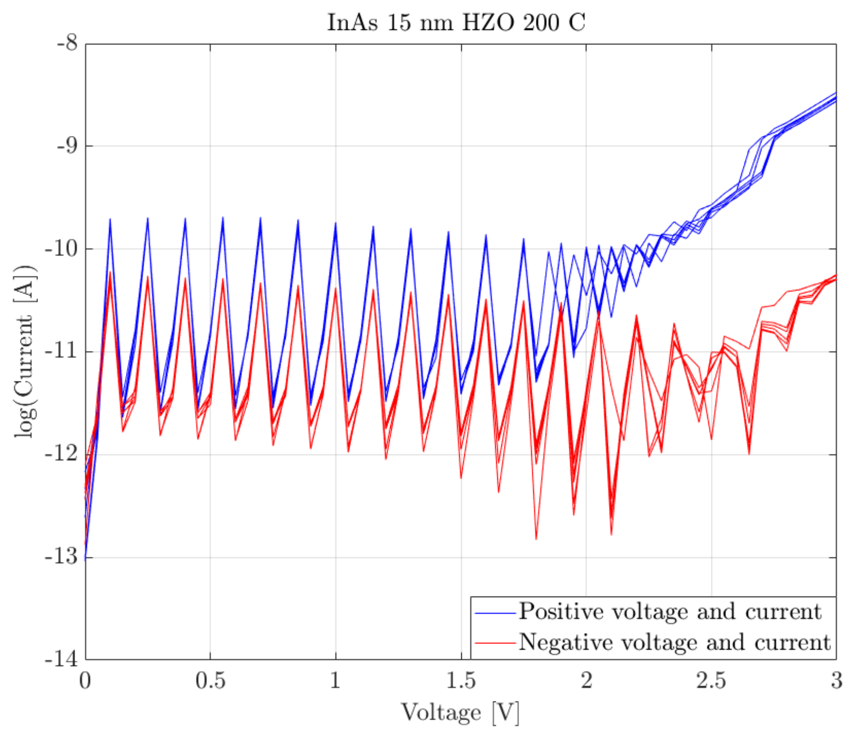

Figure 5.6: I-V measurements of the InAs sample with both positive and negative voltages.

However, it is difficult to say anything more about this graph because there are too many variables. These three samples have different oxide thicknesses, deposition temperatures and one of them has a different substrate. Thus, one cannot say if the low leakage current of the InAs sample is due to the oxide thickness, or deposition temperature, the substrate itself, or a combination of the three. All that can be said about this graph is that the InAs sample has smaller leakage current than the other two.

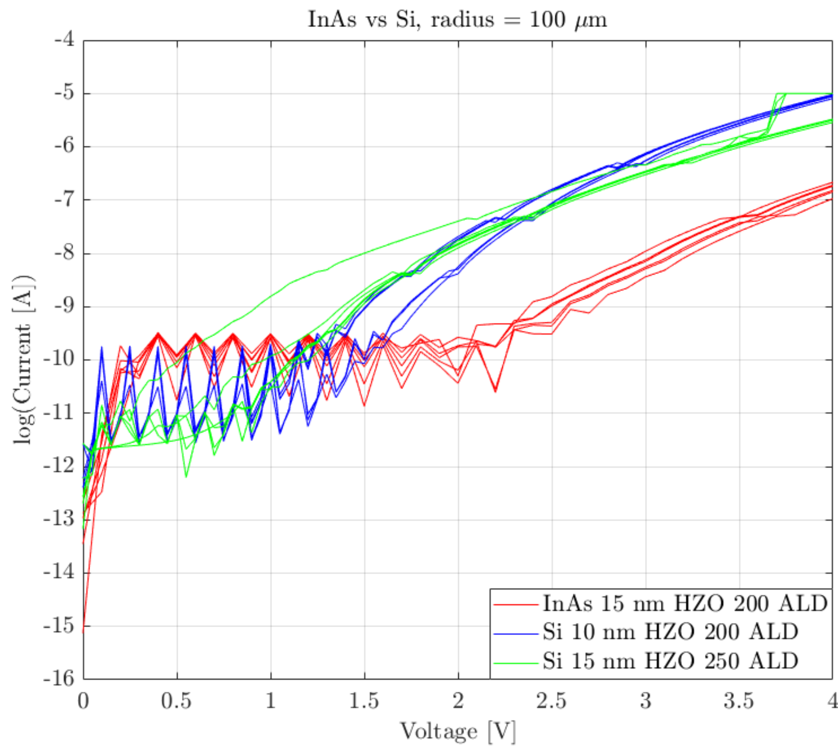

Figure 5.7: I-V measurement of InAs and Si samples.

5.2 P-E Measurement Results

In this section, the results from the P-E measurements are presented.

The first sample measured on here is the silicon sample with 10 nm $Hf_{0.5}Zr_{0.5}O_2$ and deposited in the ALD at 200 $°C$. The results from this sample is presented in figure 5.8, and one can see the hysteresis curves and current from voltage sweeps. In this figure, voltage V_{pp} (see figure 4.1) is swept from 3 to 9 V in increments of 1 V. In the figure, one can see that when the voltage is increased, the polarization is also increased. This corresponds to more domains switching that were not switched at a lower voltage. One can also see that the current increases with increasing voltage. By looking at the current, one sees how the current increases differently depending on whether a positive or negative bias is applied. The negative current occurs at a lower electric field than the positive current. This means that the sample is not symmetric and shows the same effect as in the I-V measurement section.

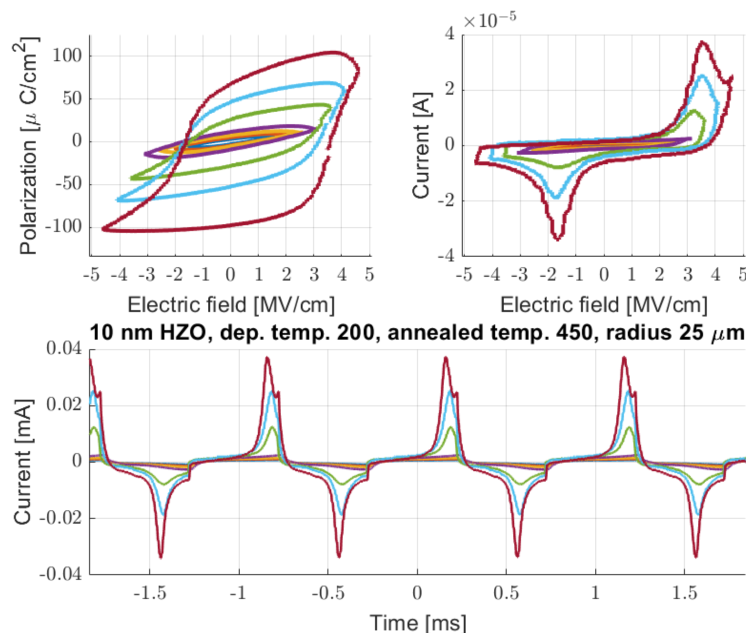

Figure 5.8: P-E measurements with increasing V_{pp}.

In the positive electric field, it is noted that another peak, together with the ferroelectric peak, is also growing with increasing voltage. This is the leakage current, which becomes more prominent at higher voltages. See figure 5.8, 9 V. This leakage current is not filtered out in this measurement and will affect the hysteresis curve. As can be seen in figure 5.8, the largest of the hysteresis curves (9 V) has a well-defined saturation tail in

the negative polarization area. However, in the positive polarization area, the saturation is not well-defined and is more rounded compared to the negative polarization saturation. This effect is due to leakage current. As can be seen in the current vs. electric field graph in figure 5.8, there is no leakage peak in the negative current area. Which would affect the hysteresis curve in the negative polarization area.

To verify that the measurement method is actually working, and does give a response to ferroelectric materials, the method was performed on a sample which had not been annealed. The results of this can be seen in figure 5.9. In the polarization diagram, the curves show how a leaking capacitor responds to a P-E measurement. It is similar to the curve showed in fig 2.4.

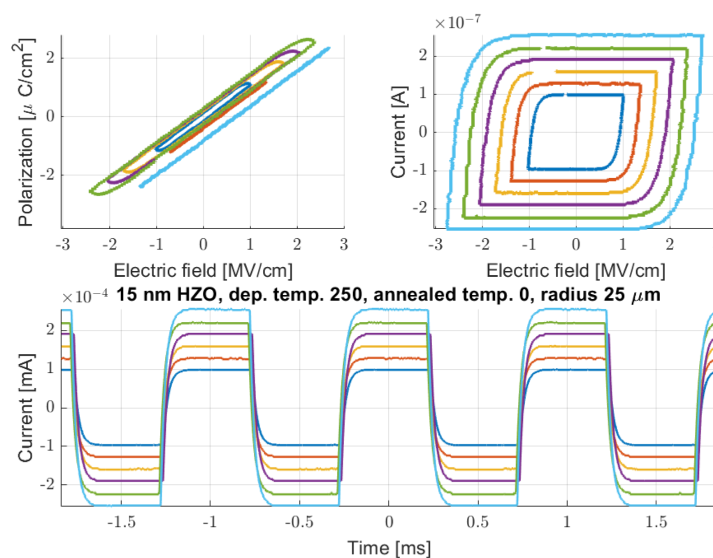

Figure 5.9: P-E measurement of a sample which has not been annealed.

The next step was to measure how the annealing temperature affects the hysteresis curve. In figure 5.10, the results from four annealing temperatures are plotted from the silicon sample with 10 nm $Hf_{0.5}Zr_{0.5}O_2$ and deposited at 200 $°C$ ALD. Here, all the curves had the same electric field applied (7 V) and were measured on devices with the same top contact radius. It can be clearly seen how the annealing temperature affects the hysteresis curves. The highest annealing temperature was 600 $°C$ and is the purple curve in the figure. In the current vs. electric field graph, it is shown in the negative electric field area that there are two peaks. One is the leakage peak and the other is the ferroelectric peak. At the positive electric field area, there is also a leakage peak. These peaks, together, give this rounded shape in the hysteresis curve. It can also be seen that these leakage peaks

are reduced as the annealing temperature is decreased, especially the peak in the negative electric field region. For the 550 °C and 500 °C temperatures in figure 5.10, the hysteresis curves have a very similar shape, with the 450 °C temperature being smaller but have more well defined hysteresis curve. To compare these curves, the remnant polarization is extracted and is shown in table 5.1. Comparing these values, they show that 450, 500 and 550 °C remnant polarization (positive and negative polarization) are very close to each other. This, however, is not the case for 600 °C, since its values are further away compared to the other temperatures. This is likely due to leakage current.

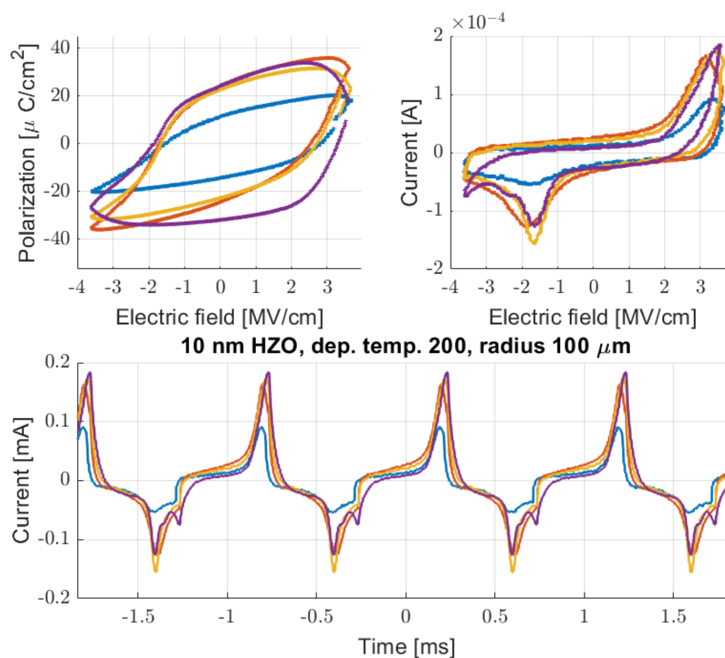

Figure 5.10: P-E measurements of Si sample with 10 nm $Hf_{0.5}Zr_{0.5}O_2$ 200 °C ALD for four annealing temperatures at $V_{pp} = 7$ V. Blue was annealed at 450 °C, copper at 500 °C, orange at 550 °C and purple at 600 °C.

The same type of graphs shown in figure 5.10 were also put together for the Si 15 nm $Hf_{0.5}Zr_{0.5}O_2$ 250 °C sample. However, here there are three annealing temperatures instead of four. The results can be seen in figure 5.11. The same voltage was applied to generate the results as in the previous P-E results. The largest difference here is the amount of current. In these results it is about half of the current in figure 5.10. Since the current is smaller this leads to smaller polarization (equation 4.7). This can be seen in the P-E curves. The extracted remnant polarization can be seen in table 5.2. These values are smaller compared to the ones in the previous results. This is likely due the

Remnant polarization of four annealing temperatures		
Temperatures [$^\circ C$]	Polarization [$\mu C/cm^2$]	Negative polarization [$\mu C/cm^2$]
450	12	-14
500	24	-24
550	23	-23
600	24	-32

Table 5.1: Remnant polarization of four annealing temperatures of the Si sample with 10 nm $Hf_{0.5}Zr_{0.5}O_2$ deposited at 200 $^\circ C$ ALD.

current levels being lower.

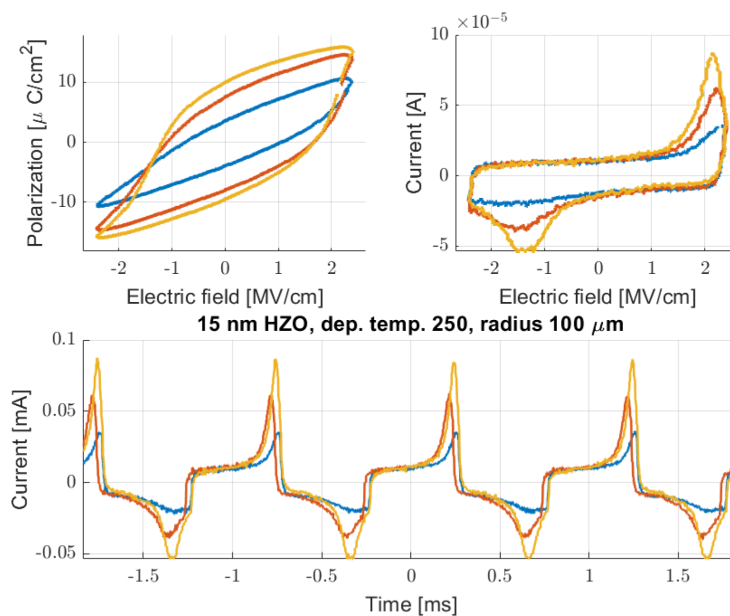

Figure 5.11: P-E measurement of Si sample with 15 nm $Hf_{0.5}Zr_{0.5}O_2$ deposited at 250 $^\circ C$ ALD for three annealing temperatures at $V_{pp} = 7$ V. Blue was annealed at 400 $^\circ C$, copper at 450 $^\circ C$, orange at 500 $^\circ C$.

For the InAs sample, the results can be seen in figure 5.12. Here, the same voltage and radius was used as in the previous P-E results. The current curves are very symmetrical in these results, with both the positive and negative currents being almost at the corresponding electric field. There is also no leakage current here, leading to very sharp, well-defined hysteresis curves in the P-E graphs. However, the 350 $^\circ C$ annealed sample in the P-E graph is just a straight line meaning the lower bound of the annealing to make

Remnant polarization of three annealing temperatures		
Temperatures [°C]	Polarization [$\mu C/cm^2$]	Negative polarization [$\mu C/cm^2$]
400	4	-4
450	7	-8
500	10	-10

Table 5.2: Remnant polarization of four annealing temperatures on the Si sample with 15 nm $Hf_{0.5}Zr_{0.5}O_2$ deposited at 250 °C ALD.

the material ferroelectric has been reached. But with the overshoot of the machine it is hard to say what temperature exactly the lower bound is at. The remnant polarizations can be seen in table 5.3. The positive and negative polarization values are also very close to each other here.

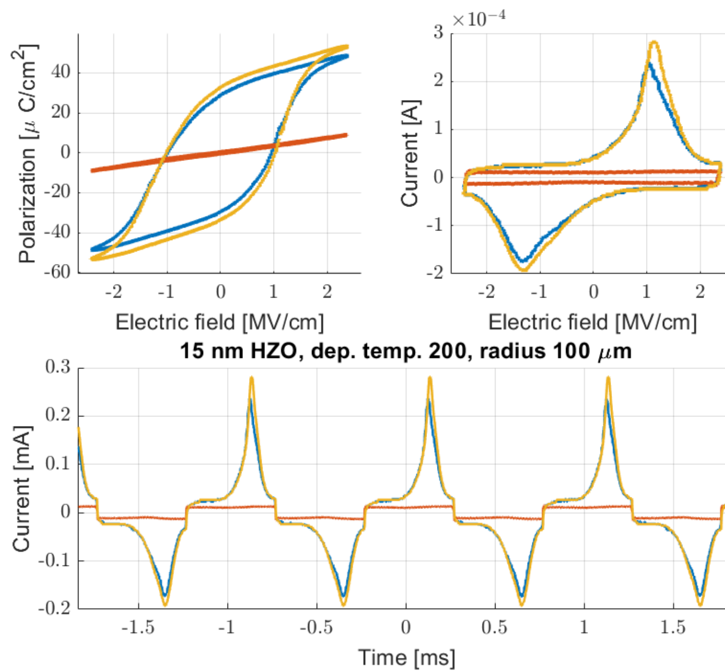

Figure 5.12: P-E measurements of InAs sample with 15 nm $Hf_{0.5}Zr_{0.5}O_2$ deposited at 200 °C ALD for three annealing temperatures at V_{pp} = 7 V. Blue was annealed at 400 °C, copper at 350 °C, orange at 3750 °C.

In figure 5.13, the InAs annealed at 375 °C is plotted for different top-contact areas. The V_{pp} applied here was 6 V. There should not be a dependence on the area, since the current is divided with the area to plot the hysteresis curves and because in a larger

Remnant polarization of three annealing temperatures		
Temperatures [$°C$]	Polarization [$\mu C/cm^2$]	Negative polarization [$\mu C/cm^2$]
400	29	-29
375	33	-34
350	1	-1

Table 5.3: Remnant polarization of four annealing temperatures of the InAs sample 15 nm $Hf_{0.5}Zr_{0.5}O_2$ 200 $°C$ ALD sample.

area, more current goes through. This is what the P-E plot is showing. There is some deviation though, since the areas used in the calculations are assumed to be those stated in the sputtering section and are not necessarily exact. The remnant polarization can be seen in table 5.4.

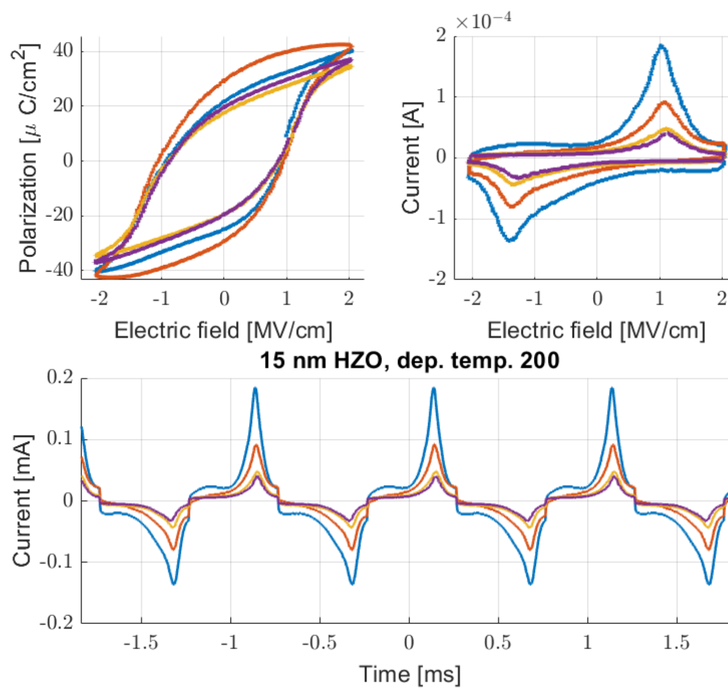

Figure 5.13: P-E measurement of InAs sample annealed at 375 $°C$ for different areas. Blue curve = 100 μm, copper = 70 μm, orange = 60 μm, purple = 50 μm

Remnant polarization of four annealing temperatures		
Radius [μm]	Polarization [$\mu C/cm^2$]	Negative polarization [$\mu C/cm^2$]
100	22	-25
70	30	-29
60	18	-19
50	20	-20

Table 5.4: Remnant polarization of InAs annealed at 375 $°C$ for different areas.

5.3 PUND Measurement Results

In this section, the PUND measurement results are presented. This measurement technique developed over time and did not work until late in the thesis work. Due to this, the data gathered by the PUND measurements cannot be fully compared to the data shown by the P-E measurements in the previous section. These differences included the applied V_{pp} and the size of the top contact. Since the measurements where performed so late in the thesis work, only InAs samples were able to be measured on.

The first result here is the not-annealed InAs sample. This was to make sure there is no ferroelectric response. It can be seen in figure 5.14. Here, there is no difference between the first and second pulses; the same with the third and fourth pulses. This kind of response confirms that the sample is not ferroelectric.

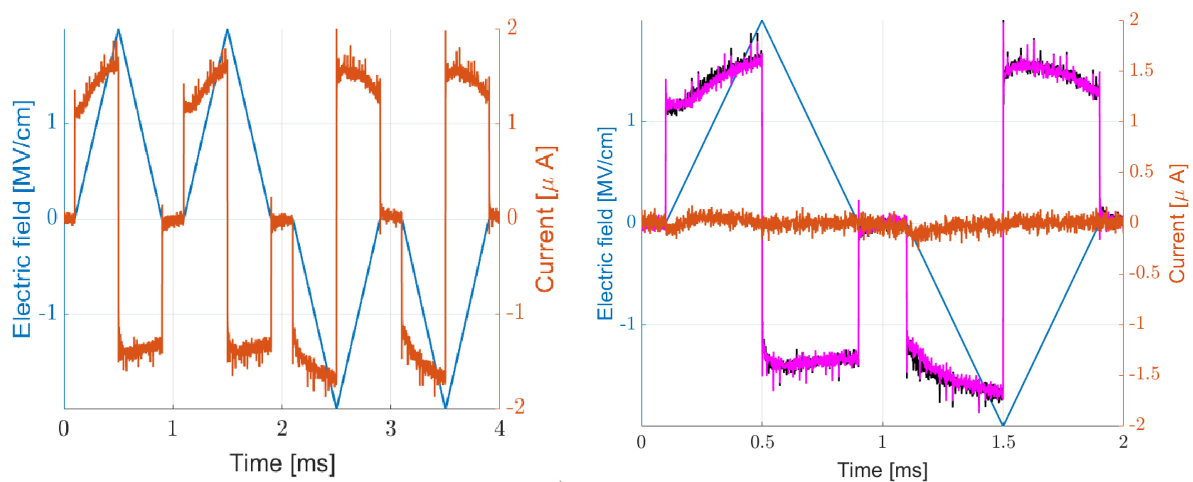

Figure 5.14: PUND measurements of a non-annealed InAs sample 15 nm $Hf_{0.5}Zr_{0.5}O_2$ 200 $°C$ ALD, V_{pp} = 6 V, radius = 30 μm.

The second sample investigated was the InAs sample, which was annealed at 400 $°C$. From the previous section (P-E measurements) this sample was expected to be ferroelectric. The PUND results for this sample can be seen in figure 5.15. As expected, the measurement gives a ferroelectric response with a $P_r = 17\mu m/cm^2$ and a $-P_r = -18\mu m/cm^2$, for a V_{pp} of 6 V. As stated, these results cannot be compared with the same results from the previous section. Here V_{pp} is set 6 V and in figure 5.12 V_{pp} is set to 7 V.

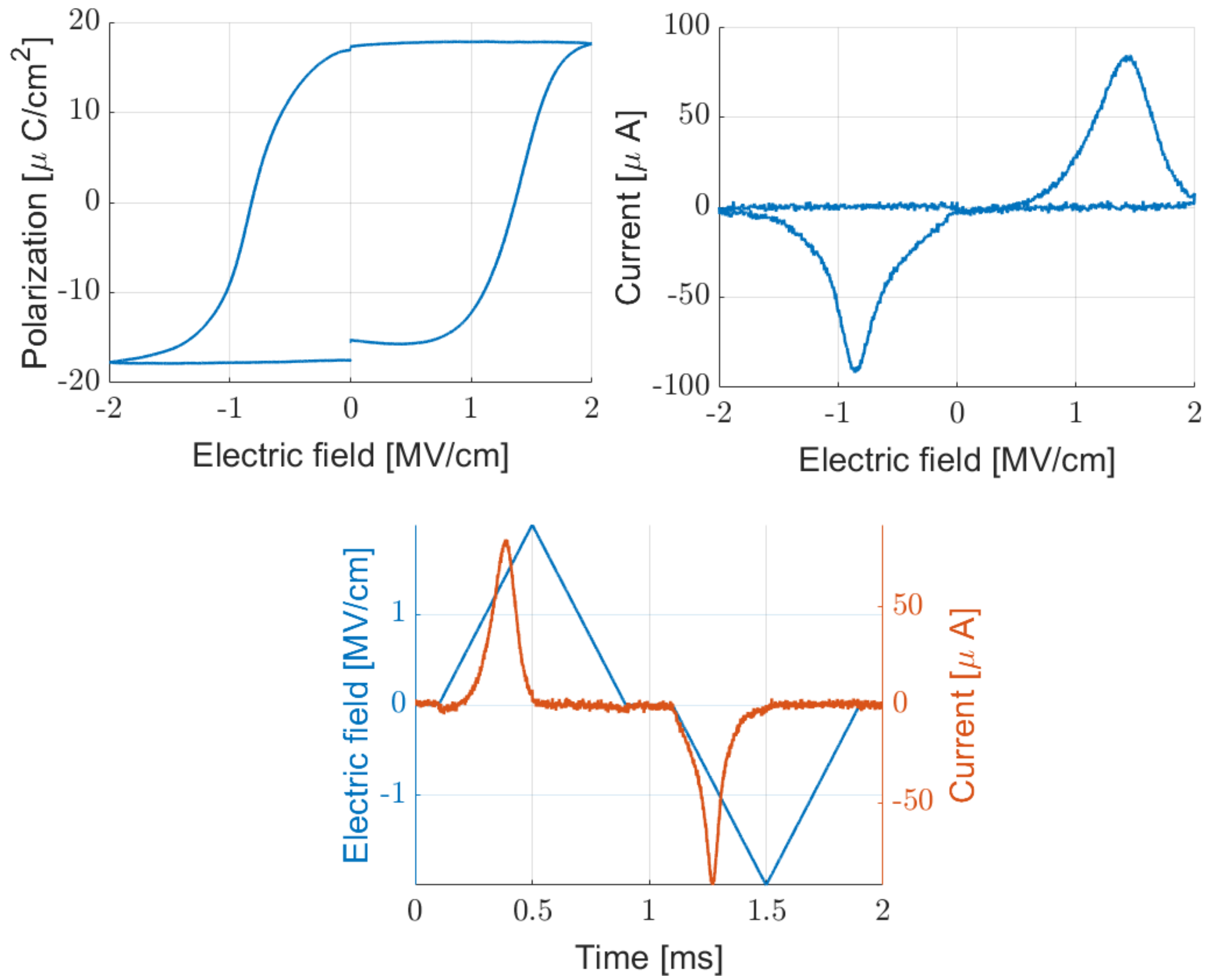

Figure 5.15: PUND measurements of InAs sample 15 nm $Hf_{0.5}Zr_{0.5}O_2$ 200 $°C$ ALD, annealed at 400 $°C$, $V_{pp} = 6V$, $radius = 100\mu m$.

The third sample is the InAs sample which was annealed at 375 $°C$. As with the 400 $°C$ annealed InAs, it was also expected to be ferroelectric. It was, as is shown in the P-E measurement results section. The PUND result can be seen in figure 5.16. As expected, there was a ferroelectric response, with $P_r = 40\mu m/cm^2$ and $-P_r = -41\mu m/cm^2$. V_{pp} was set to 6 V. In figure 5.13, the same V_{pp} is applied and the 50 μm component has about half the remnant polarization. It is hard to say if this difference is due to the component, since the data is not from the same device. The two components can have different top contact areas but in the calculations they were assumed to have the same area. Also, it is hard to say if the methods give different results because this is just one data point and the data set for the PUND measurement is not large enough to make comparisons with the other results or to make any conclusions.

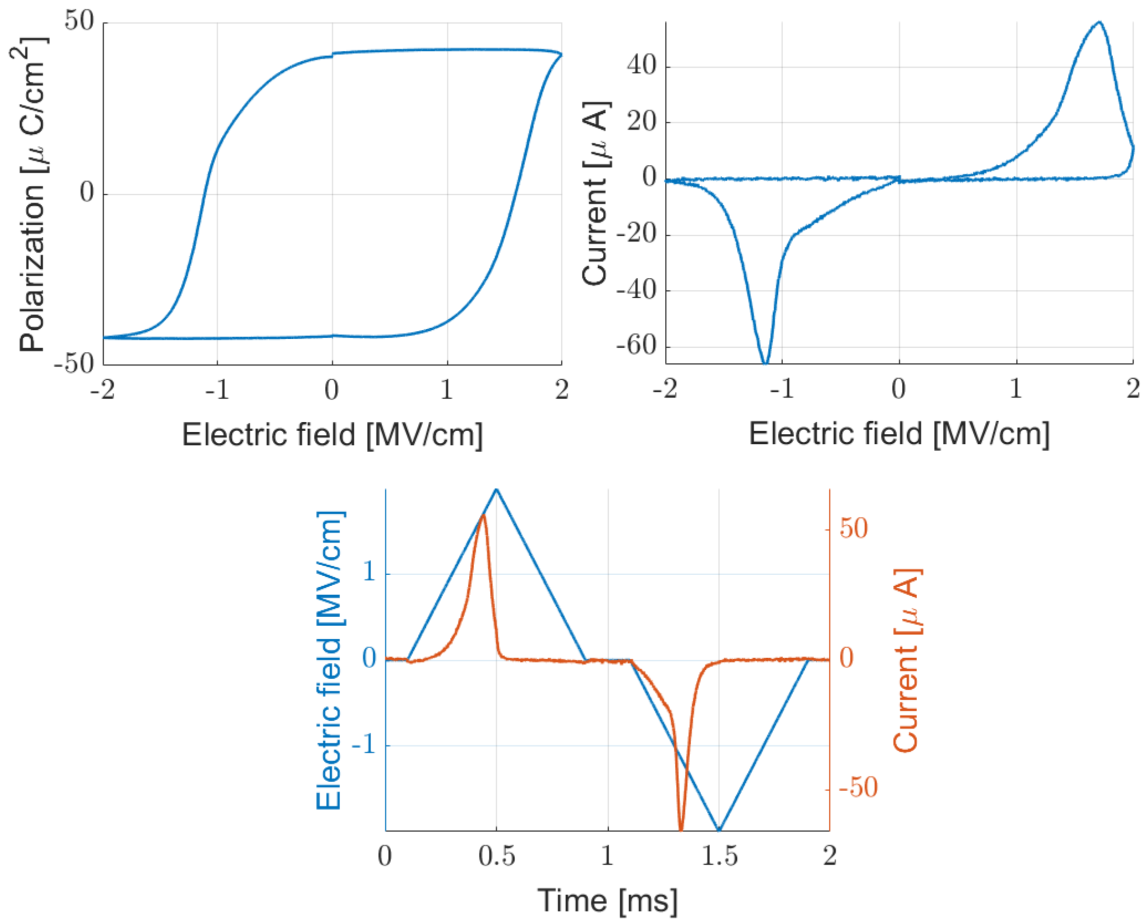

Figure 5.16: PUND measurement of InAs 15 nm $Hf_{0.5}Zr_{0.5}O_2$ 200 °C ALD, annealed at 375 °C, $V_{pp} = 6V$, $radius = 50\mu m$.

The 350 °C annealed InAs sample was also measured and the result can be seen in figure 5.17. This sample was not expected to be ferroelectric from the results shown in the P-E measurement section. However, as can be seen in this figure, there is a ferroelectric response, though it is very small. The remnant polarization here is $P_r = 4\mu m/cm^2$ and a $-P_r = -4\mu m/cm^2$ for a V_{pp} of 8 V. The small polarization is attributed to the low current in the figure, which is much smaller compared to the current levels in figure 5.15 and figure 5.16. The V_{pp} applied here is also large. However, as noted before, increasing the voltage increases the polarization. Since the advantage of the PUND measurement is to be able to filter out it‘s possible that there is a ferroelectric current in the P-E measurement in figure 5.12 but it cannot be resolved from the leakage current due them having similar absolute values. However, it is hard to say if this is due to the sample, or due to the measurement methods‘because the same components were not measured with both methods.

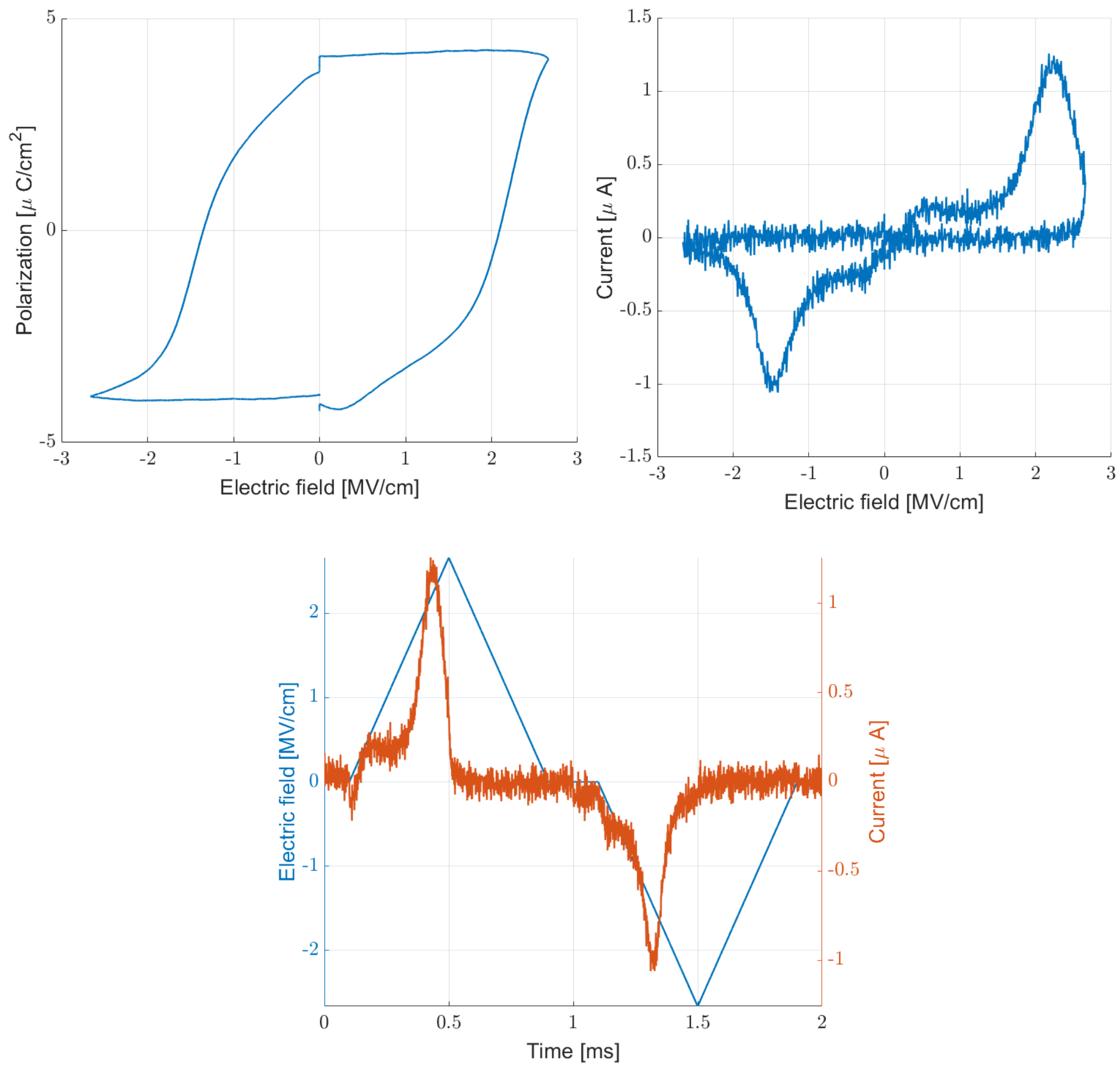

Figure 5.17: PUND measurement of InAs 15 nm $Hf_{0.5}Zr_{0.5}O_2$ 200 °C ALD, annealed at 350 °C, $V_{pp} = 8V$, $radius = 25\mu m$.

5.4 XPS Measurement Results

Two of the samples that were made were sent to be measured by XPS. These samples where Si 10 nm $Hf_{0.5}Zr_{0.5}O_2$ 250 $°C$ ALD and the silicon reference sample with 10 nm TiN between the substrate and the oxide (see table 3.2). The analysis of the data from this measurement takes time and thus was not able to be reported in this thesis.

Chapter 6

Conclusion

This thesis project has shown that is possible to fabricate ferroelectric films on a III-V material in Lund Nano Lab. In this work, capacitors with a MOS-cap structure were fabricated with $Hf_{0.5}Zr_{0.5}O_2$ as the dielectric, on both Si and InAs substrates, with their properties characterized. The structures were characterized with different electrical and structural measurements and the results were presented in chapter 5.

The electrical measurements show clear hysteresis curves from the ferroelectric films. The I-V measurements show how the oxide thickness and deposition temperature affects the I-V curves. The XPS analysis was unfortunately not completed and could not be put in this report. For future work, more systematic measurements need to be performed to correlate the data between the P-E measurements and PUND measurements.

The results from this project demonstrate the ability to fabricate ferroelectric films for future projects at the Lund Nano Lab. Here, only two deposition temperatures in the ALD were measured and they might not be fully optimized. The settings for the ALD (pulse time, purge time, etc.) were not changed in this work and might also not be optimum. The ALD machine itself also could contribute to problems in the films as shown in Chapter 3.

The largest challenges will come with integration into a transistor. The transistor switches millions of times during its lifetime and so the ferroelectric film must also have a similar lifespan after these cycles. This is an important metric to consider and future scientists should to develop methods to measure the endurance of these films [21] and learn how to prolong their lifetime. The scalability of the oxide is also a topic which needs to be investigated.

The results from this work represent a good foundation for future research here at the Lund Nano Lab, particularly for the future of the transistor.

Chapter 7

Acknowledgement

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