Simulation and Measurement of Inductive Coupling between Bond Wires in Integrated Circuits

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Abstract

When making an Integrated Chip, there is a process called contacting or bonding. In this process, the circuit is connected to the capsule. As a result, there is interference between the bond wires through inductive coupling. At higher frequencies, the problem becomes more apparent, which means that the role of frequency in interference should be investigated. By using a bonding machine and making our own measurement prototype, measurements were conducted. Bonding wires on PCB's with different layouts made it possible to investigate differences in interference and coupling. The measurements are also compared with values from a simulated model. PCB's were manufactured with different spacings for bond wires located on them. Measurements showed a measurable increase in crosstalk as the spacing decreased. Simulations with a model representing the different spacings yielded simulated values which showed a good accordance with measurements. Efforts to limit the coupling were made using two methods. The first method involved using grounded conducting lines beneath the bond wires. These were routed both parallel and perpendicular to the wires. The second method involved copper lines in a similar fashion to the first method, but placed in a way such that an additional bond wire can be placed on them parallel to the existing bond wires, in between them. While the first method had little effect on the coupling between the wires, the second method using a ground wire arrangement was found to be effective. On average, the crosstalk was reduced by 4.50, 4.82, and 6.16 dB on the different PCB's.

Sammanfattning

När Integrerade Kretsar konstrueras finns en process för att koppla krets och kapsel som heter kontaktering eller bondning. Under denna process kopplas kretsen till kapsel. Till följd av detta blir det induktiv koppling mellan kontaktledningar. Vid högre frekvenser blir detta ett mer påtagligt fenomen vilket innebär att induktionens roll bör undersökas. Med hjälp av en bondningsmaskin och vår egna mätprototyp genomfördes mätningar. Bondtrådar på kretskort med olika utformningar gjorde det möjligt att undersöka skillnader i koppling och störningar. Överhörningen ökade då avståndet mellan trådarna minskade. Överhörning som uppmätts på mätprototypen jämfördes sedan med simulerad överhörning från en simulerad modell. Simulerade värden för de olika trådavstånden stämde bra med motsvarande mätvärden. Två metoder undersöktes för att minska kopplingen. Den första metoden involverade jordade kopparledningar som låg både parallelt och vinkelrätt mot bondtrådarna. Den andra metoden involverade ledningar som liknar de förutnämnda, med tillsatsen av en ytterligare bondtråd mellan de övriga trådarna. Den första metoden visade sig vara ineffektiv för att minska överhörningen mellan bondtrådarna. Dock visade mätdata från den senare metoden att kopplingen minskade. I genomsnitt minskades överhörningen mellan trådarna med 4.50, 4.82, och 6.16 dB på de olika tillverkade mätprototyperna.

Popular Science Summary

What happens when electronic devices are pushed to their limits?
Many electrical devices contain some sort of Integrated Circuit, or IC. These small chips can operate as timers, oscillators or even CPU's, making them invaluable in many applications. IC's have pushed the boundaries of both performance and space, making it possible to manufacture high-performance devices in compact spaces. IC manufacturers have managed to make IC elements as small as only 10 nm![11]. Compact dimensions can cause problems however, which becomes apparent when connections to IC's are formed, for instance.

Bond wires are a cost-effective and relatively practical way of forming connections to an IC, making them a popular option for many manufacturers. Compact IC's and a large number of input- and output-connections mean that the spacing between these wires often becomes small. It is then that the problem of coupling between wires manifests itself. Depending on the application, coupling between wires can have a significant deteriorating effect on the performance of chips. Signals sent along one path can leak over to an adjacent path and cause issues, depending on the sensitivity of the chip. Higher frequencies serve to worsen this problem as inductive coupling increases.

In this thesis, forward transmission and crosstalk between bond wires was measured. PCB's, or Printed Circuit Boards, with space for bond wires were manufactured for the purpose of investigating the coupling. Boards with bond wire spacings of 0.15 mm, 0.325 mm, and 0.5 mm were manufactured. In order to investigate possible methods of limiting the inductive coupling, circuits with different limiting arrangements were manufactured. The first method was a simple structure beneath the wires for the purpose of disrupting the magnetic field of the bond wires. The second method involved an additional wire in between to bond wires, which was connected to bond pads in turn connected to a ground. The first method was relatively ineffective in reducing the crosstalk. The latter method showed promise however as the coupling was reduced by several magnitudes.

The phenomena investigated in this thesis can serve to better understand the interference that manifests itself as coupling between bond wires. This is especially important as higher frequency applications are becoming more and more common

in electronics. Methods that have been investigated for the purpose of limiting the coupling that occurs has the possibility of aiding in the design of circuits such as RF-frequency Integrated Circuits, or RFIC's. Coupling problems discussed in this thesis is not only limited to RFIC's however. These methods can also be helpful in the design of digital circuits, as signals with short rise- and fall-times can also cause unwanted coupling between bond wires.

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Abbreviations

ADS Advanced Design System

BNC Bayonet Neill-Concelman

EDA Electronic Design Automation

IC Integrated Circuit

IEC International Electrotechnical Comission

JEDEC Joint Electron Device Engineering Council

PCB Printed Circuit Board

SMA SubMiniature version A

VNA Vector Network Analyzer

Nomenclature

F Farad

GHz GigaHertz 10^9

Hz Hertz

MHz MegaHertz 10^6

mm millimeter 10^{-3}

Ω Ohm

μm micrometers 10^{-6}

Chapter 1
Introduction

1.1 IC-Circuits and Bonding Wires

An integrated circuit, or IC, is a small commonplace chip that can be used in many different applications. Many IC's are used as amplifiers, timers or even computer memory depending on their purpose and type. When manufacturing integrated circuits there is a process known as bonding, where the chip is connected to its packaging using thin wires usually consisting of metals such as gold, silver, copper or aluminum. This process is considered cost-effective in forming connections between the circuit and its surrounding inputs and outputs[6]. One problem that arises from the use of bond wires for connecting chips and casings is interference. When current is routed through bond wires surrounding the chip, magnetic fields surrounding the wires are formed. Subsequently it is possible that there could be measurable magnetic coupling between different wires and as such some interference can be experienced. Whether or not this interference is significant will be discussed throughout this thesis. This interference may manifest itself as induced voltage or crosstalk between wires. Higher frequencies serve to worsen the problem as inductive coupling becomes a markedly more obvious phenomenon. As frequencies in circuits are becoming higher and higher in different applications, integrated circuits become more susceptible to the problem of inductive coupling between bonding wires. A better understanding of how the phenomenon of induction creates interference at different frequencies is needed. This would serve to create better IC's in the future that function better at high frequencies with inductive interference having less of an effect on the performance of the chip.

1.2 Questions and Objectives

There are many different questions that can be asked in relation to the different properties of bond wires. We chose to focus the research based on a number of questions that we believe are the most important questions that can be asked to cover the topic.

- How is it possible to measure the inductive coupling between bond wires?
- What causes coupling to occur when a bond wire is used to connect an integrated circuit and its casing?

- How is the interference characterized?
- Is it possible to limit the effect of the interference?
- What methods can be effective in reducing the impact of interference?
- How is the forward transmission effected by the coupling at higher frequencies?
- Is the interference significant?
- How does the bonding process for integrated circuits work?

In order for us to be able to adequately answer these questions in a satisfactory way we had devised a number of goals that aimed to give us insight into the problems at hand. These goals would give us a number of tasks in which we would investigate the problem further. The tasks were as follows:

1. Literature study of articles, papers and books covering the subject
2. Design and manufacture a prototype board suitable for bond wire testing
3. Conduct tests and measurements
4. Compare theoretical results to practical results
5. Create a representative model of bond wires for simulation
6. Simulate the aforementioned model
7. Compare practical data to simulated data
8. Investigate coupling limitation measures
9. Discuss and analyze results

1.3 Main Challenges

In researching the stated problems there are a number of problems and challenges to overcome in reaching a satisfactory conclusion:

- Designing a model that is reasonably accurate and thus suitable for simulation and comparisons with measurements in practice is a challenge given the complexity of different electromagnetic phenomenons. Adjustments to the model will have to be made to suit the designs of the PCB's.
- Given the scale of the bond wires, suitably conducting measurements on the testing prototype will be a challenge. Phenomenons such as capacitive coupling and unrelated interference may prove to be a problem.
- Given the limited timeframe available for us, making a suitable design for testing will be a challenge. This is emphasized especially considering the time required in designing and manufacturing testing prototypes. Several iterations may be necessary.

1.4 Limitations

This thesis is limited to only simulate and test the inductive coupling between the bond wires on a circuit and not bond wires connecting a case and a circuit. The types of bond-wires investigated in this thesis are limited to aluminum type bond wires with a diameter of 18 μm. This is due to the fact that aluminum bond wires are the ones available for us to use. The effect of wire diameter and type of material is discussed in theory however. Frequency ranges which are investigated in this thesis have an upper limit of 4 GHz due to the testing equipment and instruments available.

1.5 Structure

This thesis consists of 7 chapters including this introductory one. The second chapter gives the background and motivation for the subject of the thesis. Mainly this includes the induction problem associated with high-frequency signals traversing bond wires and common methods of reducing interference and coupling. Chapter 3 details the relevant underlying theory and concepts of electromagnetism and the associated laws. Further, the measurements for both simulations and practical testing are explained and motivated. Presented in Chapter 4 are results yielded by the measurements and simulations, and a detailed presentation of the measurement setup. The details of both the simulations and testing in practice are given. Results, theoretical and practical, are discussed and analyzed in Chapter 5. Main topics of discussion here include whether or not the coupling limitation efforts have been successful and how the spacing of the bond wires affects the coupling. Simulated results are also compared to practical results here, and different motivations are given for the discrepancies. Chapter 6 serves to reiterate the original goals given in section 1.2 and summarize the findings relative to the problem statements. Finally, Chapter 7 gives some challenges encountered during this thesis that may be the base on which to conduct further research projects in the future.

1.6 Software used in this Thesis

1.6.1 Autodesk Eagle

Autodesk Eagle is an Electronic Design Automation, or EDA, software suitable for creating designs and schematics for PCB's[12]. Eagle was used in this thesis to make designs and generate files to enable the manufacturing of the PCB's used in measurements. The software also made examining the dimensions and layout of different design proposals possible in order to ensure satisfactory measurement results.

1.6.2 Mathworks Matlab

Matlab is a multi-purpose program that can be used for data processing and calculations[23]. Matlab was used in this thesis for the purpose of processing the

measurement data acquired during the course of the project consisting of measures of, among other things, S-parameters and capacitive coupling. Plots and graphs were generated in this program allowing for visualization of the data and also a comparison of the performance of the different PCB's.

1.6.3 Keysight Agilent ADS

Agilent ADS is a design automation software used in this thesis to represent the prototype PCB's in a simulated environment and thus allowing for further comparisons and contrasts between practical and theoretical results[22]. ADS is a software appropriate for simulations of inductive coupling and different loss-parameters in the RF-spectrum.

1.6.4 draw.io

The figures and illustrations in this thesis were made by us using the online-tool draw.io[1].

Chapter 2
Background

2.1 Integrated Circuits

According to the standardization body JEDEC, and integrated circuit is defined as:

> A circuit in which all or some of the circuit elements are inseparably associated and electrically interconnected so that it is considered to be indivisible for the purposes of construction and commerce.
> (Ref. IEC 748-1.)[13]

Integrated circuits commonly consist of circuit components such as resistors capacitors and transistors on a semiconductor wafer, such as silicone. This method of constructing circuits has seen wide usage since the first integrated circuit was conceived by Jack Kilby in 1958[15]. The main advantages of this process compared to the process of using discrete electronic components in creating circuits is the cost-effectiveness and efficiency in comparison to conventional discrete circuits. In general, integrated circuits feature a much more compact design and speed several magnitudes greater and as such are a preferable alternative. IC's have thus seen wide-spread use on a large scale in applications such as computers, phones and many other appliances. The versatile nature of IC's mean they can function as, for instance, amplifiers, oscillators, or timers[26]. One important application for integrated circuits is applying the circuits as microprocessors, where the function of a central processing unit is applied to an IC. The development of integrated circuits has been continuously ongoing since the IC gained wide-spread attention in the 1960's. Both transistor and logic-gate counts have increased considerably with integrated circuits proceeding through a number of generations[2]. The first generation of IC's are denoted as the SSI-generation, while the current generation following a number of successors is the ULSI, or ultra-large-scale-integration generation, reflecting the increased efficiency and complexity of the chips produced. As such, the IC's in use today are considerably more powerful and suited to more performance-dependant tasks. Table 2.1 lists the generations of integrated circuits since 1964 and the corresponding transistor-counts.

Table 2.1: IC generations

Generation	Year	Transistor-count
SSI	1964	1-10
MSI	1968	10 - 500
LSI	1971	500 - 20 000
VLSI	1980	20 000 to 1 000 000
ULSI	1984	>1 000 000

The ever-increasing density of transistors in IC's means the scale of which the components are built at is steadily decreasing. This adds to the challenge of designing the architecture of chips in such a way that the compact layout does not have an adverse effect on performance. Compact size circuits mean that there is less space between incoming connections to ports on the chip.

2.2 Wire Bonds

In order for integrated circuits to easily be integrated or applied in different applications, IC's are often encased in a casing which is often referred to as a "package". In order to form input- and output-connections from the circuit to the pins present on the package, wire bonds are formed between pins in the casing and certain points in the circuit. Wire bonds are also a general method for connecting IC's to external copper lines, even when no package is present. There are a number of advantages to the process of wire bonding compared to other methods[7]:

- Low process temperature
- High level of dependability
- Saves space
- High degree of design flexibility
- Ideal repair option
- Versatile substrate-component combination
- Simplification of complex circuits

Low cost is also a significant advantage of wire bonding, often making it the most cost-effective option[6]. If drawbacks such as the inductive coupling between wires could be better understood and solutions for limiting it could be found, it would make it possible for IC's to function better at higher frequencies. Wire bonds that have commonly consisted of gold are also being replaced with copper bonds due to reasons related to cost and material availability[7]. Aluminum, a material less commonly used in wire bonds, is the material of choice for practical testing in this thesis. The conductance of a material plays a role in the efficiency of

Table 2.2: Properties of common bond wire materials

Material	Specific Resistance ρ,10^{-6} Ω	Specific Conductance K, 10^6 S/m
Silver	0.016	62
Copper	0.018	56
Gold	0.022	44
Aluminum	0.028	36

a bond wire[4]. Conductance and specific resistance values for different materials are shown in table 2.2. While copper has a higher specific conductance than gold, the physical properties of the material, for instance hardness, have historically made it somewhat unsuitable for use in wire bonds. Recently however, due to reasons of cost and availability, the use of copper in wire-bonding has increased.

The wire-bonding process for gold and aluminum differs slightly. This process also depends on the machine and equipment used in creating an IC. Gold bond wires require high temperatures of up to 120 degrees Celsius in the substrate. The bond pads which the wires are fused to also cannot have any unevenness or contamination as it would compromise the connection between wire and pad. In contrast with aluminum, wires made out of gold make for a faster process but also cost more. Aluminum is connected using a process using a certain amount of pressure and are thus friction welded. This is caused by ultrasonic oscillations in the material fusing it to the pad. In order to achieve this, a device known as a transducer is used[4].

There are a number of factors that determine the coupling between bond wires through which high-frequency signals are sent. Factors that have been found to impact the inductance significantly are the following [14]:

1. Wire diameter
2. Wire metal
3. Length of wire
4. Frequency of operation
5. Height above the substrate
6. Separation between wires

The main factors investigated in this project are separation between wires and frequency of operation, the reasoning being that these factors can be influenced in practice on a chip in order to mitigate coupling. Practical reasons such as time and resource constraints also play a part in this. In order to adequately assess the impact of frequency, it is believed that frequencies in the RF-band are interesting to investigate. Specifically, the frequency range from 500 MHz to 4 GHz is where the inductive coupling might have an adverse impact on the bond wires in the form

of interference. While higher frequencies will probably have a further impact, we believe 4 GHz is a suitable ceiling for the frequency range in order to note the trends that manifest themselves at RF-Band frequencies. This interference will be modeled as a parasitic inductor in series with a resistor, representing the bond wire and its inductive and resistive properties respectively.

2.3 The impact of Frequency

As previously mentioned, frequency is a factor in the inductive coupling between bond wires. Frequencies used in computers, mobile phones and many other devices are steadily increasing, which emphasizes the need for methods of managing the effects of high clock frequency in circuits. Wireless networks that have previously used the IEEE 802.11 2.4 GHz standard have given way to the use of 5 GHz networks. Networks with frequencies including 60 GHz are also in development and included in the 802.11 set. It is important to consider that for wireless signals of high frequency there may also be physical circuits in the operation of these networks that are affected by higher frequencies. Typical frequency-ranges for different electrical devices are detailed in table 2.3 [19].

Table 2.3: Frequencies of electronic devices

Device	Frequency
Radio transmitters operated in the long wave range	30 kHz - 300 kHz
Welding devices *H*	<500kHz
Electrosurgery systems *W*	300 kHz
clinical MRI devices	63 MHz
Mobile telephony: GSM 900	900 MHz
Mobile telephony: GSM 1800	1800 MHz
Mobile telephony: UMTS 2100	2100 MHz
Anti-theft devices	10 Hz - 5 GHz

2.4 The Induction Phenomenon

A current through a wire leads to a magnetic field circulating the conductor being created. As such, interference is induced in surrounding wires creating adjacent magnetic fields[10]. With two parallel wires the inductive field of one wire has an effect on the other(Figure 2.1). This phenomenon manifests itself as induced current in each conductor. As illustrated by the figure, this arrangement has the potential to cause interference as a consequence of the opposing magnetic fields caused by the flow of current.

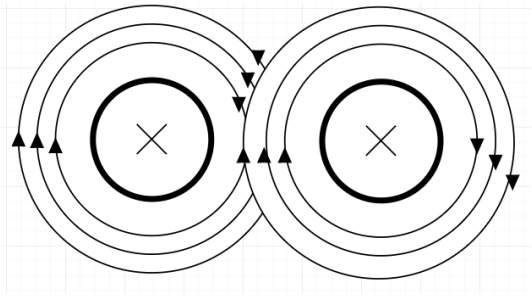

Figure 2.1: An illustration of the magnetic field surrounding adjacent parallel wires in crossection

The voltage $u(t)$ induced in a wire through which current is routed is defined as

$$u(t) = L\frac{di(t)}{dt}. \tag{2.1}$$

Formula 2.1 implies that a higher rate of change in the current $i(t)$ through a wire, or frequency, gives a higher induced voltage. L denotes the inductance of the wire. The self and mutual inductance between two parallel conductors can be calculated using the formulas 2.2 and 2.3[21]. This assumes the wires are straight and are equally long with the same radius. In these formulas l denotes the length of the wires and d denotes the center-to-center distance between the wires. The radius of the conductors is denoted r. Figure 2.2 shows these parameters.

$$L = 2\left(l\log\frac{l+\sqrt{l^2+r^2}}{r} - \sqrt{l^2+r^2} + \frac{l}{4} + r\right) \tag{2.2}$$

$$M = 2\left(l\log\frac{l+\sqrt{l^2+d^2}}{d} - \sqrt{l^2+d^2} + d\right) \tag{2.3}$$

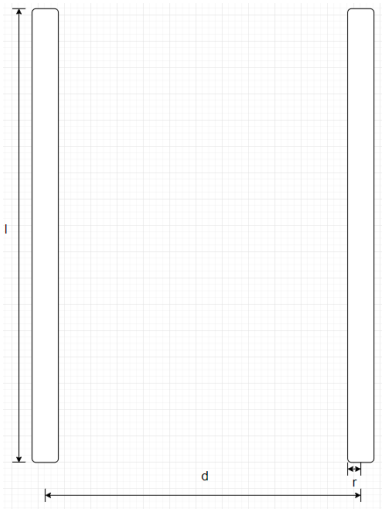

Figure 2.2: Dimensions in formulas 2.2, 2.3

2.5 Limiting the Interference

Interference limitation and mitigation in electronics is an area of research in the field of electronics and as such there are a number of proven methods that aim to limit or reduce interference in different electrical devices[8]. Applying these methods to bond wires is not always possible. In the field of EMC, or Electromagnetic compatibility, the method of shielding cables is a proven way to reduce unwanted interference from electromagnetic emissions[24]. In this method of combating interference a wire is encased in a layer of conductive material on its surface, which is grounded, thus preventing internal signals from leaking and interfering with surrounding components. EMI, or Electro-Magnetic Interference, is absorbed by the casing. This induces current which is then absorbed by the ground connected to the casing. Because of the scale at which bonding wires are operate and the diameter of the wiring used, such a solution is not practically viable in bond wire applications as it would require not only surrounding the bond wire in shielding-material but also grounding the casing. Further adding to the difficulty is the irregular shape of bond wires which result from the bonding process. The scale and manufacturing process of bond wires also makes the use of the twisted-pair method very difficult. In practice this method would reduce emissions thanks to the geometry it introduces. A coaxial-cable, another efficient to shielding wires from interference, would also be a useful solution were it not for the small scale at which IC's operate.

One effective option of reducing the EMI-impact considerably is simply placing a separating wall of conducting material between wires. Grounding this wall would in theory restrict the reach of each wires respective magnetic field and thus limit interference. Bond wires are typically closely spaced together when connecting to a circuit with a large number of connections. This, among other factors, would make this technique impractical. It is possible to create other structures which are

easier to manufacture. A copper pour is one structure that can be placed near bond wires. Connecting the pour to the copper bottom plate of a PCB would create a ground connection. Another attempt to restrict the crosstalk is the bonding of a wire parallel to other bond wires, located in between them. A connection to ground on both ends of the wire is an important part of this method. This is achieved by drilling a connection to the bottom copper plate on the PCB.

Chapter 3
Theory

3.1 The Laws of Induction

3.1.1 Magnetic formulas

In order to describe the phenomenon of electromagnetism a number of fundamental laws are available that serve to describe and characterize magnetic fields[9]. One of the essential formulas used in this field is Faraday's Law, which states that the electro-motive force induced in a loop is equal to the derivative of the flux through a loop. Further, Lenz's law specifies that this current will oppose the change in the flux which caused the induction. The formula for this relation is equation 3.1.

$$\epsilon = -\frac{d\Phi}{dt} \tag{3.1}$$

The magnetic quantity B is surrounding a conductor, in which a current is flowing, is defined according to formula 3.2. Here, $\mu = \mu_r\mu_0$ refers to the permeability of the conducting material and magnetic permeability in vacuum. I is the current flowing through the conductor while r refers to the radial distance from the core of the conductor. Formula 3.2 can be used in deducing the reduction of the field strength of a magnetic field the further the distance is from the conductor core.

$$B = \frac{\mu I}{2\pi r} \tag{3.2}$$

A measure of the magnetic field strength H given the magnetic quantity B is given by formula 3.3.

$$H = \frac{B}{\mu} = \frac{B}{\mu_r\mu_0} \tag{3.3}$$

For two circular straight parallel wires in free space, a measure of the capacitive coupling between the wires is given by formula 3.4[18]. The radii of wire 1 and wire 2 are denoted r_{w1} and r_{w2} respecively. Spacing between the wires is denoted s. It is assumed the wires have an equal length which is denoted l.

$$C = \frac{2\pi l\epsilon_0\epsilon_r}{\cosh\left(\frac{s^2 - r_{w1}^2 - r_{w2}^2}{2r_{w1}r_{w2}}\right)} \tag{3.4}$$

3.1.2 Induction formulas

In general, a bond wire can be represented using a lumped-element model in which the wire has an inductance between the wire and the ground plane. Equations 3.5 and 3.6 give approximate values of the straight-line self and mutual inductance between two straight bond wires and are often used to estimate the inductance between bond wires[16]. This value is based on the length l of the bond wires, the radius r and the center-to-center distance d. The constant μ_0 denotes the permeability of free space.

$$L \simeq \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{r}) - 0.75] \tag{3.5}$$

$$M \simeq \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{d}) - 1 + \frac{d}{l}] \tag{3.6}$$

While M is largely independent of frequency, the impedance of an inductor can be described using Formula 3.7, where Z_L signifies the impedance and M signifies the mutual inductance[20]. Increasing the frequency gives an increased impedance, which is to be taken into account when assessing the results.

$$Z_L = j\omega M \tag{3.7}$$

3.2 Measuring the Inductive Coupling

In order to measure the inductance of bond wires and its impacts a number of considerations are necessary in order to conduct measurements that lead to results with satisfactory accuracy. Measuring the bond wires in practice requires bespoke circuit-boards. This will require designing and manufacturing a purpose-built circuit-boards with which the inductive coupling between bond wires can be measured without excessive external influence. The initial designs of the circuit-boards included two parallel copper microstrip-lines leading to points to which the bond wires would be connected using a bonding-machine (Figure 3.1). This design was later found to be flawed as the coupling of the two adjacent microstrip lines would be considerable and would thus impact the measurements of the bond wires. This problem is especially evident when considering that bond wires require a narrow gap between them for measurable inductive coupling to occur, while the microstrip lines require a considerable margin in between them in order to reduce capcacitive and inductive coupling. The solution was to design a circuit in which the microstrip lines run perpendicular to each other up until the contact points, at which the bond wires are bonded parallel to each other (Figure 3.2). As such, the inductive interference between the lines is minimized while the bond wires, still running parallel to each other, are in close proximity. SMA-contacts are connected to each end of the microstrips which make a connection to a VNA possible. Three different boards with different dimensions are built in order to also investigate the impact of the proximity of the wires. Bond wire spacings of 0.15 mm, 0.325 mm, 0.5 mm were designed. With the grounding mentioned in section 2.5 implemented into the board, there was eight boards in total. This number included two boards that were manufactured for the purpose of evaluating if a grounded copper pour

alone without a wire is sufficient for efficiently limiting interference. Specifications for these two boards are the same as for the 0.5 mm board in Figure 3.1. Table 3.1 also gives the general specifications of the remaining boards and the contact points located of them. A visualization of how the layout looks with a ground wire is shown in Figure 3.3. Formula 3.6 was used to estimate inductance values

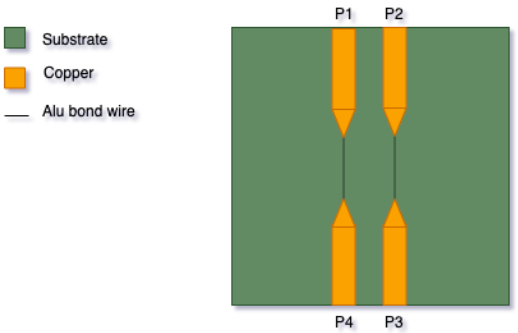

Figure 3.1: Measuring board model with parallel microstrip lines

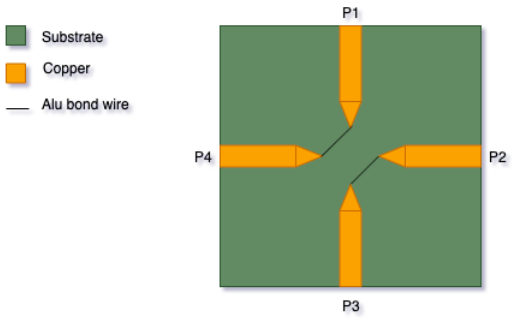

Figure 3.2: Measuring board model with perpendicular microstrip lines

for different spacings, after which the dimensions for the spacing between bond wires were chosen. Table 3.1 shows the general specifications for the boards. The microstrip-line width and height are also defined in this table. Differences between the boards are mainly limited to the spacing between the bond wires and the subsequent adjustments to microstrip placement. Table 3.2 gives the spacing and length of the bond wires of each board as illustrated in Figure 3.4.

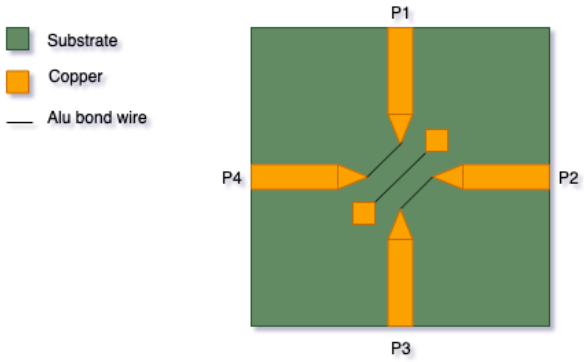

Figure 3.3: A topview picture which explains the two Alu bond wires and the Ground wire between them.

Table 3.1: General Specifications of the measuring boards

Substrate type	FR4
Substrate height H	0.8 mm
Microstrip width W	1.45 mm
Contact type	SMA
Contact width	8.5 mm
Microstrip height	18 μm
Bond wire material	Aluminum
Bond wire diameter	18 μm
Board dimensions	20.5x20.5 mm

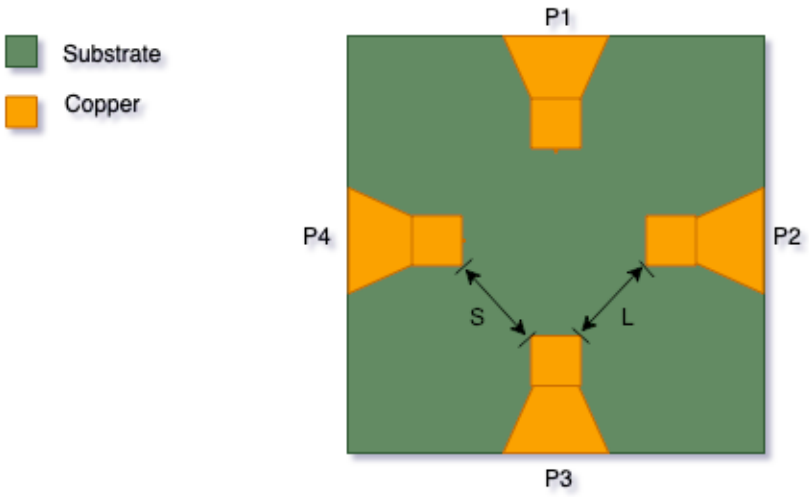

Figure 3.4: Contact point dimensions

Table 3.2: Contact point dimensions of the different circuits

Circuit A	L = Bond wire Length	0.5 mm
	S = Bond wire Spacing	0.5 mm
Circuit B	L = Bond wire Length	0.5 mm
	S = Bond wire Spacing	0.325 mm
Circuit C	L = Bond wire Length	0.5 mm
	S = Bond wire Spacing	0.15 mm

In Figure 3.5 the parameters for the dimensions of the microstrip line are displayed. A substrate height H of 0.8 mm was chosen for the FR4-type laminate. This value was then used along with the copper line width W in Figure 3.5 in order to calculate the characteristic impedance Z_0. In order for the reflection and return loss to be minimal during testing the characteristic impedance of the microstrip line was set to 50 Ω, matching the impedances of the instruments and cables described in Chapter 4. This was achieved by dimensioning the length and width of the copper lines accordingly using formulas 3.8, 3.9, 3.10 and 3.11.

$$If \frac{W}{H} < 1 : \epsilon_{eff} = \frac{\epsilon_R + 1}{2} + \frac{\epsilon_R + 1}{2} \left(\frac{1}{\sqrt{1 + 12\frac{H}{W}}} + 0.04 \left(1 - (\frac{W}{H})^2 \right) \right) \quad (3.8)$$

$$Z_0 = \frac{60}{\sqrt{\epsilon_{eff}}} ln \left(8\frac{H}{W} + 0.25(\frac{H}{W}) \right) \quad (3.9)$$

$$If(\frac{W}{H}) > 1 : \epsilon_e ff = \frac{\epsilon_R + 1}{2} + \left(\frac{\epsilon_R - 1}{2\sqrt{1 + 12(\frac{H}{W})}} \right) \tag{3.10}$$

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_{eff}}\frac{W}{H} + 1.393 + \frac{2}{3}ln(\frac{W}{H} + 1.444)} \tag{3.11}$$

These formulas describe the characteristic impedance of a microstrip line [25][27]. Using the data available in table 3.1, it was deduced that a width of 1.45 mm in the copper line gave a characteristic impedance near 50 Ω on an FR4 substrate with a height of 0.8 mm.

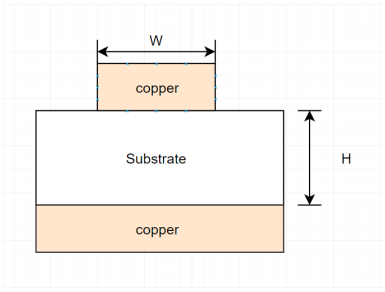

Figure 3.5: Microstrip layout and dimensions

A factor in this calculation is the dielectric constant of the substrate ϵ_r which is 4.7 according to the data sheet available. In practice this constant will probably not be completely consistent throughout the substrate layer of the board. This adds a minor source of error to the measurements, which will be taken into account.

3.3 Measurements in Practice

In the setup for conducting the measurements, the four ports of the measuring boards are designated a number ranging from 1 to 4. Ports 1 and 4 are connected using a bond wire, as are ports 2 and 3. A VNA will be the main instrument used in the measurement. A signal generator will be used in conjunction with a spectrum analyzer in the measurements in order to compare the findings from the VNA. In order to quantify the losses incurred by signals traversing the board, the input signal will be compared with the outgoing signal. It will be possible to conduct measurements at different ports and thus compare and contrast results from different setups. The performance of the circuit can be characterized in terms of both S-parameters and related certain loss terms. S-parameters, or Scattering parameters are measured using power waves and describe the relationship between ports[5]. A two-port network can be described using Formulas 3.14 - 3.15, where out_1 and out_2 describe the outgoing signals at ports 1 and 2 respectively, while in_1 and in_2 describe the ingoing signal at port 1 and 2 respectively[17].

Figure 3.6 gives an illustration of this set-up. Differences between measuring boards will then be analyzed to determine whether or not the grounded wire is effective in reducing the coupling between the wires.

$$out_1 = S_{11}in_1 + S_{12}in_2 \tag{3.12}$$

$$out_2 = S_{21}in_1 + S_{22}in_2 \tag{3.13}$$

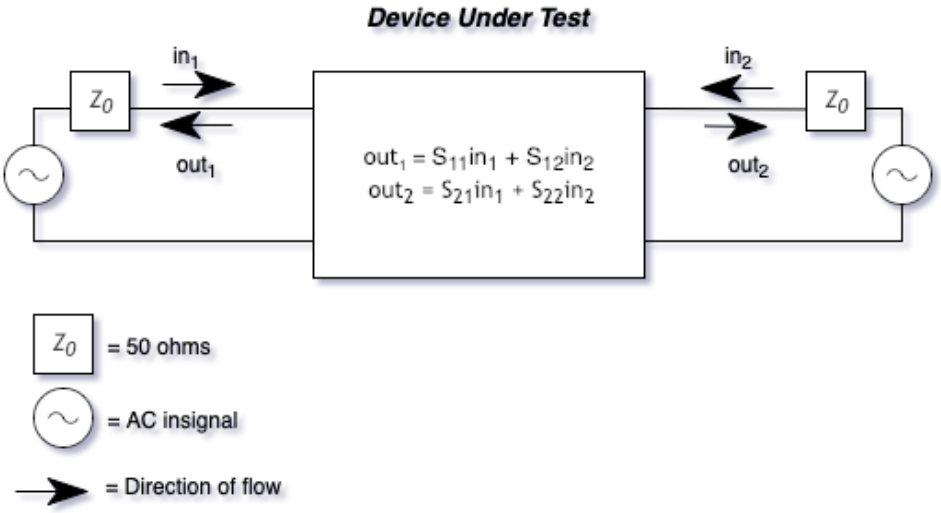

Figure 3.6: An illustration of S-parameters

$$S_{11} = \frac{out_1}{in_1}\Bigg|_{in_2} \tag{3.14}$$

$$S_{21} = \frac{out_2}{in_1}\Bigg|_{in_2} \tag{3.15}$$

$$S_{12} = \frac{out_1}{in_2}\Bigg|_{in_1} \tag{3.16}$$

$$S_{22} = \frac{out_2}{in_2}\Bigg|_{in_1} \tag{3.17}$$

A two-port VNA is used in the measurements, as such there is one outgoing signal at one of the ports of the PCB and a signal being analyzed at another port, also on the PCB. The remaining ports are terminated using 50 Ω terminations on the SMA-connectors, thus preventing reflections from the unused ports. Modelling the circuit yields two distinct parallel paths from port 1 to port 4 and port 2 to port

3 respectively. Generating a signal through one of the paths over a bond wire and listening on the adjacent line will give readings relating to the coupling between the wires. One consideration here is the capacitive coupling between the microstrip lines due to their proximity. Before bond wires are added, the coupling can be measured and taken into consideration when estimating the inductive coupling between the wires. Measurable coupling exists between not only from one line to the adjacent microstrip line but also to some extent to the one in front.

3.4 Simulation of the Bond Wires

Bond wires can be modelled with a lumped-element representation in order to represent electromagnetic properties (Figure 4.2). The representation chosen consists of two inductors and resistors in parallel, representing the inductance and resistance of bond wires respectively. It is important to take the differences between simulations and practical testing into account. In practice there are a number of factors that are not reflected in the lumped-element representation and thus not taken into account in simulation. The impedance of the transmission lines is represented as closely as possible by using both rectangular transmission lines and tapered ones as in the PCB designs. BNC-cables, which are used to connect measuring-equipment to the manufactured measuring boards, are also imperfect in practice. The practical results from the measuring equipment itself are also going to have some inaccuracy due the calibrations on the instruments. As such, differences in simulated and practical results can be partially explained by these factors. There are a number of programs that can be used to simulate bond wires and their electromagnetic properties. Agilent ADS is a simulation software from the company Keysight and is suitable for creating and simulating circuits at frequencies in the RF-band. The software offers the possibility of creating four distinct ports, making it possible to conduct simulations in a manner similar to the practical testing on the measuring boards. As such it should be possible to compare the data and make conclusions based on the contrast between the simulated and practical behavior of the bond wires.

Chapter 4
Methodology and Results

4.1 Bond wire Modelling

Agilent ADS 2012 was the software chosen for the simulations. Using this software, we simulated the three circuits described under section 3.2. Analog to the practical measurements, the goal of the simulation was to obtain S-parameters of the system. This would yield data describing the performance of the circuit and the coupling between the wires in particular. A circuit representing the bond wires was created, as shown in figure 4.1. Ports in the figure are number according to 'Num = n', where n is the port number. Figure 4.2 gives the full picture including the signal parameters. Measurements between port 1 and 4 represent a signal traversing the network, meaning measurements between port 1 and 3 are used to read crosstalk between the two wires. The frequencies investigated were the range from 500 MHz to 4 GHz as in the practical measurements.

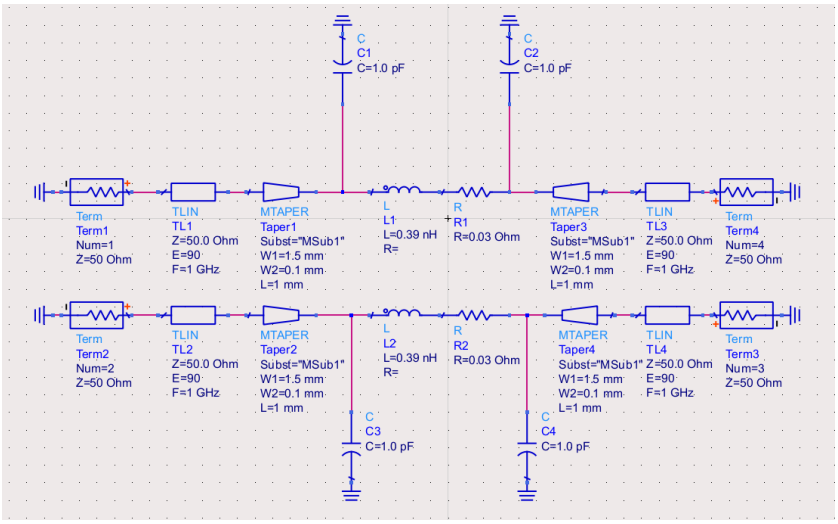

Figure 4.1: The circuit used in simulations

The aim of the simulation was to represent the physical measuring boards and thus mirror the measurements to some extent in a simulated environment. In figure 4.1 it is seen how the bond wires are represented using an inductor and a resistor in series. Represented by the capacitors on either side of the bond wire is the capacitance to the ground. Transmission lines are present after each of the four ports and act as the microstrip lines which are present on the physical board. The transmission lines are of the tapered kind, much like the physical ones. Finally, the simulation has parameters for the mutual coupling K and the mutual inductance M. M was estimated using analytical formulas described under section 3.1.2. Using an M-value overrides the K-value, meaning it is not used. As the three different types of circuits have three different spacing measurements of 0.15 mm, 0.325 mm and 0.5 mm, the parameters were calculated and adjusted accordingly using formula 3.6. As the center-to-center spacing decreases, M increases. Parameters related to the properties of the substrate, described under section 3.2, used in the measurement circuits were specified under 'MSub' (Figure 4.2).

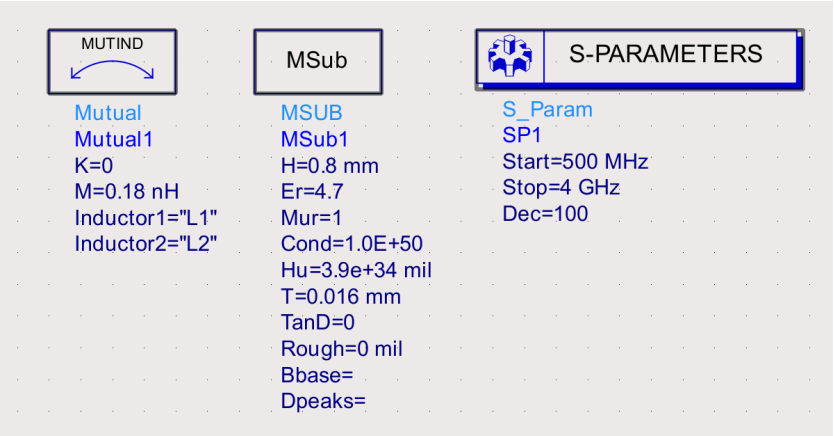

Figure 4.2: Simulation parameters for the simulation. The M parameter changed depending on the bond wire spacing.

4.2 Simulation Results

Figures 4.3 and 4.4 show the results from the simulations. The parameters shown are the amplitudes of the S_{41} parameter, describing the transmission across a bond wire, and the S_{31} parameter, showing the crosstalk between the bond wires. A logarithmic scale is used to display the signal strength in decibels. Simulations were conducted for a spacing between the bond wires of 0.5 mm, 0.325 mm, and 0.15 mm.

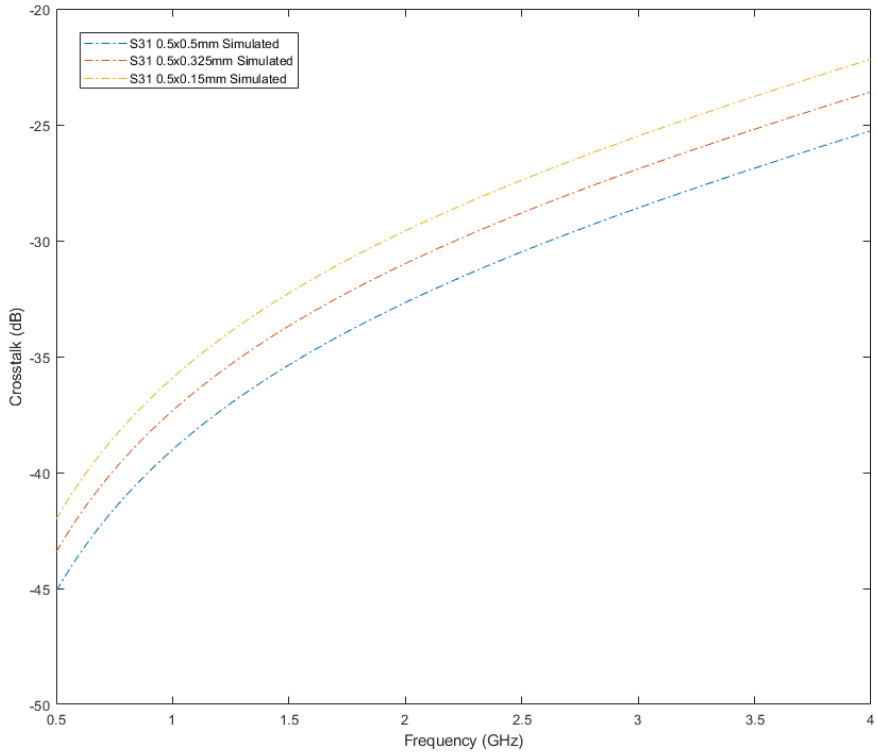

Figure 4.3: S_{31} (Crosstalk)Parameters for 0.5 mm, 0.325 mm, and 0.15 mm spacing

Figure 4.3 shows the simulated crosstalk for a spacing of 0.5 mm, 0.325 mm, and 0.15 mm. The yellow dashed line, representing a spacing of 0.15 mm, shows the highest level of crosstalk with a maximum of -24.168 dB. The blue dashed line represents the 0.5 mm spacing, which shows consistently lower crosstalk levels than the other spacings across the spectrum with a maximum of -27.264 dB. In between the values for the 0.5 mm and 0.15 mm spacings are the values for the 0.325 mm spacing with a maximum crosstalk level of -25.083 dB. Figure 4.4 meanwhile shows the transmission attenuation. The three different spacings of 0.5 mm, 0.325 mm and 0.15 mm are represented by yellow points, blue circles, and a dashed red line respectively. The differences between the plotted values are small, with a negligible difference at 500 MHz and a maximum difference of 0.002 dB at 4 GHz between 0.15 mm and 0.5 mm.

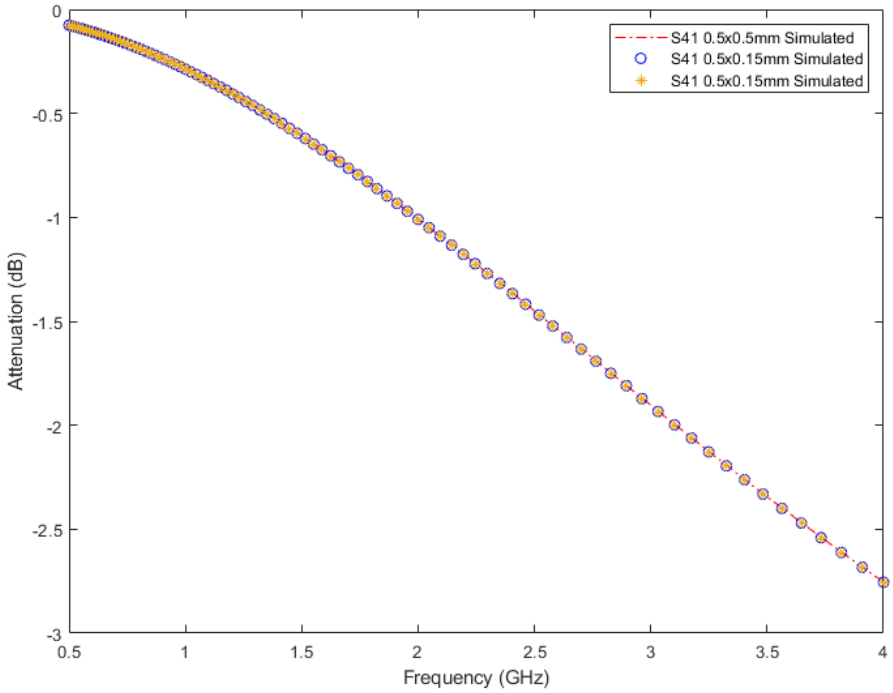

Figure 4.4: S_{41} Parameters(Attenuation) for for 0.5 mm, 0.325 mm, and 0.15 mm spacing. The differences between the plotted values are small.

4.3 Measurement Setup

The Vector Network Analyzer used to conduct these measurements was a Rohde & Schwarz with a frequency range from 9 kHz to 4 GHz. A BNC-type cable was used in conjuction with adapters in order to create a connection between the SMA-type connectors on the four different ports on the circuit and the BNC-connectors on the VNA. BNC-cables with a length of 0.5 m and an impedance rating of 50 Ω were used between the circuit and the instruments. Ports on the instruments also had a matching impedance rating of 50 Ω. Any ports without incoming or outgoing connections had 50 Ω terminations on them for the purpose reducing reflections. A signal generator of the same make as the VNA, Rohde & Schwarz, with a signal range from 5 kHz to 3 GHz was used to confirm the readings from the VNA with a similar measurement setup. An Advantest R1313 Spectrum Analyzer was used to read the signals generated. Comparisons showed only minor differences and confirmed the accuracy of the VNA. Before bond wires were bonded on the PCB's, measurements were conducted on the VNA in order to measure the coupling between the microstrips. This coupling is mainly due to

capacitive and inductive coupling between the microstrip transmission lines and is also frequency dependent. The ports on the measurement boards are shown graphically in figure 4.5.

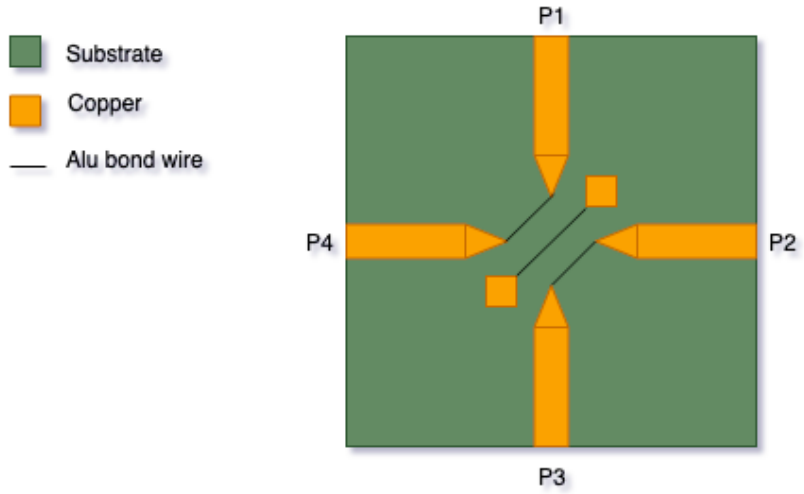

Figure 4.5: Measuring board ports

Figure 4.6 shows the manufactured PCB's. The two circuits labeled 'v.1.' were the circuits with a grounded point in the center. These were the first to be measured, with coupling limitation measures that were later found to be ineffective(Figure 4.8). This is due to the negligible difference found between the crosstalk levels in the PCB with the ground point and the PCB without a ground point arrangement. This suggested the ground point has little effect on crosstalk. The results of these are not included. Remaining PCB's, half of which include the ground wire arrangement(Figure 4.7) are labeled 'v.2.'. Figure 4.7 shows a close-up of the ground wire arrangement.

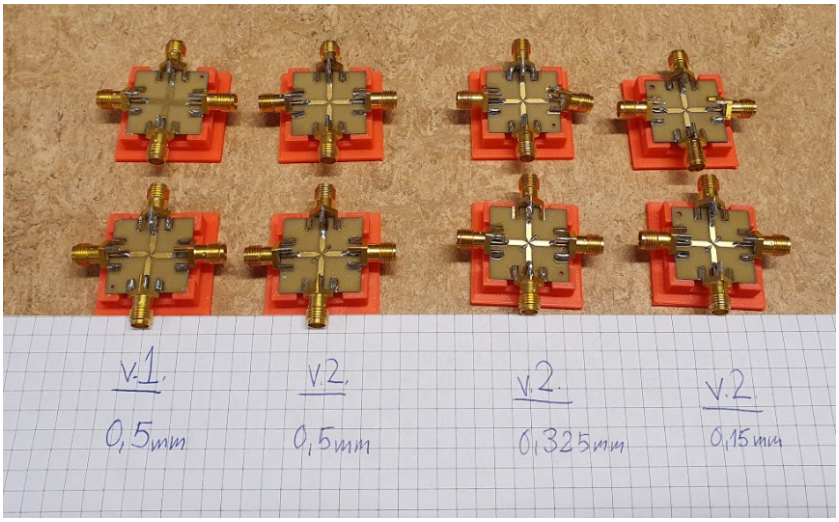

Figure 4.6: Testing PCB's with specified spacings of bond wires. PCB's that have a corresponding PCB with a ground point arrangement are labeled 'v.1.' and circuits that have a corresponding center wire arrangement are labeled 'v.2.'.

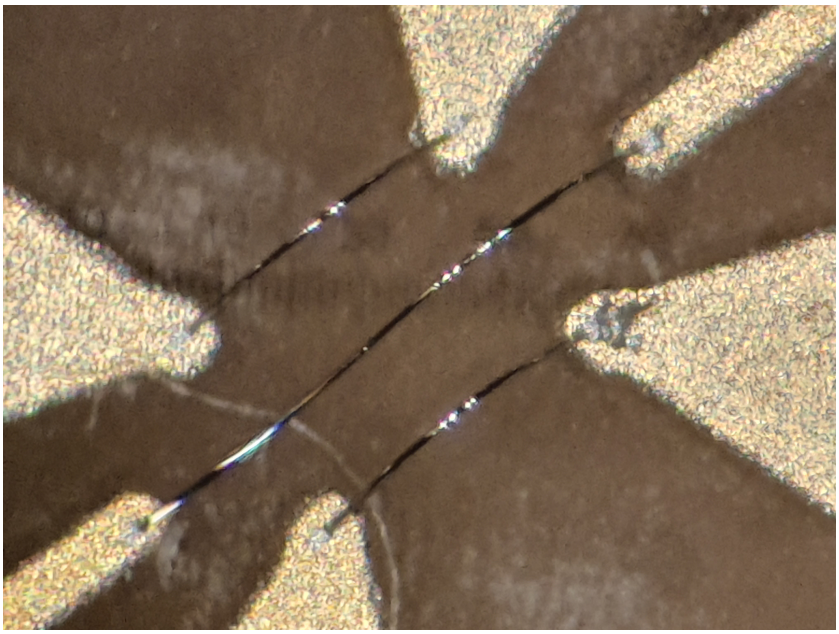

Figure 4.7: Ground wire arrangement on a PCB (Center)

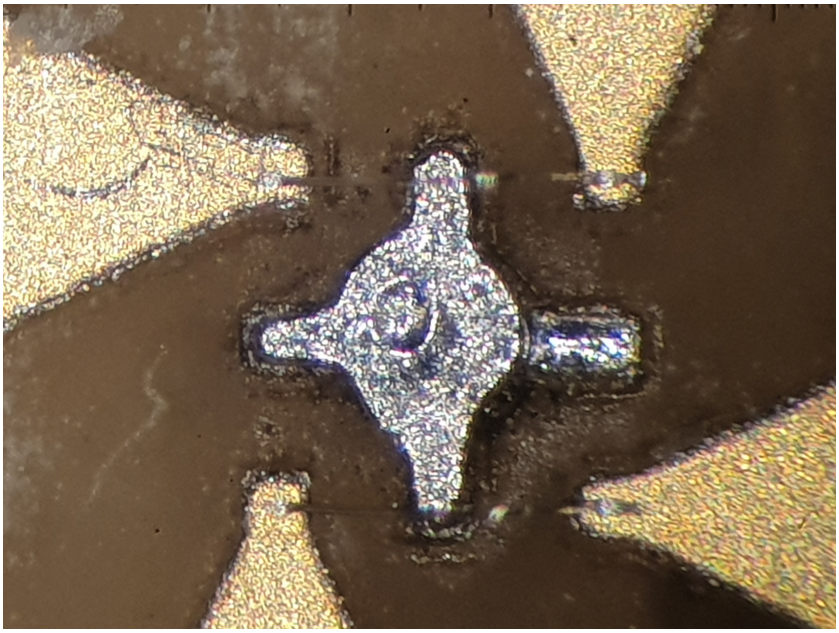

Figure 4.8: Ground point arrangement

4.4 Measurement Results

Following are the measurements of the parameters S_{41}, which shows the transmission across the bond wires, and S_{31}, showing the crosstalk between the bond wires read on port 3. Signals were sent from port 1. The values presented in this section were the raw data read from the VNA during measurements and were plotted using Matlab. Coupling on different PCB's before bond wires were added, are also presented.

4.4.1 Transmission Line Coupling

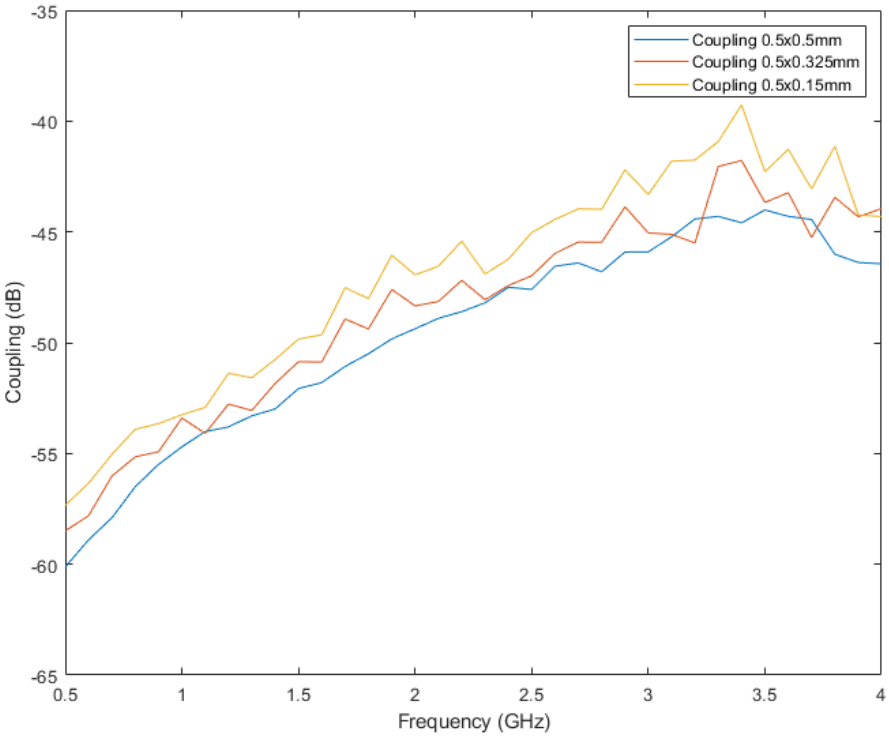

Figure 4.9: Coupling between transmission lines for circuits without center ground wires (No Bond Wires)

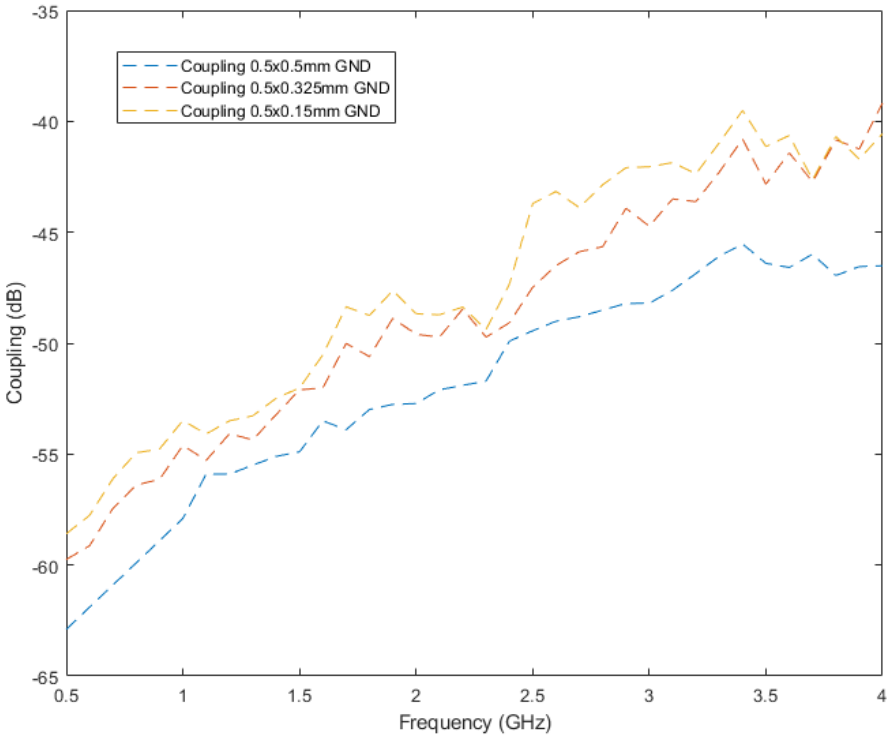

Figure 4.10: Coupling between transmission lines for circuits with center ground wires (No Bond Wires)

Figure 4.9 and 4.10 show the crosstalk measured on port 3 with signals sent on port 1(Figure 4.5). The crosstalk shown on these graphs give measures of the coupling without bond wires. Trends here indicate that the closer the spacing is, the higher the level of crosstalk is experienced across the frequency range from 500 MHz to 4 GHz. The yellow lines represent the results for the 0.15 mm spacing, while red and blue represents the 0.325 mm and 0.5 mm spacing respectively. Solid lines represent measurements on circuits without a center wire and dashed lines represent measurements on circuits with a center wire arrangement. The graphs also show an increase across the spectrum from 500 MHz to 4 GHz.

4.4.2 Crosstalk

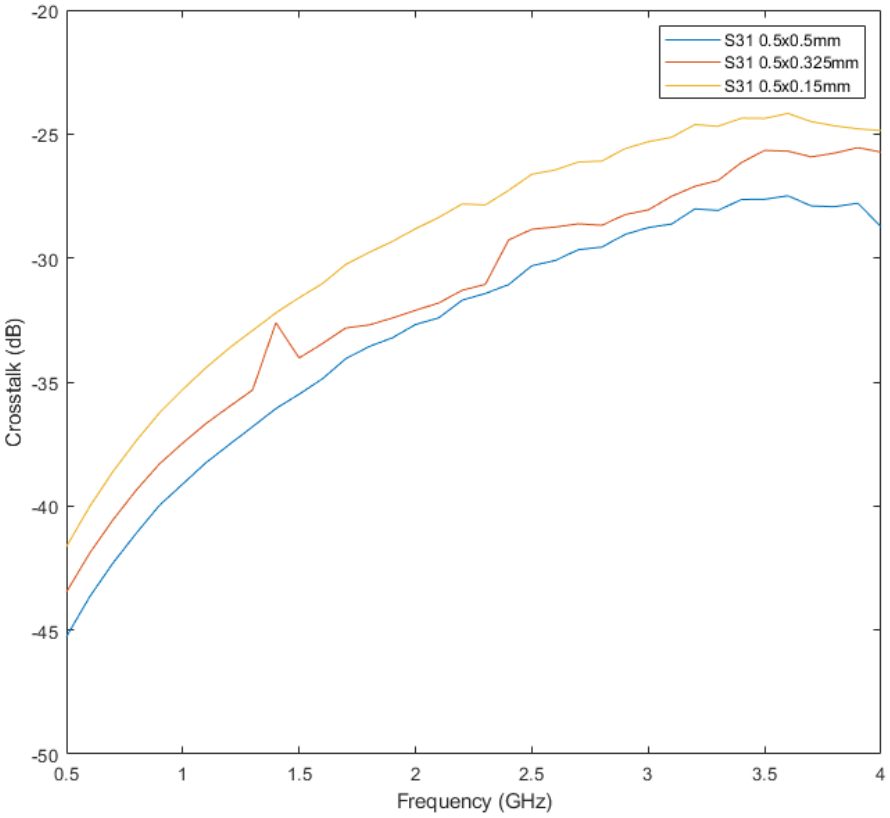

Figure 4.11: S_{31} Parameter(Crosstalk) for 0.5 mm spacing, 0.325 mm, and 0.15 mm spacings with and without the center ground wire

Figure 4.11 shows the values obtained during measurements for crosstalk between ports 3 and 1(Figure 4.5). Measurements conducted on PCB's with bond wires on the boards. The crosstalk experienced here greater than values obtained without bond wires (Figures 4.9, 4.10) as the coupling between the bond wires increases the crosstalk levels. Figure 4.12 allows for a comparison between crosstalk levels on PCB's with center wire arrangements, shown with dashed lines, and those without, shown with solid lines. What is evident from 4.12 is the consistently lower crosstalk levels on the PCB's with center grounded wire arrangements.

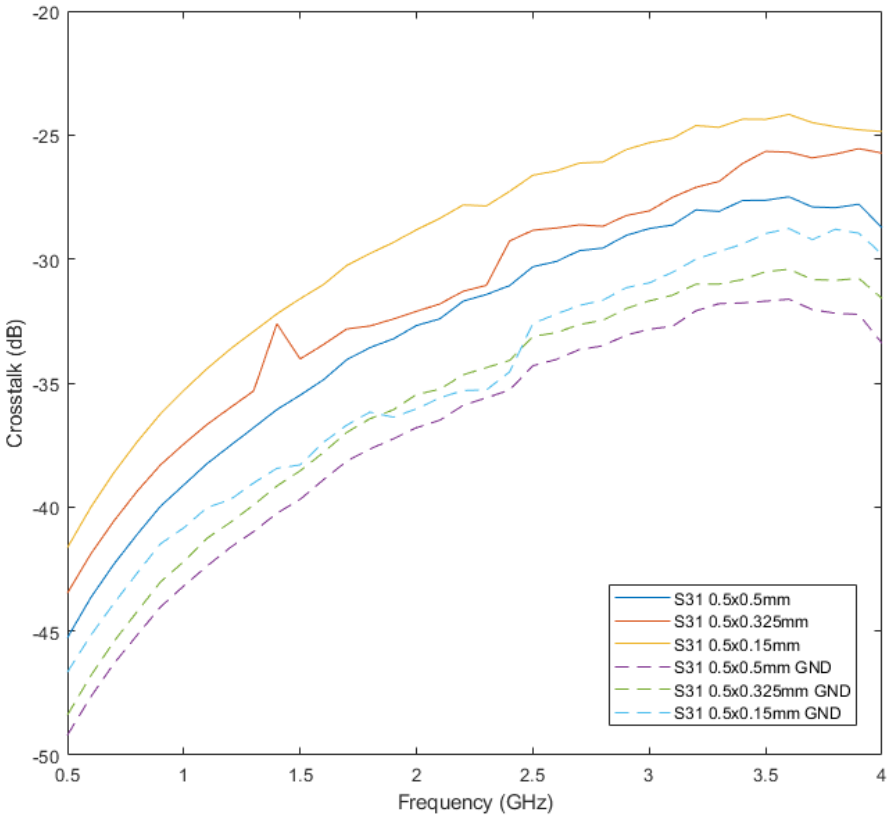

Figure 4.12: S_{31} parameters for circuits with and without center ground wires, with ground wire circuits shown with dashed lines

4.4.3 Forward Transmission and Attenuation

Figure 4.13 shows the attenuation of the signal sent from port 1, read on port 4. Attenuation for both PCB's with center grounded wires and without are shown. Differences between the results are small, leading to some overlap between the results.

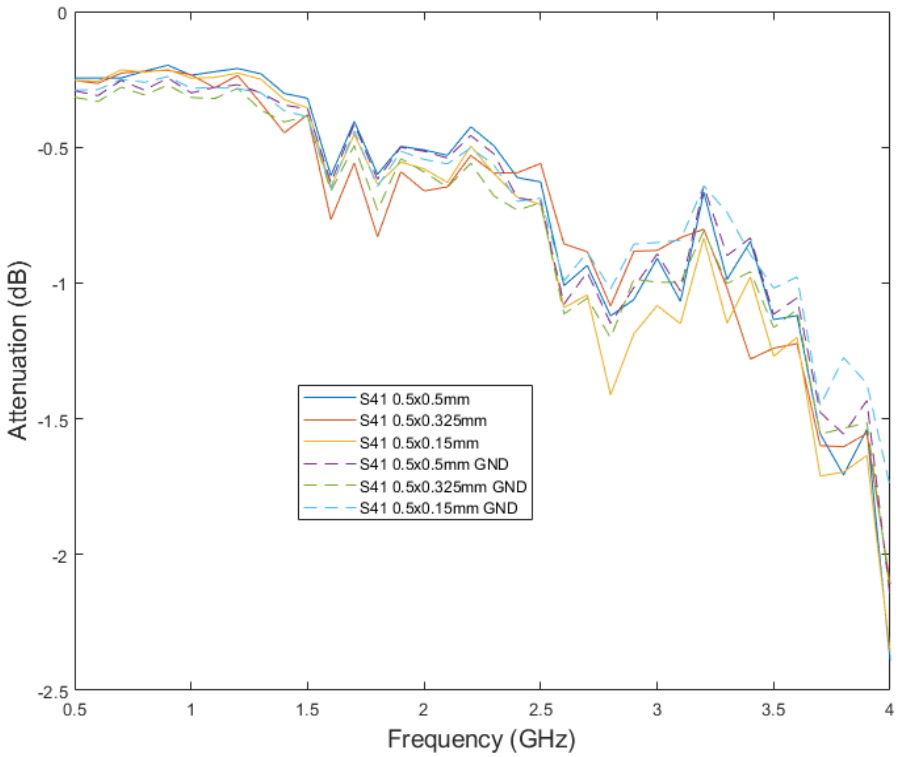

Figure 4.13: S_{41} parameter (Attenuation) with and without center ground wires, with ground wire circuits shown with dashed lines

Chapter 5
Discussion and Analysis

The results presented in Chapter 4 give some interesting insight to the properties of the measurement PCB's versus the simulated representations. There is however the question of what these results represent and what conclusions can be drawn from them.

5.1 Sources of Error

There were a number of factors that most likely impacted the readings to some extent during measurements. Couplings between the microstrip transmission lines on the PCB's manufactured have been taken into consideration. Measurements without bond wires have given some estimations. Capacitive coupling between the bond wires also exists to some extent, and is more difficult to measure. This phenomenon is discussed in section 5.4

Then there is also the question of the accuracy of the equipment and PCB's used in this thesis. Initially it can be stated that the VNA's, Signal Generators and Spectrum analyzers available to us most likely had some calibration errors. The setup that was used with SMA-contacts and the appropriate adapters causes some reflections to occur, affecting measurements. One additional source of inaccuracy is the fact that it is not possible to perfectly manufacture a PCB to specification. As such there is probably some difference in comparison with the templates. The bond pads on the PCB's are meant to serve as a surface to which the bond wire can attach. In the design process the spacing and length of the bond wires were take into consideration and the bond pads placed accordingly. In practice, it is difficult in the bonding process to perfectly match the length and spacing of the wires perfectly to the specified dimensions. Examining the circuits under a microscope revealed minor deviations to specification. The differences are found to be within an acceptable margin.

5.2 Simulations and Measurements

As seen in graph 5.1 and 5.2, there are some differences between simulated values and measured values. Simulated S-parameters show results that can be expected in an ideal environment. The three different crosstalk parameters, or $|S_{31}|$-parameters, show a constantly increasing level of crosstalk from 500 MHz to 4GHz

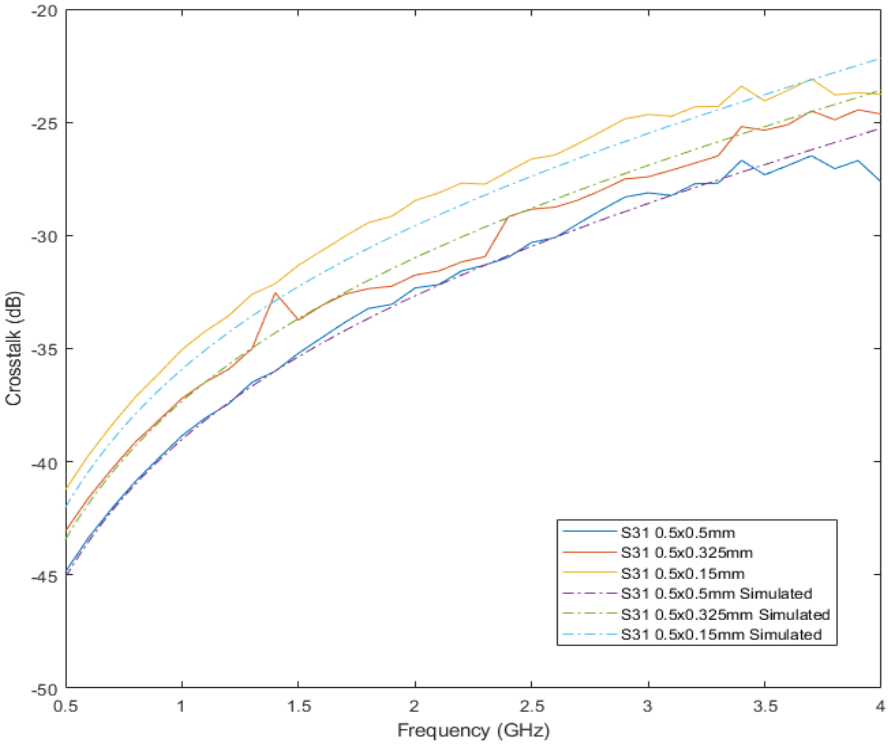

Figure 5.1: Comparison between simulated and actual crosstalk

(Figure 4.9). Taking the values from the 0.5 mm chip as an example, the crosstalk starts at -44.86 dB of the input signal at 500 MHz. It then shows an increase to -27.65 dB at the end of the spectrum at 4 GHz. Thus, the proportion of the signal leaking over to the adjacent wire compared to the input increases from 0.57% to 4.14%. These values are calculated using formulas 3.14 to 3.17. The maximum coupling measured was -24.45 dB @ 3.5 GHz, which corresponds to 4.7% of signal voltage leaking over to the adjacent wire. Similar trends can be seen for the 0.325 mm chip and the 0.15 mm chip. The coupling is even more apparent for the 0.15 mm chip, as the maximum level measured was -23.08 dB @ 3.6 GHz. This corresponds to 7.0% of the input signal leaking over. What is interesting here is the increase in coupling as the spacing between the wires decreases. The 0.325 mm circuit confirms this trend with a maximum measured coupling of -24.45 dB @ 3.9 GHz, or 6.0% signal leakage.

Comparing the simulations to the practical PCB measurements reveals some interesting facts. Figure 5.1 shows the simulations of crosstalk compared to the actual $|S_{31}|$ parameters. The circuits with a center ground wire are also included in Figure 5.2. Figure 5.1 shows that there is a good accordance between the simulated

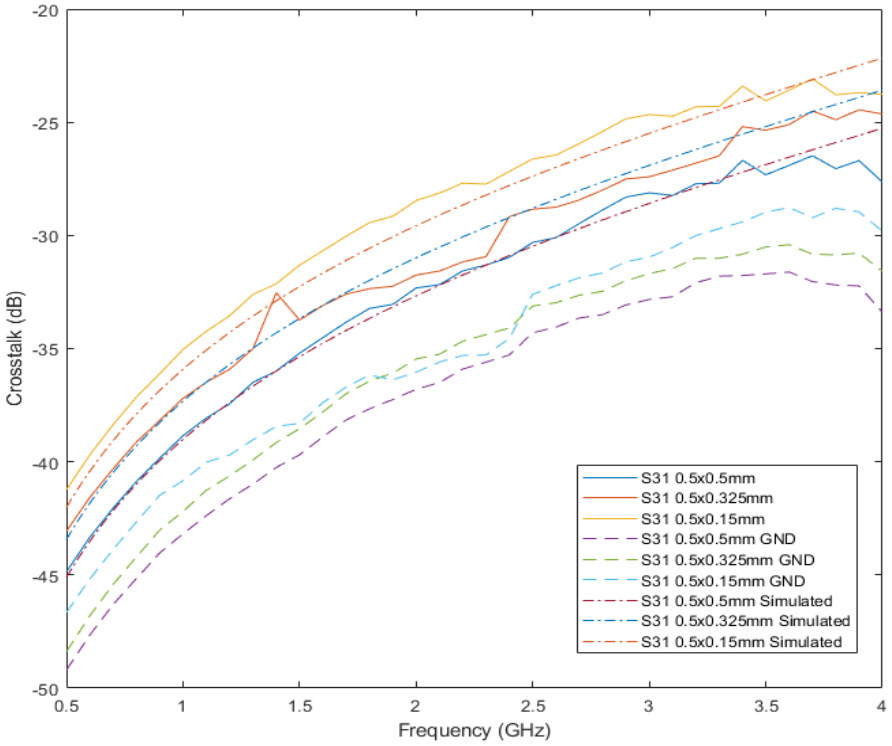

Figure 5.2: Comparison between simulated and actual crosstalk, with center ground wire crosstalk included

and actual $|S_{31}|$ parameters for all three tested PCB's. Simulation parameters were adjusted from the mutual inductance values calculated using formula 3.6 to fit the measurements. Resulting inductance values between the bond wires were found to be higher than the theoretical values calculated, as shown in table 5.1. The difference can be explained partly by the factors described under section 5.2, but also by the straight-line approximations made by the formula. In practice, the height and shape of the bond wire affect the mutual inductance between bond wires[14].

5.3 Have the decoupling efforts been successful?

In Chapter 4, the $|S_{31}|$ parameters for the measured PCB's have been presented. For each circuit there has been a corresponding design manufactured with a grounded wire, with appropriate bond pads, routed parallel in between the signal bond wires (Figure 3.3). Results of the crosstalk measurements reveal some interesting results. Across all three circuits manufactured, with wire spacings of

Table 5.1: Theoretical mutual inductance M values (Formula 3.6) and measured M values

Spacing	Theoretical M (nH)	Actual M (nH)	$\Delta(nH)$	Difference (nH)
0.5 mm	0.0693	0.11	0.0583	58.7%
0.325 mm	0.0741	0.14	0.0601	88.9%
0.15 mm	0.1197	0.18	0.0603	50.7 %

0.15 mm, 0.325 mm and 0.5 mm, the ground wire arrangement shows a decrease of coupling across the frequency spectrum. Circuits with the center ground wire arrangement show consistently lower coupling values than circuits without. Table 5.2 gives the difference in terms of the average coupling across the spectrum.

Examining tables 5.2 leads to the conclusion that putting a grounded wire in

Table 5.2: Mean crosstalk levels (No GND/GND)

Spacing	Mean $\|S_{31}\|$ No GND (dB)	Mean $\|S_{31}\|$ GND (dB)	$\Delta(dB)$
0.5 mm	-32.59	-37.09	4.50
0.325 mm	-31.15	-35.96	4.82
0.15 mm	-28.96	-35.11	6.16

between closely spaced bond wires does indeed seem to reduce the coupling. The coupling is reduced considerably at 0.5 mm with an even more drastic reduction at 0.325 mm. The 0.15 mm circuit continues this trend with an average 6.16 dB reduction across the spectrum, a considerable difference. Further, circuits with the ground wire arrangement show a higher degree of coupling limitation the closer the spacing. There is the question of how the coupling of the transmission lines have any significant impact on the results. Coupling between the transmission lines is affected by the ground wire arrangement. Figures 5.3, 5.4 and 5.5 show coupling as a ratio between the coupling measured with bond wires and without bond wires. In other words, the graphs express how much the crosstalk increases from adding bond wires. Formula 5.1 thus expresses the increased crosstalk with bond wires in comparison to the capacitive and inductive coupling without bond wires. $|S_{31lines}|$ denotes the signal amplitude without bond wires, $|S_{31wires}|$ denotes the signal amplitude with bond wires. Thus the graphs take into account the coupling differences between the circuits with a center ground wire and those without before bond wires are added.

$$Crosstalk\_Gain = \frac{|S_{31wires}|}{|S_{31lines}|} \tag{5.1}$$

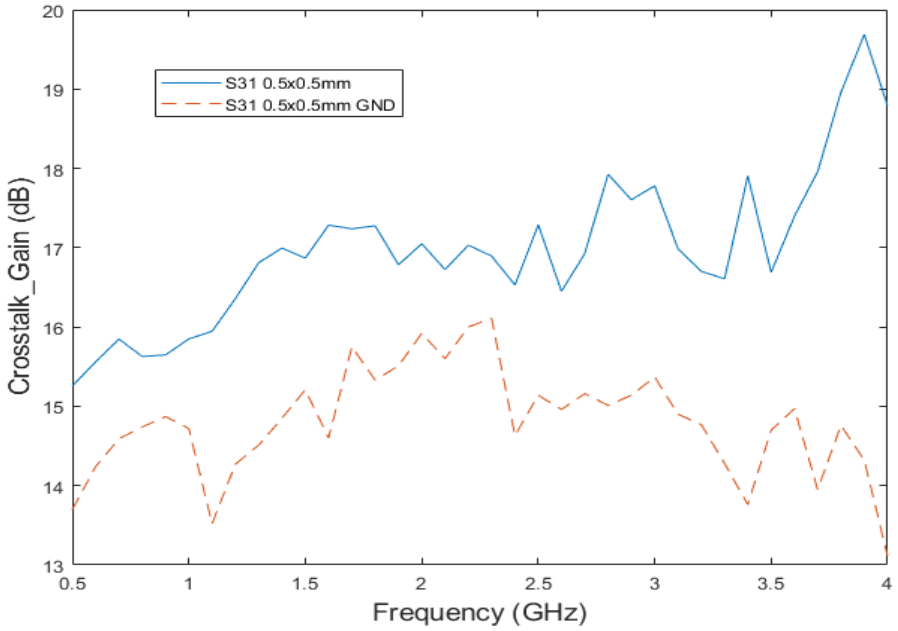

Figure 5.3: Increased crosstalk with bond wires compared to without bond wires for 0.5 mm spacing. Results include PCB's with and without the center ground wire.

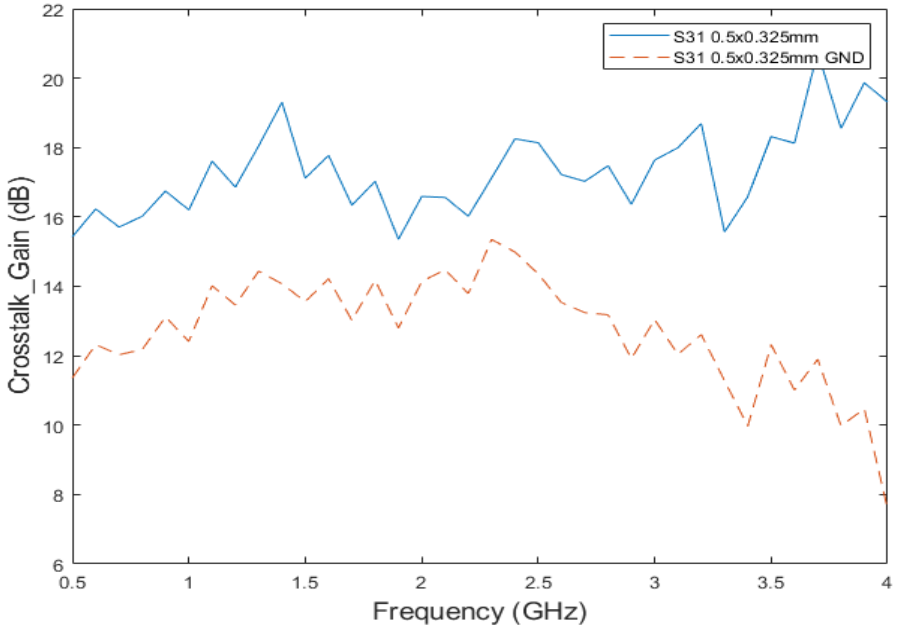

Figure 5.5: Increased crosstalk with bond wires compared to without bond wires for 0.325 mm spacing. Results include PCB's with and without the center ground wire.

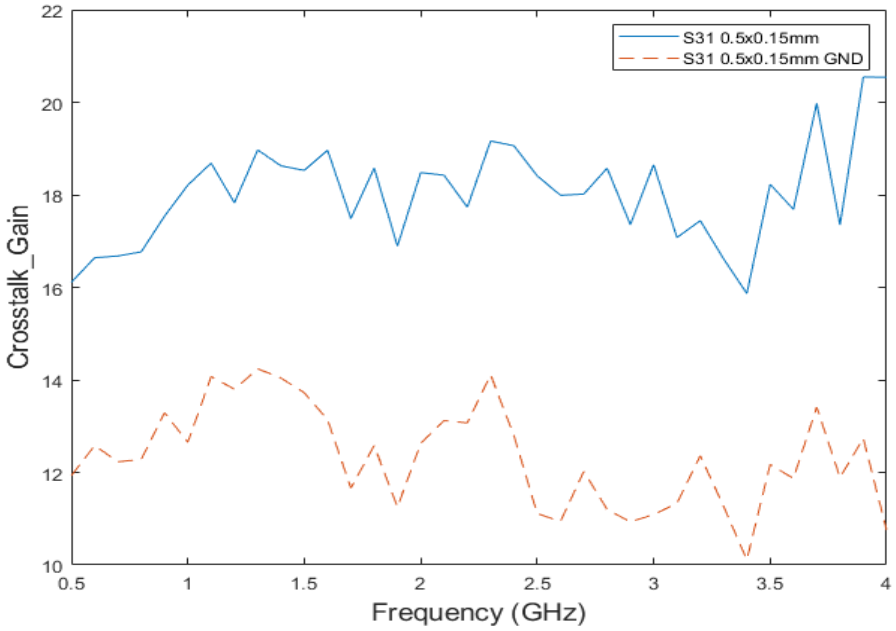

Figure 5.4: Increased crosstalk with bond wires compared to without bond wires for 0.15 mm spacing. Results include PCB's with and without the center ground wire.

Table 5.3: Bond wire crosstalk gain (No GND/GND)

Spacing	Mean $\|S_{31}\|$ No GND (dB)	Mean $\|S_{31}\|$ GND (dB)	$\Delta(dB)$
0.5 mm	-16.97	-14.80	-2.17
0.325 mm	-17.33	-12.73	-4.60
0.15 mm	-18.04	-12.34	-5.70

Expressing the coupling with wires as a gain compared to the measurements without wires shows similar trends to the previously presented data. The circuits with the ground wire arrangement continue to show reduced levels of coupling compared to the counterparts without. This confirms the theory that the ground wire arrangement has been effective in reducing the coupling between bond wires. The mean coupling gain for the different circuits are shown in Table 5.3.

5.4 Inductive vs Capacitive coupling

Coupling between microstrip transmission lines exists and has been discussed in previous sections. There is also a certain capacitive coupling between the bond

wires themselves which affects the measurements to an extent. In order to assess the magnitude of the impact the capacitive coupling was simulated in ADS. The model described in Figure 4.1 was modified to suitably incorporate a capacitor between the two lines. An estimation of the capacitance was given by the straight-wire equation, formula 3.4, described in Chapter 3. Inserting the value into the simulation was found to have a negligible impact on measurements, which was expected to a certain extent given the computed value of $8.087 \cdot 10^{-15}$ F was relatively small compared to the mutual inductance between the wires.

Further investigations into the impact of capacitive coupling between the wires were conducted by modifying one of the PCB's. The chip with a 0.5 mm spacing and grounded wire in the center was chosen. Grounding the wire using vias on both ends creates a loop with the bottom copper plate. The crossection-area reduces the inductive coupling and the crosstalk between the wires. Cutting the line on one side of the center wire breaks this loop. Measurements confirmed that the effectiveness of the arrangement was reduced considerably as the crosstalk was comparable to the levels measured on the 0.5 mm PCB without a center wire arrangement(Figure 4.9). This suggests the crosstalk between the wires consists largely of inductive coupling rather than capacitive coupling, as capacitive coupling would in theory be unaffected by severing one of the connections to ground so long as it is connected on the other end. Studies exist that have partially discussed the mutual coupling between bond wires. Bronckers et al.(2009) state that while capacitive coupling exists between on-chip interconnects, the dominant coupling factor between bond wires is the inductive coupling[3].

5.5 Further Considerations

The ground wire concept was chosen for a number of reasons. Most importantly, this method of decoupling wires was found to be a practical one that may be useful in circuit design. This is due to the ease of accommodating an extra bond wire into a space containing other conducting bond wires. Other methods of decoupling may include adding an angle to bond wires relative to the perpendicular line from the edge of the chip. This may be impractical when considering chips with a large number of bond wires. The same problem applies to the method of increasing spacing between bond wires as space may be an issue considering the compact nature of IC's. One difference between the testing done in this thesis and IC chips which are used in practice is that a method of sealing IC's is the addition of a layer of epoxy or a similar compound for the purpose of protecting the components from external impact. As such, those IC's have bond wires which are sealed in the surrounding compound and not air, which was not the case in this survey. One difference in that case can be found in formula 3.3, where the μ_r factor will be different depending on the material used. The magnetic field strength will thus be different.

Chapter 6
Conclusions

This chapter reconnects to the initial problem statements detailed in Chapter 1. Research questions are reiterated and the relevant findings in relation to the question are summarized. In total there are seven questions explaining conclusions that are drawn from the contents of this thesis.

How is it possible to measure the inductive coupling between bond wires?

The design setup is described in detail in Chapter 3, section 3.2. Bespoke PCB's were manufactured for the purpose of testing with a VNA. It was decided that the best way of going forward was manufacturing boards with varying spacing for the bond wires. The dimensions chosen for the center-to-center spacings was 0.5 mm, 0.325 mm, and 0.15 mm. As such it was possible to measure the increase in coupling as the spacing decreased. Placing the microstrip transmission lines perpendicular to one-another made it possible to limit the capacitive and inductive coupling between transmission lines as they were not relevant for the measurements between the wires.

What causes coupling when a bond wire is used to connect an integrated circuit and its casing?

In this thesis, the results show that there is significant coupling between wires. One of the causes for this has been shown to be the proximity of the wires. As it can be seen in the results, the 0.15mm chip shows more coupling than the 0.325mm chip, which in turn shows more coupling than the 0.5 mm chip. Frequency plays a large part in the coupling as the results indicate that there is significantly more coupling at higher frequencies. At 500 MHz the coupling can be considered insignificant for performance while at 4 GHz, the coupling starts to become much more marked. As such, high frequencies and bond wire proximity were the main factors contributing to the coupling.

How does the bonding process for integrated circuits work?

Bespoke equipment for the purpose of placing bond wires on PCB's exists and is necessary considering the small scale at which bond wires function. High-frequency oscillations are used to bond the wire to the pad on which it is to be connected.

Placement of the wire is done using input parameters which are processed to move the needle containing the wire.

Is the interference significant?

The answer for this question depends on many different factors. Not least, it depends on the chip itself. What is possible to say is that the coupling effect becomes more of a problem at higher frequencies, becoming a distinguishable phenomenon beginning at 500 MHz. Approaching 4 GHz, which was the highest frequency measured, showed crosstalk approaching levels under -20 dB. Depending on the application, this level of coupling can be considered significant. It is also important to consider what higher frequencies might lead to. The setup described in Figure 4.1 was simulated at frequencies up to 30 GHz. This lead to theoretical crosstalk of levels up to a maximum of -19.164 dB at 30 GHz (Figure 6.1). The blue line shows the simulated crosstalk for the 0.5 mm spacing, while the yellow and red lines show the crosstalk for the 0.15 mm and 0.325 mm spacings respectively. It is hard to say how well this simulation represents reality without actual testing at higher frequencies, but it does give an indication of how the coupling continues to increase beyond the frequencies tested in this thesis. Whether or not design considerations have to be taken to mitigate this is a question related to the architecture of the IC in question. As was discovered during both testing and simulation, closer wire spacing increases the coupling effect making the interference more significant.

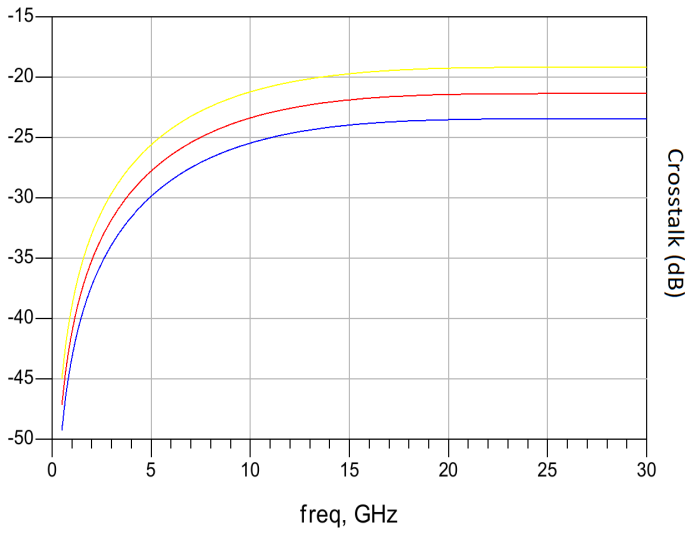

Figure 6.1: Crosstalk levels($|S_{31}|$)for 0.15 mm spacing up to 30GHz

How is the interference characterized?

Bond wires used to transmit RF-range signals are mainly subjected to interference in the form of coupling crosstalk, as has been discussed in Chapter 5. It was found that the forward transmission is largely unaffected by induction between the bond wires at higher frequencies. Attenuation was found to be largely unaffected by adding a ground wire. Crosstalk however is affected by inductive coupling between bond wires as shown in Figure 4.10. Frequency is a factor as higher frequencies lead to increased coupling. Thus the main factor to consider here is the magnitude of the signal leaking into adjacent bond wires as a result of the coupling.

Is it possible to limit the effect of the interference? What methods can be effective in reducing the impact of interference?

It was found that placing an additional bond wire in between existing bond wires and connecting it to ground limited coupling of the existing bond wires. This arrangement was found to be effective on all three tested bond wire spacings, with the method being more effective the closer the spacing was. It was found that the method of placing a grounded point of conducting metal, as described under section 4.3, was not effective in limiting interference. This was concluded after reviewing results from the PCB with this arrangement as the crosstalk levels were not reduced. Other methods related to the shape and placement of the bond wires have also been discussed throughout this thesis, however these have not been tested. Additional measures may be tested in future research projects.

How is the forward transmission effected by the coupling at higher frequencies?

Testing has showed that there are some differences in forward transmission between the six different PCB's. The differences are relatively small however. Results seem to imply what has been shown in the simulations; that forward transmission seems to be largely unaffected by the inductive coupling between bond wires, even at close spacing. The main impact of the coupling is the crosstalk experienced between the wires at higher frequencies.

Chapter 7
Future Work

This thesis has investigated the inductive coupling between bond wires. The coupling has been measured with different wire spacing and some grounding measures tested. It is possible to build on this and explore the impact of the angle of the wire. Bond wires in this thesis have been tested were parallel to one another. Testing varying angles should give ideas of how the coupling can be reduced with this method. It is also possible to make a comparison of the couplings using different materials commonly used in bond wires, such as copper, gold or silver. Increasing the frequency range with equipment capable of measuring at 10GHz - 100Ghz could also yield some interesting results and observations.

The implementation of a coupling-limiting bond wire has lead to some interesting questions regarding its use. It should be possible to conduct a EM analysis and simulate the effect it has on the magnetic field of bond wires. It could then lead to some conclusions on how to optimally place and shape the wire in relation to others on a PCB. This would be useful considering the large amount of bond wires that can be present on PCB's, theoretically leading to a stronger coupling than the two adjacent ones tested.

Bibliography

[1] //SEIBERT/MEDIA and JGraph. *draw.io*. `https://www.draw.io/`, last accessed on 20/12 - 2019.

[2] George Alexander. *SSI/MSI/LSI/VLSI/ULSI*. Mosaic, 1984, pp. 10–17.

[3] Stephane B. et al. *Experimental Analysis of the Coupling Mechanisms Between a 4 GHz PPA and a 5–7 GHz LC-VCO*. IEEE transactions on instrumentation and measurement, VOL. 58, NO. 8, 2009.

[4] *Bonding Wires for Semiconductor Technology*. Heraeus, 2017, pp. 8–9.

[5] F. Caspers. *RF engineering basic concepts: S-parameters*. CERN, 2012.

[6] E. Jan Vardaman Chet A. Palesko Amy J. Palesko. *Cost comparison for Flip Chip, Wire Bond, and Wafer Level packaging*. SavanSys Solutions, LLC, TechSearch International, Inc, 2010.

[7] Würth Elektronik. *Wire Bonding*. 2019.

[8] Torbjörn Frederick M. Tesche Michel Ianoz. *EMC Analysis Methods and Computational Models*. John Wiley Sons Inc., 2017.

[9] Nicholas Giordano. *College Physics: Reasoning and Relationships*. Cengage Learning, 2017.

[10] Frederick W. Grover. *Inductance Calculations*. Dover Publications, New York, 1952.

[11] Hitachi. *What are semiconductors?* `https://www.hitachi-hightech.com/global/products/device/semiconductor/ic.html`, last accessed on 20/12 - 2019.

[12] Autodesk Inc. *Eagle*. `https://www.autodesk.com/products/eagle/overview`, last accessed on 20/12 - 2019.

[13] JEDEC. *integrated circuit (IC), JESD99B, 5/07*. 2000.

[14] AV Nirmal Kamaljeet Singh. *Bond Wire and its Characterization at RF Frequencies*. High Frequency Electronics, 2017.

[15] Jack S. Kilby. *Invention of the Integrated Circuit*. IEEE Transactions on Electron Devices, 1978, pp. 1–4.

[16] Thomas H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 1998.

[17] Rafie Mavaddat. *Network Scattering Parameters*. World Scientific, Signapore, 2009.

[18] Clayton R. Paul. *Analysis of Multiconductor Transmission Lines 2nd Ed.* John Wiley Sons, Inc., 2008.

[19] Prof. James Bridges Prof. Mats-Olof Mattsson Prof. Anders Ahlbom. *Health Effects of Exposure to EMF*. Scientific Committee on Emerging and Newly Identified Health Risks , SCENIHR, 2009.

[20] Xiaoning Qi. *High frequency characterization and modeling of on-chi interconnects and rf ic wire bonds*. Stanford University, 2001.

[21] Edward B. Rosa. *The Self and Mutual Inductances of Linear Conductors*. U.S. Department of Commerce and Labor, Bureau of Standards, 1908.

[22] Keysight Technologies. *Agilent ADS*. `https://www.keysight.com/en/pc-1297113/advanced-design-system-ads?cc=US&lc=eng`, last accessed on 20/12 - 2019.

[23] Inc. The Mathworks. *Matlab*. URL: `https://se.mathworks.com/products/matlab.html`.

[24] *Understanding Shielded Cable*. Alpha Wire, 2009.

[25] Brian C. Wadell. *Transmission Line Design Handbook*. Artech House, 1991.

[26] Y.P. Zhang Wei Wang. *0.18-m CMOS push-pull power amplifier with antenna in IC package*. IEEE Microwave and Wireless Components Letters, 2004.

[27] Harold A. Wheeler. *Transmission-line properties of a strip on a dielectric sheet on a plane*. IEEE Tran. Microwave Theory Tech., vol. MTT-25, 1977.

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