Ring amplifiers for high speed pipeline assisted SAR ADCs

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Ring amplifiers for high speed pipeline assisted SAR ADCs

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Abstract

This thesis contains a review of published ring amplifier topologies. It is suggested to split the input stage of the ring amplifier into two. In this way, a robust ring amplifier can be designed without stacking the transistors in the second stage of the ring amplifier, boosting its speed properties. The split input stage can also be used to design a fully differential bias enhanced ring amplifier, boosting the ring amplifiers settling properties at the cost of lower gain. A figure of merit for the ring amplifiers is suggested. The advantages and disadvantages of using ring amplifiers in pipeline assisted SAR ADC is discussed with regards to noise power, linearity, settling speed and PVT robustness. A figure of merit for ring amplifiers is suggested.

A ring amplifier based pipeline assisted SAR ADC is implemented with some non-critical components realized using behavioral modelling. The implemented ADC reaches, SNR 58 dB, SFDR 71 dB, consuming 3.3 mW operating at 550 MHz. The performance of the pipelined SAR ADC is compared with an existing conventional SAR ADC. It is concluded that the ring amplifier is well suited for high speed pipeline assisted SAR ADCs from a noise, linearity and power perspective but it is somewhat limited by its relatively low settling speed.

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Abbrevations

SAR	Successive approximation register
ADC	Analog to digital converters
DAC	Digital to analog converters
CDAC	Capacitive digital to analog converters
MCS	Merged capacitor switching
CMS	Common mode based switching
RF	Radio frequency
RAMP	Ring amplifier
FD-SOI	fully-depleted, Silicon-on-Insulator
FF	Fast-fast process corner
SS	Slow-slow process corner
FS	Fast nmos-slow pmos process corner
SF	Slow nmos-fast pmos process corner
TT	Typical-typical process corner
PVT	Process, temperature and supply variations
MSB	Most Significant Bit
LSB	Least Significant Bit
CMFB	Common mode feedback

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Chapter 1

Introduction

Global total mobile data traffic reached approximately 38 exabytes per year at the end of 2020, and is projected to grow by a factor of 4 to reach 160 exabytes in 2025 [1]. In 2025 it is estimated that the average smart phone user might consume as much as 24 Gbyte per month [1]. Existing commercial telecommunication, 4G are limited to frequencies below 2.7GHz [2]. In the future this could lead to frequency congestion, especially in highly urbanized areas. This has caused telecommunication companies such as Ericsson to design radio circuits for the 5th generation of mobile communication, operating in the mostly unused millimeter-wave spectrum, *i.e.* frequencies from 30 GHz to 300 GHz. Not only will this solve the problem with frequency congestion, but it will also allow for channel bandwidths much larger than what is used in 4G today. The increased channel bandwidth will allow for drastically increased data rates [2].

In 4G receivers the sigma delta ADC has been the most prevalent converter. However, the increased channel bandwidth in 5G systems makes sigma delta ADCs unpractical. Instead Nyquist ADCs will most likely be used. A combination of scaling, new architectures and circuit solutions during the last decade have lead to substantial improvement of Nyquist ADCs [3]. Implementation of ADC that passes the stringent, linearity noise and power required of state of the art receivers is still very challenging. One promising Nyquist ADC architecture is the successive approximation (SAR) ADC. While (SAR) ADC are capable of high performance, they are somewhat limited by the fact that the conversion speed is relatively low. One approach when faced with this problem has been to split the SAR ADC into a pipelined SAR ADC, using a residue amplifier. Unfortunately, the residue amplifier consumes a substantial part of the energy budget. This has sparked a pursuit of novel residue amplifiers with low power consumption and fast settling speed.

1.1 This thesis

This thesis was conducted at the mixed signal research unit at Ericsson AB in Lund, Sweden. The aims of this thesis have been to study ring amplifier applicability on ADCs further. There has been a strive to put the ring amplifier in a context that is of some academic interest and that is preferably in line with the activities conducted at Ericsson research. All simulations were done using Cadence Virtuoso. The design kit used was a 22 nm, fully-depleted Silicon-on-Insulator (FD-SOI) CMOS from Global Foundries and the supply voltage used was 800 mV.

1.2 Report organization

This thesis is organized as follows.

- **Chapter 2**: A brief introduction to Nyquist analog to digital converters (ADC) is given.
- **Chapter 3**: Introduces the ring amplifier, discusses its theory and reviews various circuits topoligies.
- **Chapter 4**: Proposes two fully differential ring amplifiers, designed for fast settling.
- **Chapter 5**: A pipeline assisted ring amplifier based SAR ADC is implemented, with some of the components realized using ideal models and some components reused from an existing SAR ADC design at Ericsson.
- **Chapter 6**: The implemented ADC is discussed and conclusions are drawn.

Chapter 2

Fundamentals of data converters

2.1 Fundamental noise sources

2.1.1 Quantization noise

An inherent property of sampling is quantization noise. If the quantization stage is Δ, the maximum quantization error is bounded by $|\Delta/2|$. Assuming that the quantization errors are uniformly distributed between $-\Delta/2$ and $\Delta/2$ exists with equal probability. Where the probability is $p(\varepsilon_Q) = 1/\Delta$. The power of the quantization noise can be derived, eq 2.1.

$$P_Q = \int\limits_{-\Delta/2}^{+\Delta/2} \varepsilon_Q^2 p(\varepsilon_Q) \mathrm{d}\varepsilon_\mathrm{Q} = \frac{\Delta^2}{12} \tag{2.1}$$

According to [4] there are four conditions to be fulfilled for the qntization noise to be white.

- All the quantization levels are exercised with equal probability
- Large number of quantization leves are used
- The quantization stages are uniform
- The quantization error is not correlated with the input

White noise corresponds to a Dirac auto correlation function. Under very short time frames it is not reasonable to say that there is no correlation between different outputs codes. A full mathematical analyses have been carried out in [5], where it is shown that the autocorrelation function approach zero even for short correlation times, under the conditions stated above, making the Dirac pulse a good approximation.

2.1.2 Clock Jitter

Noise in the clock generation cause uncertainty in the sampling time. This is illustrated in fig, 2.1, Where T is the time between different sampling instants and ΔT_n is the error associated with sampling number n. The connection between the sampling time error and the amplitude error is given by eq 2.2. From eq 2.2 the noise power can be calculated,

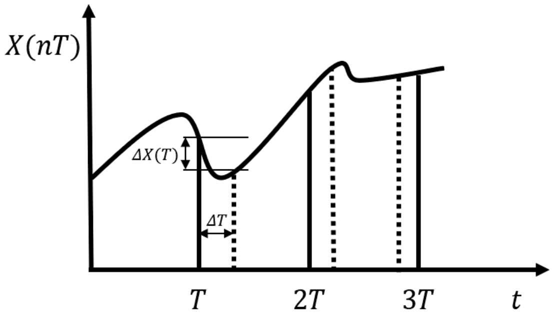

Figure 2.1: Illustration of sampling jitter.

eq 2.3 and eq 2.4 in dB. Where $< \Delta X^2 >$ is the average noise power and $< \Delta T^2 >$ is the average jitter.

$$\Delta X_n(nT) = A\omega_{in}\Delta T_n cos(\omega_{in} nT) \tag{2.2}$$

$$< \Delta X^2 > = \frac{A^2\omega_{in}^2}{2} < \Delta T^2 > \tag{2.3}$$

$$SNR_{quantization,\,\mathrm{dB}} = 10\ log(\omega_{in} < \Delta T >) \tag{2.4}$$

2.1.3 kT/C noise

Another very important noise source is the kT/C noise. The kT/C is unavoidable when sampling an input voltage on a capacitor. Consider Fig. 2.2 (a), the switch is open and the output voltage doesn't change. In 2.2 (b) the switch is closed and the output voltage follow the input voltage v_s if $RC >> 1/f_{sig}$. Where f_{sig} is the frequency of the input signal. The switch resistor is modeled by R_{sw} and the noise from the switch resistor is denoted by v_n. The resistors noise spectrum is white and has the spectral power density of $v_n^2 = 4kTR_n\Delta f$. Integrating the resistor noise over the low pass filter, kT/C is obtained, eq 2.5.

$$\int_{-\infty}^{\infty} 4kTR * H(f)^2 df = \int_{-\infty}^{\infty} \frac{4kTR}{1+(2\pi fCR)^2}\mathrm{df} = \frac{\mathrm{kT}}{\mathrm{C}} \tag{2.5}$$

2.2 SNR, SFDR and SNDR

SNR, is the signal to noise ratio. Signal-to-noise ratio (SNR) is defined as the ratio of the signal power to the noise power.

$$SNR = 10\ log_{10}\Big(\frac{Signal\ power}{Noise\ power}\Big) \tag{2.6}$$

SFDR, is the spurious-free dynamic range. Spurious-free dynamic range (SFDR) is defined as the ratio of the signal power to the largest spur.

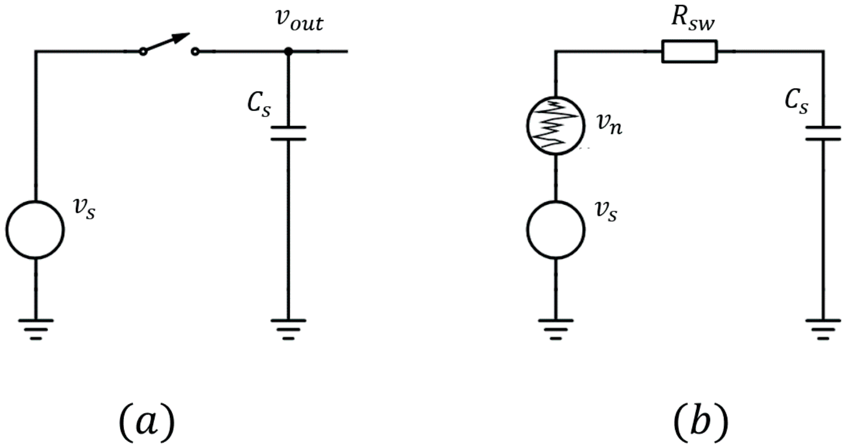

Figure 2.2: Simple sampling model.

$$SFDR = 10\ log_{10}\Big(\frac{Signal\ power}{Largest\ spur}\Big) \tag{2.7}$$

SNDR, is the signal noise and distortion ratio. Signal-to-noise-and-distortion ratio (SNDR) is defined as the ratio of the signal power to the sum of the distortion and the noise power.

$$SNR = 10\ log_{10}\Big(\frac{Signal\ power}{Distortion\ power\ +\ Noise\ power}\Big) \tag{2.8}$$

2.3 Effective number of bits

The power of a full scale sine wave is given by, eq 2.9, where n is the number of bits. The signal to noise ratio can be written as eq, 2.10 and 2.11. By including all noise and distortion sources, it's possible to define [4] the effective numbers of bits (ENOB).

$$P_{sin} = \frac{1}{2}\Big(\frac{\Delta 2^n}{2}\Big)^2 \tag{2.9}$$

$$SNR_{quan,dB} = 10\ log(\frac{P_{sin}}{P_Q}) = 6.02 \times n + 1.76 \tag{2.10}$$

$$n = \frac{SNR_{quan,dB} - 1.76}{6.02} \tag{2.11}$$

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.12}$$

2.4 ADC figure of merit

Analog to digital converters are characterized by numerous performance metrics, such as die area, power dissipation, conversion rate, analog input bandwidth, resolution, harmonic distortion and power supply voltage. More performance metrics can be found in [4]. A useful figure of metrics can only incorporate a subset of these metrics. Ideally the figure of merit should capture as much fundamental physics as possible.

The two most common figure of merit for ADCs are the Walden FOM [6] and the Schreier FOM [7]. Both FOMs focus on the trade off between SNDR, power and conversion rate. If the circuit operates well below its bandwidth limit, the connection between power and conversion rate is straight forward. A doubling of the conversion rate will result in a doubling of the power consumption, $Power = E * f_s$. The connection between energy and SNDR is more complex. It can be shown empirically by looking at a large number of publication [3], that for a low resolution ADCs, SNDR < 50 dB, an extra bit added result in twice the power consumption. For these low resolution ADCs, the Walden FOM is appropriate, eq 2.13.

$$FOM_w = \frac{P}{f_s\, 2^{ENOB}} \tag{2.13}$$

High precision ADCs with SNDR $> 50dB$ are on the other hand limited by thermal noise. In this case, adding an extra bit will require a quadrupling of the power consumption [3]. For this case the Schreier FOM ought to be used, 2.14.

$$FOM_s = SNDR + 10\, log_{10}\left(\frac{f_s/2}{P}\right) \tag{2.14}$$

2.5 Comparator

The comparator is a fundamental building block in almost all type of data converters and is a bottle neck in some types of data converters. This section gives a short introduction to the topic, treating the most important metrics and trade offs. The comparator in Fig. 2.3 is used for the discussion. The concepts and methodology discussed here can be relatively easily be generalized to other types of latch based comparators. The operation of the comparator in Fig. 2.3 can be divided into four phases. It will be assumed that the circuit can be modeled by its small signal parameters during each of the phases and that small signal parameters remain relatively constant during each phase.

Phase zero. When the clk signal is low the internal nodes (P, Q, X, Y, W) are pre charged to Vdd. All the transistors M_1 to M_6 are turned off and the comparator does not consume any power.

Phase one starts when the clk signal is pulled high and ends when the transistors M_3 and M_4 turns on, $v_X = Vdd - v_{th}$ and $v_Y = Vdd - v_{th}$. When the clk signal is pulled high the voltage at node W drop steeply until it is close to ground. It's assume that the time needed for W to drop from Vdd to ground is sufficiently small to be neglected in a first order analyse. Next M_1 and M_2 turn on and the capacitance, $C_{X,Y}$ seen at

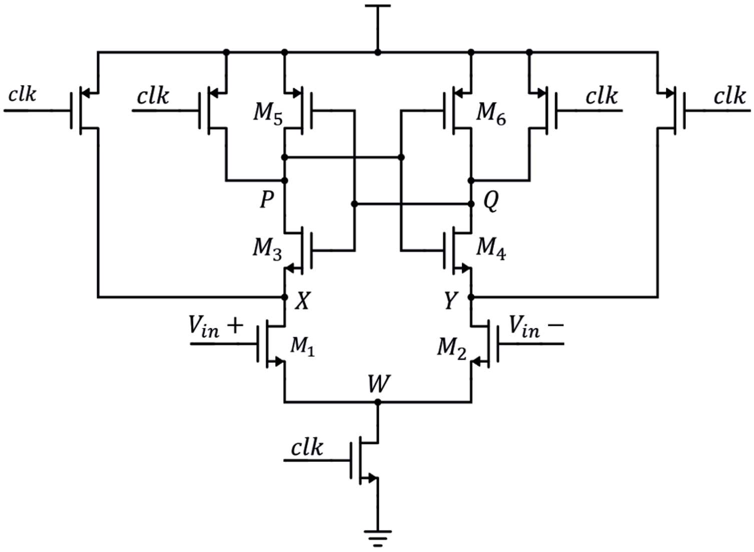

Figure 2.3: Strong-ARM latch.

X,Y starts discharging. Phase one lasts approximately $t_1 = C_{(X,Y)}v_{th}/I_{cm}$, where I_{cm} is the common mode current under the assumption that v_{in+} and v_{in-} are approximately equal. The gain i.e the voltage difference between V_X and V_Y can be approximated by $|v_X - v_Y| = g_m(v_{in+} - v_{in-})t/C_{(X,Y)}$

Phase two starts at the end of phase one and lasts as long as the transistors M_1 and M_2 remain in saturation. In other words phase two lasts as long as the node (X,Y) is resistively isolated from ground. The transistors M_3 and M_4 are active during phase two and the circuit exhibits negative feedback. The regeneration time constant in phase two [8] can be calculated as in eq, 2.15. If $C_{(x,y)} < C_{(p,q)}$ the regeneration time is very long and practically no regeneration occurs during phase two. Phase two is however often very short [8], the comparator doesn't necessarily suffer if no generation occurs during this phase.

$$t_2 = \frac{c_{(p,q)}}{g_m(1 - c_{(p,q)}/c_{(x,y)})} \tag{2.15}$$

Phase three is the final phase and is defined to start when all the transistors M_3, M_4, M_5 and M_6 are all active, the nodes X,Y is assumed grounded. The positive feedback will drive either X, or Y to ground or vdd respectively. The regeneration constant can be calculated to be $\tau_3 = g_m/c_{p,q}$. When the generation have occurred the comparators decision have been made, there is no open path to ground and hence no static power consumption in the end of phase three. As phase three isn't defined to start when phase two ends there may be a glitch between phase two and three, hopefully this glitch is small.

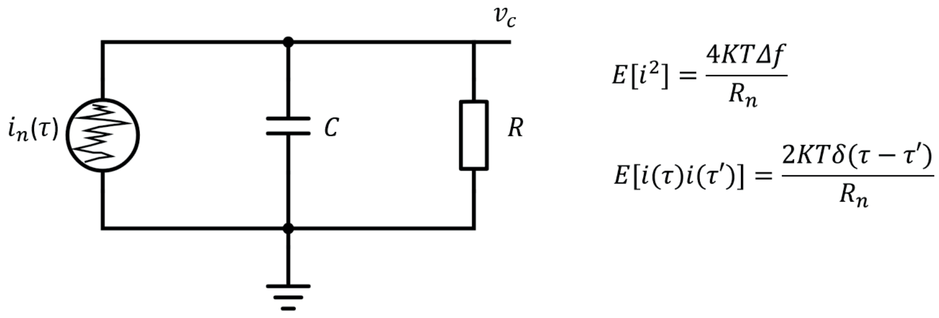
v_c
$i_n(\tau)$
C
R
$E[i^2] = \frac{4KT\Delta f}{R_n}$
$E[i(\tau)i(\tau')] = \frac{2KT\delta(\tau - \tau')}{R_n}$

Figure 2.4: Noise model during phase one. The noise source, is a current noise source.

2.5.1 Meta stability

If the compactor aren't capable of making a decision during the allocated time. Meta stability occurs. Eq 2.16 estimates the probability for meta stability. τ_{eff} is the regeneration time of the entire compactor, A_0 the gain of the compactor and t the allocated decision time.

$$P_E = \frac{V_o}{V_{in}A_0} e^{-t/\tau_{eff}} \tag{2.16}$$

2.5.2 Noise

Since the comparator is dynamic, it is natural to study the noise properties in the time domain. Unlike a frequency domain approach, a time domain approach can easily be extended to cover non linear circuits. The noise analyses presented here closely follows the one presented in [8]. The discussion here will be limited to the noise originating from M_1 and M_2. It's noted in [9] that M_1 and M_2 are often the major noise source. The interested reader can consult [8] for a discussion of the other noise sources, M_3 and M_4.

A small signal noise model of phase one can be modeled as illustrated in 2.4. The voltage over the capacitor originating from the noise source in Fig. 2.4 can be calculated as in, eq 2.17. If i_n is a stochastic process, the mean of the integral in, eq 2.18 can be calculated. Several interesting observations can be made from, eq 2.18. First, assuming that the noise source in Fig. 2.4, is the thermal noise from a conventional resistor, $R_n = R$. If the time is sufficiently large, $RC << t$. The noise power will approach the familiar KT/C expression. Secondly, assuming that the noise source is the thermal noise from a transistor in saturation, $R_n = 1/\gamma g_m$. If the time is sufficiently small, $RC >> t$. The noise power will approach eq 2.19. Where the Taylor approximation have been used. The gain at a specific time under phase one is given by eq 2.20. By dividing eq 2.19 with eq 2.20, the input referred noise can be obtained eq 2.21. In eq 2.21, the noise originating from the clock switches have been neglected, σ_0^2. Eq 2.21, highlights the trade off between speed, power and noise in latch based comparators. The noise power can be lowered by increasing the transconductance g_m, resulting in higher power consumption.

Alternatively, the noise power can be lowered by increasing the decision time t. Other noise contributors, i.e M_3 and M_4 is discussed in [8].

$$v_{Cn}(t) = \frac{e^{-\tau/RC}}{C}\int_0^t \frac{e^{\tau/RC}}{C} i_n(\tau)d\tau + v_n(0)e^{-t/RC} \tag{2.17}$$

$$E[v_{Cn}(t)^2] = \frac{kTR}{CR_n}(1-e^{-2t/RC}) + \sigma_0^2 e^{-2t/RC} \tag{2.18}$$

Assuming that $RC >> t$ equation can be written eq 2.18, can be written as 2.19.

$$E[v_{Cn}(t)^2] = \frac{2kT\gamma g_{m\ 1,2}}{C^2}t + \sigma_0^2 \tag{2.19}$$

$$A_v = \frac{g_m t}{c_{(x,y)}} \tag{2.20}$$

$$\sigma_{in}^2 = \frac{4kT\gamma}{2g_m t} \tag{2.21}$$

2.5.3 Kick back

When the clock goes high, the M_1 and M_2 transistors draws large transient currents. The current through M_1 and M_2 are couples with the input through the gate-source and gate-drain capacitances. The gate source will primarily give rise to a common mode voltage drop of the input voltages v_{in+} and v_{in-}. The gate drain capacitance will give rise to a common mode and differential voltage drop of the input voltages v_{in+} and v_{in-}. If v_{in+} is larger then v_{in-} the voltage at p will drop faster than the voltage at node Q. Both Q and P will couple back to the input, but since P drops faster, v_{in+} will drop more then v_{in-}. If the differential input voltage is small, the kickback can flip the polarity of v_{in+} and v_{in-}, resulting in wrong decision. The common mode kickback doesn't change the polarity of v_{in+}, v_{in-} and is therefore of less concern.

2.6 ADC architectures

2.6.1 SAR ADC

The successive approximation analog to digital converters, SAR ADC is a very digital intensive analog to digital converter, and therefore highly suitable for scaling. A basic SAR ADC can be seen in Fig. 2.5. The input voltage, v_{in} is sampled and stored by the sample and hold circuit. Simultaneously, the output from the DAC is set to the half the reference voltage, $V_{ref}/2$. It's then up to the comparator to deduce if the input voltage is larger than half the reference voltage. If the input voltage is larger than half the reference voltage, $V_{ref}/2$, the DAC will adjust its output to $3V_{ref}/4$. If the input voltage is smaller than half the reference voltage, $V_{ref}/2$, The DAC will adjust its output to $V_{ref}/4$. In this way the SAR ADC performs a binary search of the input signal. The progression of the DAC can be seen to the right in Fig. 2.5, where the curved dotted line is the output of the DAC and the straight dotted line is the input voltage. Broadly speaking there is two ways of implementing the logic and the registers of the SAR ADC. Asynchronous and synchronous.

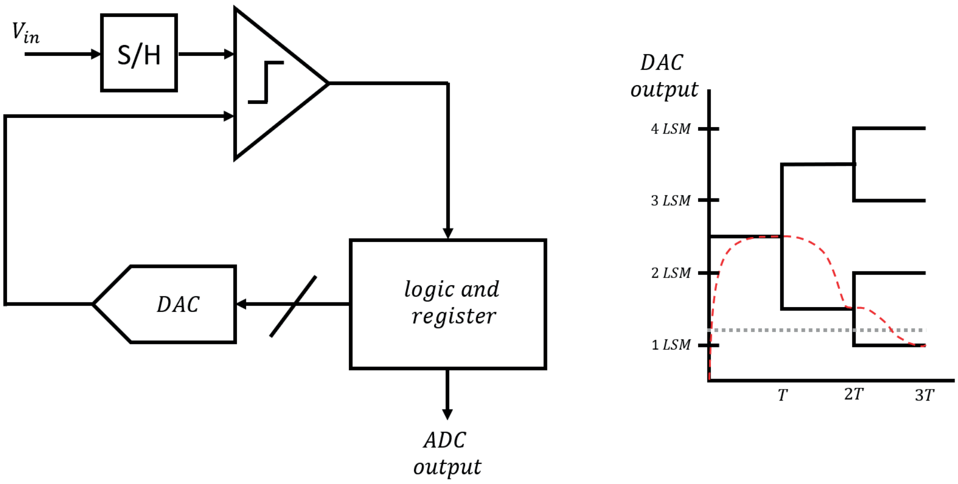

Figure 2.5: SAR ADC.

The synchronous version is clocked similar to conventional synchronous circuits. Asynchronous SAR ADCs on the other hand, use an internal clock generated by a comparator ready signal. This eliminates the need for high speed clock in the design boosting speed and lowering power consumption. For this reason, essentially all high performing SAR ADCs today employs asynchronous operation. Due to the digital intensive architecture of the SAR ADC, it is capable of operating at low power and reach high figure of merit.

C DAC

In high performance SAR ADCs the DAC is typically implemented as a capacitive based DAC, CDAC. A number of switching schemes have been proposed. These have advantages and drawbacks in terms of logic complexity, energy consumption, linearity and dependency on the accuracy of the common mode voltage. Only common mode switching (CMS) [10], [11] and Merged capacitor switching (MCS) will be discussed here.

Common mode based switching, Fig. 2.6 shows a CDAC that can implement common mode based switching. CMS works as follows, first the DAC output is connected to common mode, v_{cm} and the switches to the input voltage is closed. This way a charge proportional towards to the input voltage is sampled on the capacitors. Secondly, the common mode voltage is disconnected from the DAC output, and the input voltage located underneath the capacitors is disconnected from the bottom of the capacitors and the common mode voltage is connected. The above two stages are done in order to sample the input voltage on the DAC. By disconnecting the common mode voltage, v_{cm} underneath the capacitors and connecting the positive reference $v_{ref\ p}$ or the negative reference, , $v_{ref\ n}$ the receptively, the CDAC can be controlled in a binary fashion.

Merged capacitor switching is identical to common mode based switching apart from the fact that the input signal is sampled directly at the output node. This leads to lower conversion time but result lower in linearity, due to the fact the output of the CDAC sees a nonlinear capacitance from the comparator.

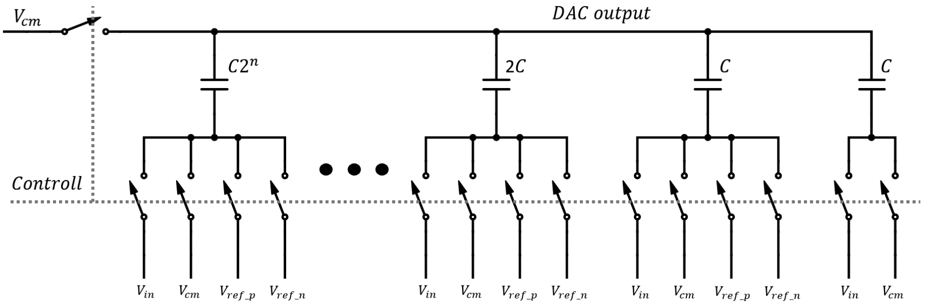
V_cm
DAC output
C2^n
2C
C
C
Controll
V_in V_cm V_ref_p V_ref_n
V_in V_cm V_ref_p V_ref_n
V_in V_cm V_ref_p V_ref_n
V_in V_cm

Figure 2.6: Common mode based switching.

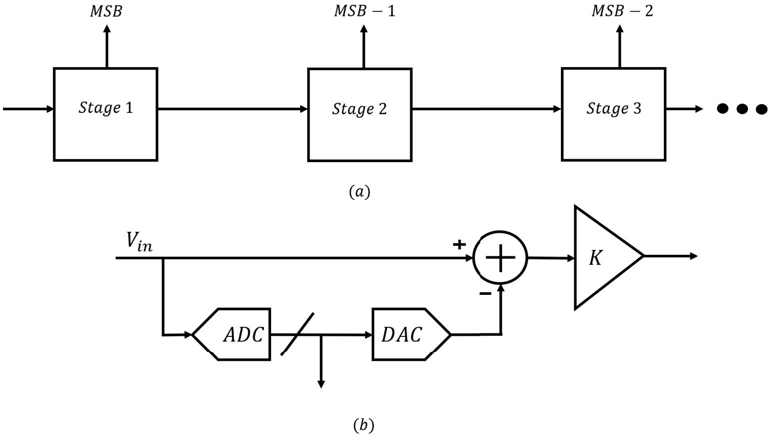
MSB
MSB − 1
MSB − 2
Stage 1
Stage 2
Stage 3
(a)
V_in
+
−
K
ADC
DAC
(b)

Figure 2.7: Illustration of the concept behind pipeline.

2.6.2 Pipeline ADC

Similar to the SAR ADC, the most basic pipeline also preforms a binary search of the input signal. Fig. 2.7, illustrates how a pipeline ADC works. The first stage check if the input signal is larger than half the reference, $v_{in\ stage1} > V_{ref}/2$, see Fig. 2.7 a. If the signal is larger then $V_{ref}/2$, the MSB is set to ”1” and $V_{ref}/2$ is subtracted from the signal $v_{in\ stage1}$. If $v_{in\ stage1} < V_{ref}/2$ the MSB is set to zero. The second stage check $v_{in\ stage2} > V_{ref}/4$. In order to check this equality, the reference needs to be scaled from $V_{ref}/2$ to $V_{ref}/4$. Instead $v_{in\ stage2}$ is multiplied by two and $2v_{in\ stage2} > V_{ref}/2$ is checked instead. Fig. 2.7 b, shows a generic pipeline stage. The amplifier with gain K ensure that the reference voltage doesn’t need to be scaled. It is possible to extract more than one bit per stage. The amplifier gain is then chosen as $K = 2^n$ where n is the number of bits per stage. Pipeline ADC are capable of reaching good performance in terms of noise and linearity at high speed, But often at the cost of high power consumption.

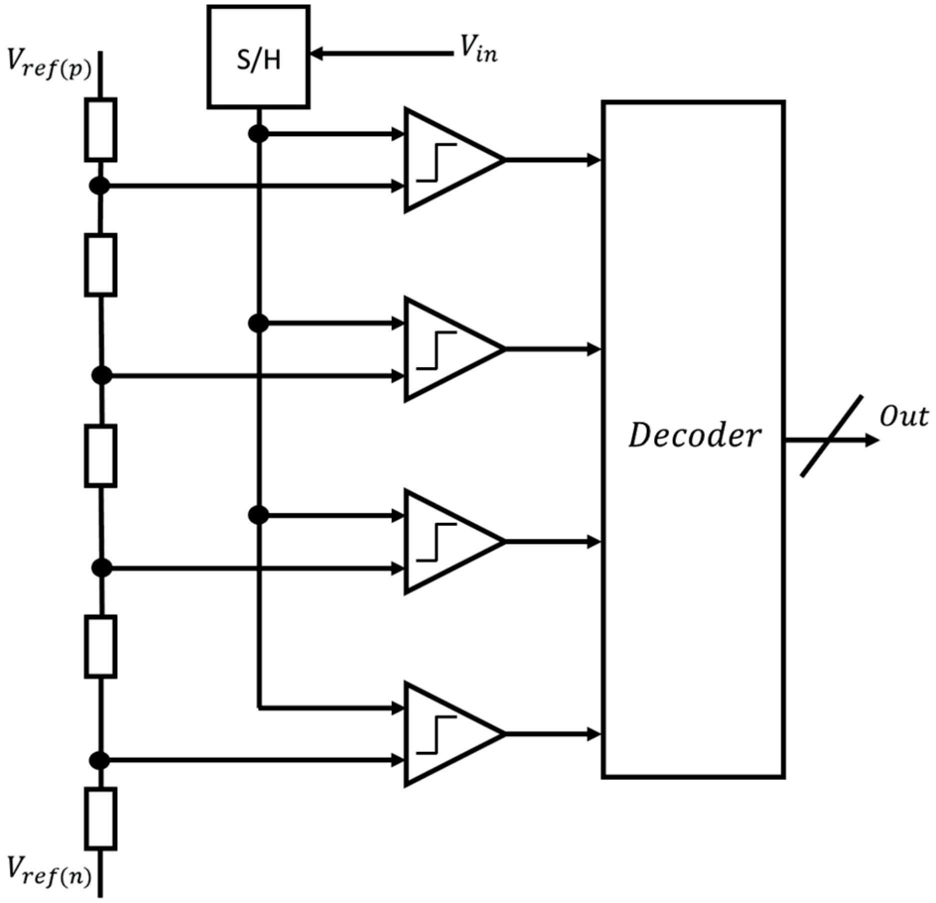

Figure 2.8: Two bit flash ADC.

2.6.3 Flash ADC

Fig. 2.8 shows two bit Flash ADC. The references are scaled down by the resistive ladder and then compared with the input voltage. The output of the Flash is thermometer coded and therefore needs to be decoded to binary, this is done by the decoder in Fig. 2.8. The Flash ADC carry out the conversion in one clock cycle, which enables the Flash ADC to reach very high speed at the cost of low resolution. Adding an extra bit will require twice as many comparators, doubling the power consumption.

2.6.4 Time interleaved ADC

With increasing sampling speed, the power-speed trade offs becomes strained. This is where time interleaving enters the picture. A number of slower sub ADCs can be operated in parallel. Fig. 2.9 features a time interleaved ADC with 4 sub ADCs. The sub ADC only need to operate at one quarter of the entire ADCs speed. This greatly relaxes the design of the sub ADCs in terms of speed. Unfortunately, time interleaving also leads

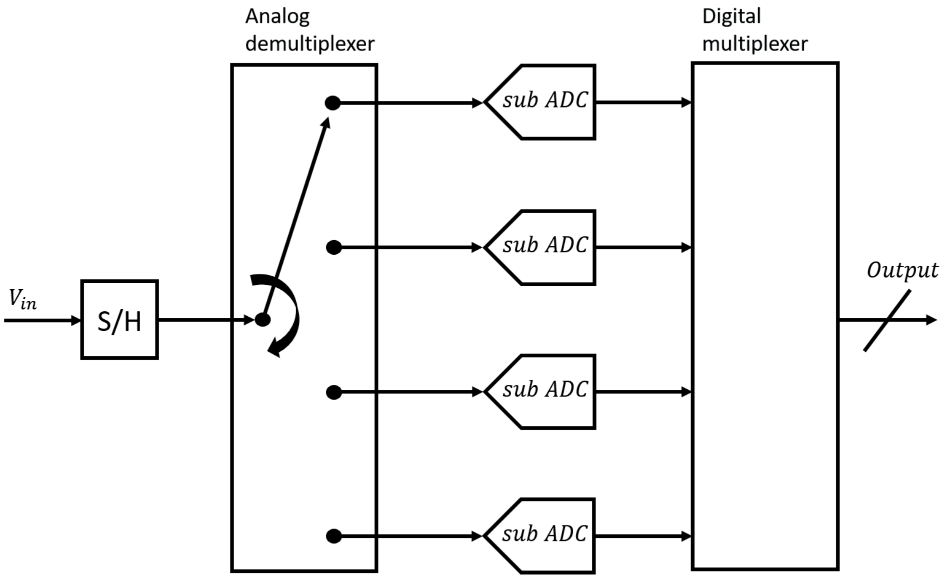
Analog
demultiplexer
Digital
multiplexer
V_{in}
S/H
sub ADC
sub ADC
sub ADC
sub ADC
Output

Figure 2.9: Time interleaved ADC.

to a number of problems. Gain and offset difference between sub ADCs lead to spurs. Difference in clock phase between the various ADCs also leads to spurs. Further, time interleaving doesn't relax the sample and hold circuit. The large number of subADCs consume a substantial amount of area. Furthermore, their parasitics will load the sample and hold circuit, thereby increasing its power consumption

Chapter 3

Review of ring amplifiers

Ring amplifiers have many attractive features, including high gain, high linearity, fast settling, relatively low noise and almost rail to rail output swing. This chapter outline the circuit theory of the ring amplifier and reviews various circuit topoligies.

3.1 Ring amplifier introduction

The conventional ring oscillator, shown in Fig. 3.1 is unstable due to the two internal poles and the output pole. Employing the Miller approximation, the small signal transfer function of the ring oscillator can be derived.

$$A_v(s) = \frac{A_1 * A_2 * g_m * r_{out}}{(1 + s * c_L r_{out}) * (1 + s * r_1 c_1) * (1 + s * r_2 c_2)} \tag{3.1}$$

The sub index's 1 and 2 refers to the first respective second stage in the oscillator. g_m denotes the transconductance of the output stage, $A_{1,2}$ is the gain. $c_{1,2}$ is the Miller capacitance, and is calculated by $c_i = c_{gs,i} + c_{gd,i} \times A_i$. If the output pole can be turned into a dominant pole by pulling it down in frequency, the ring oscillator could be stabilized in a feedback configuration, this is illustrated graphically in Fig. 3.2. It is assumed that c_L is relatively large compared to the internal capacitance's $c_{1,2}$, such that the output pole is located lower in frequency than the internal poles. Rewriting the transfer function 3.1, neglecting the internal poles and assuming that $\omega * C_L >> 1$, eq 3.2 is obtained. It's observed that the unity gain bandwidth is proportional to the transconductance of the output stage, eq 3.3, indicating that the ring oscillator could be stabilized by reducing output transconductance. The internal poles then become non-dominant and located well above the unit gain frequency. Stabilizing a ring oscillator by reducing the output transconductance is the central idea behind the ring amplifier [12].

$$A_v(s) = \frac{A_1 * A_2 * g_m}{s * c_L} \tag{3.2}$$

$$\omega_{UGB} = \frac{A_1 * A_2 * g_m}{c_L} \tag{3.3}$$

Perhaps the most common way of creating a ring amplifier from a ring oscillator, is illustrated in Fig. 3.3. The transconductance of the output stage is decreased by the resistor R, inserted between the two transistors M_1 and M_2. The resistor crates an offset

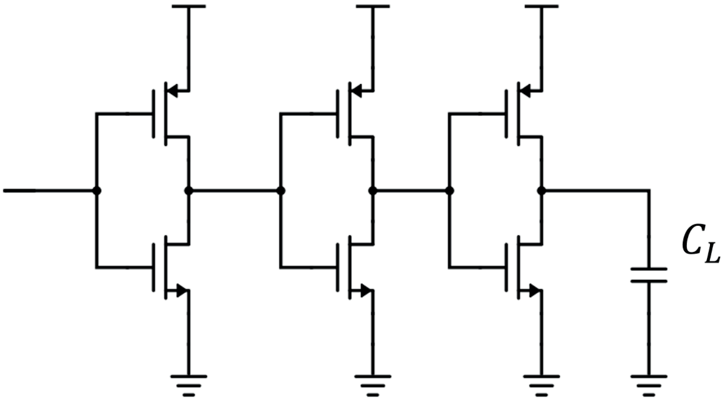

Figure 3.1: Conventional ring oscillator.

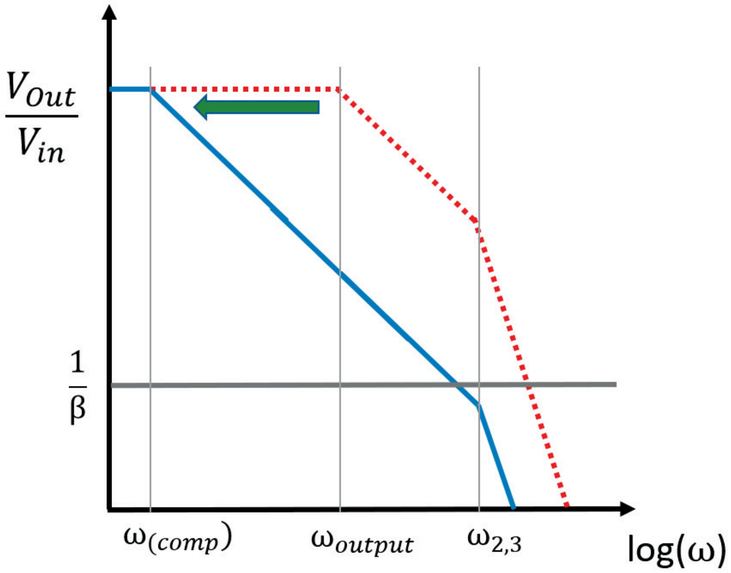

Figure 3.2: Plot of transfer function.

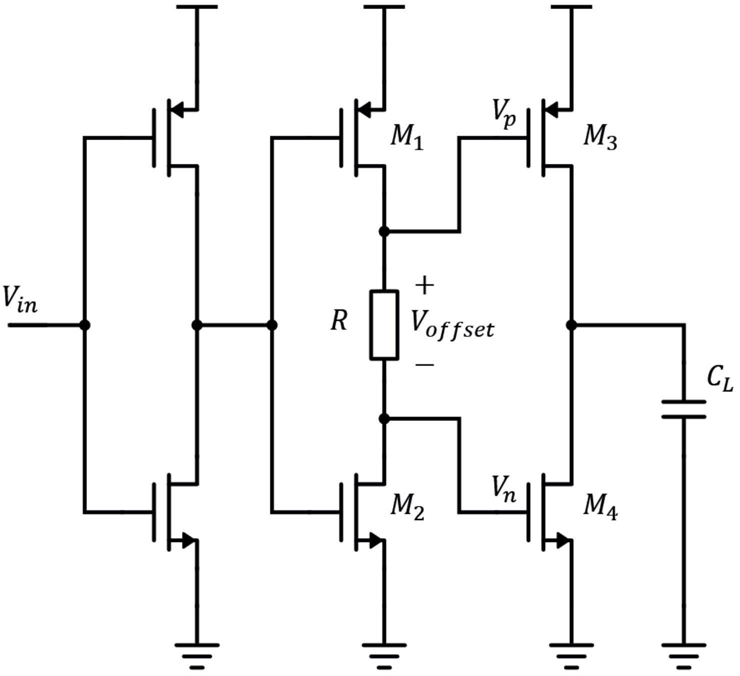

Figure 3.3: Common implementation of ring amplifier.

voltage, V_{offset} that decrease the gate source voltage over the transistors M_3 and M_4, biasing them in weak inversion. The extra stage added greatly boost the gain of the overall amplifier. The reduced of transconductance M_1 and M_2 is compensated by an increase in output resistance of the last stage. Ensuring that the gain of the output stage is approximately equal to the gain of stage one. The value of the offset voltage, V_{offset} is very important for the performance of the ring amplifier. In this thesis the offset voltage, V_{offset} is defined as the voltage drop over the resistor, R in Fig. 3.3 when the input voltage of the ring amplifier is set to common mode, $V_{in} = V_{cm}$.

The dynamic behavior of the ring amplifier is best understood by looking at an transient example. Fig. 3.4 feature a single ended switched capacitor ring amp based amplifier. During the sampling phase, Φ closed and $\overline{\Phi}$ open. The charge is sampled on capacitor c_1. During the amplification phase the charge on c_1 is transferred from c_1 to c_2. The voltage at the end of the amplification phase is given by, eq 3.4. Where A_v is the voltage gain of the ring amplifier. Eq 3.4 is only accurate if the amplification phase last long enough for the ring amplifier to fully settle.

$$V_{out} = \frac{c_1}{c_2} \frac{A_v}{A_v + c_1/c_2} V_{in} \tag{3.4}$$

Fig, 3.5 shows the transient response of the switched capacitor amplifier in Fig. 3.4. The transient settling can ruffly be divided into three relative distinct operation phases [12], slewing, stabilization and steady state.

Slewing, during the slewing phase both Vp and Vn rails to ground. Consequently,

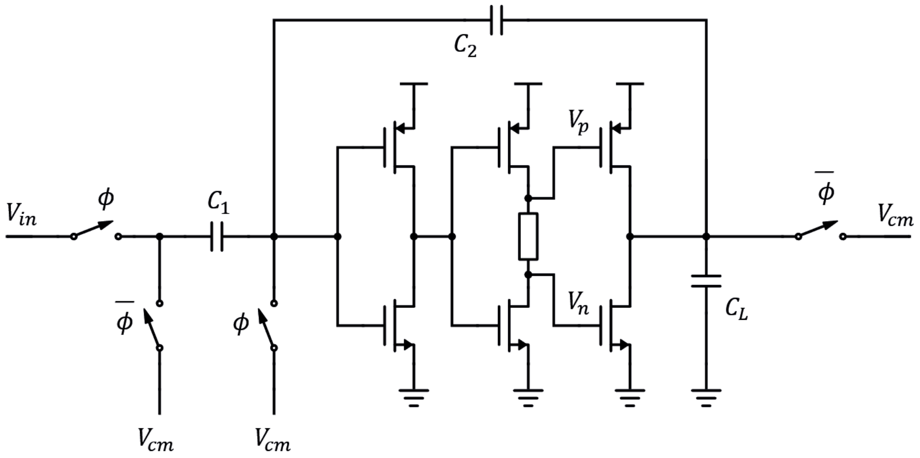

Figure 3.4: Simple switched capacitor amplifier, utilizing ring amplifier.

the nmos is turn off and the pmos is fully turn on. The ring amplifier slews as if it were a digital inverter. Making the slewing phase highly effective. Naturally, the voltage node Vp and Vn would rail to the supply voltage if the output were to be discharged.

Stabilization, during the stabilization phase, the ring amplifier exhibits damped oscillations until it reach steady state. Studying Fig. 3.6 can give deeper insight into ring amplifiers dynamic behavior in the stabilization phase. Looking at the voltages V_p and V_n intersected by $line1$ in Fig. 3.6, it can be seen that p device is almost entirely turned off and the overdrive over the n device has increased substantially. The increased overdrive over the n device translates to a substantially higher output transconductance. If the small signal parameter of the ring amplifier were to be extracted, in the instance marked by $line1$. It is perfectly possible that the small signal transfer function is unstable in negative feedback configuration. The conclusion from this is that at the time instance marked by $line1$ the ring amplifier most probably adds energy to the oscillations. Looking at the voltages V_p and V_n intersected by $line2$ in Fig. 3.6. Both the p and n devices is deep in weak inversion leading to a low output transconductance. From the discussion of the AC stability above, it is clear that in the instance marked by $Line2$ there is a positive phase margin if the ring amplifier is stable and energy is removed from the oscillation. Consequently, it is not sufficient with positive phase margin when the input voltage is at common mode to ensure stability. In order to obtain satisfactory stabilization, the oscillation energy most on average decrease. When the oscillation amplitude decrease, the ring amplifier spends more time in the region where the ring amplifier has a healthy phase margin. This leads to a non linear behavior that's make the ring amplifier hard to understand and analyses.

Steady state, the steady state ought to be straight forward, the signal is stable and the output voltage is given by eq 3.4. However, due to the a ring amp specific quark, the is some ambiguity on what exactly steady state refers to. Insight into this can be gain by studying Fig. 3.7. A voltage source is connected at the output and the input voltage of the ring amplifier is sweep. The current through the voltage source is plotted on the y axes, Fig. 3.7. The current supplied to the voltage source at the output, is identical

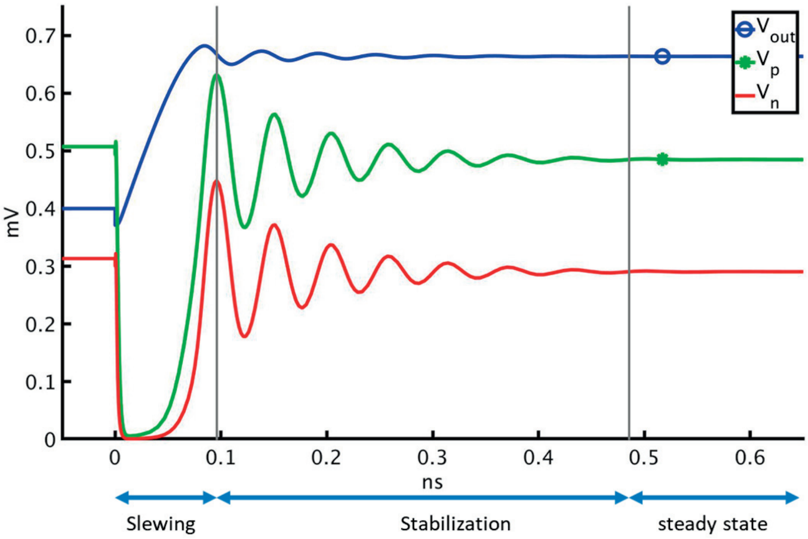

Figure 3.5: Transient response of ring amplifier. Highlighting the three different phases, slewing stabilization and steady state

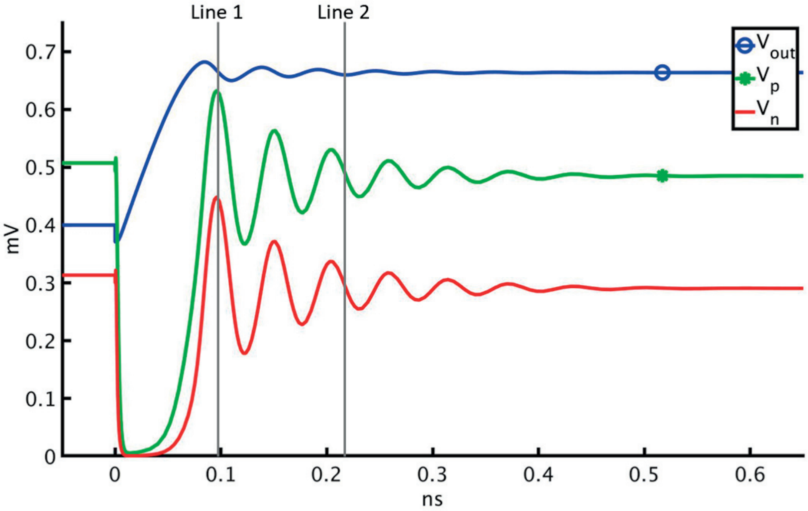

Figure 3.6: Transient response of ring amplifier.

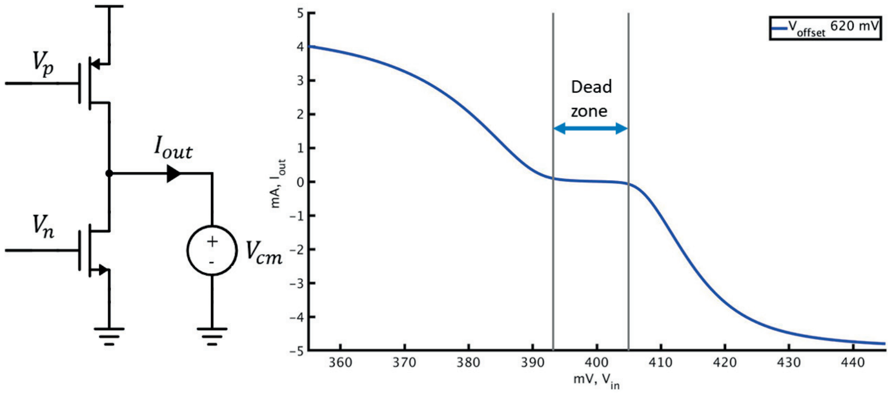

Figure 3.7: Ring amp dynamics.

with the current supplied to the capacitor for various input voltages, V_{in}. The slope of the curve in the plot 3.7 can in this case be thought of as the transconductance for the entire ring amplifier. The width of the flat area in the plot, denoted the dead zone [12] and is closely related with the offset voltage, V_{offset}. If the offset voltage, V_{offset} is large the dead zone is large and there is a relatively large range of input voltages where there are no to very little bandwidth. The implication of a very large voltage, V_{offset} and consequently a large dead zone can be seen in Fig. 3.8. After the slewing phase the input voltage enters the dead zone and decaying oscillation occurs. While the settling is free from oscillations, the settling is very slow when the input voltage approach common mode. Note that the plot is an extreme example, to illustrate the argument. One definition, is to say that the ring amplifier is settled when signal enters and not overshoot the dead zone [12]. In bulkier technologies this definition makes sense, because long channel transistors have low bandwidth when biased in weak inversion, the signal would settle very slowly ones inside the dead zone. However, the transistor characteristics in highly scaled design kits differ notably from there longer cousins, something that effects the ring amplifier dynamics. Short channel transistor has higher threshold voltage and more importantly can operator with relatively high bandwidth deep in sub threshold. In this rapport the ring amplifier is said to be settled or in steady state when the signal reaches its final value.

3.2 Design and trade offs

The ring amplifiers frequency compensation take place at the output stage. It's also the output stage that give rise to the complicated non-linear behavior of the ring amplifier. Fortunately, the IC designer only needs to take two design parameters into account when designing the output stage. The output transconductance is set by the *width* of the output transistors and the offset voltage, V_{offset}. Fig. 3.9 shows how the offset voltage affects the transient response of a ring amplifier, where the *width* has been held constant. The signal with offset voltage $600mV$ has a large dead zone leading to slow settling when the input voltage is close to common mode. The signal with offset voltage $380mV$ is under damped leading unnecessary oscillation before steady state, while a $490mV$ offset voltage depicts

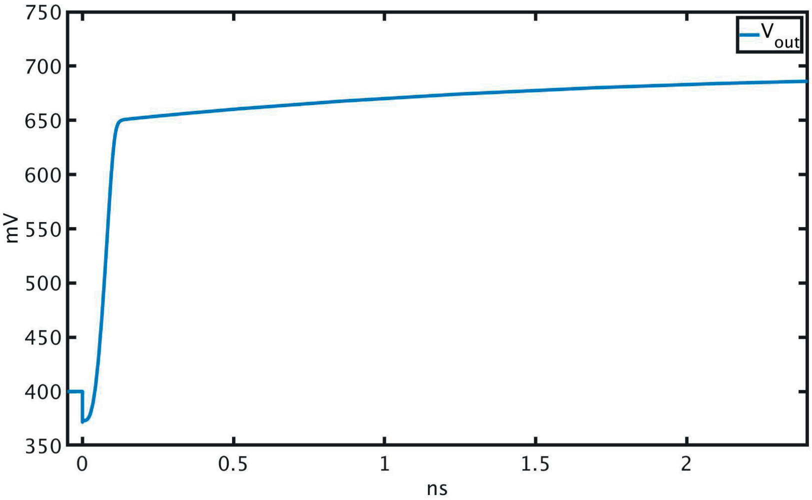

Figure 3.8: Transient response of ring amplifier with large offset voltage.

a somewhat optimized ring amplifier for a given output *width*.

At the end of the slewing phase and beginning of the stabilization phase, the ring amplifier overshoots as shown in Fig. 3.10 and calculated with

$$V_{overshoot} = \frac{t_d \times I_{slew}}{C_L} \tag{3.5}$$

where t_d is the delay time. The value of the overshoot voltage is determined by the slewing current (set by the *width* of the output transistors) and the delay time needed for the voltage v_p and v_n to recover. A larger overshoot needs to be compensated by a larger offset voltage. This is because a larger overshoot will result in more energy being added at the peak of the oscillation, previously shown by $line1$ in Fig. 3.6.

During the slewing phase, the voltages v_p and v_n rails. It's important that the second stage can provide enough current to very quickly recharge v_p and v_n to their final values, in order to ensure that the delay time, t_d and consequently the overshoot is sufficiently small. For example, if there is a large positive phase margin in steady state, the ring amplifier can be unstable if the current through the second stage is very small, introducing extra delay for charging the output stage. On the other hand, if the second stage carries a very large current, the delay of the second stage approaches that predicated by small signal analysis. The size of the offset voltage also has some effect on the second stage. If the offset voltage is large, the drain source voltage over the transistor becomes small. This pushes the transistors in the second stage towards the linear region and increases speed due to the lower Miller capacitance at the cost of lower gain.

The input stage of the ring amplifier experiences less slewing. The width of the transistors in the input stage are most probably not set by slewing requirements but rather

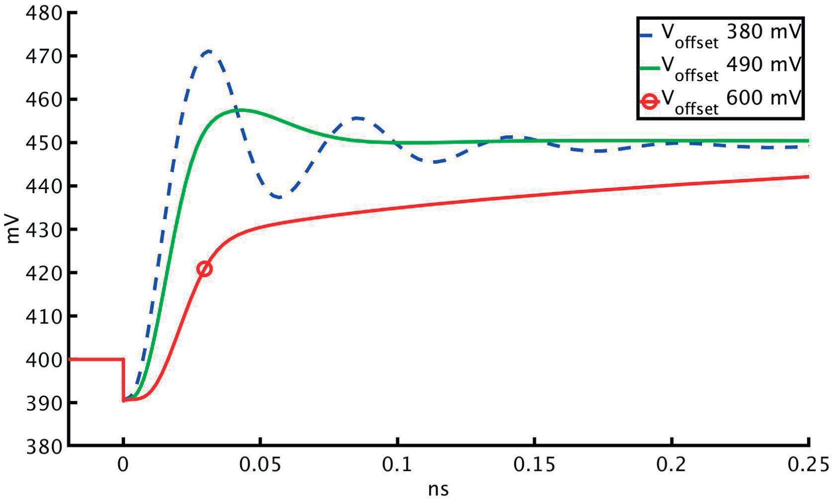

Figure 3.9: Transient simulation of ring amplifier with varying offset voltage.

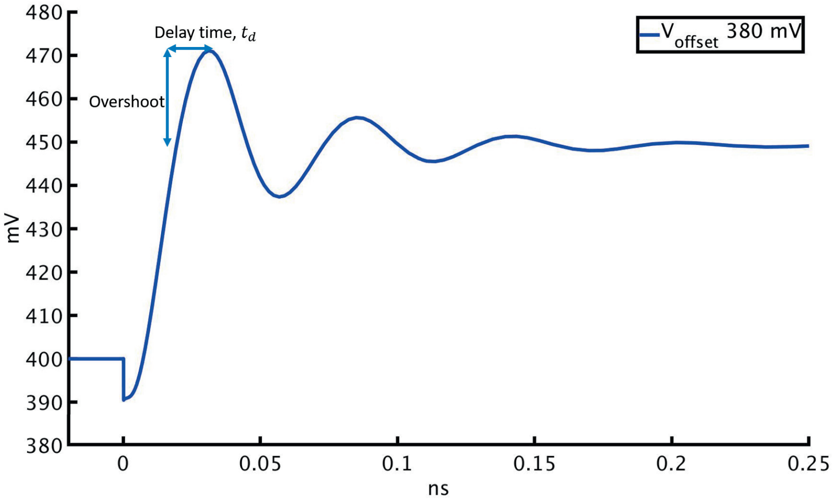

Figure 3.10: Illustration of overshoot in ring amplifier.

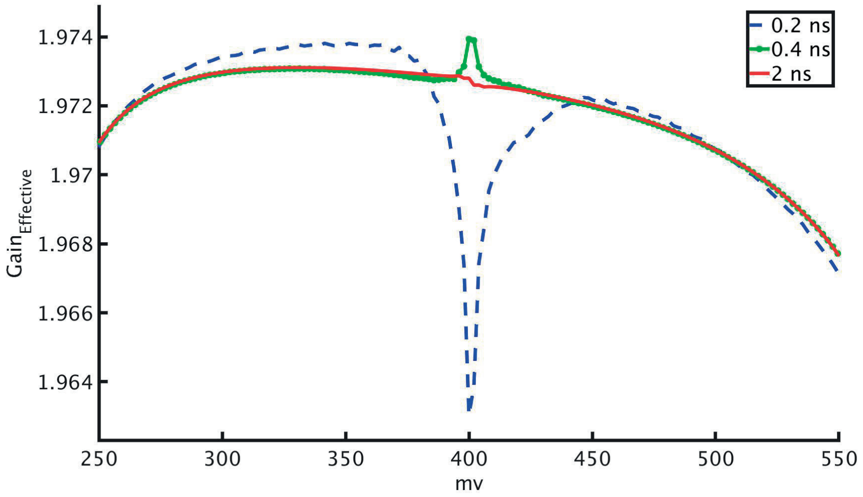

Figure 3.11: Effective gain of ring amplifier versus input voltage, plotted at different times.

by noise constraints. The input referred noise of the amplifier is

$$\bar{v_{n,in}}^2 = \frac{1}{\beta}\frac{4kT\gamma}{g_{m(in)}} * BW \tag{3.6}$$

where $g_{m(in)} = g_{m(p)} + g_{m(n)}$, BW denotes the bandwidth of the ring amplifier and β is the amplifier the feedback factor. The ring amplifier can be said to have noise filtering properties. When the ring amplifier is fully settled the output transistors is in weak inversion and their bandwidth is low. A larger offset voltage give rise to a lower bandwidth and hence filter more noise.

Fig. 3.11 illustrate how the settling of the ring amplifier is affected by the output amplitude of the ring amplifier. The x axis shows the input voltage and the y axis shows output voltage divided by the input voltage sampled at a specific time $0.2ns$, $0.4ns$, $2ns$. This is denoted the effective gain. The feedback factor is approximately $1/2$. Interestingly, the ring amplifier settles slower for smaller input amplitudes (V_{in} near common-mode level, 400mV). This appears to be a result of two effects. First, if the input amplitude is small, the ring amplifier will not go into slewing and will have to transverse the deadzone for a longer time before finally settling. Secondly, the fully settled ring amplifier resides were closed to common mode bandwidth is at its lowest.

It's observed in [13] that the ring amplifier settles faster when configured with a lower feedback factor. If the feedback factor decreases from 1 to $1/2$, the designer can choose to either increase the width of the transistors in the output stage or decrease the offset voltage, v_{offset}. If the transistors in the output stage is increased, the time the ring amplifier spend in slewing is decreased, leading to somewhat faster settling of the ring amplifier.

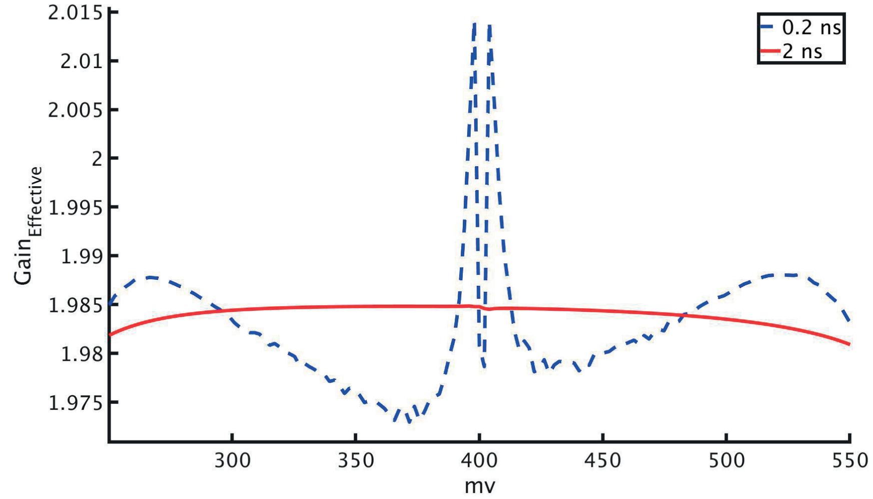

Figure 3.12: Effective gain of ring amplifier versus input voltage, plotted at different times.

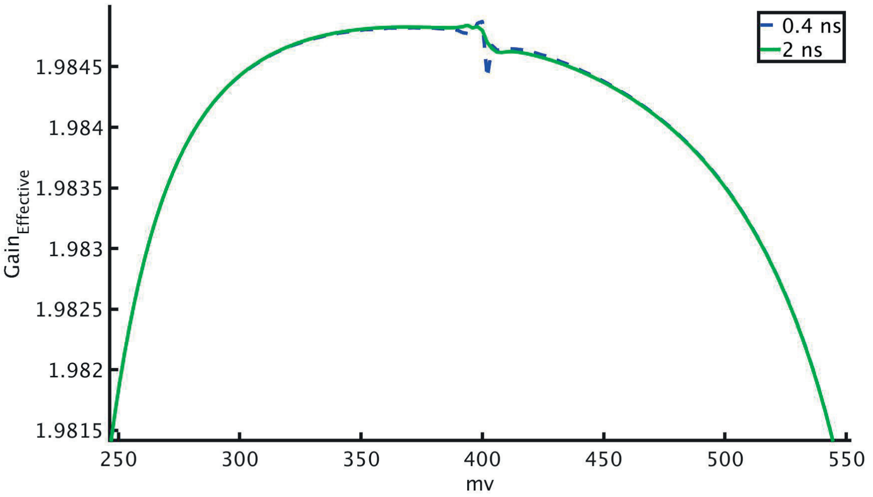

Figure 3.13: Effective gain of ring amplifier versus input voltage, plotted at different times.

3.3 Design methodology

From the discussion above, it's possible a propose a design methodology for the ring amplifier in Fig. 3.3. The central idea behind this method is to try to isolate the trade-off between the *width* of the output transistors and the offset voltage, V_{offset}, since the output stage give rise to the complicated nonlinear behaviour. The way to do this is to start out with large transistors in stage one and two. Then, the *width* of the output transistors and the offset voltage are empirically changed until a good transient response is obtained. The transistors in stage one and two can then be scaled down until a satisfactory trade off between power and settling speed is reached. The recommended design stages is listed beneath, in chronological order. Another design methodology is presented in [14]. It's assumed that the length L of the transistors is set to the minimum size allowed by the technology, in order to maximize the ring amplifier slewing and bandwidth properties. If the ring amplifier is designed to operate at low speed with high gain, the transistor length could be increased.

One, choose the width of transistors at the input stage such that the noise constraint is satisfied, eq 3.6.

Two, choose the width at the second stage such that large current goes through the second stage.

Three, select the value of the common mode feedback capacitor (Fig. 3.21) and place it in parallel with the load capacitor

Four, select a reasonable width of the output transistors given the capacitive load. Sweep the resistor R using a transient simulation. If the slewing phase consume a large part of the total settling time (slewing + stabilization), increase the *width* and sweep the resistor again. If on the other hand the slewing phase is very short and the oscillator decaying slowly, reduced the *width* and sweep the resistor again. Iterate in this way until the ring amplifier settles quickly.

Five, scale down the size of the transistors in the second stage until a satisfactory compromise between power and settling speed is reached, also using transient simulations.

3.4 Circuit topologies

While the core of the ring amplifier remains relatively unchanged, modifications have proposed in order to tackle gain, linearity and improve the PVT robustness.

3.4.1 Anti parallel pair

One attempt to boost the speed of the ring amplifier have been proposed in [15], [16]. It is suggested that the resistor can be replaced by the anti parallel pair in Fig. 3.14. During

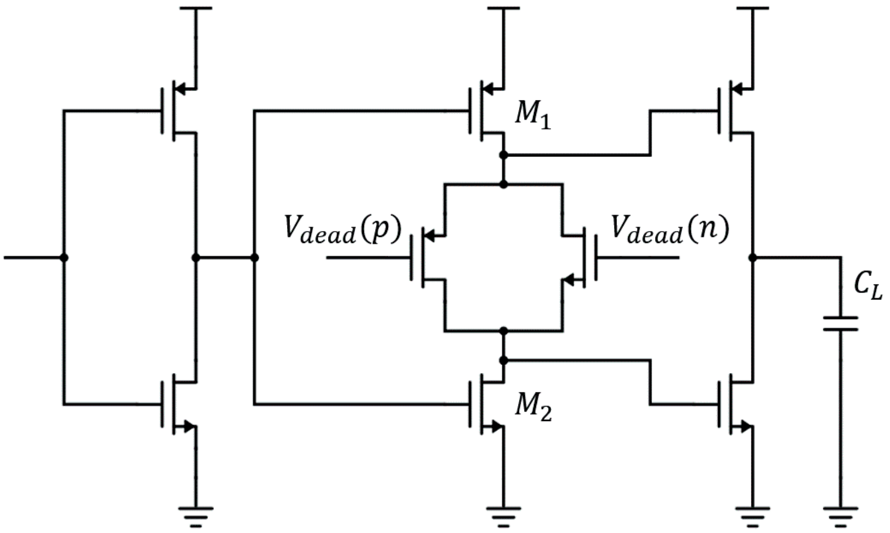

Figure 3.14: Ring amplifier with anti parallel arrangement.

the slewing phase, one of the transistors is turned off and the other enters the linear region, which provides a low resistance during the slewing phase. During the stabilization phase, the anti parallel pair enters saturation and the anti parallel pair resembles a battery [15], giving rise to a DC offset between v_p and v_n, that are in the ideal case transparent from a AC prospective. The AC transparency of the battery is beneficial from a zero, pole perspective [15]. In practice the resistance $1/g_m$ might be approximately equal to the value of the resistor. In addition, the *CMOS* transistor have a relatively large parasitic capacitance compared with polysilicon resistors [15], [16], reducing the speed advantage given by the anti parallel pair. The remaining main benefit of the anti parallel pair is that the offset can be tuned by changing the bias on, $V_{dead(p)}$ and $V_{dead(n)}$. The anti parallel pair can also be used to power down the second stage.

3.4.2 Bias enhancement

The output transistors of a ring amplifier is biased in weak inversion and is therefore often the largest transistors in a ring amplifier. Consequently, the load seen by the transistors in the second stage is larger than the load seen by the first stage, resulting in the pole of the second stage being located lower in frequency than the pole of the first stage. Bias enhancement aims to raise the pole of the second stage to a higher frequency by increasing the voltage overdrive of the transistors in the second stage, [17]. One way of implementing an bias enhanced ring amplifier is illustrated in Fig. 3.15, where a resistor, R, has been inserted between the transistors, M_1 and M_2. Bias enhancement has several effects. When the overdrive voltage of M_3 and M_4 is increased, the transistor approaches the linear region and the gain is reduced. The higher overdrive also enables to reduce the *width* for a certain current for M_3 and M_4. This leads to higher f_t due to lower capacitance, reducing

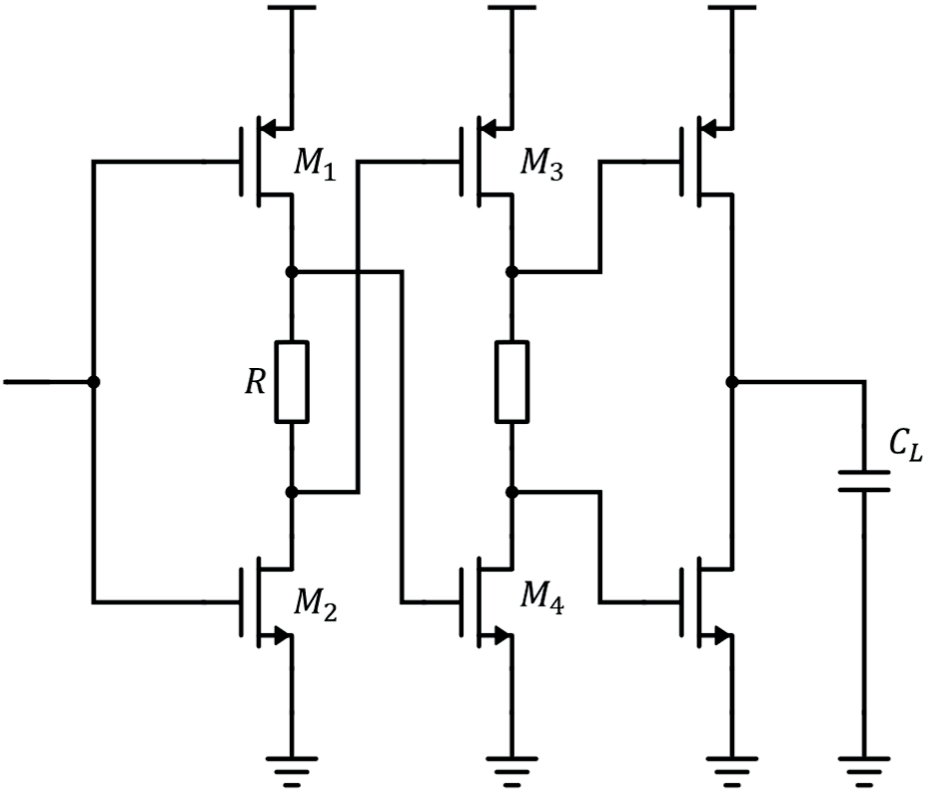

Figure 3.15: Implementation of ring amplifier with bias enhancement.

the troublesome gate to drain capacitance, C_{gd}. These two facts lead to decreased Miller capacitance. For the specific implementation in Fig. 3.15, the source drain voltage of the transistors in the first stage is reduced, resulting in lower output resistance, leading to lower gain. A transient simulation with and with out bias enhancement is shown in 3.16. The circuit is identical with the exception of the bias enhancement. Bias enhancement should be employed improve the settling speed at the expense of gain.

3.4.3 Dual dead zones

As discussed above, large output transistors lead to faster slewing. The down side of larger output transistors is that the overshoot increases and consequently, the offset voltage have to be increased to maintain stability. This leads to slower settling when the input voltage approaches common mode. This trade off can partly be alleviated be introducing the dual dead zone ring amplifier [18], Fig. 3.17. Here, the high voltage transistors are active during the slewing phase to provide most of the current for the load. During the stabilization phase, the high voltage transistors are essentially turned off and the low voltage transistors continue to be active and ensuring that the ring amplifier has a moderate

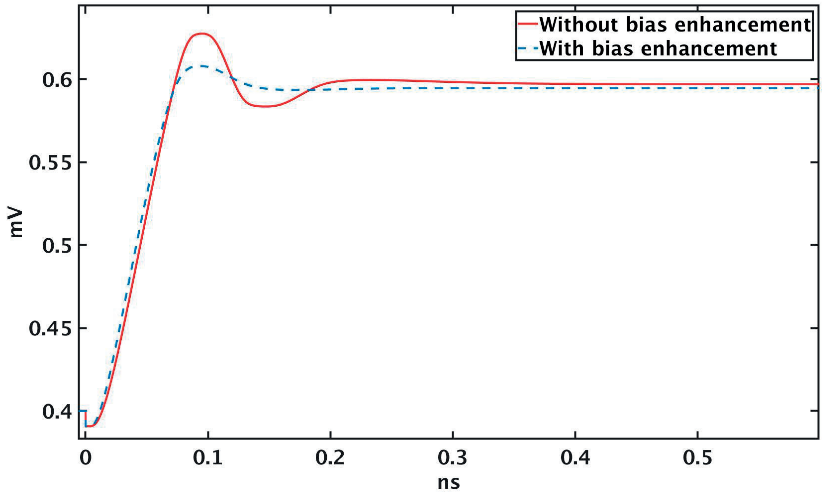

Figure 3.16: Transient of ring amplifier with and without bias enhancement.

bandwidth as the input voltage approach common mode.

Another way of looking at the dual dead zone ring amplifier is to look at the current through the ideal voltage source plots, 3.7. The dual dead zone concept gives an additional degree of freedom to tune these curves and in this way boost the settling speed of the ring amplifier. This is what is depicted in Fig. 3.18, where the solid curve is without dual dead zone and the dashed includes it. To increase the bandwidth close for inputs near common mode, a small extreme low vth transistor is added shown in the dotted curve, Fig. 3.18. For highly scaled processes, the dual dead zone will most likely not improve the performance substantially since the transistor have relatively high bandwidth in weak inversion, but it is a very attractive approach for long channel devices [18].

3.4.4 Cascoded dead zones

It can be observed that the unit gain bandwidth, ω_{UGB} (repeated below for convenience) doesn't depend on the output resistance

$$\omega_{UGB} = \frac{A_1 * A_2 * g_m}{c_L} \tag{3.7}$$

Consequently, the output resistance can be boosted to get more gain without affecting the AC stability of the ring amplifier. One way of boosting the output resistance can be found in Fig. 3.19, where the output stage has been stacked with cascodes. This increases the gain from three to four times the intrinsic gain of the transistor. However, two disadvantages are identified. Firstly, the bias voltage v_{bias} limits the gate source voltage over the transistor M_2 and M_3 to $vdd - v_{bias}$ and v_{bias}. This will limit the slew rate during the slewing phase of the ring amp. Secondly, the output voltage head room has to be lowered if good linearity is to be maintained.

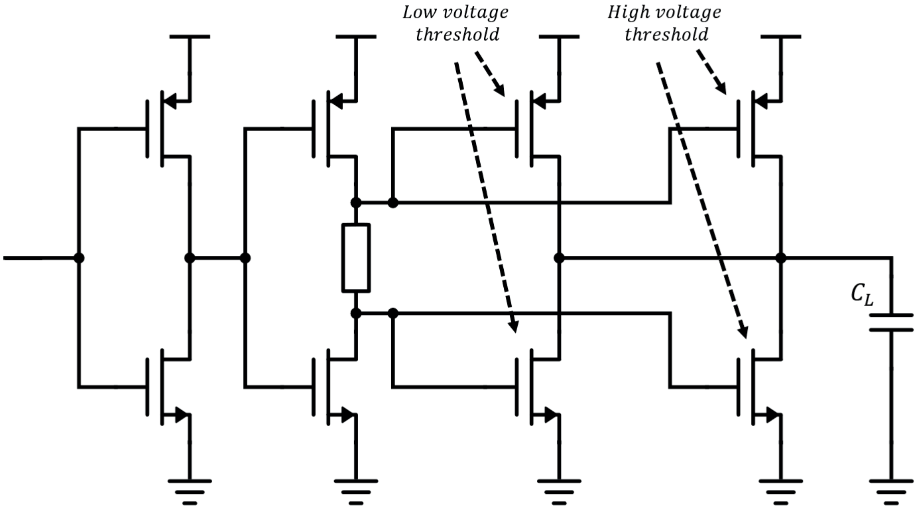
Low voltage threshold
High voltage threshold
C_L

Figure 3.17: Dual dead zone ring amplifier.

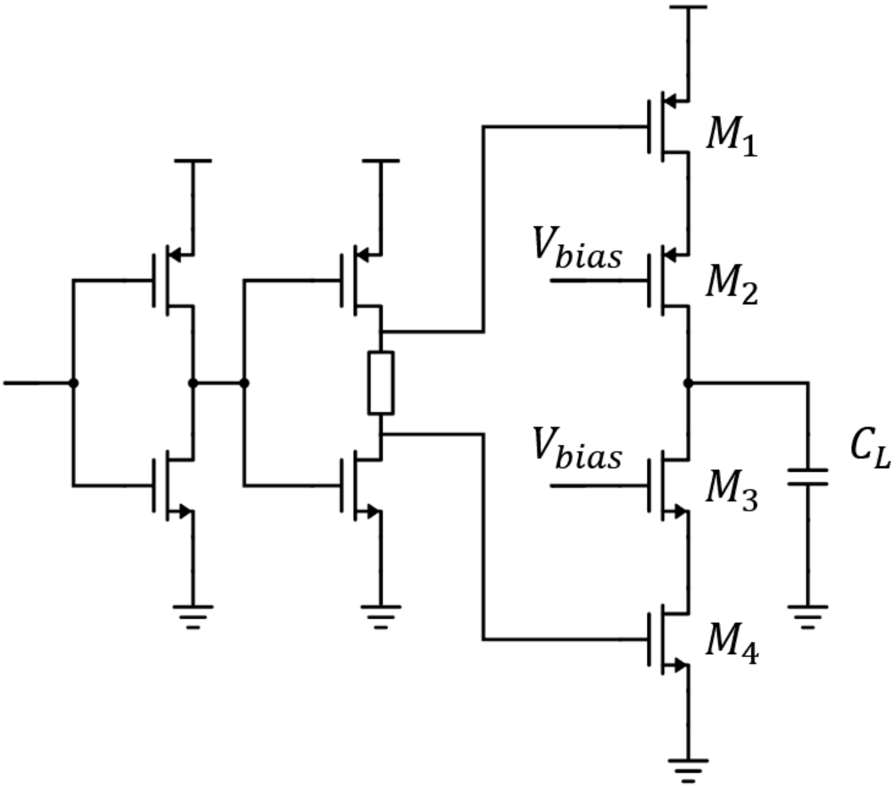
M_1
V_{bias}
M_2
V_{bias}
M_3
C_L
M_4

Figure 3.19: Ring amplifier with boosted output resistance.

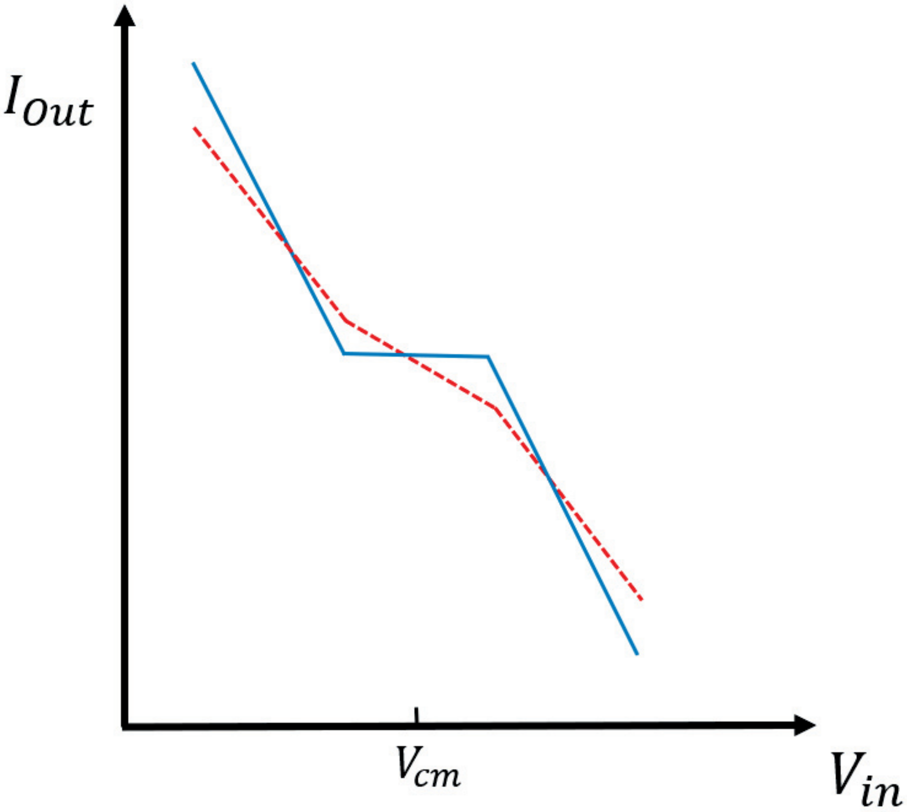

Figure 3.18: Sketch of how the ring amplifier dynamic can be changed using the dual dead zone concept.

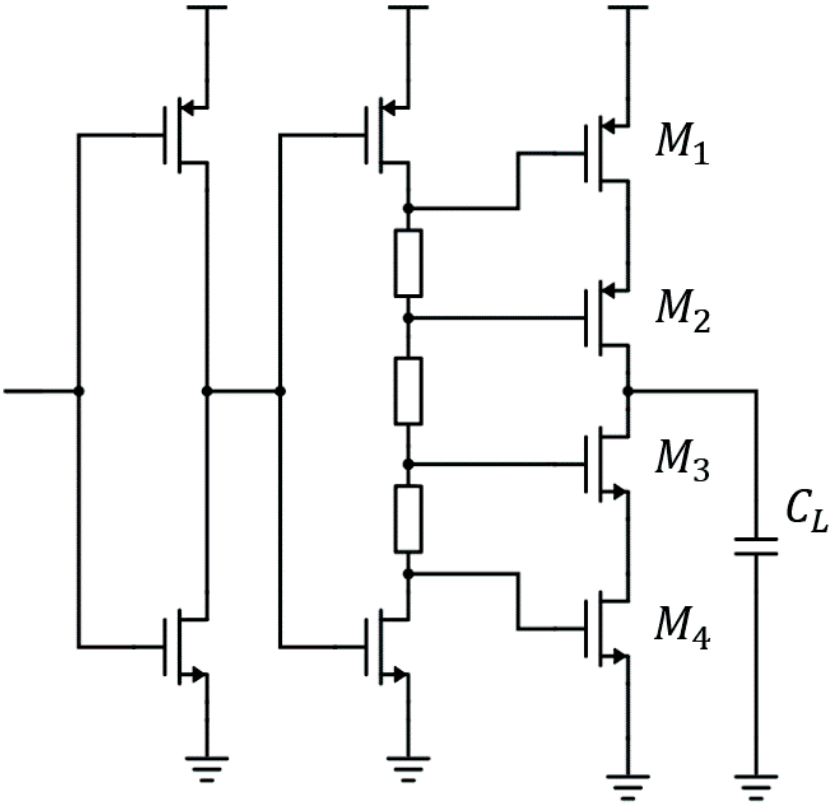

Figure 3.20: Ring amplifier cascoded dead zones.

The slewing limitation of the circuit in Fig. 3.19 can be partly be alleviated by introducing the cascoded deadzone ring amplifier [19], Fig. 3.20. This allows the gate source voltage over M_2 and M_3 reach almost vdd. Greatly boosting the slewing properties compared with the ring amplifier in Fig. 3.19. The circuit is also self biased.

3.4.5 Fully differential ring amplifier

The ring amplifiers discussed so far are single ended and thus suffer from the limitations associated with other single ended circuits, e.g. no suppression of even-order harmonics, no supply noise rejection and lack of inherent common mode rejection. These limitations can partly be alleviated by designing a pseudo differential ring amplifier, Fig. 3.21. The right side of the picture shows the feedback network for common mode and differential input signal during the amplification phase, where c_s are the capacitors for sensing the common mode level. The differential and common-mode gain are given by

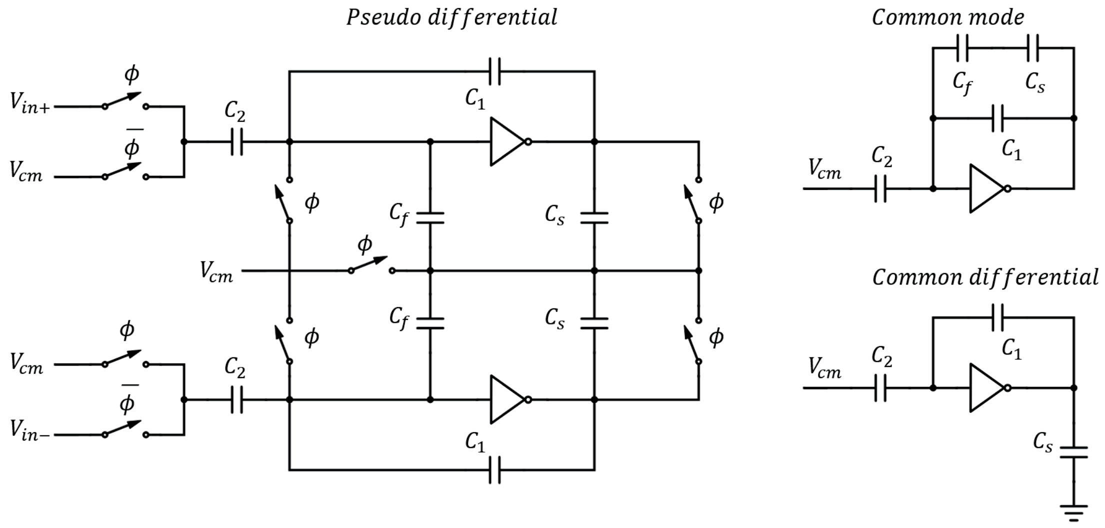

Figure 3.21: Pseudo differential ring amplifier. The inverter in the figure denotes a single ended ring amplifier.

$$A_{Differential} = \frac{C_2}{C_1} \tag{3.8}$$

$$A_{Common} = \frac{C_2}{C_1 + \frac{C_s C_f}{C_s + C_f}} \tag{3.9}$$

Ideally, the common mode gain including the feedback should be zero. In order to achieve a good common mode rejection, this requires C_f and C_s to be several times larger than C_1 as seen in, eq 3.9. This relationship makes it very hard to obtain good performance and fast settling for both the common mode and differential mode.

The fully differential ring amplifier in Fig. 3.22 solve the limitations associated with single ended ring amplifiers [20]. The transistors M_1 and M_2 is responsible for reducing the common mode gain of the first stage. The common mode feedback is applied to the transistor M_3. A differential input signal sees essentially a current starved inverter. Naturally the transistors M_1, M_2 and M_3 occupies some voltage headroom, lowering the gate source voltage over M_1, M_2, M_3 and M_4. This decreases f_t, lowering the bandwidth of the input stage and consequently the speed of the whole amplifier. From a noise perspective, the lower overdrive over M_1, M_2, M_3 and M_4 is beneficial as the transconductance increases.

3.4.6 Four stage ring amplifier

In high precision SAR ADCs, conventional ring amplifier don't have sufficient gain to meet the very stringent linearity requirements, [21], [18]. The cascaded ring amplifier offers high gain but limits the output voltage range due to the stacked output transistors.

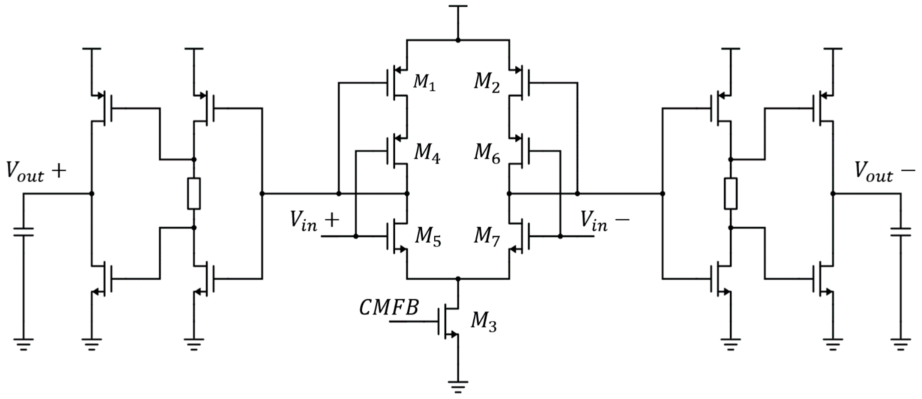

Figure 3.22: Fully differential ring amplifier

A four stage ring amplifier has been proposed in [21], which is capable of operation with almost rail to rail output voltage. The four stage ring amplifier introduces new problems. The delay time, t_d, increases due to the extra added stage, leading to slower settling. Another problem with the four stage ring amplifier is the risk of latching due to the positive common mode gain of the amplifier.

3.5 Continuous time ring amp

A valid question is if the ring amplifier can be used in continuous time applications. As previously mentioned, the output stage of the ring amplifier can only deliver a small amount of current to the load. If a sufficiently small resistive load is connected at the output, the ring amplifier will be forced into slewing in order to supply enough current. This will render the ring amplifier useless for almost all applications. It has been proposed [22] that the offset could be moved from the second stage to the first stage, Fig. 3.23. If the input voltage changes slowly, such that the second stage can charge the compensation capacitor, C_c without going into slewing, it is likely that this topology works well with high linearity.

3.6 PVT

Ring amplifiers are in general considered to be quite robust against PVT changes, [20], [23], [24]. The most important aspect to consider when designing a PVT robust ring amplifier is to ensure that the offset voltage, $v_{offset} = v_p - v_n$ is kept constant with regard to PVT changes [24], see Fig. 3.24. The offset voltage is measured as the difference between v_p and v_n. The offset is the compared to a offset reference and fed into an amplifier biasing $V_{bias(p)}$ and $V_{bias(n)}$, all using a replica circuit. One drawback with this approach is that the current starving reduces the slewrate and bandwidth of the second stage, limiting the speed. In addition, it is important to ensure that the ring amplifier is biased in the high gain region under PVT changes using for example auto zeroing.

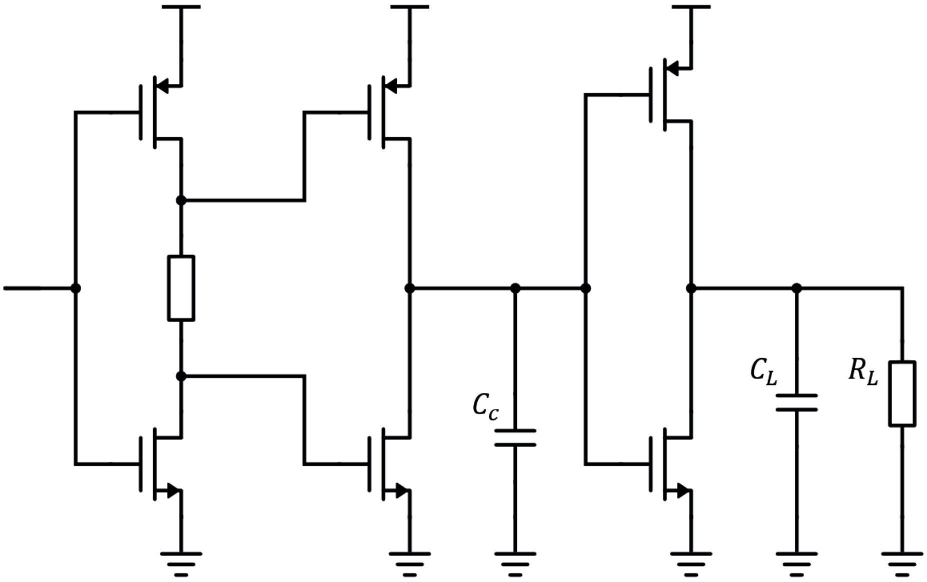

Figure 3.23: Ring amplifier for time continuous applications, capable of driving resistive loads without entering slewing

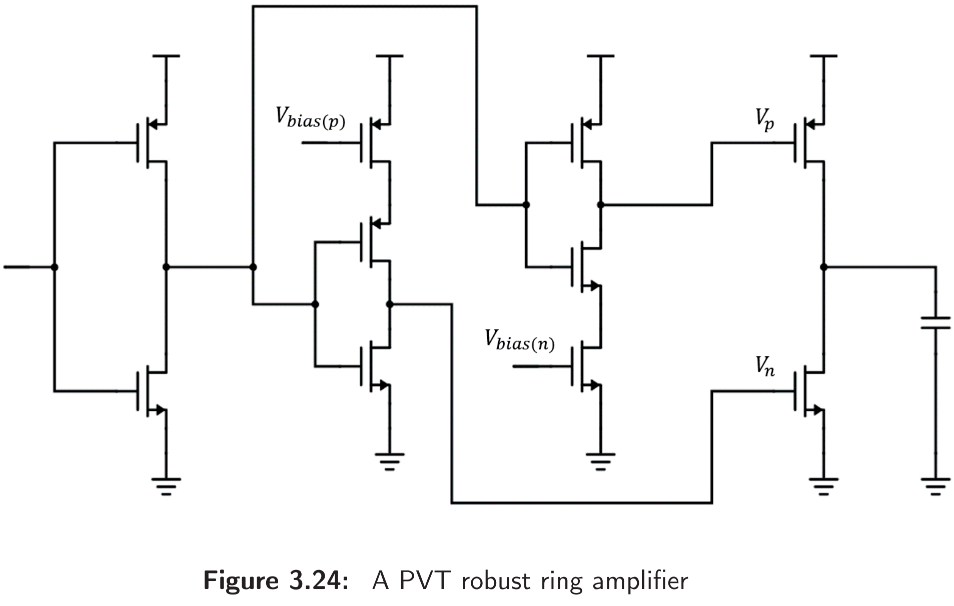
$V_{bias(p)}$
$V_{bias(n)}$
V_p
V_n

Figure 3.24: A PVT robust ring amplifier

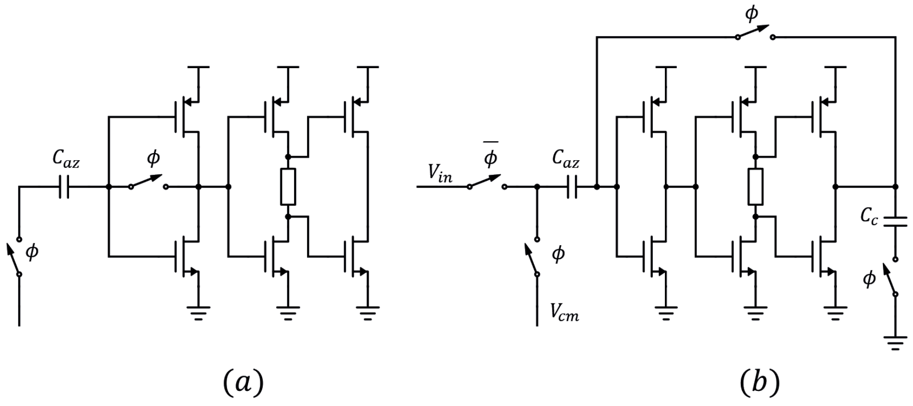

Figure 3.25: Two auto zero schemes

3.7 Auto zero

Auto zeroing of ring amplifiers poses new problems. If the feedback factor is low, the ring amplifier could potentially start to oscillate during the auto zero phase, when the feedback factor is changed to one. Even if the feedback factor is close to one during the amplification phase, i.e $1/2$, the ring amplifier might perform poorly during the auto zero phase. If the ring amplifier is stable during the auto zero phase, it might require longer time to stabilize during the auto zero phase then the amplification phase. Two schemes have been proposed to tackle this, see Fig. 3.25. The first idea [12] suggests to only auto zero the first stage, see Fig. 3.25a. During auto zero phase, the offset of the input stage is sampled on C_{az}. The second scheme in Fig. 3.25b proposes to connect a compensation capacitor C_c during the auto zero phase to keep the loop stable. The compensation capacitor is then disconnected during the amplification phase to avoid a reduction in speed.

The charge is stored on the capacitor C_c from cycle to cycle, speeding up the auto zeroing phase and reducing power consumption, as the capacitor is connected again. The biggest drawback with this compensation scheme is the required size of C_{az} and C_c. In particular if the feedback factor is small, the sum of C_{az} and C_c needs to be large to keep the unity gain bandwidth the same and ensure stability. The relationship between the required size of the capacitors C_{az} and C_c with C_L is given by eq 3.10. If the feedback factor is small, the auto zero scheme in Fig 3.25 b give rise to a significant area penalty.

$$B(C_{az}+C_c) \approx C_L \tag{3.10}$$

3.8 FOM

Design of ring amplifiers is associated with tradeoffs that are relatively straight forward such as size of the input transistors and the noise of the ring amplifier. Other design tradeoffs are considerably “murkier”. One example is the trade off between noise and linearity due to changing the offset voltage. This makes it hard to compare ring amplifiers operating with different speed, noise and distortion. One way to tackle this could be to introduce a figure of merit. It's here proposed to use a slightly modified Schreier figure of merit for the ring amplifier. Unlike the conventional Schreier figure of merit, the power is not the power of the entire design but rather the power delivered to the capacitive load, P_L. If the design operates well below the speed limit of the technology, $P = f_s \times E$ will be satisfied. If it is assumed that the first stage consumes the majority of the power and that the ring amplifier is limited by thermal noise, adding 6 dB to SNR will require a quadrupling of the power consumption. This is consistent with the Schreier figure of merit and makes this figure of merit somewhat based on fundamental physics. This figure of merit for could be used as guidance for deciding the operating speed for ring amplifiers.

$$FOM_s = SNDR + 10\ log_{10}\left(\frac{f_s/2}{P_L}\right) \tag{3.11}$$

Chapter 4

Proposed ring amplifiers

This chapter introduces two ring amplifiers that aims to boost settling speed.

4.1 Split input ring amplifier

In situations where speed is paramount, gain is of less importance and a low feedback factor is used. It would be advantageous if bias enhancement could be utilized in fully differential ring amplifiers. Unfortunately, the input stage of a fully differential ring amplifier does not have the voltage headroom to accommodate bias enhancement, if it is to be implemented similar to as in Fig. 3.15. Instead, it is proposed to split the input stage of the ring amplifier in two. In this way the voltage at the nodes V_{out1} and V_{out2} can be designed with different bias voltages, see Fig. 4.1, ensuring a suitable overdrive for the transistors in the second stage.

The split input stage also provides means for making the ring amplifier more robust during PVT changes. The offset voltage can be held constant under the influence from PVT variations, by selecting an appropriate overdrive for the transistors in the second stage. In practice, this can be done by introducing a variable offset in the common mode feedback path, controlled through $CMFB(p)$ and $CMFB(n)$. This can be done using a replica circuit of the first and second stage. The offset voltage is measured and compared with a target offset voltage and the resulting error signal is fed to an amplifier. The resulting output voltage from the amplifier is then added as an offset between $CMFB(p)$ and $CMFB(n)$ in the common mode feedback path. This approach to a PVT robust ring amplifier comes with several advantages over the PVT robust ring amplifier proposed in [24] and discussed in chapter 3. It eliminates the needs for extra stacking in the second stage, greatly boosting its speed and slewing properties. Since the offset voltage is proportional to the current in the second stage, the split input ring amplifier also ensures that the current through the second stage is kept constant.

4.2 Complementary differential pair ring amplifier

The complementary differential pair ring amplifier is an attempt to design ring amplifier that has all the speed advantage of a single ended ring amplifier but still has some inherent common mode rejection. The proposed ring amplifier is shown in Fig. 4.2. The design

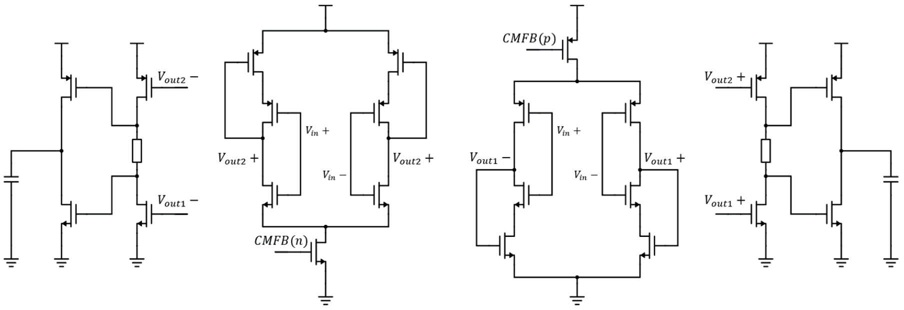
V_{out2} −
V_{out1} −
V_{in} +
V_{out2} +
V_{in} −
V_{out2} +
$CMFB(n)$
$CMFB(p)$
V_{out1} −
V_{in} +
V_{in} −
V_{out1} +
V_{out2} +
V_{out1} +

Figure 4.1: Split input ring amp

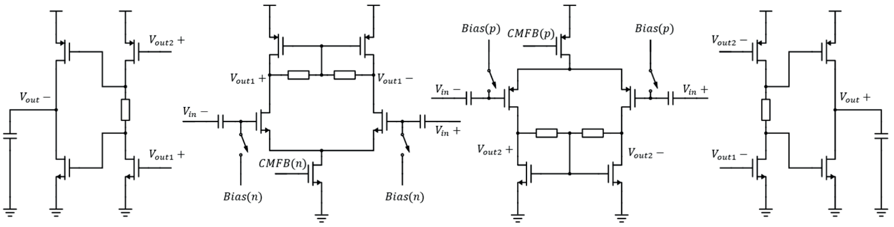
V_{out2} +
V_{out} −
V_{out1} +
V_{out1} +
V_{out1} −
V_{in} −
V_{in} +
$CMFB(n)$
$Bias(n)$
$Bias(n)$
$Bias(p)$
$CMFB(p)$
$Bias(p)$
V_{in} −
V_{in} +
V_{out2} +
V_{out2} −
V_{out2} −
V_{out1} −
V_{out} +

Figure 4.2: Complementary differential pair ring amplifier

is similar to the split input ring amplifier, but the inverter in the input stage is replaced by a complementary differential pair. The capacitors on the input stage is used to rise the input voltage over the *nmos* transistors and lower the input voltage over the over the *pmos* transistors. This is done during the sampling phase. In this way, all the transistors can be biased in the active region. This comes with two drawbacks, the differential pair have a higher noise contribution for a given amount of current in comparison to the inverter. In addition, the differential gain is approximately a factor of two lower for the same current.

Chapter 5

Pipeline assisted ring amplifier based high speed SAR ADC

This section describes the ADC and its various parts with emphasis on the ring amplifier. An existing non-pipelined asynchronous SAR ADC, designed in $FDSOI$ 22, was used as a platform for evaluating the ring amplifier as a pipeline amplifier. Many components were stripped from this design to design the pipeline assisted ring amplifier based SAR ADC. In the rest of this report, the ADC will be referred to as Ericsson's conventional SAR ADC. The architecture of the pipline SAR ADC is shown in Fig. 5.1, the actual implementation is fully differential.

5.1 CDAC stage 1

The common mode switching schemes is used, described in chapter 2. The DAC capacitances are binary weighted as $64fF$, $32fF$, $16fF$, $8fF$, $8fF$. The total capacitive load of the CDAC equals $128fF$. The switches where taken from Ericsson's conventional SAR ADC, these switches include logic ensuring that there is no overlap between v_{cm}, v_{refp} and v_{refn}. The n reference voltage, V_{refn} is $150mV$ and the p reference voltage, V_{refp} is $650mV$. Consequently, the maximum allowed peak to peak differential input voltage is 1 V. Furthermore, $200ps$ is allocated for the CDAC sampling phase.

5.2 CDAC stage 2

The CDAC of the second stage also uses the common mode based switching scheme. The capacitances are binary weighted as $16fF$, $8fF$, $4fF$, $2fF$, $2fF$. The total capacitive load of the CDAC equals $32fF$. The n reference voltage, V_{refn} is $150mV$ and the p reference voltage, V_{refp} is $650mV$.

5.3 Comparator

The comparator in the Ericsson's conventional SAR ADC was used. Unfortunately, the comparator suffers from large kickback effects, ruining the performance of the pipelined SAR ADC. The kickback was reduced by reducing the sizes of the input transistor from

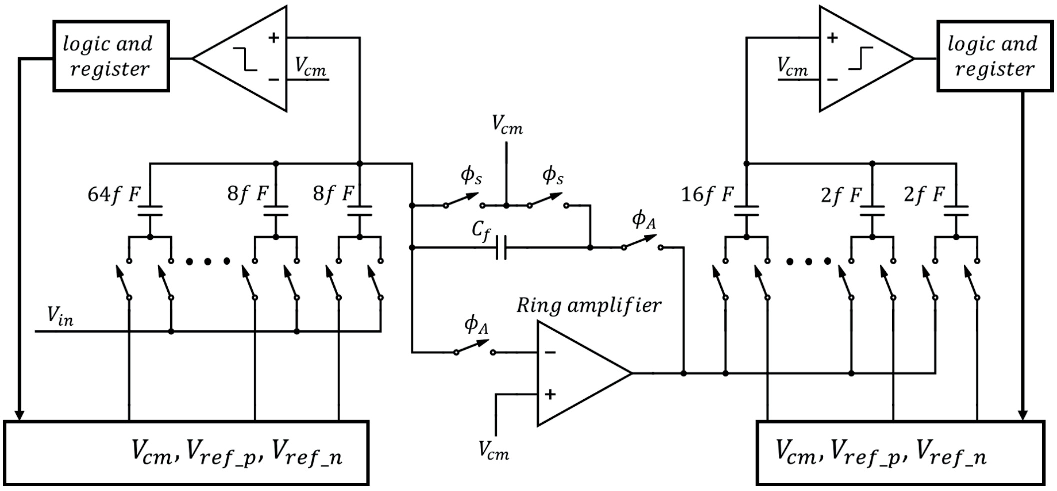

Figure 5.1: ADC architecture. Actual implementation is fully differential

$W = 4\mu$ and $L = 50n$ to $W = 0.8\mu$ and $L = 20n$. This increased the decision time of the comparator with approximately $8ps$. The decision time of the modified comparator is approximately $55ps$. This comparator is used in both the first and second stage. When the ADC operates at a sample rate of $550MHz$ the combined power consumption of both the comparators is $1.4mW$.

5.4 Logic and register

The logic and register are implemented in verilogA code, the code can be found in appendix. The logic and register block are implemented to emulate asynchronous operation. Some effort was put in to ensure that the verilogA code have realistic latency by examining the logic and registers of Ericsson's conventional SAR ADC. Similarly, by studying Ericsson's conventional SAR ADC it was concluded that the ADCs logic and register consumes $1.7mW$ when operated at $550MHz$.

5.5 Ring amplifier

The split input ring amplifier is used as residue amplifier. The complementary differential pair ring amplifier was not considered, since the gain is too low to properly rail the internal nodes V_p and V_n with the low feedback factor, leading to a poor trade-off between speed and noise. Super-low threshold voltage devices are used trough out the design, prioritizing speed over gain. Bias enhancement was not used in the second stage, instead gain is prioritized over speed. The table below summarizes some of design parameters. The length of the transistors refers to the length of the transistors in the inverters, not in the common mode feedback transistors. The second stage consumes a relatively large current to boost speed. A relatively large offset voltage, $430mV$ is chosen, this reduce the

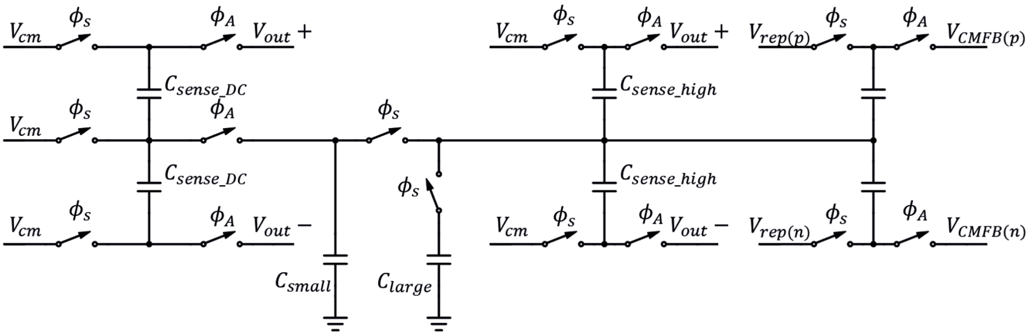

Figure 5.2: Common mode feedback network

source drain voltage for the transistors in the second stage. The result is that the second stage only has approximately half the intrinsic gain, i.e. 5. The relatively large offset voltage is chosen to suppress noise and overshoot. The differential gain of the ring amplifier is approximately 900. The ring amplifier in feedback configuration should have a gain of 32. Since the load of the entire CDAC of stage one is $128fF$, the feedback capacitor should be $4fF$. This is however only true if the gain of the ring amplifier is sufficiently large. With the low gain of the ring amplifier used, a somewhat lower feedback capacitor, $3.6fF$, was implemented.

	ring amplifier design parameters		
	stage 1	stage 2	stage 3
Width p	6μ	1.36μ	2.997μ
Width n	6μ	0.99μ	2.997μ
Length	$20nm$	$20nm$	$20nm$
current	$207\mu A$	$240\mu A$	$23\mu A$
gain	12	5.1	14.5

The common mode feedback part of the ring amplifier is shown in Fig. 5.2. The CMFB has two paths. A low frequency switched capacitor path and a high frequency path. The low frequency switched capacitor path measures the common mode voltage over the capacitors $c_{senseDC}$ during the amplification phase. The sampled common mode voltage is sampled on the capacitor c_{small}. During the sampling phase of the ring amplifier the $c_{senseDC}$ is reset and the charge on c_{small} is transferred to c_{large}. It is essential that ratio between the small and large capacitor is sufficiently large, to ensure convergence. In this implementation the small capacitor is set to $4fF$ and the large is set to $40fF$. The high frequency path measures the common mode voltage of the capacitor, $c_{senseHigh}$. The two capacitors to the right in figure 5.2 ensure that there is an offset between $CMFB(p)$ and $CMFB(n)$, to be held constant as described in chapter 4, using a replica circuit. The common feedback circuit also ensure that the ring amplifier is biased in a high gain region. The ring amplifier is powered down when not used, the duty cycle is 0.275 and the average power consumption is $120\mu W$. It is important to note that the ring amplifier performance is extracted from schematic level simulations.

The following plots show the transient response of the ring amplifier used in the ADC.

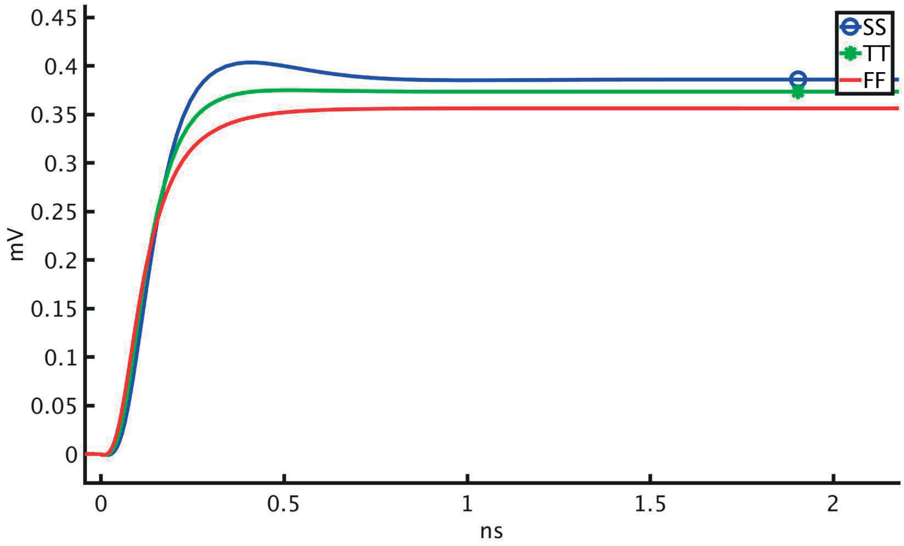

Figure 5.3: Ring amplifier transient response of the slow slow, fast fast and typical typical corners

The differential output is plotted on the x axis for various corners. Fig. 5.3 shows the transient response of the slow-slow (SS), fast-fast (FF) and typical-typical (TT) corners. The gain of ring amplifier in the SS corner is 1600, almost twice as high as the gain in the TT corner (900). This in combination with somewhat slower transistors give rise to a somewhat under-damped response. The lower gain in the FF corner results in an over-damped response. Fig. 5.4 compares the fast-slow (FS) and slow-fast (SF) corners with the TT corner. The reason that the SF (slow nmos, fast pmos) slews significantly faster than the other cases is that the output voltage increases and the fast pmos device is turned on during the slewing phase. Fig. 5.5 shows the transient response for different temperatures. The final output voltage change with approximately 8 percent for a temperature range of -20 to +90. Fig. 5.6 shows the ring amplifier transient response with various supply voltage levels. Fig. 5.7 features what is probably the worst corner. In this corner the ring amplifier needs 1.2 ns for settling within 1 mV for the final output value and approximately 2.2 ns to settle fully.

5.6 Result, typical-typical

Fig. 5.8 and 5.9 show how *SNR* and *SFDR* are affected by incomplete settling of the ring amplifier. The x axis shows how long the amplifier is active in nano seconds and the y axis shows the corresponding *SNR* and *SFDR*. The plots in 5.8 and 5.9 do not include any noise sources. The plots are decimated to 256 FFT points and are simulated under TT conditions. Fig. 5.10 shows the output spectrum of the ADC, including noise sources. Clock jitter is not included in any of the simulations. The ring amplifier has been given 500 *ps* to perform the amplification in 5.10. Under TT conditions the ring

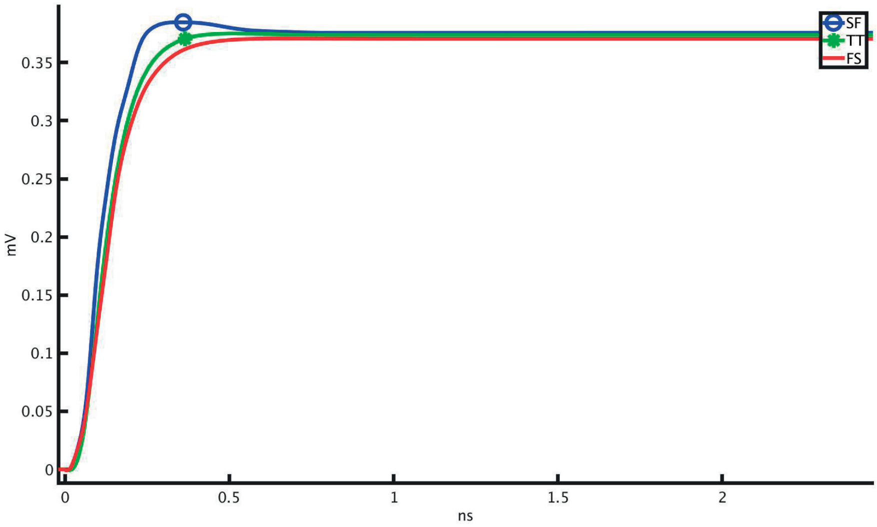

Figure 5.4: Ring amplifier transient response of the slow fast, fast slow and typical typical corners

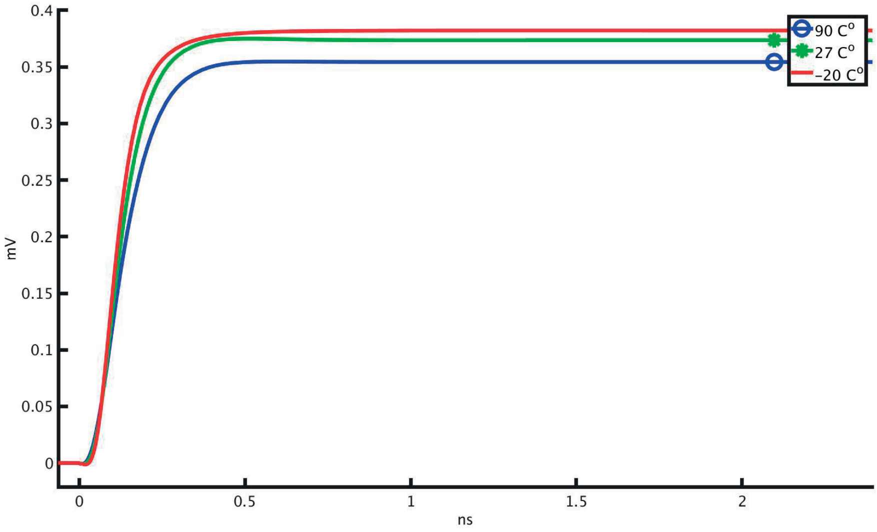

Figure 5.5: Ring amplifier transient response for various temperatures

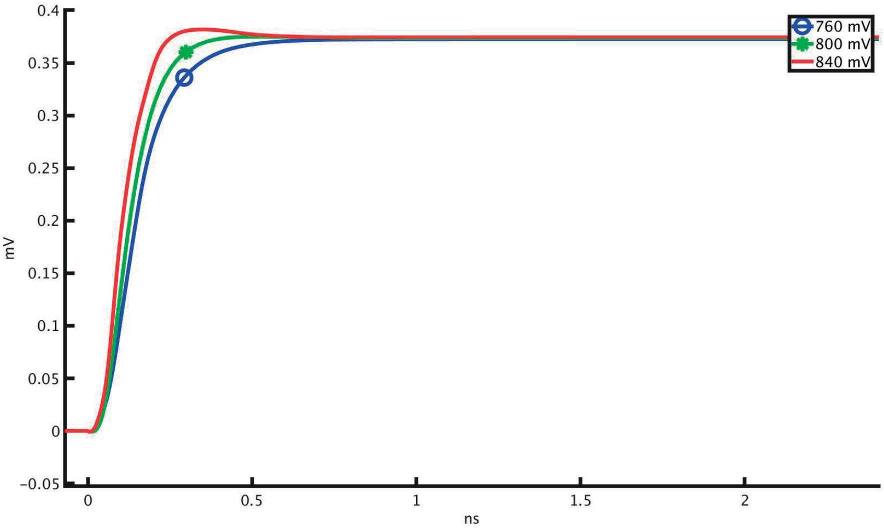

Figure 5.6: Ring amplifier transient response with different supply voltage variations

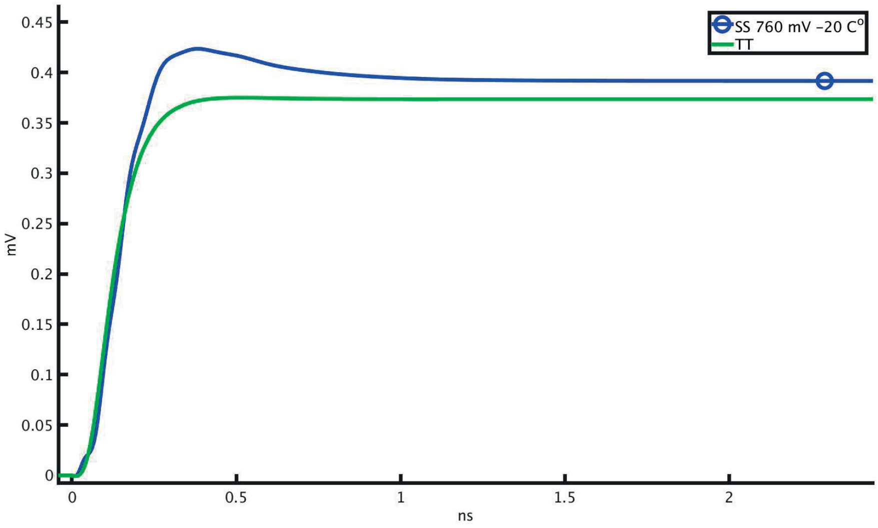

Figure 5.7: Ring amplifier transient response, slow slow, 760mV supply and minus 20 Celsius.

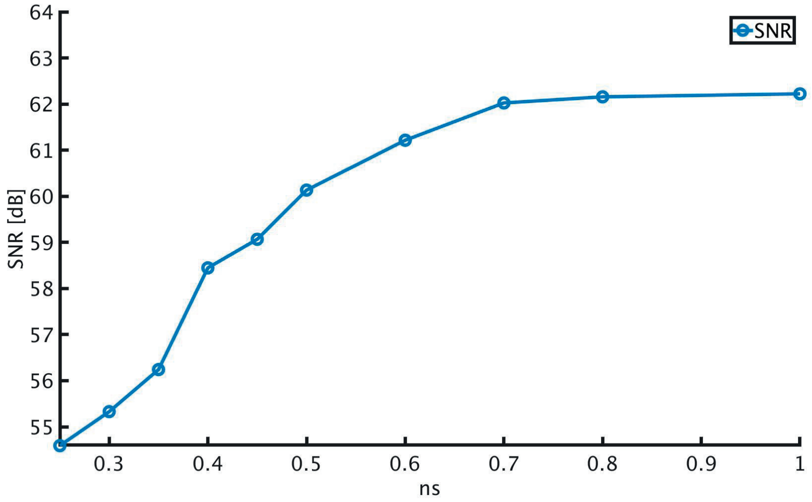

Figure 5.8: SNR versus settling time.

amplifier consumes $120\mu W$, excluding the replica circuit. It is assumed that the replica circuit, will be powered down for most of the time, only negligibly contributing to the power consumption. The ADC has been simulated with circuit noise enabled, and SNR and SFDR recorded for an input amplitude sweep, reaching a peak SNR of 58dB, see Fig. 5.11.

5.7 Result, slow-slow

The feedback capacitor is adjusted to $3.76fF$ to compensate for the increased DC gain. It is assumed that this change would be performed by a first order gain calibration scheme in a fully implemented ADC. Fig. 5.12 and 5.13 show the SNR and SFDR as a function of settling time for the SS corner.

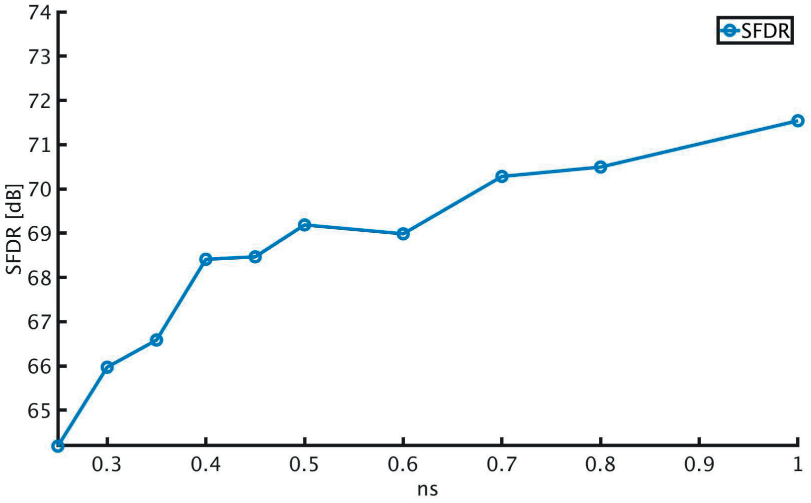

Figure 5.9: SFDR versus settling time.

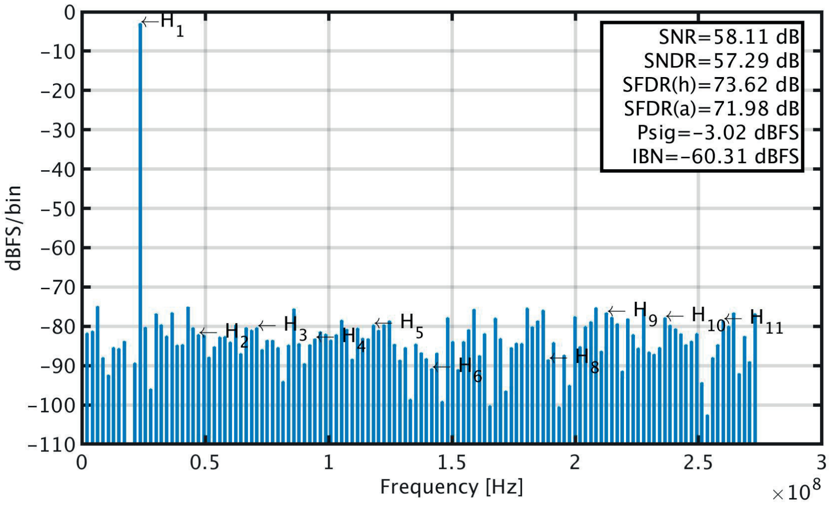

Figure 5.10: Output spectrum of the ADC.

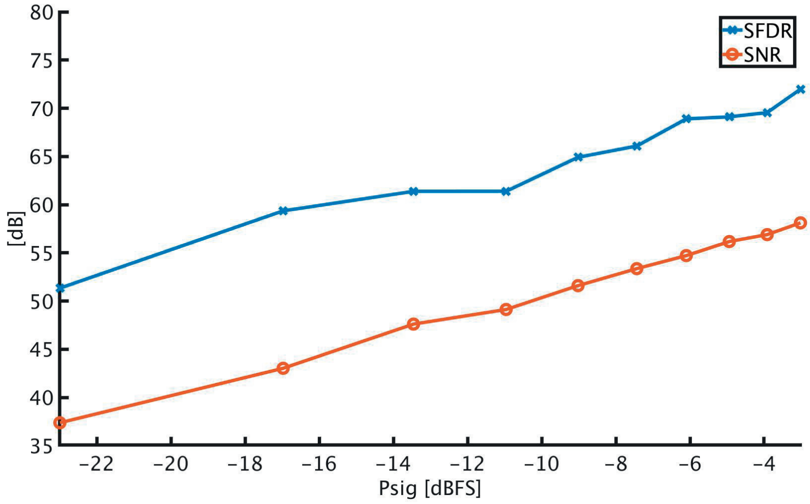

Figure 5.11: SNR and SFDR versus input amplitude.

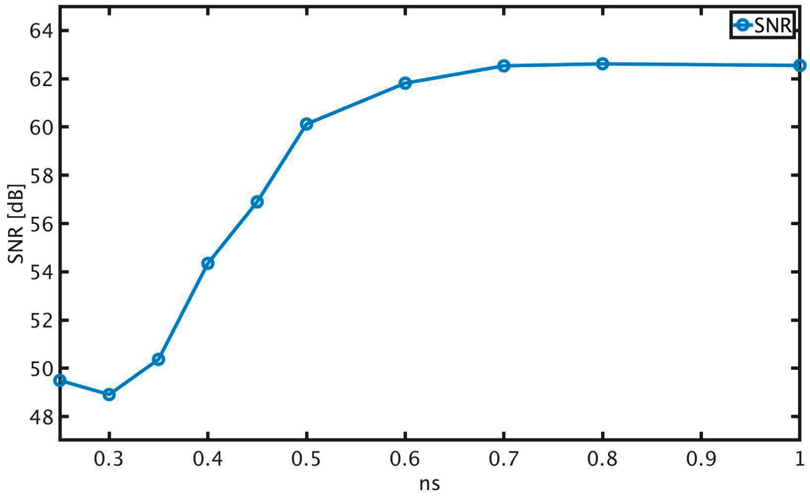

Figure 5.12: SNR versus settling time for the slow-slow corner.

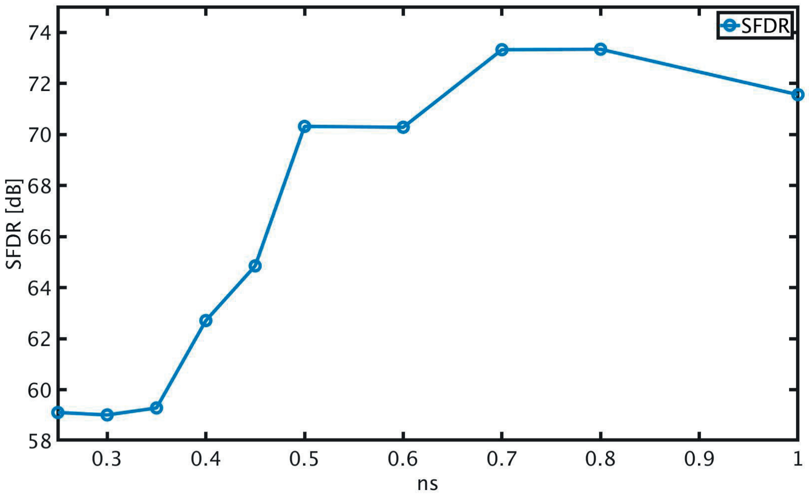

Figure 5.13: SFDR versus settling time for the slow-slow corner.

Chapter 6

Discussion and Conclusion

6.1 Discussion

For low sampling rates and high resolution, ring amplifier based pipeline SAR ADCs performs very well [20], [20], [18], with Schreier figure of merit reaching as high as 180 dB [18]. High speed pipeline assisted SAR ADCs are often implemented with an open loop amplifier [25], [26], [27], [28]. Open loop amplifiers can be classified in two group, integrating amplifiers and transconductance amplifiers. Due to the open loop nature of these amplifiers, they settle faster than ring amplifiers but suffer from low linearity, small output voltage range and sensitivity to PVT variations. Table 6.1 shows a comparison between different state-of-the-art ADCs, Ericsson's conventional SAR ADC and this work.

Noise

Unlike operational amplifiers, ring amplifier features a complicated connection between bandwidth and settling speed. This makes it harder to compare the noise properties of the ring amplifier with open loop amplifiers. Ring amplifiers have lower bandwidth than open loop transconductance amplifiers, leading to lower output noise from the ring amplifier than from open loop transconductance amplifier for a given current. The slower settling time of the ring amplifier means that the ring amplifier will have to be active longer, leading to higher power consumption for a given noise budget. In comparison to Ericsson's conventional SAR ADC the pipeline architecture offers somewhat lower noise and lower speed constraint on the comparator in the first stage. The comparator in the second stage is relaxed immensely in terms of noise. The comparators consume $1.4mW$, more than 10 times that of the ring amplifier, $120\mu W$. Potentially, a redesign of the comparator in the second stage could offer significant improvements in terms of power consumption, compensating for the power consumption introduced by the ring amplifier, while still obtaining somewhat better noise performance than Ericsson's conventional SAR. Another aspect that complicates the comparison between Ericsson's conventional SAR and the pipelined ring amplifier based SAR ADC is that Ericsson's conventional SAR ADC is implemented with redundancy, potentially correcting some of the errors originating from thermal noise.

Linearity

The ADC performance data is based on the simulation of 256 samples. Unfortunately, 256 FFT points is not sufficient to accurately predict SFDR, as the CDAC is ideal with exception of the nonlinear load introduced by the comparator. Apart from the CDAC, the only contributors to the non-linearity are the input switches and the ring amplifier, as harmonic generation of the ring amplifier is very low, on the order of $+70dB$ [29], [16], [15],[30]. Also, the fact that the ring amplifier operates on the residue after five bits already have been converted, reducing the requirement of the ring amplifier, makes it plausible to assume that the ADCs linearity will be very high, even if the ring amplifier does not have sufficient time to fully settle. If very high linearity is desired, say $+80dB$, the ring amplifier might need to settle fully, leading to a longer amplification time.

PVT

It is evident from the plots in chapter 5 that the ring amplifier requires first order gain calibration, due to the gain variation across PVT. For low speeds, the ring amplifier can be designed with higher gain, eliminating the need for calibration. A differential offset may also result from PVT variations. This offset also must be tackled with calibration. The input voltage is sampled on the CDAC during $200ps$, if the sampling frequency of the ADC is $410MHz$ for 10 bit, the total conversion time is $2.2ns$, with the $200ps$ for sampling the input voltage not included. Since the first stage has five bits, half of the conversion time, $1.1ns$, is consumed by the first SAR ADC stage. If the pipelined SAR ADC should be able to provide a higher sampling speed, the ring amplifier needs to perform the amplification within $1.1ns$. This is feasible in for the typical-typical corner but for some of the more extreme corners it could, potentially, be a problem. Considering the corner $-20C^o$ slow-slow and $760mV$ supply voltage, the ring amplifier needs more the $1.1ns$ to settle. However, in this corner the digital circuitry is also considerably slower. By simulating the propagation speed of a signal trough a chain of inverters it is estimated that digital circuitry is 30 percent slower than for the typical-typical corner. This gives the ring amplifier $1.4ns$ to settle. Consequently, the ring amplifier will most likely boost the speed of Ericsson's conventional SAR ADC even in this corner.

The first stage in the ring amplifier does not have any means of regulating the current through the first stage. Consequently, in the slow-slow corner the current through the first stage is reduced leading to lower gain and higher noise. The effect is somewhat mitigated by the fact that the transistors dive deeper into sub-threshold region in the SS corner, improving gain efficiency. This effect can however only partly compensate for the reduced current. In the fast-fast corner, the current through the first stage is increased, resulting in increased power consumption. The internal common mode feedback, does however help keeping the output voltage of the first stage close to the desired common mode. The ring amplifier is capable of operating with somewhat higher output voltage than the proposed design, but the common mode of the ring amplifier varies with some $+-50mV$ over PVT, limiting the output voltage headroom.

Table 6.1: Performance summary and comparison of high speed analog converters. Reference power consumption is not included.

	This work	Ericssons conventional SAR	Pipelined [30]	Pipeline SAR [27]	SAR [31]	Pipeline SAR [25]
Sampling rate (MHz)	550	410	600	1000	300	410
SNR (dB)	58	54	60.4	60	60.5	58.5
SFDR (dB)	71	67	83.1	74.6	78.5	68
Power (mW)	3.34	2.3	6	7.6	3.3	2.1
ENOB (b)	9.3	8.7	9.7	9.2	9.7	9.4
FOM (Schreier)	167	163.5	167.2	168	167.1	167
V_{pkpk}	1	0.8	1.5	N/A	0.8	N/A
VDD (V)	0.8	0.8	0.85	1	0.85	0.9
Process	FD-SOI 22nm	FD-SOI 22nm	FinFet 16nm	CMOS 28nm	FinFet 14nm	CMOS 28nm

6.2 Future work

The pipeline assisted ring amplifier based SAR ADC implemented here can be improved further. All simulation is based on a schematic level setup, with ample use of ideal components. In particular, the CDAC have an unrealistically high linearity performance, due to its ideal capacitors. The ring amplifier relaxes the linearity of the second CDAC substantially while also reducing the impact from comparator noise in the second stage of the ADC. It is not investigated if another switching scheme ought to be used in the second stage CDAC. Due to the lower linearity requirement on the second CDAC. One alternative could be Merged capacitor switching. This would save valuable time for the second stage. Another drawback of the implementation is that more conversions take place in stage one than stage two. Putting further strain on the comparator in the first stage. If the second stage incorporate redundancy, it would relax the requirement on the first stage and balance the stage between stage one and two. The ADC should most likely incorporate redundancy, as in the original design, as this offers the opportunity to correct for error resulting from comparator and noise. In addition, the comparators can be optimized to better suit the new ADC architecture. The logic and registers for Ericsson's conventional SAR ADC will need to be redesigned as well. Layout of the ring amplifier is also important as it will degrade the settling speed in the ring amplifier somewhat. It is well known that the Flicker noise is filtered by auto-zeroing. Auto-zeroing would, however, be impractical for the ring amplifier implemented, because of the large auto zeroing capacitance needed and somewhat higher power consumption. Another way of tackling the Flicker noise could be bias the ring amplifiers transistor in accumulation during the sampling phase. In [32] this is shown to reduce flicker noise with 8 dB. This path is not investigated further.

6.3 Conclusion

The low noise and low power consumption of the ring amplifier, typically one tenth or less of the power consumption of high speed SAR ADC, makes the ring amplifier an alternative as residue amplifier in pipline assisted SAR ADC. Surprisingly, the biggest problem with the ring amplifier is not noise, linearity or power. But rather the settling time, where the ring amplifier needs more than $500ps$ to fully settle. This settling time is expected to increase somewhat with layout parasitics included. Another challenge with the ring amplifier in a commercial setting is that the ring amplifiers performance deteriorate substantially more than the digital circuitry with respect to PVT changes. Despite these problems, it is possible that pipeline assisted ring amplifier based SAR ADC will show improved speed, noise and most likely power consumption over Ericsson's conventional SAR ADC at the cost of higher design complexity and increased sensitivity to PVT variations.

References

[1] Ericsson, "Mobile data traffic outlook." `https://www.ericsson.com/en/mobility-report/reports/november-2019/mobile-data-traffic-outlook/`, Nov. 2019.

[2] T. S. Rappaport, S. Sun, R. Mayzus, H. Zhao, Y. Azar, K. Wang, G. N. Wong, J. K. Schulz, M. Samimi, and F. Gutierrez, "Millimeter wave mobile communications for 5g cellular: It will work!," *IEEE Access*, vol. 1, pp. 335–349, 2013.

[3] B. Murmann, "Energy limits in a/d converters," in *2013 IEEE Faible Tension Faible Consommation*, pp. 1–4, June 2013.

[4] F. Maloberti, *Data Converters*. Springer, 1nd ed., 2007.

[5] W. R. Bennett, "Spectra of quantized signals," *The Bell System Technical Journal*, vol. 27, pp. 446–472, July 1948.

[6] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, vol. 17, pp. 539–550, April 1999.

[7] A. M. A. Ali, A. Morgan, C. Dillon, G. Patterson, S. Puckett, P. Bhoraskar, H. Dinc, M. Hensley, R. Stop, S. Bardsley, D. Lattimore, J. Bray, C. Speir, and R. Sneed, "A 16-bit 250-ms/s if sampling pipelined adc with background calibration," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2602–2612, Dec 2010.

[8] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable adc architectures," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, pp. 1441–1454, July 2008.

[9] B. Razavi, "The strongarm latch [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, pp. 12–17, Spring 2015.

[10] Y. Zhu, C. Chan, U. Chio, S. Sin, S. U, R. P. Martins, and F. Maloberti, "A 10-bit 100-ms/s reference-free sar adc in 90 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1111–1121, June 2010.

[11] Y. Zhu, C. Chan, U. Chio, S. Sin, S. U, R. P. Martins, and F. Maloberti, "Split-sar adcs: Improved linearity with power and speed optimization," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, pp. 372–383, Feb 2014.

[12] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U. Moon, “Ring amplifiers for switched capacitor circuits,” *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 2928–2942, Dec 2012.

[13] S. Leuenberger, P. K. Venkatachala, A. ElShater, M. Oatman, C. Lee, B. Xiao, and U. Moon, “An empirical study of the settling performance of ring amplifiers for pipelined adcs,” in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, May 2018.

[14] K. M. Megawer, F. A. Hussien, M. M. Aboudina, and A. N. Mohieldin, “A systematic design methodology for class-ab-style ring amplifiers,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, pp. 1169–1173, Sep. 2018.

[15] J. Lagos, B. Hershberg, E. Martens, P. Wambacq, and J. Craninckx, “A single-channel, 600-ms/s, 12-b, ringamp-based pipelined adc in 28-nm cmos,” *IEEE Journal of Solid-State Circuits*, vol. 54, pp. 403–416, Feb 2019.

[16] J. Lagos, B. P. Hershberg, E. Martens, P. Wambacq, and J. Craninckx, “A 1-gs/s, 12-b, single-channel pipelined adc with dead-zone-degenerated ring amplifiers,” *IEEE Journal of Solid-State Circuits*, vol. 54, pp. 646–658, March 2019.

[17] Y. Chen, J. Wang, H. Hu, F. Ye, and J. Ren, “A 200ms/s, 11 bit sar-assisted pipeline adc with bias-enhanced ring amplifier,” in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, May 2017.

[18] A. ElShater, P. K. Venkatachala, C. Y. Lee, J. Muhlestein, S. Leuenberger, K. Sobue, K. Hamashita, and U. Moon, “A 10-mw 16-b 15-ms/s two-step sar adc with 95-db dr using dual-deadzone ring amplifier,” *IEEE Journal of Solid-State Circuits*, vol. 54, pp. 3410–3420, Dec 2019.

[19] C. Y. Lee, P. K. Venkatachala, A. ElShater, B. Xiao, H. Hu, and U. Moon, “Cascoded ring amplifiers for high speed and high accuracy settling,” in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, May 2019.

[20] Y. Lim and M. P. Flynn, “A 1 mw 71.5 db sndr 50 ms/s 13 bit fully differential ring amplifier based sar-assisted pipeline adc,” *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 2901–2911, Dec 2015.

[21] Y. Lim and M. P. Flynn, “A calibration-free 2.3 mw 73.2 db sndr 15b 100 ms/s four-stage fully differential ring amplifier based sar-assisted pipeline adc,” in *2017 Symposium on VLSI Circuits*, pp. C98–C99, June 2017.

[22] A. S. Ahmed, M. M. Aboudina, F. A. Hussien, and A. N. Mohieldin, “A ring amplifier architecture for continuous-time applications,” in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, May 2018.

[23] P. Llimós Muntal and I. H. H. Jørgensen, “34.3 fj/conv.-step 8-mhz bandwidth fourth-order pseudo-differential ring-amplifier-based continuous-time delta–sigma adc in 65 nm,” *IEEE Solid-State Circuits Letters*, vol. 1, pp. 198–201, Oct 2018.

[24] P. K. Venkatachala, S. Leuenberger, A. ElShater, C. Lee, Y. Xu, B. Xiao, M. Oatman, and U. Moon, “Process invariant biasing of ring amplifiers using deadzone regulation circuit,” in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, May 2018.

[25] B. Verbruggen, M. Iriguchi, M. de la Guia Solaz, G. Glorieux, K. Deguchi, B. Malki, and J. Craninckx, “A 2.1 mw 11b 410 ms/s dynamic pipelined sar adc with background calibration in 28nm digital cmos,” in *2013 Symposium on VLSI Circuits*, pp. C268–C269, June 2013.

[26] F. van der Goes, C. M. Ward, S. Astgimath, H. Yan, J. Riley, Z. Zeng, J. Mulder, S. Wang, and K. Bult, “A 1.5 mw 68 db sndr 80 ms/s 2 × interleaved pipelined sar adc in 28 nm cmos,” *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 2835–2845, Dec 2014.

[27] W. Jiang, Y. Zhu, M. Zhang, C. Chan, and R. P. Martins, “A temperature-stabilized single-channel 1-gs/s 60-db sndr sar-assisted pipelined adc with dynamic gm-r-based amplifier,” *IEEE Journal of Solid-State Circuits*, vol. 55, pp. 322–332, Feb 2020.

[28] K. Moon, H. Kang, D. Jo, M. Kim, S. Baek, M. Choi, H. Ko, and S. Ryu, “A 9.1 enob 21.7fj/conversion-step 10b 500ms/s single-channel pipelined sar adc with a current-mode fine adc in 28nm cmos,” in *2017 Symposium on VLSI Circuits*, pp. C94–C95, June 2017.

[29] B. Hershberg, D. Dermit, B. v. Liempd, E. Martens, N. Markulic, J. Lagos, and J. Craninckx, “3.1 a 3.2gs/s 10 enob 61mw ringamp adc in 16nm with background monitoring of distortion,” in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, pp. 58–60, Feb 2019.

[30] B. Hershberg, B. v. Liempd, N. Markulic, J. Lagos, E. Martens, D. Dermit, and J. Craninckx, “3.6 a 6-to-600ms/s fully dynamic ringamp pipelined adc with asynchronous event-driven clocking in 16nm,” in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, pp. 68–70, Feb 2019.

[31] D. Luu, L. Kull, T. Toifl, C. Menolfi, M. Brändli, P. A. Francese, T. Morf, M. Kossel, H. Yueksel, A. Cevrero, I. Ozkaya, and Q. Huang, “A 12-bit 300-ms/s sar adc with inverter-based preamplifier and common-mode-regulation dac in 14-nm cmos finfet,” *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 3268–3279, Nov 2018.

[32] E. A. M. Klumperink, S. L. J. Gierkink, A. P. van der Wel, and B. Nauta, “Reducing mosfet 1/f noise and power consumption by switched biasing,” *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 994–1001, July 2000.

Chapter 7

Appendix

7.1 VerilogA code

```
‘include "constants.vams"
‘include "disciplines.vams"

‘define SAR_BITS 10  // Number of ADC bits

module reg_10_CMS_CMS(vdd, vss, SMP, comp_p, comp_m, comp_p2,
comp_m2, comp_ready1, comp_ready2, clk_1, clk_2, sar_data, sar_c,
sar_d, sar_d_n, amp_en);

input comp_p, comp_m, comp_ready1, comp_ready2, SMP, comp_p2, comp_m2;
inout vdd,vss;

// For an n bit ADC, n-1 bits are used in the capacitor bank,
because the LSB is found without switching the DAC.
output [‘SAR_BITS:0] sar_c; // controls connection of Vcm
output [‘SAR_BITS-1:1] sar_d; // controls connection to Vref{p,m}
output [‘SAR_BITS-1:1] sar_d_n; // controls connection to Vref{p,m}
output [‘SAR_BITS:1] sar_data;
output clk_1, clk_2;
output amp_en;

electrical vdd, vss, comp_ready1, comp_ready2;
electrical [‘SAR_BITS:0] sar_c;
electrical [‘SAR_BITS-1:1] sar_d;
electrical [‘SAR_BITS-1:1] sar_d_n;
electrical [‘SAR_BITS:1] sar_data;
electrical  comp_p, comp_m, SMP, clk_1, clk_2, amp_en, comp_p2, comp_m2;

// Temporary variables, later written to the outputs.
integer i_sar_c[‘SAR_BITS:0];
integer i_sar_d[‘SAR_BITS-1:0];
integer i_sar_d_n[‘SAR_BITS-1:0];
integer i_sar_data[‘SAR_BITS:1];
integer i_state_1;
integer i_state_2;

genvar i;

// Dealy, rise and fall time for c
real c_td = 25p;
real c_tr = 20p;
real c_tf = 20p;

// Dealy, rise and fall time for d
real d_td = 25p;
real d_tr = 20p;
real d_tf = 20p;

// Dealy, rise and fall time for d_n
real d_n_td = 25p;
real d_n_tr = 20p;
real d_n_tf = 20p;

// Dealy, rise and fall time for comparator clock
real td_cmp_clk = 50p;
real tr_cmp_clk = 10p;
real tf_cmp_clk = 15p;

// Dealy, rise and fall time for power control of residue amplifier
real td_amp_en = 5p;
real tr_amp_en = 10p;
real tf_amp_en = 15p;


//Setting for Async ADC
parameter real vth = 0.4;
parameter real vhigh = 0.8;
parameter real time_SMP_to_clk = 70p;
parameter real time_clk_width =  65p;
parameter real time_amp_active = 500p;

real ctrl_time1;
real ctrl_time2;
real ctrl_time3;
real time_amp_en;


//Internal signals
```

```
real i_cmp_clk_1;
real i_cmp_clk_2;
real i_amp_en;


analog begin

// **********   INITIAL stage   **********
@(initial_stage) begin // Setup

ctrl_time1 = 0;
ctrl_time2 = 0;
ctrl_time3 = 0;
time_amp_en = 0;

i_state_1 = 1;
i_state_2 = 1;

i_cmp_clk_1 = 0;
i_cmp_clk_2 = 0;
i_amp_en = 0;

for (i = 10; i>=0; i = i-1) begin
i_sar_c[i] = 0;
end

for (i = 9; i>=1; i = i-1) begin
i_sar_d[i] = 0;
i_sar_d_n[i] = 0;
end

for (i = ‘SAR_BITS-1; i>=1; i = i-1) begin
i_sar_data[i] = 1;
end

end // initial stage


@ (cross(V(SMP) - vth, 1)) begin
i_sar_c[0] = 0;
for (i = 5; i>=1; i = i-1) begin
i_sar_c[i] = 0;
i_sar_d[i] = 0;
i_sar_d_n[i] = 0;
end
end
```

```
@ (cross(V(SMP) - vth, -1)) begin
i_sar_c[0] = 1;
for (i = 5; i>=1; i = i-1) begin
i_sar_c[i] = 1;
i_sar_d[i] = 0;
i_sar_d_n[i] = 0;
end
    i_state_1 = 1;
ctrl_time1 = $abstime + time_SMP_to_clk;
end


// Generate a comparator clock pulse
@(timer(ctrl_time1))
if(ctrl_time1>0)
i_cmp_clk_1 = 1;
@(timer(ctrl_time1+time_clk_width))
i_cmp_clk_1 = 0;

@(timer(ctrl_time2))
if(ctrl_time2 > 0)
i_cmp_clk_2 = 1;
@(timer(ctrl_time2 + time_clk_width))
i_cmp_clk_2 = 0;


   // Generate amplification phase
@(timer(time_amp_en)) begin
if(time_amp_en>0)
i_state_2 = 1;
i_amp_en = 1;
for (i = 10; i>=6; i = i-1) begin
i_sar_c[i] = 0;
end
for (i = 9; i>=6; i = i-1) begin
i_sar_d[i] = 0;
end
for (i = 9; i>=6; i = i-1) begin
i_sar_d_n[i] = 0;
end
end

@(timer(time_amp_en+time_amp_active)) begin
i_amp_en = 0;
for (i = 10; i>=6; i = i-1) begin
i_sar_c[i] = 1;
```

```
end
end


@ (cross(V(comp_ready1) - vth, 1)) begin

// **********   1 <= STATE ADC_1 <=    **********
if((i_state_1 <= 4) && (V(SMP) < vth)) begin
ctrl_time1= $abstime + 5p;
if(V(comp_m) < vth) begin
i_sar_d_n[6-i_state_1] = 1;
end else begin
i_sar_d_n[6-i_state_1] = 0;
end
if(V(comp_p) < vth) begin
i_sar_d[6-i_state_1] = 1;
end else begin
i_sar_d[6-i_state_1] = 0;
end
    i_sar_data[6-i_state_1] = i_sar_d_n[6-i_state_1];
i_sar_c[6-i_state_1] = 0;
  i_state_1 = i_state_1 + 1;
// **********   STATE ADC_1 = 5   **********
end else if((i_state_1 == 5) && (V(SMP) < vth)) begin
ctrl_time2 = $abstime + time_amp_active+50p;
time_amp_en = $abstime + 50p;
if(V(comp_m) < vth) begin
i_sar_d_n[6-i_state_1] = 1;
end else begin
i_sar_d_n[6-i_state_1] = 0;
end
if(V(comp_p) < vth) begin
i_sar_d[6-i_state_1] = 1;
end else begin
i_sar_d[6-i_state_1] = 0;
end
    i_sar_data[6-i_state_1] = i_sar_d_n[6-i_state_1];
i_sar_c[6-i_state_1] = 0;
  i_state_1 = i_state_1 + 1;
end
end


@ (cross(V(comp_ready2) - vth, 1)) begin
// **********   1 <= STATE ADC_2 <= 4   **********
if((i_state_2 <= 4) && (V(amp_en) < vth)) begin
ctrl_time2 = $abstime + 5p;
```

```
if(V(comp_m2) < vth) begin
i_sar_d_n[5+i_state_2] = 1;
end else begin
i_sar_d_n[5+i_state_2] = 0;
end
if(V(comp_p2) < vth) begin
i_sar_d[5+i_state_2] = 1;
end else begin
i_sar_d[5+i_state_2] = 0;
end
    i_sar_data[5+i_state_2] = i_sar_d[5+i_state_2];
i_sar_c[5+i_state_2] = 0;
  i_state_2 = i_state_2 + 1;
// **********   STATE = 10   **********
end else if((i_state_2 == 5) && (V(amp_en) < vth)) begin
if(V(comp_p2) < vth) begin
i_sar_data[5+i_state_2] = 1;
end else begin
i_sar_data[5+i_state_2] = 0;
end
  i_state_2 = i_state_2 + 1;
end
end


// ***** Outputs *****

for (i = 10; i>=0; i = i-1) begin
V(sar_c[i])  <+ transition(i_sar_c[i]*vhigh, c_td, c_tr, c_tf);
end

for (i = 9; i>=1; i = i-1) begin
V(sar_d[i])  <+ transition(i_sar_d[i]*vhigh, d_td, d_tr, d_tf);
V(sar_d_n[i])  <+ transition(i_sar_d_n[i]*vhigh, d_n_td, d_n_tr, d_n_tf);
end

for (i = 10; i>=5; i = i-1) begin
V(sar_data[i]) <+ transition(i_sar_data[i]*vhigh, 30p, 10p);
end


for (i = 5; i>=1; i = i-1) begin
V(sar_data[i]) <+ transition(i_sar_data[i]*vhigh, 30p, 10p);
end

V(amp_en)<+ transition(i_amp_en*vhigh, td_amp_en, tr_amp_en, tf_amp_en);
    V(clk_1)<+ transition(i_cmp_clk_1*vhigh, td_cmp_clk,
    tr_cmp_clk, tf_cmp_clk);
V(clk_2)<+ transition(i_cmp_clk_2*vhigh, td_cmp_clk,
tr_cmp_clk, tf_cmp_clk);
end

endmodule
```

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