Growth and Characterization of Ferroelectric Lanthanum-Doped Hafnia

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Abstract

Hafnia-based ferroelectrics show great promise as future nonvolatile memory devices, however, their issues regarding device inconsistency across their lifetime, coupled with the relatively short total lifetime, makes these devices only theoretical as of now. In this thesis, an ALD deposition recipe for lanthanum oxide deposition was created. Using this recipe, lanthanum-doped hafnia thin films were manufactured and characterized. Although several issues emerged which limited the ALD-step of the process, ferroelectric devices were created and characterized. The devices have a coercive field between 0.9 and 1.2 MV/cm with remanent polarizations of up to 20 μC/cm^2. Endurance measurements showed no sign of fatigue even after 10 million cycles - indicating a relatively long lifetime of the devices. This long lifetime is accompanied by a very long wake-up, which could be due to the issues with the ALD recipe. A comparison between Rapid Thermal Annealing (RTA) and Flash Lamp Annealing (FLA) as the selected annealing method was made. Although the results indicate no ferroelectricity in the samples annealed in the FLA, no conclusion can be drawn as to whether this is due to the FLA process or underlying problems with the oxide on the samples.

Popular Science Summary

Memory is an oftentimes hidden aspect of computing, and has not until very recently been a limiting factor in what types of tasks can be performed on a computer. However, the nature of memory today causes it to drain a lot of energy, an issue which would be very beneficial for both computer performance and energy consumption.

A typical computer has some long-term memory, such as a hard-disk drive, or in more recent years, a solid state drive. These memories are nonvolatile, meaning that once written to, they retain their information for decades years without losing it. The downside with these memories is that they are so slow that the brains of the computer, the processor, could have done millions of calculations in the time it takes the memory to change a bit of information [1]. This necessitates some high-speed memory which is in direct communication with the processor. Typically, this high-speed memory consists primarily of Dynamic Random Access Memory, or DRAM, which allows read- and write operations to occur in tens of nanoseconds. The problem with this memory is that it leaks its memory state with time. Imagine DRAM like a reservoir of water connected with a tap. If you open the tap, you can find out if there is water or not in the reservoir, but a hole in the bottom makes the water leak out over time. This problem results in the need to constantly refresh DRAM. This is done once every 64 milliseconds, and is a large reason for power consumption in this high-speed memory [2].

The "holy grail" of memory technology is thus some memory device which is quick, but retains its information over long periods of time, all while being compact enough for gigabytes of data storage. There are devices which could work for these purposes, but they face several issues which prevent them from reaching markets. One type of these memory devices are based on so-called ferroelectric films. These memories are based on materials with a specific crystalline structure which shifts its properties in measurable ways when subjected to electric signals. These shifts are permanent and quick, solving both of these problems. While these memories are developed to the point where they have been implemented in actual market-viable products, they faced one primary issue. The devices are too large, and needed shrinking in order to become viable for large-scale integration.

Recent developments in this field have discovered alternative materials which can become ferroelectric, while allowing for reasonable scaling. These techniques have to be refined and research is currently investigating ways of creating these memory devices while solving some of the issues they are facing. This thesis is looking in to just that, and is focused on developing and characterizing ferroelectric thin films, which may in the future find a home in your computer.

[1] Wong, H., Salahuddin, S. Memory leads the way to better computing. Nature Nanotech 10, 191194 (2015).
[2] Dynamic RAM, DRAM Memory Technology, www.electronics-notes.com

Abbreviations and Acronyms

ALD - Atomic Layer Deposition
RTA - Rapid Thermal Annealing
FLA - Flash Lamp Annealing
RAM - Random Access Memory
NVRAM - Nonvolatile Random Access Memory
FeRAM - Ferroelectric RAM
FeFET - Ferroelectric Field Effect Transistor
FTJ - Ferroelectric Tunnel Junction
NCFET - Negative Capacitance Field Effect Transistor
PZT - Lead Zirconate Titanate
DRAM - Dynamic Random Access Memory
CMOS - Complementary Metal-Oxide-Semiconductor
HLO - Hafnium-Lanthanum-Oxide / lanthanum-doped hafnia
E_c - Coercive Field
P_r - Remanent Polarization
MOSFET - Metal-Oxide-Semiconductor Field Effect Transistor
PUND - Positive-Up Negative-Down
MIM - Metal-Insulator-Metal
MFM - Metal-Ferroelectric-Metal
TDMAHf - Tetrakis(Dimethylamido)Hafnium
DMA - Dimethylamide
$(iPrCp)_3La$ - Tris(IsoPropylCycloPentaDienyl)lanthanum
GPC - Growth Per Cycle
PVD - Physical Vapor Deposition
CVD - Chemical Vapor Deposition
RF - Radio Frequency
DC - Direct Current
RPM - Revolutions Per Minute
WGFMU - Waveform Generator/Fast Measurement Unit
SMU - Source Measurement Unit
DUT - Device Under Test

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Contents

1 Introduction

Ferroelectricity was first discovered in 1920 by J. Valasek, who noticed a hysteresis loop emerging in the polarization as the electric field was varied across a capacitor using Rochelle Salt as the dielectric [3]. It was later realized that ferroelectric materials could be utilized to improve or create new electronic devices. For instance, nonvolatile random access memories (NVRAMs) based on ferroelectrics such as Ferroelectric RAM [4], Ferroelectric FETs (FeFETs) [5–7], or Ferroelectric Tunnel Junctions (FTJs) [8] which retain memory without a constant power supply. Another application of ferroelectric films in microelectronics is Negative Capacitance FETs (NCFETs) which are theorized to be able to stabilize an otherwise unstable negative-capacitance state in a ferroelectric to yield sub-60 mV/decade operation of transistor devices for more energy efficient computation [9].

Several of these devices have been produced using perovskites, such as Lead Zirconate Titanate (PZT) [10]. Devices made from ferroelectric perovskites have shown both retention times greater than 35 years and more than 10^{15} switching cycles [11]. Although smaller arrays of high-speed FRAM exists in contemporary products, the ceramics-based ferroelectrics have certain disadvantages such as difficult deposition techniques, CMOS (complementary metal-oxide-semiconductor) integration- and scaling issues [11] which make these materials unsuitable for larger memory arrays that could facilitate the replacement of the power-hungry Dynamic Random Access Memory (DRAM) with a more efficient nonvolatile alternative.

When, in 2011, hafnia was found to become ferroelectric when confined between two metal electrodes as it was crystallized [12], the ferroelectrics field was naturally interested in further researching this phenomena. Hafnia as a material has already been incorporated in CMOS technology as a high-k dielectric, which meant that fully developed stable deposition processes were already in place for the material. The ferroelectric effect was also shown to persist even for hafnia layers on the order of a few nm in thickness, which also solved the scaling issues perovskites had faced. Researchers found that doping hafnia with various other elements could help promote the ferroelectric effect [13]. In particular, past research has shown lanthanum to be a viable dopant for a large remanent polarization [14] while demonstrating a wide process window.

However, hafnia-based ferroelectrics face other issues. Most notably are the wake-up effect and low endurance [15] that stop these devices from becoming market-viable. The wake-up effect is characterized by an initially low remanent polarization which increases in strength until reaching its final (maximal) value. The low endurance of the devices means that the ferroelectric breaks down after some number of cycles, rendering devices useless for practical applications where millions of switches can occur in a second. Current endurance times for hafnia-based ferroelectrics are at best on the order of 10^{10} cycles [16], which is insufficient for high-speed memory applications.

The goal of this thesis is to investigate lanthanum oxide deposition conditions in the local Atomic Layer Deposition (ALD) system as the lanthanum oxide precursor has not previously been used locally. Using the developed recipe, a ferroelectric lanthanum-doped hafnia (HLO) film will be created and its properties investigated electronically as the annealing temperature and lanthanum concentration is varied. Lanthanum is chosen specifically as it has been shown

to have a wide process window, and provide strong remanent polarization.

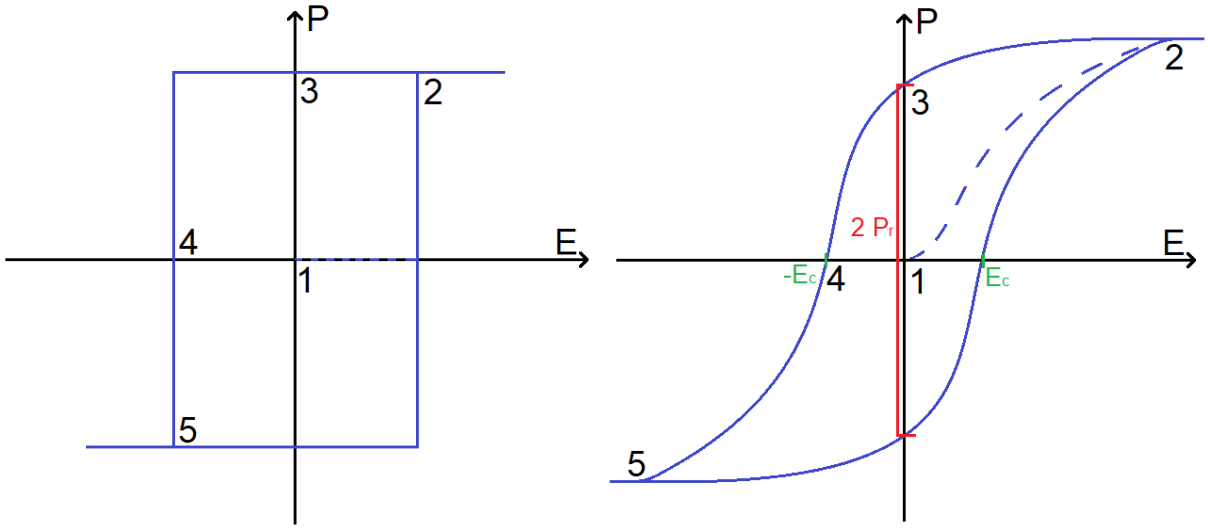
Lastly, a comparison between using Rapid Thermal Annealing (RTA) and Flash-Lamp Annealing (FLA) to crystallize the films will be carried out. The hypothesis being that an FLA process heats the sample to the crystallization temperature to yield the ferroelectric behaviour, while not remaining at this high temperature long enough for diffusion to generate defects. This may result in a longer endurance and lower measured leakage.

2 Theory

2.1 Ferroelectricity

Ferroelectricity implies a hysteresis in polarization with a varying electric field. This means that an external electric field can induce electrical dipoles which remain after the field is removed (see Figure 1). In normal circumstances, dielectrics allow a slight shift in the average equilibrium position for internal electrical charges resulting the creation of internal dipoles. The strength of polarization in the material is proportional to the magnitude of the electric field, and once the field is removed, the dielectric returns to its non-polarized state. The net-result of dielectric polarization is the collection of charged particles at either edge of the dielectric film, which attracts charge of the opposite side from the conductor it is in contact with. The strength of the polarization is proportional to the charge stored per unit area of a capacitor and has the unit C/m^2.

Ferroelectricity is a property which is only seen in one of the 32 possible crystal classes, it belongs to a larger group of materials known as piezoelectrics. These materials show a polarization dependent on mechanical strain, and conversely, may grow or contract when external electric fields are applied. There are in total 20 crystalline classes which exhibit piezoelectricity, all of them have non-centrosymmetric structures. Among the piezoelectric materials, a further 10 of these are classified as pyroelectrics, which additionally generate a polarization dependent on temperature. One of the pyroelectric materials can also permanently switch its polarization in response to an external electric field. This is the rhombic-pyramidial crystal, which in hafnia has the space group $Pca2_1$.



(a) (b)

Figure 1: The hysteresis loop for a ferroelectric material. **(a)** shows an ideal ferroelectric, where each domain switches completely at the coercive field, E_c and remains switched until an electric field $-E_c$ is felt. **(b)** shows a realistic ferroelectric where misaligned domains cause a range of effective coercive fields. The marked points are: 1) The initial state of the material has domains with random polarization, resulting in a net-polarization of zero. 2) An electric field has been applied forcing all internal domains to align with the field, reaching saturation. 3) The electric field has been released, the measured polarization is entirely due to spontaneous polarization. 4) The negative coercive field ($-E_c$) is reached. 5) Saturation is reached in the opposite direction. The remanent polarization is defined as the half the difference between the two measured polarizations at 0 electric field. The coercive field is defined as the field which results in 0 polarization.

2.1.1 Physical Process of Ferroelectricity

In ferroelectric materials, an atom in the lattice with a net nonzero charge has two energetically stable positions within the crystal, separated by an energy barrier. This leads to an initial polarization in the material which is near zero as the ferroelectric domains inside the material are polarized randomly. As an electric field is applied, the energy landscape is shifted along with the electric field. At some point, the electric field reaches the coercive field, E_c, which is large enough for the atom to overcome the energy barrier and move to the other stable point. Once the electric field is removed, the atom remains in place. As every one of these atoms in the crystal is now in the same position there is a remanent dielectric polarization, denoted P_r. See figure 2.

In a real ferroelectric, the domains in the material are not all aligned with one another. This means that not every charged atom will move along the electric field, but at an angle to it. This means that the resulting force on the atom will be proportional to the electric field with

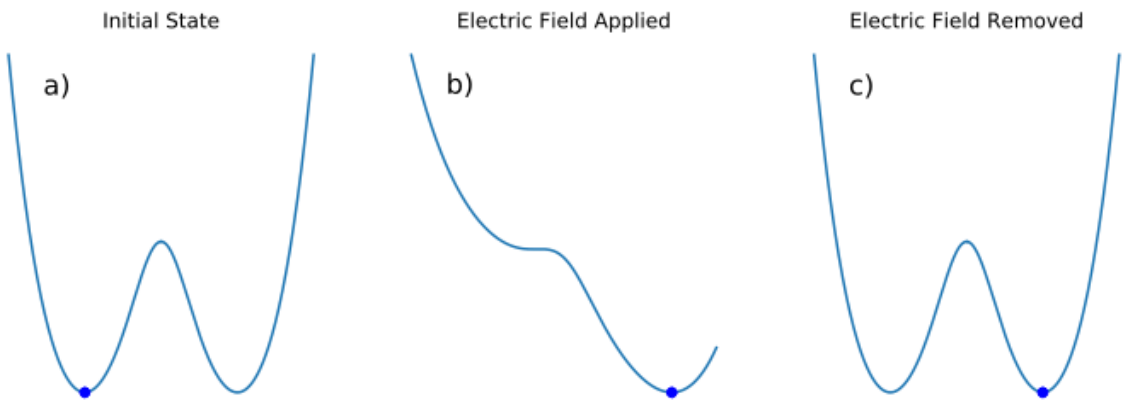


Figure 2: The mechanism behind the ferroelectric effect illustrated. Going from the inital polarization state (a) of the ferroelectric crystal, an applied electric field shifts the energy structure which lets the state transfer to another local minima (b). Once the electric field is removed, the particle remains in this state (c) until a reverse electric field is applied.

a factor dependent on the angle. A perfectly aligned crystal will switch at exactly E_c, but a crystal aligned perpendicularly to the field will never switch.

A perfect, monocrystalline ferroelectric aligned exactly with the external field, would instantly switch its polarization once the coercive field is reached, resulting in a square-like hysteresis loop. In real ferroelectrics the varying orientation of the domains as well as the presence of defects in the material causes a spread of coercive field, resulting in a curved hysteresis loop such as the one in figure 1.

2.1.2 Crystallization of Ferroelectric Doped Hafnia

Ferroelectricity was first found in hafnia for a thin film crystallized under the confinement of two metal electrodes. This confinement was thought to strain the film to allow alternate crystalline phases to emerge [12]. It was also found that doping the hafnia with a range of various other elements promoted the emergence of the ferroelectric phase [13].

Using simulation methods, it was shown that the emergence of ferroelectricity in hafnia is due to the compressive strain applied to the film when it is crystallized while confined between the two metal electrodes. This strain shifts the energy requirement for formation of the monoclinic and orthorhombic phases such that the transition form the tetragonal phase to the orthorhombic phase is promoted [17].

It was also found that the role of dopants in ferroelectric hafnia films, is not to make the t-o transition more favorable, but to stabilize the tetragonal phase during growing stages of the film, thus resulting in more tetragonal structures that during the relaxation of the film in the annealing process can then transform into the orthorhombic crystal phase.

2.1.3 Operation of FE Devices

The ferroelectric switching behavior can be utilized in a wide variety of devices, most notably for memory applications. Since the remanent polarization in the ferroelectric film is stable, devices made with ferroelectrics can have a retention time > 10 years, which in industry classifies them as nonvolatile.

The first nonvolatile memory device based on ferroelectricity is the FeRAM. In design, it is similar to a DRAM which has a capacitor in series with the drain of a transistor, but instead of a linear dielectric in the capacitor, FeRAM uses a ferroelectric material, such as PZT. The writing operation is similar, both rely on applying a field to charge the capacitor. The reading operation is where the two memories differ. In a DRAM, the read operation is conducted by opening a transistor between the output line and the DRAM, and applying a low bias on the readout. If a current flow is measured, the DRAM was charged, thus had a value of 1. In a FeRAM, the readout is done by forcing the FeRAM into a specific state. If this state is opposite to its currently held state, a switch will occur, which will result in a spike in current. If the device is storing the forced state already, no such current pulse will be detected. The FeRAM is thus, similarly to the DRAM, a memory with a destructive readout operation, requiring a rewrite of the state after measurement.

The Ferroelectric FET (FeFET) is another ferroelectric-based memory device, implementing a regular MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) architecture, but replacing the oxide with a ferroelectric thin film, making a "MFSFET". The polarization of the ferroelectric film can be controlled by the gate, and depending on which state it is in, will alter the conductivity of the silicon channel, which can be measured by driving the FeFET with a gate bias lower than the coercive field. As this type of device requires direct contact with the doped silicon channel, perovskite-based ferroelectrics struggle, as diffusion of e.g. lead from ferroelectric perovskites into silicon occurs easily [18].

More recently, the ferroelectric tunneling junction was proposed. This junction works by the principle that a remanent polarization slightly bends the band structure of nearby materials, causing an asymmetry in tunneling currents depending on which polarization state the device is set to.

One final device that has been proposed is the so-called Negative Capacitance FET (NCFET), which is not a memory device, but rather a computing device. The NCFET works by stabilizing an otherwise unstable negative capacitance state in the ferroelectric device using a regular capacitor. A negative capacitance can be utilized for a so-called step-up voltage transformer. Essentially, as a low voltage is applied to one side of the capacitor, the voltage on the other end increases. This allows for lower-energy gate modulation for computation devices with a subtrehshold slope of less than 60 mV/Decade.

2.2 Measuring Ferroelectricity

The strength of ferroelectricity is evaluated using the remanent polarization, P_r. This quantity represents the amount of permanent dipoles leading to the ferroelectric switching behavior per unit area of the device. Measurements of this may be conducted by constructing a metal-insulator-metal (MIM) capacitor and measuring the current passing through this as a function

of the applied voltage. As the capacitor accumulates charge, a current is measured equal to the derivative of charge in time. The charge stored on a capacitor is proportional to the bias applied across it as

$$Q = CV \tag{1}$$

Where C is the capacitance. This means that the current passing through an ideal capacitor can be written as

$$I = C\frac{dV}{dt} \tag{2}$$

Consider a ferroelectric capacitor with permanent dipoles oriented to the right. An applied bias causes charges to accumulate on the electrodes. Unlike a normal capacitor, the ferroelectric capacitor retains its internal polarization until the external electric field reaches E_c. At that point, the internal dipoles switch orientation. As they switch orientation, a physical movement of charge occurs within the crystal. This yields a large current spike as charges rapidly relocate. After the ferroelectric switching has occurred, the charges continue to accumulate linearly with increasing bias. Thus, for a pre-set ferroelectric MIM capacitor, the I-V characteristics should look like a square wave with a spike at the coercive field when the polarization switches, given a linear change in bias, such as in figure 3.

The integral of this current spike corresponds to the total charge deficit created at the boundary when the switching happens, i.e. it is a direct measurement of the polarization with a scaling factor equal to the area of the capacitor.

2.2.1 PUND

The PUND (Positive-Up Negative-Down) method creates an easy way to measure the ferroelectric peak area by measuring the current for several consecutive voltage pulses. The measurement utilizes five voltage pulses, shown in Figure 3. The first pulse sets the ferroelectric into an initial state. Two consecutive pulses are then applied in the opposite direction from the initial pulse, followed by two more pulses in the initial direction. The first pulse of each pair will then be switching the ferroelectric, yielding the ferroelectric current peak, while the second pulse will merely charge a capacitor. By subtracting the current of the first pulse from the second in each pair, one can isolate the ferroelectric current for easy integration.

Plotting the cumulative integral of the current spike, scaled by the area, versus the applied potential, provides a hysteresis plot with only the ferroelectric contribution. The remanent polarization for a device is defined as half the polarization difference between the high- and low polarization states, i.e. the two states at 0 bias.

2.2.2 Endurance and Wake-up

The two largest issues facing hafnia-based ferroelectrics is the wake-up effect and low endurance. The wake-up effect causes a weaker remanent polarization that grows with time until it reaches a final saturated value. This growth was initially thought to be proportional to the number of cycles in the film [19]. It was later found, however, that the wake-up effect was dependent on

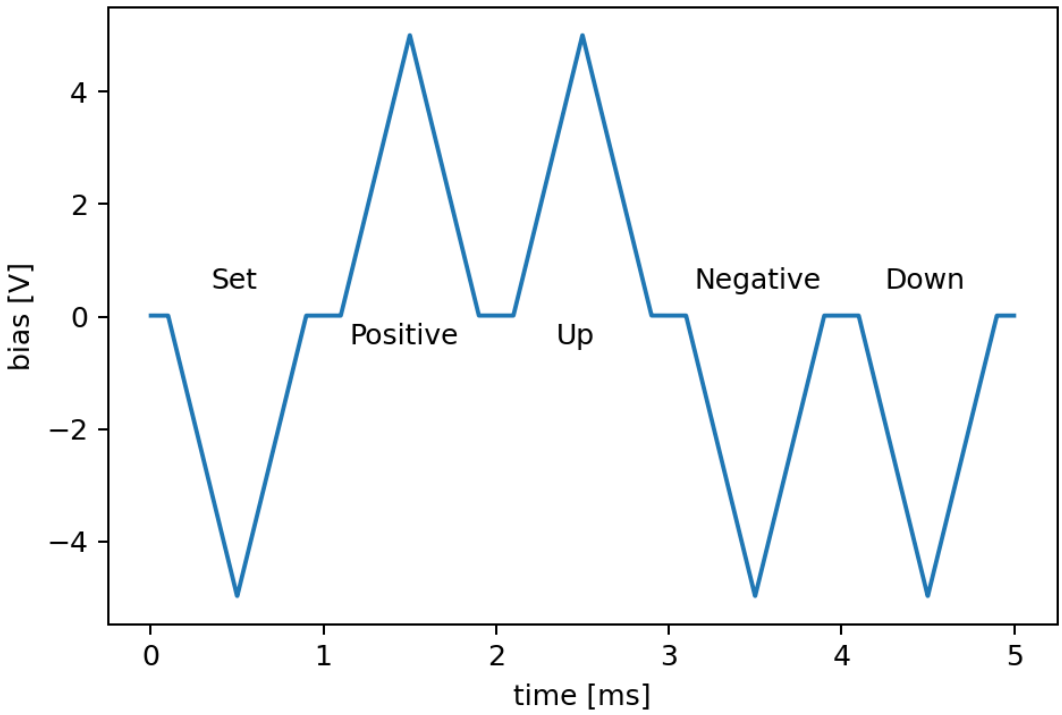


Figure 3: The PUND measurement scheme measures the current for the voltage pulses illustrated above. By finding the difference in current between the two pulses in each pair, one can find the strength of the ferroelectricity in a MIM strcture.

the duration of applied electric field, and that oxygen vacancies were redistributed during this time [20].

Compared to perovskites, hafnia-based ferroelectrics also have a low endurance, with some of the longest-lasting devices only reaching the order of 1 billion cycles, whereas perovskites only break down after approximately 10^{15} [18]. One cause for breakdown in hafnia-based devices is due to the high coercive fields relative to perovskite structures, which in hafnia-based devices are around 1-2 MV/cm. This is around half the breakdown voltage, which means that the film is stressed as the device is cycled. As a point of comparison, the coercive field of perovskite ferroelectrics lie on the order of 0.1 MV/cm, meaning that these devices do not have this issue. Another cause for breakdown is suggested as being charge carrier injection. Fatigue due to carrier injection was found to be reversible by annealing the device to recrystallize it [21].

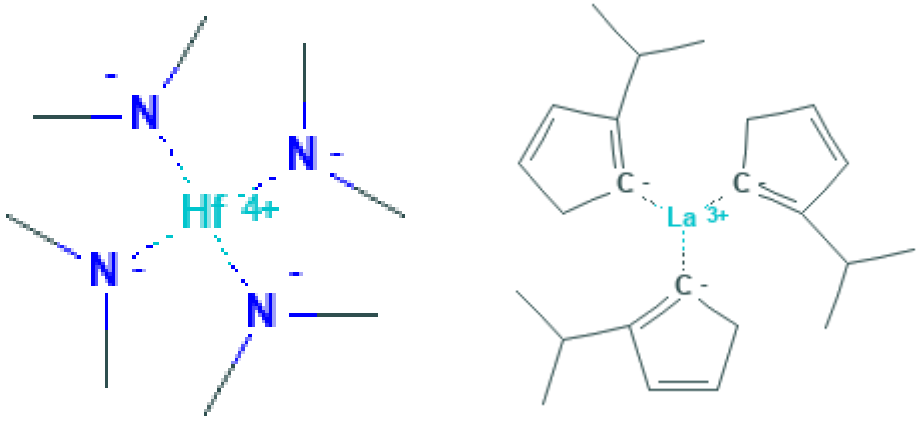
2.3 Device Processing

The processing required to make a ferroelectric MIM (MFM) capacitor is relatively simple, due to the fact that the top- and bottom electrodes easily act as the confining layers required to crystallize the doped hafnia-film into the ferroelectric phase. Thus, the processing involves the creation of a MFM layer, followed by lithography to define top contacts, as well as an etch step

to remove the top electrode material between the devices.

2.3.1 ALD

ALD is a technique used to grow thin layers with atomic layer control. This is done by cyclically pulsing so-called precursor materials into the chamber followed by a reactant. The two pulses are separated by a purging step using an inert gas such as Nitrogen or Argon to remove remaining precursor or reactant. Which reactant to use depends on the type of film one wishes to grow. For oxides the most common reactants are water and ozone. The precursors used in ALD processes have been engineered specifically to allow a self-limiting growth of the material. In the case of hafnia, the precursor Tetrakis(dimethylamido)hafnium, TDMAHf, is used. This molecule consists of a hafnium atom surrounded by four methyl amide groups. The precursor for lanthanum oxide, Tris(IsoPropylCycloPentaDienyl)lanthanum, iPrCp)$_3$La, has a similar structure, see Figure 4 for visual representations.



(a) TDMAHf. (b) (iPrCp)$_3$La

Figure 4: The molecular structure of the two precursors primarily implemented during this thesis [1]

These molecules react with OH groups on the surface of oxides such that the dimethylamide (DMA) groups bind to the hydrogen and leaves the oxygen free to bind with the center atom. In the case of TDMAHf, this causes two of the DMA groups to detach in the initial pulse, leaving the hafnium atom bound to two oxygen atoms as well as the two remaining arms. In the oxidation pulse following, the arms steal a hydrogen from the injected water and leaves a free OH group to bind to the hafnium, thus finishing the oxidation of the hafnium and resetting the top layer to begin the process with the next pulse. See Figure 5

Note that during each step of the cyclic process described above, it is limited by the chemistry of the surface, thus ideally only allowing a monolayer of material to be grown in each cycle. In a real system however, many different factors can disrupt this ideal, self-limiting, process. A good ALD recipe aims to reduce these sources of errors that will be described below.

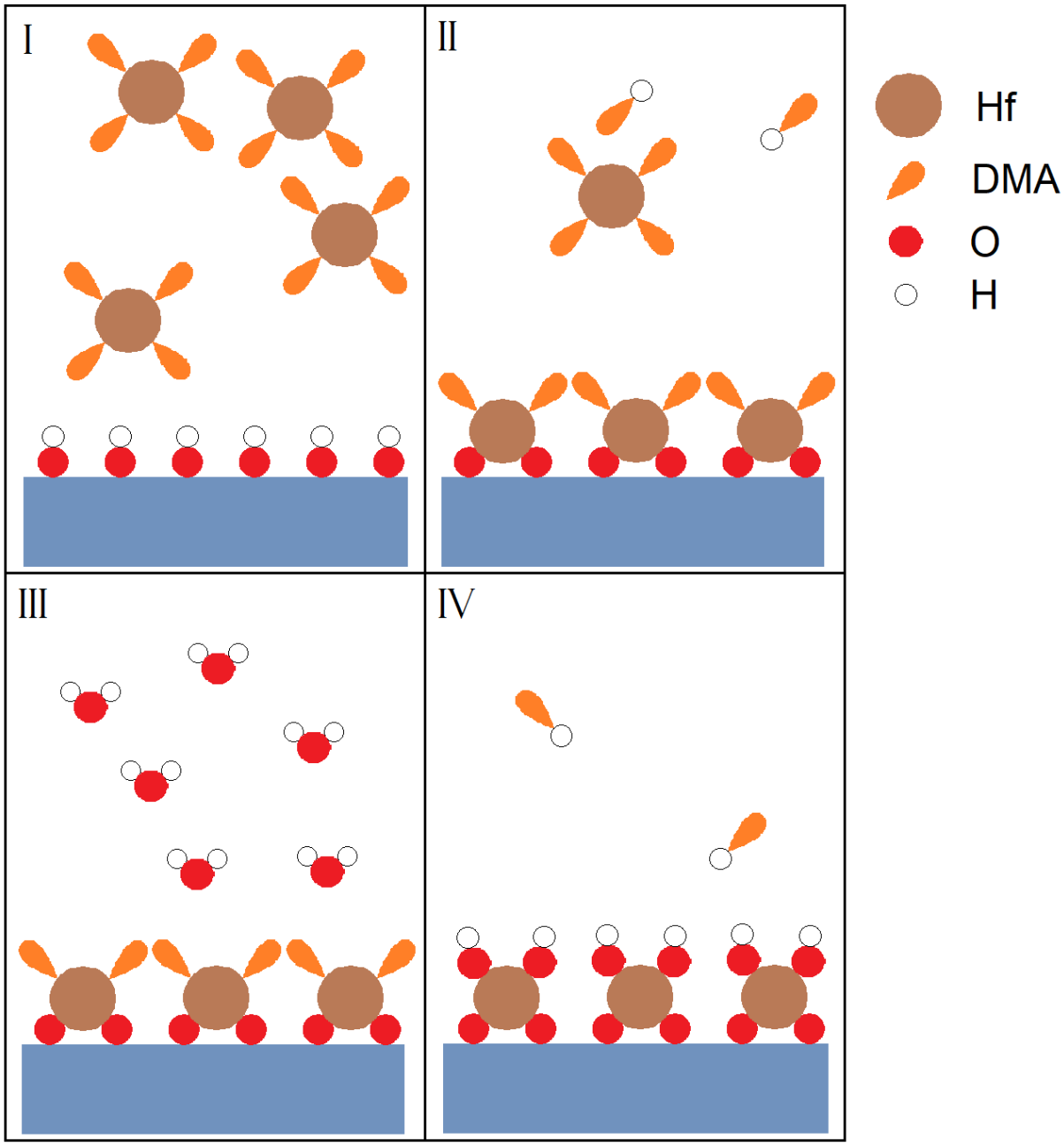


Figure 5: Illustration of the ALD process for HfO_2 using TDMAHf. The process begins with a substrate with OH groups on the surface as the precursor (TDMAHf) is pulsed into the chamber (**I**). The chamber then reaches saturation as the DMA groups bind to hydrogen, leaving the oxygen bound to the hafnium (**II**). The remnants are purged from the chamber and the reactant (water) is pulsed into the chamber, saturating it (**III**). The water molecules react once again with the DMA, while attaching to the hafnium (**IV**). This leaves a surface layer of OH-groups which allows the repetition of the process, starting from (**I**)

In a typical thermal ALD tool, the user has control over several variables that each impact the growth in their own ways. Primarily, the variables which influence growth the most are the precursor temperature, chamber temperature, and dosing and purging time(s).

The precursor temperature determines the vapor pressure of the precursor. Some precursors such as TDMAHf are solid at room temperature and have no significant vapor pressure. Heating up the material allows vapors to form which can be carried to the chamber where the reaction happens. If an insufficient precursor temperature is set, the chamber will not be saturated properly which can result in inhomogeneous deposition. However, precursor temperatures may not be set too high, as this can cause the precursor to decompose [22]

The deposition temperature determines how the precursor and reactant behave in the chamber. Depending on the precursor used the edge-cases for high and low temperature depositions may vary. Commonly referenced is something akin to Figure 6 (above) which shows the so-called ALD window where Growth Per Cycle (GPC) is constant or barely dependent on temperature. The four edge-cases describe what may happen depending on which precursor is used. Condensation refers to the precursor failing to remain in gas phase at low temperatures, resulting in deposition of the precursor rather than ALD. Some precursors may have a low reactivity at low temperatures, resulting in lower deposition rates. At high temperatures the precursor might decompose, losing its engineered properties, causing it to cease reaction with the reactant and remain as it is on the substrate, again resulting in higher deposition rates. Lastly, higher temperatures may cause desorption from the substrate yielding a loss of material and lowering the GPC.

The dosing time, t_d, is the time during which the corresponding precursor or reactant is introduced to the reaction chamber before the subsequent purging step. Insufficient dosing times can again result in incomplete deposition which produces an overall reduced deposition rate. As the dosing time increases, the chamber reaches saturation and complete deposition is observed. For excessively long dosing times, however, the abundance of material may not be properly removed in the subsequent purging step which can result to remnants of the precursor reacting in gas-phase with the reactant, causing chunks of material to form in the chamber. These chunks can then deposit on the substrate as well as cause contamination inside the chamber. Furthermore, an increased dosing time leads to increased material consumption which causes the precursor to deplete faster than necessary.

The purging time, t_p, is the time during which the chamber is purged of the vapors from the previous dose. If an insufficient purging time is used the same gas-phase reactions may occur that were described previously. As the purging time reaches a sufficient value, further increases to this variable have barely any consequence for the resulting deposition of the film. Excessive purging times have been found to slightly reduce GPC due to removal of material from the substrate, but these effects are minimal. The dependence on pulsing- and purging times can be schematically seen in Figure 6

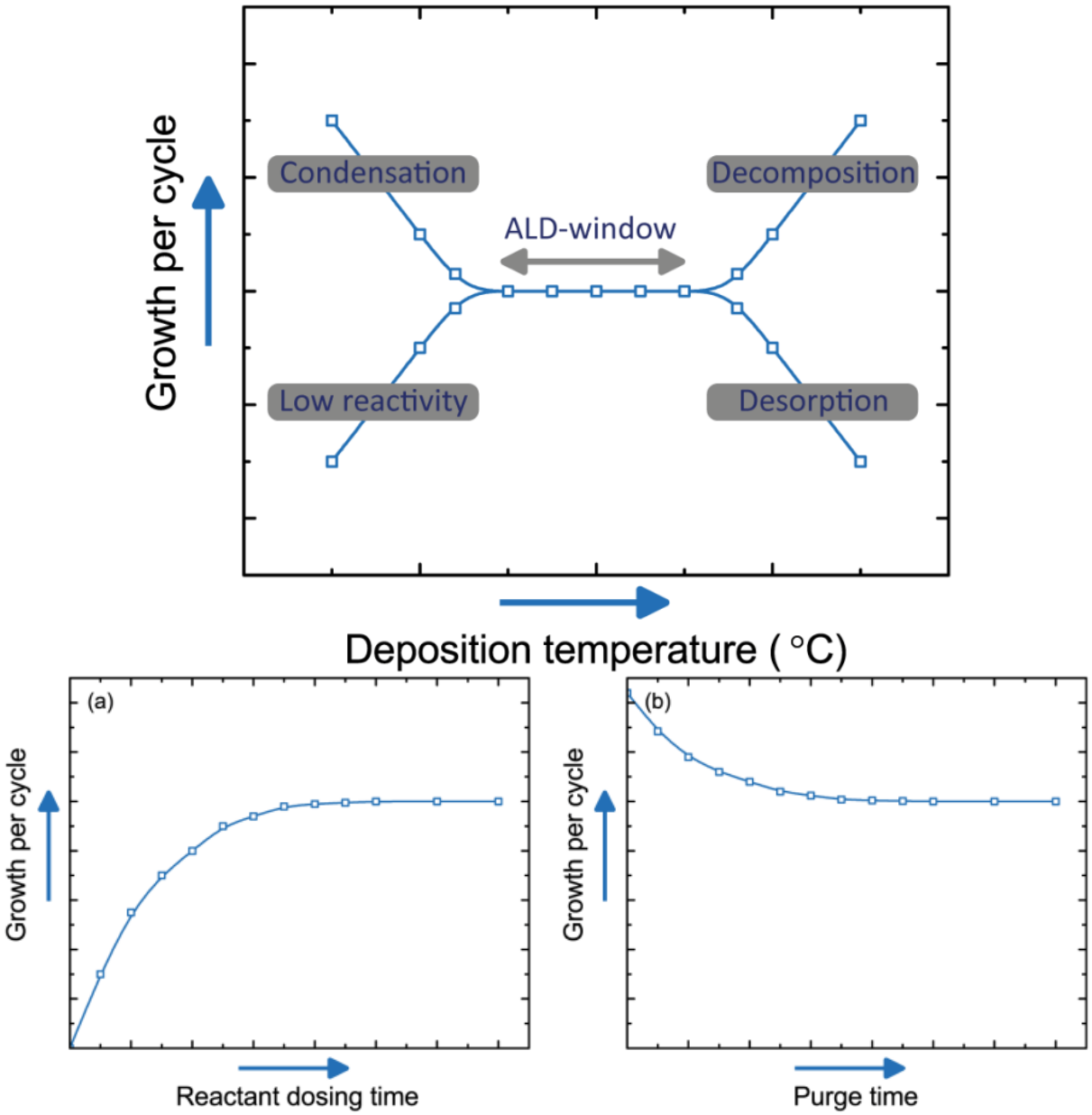


Figure 6: The images, reprinted from by M.J. Vos [2], shows **(above)** the oft-referenced ALD window defines the deposition temperature region in which the GPC is relatively constant with temperature. At the high- and low temperature regions, one or more effects may result in changes to the GPC. **(below)** the saturation of ALD with respect to pulse time and purge time. **(a)** A short pulse time results in insufficient saturation of the chamber resulting in lower deposition rates. **(b)** Conversely, a short purging time results in gas-phase reaction, causing particulates to adsorb onto the substrate in a non-self-limited manner, resulting in increased deposition rates.

2.3.2 Ellipsometry

Ellipsometry is a method with which one can easily find the thickness of thin films of materials. An ellipsometer shines light with varying wavelength at a sample with a regular surface structure, which reflects the light into a detector. The change in polarization is measured using the amplitude change, Ψ, and the phase change, Δ. The results are fitted to a material model to find the proper thickness of the material given the polarization data. Provided that the correct model is used, ellipsometry can provide information about the material thickness with a resolution of an atomic layer. However, if an incorrect model is used, one may receive erroneous information.

2.3.3 PVD techniques

Physical Vapor Deposition (PVD) techniques are used in microprocessing to deposit thin films. Unlike CVD processes (such as ALD), these techniques do not rely on chemical reactions to deposit the resulting film, but ratherddd on physical adsorption of the to-be-deposited material with the substrate. The two PVD techniques employed in this thesis were Sputtering and Evaporation.

Sputtering is a somewhat conformal PVD technique, that deposits material uniformly on the sample. The sputterer uses plasma sputtering with Argon (either with an RF or DC plasma) to chisel away material from a material source target. The material then freely travels around the deposition chamber at a relatively high pressure, causing the conformal coverage of the sample. To ensure uniformity across a large area, the deposition surface is usually rotated.

Evaporation on the other hand is a high-vacuum deposition technique designed for maximal anisotropy. The technique places the substrate at some relatively large distance away from the material source which is then heated to the point that particles begin desorbing from the surface. As the system is in a high vacuum, there is little interaction between particles, causing them to travel in a straight path until they hit something which they then stick to. For a sample placed sufficiently far away, this will mean that incident particulates are essentially orthogonal to the sample surface, causing little-to no sidewall coverage.

2.3.4 UV-ithography

Lithography is the collective name of small-scale pattern transfer. Lithography processes generally involve the patterning of a polymer resist layer which then acts as a mask for future processes. In UV-lithography, a aresist layer is created by spinning a sample with a polymer-solution on it at a high angular frequency, usually in the 1000s of revolutions per minute (RPM). After spinning, the sample is heated to allow the resist to bake, during which time it hardens. The baking time is usually very precise, as too long baking may result in a hardening of the resist which makes chemical removal difficult. The sample is then exposed to a UV-source while covered by a mask. The exposed areas will either weaken (if a positive resist is used) or harden (if a negative resist is used). After the exposure, the samples are placed in a chemical developer or remover, which dissolves the weak areas of the resist layer. Thus, if a positive resist is used, the exposed areas will leave holes in the resist, whereas in a negative resist, the covered areas are removed.

2.3.5 RTA / FLA

The crystallization of the ferroelectric is achieved using Rapid Thermal Annealing (RTA) or Flash-Lamp Annealing (FLA). These techniques implement the use of high-intensity lamps to heat up samples. In RTA, the samples are rapidly heated to a set temperature, as detected by a thermocouple, where it is kept for a desired time. The FLA technique also utilizes high-intensity lamps, but only shine these onto the sample for a very short time. This is achieved by powering the lamps through a large capacitor discharge. Due to the rapid heating of samples in an FLA, a large temperature gradient is produced across the wafer. This gradient will depend on the duration of the flash, the intensity of the flash, and the heat conductivity of the material in the FLA. The best way to learn what parameters one should use to achieve a desired temperature is to use a simulation tool which accounts for the structure of the surface layers to calculate the reflectivity of the sample, and thus the resulting energy transfer.

3 Methods

3.1 Investigation of HfO_2/ZrO_2 Deposition

Prior to the creation of a lanthanum oxide deposition recipe in the ALD, an investigation was carried out to determine whether the materials in present use (HfO_2, and ZrO_2) were being deposited with optimal conditions. In particular, it was of interest to see whether these two were within their respective saturation windows with regards to pulsing and purging times. The recipes were both set to use the same pulse- and purge times, namely 1.6- and 5.0 s respectively, followed by identical H_2O pulses at 0.1 s pulse and 10 s purge. The reactor temperature was 200°C, and was left unchanged for all of the experiments. A rough study was carried out where each variable was altered independently (see Table 1) with one data point above the current value and one data point below. Should these reveal some gradient, additional measurements would then be performed to find the point of saturation for this variable.

Table 1: The initial pulse- and purge configurations

Sample	Pulse (s)	Purge (s)
1	1.0	5.0
2	2.0	5.0
3	1.6	1.0
4	1.6	10.0

3.2 Calibration of Lanthanum Oxide Deposition

As it had not been grown in the ALD-system prior to this thesis work, the correct growth conditions for the lanthanum oxide were to be determined before any device processing. This was done by finding saturation curves for each of the tool parameters. Initially, the appropriate precursor temperature was found by using the pulsing and purging times used with hafnia and zirconia, while increasing the source temperature. The source temperature is then adjusted and deposition carried out until no change in deposition rate is observed for higher temperatures.

The lanthanum oxide precursor Tris(IsoPropylCycloPentaDienyl)lanthanum, $(iPrCp)_3La$, was used for this project. The most pressing concern with this precursor was its high temperature requirement. In order to produce sufficient vapor pressure for ALD the source has to be heated to at least 150°C. The initial heater temperature was thus set to 160°C, with the reactor temperature set to 200°C. The temperature was then increased in steps until the maximal accepted temperature was reached. The ALD system has a maximal heater temperature and specified maximum source temperature of 200°C. To avoid potential damages to the system, the highest source temperature investigated was 190°C. The measurement was conducted on a 2" Si wafer where 200 cycles were produced with the La-pulse/purge/H_2O- pulse/purge of 1.6/5/0.1/10 seconds.

As the results will show, the chamber did not saturate properly which resulted in a gradient-like behavior, as this is most likely due to insufficient precursor heating which could not be achieved, it was decided that samples for the ferroelectric HLO would be grown in the area

of the chamber with the highest overall deposition rates. However, as the recipe produces a gradient even in this area, the resulting HLO films will have an uncertainty in La concentration depending both on where the sample was placed in the chamber as well as where on the sample one measures. This uncertainty will be reflected in the accuracy of the results.

3.3 MFM Capacitor Process Flow

The capacitors used in this project were processed starting from a polished silicon wafer following the process flow depicted in Figure 7a. The electrodes were deposited using a plasma assisted sputtering system, the AJA Orion 5. The contacts were made with TiN sputtered with an RF plasma at 150 W (resulting in a DC bias around 430 V). The sample was placed on a carrier wafer which was set to rotate in the holder at 40 rpm to allow for uniform coverage. Although a thickness monitor was installed in the system, the devices were created at a fixed deposition time of 10 minutes rather than following the thickness monitor. This yields a thickness of approximately 10 nm.

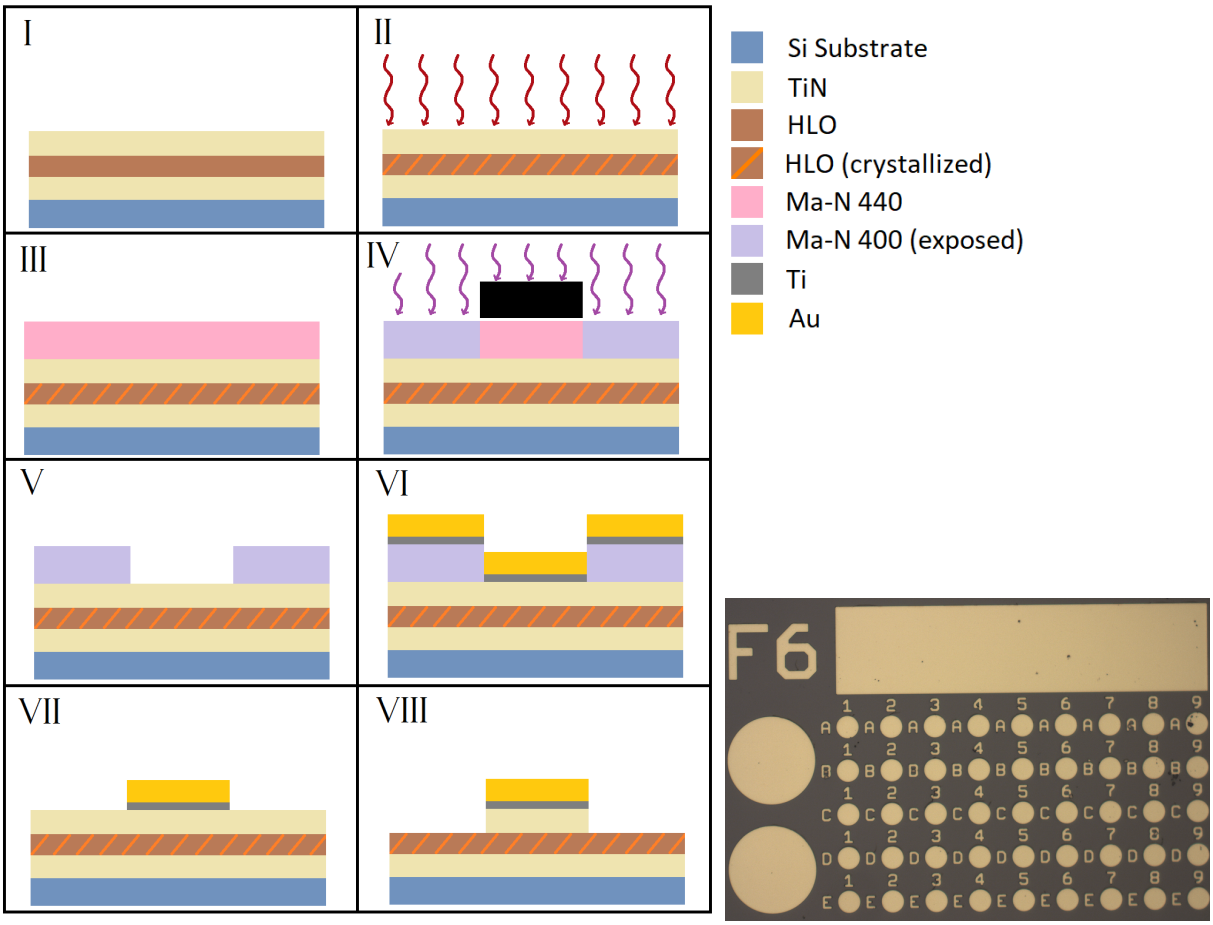
The ferroelectric oxide was then deposited using the Picosun Picohot ALD. The source temperature of the TDMAHf bottle was set to 100°C and the $(iPrCp)_3La$ to 190°. The pulse- and purge times for both sources was set to 1.6 and 5.0 seconds respectively. The pulse- and purge times for the water were set to 0.1 and 10.0 seconds. The rate of lanthanum was varied using the thickness as a metric for concentration, i.e. a sample with 150 Å of HLO, where 15 Å is from lanthanum oxide is denoted as having 10 % La. Additionally, the material was deposited such that the lanthanum oxide was evenly deposited within the material.

After the top electrode of TiN was deposited in the same manner as the bottom electrode, the samples were crystallized. This was done either by RTA or FLA. In the RTA the samples were rapidly heated to the target temperature in a nitrogen atmosphere and kept there for 30 seconds followed by rapid cooling. In the FLA, the samples were first pre-heated and then subjected to a short light flash. The FLA does not allow a target temperature to be set, rather a pulse duration and pulse energy is defined, and the resulting temperature is measured using a pyrometer and thermocouple, each reading the temperature from the bottom of a carrier wafer.

After the samples had been annealed, they were patterned using UV lithography. Samples were cleaned with Acetone and IPA and then placed on a hot plate at 95°C where they rest for at least 3 minutes to dehydrate. After the heating, the sample is quickly cooled and then placed on a spinner where it is covered in ma-N 440 (negative resist). The spinner is then turned on to 6000 RPM for 40 seconds, after which the bottom side of the sample is cleaned with acetone and then baked for exactly 3 minutes at 95°C.

The samples are then placed in a mask aligner where they are exposed to a UV source for 30 seconds under a mask. After exposure, the samples were placed in ma-D 532/S developer for 3 minutes and then swirled in water while held with tweezers for 3 minutes. The surface of the sample is inspected through microscope for remaining particulates of resist, and eventually the developing/swirling is repeated for an additional 30-60 seconds each to remove residual resist.

5 nm of Ti followed by 200 nm of Au is then deposited using an evaporation technique. The resist is removed along with the gold covering it by placing the samples in Acetone for five minutes. A pipette may be used to carefully blow acetone onto the samples while held by tweezers to remove the gold from the surface. The samples are finally cleaned using IPA.



(a) (b)

Figure 7: **(a)** The full process flow, starting with the as-deposited thin films of TiN-HLO-TiN (I). The MIM structure is then annealed using either RTA or FLA to crystallize the HLO (II). Following this, a polymer resist is spun (III) and exposed with UV light from under a mask (IV). The un-exposed resist is removed using a chemical developer (V). Ti and Au is evaporated onto the sample (VI) and the remaining resist is removed along with the metal on top of it (VII). Lastly, the now-exposed TiN is etched away (VIII). **(b)** A finished sample, as seen through an optical microscope. The small circular pads are devices, with a radius of 25 μm each. This pattern repeats across the full sample, resulting a few thousand devices per sample.

Lastly, the now-exposed TiN will be etched away in APM. 25 ml of H_2O is mixed with 5 ml of 25 % Ammonia and 10 ml of 30 % H_2O_2 and heated to 60°. The samples were held in the APM for 10-20 seconds (or until the TiN is entirely removed) and then washed in water and blow-dried with an N_2-gun. This resulting samples can be seen in Figure 7b

3.4 Ferroelectricity Measurements

Measurements were performed on the Semi-Auto probe station TS2000-SE, using test modules programmed in EasyExpert using the Keysight Semiconductor Device Parameter Analyzer - B1500A. Two probes are used to measure on the devices. The probes are connected to the B1500A with both WGFMU (Waveform Generator/Fast Measurement Unit)- and SMU (Source Measurement Unit) cables. First, the two probes are placed on any two large pads nearby the device under test (DUT). A ramping bias is applied through the SMU cable to cause a breakdown of the oxide, creating a conductive path through the oxide. One probe is then moved to one of the devices, while the other remains on its shorted pad. This ensures that the only capacitive element between the two contacts is the oxide under the DUT. PUND measurements are then carried out through the WGFMU cables. Measurement series on a single device consist of a wake-up followed by PUND measurement at a given bias. Three peak biases are selected: 3, 4, and 5 V. The wake-up measurement does 1000 cycles of alternating triangular waves with a peak bias. The PUND waves are applied with a frequency of 1 kHz, as can be seen in Figure 3

Endurance measurements are performed by cycling alternating triangular waves. Fatiguing is done at 10 kHz, whereas measurements are taken at 1 kHz. The PUND cycling is not done here as alternating triangular waves more closely match the expected operation in real devices. This results in PE curves with the dielectric polarization included, and will be seen in the data as the addition of a linear component of polarization versus electric field.

4 Results

4.1 HfO_2/ZrO_2 Investigation

Using the same base recipe for hafnia and zirconia (1.6 seconds pulse, 5.0 seconds purge), oxides were grown on a 2" wafer for 400 complete cycles. The thickness of the deposited film is measured with an ellipsometer at 70^o incidence angle. Measurements are taken at the center, following a polar pattern outwards, yielding a total of 32 points of data across the full wafer. The results are plotted in Figure 8, which shows a box plot distribution of the measured GPC for each point in a wafer. As can be seen in subfigures **(c)**, and **(d)**, the growth of zirconia is stable with changes, aside from a few points of increased deposition rate in **(c)**. This implies that this recipe lies within the saturated region of Figure 6 (below). On the other hand, the data indicates a large spread in the deposition rates across the wafers for both of the altered hafnia runs in **(a)**, and **(b)**. The variations in these deposition rates, however, do not match those one would expect as a result of pulsing- or purging times outside of saturation.

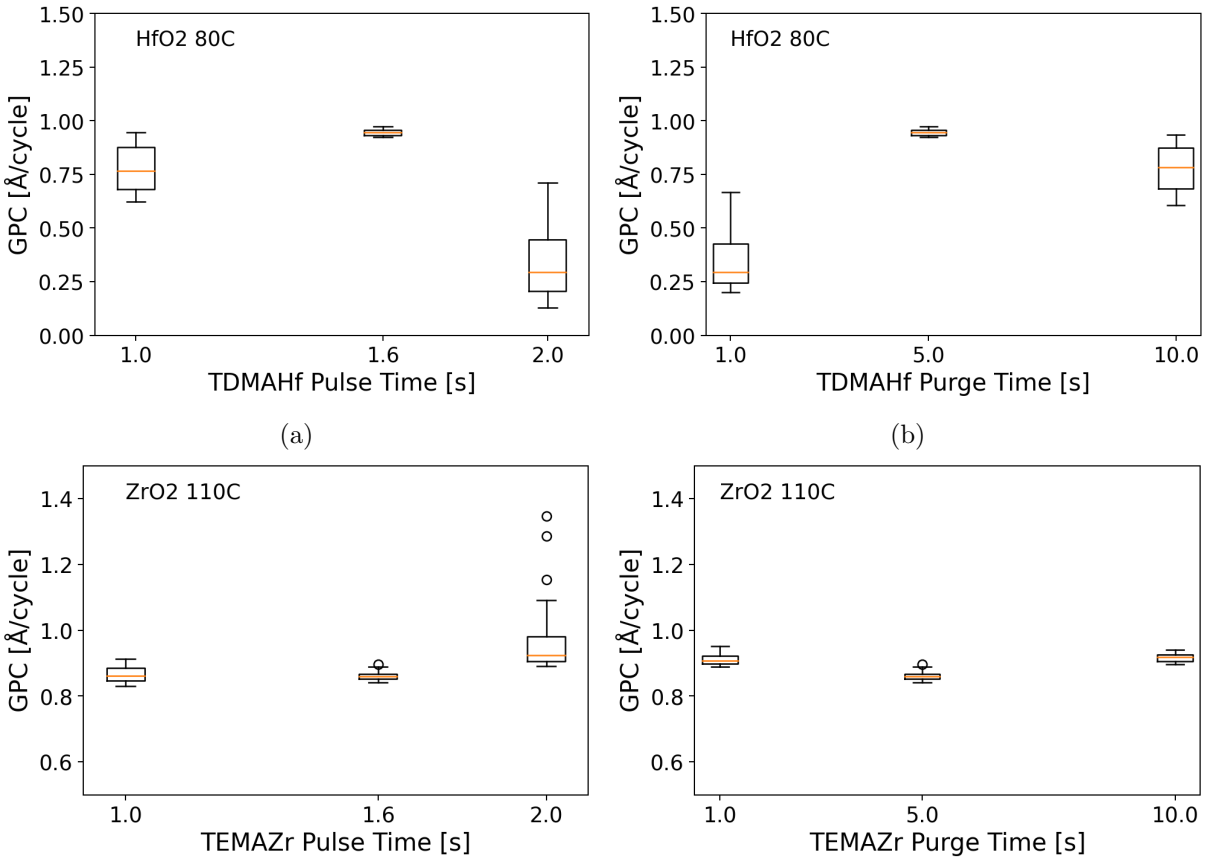


Figure 8: The initial results for the pulse and purge times tests. The data shown is the collected thickness data across the full 2" wafer with varying parameters. **(a)** and **(b)** show the pulsing- and purging time variations for hafnia, **(c)** and **(d)** show the data for zirconia.

In Figure 9, the heat maps for the deposited material is shown, normalized by number of cycles to indicate the growth rate. It is from this data obvious that a gradient in the growth has appeared, with increasing GPC towards the TDMAHf inlet.

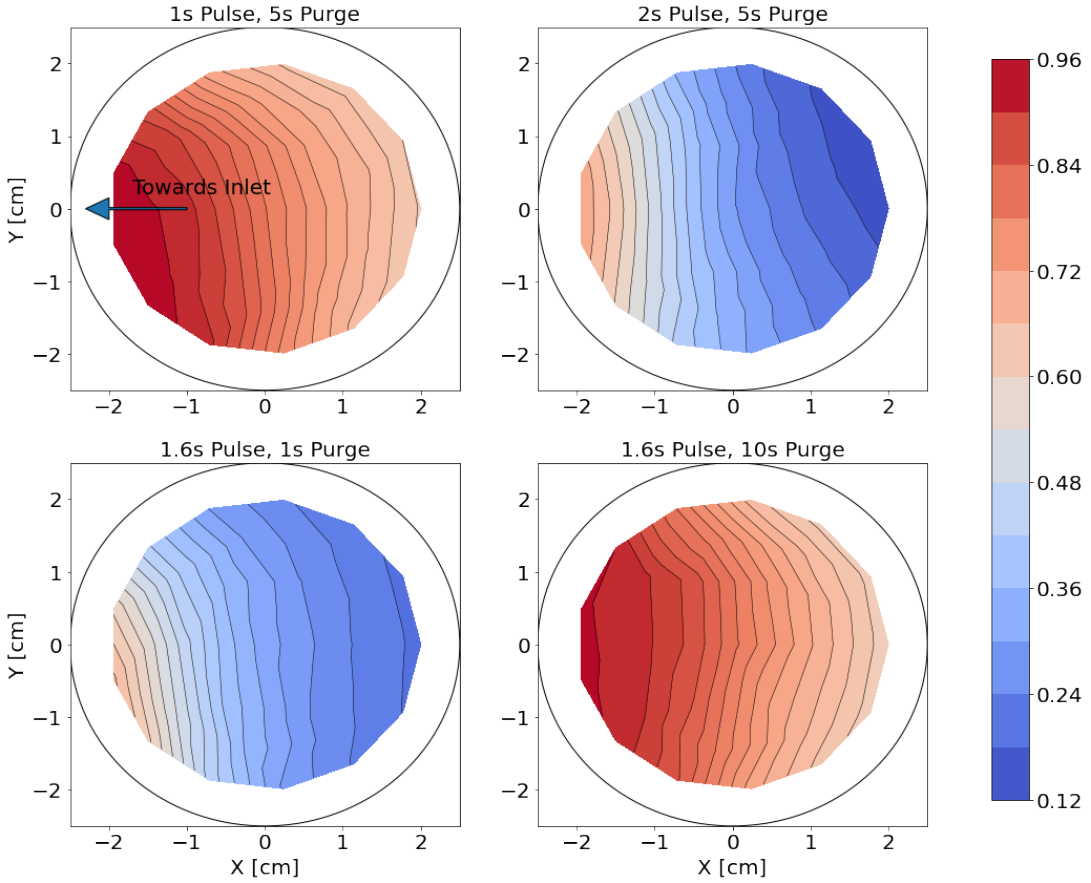


Figure 9: The deposition maps showing the growth per cycle (GPC) of the four altered hafnia recipes. A clear gradient is observed in the same direction for each sample. Note that the samples share a scale, so as to highlight the large difference in GPC between the four samples.

To verify the stability of the recipe, an additional deposition was made using the default conditions. The resulting deposition map is compared with the one created before. Shown in Figure 10 is the heat map of the first reference sample created, as well as the heat map of the newer deposition using the reference. The appearance of a gradient in the newer reference run suggests that something has changed with the conditions of the tool since the investigation began.

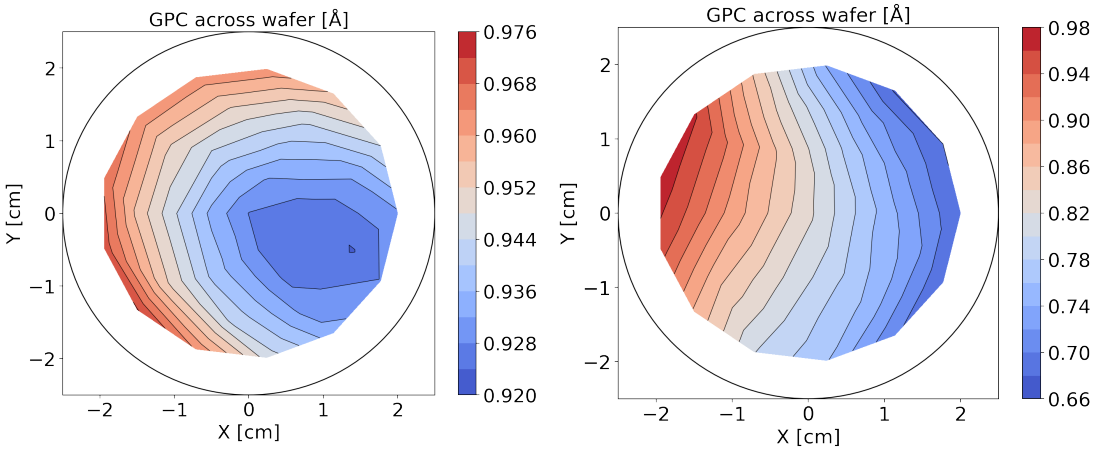
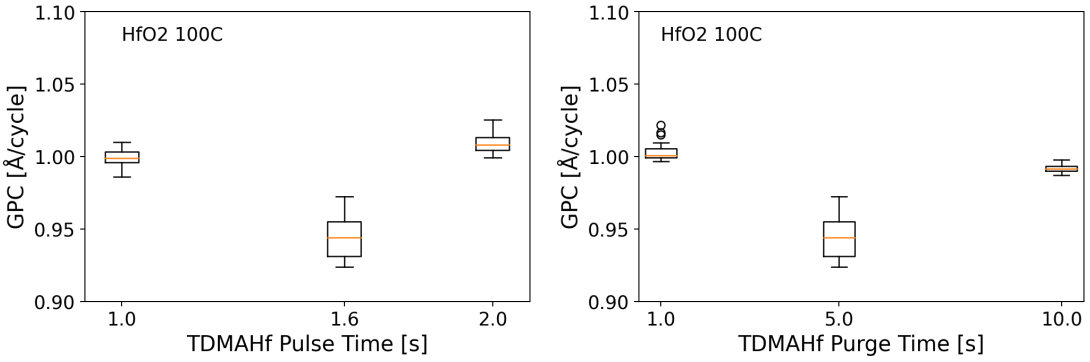


Figure 10: Two reference samples, **(b)** taken one month after **(a)**, using the same (nominal) configuration for hafnia deposition. The difference in results indicates there are some issues with the deposition.

The gradient-like behavior sloping towards the inlet suggests a low vapor pressure. This may be due to insufficient heating of the source, however, as the same parameters had been used previously, it was concluded that the low vapor pressure was a result of the source running low on precursor. The source bottle was removed and weighed by lab staff. Although it was found to still contain 14 g of precursor, switching the bottle and increasing the source temperature to 100°C solved the issue. This can be seen in Figure 11, where the altered deposition recipes for hafnia were once again implemented, and compared to the first reference sample. The data now indicates that increasing the temperature to 100°C improved the precision in the deposition rate across the wafer, suggesting that the increased vapor pressure yielded better chamber saturation. The largest difference in GPC across any of the four wafers was 0.04 Å/cycle, as compared to the reference recipe which has a largest variation of 0.06Å/cycle. As can be seen more clearly in Figure 12 the largest variations occur near the edges of the samples compared with Figure 10a which appears does sport some consistent gradient, reflected in the width of its box in Figure 11



(a) (b)

Figure 11: The thickness map data for the wafers deposited at 100°C with the reference sample being the original deposition recipe at 80°C source temperature

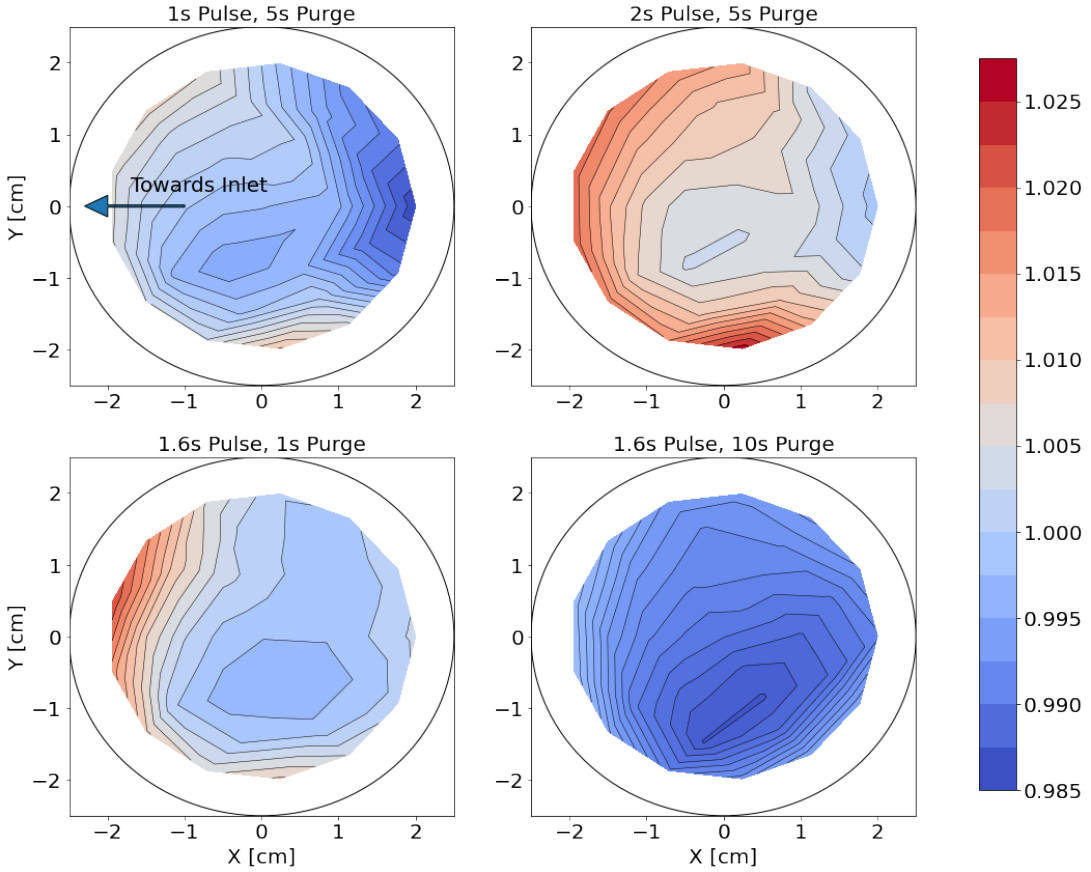
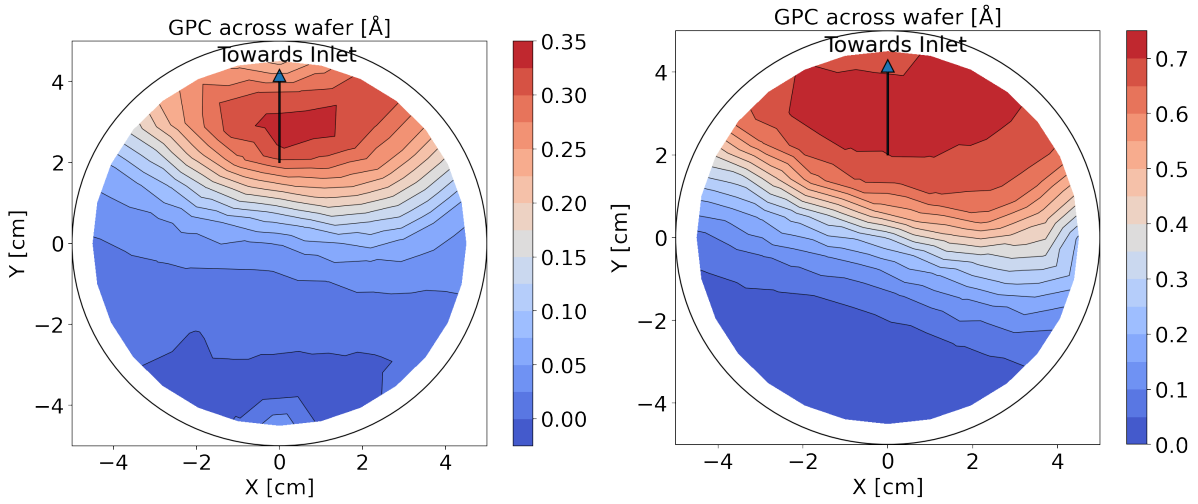


Figure 12: The heat maps showing the GPC for the four altered recipes when grown with a source temperature of 100°C.

4.2 Lanthanum Oxide Deposition

Using the Picosun Sunale R-100 ALD system, the initial pulse- and purge times the lanthanum oxide were set to 1.6 s and 5 s respectively. These values are the same as for hafnia and zirconia deposition processes that have been shown to work well for those two oxides. The initial source temperature was set to 160°C as this exceeds the theoretical minimal value for deposition by 10°C. The chamber temperature is fixed at 200°C for every process. Measurements of the film thickness were taken on 2" Silicon wafers placed in the middle of the 4" sample area using an ellipsometer with a Cauchy model. The MSE values for the measurements were around 10, implying a good fit was achieved.

The first deposition test yielded only small amounts of lanthanum oxide, with a rate between 0 and 0.1 Å/cycle across the entire wafer. An increased pulse time of 3 seconds showed no change in resulting deposition. Increasing the source temperature to 170°C yielded deposition at a gradient ranging from 0 to 0.2 Å/cycle across a 2" wafer. Further increasing the temperature of the source bottle to 175°C again yielded a gradient ranging from 0 to 0.35 Å/cycle shown in Figure 13a, where deposition had been made on a clean 4" silicon wafer and measured using the ellipsometer.The temperature was increased to 190°C and another 4" wafer was measured at this temperature, see Figure 13b. This configuration also yielded a steep gradient with essentially no deposition in a third of the chamber, but with a large area of relatively uniform deposition at a rate of around 0.7 Å/cycle, which is in the range of values reported within literature. As the source temperature was close to the specified maximum of the system, further temperature increases were not feasible. Due in part to time constrains, no alterations were made to this recipe with regards to the pulsing- or purging times. This configuration was thus what the following MFM capacitors were created with, while keeping the samples confined to the area of the chamber where the deposition rate is the highest, and the gradient is the smallest.

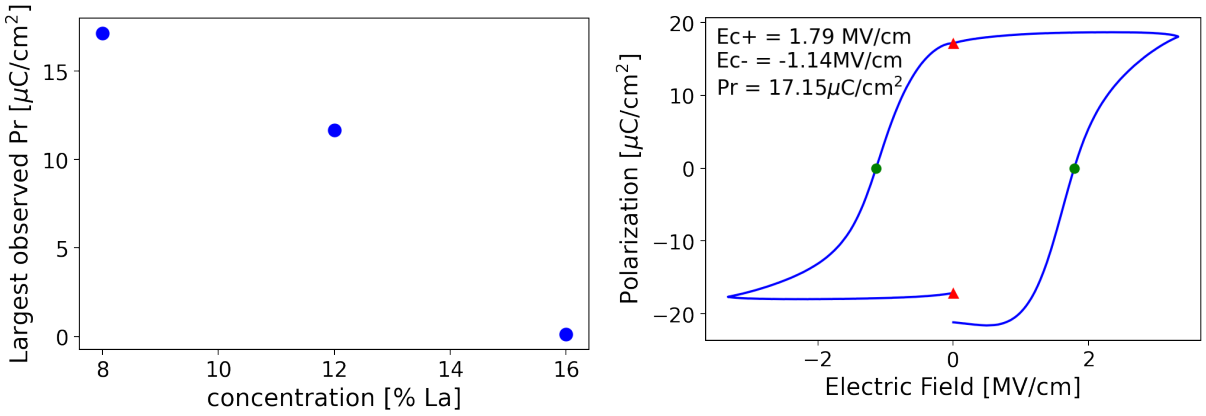


(a) 175°C (b) 190°C

Figure 13: The deposition maps of the lanthanum oxide as measured by the ellipsometer at two different source temperatures, 175°C in **(a)** and 190°C in **(b)** . The measurements show data points on a 4" si-wafer (covering the entire deposition area of the ALD) with 200 cycles of lanthanum oxide. Note the overall increase in deposition rate for the higher temperature.

4.3 MFM Capacitors

A first set of MFMs were created with the lanthanum oxide deposition at a source temperature of 175°C. These were created at three different concentration values: 8, 12, and 16 % lanthanum and annealed at 500, and 600°C after having had top electrode and gold contact sputtered onto them using a shadow mask. The measured remanent polarization for these samples can be seen in Figure 14a where a large remanence is seen for 8 %, a somewhat low remanence for 12 % and none for 16 %. In Figure 14b the P-E hysteresis curve is shown for the 8 % sample, with P_r and E_c indicated.



(a) (b)

Figure 14: **(a)** The first series of samples showed a strong remanent polarization at 8 % lanthanum with decreasing polarization for the samples created at 12 %. 16 % lanthanum showed no remanent polarization. **(b)** Shows the hysteresis plot for the sample with 8 % lanthanum, with the remanent polarization and coercive fields indicated. The fact that the hysteresis loop is not closed indicates that the polarization is stronger in one direction.

This motivated the final sample series to be centered around the 8 % point, this time with a source temperature . Samples were created at 4, 6, 8, 10, and 12 % lanthanum, with extra samples being made at 8 % lanthanum for a comparison between RTA and FLA. The RTA-samples were annealed at 500, 600, 700, and 800°C to find the onset temperature of ferroelectricity with a varying concentration. After annealing, however, it was noted that the samples were discoloured increasingly with increasing temperature, to the point where those annealed at 800°C were in parts dark purple rather than the yellow-golden color of TiN. After the lithography processing, it was also found that the time to etch away the TiN was longer for the samples annealed at a higher temperature, and the samples annealed at 800°C could not be etched at all, resulting in them being discarded. The discoloration is thought to be due to formation of TiOx, possibly through oxygen scavenging from the ferroelectric film.

From the remaining devices, PUND measurements were taken and the remanent polarization was plotted. The results in Figure 15 show that only the devices created with 4 % lanthanum were ferroelectric with a remanent polarization of around 20 μC/cm^2 when biased with the peak voltage at 5 V. In Figure 16a, the hysteresis curves for the three different biasing points is plotted. Here one sees that the remanent polarization increases with bias, indicating a relatively wide range of coercive fields for the domains in the crystal. In Figure 16b the coercive field has been plotted as a function of the peak bias for each sample with 4 % lanthanum. The samples show good consistency in coercive field statistics, with a slight increase in E_c with bias. The hysteresis loops were also plotted for the remaining concentrations annealed at 600 °C. The same data was acquired for the remaining concentrations as well, and has been plotted in figure Figure 17.

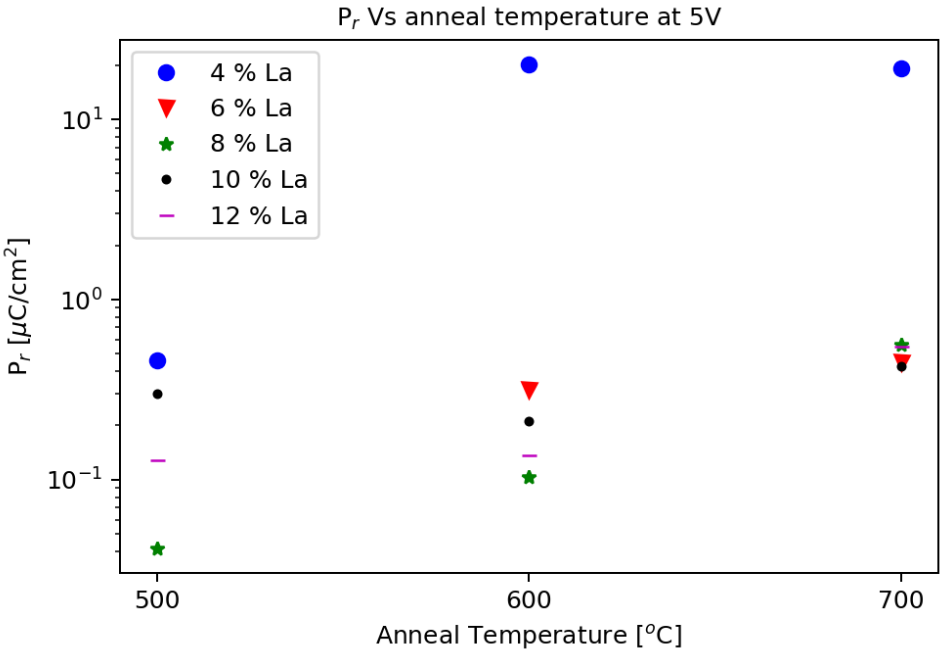
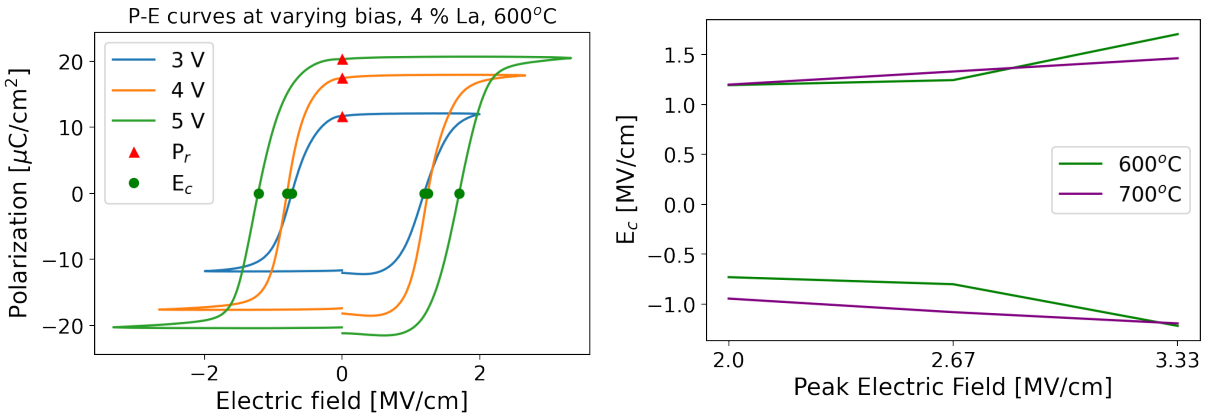
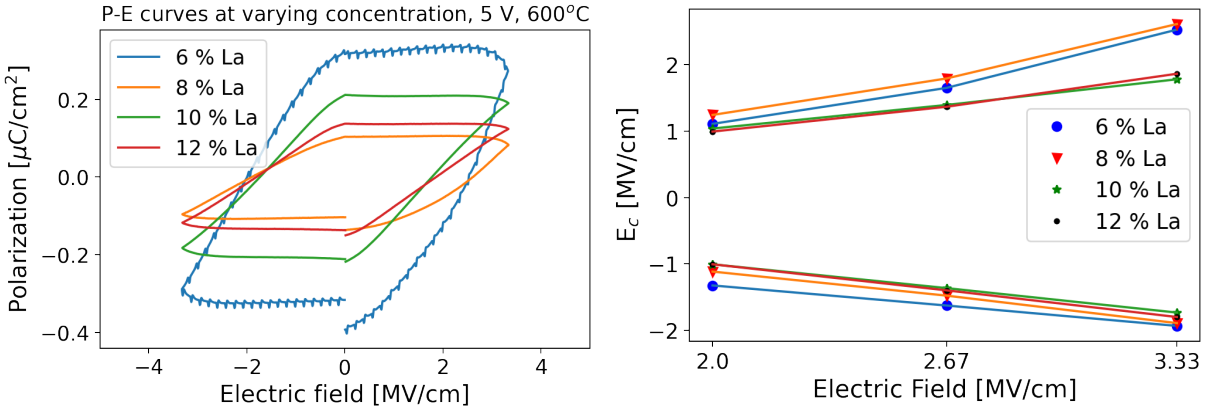


Figure 15: For the samples which were prepared, only those created with 4 % lanthanum thickness became ferroelectric. The onset of ferroelectricity lies between 500 and 600°C.



(a) (b)

Figure 16: The polarization data for the devices with 4 % lanthanum. **(a)** shows the P-E curves with the remanent polarization and coercive field points indicated. The data has been treated such that there is no discontinuity in the top of the hysteresis loop, and such that the two points approaching 0 electric field have the same remanent polarization. **(b)** shows how the coercive field changes with increasing bias. Ideally this field should be the same for each biasing point as only the dielectric current should increase with increasing voltage slopes.



(a) (b)

Figure 17: **(a)** shows the hysteresis loops for the devices at the other concentrations, annealed at 600°C, **(b)** shows their respective coercive fields as a function of the applied peak bias.

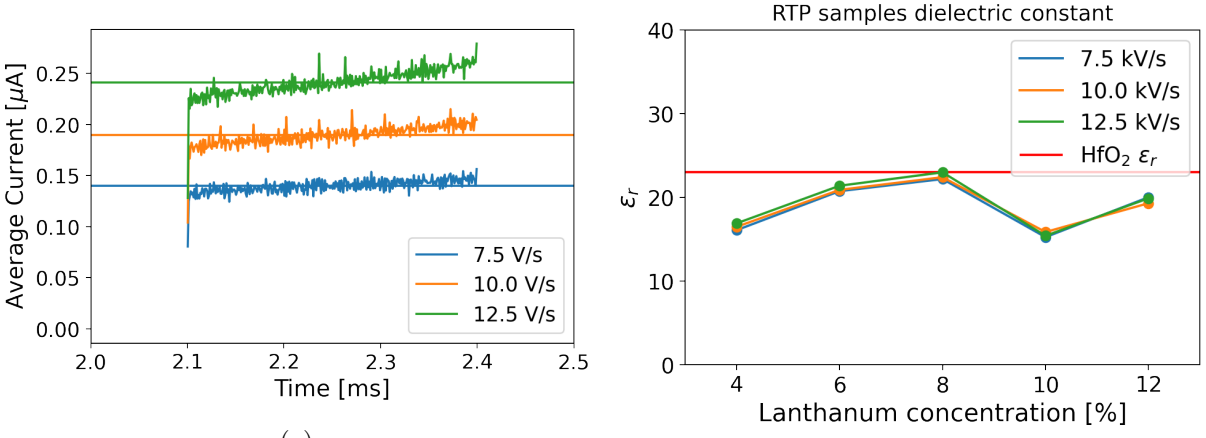
An attempt to find the true lanthanum content of the devices was made by considering the relative permittivity of the samples to be a linear combination between that of hafnia ($\varepsilon_r = 23$) and La_2O_3 ($\varepsilon_r = 27$). The relative permittivity can be found by calculating the capacitance. This is done by finding the current in the two secondary measurement peaks (denoted U and D in figure 3). The current is measured from the point where the current starts to spike, until 75 % of the peak, to avoid including the leakage current. Due to asymmetries in the measurement setup, the positive and negative current vary. The average of the magnitudes of current are thus considered as the "true" current for any given voltage slope, see Figure 18a. Since the voltage is increasing linearly at the same rate for the entire sampling range, the factor dV/dt is constant. The permittivity is thus easily found as

$$\varepsilon_r = \frac{Id}{A}\left(\frac{dV}{dt}\right)^{-1} \tag{3}$$

using the capacitor radius 25 μm and thickness of 15 nm, the resulting relative permittivities are plotted in figure 18b, with the hafnia permittivity indicated with a horizontal line. As can be seen, the permittivities measured this way do not lie between that of hafnia and La_2O_3, meaning that no connection can be made between this calculated permittivity and the true concentration. However, the large variations between relative permittivities are worth noting, as it is an indication of some difference in oxide structure or chemistry.

4.4 FLA Samples

As the only samples displaying ferroelectricity were those created with 4 % lanthanum, the remaining samples from that series were used for the FLA series. In total, three samples were created and were each annealed with the same flash duration, 1.5 ms, and energy, 19.5 J/cm^2, while adjusting the preheating temperature. The three pre-heating set-points were 250, 300, and 350°C, with a resulting simulated surface peak temperature of 450, 535, and 610°C respectively,



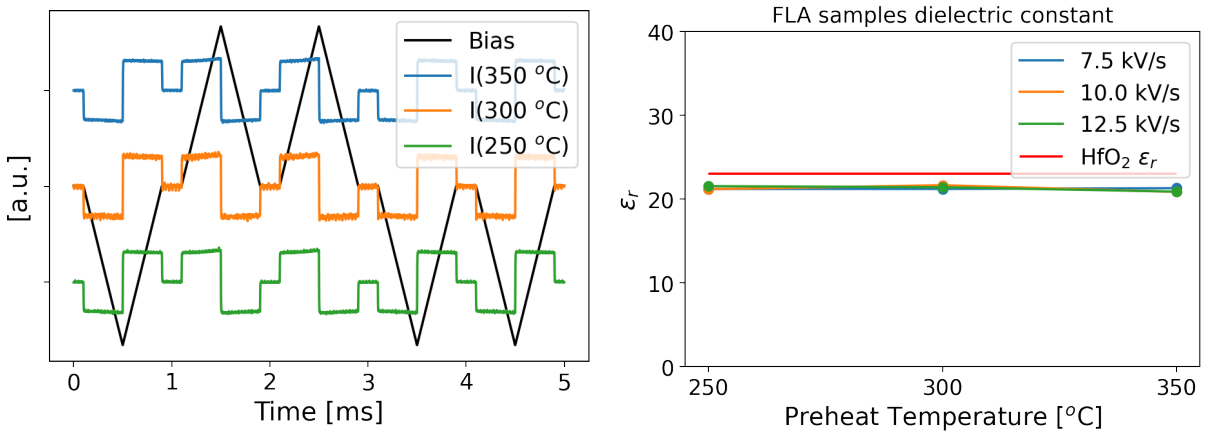
(a) (b)

Figure 18: **(a)** Shows the raw current data considered for calculations of relative permittivity, as well as the extracted median value of this current. **(b)** shows the calculated relative permittivity vs the lanthanum concentration of the samples.

and a simulated backside temperature of 302, 356, and 407°C. The backside temperature readout from the pyrometer indicated 374, 440, and 506°C respectively.

After the annealing process, the samples were slightly damaged as bits near the corners had broken off from the silicon substrate. In one of the FLA runs, the carrier wafer did also break as a result of the anneal process.

The current output data for the PUND measurements can be seen in Figure 19a, where it is clear that none of the three samples became ferroelectric. The measured capacitive current in each of the devices is nearly identical, and have here been plotted offset from each other to indicate their similarities. Notably, each of the three samples show no ferroelectric peaks. Using the same method as for the RTA samples, the relative permittivity is measured to be 21.3, with minimal variations between the three samples, this data can be seen in Figure 19b.



(a) (b)

Figure 19: **(a)** The current output data for the PUND-measurement of the samples annealed in an FLA. The currents have here been plotted offset from each other as they would otherwise overlap each other entirely. **(b)** Using the capacitive current and the known voltage ramp, the relative permittivity is calculated to be 21.3±0.16 for the samples.

4.5 Endurance

The devices from the sample with 4 % La, annealed at 600°C were subjected to endurance measurements. One device, shown in figure 21, was cycled 10 M cycles without showing indications of fatigue, however, the device appears to not be out of wake-up yet, this is clearly seen in the hysteresis loop, where an increasing remanent polarization can easily be noticed with increasing cycling number. For early cycles, one can notice antiferroelectric-like behavior, shown in blue the figure. Additional measurements for five other devices were taken from two different locations on the same sample to see the spread of the endurance. As can be seen in Figure 20, the devices behave very consistently across the sample.

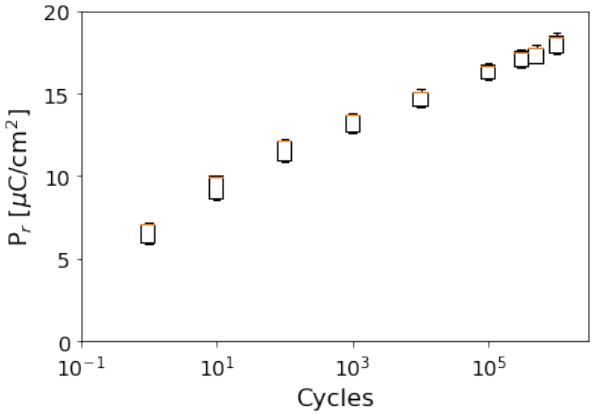


Figure 20: Five samples were each subjected to one million cycles, the results show good consistency between devices.

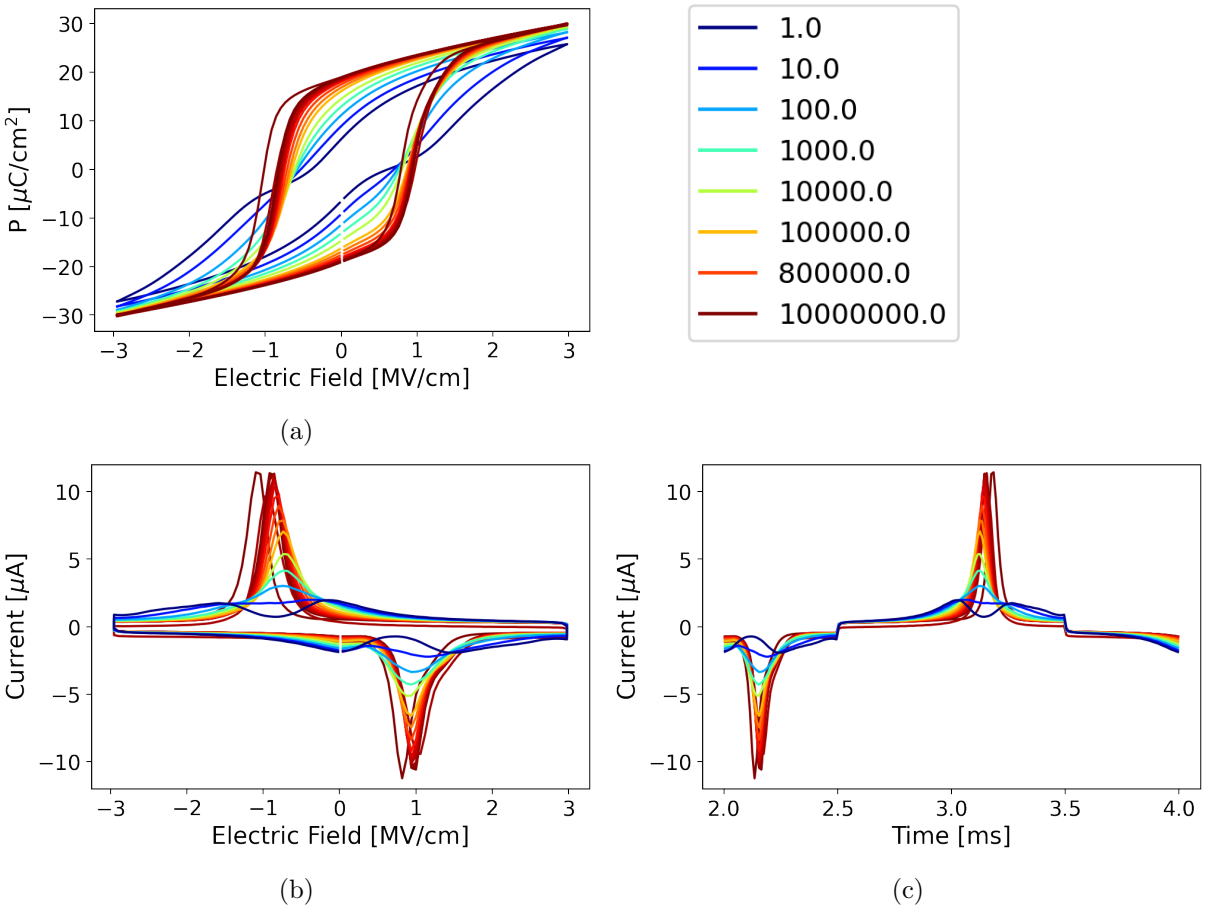


Figure 21: **(a)**A single device with 4 % La was subjected to endurance measurements for 10 M cycles, with the hysteresis curve for each measured cycle being plotted. The sample survived 10M cycles, without indication of fatigue, however, the device has a very long wake-up. **(b)**, and **(c)** show the I-V, and current output characteristics of the device, one can more clearly see the two peaks indicating antiferroelectric-like behavior in the blue curve corresponding to the first cycle, as well as the rapid tendency to pure ferroelectricity within 100 cycles.

5 Discussion

The large gradients shown in the ALD investigation of the hafnia and later lanthanum oxide deposition were likely due to insufficient vapor pressure produced in the source bottle, resulting in incomplete saturation of the chamber due to a lack of material. One would have thought that increasing the pulsing duration would help improve the saturation of the chamber, and make up for the low vapor pressure, but this does not appear to be the case in this system. By looking at the pressure data from the precursors in the ALD tool, it was noticed that no matter the pulse-duration, there is an identical large spike in pressure followed by nothing. What seems to be the case then, is that the tool collects and pressurizes precursor vapor and then quickly

injects this into the chamber. The pulsing duration then does not affect the amount of injected gas, but rather the duration the precursor is given to saturate the chamber before being purged.

Once the lanthanum oxide precursor source bottle was in place, it was quickly found that reaching high temperatures would be imperative for the deposition of the lanthanum oxide film. It was with this source temperature that the first HLO samples were created. Looking at Figure 13a, the samples were created two at a time, placed in the area showing highest deposition (bright red area of the figure). As this area is so small, it is reasonable to expect variations in the deposition temperature, and it is not well-known how stable this deposition map is. Since HLO samples would be created with a majority hafnia, measuring the deposited lanthanum oxide in isolation would be difficult. Nevertheless, the samples created with this configuration acted as a guideline for the final sample series, which was created with the lanthanum oxide deposition recipe seen in Figure 13b. This of course adds an additional source of uncertainty, as the two recipes are not necessarily comparable.

At the time, the ambitions were to create samples at five different concentrations that could be annealed at several different temperatures, as well as some samples to be annealed with the FLA at the 8 % concentration mark, that seemed to show the greatest promise for ferroelectricity. In hindsight, due to the uncertain nature of the deposition, it would have been better to create more samples at fewer lanthanum concentration points, e.g. 4, 8, and 12 % lanthanum, or even just at one concentration. The possible data yield would have been smaller, but a more compelling and thorough analysis of the FLA tool as an annealing method could have been conducted, which would have been the more interesting result. The results of the Flash-Lamp Annealer are also not necessarily indicative of the ability for the tool to result in ferroelectric films. The devices created with the FLA were not grown simultaneously with the devices which showed ferroelectricity in the RTA. Coupling this along with the fact that the measured ε_r for the FLA samples (21.3±0.16) does not match that of the corresponding RTA samples (16.46±0.33) indicates that there is some difference in the oxide. If this is a result of the RTA samples having been somewhat crystallized, or if it is purely because of differences in oxide growth is uncertain.

It is thus possible that variations in growth resulted in only some devices working, depending heavily on which batch of samples were investigated. This could have been investigated either by submitting the samples to further annealing in the FLA at higher preheating temperatures, or by annealing one of the samples in the RTA at 600°C to verify whether these samples could become ferroelectric with the alternative annealing method.

Another thing to note is the usage of "%" of lanthanum in this thesis. Since no formal way of measuring the atomic content of the films was employed, the values indicated here as percentages are likely not accurate when compared to atomic %, and should thus be taken with a grain of salt. To measure the proper atomic concentration of lanthanum, one could have taken SEM images using an XEDS detector to find the measured signal of lanthanum oxide and hafnia. One could also investigate the presence of different crystalline structures by implementing some surface-sensitive methods such as grazing-incidence X-ray diffraction which could have given a better idea of the crystal phases present in the films.

Furthermore, the devices created were 15 nm thick, this was based on the processing done to create $HfZrO_2$ devices. However, this thickness is near the upper limit of the oxide thickness. The thicker the oxide is, the weaker the strain exerted on the oxide by the surrounding layers.

It is possible that the samples exceeded the maximal thickness, and that devices created with a 10 nm thickness rather than 15 would have yielded better results.

For the devices that did work, the remanent polarization measured is similar in magnitude to those reported in [14]. The measured coercive fields from the P-E curve indicates that there is an asymmetry in the devices, as the coercive field is larger in one direction than the other. This is likely due to asymmetrical series resistances in the measurements. These are likely the result of the fact that the the side of the bottom electrode is connected in series with a shorted capacitor in which a conductive filament has been formed, as opposed to the direct connection to the gold contact that the top electrode has. It can also be noted that the coercive field appears to increase with increasing peak bias, something which is not expected to occur in ferroelectric devices. This could indicate a wide range of coercive fields in the crystal, as an increased peak bias in this case would mean that more domains align themselves permanently, which means that the coercive field at lower peak biases will no longer switch half of all domains in the crystal, resulting in a larger E_c.

As shown in Figure 21, an endurance of 10 million cycles was achieved, which is significant enough to warrant notice. However, the data also shows a very long wake-up which could be due to poor oxide quality as a result of the ALD process not having been optimized to the point of self-limiting ALD-type growth. It would have been desirable to extend the endurance measurements by another factor 10 to reach 100 million cycles, as that result would have been more impressive, but the large size of the devices limits the RC constant, which in turn limits how quickly the device can be cycled. Attempts were made to increase the cycling frequency past 10 kHz, but it was found that the time delay of the devices would have impacted these measurements too much to allow that.

Figure 17 show that even the other devices with a very low remanent polarization still have a distinguishable ferroelectric loop, however, as noted by [23], closed loops in the P-E diagram could just indicate a lossy dielectric. Although these curves do not appear as 'cigar'-shaped as those demonstrated in that paper, it is possible that this is an indication of weak ferroelectricity.

The disparity in simulated- and measured backside temperatures in the FLA tool is quite large. Since the backside temperature should be a result of thermal diffusion, this temperature should be consistent with the simulations for a given material and input conditions. The fact that the simulation does not agree with the actual output could indicate that some values for e.g. reflectivity in the model do not match the actual values. Another source of error lie in the fact that the pre-heating lamp was on during the measurement, this additional source of heating may have affected the temperature readout of the pyrometer. The simulated values are also relatively low if one considers the results which indicate that crystallization occurs around 600°C, in hindsight, it would have been better to shift these data points up by 50°C each to reach higher peak temperatures.

As was shown in Figure 19a, the samples annealed with the FLA indicate that there is no ferroelectricity. This does not necessarily indicate that FLA is an unsuitable method for the crystallization of ferroelectric films and further investigation into this method are in order to determine this. There are, however, some issues which were noted with it. Firstly, the use of silicon as a substrate for the devices yields a large thermal conductivity with 1.3 W/(cm°C), resulting in a lower temperature gradient, as compared to e.g. an InAs substrate which has a

lower thermal conductivity of 0.27W/(cm^{o}C). This forces the use of higher preheating temperatures which to some degree defeats the use of the FLA, as this tool is intended to remove the need for high-temperature annealing.

It should also be noted that the high temperature gradients that are produced within the samples may cause internal stress due to thermal expansion to cause the samples to break. This was experienced at one point in the thesis, where one sample was damaged slightly, and the carrier wafer used for the annealing process also shattered at one time. It may be desirable to increase the flash duration, or decrease the flash energy so as to reduce the gradient to prevent this, although this would necessitate the use of higher preheating temperatures, which as noted above, is not desirable.

One may also choose to use the FLA tool for other hafnia alloys with lower crystallization temperatures, such as $HfZrO_2$ (HZO), which becomes ferroelectric around 420^{o}C, as compared to above 500 C for the HLO which was used in this thesis. One might even consider investigating the combination of HZO with lanthanum, creating some $Hf_{1-x}Zr_{1-x}La_{2x}O_y$, which may inherit the low crystallization temperature of the HZO alloy, while retaining the wide doping window and strong remanent polarization provided by the inclusion of lanthanum.

6 Conclusion and Outlook

To conclude, the thesis showed that deposition of lanthanum oxide can be accomplished, although not in a self-limited manner, using the local ALD system. Using the deposited lanthanum oxide films, MFM devices containing ferroelectric HLO-films were created and characterized. The devices show remanent polarizations of up to 20 μC/cm^2, which matches that of other publications [14]. The devices display good endurance properties with 10^7 cycles demonstrated without indication of fatigue. The endurance is accompanied by long wake-up times, likely as a result of the incomplete oxide deposition process. However, the fact that the deposition of the oxide is far from perfect is a compelling reason for this project to resume at a later time. Once a reliable, self-limited process has been developed for deposition of lanthanum oxide, it is the opinion of the author that a more thorough analysis of the HLO system can yield interesting results and produce devices of good quality. Such a study should include proper techniques to determine the real lanthanum content of the HLO films and relate this to the investigated properties. An interesting result would be to see how the temperature threshold for orthorhombic crystallization varies with increasing lanthanum content. Further studies would also benefit from a new device architecture which results in smaller capacitors that would reduce the RC-constant of the devices, allowing for higher frequency endurance measurements to more quickly find the endurance of devices. More time could also be dedicated to implementing FLA as an annealing method. Focus on finding processing methods for substrates with a lower thermal conductivity than silicon would be beneficial to allow higher temperature gradients to be reached during the flash, one might also consider the use of ferroelectric films which crystallize at a low temperature to further reduce the need for preheating prior to annealing.

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A Code for Analysis

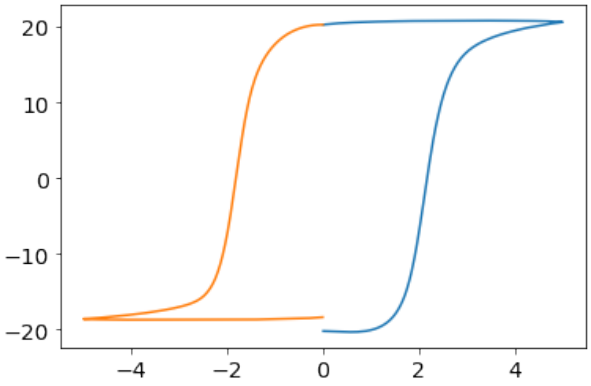
Here, the necessary code for the production of hysteresis curves will be shown. It is assumed that the operator has access to PUND data of the time of each measurement, output current, and set voltage. These are stored in arrays, called time, curr, and pot respectively.

First, import the necessary packagesm numpy comes with arrays and certain mathematical tools like the np.median function. Matplotlib allows the plotting of data. Additionally the packages "glob", "re" and "pandas" were used to search directories for files, extracting information regarding process parameters from file names, and creating dataframes containing the relevant data directly from the data files. This all goes in to the creation of the original arrays, as well as the identification of which data is visualized.

```
1   import numpy as np
2   import matplotlib.pyplot as plt
```

The below contains a numerical integral (summation) of the current to find the charge passing through the capacitor at any time, and normalizes this by the area to make it a measurement of the polarization. The remanent polarization is calculated by subtracting the polarization resulting from the 3rd and 5th pulses from the 2nd and 4th respectively. This removes any dielectric component and only leaves ferroelectric polarization. The last values in the respective halves of the polarization data are then subtracted from each other to get $2P_r$, and then divided by 2 to return P_r.

```
3   """Remanent polarization and Polarization list"""
4   Q = []; q = 0
5   for j in range(len(time)): #"integarting" the current.
6     q += curr[j]-curr[0]
7     Q.append(q)
8   Q = np.array(Q)*1e6*(time[1]-time[0]) #uC
9   r = 25e-04 #cm
10  A = np.pi*r**2 #cm2
11  Pol = np.array(Q).astype(float)/A #uC/cm2
12
13  """The following is needed to calculate the remanent polarization"""
14  pulse_length = 800 #number of data points in the triangle wave
15  P0 = 1100; U0 = 2100; N0 = 3100; D0 = 4100
16  Pol1 = Pol[P0:P0+pulse_length]-Pol[U0:U0+pulse_length]+Pol[U0]
17  Pol2 = Pol[N0:N0+pulse_length]-Pol[D0:D0+pulse_length]
18  Pol2 = Pol2 - (Pol2[0] - Pol1[-1])
19  pr = (Pol1[-1]-Pol2[-1])/2
20
21  plt.plot(pot[P0:P0+pulse_length], Pol1-pr)
22  plt.plot(pot[N0:N0+pulse_length], Pol2-pr)
23  plt.show()
```



The plot commands towards the end are what result in the hysteresis plots as created by the code above. Below is the hysteresis plot for 5V peak biasing, 4 % lanthanum annealed at 600°C, shown in Figure 16a. Pol1 is the blue line, and Pol2 the orange one.

The coercive field is found by finding the index of the minimal value of "Pol1-pr" and "Pol2-pr", and finding the bias point of the same index. Below, Ec1 will be the positive coercive field, and Ec2 will be the negative coercive field.

```
Ec1 = pot[P0:P0+pulse_length][np.where(abs(Pol1) == min(abs(Pol1)))];
Ec2 = pot[N0:N0+pulse_length][np.where(abs(Pol2) == min(abs(Pol2)))]
```

Lastly, the determination of the dielectric constants in the capacitive films was done by specifically analyzing the "U" and "D" peaks, which inherently should not have ferroelectricity. The samples examined were also those annealed at 500C which showed no "real" ferroelectricity either. This was done to analyze the most capacitive currents. To avoid contributions from leakage, the last 0.1 ms of the data from each peak are discarded. To further avoid contributions due to leakage and noisy currents, the capacitive current is then defined as the median value of the current in the array. The relative permittivity is then calculated.

```
def capacitance(time, curr, pot):
  dv = pot[1]-pot[0]
  dt = time[1]-time[0]
  C = curr/(dv/dt)
  return(np.median(C))
C1 = capacitance(time[U0:U0+300], curr[U0:U0+300], pot[U0:U0+300])
C2 = capacitance(time[D0:D0+300], curr[D0:D0+300], pot[D0:D0+300])
e0 = 8.854e-12
er1 = C1*15e-9/(e0*(np.pi*(25e-6)**2))
er2 = C2*15e-9/(e0*(np.pi*(25e-6)**2))
```