PLL for mmWave 5G

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PLL for mmWave 5G

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Abstract

This paper presents research and implementation of a high frequency Integer-N phase-locked loop for digital beamforming in mobile devices. Multiple topologies investigated whereof two were implemented. The transient phase noise of the PLL is -104dB/-95dB @1MHz. The output frequency range is from 8G-10G. Reference signal is 163.84MHz, reference-spurs is -80dBc/-98dBc lower than main frequency. RMS jitter is about 38fs/68fs. Locking time is less than 3.5μs. The implementation consists of an LC-tank VCO with extra tail filtering. Divider chain consisting of a dual module prescaler/CML prescaler followed by a programmable divider. Charge pump with compensation method and a cascoded gain-boosting charge pump is used to decrease current mismatch. Tri-state phase detector and lastly a third-order passive loop filter. Supply voltage at 0.8V is used in the design. Total power consumption is less than 10mW. The PLL system was implemented in the CMOS FD-SOI 22nm process and simulations executed in the Virtuoso Cadence environment. Limitations and possible improvements are listed in the end.

Popular Science Summary

The upcoming 5G-New Radio Standard will enable cellular communication in the millimeter-Wave (mmWave) frequency bands,24-100GHz. These frequency bands will open up for large system bandwidth and tremendously high data rates enabling lots of new use cases, such as smart cities, connected cars, medical applications and much more! Given this cutting-edge technology, exciting challenges arises for today's RF designers that requires state-of-the-art solutions.

High isotropic path loss between radio transmitters and radio receivers makes it necessary to rely on antenna arrays with large number of antenna elements. MIMO stands for Multiple-Input-Multiple-Output. In reality this means using multiple antennas on the same frequency band, with massive indicating a high number of such antennas. Making these antennas directional through *beamforming*, focusing the transmission in the direction of the receiving party, may overcome the issues with isotropic path loss.
Traditionally mmWave has been used more for short-range communication due to its inherent characteristics and propagation loss, but in combination with MIMO and beamforming it will take the next generations of cellular communication to new levels!

Small antennas needed for mmWave open possibilities to integrate the RFIC, front end radio modules, filters, and antenna element in a singe RF chip. This fact, in combination with that 5G-NR is standardized for communication also over mmWave radio frequencies which enables mmWave communication in smartphone and IoT devices, will drastically change the way beamforming will be implemented in mobile devices in the future!

A critical component used in wireless communications that will be included in this type of integrated chip is the, so called, phase-locked loop (PLL). The PLL is a feedback system which can generate a periodic precise signal at a certain frequency and phase. This ability is quite useful and can be applied in various applications for frequency synthesis. Facing new challenges with mmWave applied with beamforming, the design of a phase-locked loop has become more challenging and requires state-of-the-art thinking to satisfy the needs of the industry.

In this Master's Thesis, we present the design process of a charge pump based phase-locked loop with 22nm technology. Each building block has been thoroughly examined to acquire enough knowledge to carry out our own designs. Multiple architectures were tested for each block until a satisfactory one was finally implemented. The entire system was then implemented using these blocks. Two finalized systems consisting of different architectures were designed and simulated, whereof both can be used in a 5G-NR mmWave application.

Acknowledgements

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I, Daniel, would like to express my gratitude towards all the people that have been by my side during my education. All of my co-students and friends who have supported me during my studies and that have provided me with laughter and joy. I would like to thank Jin for doing this project with me, he has been both resourceful and helpful, and it was nice to have someone to discuss with and to learn from. Especially, I would like to thank my parents for always being there for me and providing me with the love and energy to carry on.

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Chapter 1

Introduction

The upcoming 5G-New Radio Standard will enable cellular communication in the mmWave frequency bands, 24-100 GHz. The mmWave frequency bands open up for large system bandwidth and Gb/s data rates enabling a lot of new use cases, such as smart city, health, connected cars, advanced Augmented Reality (AR) and Virtual Reality (VR) applications etc. This technology standardization is forthcoming and is expected to be deployed for commercial applications within a couple of years. As new technological issues are introduced, alternate transceiver/receiver architectures that enable low-cost and low-power CMOS solutions for the wireless communications market has become a hot topic. Hence researchers and designers focus on all levels of optimization to meet the requirements of the market. One issue topic is the high isotropic path loss between the radio transmitter and radio receiver for mmWave that makes it necessary to rely on antenna arrays with large number of antenna element. These antenna arrays overcome the path loss by high directional gain through beamforming. Thus, a transmitter-receiver pair uses many antennas to focus energy in a particular direction in order to mitigate the high path loss in the mmWave frequency band[1].

The principles behind mmWave Beamforming applied to a 5G-NR can be explained as follows. A base station – mobile device communicates via directing the radio signal towards each other using many antenna elements at both transceiver sides. A typical number of antenna elements for mmWave communication in 5G could be 64-256 antenna elements in a radio base station and 4-16 antenna elements in a mobile device. For smartphones and IoT devices targeting the mass market, the radio architecture really needs to be optimized from cost and size perspective. An illustration of the principle is shown in Figure 1.1.

The start-up company BeammWave, develop disruptive digital beamforming architectures, by integrating the RF IC, front end Radio modules, filters, and antenna elements in a single RF chip that will drastically change the way beamforming will be implemented in mobile devices in the future, which will be based on digital beamforming.

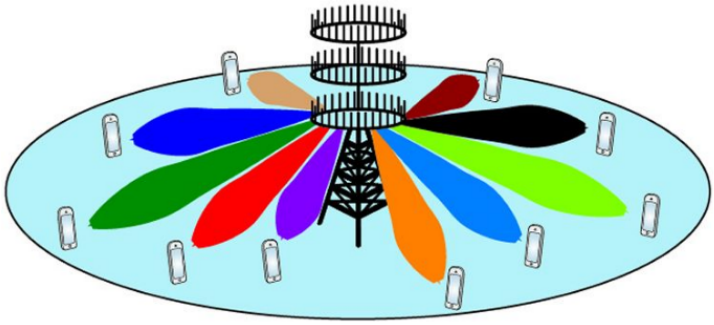


Figure 1.1: Illustration of Beamforming between radio station and mobile devices

First generation 5G mmWave smartphones using Analog Beamforming architecture, with 8 4x2 antenna panels of 25x18 mm^2 (left), Figure 1.2. BeammWave's disruptive Digital beamforming architecture where antenna element, front end modules, filters and RF IC are integrated in a single RF chip of 3x3 mm^2. 16 antennas (right). Total PCB size for digital beamforming architecture is 144 mm^2 compared to 3600 mm^2 for the analog beamforming architecture[2].

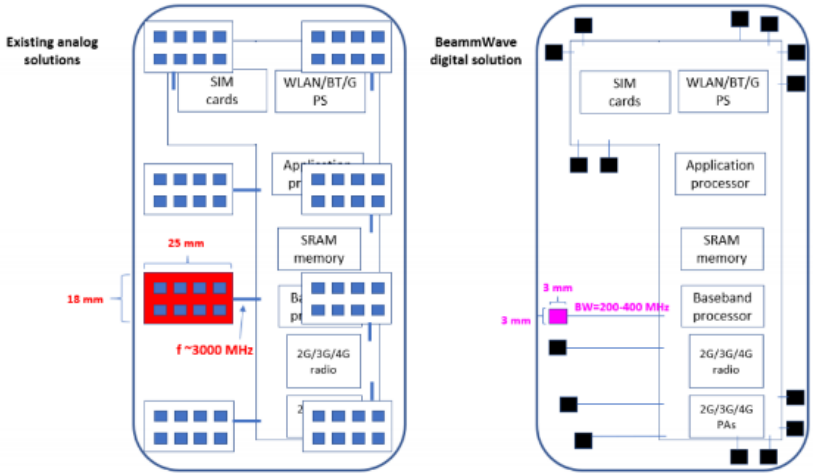


Figure 1.2: Beamforming in mobile devices

1.1 Phase locked loop

The phase locked loop (PLL) is a critical component widely used in RF frequency and wireless communication systems for frequency synthesis. The PLL synchro-

nizes an internal oscillator signal to an input reference signal in such a manner that they operate at the same phase. This ability is useful because it allows the designer to create a filtered version of the reference with control over how the output tracks the reference. Some phase locked loop applications include:

One major phase locked loop application is that of a FM demodulator. Since PLLs are relatively cheap to manufacture they have replaced the costly RF transformers formally used in FM modulators. Without having to change the basic structure of the PLL loop, it is utilized for this application by enabling high quality audio to be demodulated from an FM signal. Apart from being cheap, the PLL is also easy to implement and allows the modulator to provide good noise immunity[3].

PLLs can be used in the synchronous demodulation of amplitude modulated signals. Using this approach, the PLL locks onto the carrier so that a reference within the receiver can be generated. As this corresponds exactly to the frequency of the carrier, it can be mixed with the incoming signal to synchronously demodulate the AM[4].

The fact that the phase locked loop is able to lock to a signal enables it to provide a clean signal with suppressed noise, modulation and interference. It also allows "remembering" the signal frequency if there is a short interruption. This phase locked loop application is used in a number of areas where signals may be interrupted for short periods of time, for example when using pulsed transmissions or in CW carrier recovery[4].

The indirect form of RF frequency synthesizer based around the phase locked loop or PLL is the most commonly used form of RF synthesizer. Without breaking the basic functionality of the PLL, some additional circuitry is added to provide the frequency synthesizer action. This additional circuitry adds a frequency offset into the loop in one way or another. The synthesizer is either constructed as a digital or analog synthesizer, by introducing a digital divider or analog mixer respectively[5].

Another phase locked loop application is in the distribution precisely timed clock pulses in digital logic circuits and system, for example within a microprocessor system.

As the variety of applications increases so does the various architectures of the loop itself. Naturally, different architectures are suited for different applications. Some commonly used terms are analog phase-locked loop (APLL) also referred to as a linear phase-locked loop (LPLL), digital phase-locked loop (DPLL), all digital phase-locked loop (ADPLL), software phase-locked loop (SPLL), and charge pump phase-locked loop (CP-PLL)[6].

- ***Analog/linear PLL***
  Characterized by its phase detector, which is an analog multiplier. It consists of a voltage-controlled oscillator (VCO) and an active or passive loop filter.

- ***Digital PLL***

Uses a digital phase detector such as, XOR, JK flip-flop or phase frequency detector. Other components are the same as the analog. It may use a digital frequency divider as well.

- ***All digital PLL***
  As the name implies, it consists only of digital components. Uses a numerically-controlled oscillator (NCO).

- ***Software PLL***
  Functional blocks are implemented by software instead of hardware.

- ***Charge pump PLL***
  CP-PLL is a modification of the phase-locked loops which consists of a phase-frequency detector and square waveform signals.

1.2 Goal of project

The goal of this project is to focus in the design and design issues of an Integer-N PLL circuit for 5G mmWave transceivers. It is supposed to obtain satisfactory performance, based on given specifications given by BeammWave. The design is to be implemented using the 22nm FDSOI technology, to be implemented in an already initiated system. This system will contain a multiply-by-3 component after the VCO, hence the operating frequency of the application will be three times higher than the operating frequency of the VCO. Performance requirements for the loop include coverage of the output frequency from 8GHz to 10GHz. For the closed loop, the phase noise at 1MHz should be lower than -100dBc to meet the BER requirement. Other parameters such as power consumption and area should be optimized to be as low as possible within the limited time frame of the project. Simulation is included to verify the performance of the circuit. A report is expected to present the process of the whole project.

Chapter 2

PLL fundamentals

PLL is a control system used for clock generation. It synchronizes a signal from a voltage-controlled oscillator (VCO), that is a multiple of a high precision reference, so that the VCO and reference are phase aligned. This is achieved by constantly comparing the phase difference between the signals so that a constant phase difference is maintained during the locked state. In communication systems PLL are widely used for carrier synchronization, carrier recover, frequency division, multiplication and demodulation. There are several variations of the PLL system, all of them, obtaining the same goal of phase locking. A block diagram of a typical PLL system is shown in Figure 2.1.

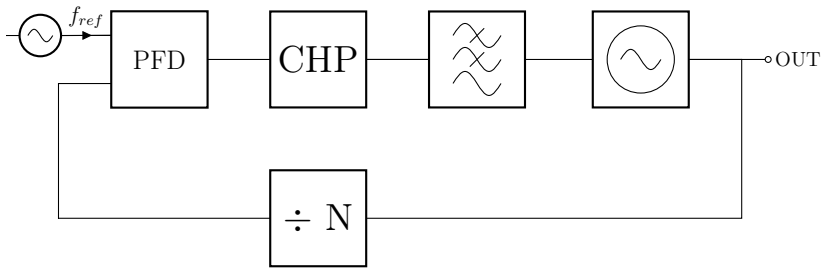


Figure 2.1: Integer-N PLL block diagram

In this project, we focus on the integer-N CP-PLL. Which consists of a phase-frequency detector, charge pump, loop filter, divider and voltage controlled oscillator. The general idea is that the phase detector detects the phase difference between its two input signals and multiplies that difference with a gain factor K_{vco}. The voltage generated by the multiplied phase difference is then fed through a loop filter, which governs many properties of the loop and removes any unwanted high frequency elements. The output voltage of the loop filter is then fed back to the control terminal of the VCO which acts as a tuning voltage. The oscillator is then either tuned up or down in frequency depending on the control voltage. The sense of any change in voltage is to reduce the phase error and hence the frequency between the two signals. This process is done repeatedly until the phase error cannot

be reduced any further. Thereby, the loop has reached its locked state. The oscillator provides an output signal at a frequency that is a multiple of the reference, depending on the division ratio in its feedback path (Equation 2.1). Hence, the PLL produces a range of frequencies that can be used for various purposes.

$$f_{vco} = N \cdot f_{ref} \tag{2.1}$$

The main parameters considered in PLL design include phase noise, RMS jitter, power consumption, reference spurs and tuning range. The following sections will explore the PLL system as a whole and each building block individually, and explain the meaning of the parameters. This chapter should serve as a basis for understanding the work done and the conducted results presented in the remaining chapters.

2.1 Phase-locked loop basics

From a purely mathematical standpoint, the system can be described as shown in Figure 2.2.

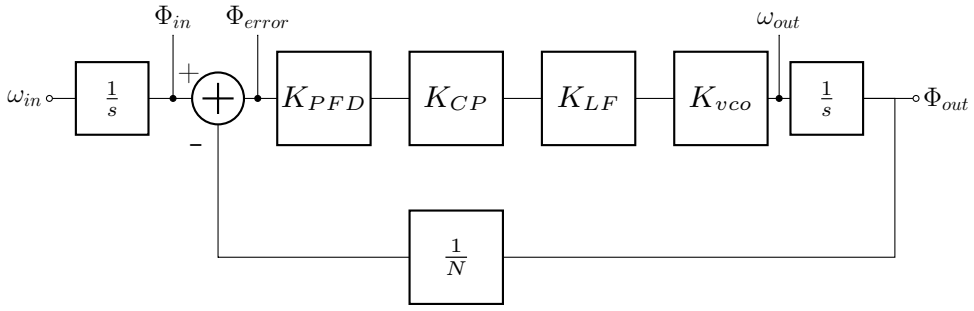


Figure 2.2: PLL matchematical model

The input to the block diagram is the reference signal which has certain frequency, ω_{in}, and phase, Φ_{in}. The phase error Φ_{error} is the phase difference between the voltage-controlled oscillator output's phase and the reference signal's phase. Since phase is the integral of frequency, the conversion of frequency to phase is shown in the s-notation. The phase detector converts the phase error to a voltage with some gain, K_{PFD}, the charge pump with some gain, K_{CP} and the loop filter also contributes with some, considered as, gain K_{LF}. Then the VCO converts the phase error voltage to a frequency with some gain K_{vco}[4].

The output phase is related to the input phase according to Equation 2.2 below,

$$\Phi_{out}(\omega) = H(\omega) \cdot \Phi in(\omega). \tag{2.2}$$

Here we see that the output phase is a function of input phase, which will include phase noise. Integrating the output phase over the range of interest, that is, the

loop bandwidth, the phase power of the output can be found in response to the input phase modulation, or modulations due to the VCO itself. Another thing worth mentioning is that the PLL output functions as a low-pass filter for phase noise arising before the VCO, while it functions as a high-pass filter for phase noise generated in the VCO. Therefore, to reduce output noise due to the VCO the loop bandwidth must be as large as possible. However, the loop bandwidth must be less than the input reference frequency in order to keep the loop stable and to suppress spurs at the output due to the reference signal. To achieve minimum phase noise within the loop bandwidth, in-band noise contributed by the other loop components should be as low as possible[7].

2.2 Jitter and Phase Noise

The concepts of jitter and phase noise are used to describe irregularities in a signal, often in comparison to another clock reference signal. Jitter describes time-domain deviations in a periodic signal, whereas phase noise is the frequency-domain representation of random fluctuations in phase of a waveform. Both concepts are widely used in all types of electronic design, especially in RFIC. To get a better understanding of the concepts themselves and their effect in the PLL system they are described in the following.

2.2.1 Jitter

Jitter is a broad concept term exising in many engineering fields. Generally, it stands for the deviation from an ideal periodic signal in the design of clock recovery applications. It can be optimized by careful design or advanced process, however, due to inevitable thermal noise and mismatch in the fabrication, it is impossible to have zero jitter in reality. In most cases, jitter would degrade the performance of applications by influencing the amplitude and phase. Thus, low jitter is one principle of designing the PLL.[8].

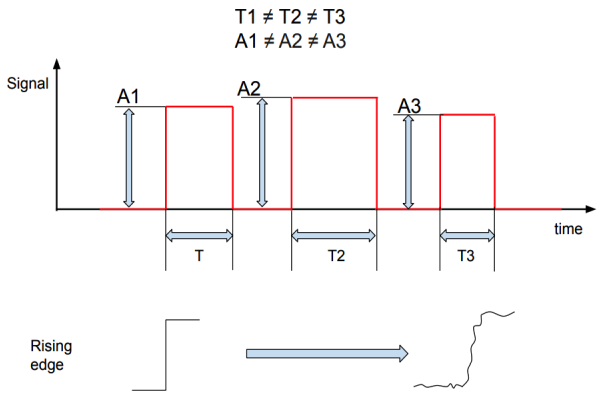


Figure 2.3: Clock jitter

Period jitter

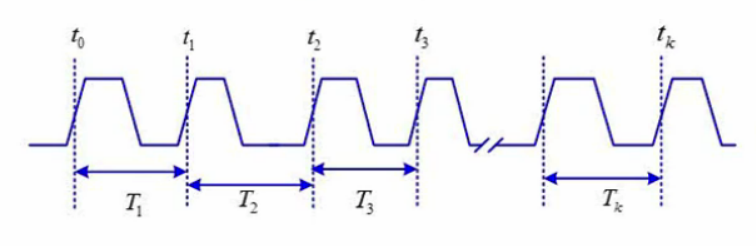


Figure 2.4: Period jitter

For calculating the period jitter, we need a standard period as reference as well as a threshold voltage to decide from what value a new cycle is counted. The RMS Period Jitter is one of the most used parameters, that is defined as standard deviation of each period.

$$Period\,Jitter_{rms} = \sqrt{\frac{\sum_{i=1}^{n}(x-\bar{x})}{n-1}} \tag{2.3}$$

Here, x represents the period of each cycle between two threshold voltages, $\bar{x}$ represents the mean value of all periods in the measurement. Generally, a normal distribution of jitter histogram will be obtained as shown in Figure 2.5.

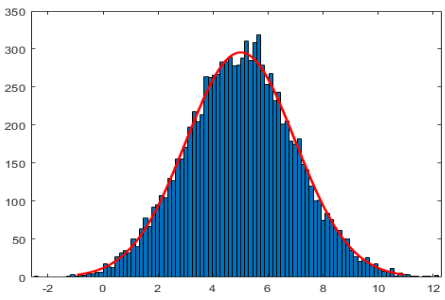


Figure 2.5: Normal distribution of sampled jitter

Notice that this period jitter is considered as a type of random jitter, this means that there is no boundary for this distribution. The more sampling we do, the higher the possibility to see an extremely high jitter is[9]. In this model, everything is based on statistics. At the mountain foot the amplitude is low, but it does not mean zero. A suitable sampling time should be considered in order to get a good budget with calculation complexity.

Cycle to cycle jitter

The cycle to cycle jitter is the maximum variation in period between two consecutive cycles during a certain measurement time. There is no reference to an average clock for comparison, as is the case for Period Jitter.

$$C2C\,Jitter = Max\{|T_n - T_{n-1}|\} \tag{2.4}$$

Cycle to cycle jitter is also a random jitter whose histogram looks like a normal distribution as well.

Peak to Peak jitter

Peak-to-peak(P2P) jitter is the difference of distance from the logic low to the logic high on the edges. Peak-to-peak value is more relevant in calculating setup and hold time budgets. This value will increase if more samples are taken into the calculation.

P2P jitter is usually given information on the product. But in reality, if we only have Period RMS jitter of a VCO. How could we know the Peak to peak jitter?

This is usually done by multiplying RMS jitter by a number, α, based on BER requirement. According the table below (Table 2.1), we can transfer the period RMS jitter into peak to peak jitter or the other way.

$$Peak\,to\,Peak\,Jitter = RMS\,Period\,Jitter * \alpha \tag{2.5}$$

BER	10^{-3}	10^{-4}	10^{-5}	10^{-6}	10^{-7}	10^{-8}	10^{-9}	10^{-10}	10^{-11}	10^{-12}	10^{-13}	10^{-14}	10^{-15}	10^{-16}
α	6.180	7.438	8.530	9.507	10.399	11.224	11.996	12.723	13.412	14.069	14.698	15.301	15.883	16.444

Table 2.1: Peak Jitter to RMS Jitter conversion

2.2.2 Phase Noise

Phase noise is actually a type of jitter that originates from oscillators. It has become such a common expression in that field that it has gotten its own definition and is handled separately. To understand the phase noise, we have to step into the frequency domain. An ideal single frequency in the frequency domain can be presented as a peak with zero width. However, due to noise, the real spectrum has a horizontal distribution. If the short term stability of an oscillator is examined using a spectrum analyzer, it shows a spectrum like in Figure 2.6. That means the signal actually contains more than one frequency, which are distributed by thermal noise, shot noise, flicker noise and jitter. This broadening is due to the phenomenon of phase noise.

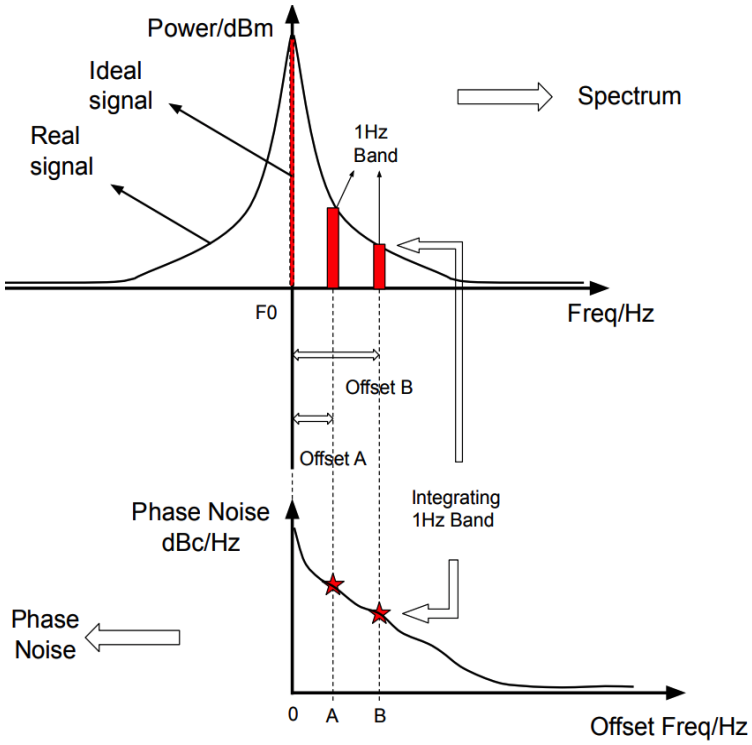


Figure 2.6: Spectrum to phase noise

2.3 Phase noise to RMS phase jitter

RMS phase jitter is another transformation of phase noise, which is partial integrated phase noise. It is usually characterized in terms of the VCO single-sideband phase noise as shown in Figure 2.7, where the x-axis is the offset frequency on a logarithmic scale of Hz and the y-axis is the magnitude of the phase noise in dBc/Hz.

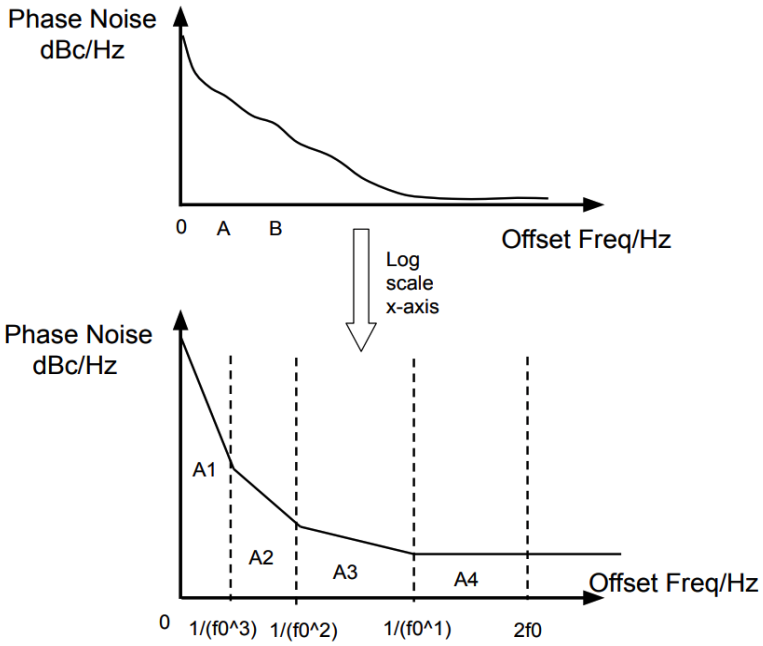


Figure 2.7: Phase noise to phase jitter

This curve is actually approximated by a number of regions, each with the slope of $1/f^x$. Each region corresponds to a different kind of noise, where x=0 corresponds to the 'white' phase noise region (slope = 0dB/decade), and the x=1 region corresponds to the 'flicker' phase noise (slope = –20 dB/decade). When x increases, the region it represents, occur closer to the carrier frequency[10].

$$A = 10log(A_1 + A_2 + A_3 + A_4) \tag{2.6}$$

$$RMS\,Phase\,Jitter(radians) = \sqrt{2 * 10^{A/10}} \tag{2.7}$$

$$RMS\,Phase\,Jitter(seconds) = \frac{\sqrt{2 * 10^{A/10}}}{2\pi f_0} \tag{2.8}$$

A=Area of interest f_0=oscillation frequency

The integration range differs from applications to applications. 12kHz to 20MHz is a common choice. To calculate whole frequency jitter, the integration usually starts from a low frequency(100Hz or a few KHz)and stops at $2f_0$.

2.4 The phase-locked loop system

Apart from jitter and phase noise, the PLL system has some other overall performance parameters. These parameters are defined and described below.

Tuning range is the range of frequencies the PLL can output while meeting system requirements. It is dependent on the RF input and/or output frequency of the application it is used in.

Lock-in range is the range of frequencies which the loop can lock, within a single period of the beat frequency. If the frequency difference between reference and VCO is less than the loop bandwidth, the loop will lock almost instantaneously. The maximum range within this fast acquisition, which can occur, is called lock-in range. *Lock-in time* is the time it takes for the loop to lock to its reference frequency[11].

The *minimum stepsize*, f_{min}, also known as, *frequency resolution* is the minimum change in frequency the PLL can generate. Its value may be big or small, depending on the application. Generally, this specifications sets minimum channel spacing in wireless communications systems.

Settling time denotes the time it takes for a system to change from a frequency, within a frequency window delimited by $\pm f_{err}$ from the desired frequency f_{lock}, after a "change of frequency" action has been activated.

Hold-in range is the range reference frequency which the PLL can maintain its lock statically, outside this range the PLL will drift out of lock. What this means is that if the PLL is in its locked state and the reference frequency is changed, the loop is able to maintain lock within a certain range of change.

Pull-in range, also known as *capture-* and *acquisition-range* denotes the maximum value, $\Delta\omega$ difference between VCO and reference frequency, for which the loop locks.

Spectral purity is desired in all systems to minimize noise energy at the output. *Spurious signals* are undesired spectral components that appears on the output of the system, which can give rise to a noisy frequency synthesizer. In a PLL, these spurs can be noticed in the output spectrum, at the frequency of $f_{vco} \pm (N * f_{ref})$. In order to keep a pure spectrum it is important to keep unwanted noise away from the input of the VCO and to make sure there is no modulation in the PLL system. The effect of a spurious signal, f_m, of a voltage-controlled output signal is mathematically shown in Equation 2.9[12].

$$S_{vco} = A_{LO} \cdot cos(2\pi f_{LO} t + \theta(t)) \tag{2.9}$$

Loop bandwidth is an important parameter that relates the speed of which the loop can achieve lock and at what phase noise level. A large bandwidth allows the PLL to lock fast, however, with degraded phase noise level. If a narrow bandwidth is chosen the phase noise will be good but the locking time will be longer. Ideally a zero lock-time is desirable, although not practically possible.

Hence, an application-dependent trade off must be made between lock-time and phase noise. The bandwidth of the PLL system can mathematically be expressed as in Equation (2.10)[13].

$$\omega_{BW} = \frac{I_{CP}K_{vco}}{2\pi N} \cdot K_{LF}. \tag{2.10}$$

2.4.1 Power consumption

The VCO is the main power consumer of the PLL system. Some designers have published extremely low power consumption VCOs in different topologies (a few hundred μ W), without deteriorating performance. One thing should be noted is that there is a direct trade off between power consumption and jitter in the oscillator. Even though the power consumption of PLL is considerably low compared to modern microprocessors, a lower power consumption is always desirable as long as the phase noise still meets the requirement.

Besides the VCO, some high power consumption structures such as CML-prescaler, or low-efficiency charge pumps should also be taken into consideration if the power consumption limitation is critical. In our project, we have two strategies to scale down the frequency from VCO output. One of them uses the CML-Divider and it turns out it consumes more power(about 2mW) than the other pre-scaler. When the whole circuit is supposed to take less power, a high power consumption CML divider should definitely be avoided[14].

2.5 Voltage-controlled oscillator

The VCO generates an output signal at a frequency which is a function on the input tuning voltage V_{tune}, fundamental frequency f_c and VCO gain K_{vco} as shown in (Equation 2.11).

$$f_{out} = f_c + V_{tune} * K_{vco} \tag{2.11}$$

The VCO is a key component in PLL design and/or frequency synthesizers. There are countless number of different oscillators described in the literature which express different tuning ranges, maximum output frequencies, phase noises, power consumption and areas, to name a few. Of the existing topologies, there are generally two categories: LC oscillators and ring oscillators. The basic structure of a ring oscillator consists of an odd number, n, of cascaded inverters which rely on the propagation delay, T_{pd}, of each inverter to realize the oscillation frequency,(Equation 2.12). An advantage of this type of structure is that many phases of the oscillation signal are available simultaneously, a property that can be used for instance vector combination beam steering[19]. LC oscillators rely on amplifying the output of an LC-tank at resonance frequency to provide the oscillation.

At operating frequencies around 10GHz, LC-oscillators dominate in performance compared to ring oscillators[15]. This project only explores the LC-oscillator.

$$f_{osc} = \frac{1}{2n \cdot T_{pd}} \tag{2.12}$$

2.5.1 LC-oscillator

As briefly mentioned, the LC-oscillator uses the resonance frequency of an LC-tank circuit to provide the positive feedback required for sustaining oscillations. There are many different structures such as the tuned collector/base, Hartley, Colpitts, Clapp, cross-coupled, etc. For integrated radio applications, the cross-coupled LC oscillator is the most attractive one. A common LC-tank VCO consists of an LC tank, varactor, capacitor bank, cross-coupled transistor pair, and a current tail (Figure 2.8). In the following, each component of the LC-tank VCO will be described thoroughly to get a better understanding on how the oscillator functions. According to the Barkhausen criterion, for sustained oscillations, a circuit will sustain stable oscillations only for frequencies at which the loop gain of the system is equal to or greater than 1 and the phase shift between input and output is 0 or an integral multiple of 2π.

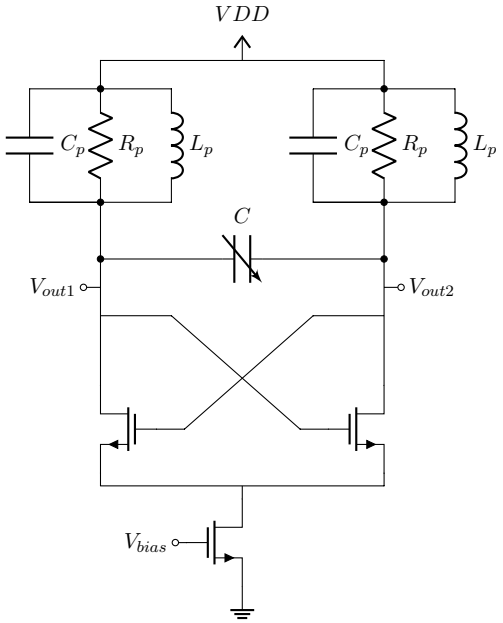


Figure 2.8: Typical LC type oscillator

LC-tank

A tank circuit consists of a capacitor connected to a coil and inductor. It is the source of oscillation signals. The resonance in a tank circuit is created by

the movement between the capacitor and the inductor, as electrical charge moves from the capacitor to the coil, the capacitor loses electromagnetic energy and the inductor becomes electromagnetically charged. Once the inductor is more charged than the capacitor, the electromagnetic field around the coil begins to dissipate and energy flows back through the wires to the capacitor. The process then restarts and repeats until all of the original energy is lost to resistance in the circuit. The frequency of resonance can be calculated with

$$\omega = \frac{1}{\sqrt{LC}}[rad] \tag{2.13}$$

The fact that the energy storage components involved are lossy, a negative resistance or a positive feedback is needed to cancel the loss, seen as R_p (Figure 2.8), to keep the oscillation from decaying. R_p can be found as an equivalent series resistance of the inductor and capacitor in the tank (Figure2.14). In addition, L_p and C_p can be found given their quality factors, as shown in (Equation 2.15) and (Equation 2.16). Lastly, the tank loaded Q-factor is given in (Equation 2.17), where ω_0 is the fundamental oscillation frequency.

$$R_p = \frac{R_{cs}(1+Q_{cs}^2)R_{ls}(1+Q_{ls}^2)}{R_{cs}(1+Q_{cs}^2)+R_{ls}(1+Q_{ls}^2)} \tag{2.14}$$

$$L_p = L_s\frac{1+Q_{ls}^2}{Q_{ls}^2} \tag{2.15}$$

$$C_p = C_s\frac{Q_{cs}^2}{1+Q_{cs}^2} \tag{2.16}$$

$$Q_{loaded} = \frac{R_p}{\omega_0 L} \tag{2.17}$$

Cross-coupled Pair

The cross-coupled pair is used to provide a negative resistance. And an oscillator that works on negative resistance property can be termed as a negative resistance oscillator. The term negative resistance refers to a condition where an increase in voltage across two points causes a decrease in current. In the LC tank, the parasitic resistance of the inductor and capacitor can be modeled as an equivalent parallel resistor if the Q of LC is large($>$10).

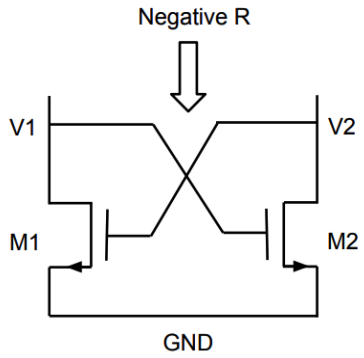


Figure 2.9: Cross-coupled pair

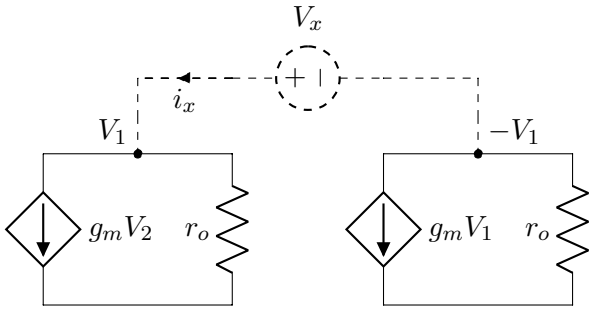


Figure 2.10: Cross-coupled pair small signal model

The idea is to cancel the positive equivalent resistance with a differential transistor pair.

The transistor pair can be taken as two identical dependent current sources. Let's take the r_o in to consideration, r_o is the output resistance of the transistor. It represents the fact that the transistor is not an ideal voltage-controlled current source. The collector/drain voltage does have some influence on the current, and that is what r_o models. Also, because the transistors are connected as cross-coupled, the gate voltage of left one is actually the drain voltage of the right one. Thus the left transistor can be modelled as a voltage controlled source $-g_{m1}V_2$ in parallel with r_o. A voltage source is connected as shown in Figure 2.10, the current comes from source is i_x, which goes into the left branch. As the transistors are identical, thus the current amplitude in left and right branches are equal. Therefore,

$$V_1 = -V_2, V_x = V_1 - V_2 = 2V_1 \tag{2.18}$$

Look at the left branch,

$$i_1 = i_x = g_{m1}V_2 + \frac{V_1}{r_0} = -g_{m1}V_1 + \frac{V_1}{r_0} \tag{2.19}$$

Take the V_1 to left, therefore we get

$$\frac{i_x}{V_x} \approx \frac{-g_{m1}V_1 + \frac{V_1}{r_0}}{2V_1} = -\frac{g_m}{2} + \frac{1}{2r_0} = -\frac{g_m}{2}(1 - \frac{1}{g_m r_0}) \tag{2.20}$$

The term of $g_m r_0$ is called intrinsic gain, which is decided during the manufacturing and is much larger than 1, thus

$$\frac{i_x}{V_x} \approx -\frac{g_m}{2} \tag{2.21}$$

which is negative. If this value is designed to cancel the positive parasitic resistance in the tank, then the oscillator is able to work.

Now, since we have cross-coupled pair added into the circuit, we need to re-estimate the oscillation frequency. The extra parasitic capacitance from cross-coupled pair will effects the total capacitance.

A more accurate frequency can be calculated by

$$\omega = \frac{1}{\sqrt{L * (C_{db} + C_{gs} + 4C_{gd})}}[rad] \tag{2.22}$$

where the C_{db},C_{gs} and C_{gd} are parasitic capacitance from transistor M1 or M2 in the cross-coupled pair. Apparently, due to extra parasitic capacitance, the oscillation frequency is lower than a LC tank.

Varactor

Varactor is a component wich corresponds to the variable capacitance seen in (Figure 2.8). It is directly controlled by the feedback signal from output of loop-filter. By changing the capacitance of varactor, the total capacitance is changed which results in the changing in frequency. The varactor consists of two NMOS transistors, whose drain and source are connected. As shown in Figure 2.11.

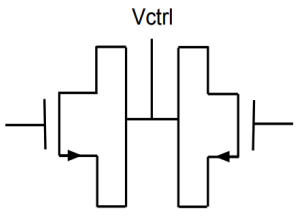


Figure 2.11: Varactor

Capacitor Bank

If the VCO is designed for a larger turning range, capacitor bank are usually used to provide some extra turning range instead of using a single varactor. Because the capacitance of a varactor is quite limited. A capacitor bank is a group of several capacitors that are connected in series or parallel. Each of those can be connected or disconnected with the circuit to change the oscillation frequency which is controlled by binary switching signals. In our design the turning range should be over 20%, that results in a demand of a large capacitor bank. The capacitor bank is commonly binary weighted. When control signals are all logic high, the highest capacitance will be reached. When control signals are all logic low, all switches are off, then the lowest capacitance will be reached.

Current Tail Design

A simple current bias circuit can be used as a tail that sets output voltage of the oscillator. One consideration that should be taken into account is that harmonics, that will add to the phase noise, occur at the node of the current source of the cross-coupled pair. In this project, an extra filtering technology is used to solve this problem. This will be mentioned later in the design chapter.

2.5.2 Gain of VCO

The gain of VCO is defined as change in frequency with respect to change in input voltage

$$K_{vco} = \frac{\Delta f}{\Delta V}[Hz/V] \tag{2.23}$$

In general, the output frequency should be proportional to the control voltage. However, in reality, this linearity becomes worse when the control voltage is close to its supply or ground. When the VCO gain changes due to non-linearity, the loop gain of the PLL changes for different frequencies within the frequency range. This results in a compromise to the jitter transfer and generation of the module. The loop filter can be designed for different regions of the frequency range to decrease this effect, but this is not an efficient solution and not possible when a passive filter is used in a real chip[16].

2.6 Divider

The divider is used to scale down the VCO output frequency in order to compare it with the reference frequency. There are both analog and digital divider structures, both frequently used in PLL design. In digital dividers, the speed of their logic gates limits their working frequency (tens of GHz). Hence, they are not suited for higher frequency applications. For very high frequencies analog dividers are commonly used. TSPC and CML structures are two topologies commonly used for higher frequencies. They are usually used as a pre-scaler, the first stage of divider

chain. Then, when the input frequency is relatively low, a programmable divider is used to scale it down further, within a range close to the reference frequency. In modern day frequency synthesis, dividers consume a large percentage of the total power [17]. In our project, the CML-prescaler has an average current of 1.6mA and accounts for 15.6% power consumption of PLL. There are several different divider architectures that are used for different applications, one consideration being the limitation of their operating frequency range. Regenerative dividers forms a feedback loop that requires additional circuitry. Parametric dividers uses a non-linear element, such as a varactor diode, to generate a subharmonic oscillation. They offer a simple circuit configuration and broader bandwidth in comparison with other analog alternatives. Injection-locked dividers uses the free-running frequency of an oscillator with an injected signal. They tend to consume less power than other structures, the drawback is their low locking range. Digital dividers dominate the market in applications working within their frequency range. The reason being that they are more efficient, easier to implement, takes up less area and consumes less current than the other structures. Although, their power consumption increases with the frequency operation. The divider structures used in the design will be covered more in detail. For some completeness, other dividers are briefly discussed.

2.6.1 Regenerative Frequency Divider

A regenerative divider, also known as Miller divider, is a feedback system that may operate over a wide bandwidth and a large range of input levels. The structure is shown in Figure 2.12. The mixer outputs a sum and difference frequency of its input and feedback. These signals are then fed to an amplifier through a filter. The amplifier can amplify the signal in case of any conversion loss while the filter is used to prevent unwanted operation because of sum frequencies. These type of mixers can operate while maintaining low phase noise and noise floor. Unfortunately, due to the required amount of circuitry they are unattractive for use as dividers in systems opting for low power[18]-[20].

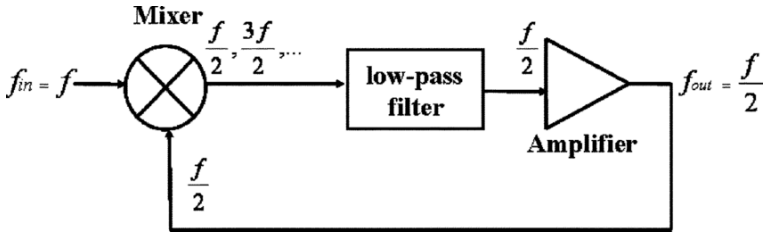


Figure 2.12: Regenerative divider structure

2.6.2 Injection-Locked Frequency Divider

These dividers are based on an oscillator(non-linear element) working in tandem with a filter(mode selection) by synchronizing the oscillator with an injected signal as shown in Figure 2.13. Consider the following example.

If the output frequency is f_{out}, then the mode filter should be a bandpass filter tuned to that frequency. Next, we need a non-linear element that can provide a spectral component at f_{out}, when the input frequencies are f_{out} and $f_{in} = 2f_{out}$. In other words, we want a non-linear element that generates a difference frequency component, i.e an oscillator. A typical schematic is shown in Figure 2.14.
There are three classes of injection-locked oscillators defined, depending upon the ratio between the oscillation frequency to the frequency of the injected signal. These classes are called first-harmonic, subharmonic and superharmonic. The first-harmonic the oscillation frequency is the same as the fundamental frequency of the injected signals. Whereas for the other two, the injected frequency is a harmonic of the oscillation frequency.
It has been shown that injected-locked frequency dividers can operate at higher frequencies and still consume relatively low power. Hence, they are quite attractive for low-power and high-frequency wireless systems. However, tradeoffs such as increased area and narrow frequency range(since it is a tuned circuit) should be considered[17][19][21].

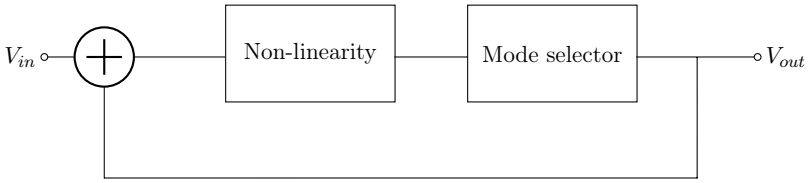


Figure 2.13: Injection-locked oscillator model

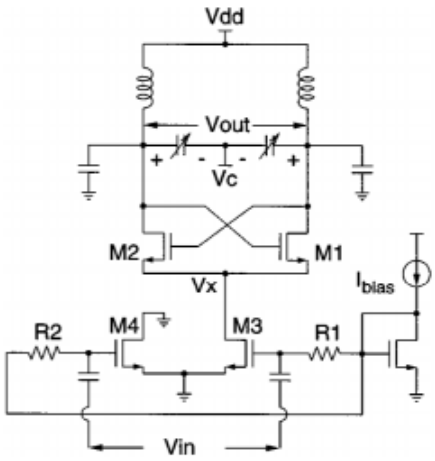


Figure 2.14: Injection locked frequency divider

2.6.3 Parametric Frequency Divider

The frequency division principle of a parametric divider relies on exciting a varactor at a frequency and to realize a negative resistance that sustains loop gain of unity at half the input frequency. Like other non-linear reactances, varactors can generate power not only at harmonics, but at subharmonics of the input frequency. The circuit consists of two coupling networks as shown in Figure 2.15, usually implemented as LC-networks that act like filters and are tuned at the desired input and output frequencies. Ideally, if the filters have high Q-values and if the varactor is not affected by non-ideal effects, it is possible to achieve very high efficiencies. Since high Q-value passive elements cannot be implemented in contemporary silicon technologies, parametric dividers are not suited for that kind of technology[22].

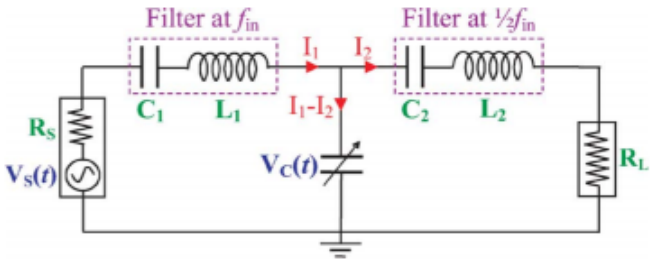


Figure 2.15: Divide-by-2 parametric divider

2.6.4 Current mode latch prescaler

A CML divide-by-2 prescaler consists of two CML latches. Using two complementary signals as input signals.

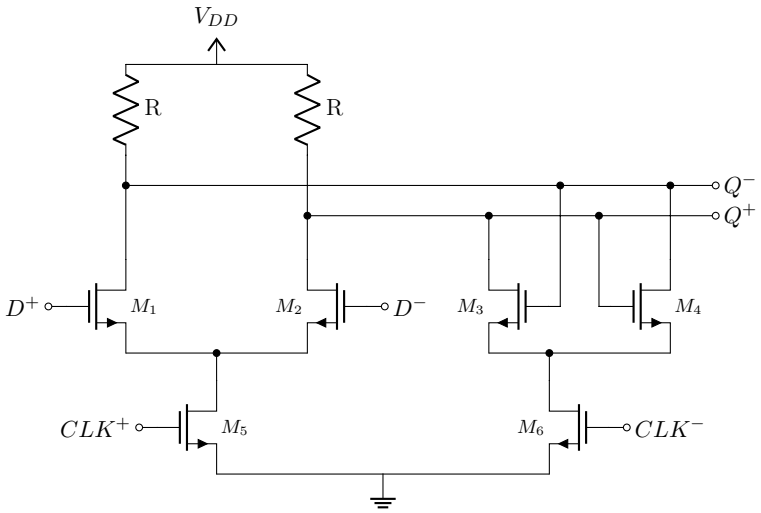


Figure 2.16: CML latch

A conventional current mode logic latch consists of a sample and a hold stage. Switching is controlled by complementary clock signals. It can scale down the frequency by a factor of 2. In a common CML latch, a current tail is used. Current flows through either one of the two branches. Output voltage takes a value $V_L = VDD - I_s * R_L$, the other branch with no current remains at VDD. The output swing is therefore $I_S R_L$. When the clock is high, M1 and M2 track the input. When the clock is low, M_3 and M_4 latches the state. M3 and M4 are supposed to provide a gain in store mode, allowing for a short cycle operation.

Conventional latches will use the same transistor sizes for sample and hold pair for complete current switching to take place in the circuit. Parasitic capacitance in the transistors require the tail current to be much larger than it needs to be in order to obtain a higher slew rate, and thus higher operation frequency. This is wasteful because the hold transistors need not be so large that the track and hold branches can use separate biasing currents to operate[23].

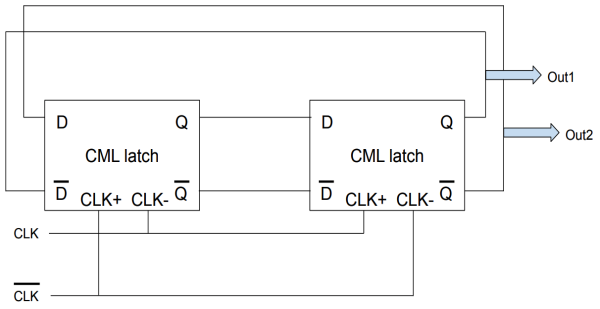


Figure 2.17: CML divide-by-2 prescaler

2.6.5 Programmable Divider

A commonly used programmable divider, also known as multi modulus divider (MMD), consists of a chain of 2/3 dividers. The division ratio can vary from 2^n to $2^{(n+1)}$-1, where n is the number of 2/3 dividers. By setting the control bits $R_4R_3R_2R_1$, a programmable ratio can be realized.

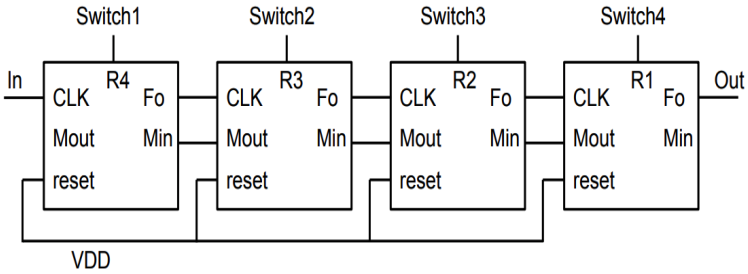


Figure 2.18: Programmable Divider

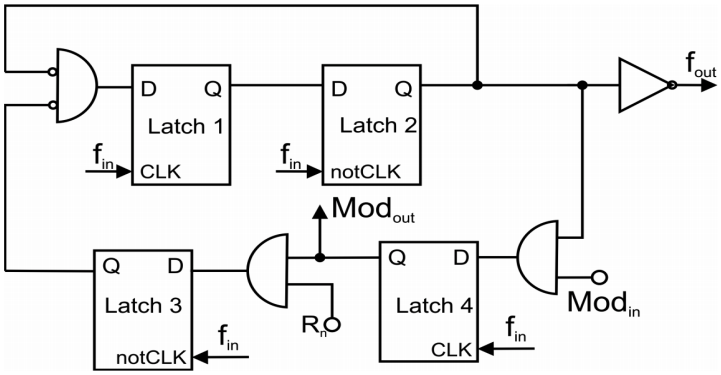


Figure 2.19: 2/3 Divider

The chain of four cascaded divide-by-2/3 units is capable of dividing clock signal by any integer number from 16 to 31. R_n represents the individual cells that will divide by 2 or 3. Mod_{in} signal is a feedback input coming from the next stage. It determines when to check the R_n signal to decide division ratio. Division by 3 is achieved by swallowing one extra period of input signal[24][25]. Thus the duty-cycle differs. For divide-by-2, duty-cycle is 50%, as for divide-by-3, duty-cycle is 2/3. Total divide-ratio is given in Equation 2.24

$$T_{out} = (2^n + 2^{n-1} * R_{n-1} + 2^{n-2} * R_{n-2} + ... + 2 * R_1 + R_0) * T_{in} \qquad (2.24)$$

2.7 Phase detector

The purpose of a phase detector is to compare the phase of two input signal and to generate an output voltage corresponding to the difference between them. There are various types of phase detectors and they are used in many different applications, one of them being the PLL system.

2.7.1 Phase only sensitive

As the name implies, the output of the phase only sensitive detector is only dependent on the phase difference between its two input signals. When there is a constant phase difference between its inputs the detector generates a constant voltage. When there is a frequency difference between the two signals, the detector generates an alternating voltage at a frequency that matches the frequency difference. The phase difference is given by the difference frequency product. A flaw with this structure is that the locking range of the PLL tends to get limited. There is a risk that the signal generated by the difference frequency product falls outside the pass-band of the loop filter, thus, no error voltage will pass through the filter onto the VCO tuning varactor, which affects the locking range[28]. There are a few different ways to overcome this problem, for instance by adjusting the tuning range of the VCO to make sure that the difference product falls within the pass-range of the filter. Unwanted signals such as harmonics, subharmonics, sum frequency and input leakage needs to be suppressed. Otherwise they may cause issues in frequency synthesizers which other detectors can mitigate.
There are several types of phase only sensitive detectors, both analog and digital detectors. The most common analog detector is the multiplier, often implemented with a Gilbert-type topology. Another common choice is the double balanced diode mixer. Analog detectors are best suited for sinusoidal input signals, whereas digital detectors are best suited for square-wave like signals. They usually operate by outputting a logic high when two input states are different or a logic zero when they are the same. In order to grasp the problems with these types of detectors two of them are described below.

XOR Gate Phase Detector

The XOR gate is a commonly used logic gate overall and can also be used for phase detection. When the average output is zero, the phase error is 90°. As shown in Figure 2.21.

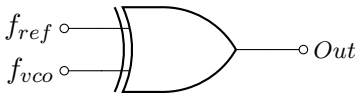


Figure 2.20: XOR gate

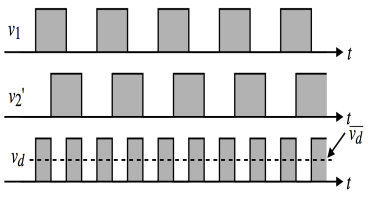


Figure 2.21: XOR Gate is locked at 90°

The ideal locking range is 0 to π or -π to 0. If there is a frequency difference between the input signals, the gain of XOR-PD will jump between a negative and a positive value. Thus, only a linear phase detection range of 180°can be obtained[26].

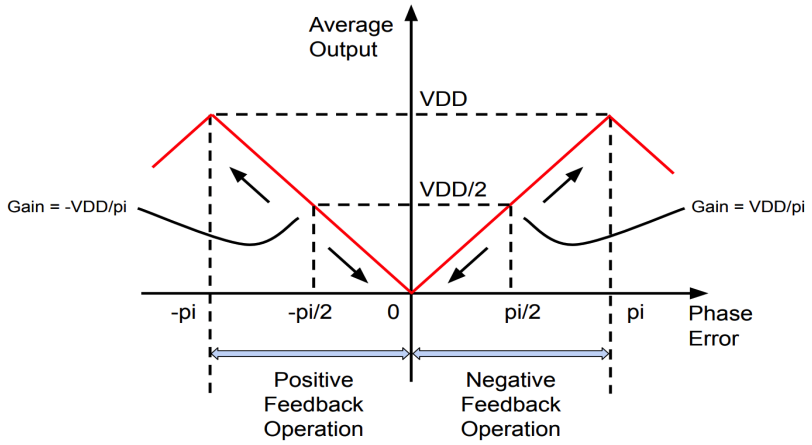


Figure 2.22: XOR input-out

The XOR-PD is sensitive to the input duty cycle. If the input signals are not 50% duty-cycle, the PLL finally will lock with a phase error. The output amplitude is independent of input amplitude. All detectors has a proportionality constant which represent its gain. The constant, often noted as K_D, relates the output voltage due to input phase difference and is for this detector given by

$$K_D = \frac{V_{DD}}{\pi}. \tag{2.25}$$

2.7.2 JK flip-flop Phase Detector

JK flip-flop is another type of phase detector, more specifically, it falls under the sequential phase detectors category. These types of detectors can provide a zero, or an 180°, phase difference in lock and have tremendously different gain constants. Although, they come with some disadvantages. Since they operate on transitions they are quite sensitive to missing edges. They also introduce a sampling into the loop system.
The JK flip-flop detector is able to lock the signals at 180° phase error. This means that when the input signals have a 180° phase error, the output signal will be zero in average. The gain constant is given by

$$K_D = \frac{V_{DD}}{2\pi}. \tag{2.26}$$

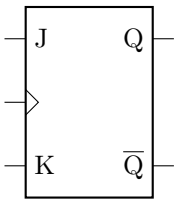


Figure 2.23: JK Flip Flop

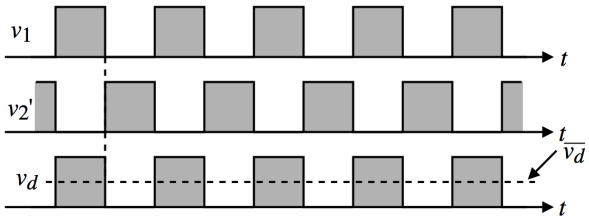


Figure 2.24: JK flip-flop is locked at 180°

Input-output characteristic of JK flip-flop is shown as Figure 2.25. It usually operates between 0 and 2π.

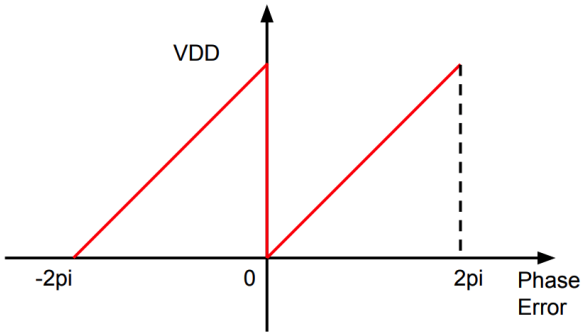


Figure 2.25: JK input-output characteristic

The JK flip-flop PD is not sensitive to input duty cycle but to rising edges. The gain of JK flip-flop PD is constant between 0 and 2π. One risk of using JK flip-flop is that it may lock at one of the harmonics from the reference clock[26].

2.7.3 Phase Frequency Detector

The other form of detectors is said to be sensitive to both phase and frequency. The main difference is that it allows phase error detection with in a range of $\pm 180°$ which allows the detector to detect if a signal is lagging in frequency compared with the other. The absolutely most common PFD is the sequential detector with extended range (also known as Dual-DFF or Tri-state PFD). It can lock at 0°, and is not sensitive to input duty cycle. It consists of two resetable edge triggered D flip-flops and an AND or NAND gate, depending on the design of the flip-flops. The D-input is always a logic high while the the clock inputs are the reference and VCO signals and it consists of two outputs noted as UP and DN. A typical implementation is seen in Figure 2.26.

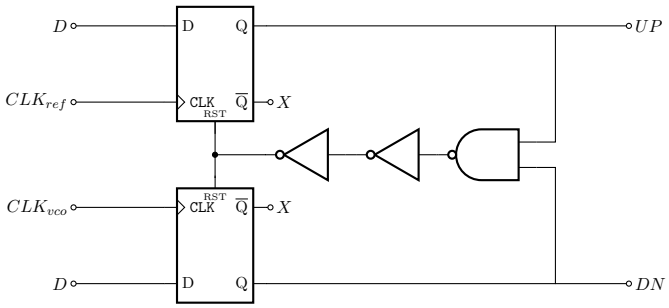


Figure 2.26: Phase-frequency detector

The basic functionality is quite easy to grasp. When the reference goes high the UP signal must go active. Accordingly, when the VCO goes high the DN signal must go active. When both UP and DN signal goes high the reset signal will activate and put UP and DN in their reset state. The behavior is represented in the following state diagram.

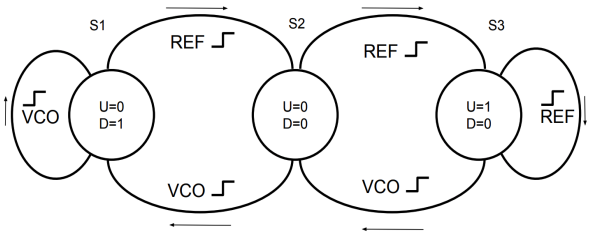


Figure 2.27: PFD state diagram

This topology has a significantly wider detecting range compared with other two mentioned above. The detection range is 4π, with a constant phase detector gain of

$$K_D = \frac{V_{DD}}{2\pi}. \tag{2.27}$$

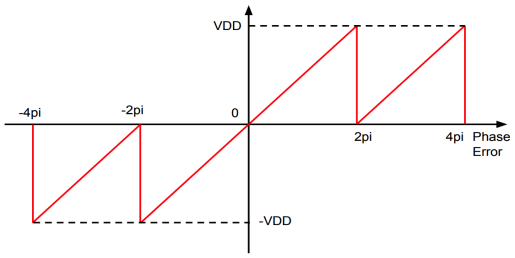


Figure 2.28: Ideal PFD input-output characteristic

An occasional, yet common, problem with the PFD is a phenomenon called dead zone. The problem occurs as the loop gets closer to in-lock, then the UP and DN signals get exceedingly narrow due to delays in the logic gate circuitry. Then the pulses may be too narrow for the next stage to function properly. Which degrades the behaviour near the locking point in a way that the detector is unable to detect phase errors reliably near lock[29].

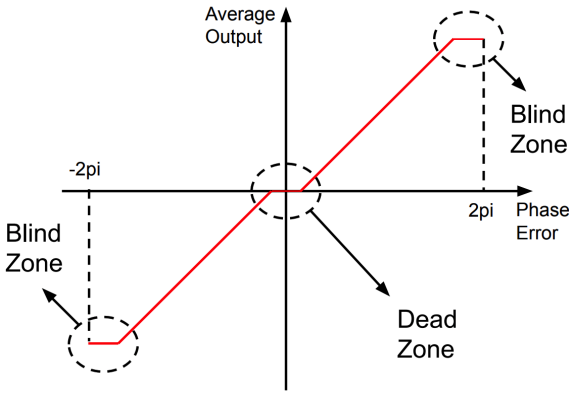


Figure 2.29: Dead zone and Blind zone

Zero dead zone is a fundamental requirement of phase detector. Which means ideally even a infinitely small difference in phase exists, PFD is able to detect it properly. If a PFD works in the dead zone, then the PLL will be locked into an incorrect phase and frequency. Also it will introduce more jitter and phase noise to the system[27].

To eliminate the dead zone, a buffer is employed in the reset path as a deliberate delay cell, which ensures the output pulses with a constant width to turn on the switch transistors of the charge pump sufficiently when the phase of the inputs is aligned. Which explains the inverters seen in the schematic (Figure 2.26)[29][27]. However, this will cause a blind zone as a cost.

The blind zone can be observed in Figure 3.17. When the phase error is close to 2π or -2π, PFD cannot response to phase error correctly, and the gain may decrease or reversed. If the rising edge of the reference falls into the blind zone it will be detected incorrectly which leads to phase error. Decreasing the minimum pulse duration, increasing DFF response speed or lower the reference frequency can minimize the blind zone. If we assume that the minimum pulse duration of the input signal that makes the PFD zero dead zone is T_{min}, the blind zone can be expressed as

$$T_{bz} = T_{DFF} + T_{min} + T_d = T_{DFF} + T_{rst} + 2T_d, \tag{2.28}$$

where T_{DFF} is the response time of the flip-flop, T_{rst} is the pulse width of the reset signal and T_d is the delay time of the NAND gate and the two inverters.

From this, the maximum phase error detection range can be derived as

$$\Delta\theta_{max} = 4\pi(1 - \frac{T_{bz}}{T_P}) = 4\pi(1 - \frac{T_{DFF} + T_{rst} + 2T_D}{T_P}) \tag{2.29}$$

where T_P represents the period time of the input signal[13].

2.8 Charge pump

Charge pump is used to sink or source current to or from the loop filter based on the output from the phase detector. When the phase detector sends an UP pulse the charge pump converts it to a current that charges the loop filter, i.e, charge current. Correspondingly the loop filter gets discharged by the DN pulse. When both switches are off the voltage is held constant since there is no current flow. The up and down charges will respectively charge and discharge the loop filter output, and as a result the VCO output frequency will increase and decrease accordingly. The switches in the model are usually implemented by NMOS and PMOS transistors. Charge pumps tend to suffer from non-idealities such as charge sharing, current mismatch, charge injection, noise and power dissipation. Various charge pump topologies exist that help reducing these non-idealities.

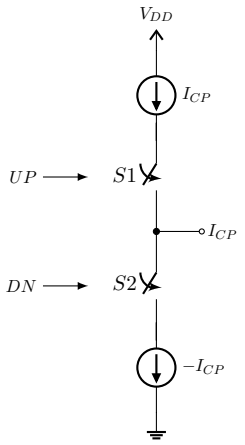


Figure 2.30: Charge pump model

Generally charge pumps can be categorized into four different topologies: conventional tri-state, current steering, differential input single-ended output and fully differential[31]. Each topology attend to the non-idealities somehow and cause different results in performance. Their performance can be summarized in Table 2.2.

Architecture	Power Dissipation	Speed	Clock skew
Tri-state	Low	Moderate	Moderate
Current steering	High	High	Moderate
Differential input single-ended output	Medium	Moderate	Low
Fully differential	High	High	Low

Table 2.2: Performance of various architectures

2.8.1 Non-ideal behavior

As mentioned there are various non-idealities that needs to be considered when designing a good charge pump. In this section they are described and some solutions to reduce their effect are proposed.

Charge Sharing

Is mainly due to the positioning of the transistor switches. When S1 and S2 are both turned off, the voltage at the nodes above and below the switches will be pulled up or down to VDD and ground respectively. Due to the reset pulse there will be narrow pules in either UP or DOWN signal which will cause both switches to be on simultaneously for a short period of time. During this time, the voltage at the nodes will increase or decrease respectively resulting in a deviation at the output due to charge sharing between the switches's capacitance and the load capacitance. A conventional solution is to use an operational amplifier to keep the voltages at an equal level when both switches are on[31].

Leakage

When charging and discharging switches are off, there should be no current flowing into or out from the load. However, because of transistor characteristics there will always exist sub-threshold leakage contributing to non-ideal behavior.

Switching Delay

The UP signal is intended to control a PMOS, which means when the UP is 0, charging path is open. Thus an inverter is needed between output of PFD and UP-input of Charge pump.

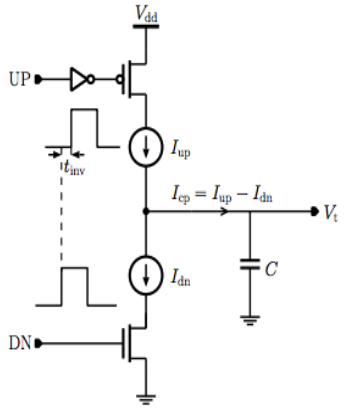


Figure 2.31: Charge pump model with transistor switches

By adding an extra transmission gate on the DN path or using complementary differential cascode inverters one is able to minimize the time delay. However it is impossible to get 100% synchronized signals.

Charge Injection and Clock Feedthrough

Charge Injection and Clock Feedthrough are non-idealities that arise due to the transistor switches.

Charge Injection

When a switch is on, there is approximately zero voltage across its drain and source terminals. During the time when the transistor is on, it holds mobile charges in its channel. Once the switch is turned off, due to the fact that there is no longer an electrical force to attract the channel charge, the mobile charges must flow out from the channel region. The charges are then injected to the source and drain terminals. Thus storing an additional charge in the output capacitor C_L, which leads to a voltage error.

Clock Feedthrough

Clock Feedthrough is an effect caused by capacitive coupling. The Gate-Drain and Gate-Source capacitance will couple the clock signal when switching happens. The voltage of C_L can rise above VDD which causes ripples in the signal.

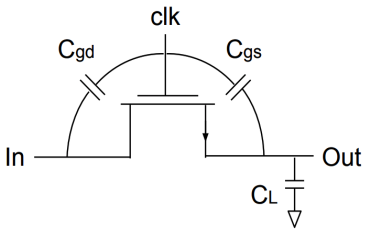


Figure 2.32: C_{gd} and C_{gs} of transistor

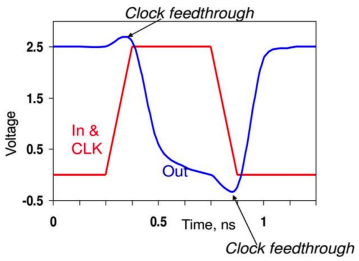


Figure 2.33: Clock Feedthrough Effect

An effective method to reduce these non-idealities is to actively place the switches away from the output or to place them at the source. Other approaches to solve the problem are to add a dummy switch or replacing the switches with transmission gates.
By adding a dummy switch with its drain and source shorted in series with the switch, controlled by the inverted signal of the switch, half of the charge when the switch turns off will be injected into the dummy. This charge will be matched with the charge induced by the dummy, hence the overall charge injection is cancelled. When the dummy turns off it will inject charge in both directions, however since drain and source are shorted and the switch is on, all the charge from the dummy will be injected onto the low-impedance voltage driven source which is charging the load. Therefore the charge will not actually affect the value of the output voltage.
Replacing the switches for transmission gates will result in lower changes on the output voltage due to complementary signals that will act to cancel each other out. Although the gate must be designed to obtain synced switching time[32].

Current Mismatch

Current mismatch is the mismatch of charging and discharging current. As mentioned above, the ideal charge pump has no mismatch. However, due to channel length modulation and the different mobility of PMOS and NMOS, UP and DN current can be different. This mismatch means that the PLL will lock with static phase error. As in frequency domain, spurs at the reference clock frequency offset will increase. Figure 2.34 shows a common case when a charge pump is poorly designed. The top line is the discharging current, the bottom line is charging current. The difference between then, i.e the mismatch line, is in the middle.

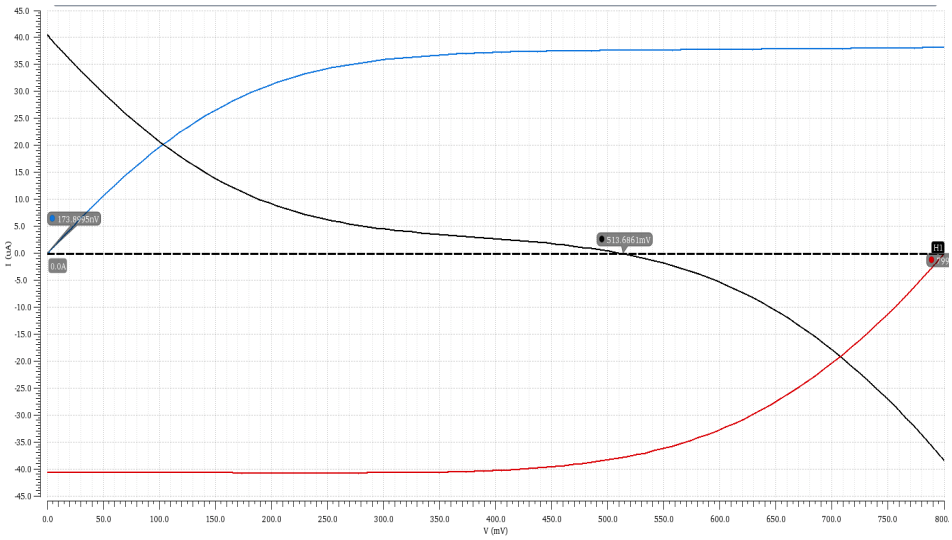


Figure 2.34: Charge Pump Mismatch

This is the most considered non-ideal behavior in charge pumps and attempts to minimize this has given rise to many different topologies. There are mainly two approaches on how to reduce current mismatch. Either by using some sort of compensation method or by increasing the output resistance. A typical compensation method is to use one or more operational amplifiers which enables tracking of the voltages that determines the charge- and discharge currents. The output resistance can be increased either by using cascoded topology or gain-boosting topology. In addition to these methods, using large devices and large overdrive may be used to reduce mismatch.

When the PFD is used with a charge pump the net current is given by

$$I = I_{pump}\frac{\Delta\Phi}{2\pi}, \tag{2.30}$$

where $I_{pump} = I_{up} = I_{dn}$. This current, multiplied with the impedance of the loop filter, generates the output voltage that goes to the VCO.

2.9 Loop filter

The loop filter is a linear filter that is mainly used to provide a tune control signal to the VCO by averaging the phase error signal from the phase detector, thus assuring that the phase error from the detector remains zero. In order to fulfil this requirement the loop filter must provide an integration. Then, to ensure loop stability, the filter must also provide a zero. There are two types of loop filters that exist, the passive and the active filter. Each of them satisfies the above mentioned requirements and can be of multiple orders. They have different topologies which are, naturally, suited for different PLL structures.

In the simplest case, a passive RC network can be used to connect the phase detector with the VCO. However, the bandwidth of the loop would be inversely coupled with the static phase error which would not be zero. Hence such a filter is limited and is not suited for critical applications.

Using a typical active filter architecture provides the necessary integration and loop transfer characteristics due to the pole-zero configuration in the feedback path and the series resistor at the input.

However, a simpler and more commonly used approach is to use the charge pump working in tandem with an RC-network. While maintaining the same loop filter transfer functionality, this approach also obtains reduced power consumption, complexity and area. Again, in the simplest case, a simple RC-network can be used where the capacitor works as an integrator that is either charged or discharged depending on the charge pump output, and the resistor provides a loop stabilizing zero.

As mentioned before, the filter can be designed with multiple orders. A higher-order filter may provide more attenuation on out-of-band components, hence reducing spurs in the signal arising from the phase detection process and other noise sources. However, the higher order, the harder it is to obtain loop stability due to the contribution of phase lag. Basically, to get better noise reduction a larger bandwidth is desirable,on the other hand, too large bandwidth will affect the phase locking time which may cause issues in systems where fast channel switching is required. Higher order filters are more complex to design and since fast locking time is crucial in most applications it is usually sufficient to use a third-order loop.

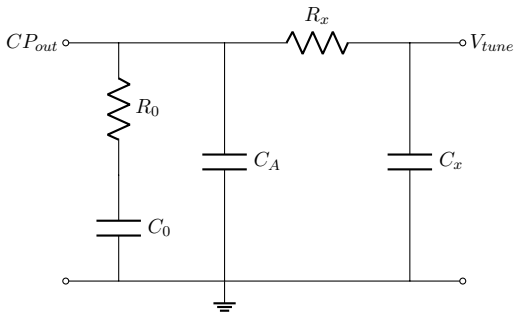


Figure 2.35: Third order passive loop filter

In Figure 2.35 the R_0C_0 network is a lead-lag filter where R_0 provides a loop stabilizing zero to the otherwise pure integration caused by C_0. Capacitor C_A suppresses reference spur and the R_xC_x network provides a low-pass filter for additional filtering. Resistor R_0 has a large thermal noise which contributes to the VCO phase noise. The loop transfer function, H_{LF} is given by

$$H_{LF}(s) = \frac{1+\tau_0 s}{(C_A\tau_0\tau_x)s^3+(C_A\tau_0+C_0\tau_x+C_A\tau_x+C_x\tau_x)s^2+(C_0+C_A+C_X)s} \quad (2.31)$$

where $\tau_0 = R_0 C_0$ and $\tau_x = R_x C_x$.

The entire filter can be designed by following the procedure shown in section 2.9.1 considering parameters as phase-margin, crossover frequency and gain from previous parts of the system[19].

2.9.1 Loop filter recipe

Step 1: *Specify a phase margin.* Once this value is chosen, it sets a constraint on capacitor values. More specifically,

$$PM \approx \arctan\sqrt{b+1} - \arctan\frac{1}{\sqrt{b+1}}, \tag{2.32}$$

and

$$b = \frac{C_0}{C_A + C_X}. \tag{2.33}$$

Here it is well advised to choose a phase margin a few degrees above the the target value to account for negative phase contributions by the nature of the loop system.

Step 2: *Select loop crossover frequency* based on the tracking bandwidth. This value is usually chosen to be at least a decade below the reference frequency.

$$\omega_c \approx \frac{\sqrt{b+1}}{\tau_z} = \frac{\sqrt{b+1}}{R_0 C_0}. \tag{2.34}$$

Step 3: *Calculate* C_0, the value of the zero-making capacitor. Thus,

$$C_0 = \frac{I_{CP}}{2\pi}\frac{K_{vco}}{N}\frac{b}{\sqrt{b+1}}\frac{1}{\omega_c^2}, \tag{2.35}$$

where I_{CP} is the charge pump current, N is the divide modulus, and K_{vco} is the VCO gain constant in radians per second per volt.

Step 4: *Calculate* $R_0 = \tau_z / C_0$. This completes the design of the main part of the filter.

Step 5: *Select* $\tau_x = R_X C_X$ within the following range:

$$0.01 < \tau_x / \tau_z < 0.1. \tag{2.36}$$

Here we have high freedom of choice in choosing the low-pass filter time-constant. A higher value results in somewhat better filtering action. However, it tends to be associated with lower stability, hence there is a trade-off between filtering and stability.

Step 6: *Complete the remaining calculations.* After *Step 3 and 5* we are able to decide a value for C_x, then from *Step 1* we know the sum of C_x and C_A and are able to decide a value for C_A as well. Arbitrarily, setting them equal is a common choice.

If the calculation result suggests a quite large capacitor or resistor, then designer should consider the area limitation in a real case and adjust the parameters to get a reasonable result.

Chapter 3

Design process

A phase-locked loop within an output working range of 8-10GHz was desired. To achieve this, a frequency plan was developed where a 9.83GHz VCO with 20% range would output a signal to be scaled down by a pre-scaler followed by a programmable divider. This divider chain was designed to obtain a division ratio based on a reference frequency of 163.84MHz. Good phase noise performance was desired with a minimum total current consumption to be less than 10mW. These requirements are given by the Beammwave company which suits the application they are developing.

In this chapter, the design process and the means to evaluate the performance are elaborated. Two different designs of the system is to be evaluated, where frequency divider chain and charge pump designs apply different topologies and the design parameters of the other components, using the same structure, deviate from each other. Using different sets of parameters will naturally give rise to different performance values. This has to be taken into consideration when designing the remaining blocks, thus the design parameters deviate. The reason why different structures and parameters are used is two-folded. The first part being that different structures allows comparison in performance and the second, main, part being that it allows us both to learn about RFIC design. Since we are two people opting for the same goals in the same project, naturally, we do our own designs that uses different parameters in order for us both to learn.

Note, that many different structures of each component were implemented, whereas the ones obtaining best performance for the given application are presented in this chapter. Starting with the VCO, the key component, moving on to the frequency divider chain, phase frequency detector, charge pump and lastly loop filter designs are discussed.

3.1 VCO

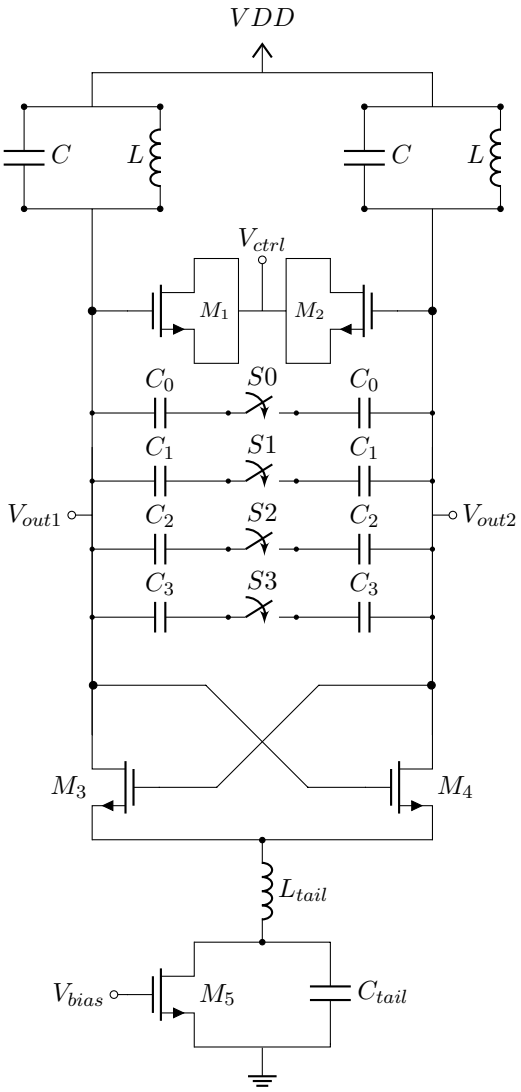


Figure 3.1: Voltage controlled oscillator

In our project, we use an LC-tank VCO. The sizing of components is given below in Table 3.1. All widths and lengths are given in meters, capacitance given in Farads and inductance given in Henry. Sizing of some capacitors and inductors are also presented For the inductor the w indicates turn width, D is the diameter and spc is the turn spacing.

	Design A	Design B
Tank C	w=30μ l=28μ C=327f	w=23μ l=23μ C=237f
Tank L	D=70μ w=4μ spc=5 L=170p	D=72μ w=6μ spc=5μ L=169p
M1,2	m=2 w=65μ l=80n	m=2 w=40μ l=100n
M3.4	w=32μ l=135n	w=25μ l=3.125μ
L tail	D=60μ w=4μ spc=5 L=143p	D=25μ w=6μ spc=5 L=58p
C tail	C=726f	C=750f
M5	w=31μ l=18n	w=30μ l=18n

Table 3.1: Size table of VCO

In order to obtain a low noise VCO, some rules should be considered. The most valuable model for oscillator single-side-band (SSB) phase noise is the one shown in (Equation 3.1) [30][33].

$$\mathcal{L} = 10log\left[\frac{1}{2}\left[\left(\frac{f_0}{2Q_L f_m}\right)^2 + 1\right] * \frac{FkT}{A} * \left(\frac{f_c}{f_m} + 1\right)\right] \tag{3.1}$$

where

$\mathcal{L}$=Single Side Band Phase Noise density[dBc/Hz]
A=Oscillator output power[W]
F=Device Noise factor at operation power level A
k=Boltzmann's constant, $1.38 * 10^{-23}$
T=Temperature[K]
Q_l=Loaded-Q[dimensionless]
f_0=Oscillator carrier frequency[Hz]
f_m=Frequency offset from the carrier[Hz]
f_c=flicker noise corner frequency[Hz]

The Quality factor(Q) indicates energy loss relative to the amount of energy stored within the system. A low Q due to a high resistance in series with the inductor produces a low peak on a broad response curve for a parallel resonant circuit. A high Q is due to a low resistance in series with the inductor. This produces a higher peak in the narrower response curve. The high Q is achieved by winding the inductor with larger diameter, lower resistance wire. In our case, the diameter is 70μ which reaches the largest value we could get.

Using a large capacitor in parallel with the resonant circuit can improve the resonator loaded-Q. Doubling the loaded-Q leads to phase noise degradation by 6dB. Doubling the operation frequency results 6dB phase noise increase.

When the VCO design is completed, the output of VCO is usually not rail to rail resulting in some voltage swing. In some cases, this little swing may cause the signal to be non applicable to the divider chain. Thus, an additional voltage converter should be added between VCO and divider chain to get an applicable

signal. The converter is a simple circuit consisting of a large resistor, an inverter and a small capacitor as shown in (Figure 3.2).

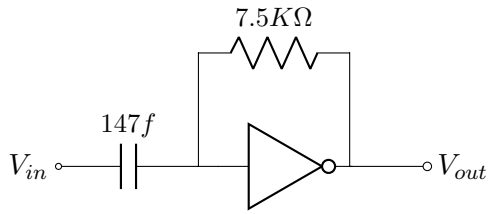
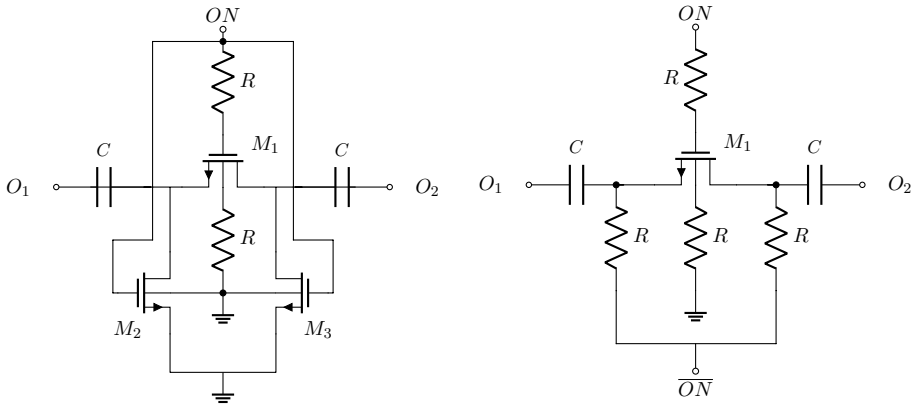


Figure 3.2: Voltage Converter

3.1.1 Switch and Capacitor Bank



(a) Topology A **(b)** Topology B

Figure 3.3: Switch circuitry

Binary controlled capacitive switches are introduced into the system in order to control the oscillation frequency. Thus, when a switch is off, there should be no extra capacitance introduced except the tank-C and varactor. However, the parasitic capacitance of capacitor bank is quite large when it is turned off. In order to minimize this non-ideal effect. We use switches as shown in Figure 3.3.

Two metal-oxide-metal capacitors are connected to three transistors. C_{mom} is the capacitance from MOM capacitor, R is on-resistance of M_1, C_{par} is the parasitic capacitance of transistor M1, C_{off} and C_{on} is the capacitance of a single capacitor bank cell when it is turned on or off. When the bank is on, due to the small R, the capacitance C_{off} will approximately be C_{mom}. In the off-state, R is large, thus the capacitance will be series combination of C_{mom} and C_{par}. Since $C_{par} \ll C_{mom}$, the total capacitance C_{off} equals to C_{par} approximately.

In order to get a high ratio of $\frac{C_{on}}{C_{off}}$, we should minimize C_{par}. However, this leads

to higher on-resistance and thereby a lower Q-value. A low Q bank cell may kill the whole circuit and make it hard to oscillate. Therefore, the switched capacitor should be designed carefully to balance the Q and $\frac{C_{on}}{C_{off}}$[34].

Components	Size/Value
M1	$11\mu/20$n
M2,3	$4\mu/20$n
R	10k
C	85f

(a) Topology A

Components	Size/Value
M1	$26\mu/40$n
R	10k
C	67f

(b) Topology B

Table 3.2: Sizing table of switched capacitor bank

3.1.2 Filter with Biasing tail

A filtering technique to lower the phase noise of the oscillator is used[35]. The idea is to add a passive filter at the tail to block the amplitude noise from the tail-current-source, and mainly so the noise does not reach the varactors in the tank. The noise near to second harmonic frequency will add to the phase noise of the whole system. Thus the filter was designed to have a high impedance at second harmonic frequency. A large capacitor is placed to filter the noise to ground, a high Q inductor is employed to provide high impedance.

In our project, we swept the parameters of tail so that we could find out the best filter to lower the phase noise. The value is given in the Table 3.1.

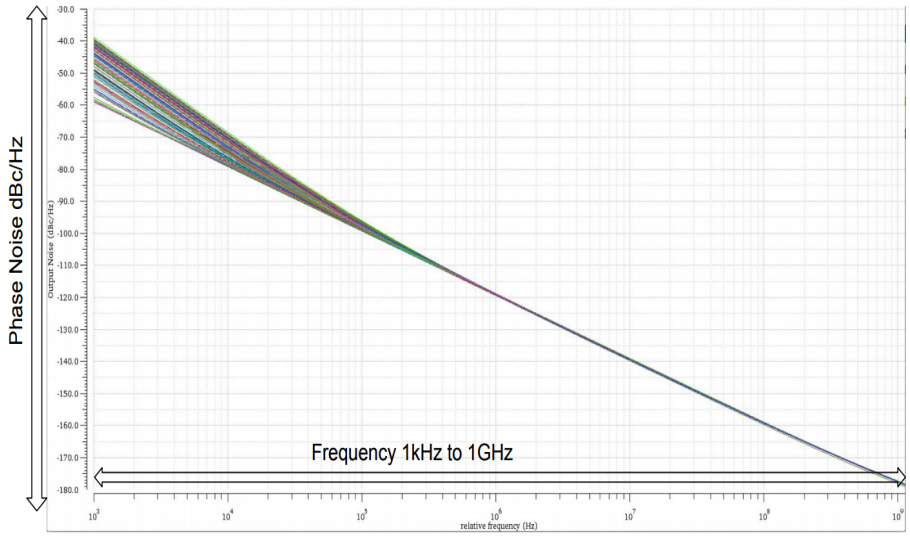


Figure 3.4: Phase Noise of VCO with different filters

The filter technique makes a difference mainly at low offset frequency. The PN at 1KHz varies from -39dBc to -58dBc. The slop of first decade(1KHz to 10KHz) varies from -30dBc/dec to -20dBc/dec. After 1MHz, all simulation results are quite identical as shown in Figure 3.4 and Figure 3.5.

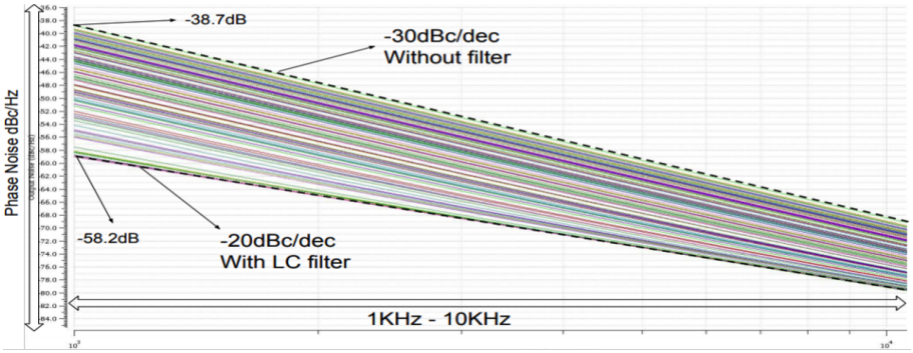


Figure 3.5: Phase noise of VCO from 1KHz to 10KHz with different filters

3.1.3 Measurement

Harmonic Balance simulation: HB simulation is a direct way to see the harmonic frequency distribution of the circuit. It is much faster compared with transient simulation within a limited number of harmonic frequencies. HB simulation can hardly be used in whole PLL simulation, because PLL is a very complex circuit, the calculation complexity is beyond the capability of simulator. The space and time it will take is impossible to access.

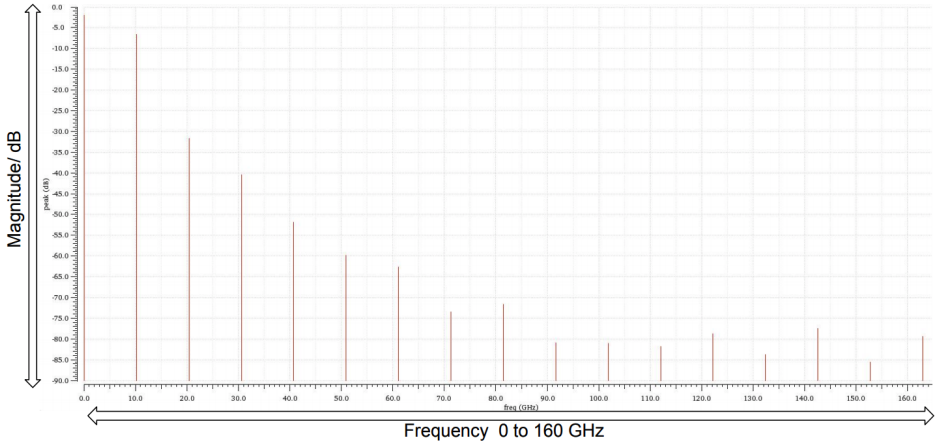


Figure 3.6: Harmonic frequency of VCO

The frequency close to 10G is the output frequency of the VCO at a certain Bias voltage and control voltage. To get the phase noise of VCO, we can run HB noise with HB simulation together or Pnoise with PSS simulation together. The results are not 100% identical. In our simulation, HB with HB noise gives us -114dB at 1MHz, PSS with Pnoise gives us a 2.5dB lower Phase noise at 1MHz. The reason of the difference between two simulations could be very interesting to dig into. However, that's not our concern in this project. The following figure of VCO phase noise is measured in HB simulator without tail filter. Thus the PN at low offset frequency is relatively higher compared with Figure 3.5.

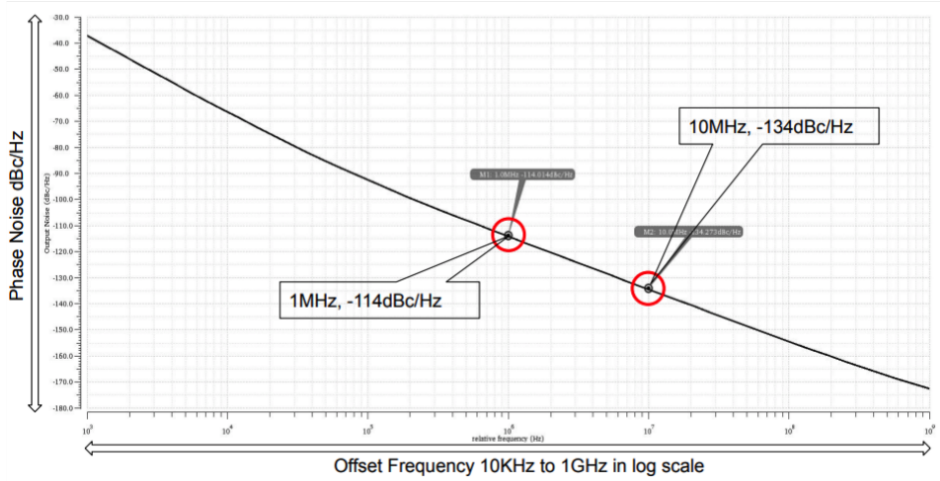


Figure 3.7: Harmonic frequency of VCO

Transient simulation: In the transient simulation, the output signal waveform can

be observed and analyzed. Thus transient simulation is a good approach to know how the changing of control voltage and switches combinations affects VCO as shown in Figure 3.8

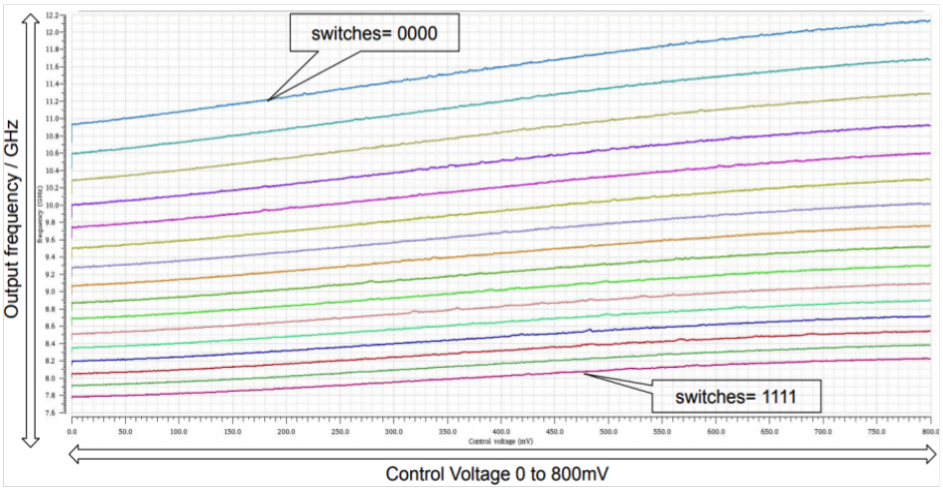


Figure 3.8: Switches Sweeping

X-axis is control voltage, Y-axis is the output frequency. When the control voltage changes from 0 to 800mV and the switches are 1111, the frequency changes like the bottom line. Other cases are the results of different switches combinations. A large turning range from 7.8G to 12G is obtained with a roughly 35% overlap in each band. The maximum gain of VCO is about 1.5GHz/V.

However, we should notice that when we simulate the whole PLL, the result is slightly different. Because of the parasitic capacitance of other components(equivalent to parallel capacitor), if the wanted frequency is achieved at $V_{ctrl} = 500mV$ in a single VCO testbench, when we look at the PLL simulation, the same frequency may be achieved at $V_{ctrl} = 600mV$.

The reason that we care about the V_{ctrl} is that if this voltage is close to 0 or VDD, there will be a large mismatch in the charge pump. The mismatch has to be compensated with wider pulse in the phase detector. All these lead to a worse phase noise and larger jitter.

The output of VCO is not rail to rail, thus an voltage converter is added at the output to make sure the output suits next stage.

3.2 Divider

The performance of divider includes working frequency range, power consumption, phase noise. In our project, the limitation of maximum working frequency and phase noise are saved. Because as long as divider work functionally in the

right frequency, we are satisfied with that. As for phase noise, it is usually quite low which will not be a dominant factor of the total phase noise in the system.
Two different pre-scalers were implemented using different architectures, dual-modulus and common-mode latch, yielding different division ratios. Next, a programmable divider based on cascoded 2/3 was used to reach the desired frequency of operation.
In Design A, CML and programmable divider are used. In Design B, 4/5 divider and similar programmable are used.

3.2.1 Dual modulus pre-scaler

As we know, pre-scalers are used to reduce a high frequency signal to a lower frequency by integer division. They may be configured so that they can divide by any integer value from 1 to 2^P, where P is the number of pre-scaler bits, and is usually a fixed value. A recurring issue when used in conjunction with a PLL is that the pre-scaler introduces undesired change in the relationship between the frequency step size and phase detector comparison frequency. For this reason, designers usually restrict the integer to a low value or use a dual-modulus pre-scaler[39]. A dual modulus pre-scaler has two separate frequency divisors, typically M and M+1. They consist of D-flip flops and NOT gates and can be configured in several ways depending on which division ratio is desired.

The dual modulus configuration used in our design is a divide-by-4/5 (Figure 3.9). The input frequency is given to all the flip flops whereas the selection of the counter depends on the Mode Control (MC) signal. When MC=1, one output cycle equals to 4 input clock cycles, hence a division by 4 is applied. Else is MC=0 one output clock cycle equals 5 input clock cycles, hence division by 5 is applied[40]. It uses the favorable master-slave configuration flip-flops instead of regular D-flip-flops and all gates are minimum sized.

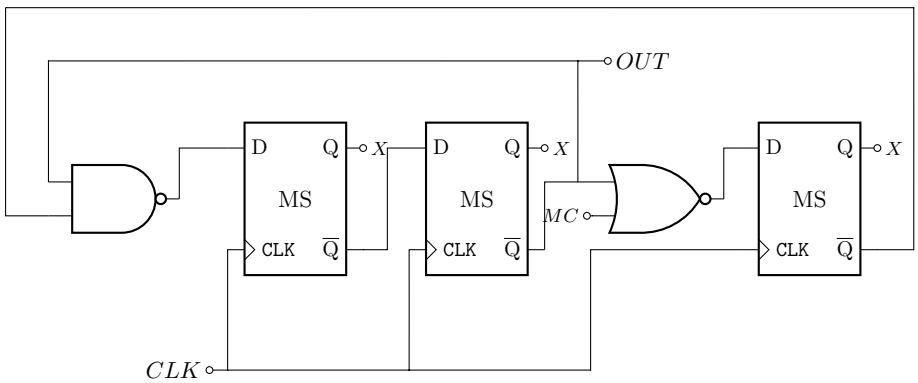


Figure 3.9: Divide by 4 or 5

The master-slave (MS) configuration is based on connecting two flip-flops in series, and inverting the enable input to one of them. It is called master–slave because

the second latch in the series (slave) changes only in response to a change in the first (master) latch. This structure ensures that the latches cannot be triggered at the same time, in doing so, overcoming the so called race-around condition. In a basic structure the problem occurs when both input signals and clock signal are high simultaneously. The configuration used in our design consists of a regular D-latch acting as the master and a gated SR-latch acting as slave (Figure 3.10).

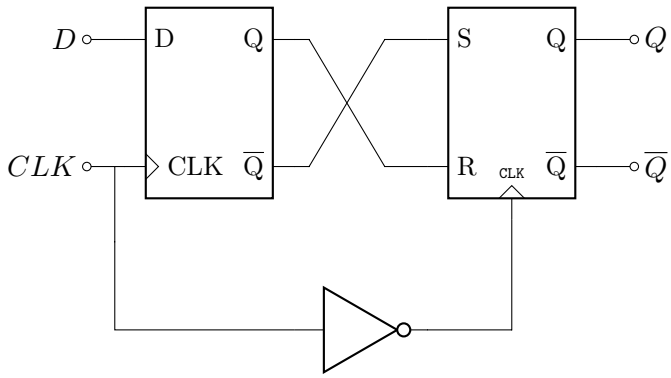


Figure 3.10: Master slave D-Flip-Flop configuration

The master takes the flip-flops inputs, D and clock. The clock input is fed to the latch's gate input. The slave takes the master's outputs as inputs (Q to R and $\overline{Q}$ to S), and the complement of the flip-flop's clock input. The slave's outputs are the flip-flop's outputs.
The main difference between the gated and non-gated SR-latch is that the gated latch is synchronous. Which means, that data is stored as soon as the data input is changed and a control input is given whereas the non-gated one stores data as soon as the data input is changed.

3.2.2 CML pre-scaler

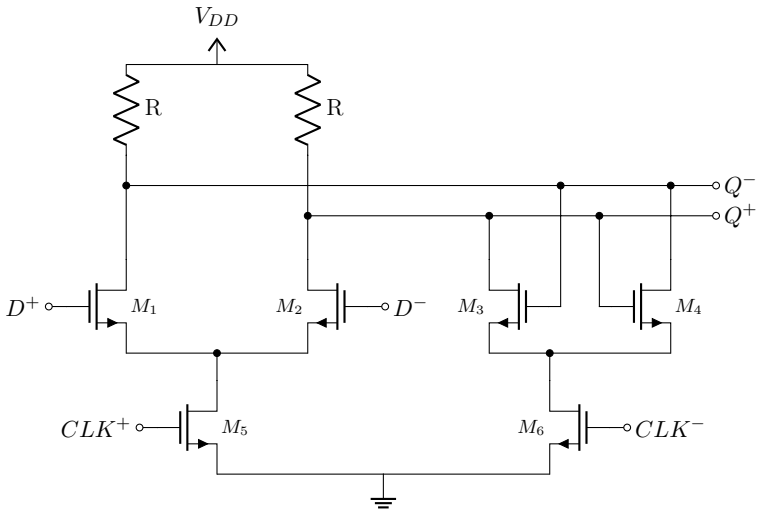


Figure 3.11: CML D-flipflop

Component	Size	
M1,2	w=4μ	l=20n
M3,4	w=4μ	l=20n
M5,6	w=6μ	l=20n
R	900Ω	

Table 3.3: transistor size of CML D-flipflop

The voltage swing is $I * R$, thus a relatively large R is used to provide a clear logic level to hold stage.

3.2.3 Programmable Divider

After the pre-scaler both designs uses a programmable divider. They are both based on cascaded divide-by-2/3 dividers and a divide-by-2/3/4 divider, but slightly differ from each other in order to obtain satisfactory division ratios for the entire chain. The CML is configured to divide by 2 and its following divider is designed to divide by 16/31, giving a total ratio of 32-62. For the 4/5 divider the programmable divider was designed to divide by 8/19, giving a total ratio of 32-95. A conceptual implementation of the programmable divider is shown in Figure 3.12. Naturally, the division ratio of the programmable divider connected with CML needs to be larger than for the one with the 4/5 ratio in order for the output frequency to reach the reference frequency.

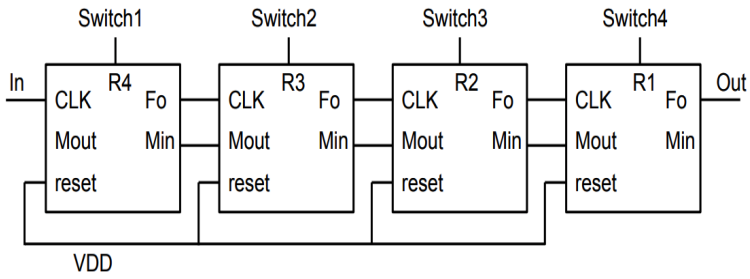


Figure 3.12: Programmable Divider

The divide-by-2/3 configuration consists a few D-latches and a couple of NAND and inverter gates, the divide-by-2/3/4 uses the same structure with some additional circuitry. Both are configured as shown in (Figure 3.13) and (Figure 3.14) respectively.
The control signal that decides the division ratio is p. When p is logic 1, the divide ratio is 3 and when p is a logic 0, divide ratio is 2. All transistors were minimized size in this circuit.

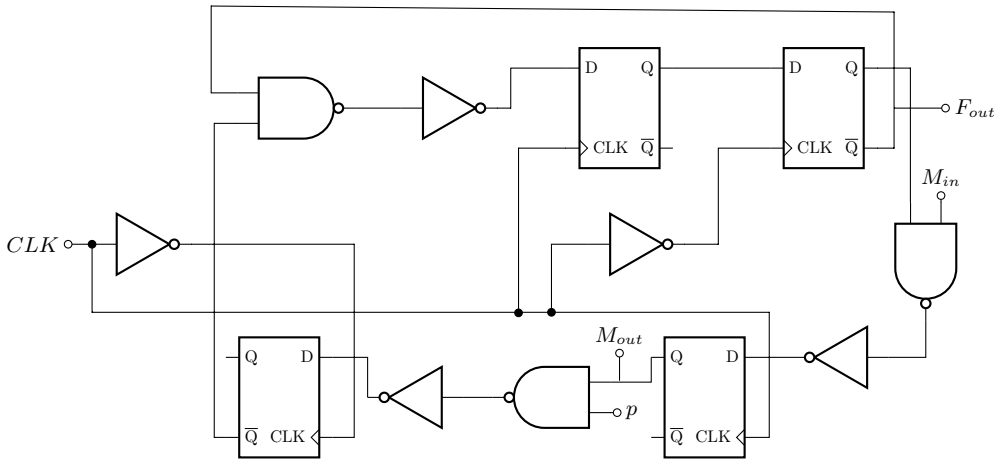


Figure 3.13: Divide by 2/3

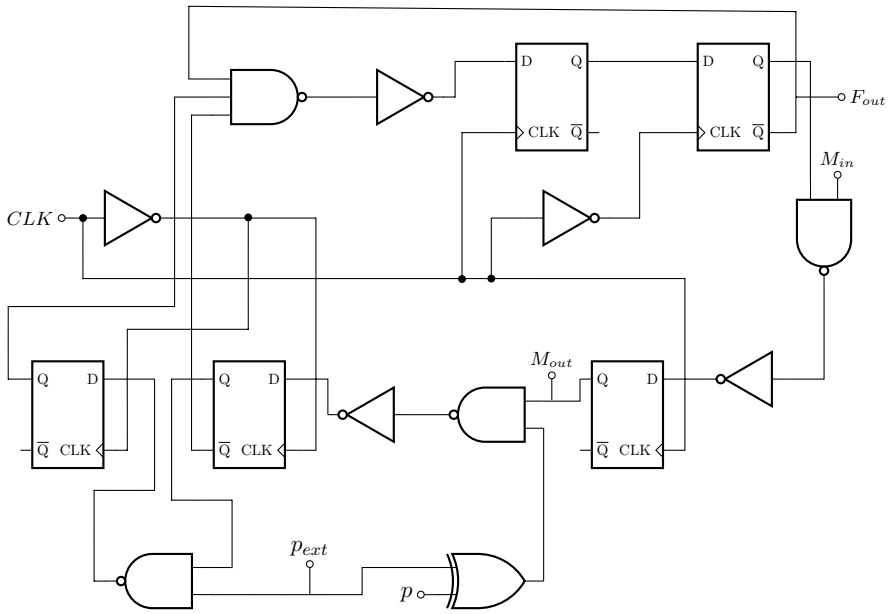


Figure 3.14: Divide by 2/3/4

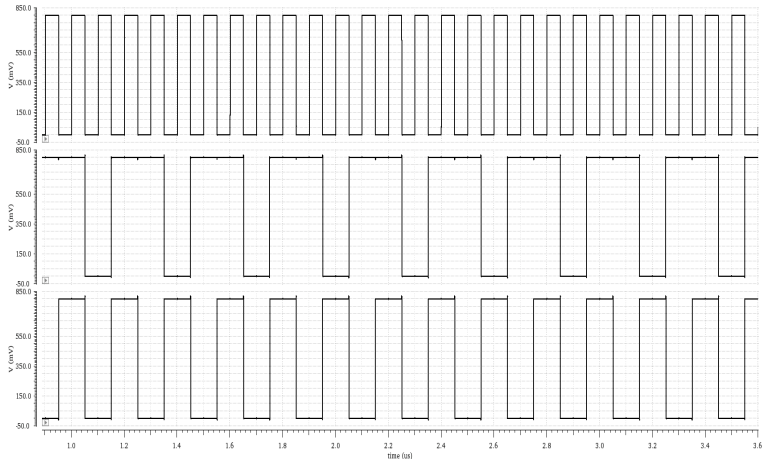


Figure 3.15: Clock input and 2 or 3 divider output

3.3 Phase Detector

The phase-frequency detector was designed by the conventional structure with two D flip-flops (NAND gate based) with added delay (two inverters) in the reset path. Minimum sized transistor were used for all NMOS:es while the PMOS:es were scaled slightly wider to obtain equal rise and fall time in the inverters.

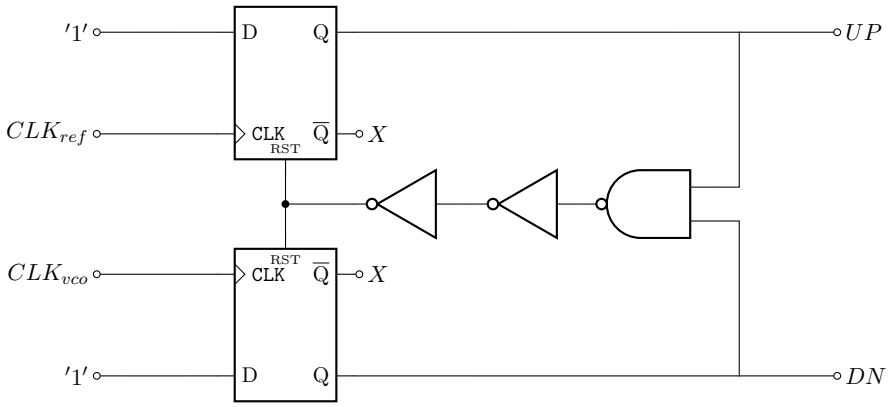


Figure 3.16: Phase-frequency detector

In the simulation, we feed two signals with the same frequency but different phase. The phase error varies from -2π to 2π.

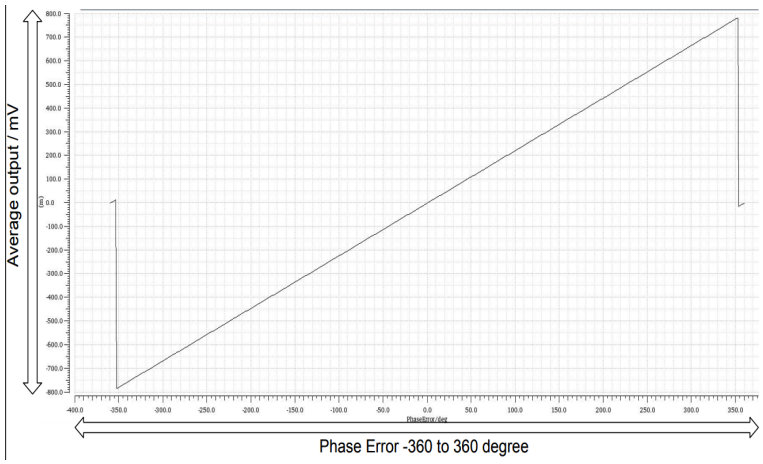


Figure 3.17: PFD input-output characteristic, -360° to 360°

The output is the average value of differential signals in one period. The result shows a good linearity characteristic from -353° to 353 °, 7° blind zone on each side. Further more, we need increase the number of sampling around zero delay to make sure there is no dead zone in the PFD. Thus we sweep the phase error from -0.5° to 0.5 ° with a step size of 0.01°.

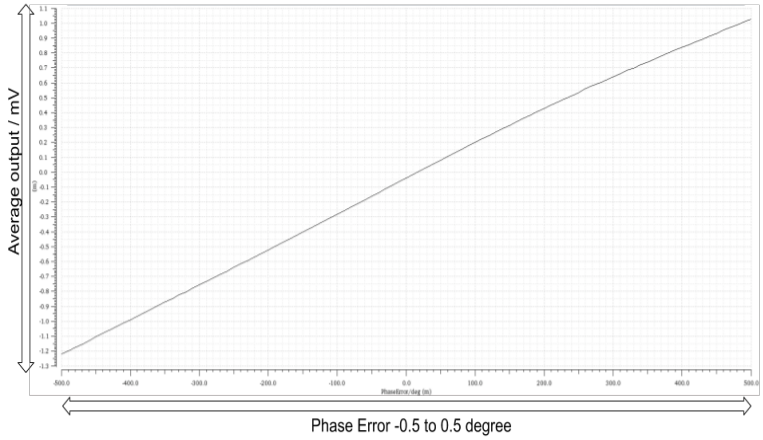


Figure 3.18: PFD input-output characteristic, -0.5° to 0.5°

According to the simulation results, when the output is zero, the phase error is about $0.015°(\frac{\pi}{12000})$. This might be caused by inaccurate clipping period which can be ignored.

3.4 Charge pump

As we know the ideal charge pump is supposed to have equal and constant charging and discharging currents and are not to be affected by the output voltage. However, in reality, charge pump current amplitude is affected by the output voltage a lot, especially when the output voltage is close to 0 or VDD. Many proposed topologies can be applied to reduce the common non-idealities. In this project various topologies has been examined, two of them has been designed to obtain the best possible outcome and they have been compared with the conventional structure of a charge pump.

3.4.1 Dual-compensated charge pump

This topology consists of two operational amplifiers that tracks the output voltages to force charging and discharging currents to be equal, see Figure 3.19.

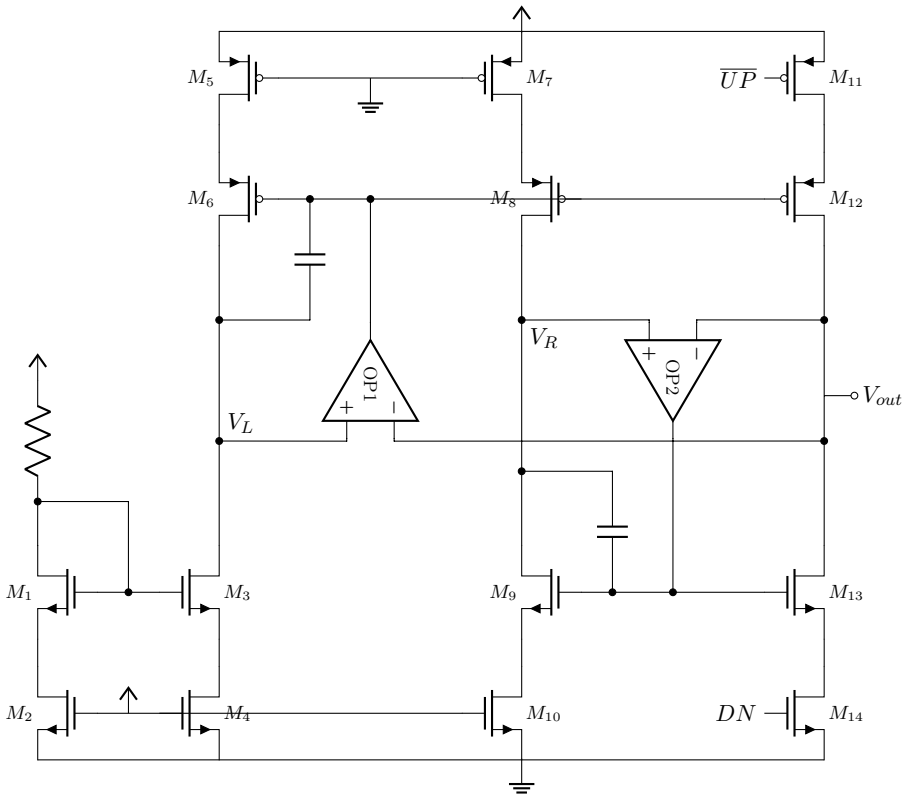


Figure 3.19: Dual-compensated charge pump

In the leftmost feedback loop V_L is controlled to track V_{out} by a compensation method so that I_{UP} equals I_{BIAS}. In the rightmost feedback loop V_R is controlled to track V_{out} to ensure that I_{DN} equals I_{UP}. By using this kind of tracking, satisfactory current matching is obtained without using the increased output resistance method[36]. The advantage of this is that a wide dynamic range is obtained. Another advantage with this technique is that it is not necessary to use long channel devices since the matching will be good anyways. Although, the length was considerably chosen to be longer than minimum to obtain almost constant pump current. The capacitors are there to ensure stability of the feedback loops. Stability was obtained practically by running DC stability simulations investing phase margin and gain margin until satisfied values was obtained. Both amplifiers are common two-stage CMOS op amps with an extra current mirror branch at the output to obtain lower gain. The lower gain amplifiers was necessary in order to obtain stability in each particular feedback system. It is not possible to use the same amplifiers since the feedback systems are slightly different. Therefore, sizing of the op amp transistor differ and so does the compensation capacitors. They were designed to obtain similar phase- and gain-margin.

Figure 3.20 shows results of DC simulation. A good mismatch from 0 to 650mV is

obtained. The gain is basically constant from 200mV to 600mV. Thus we should look back to check our VCO to make sure when the control voltage varies from 200mV to 600mV, the output frequency still has a good overlapping. Thereby, we can obtain a full output range.

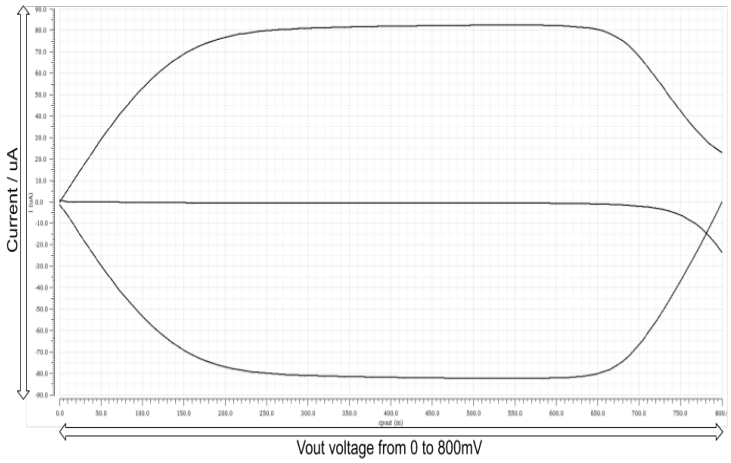
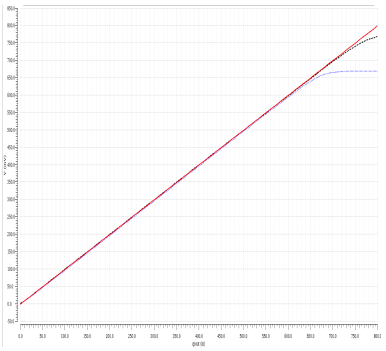
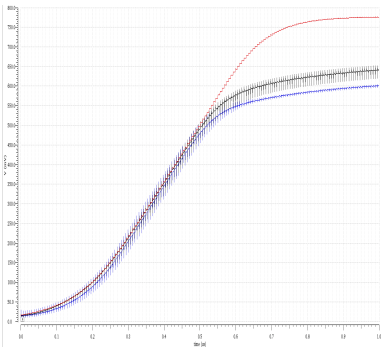


Figure 3.20: Dual-compensated CP characteristic

The following figures present the tracking process of two OP-AMPs both in DC simulation and transient simulation. V_L and V_R are compared with V_{out}(Red line). The tracking ability is more limited in transient simulation. Beyond 0-560mV, charge pump tracking ability slowly deteriorates.



(a) V_L,V_R and V_{out} in DC simulation



(b) V_L,V_R and V_{out} in transient simulation

Figure 3.21: Tracking process of Op-AMPs in Dual-compensated Charge Pump

Figure 3.22 shows the charging and discharging processes. A 3p capacitor is used as load. Sizing parameters are given in the Table 3.4.

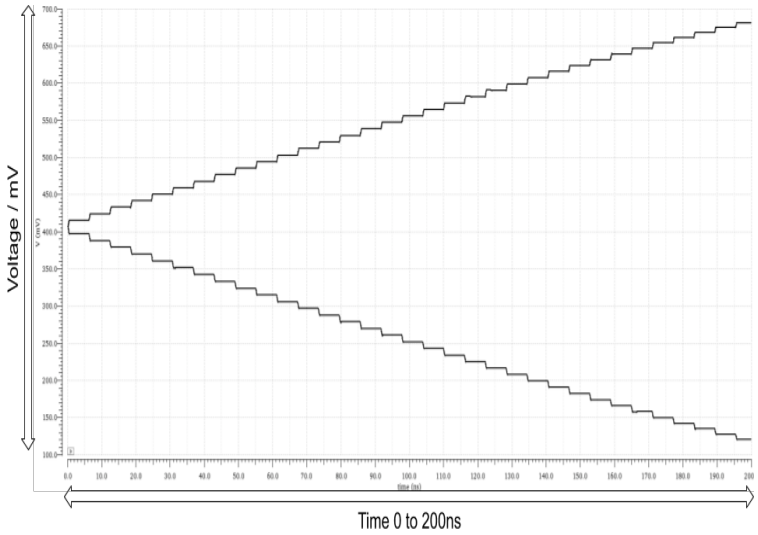


Figure 3.22: Dual-compensated Charging and discharging process

Transistor	Size
M2,4,10,14	w=80n, l=20n
M1,3,9,13	w=1μ, l=90n
M6,8,12	w=1μ, l=90n
M5,7,11	w=80n, l=20n

Table 3.4: Dual-compensated charge pump sizing

3.4.2 Gain-boosting cascode charge pump

The other topology that was implemented is the gain-boosting cascoding charge pump[37]. The main idea with this topology is to provide high output impedance with reduced channel length modulation effect and satisfactory current matching. This is obtained by using two low-voltage cascode current mirrors with embedded UP and DN switches, a gain-boosting loop consisting of a common-source amplifier and an NMOS-PMOS pair as reference current generators, see Figure 3.23.

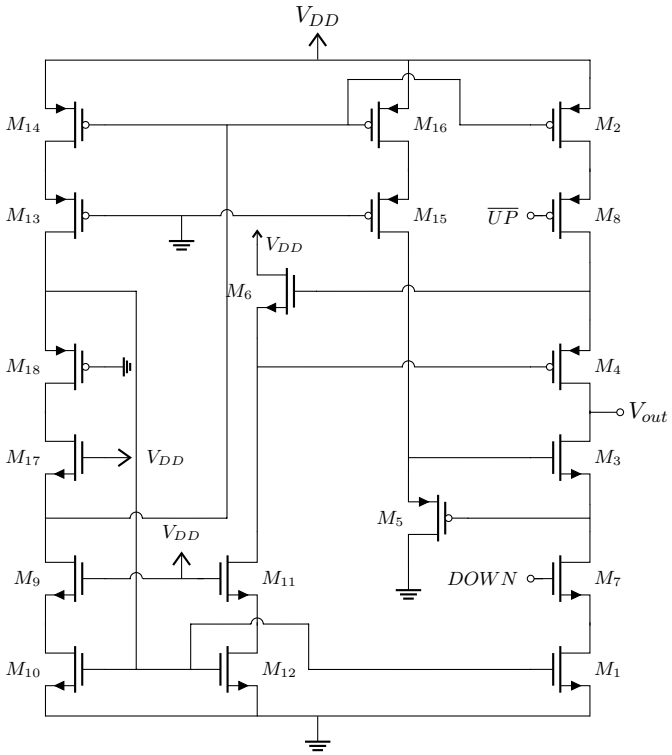


Figure 3.23: Cascoded gain-boosting charge pump

The low-voltage current mirror is used to copy the charge and discharge current from a single current source to ensure both currents are equal. This current mirror is chosen because it provides high output impedance and thus low channel length modulation. The biases for these mirrors are chosen to GND and VDD respectively since it provides better matching. They consist of transistors M9-M16 with M17 and M18 as their current reference. Usually when using the cascode current mirror structure one would connect the non-biasing gates to the drain of the reference transistor. For instance, the gates of M10 and M11 would be connected to the drain of M9. However, in this configuration the gates are instead connected to the source of M18. This offers higher gate voltage of M10 and M12 which allows a larger current to flow through. M5/M3 and M4/M6 constitute the gain-boosting loop where M5/M6 acts as a common-source amplifier. The output impedance R_{out} is given by

$$R_{out} \approx (g_{m7}r_{o7}g_{m3}r_{o3}r_{o1})(g_{m5}r_{o7})||(g_{m8}r_{o8}g_{m4}r_{o4}r_{o2})(g_{m6}r_{o6}) \tag{3.2}$$

Which results in a large value, hence long channel devices are not needed to achieve high output impedance.

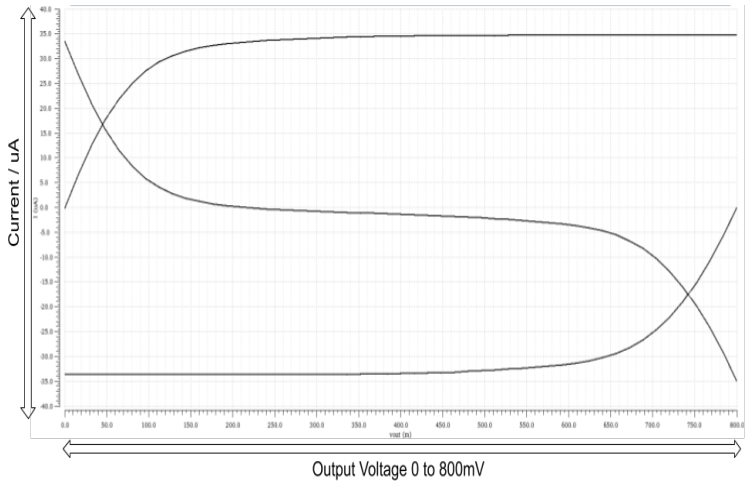


Figure 3.24: Gain boosting CP characteristic

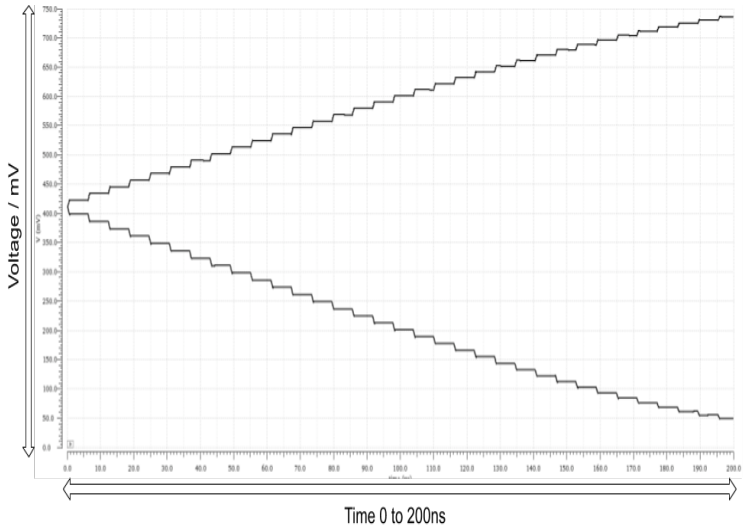


Figure 3.25: Gain boosting CP charging and discharging process

When a charge pump is poorly designed there is only one matched point at a certain output voltage that can may achieve mismatch be zero. If the PLL is locked at any other points instead of the zero mismatch point, the phase noise and jitter will increase and the degrade the performance. In order to achieve good current matching within the entire tuning range of the PLL a wide dynamic range is required in the charge pump.

In addition, DC performance is not exactly the same as transient performance. Gain and mismatch both vary a lot. Besides, it is impossible to observe how the

parasitic capacitance would influence the switching events and the overall performance. Usually the current is difficult to control. A regular, square wave like current would be ideal. But in reality, it is rather difficult to achieve a perfect square wave and the current may take different wave forms. When the PLL is locked, the pulse width of charge pump is usually a few tens of picoseconds. Thereby, in such a small time scale, fluctuation of current and slew rate becomes two important factors affecting the amount of charge moved in one period.

However, according to the simulation results, as long as satisfactory current matching is achieved when the loop is in its locked state, it does not matter that much if the shape of the current is non-square wave like.

As mentioned before, there are various architectures one might use when designing a charge pump. All of them, proposing different solutions to reduce the non-ideal behavior. Except the ones presented here, i.e., the dual compensated and gain-boosting topologies, a similar architecture as the one with compensating amplifiers that seems promising was found, but not implemented. It uses a current conveyor (CCII+) as a compensation method to match the charge and discharge currents. This application of CCII+ provides a new promising method to decrease the mismatch current[38].

3.5 Loop Filter

The loop filter design is based on the loop filter recipe mentioned above. A script is designed in Matlab to calculate the RC paramenters used in loop filter. The parameters used in our project are listed as in Table 3.5.

Parameter	Design A	Design B
Phase margin	48°	52°
CP Current	38μA	90μA
VCO Gain	939MHz/V	640MHz/V
Divider ratio	60	60
Crossing Frequency	800KHz	800KHz
τ_x/τ_z	0.03	0.05

Table 3.5: Loop filter design considerations

Parameter	Design A	Design B
C_0	52pF	93pF
R_0	9.9KΩ	6.4KΩ
C_A	4.5pF	5.86pF
R_x	3.4KΩ	3.04KΩ
C_x	4.5pF	5.86pF

Table 3.6: Loop filter parameters

One thing should be noticed is that the order of Loop Filter dominates the dynamic character of closed loop. First order loop filter can track the frequency till they are equal,however, the static phase error exists. Second order loop filter can track the phase error till zero(without non idealists). Third order loop filter can track the acceleration Phase error. To use which kind of loop filter is decided by the purpose the PLL. However, these principles are solid only when the Phase error is small and loop is linear, where the approximation $sin(\theta) \approx \theta$ is available.

Chapter 4

Results

In this chapter, the simulation results, measurement results of Design A and B are presented. In the end of the chapter in Table 4.2 a summary of all the results is presented. The PLL is simulated in Cadence Virtuoso with transient simulation includes contribution of noise from all components.

4.1 Simulation Result

4.1.1 VCO and Divider

In Design A, reference frequency is 163.8MHz, the VCO output frequency is 9.828GHz. After CML divider, frequency is scaled down to 4.914GHz. After Programmable divider, which is set to a ratio of 30, the frequency is 163.8MHz.

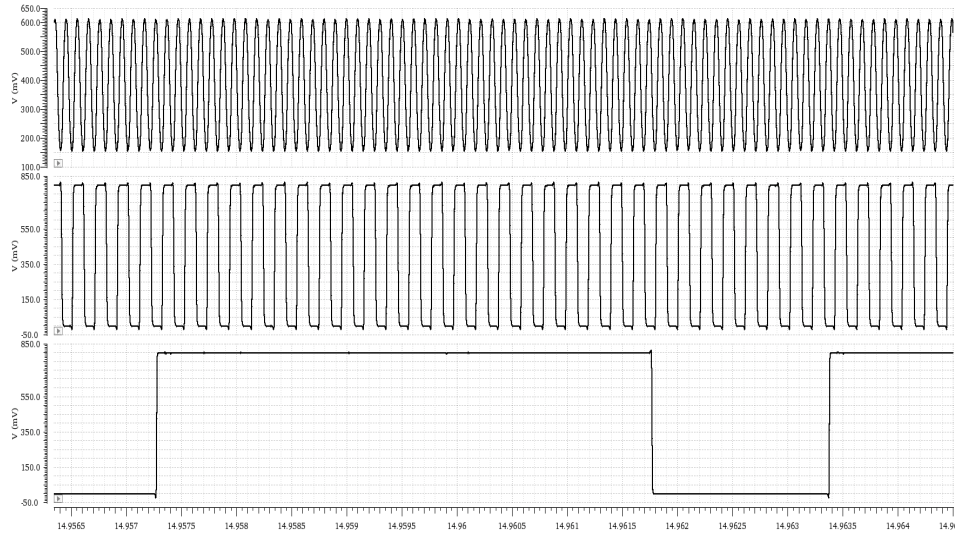


Figure 4.1: VCO output, CML divider output, Programmable divider output

Design B uses reference frequency of 163.84MHz, VCO output frequency is 9.831GHz. After pre-scaler, the frequency is scaled down by a factor of 5 to 1.966GHz. Then the programmable divider is set to divide by 12, to obtain a frequency of 163.85MHz. The waveforms are shown in Figure (4.2). Note that these results only show one of many possible division ratios.

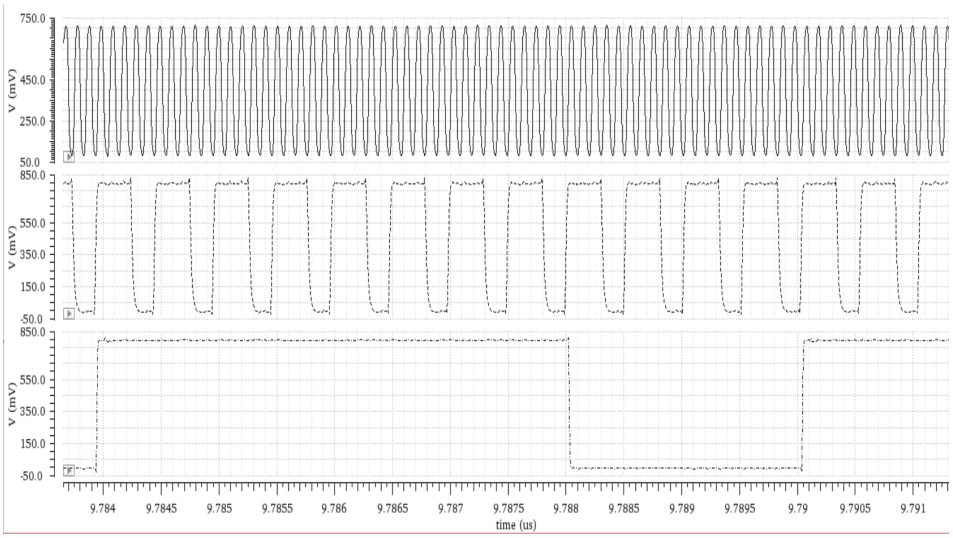


Figure 4.2: VCO output, Dual modulus divider output, Programmable divider output

4.1.2 PFD and Charge Pump

The following two figures are the input and output signals of PFD in two cases, rising edge of ref is ahead of VCO or behind VCO.

Cascoded gain-boosting CP is employed in Design A, and Dual-compensated CP is employed by Design B. Both A and B share the same PFD.

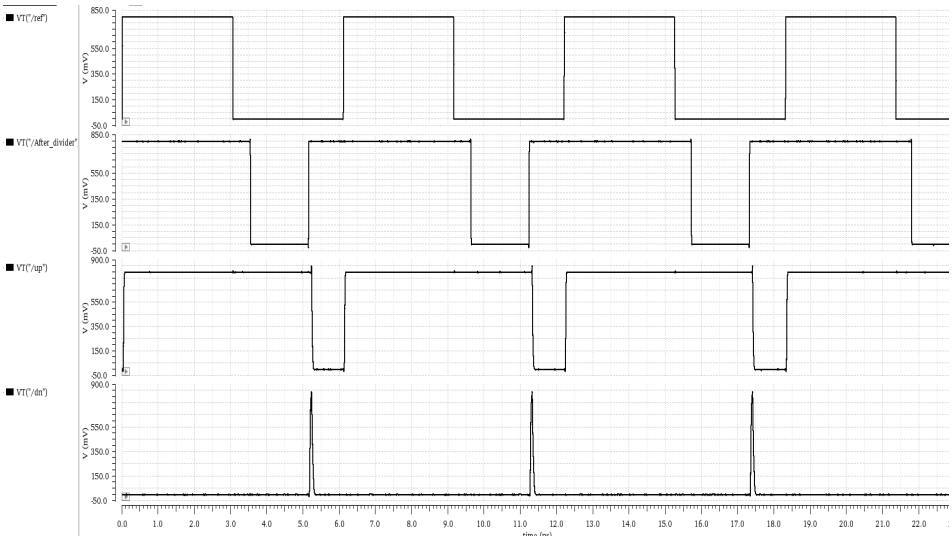


Figure 4.3: Reference is ahead of VCO

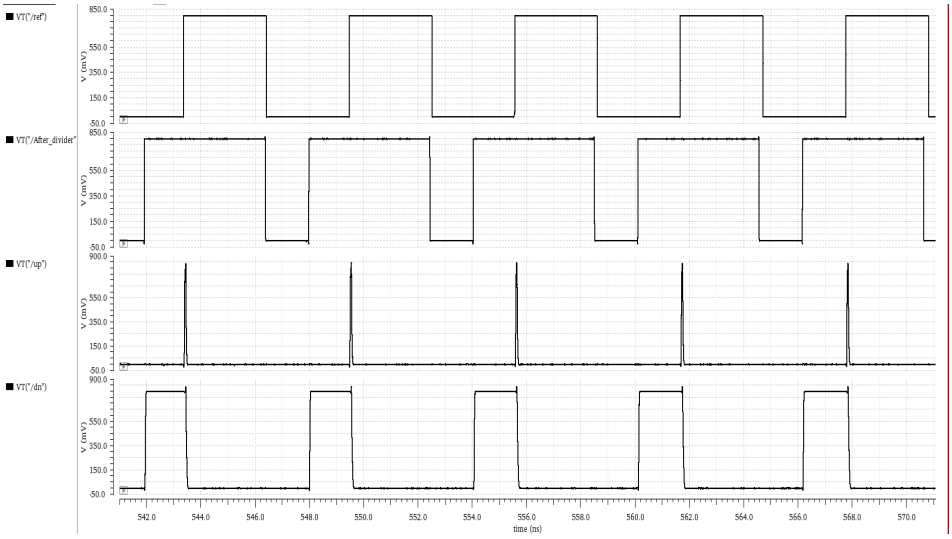


Figure 4.4: VCO is ahead of Reference

This is the output of Charge Pump, when the PLL is locked, found in Figures 4.5 and 4.6.

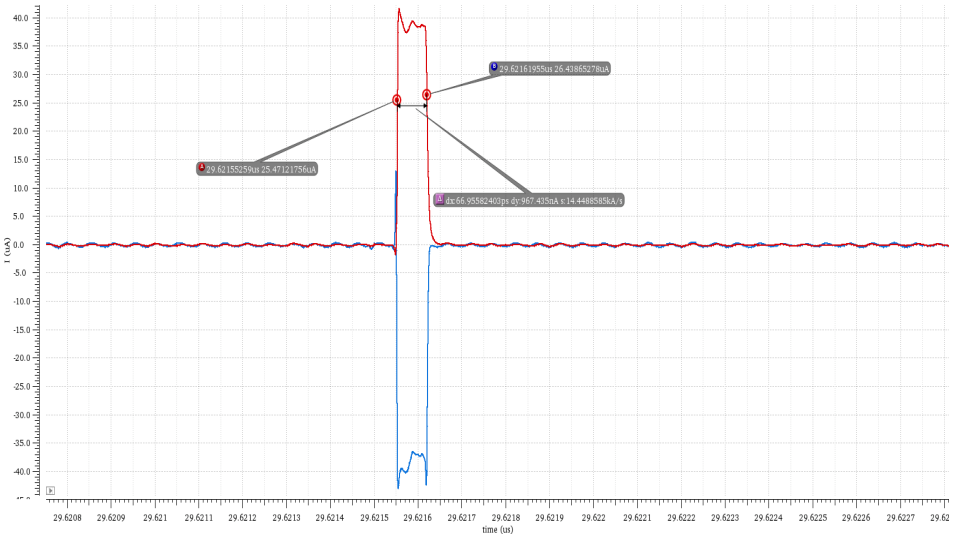


Figure 4.5: Charge Pump output of Design A

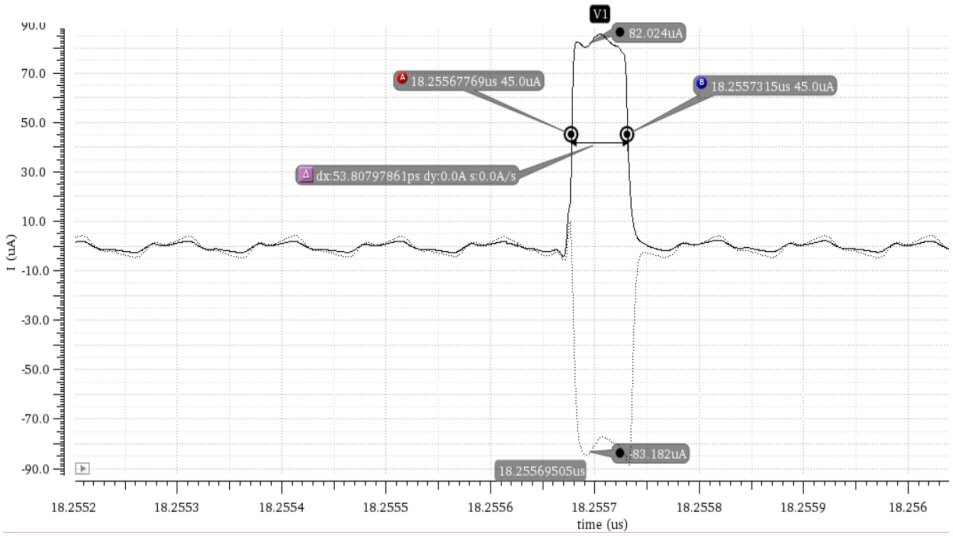


Figure 4.6: Charge Pump output of Design B

4.1.3 Loop filter

Design A is locked at 498mV, Figure 4.7, and Design B is locked at 536mV, Figure 4.8.

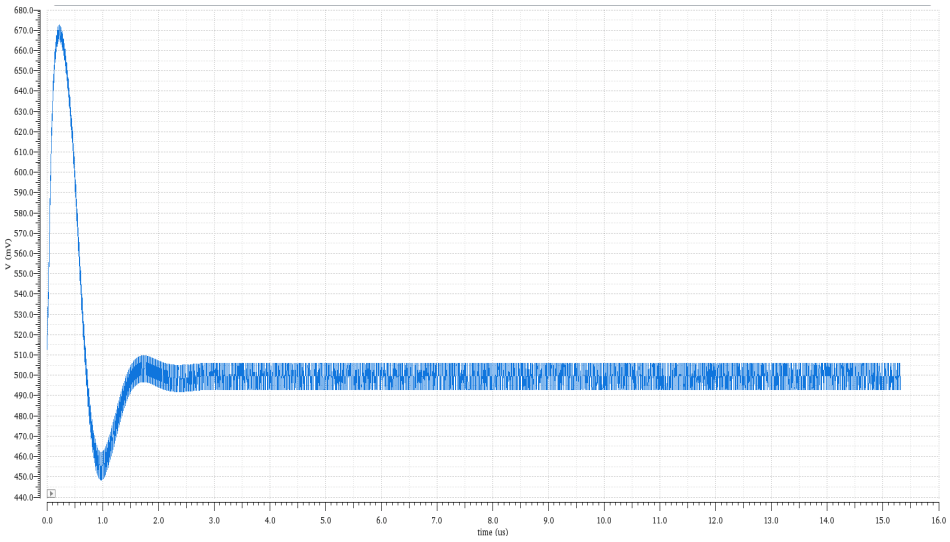


Figure 4.7: Control signal of A

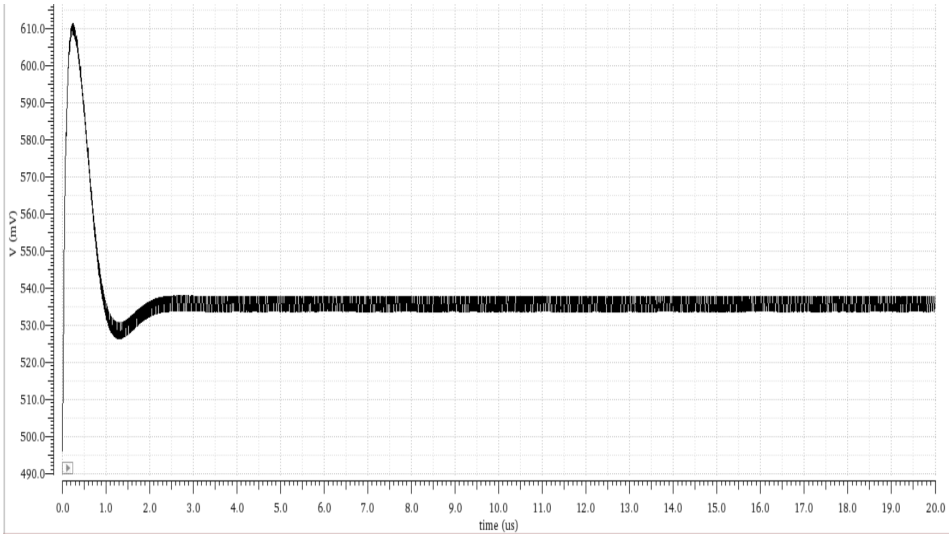


Figure 4.8: Control signal of B

4.1.4 Transient Phase Noise

After including the noise contributed from all components, we plot the transient Phase Noise at the output of VCO, as shown in Figures 4.9 and 4.10.

For Design A, PN at 1MHz is -104dBc/Hz, at 10MHz is -139dBc/Hz.

For Design B, PN at 1MHz is -95dBc/Hz, at 10MHz is -133dBc/Hz.

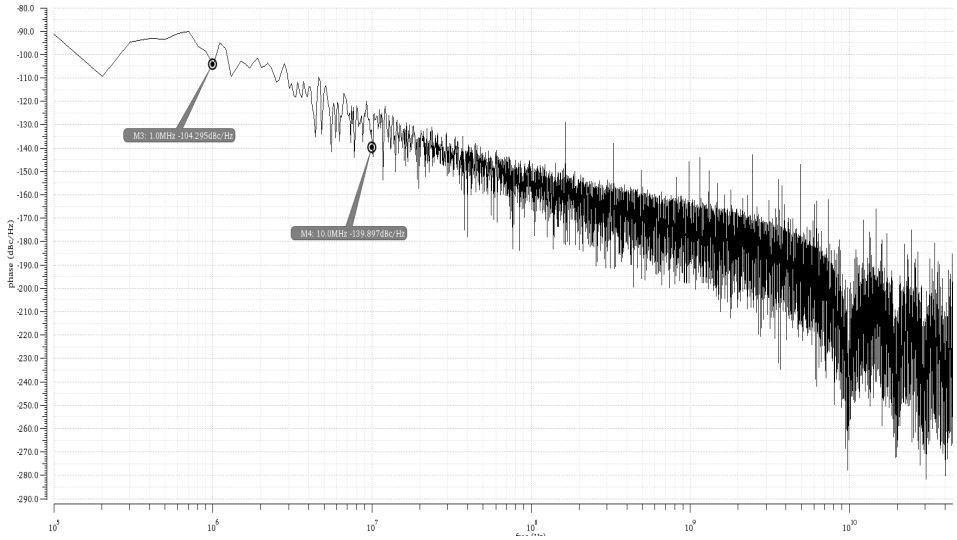


Figure 4.9: Phase Noise of PLL - Design A

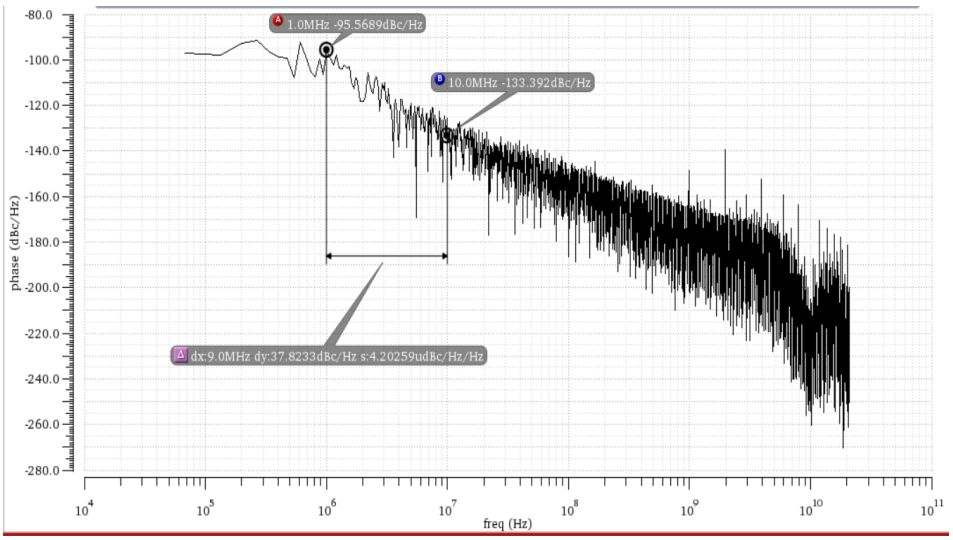


Figure 4.10: Phase Noise of PLL - Design B

4.1.5 Jitter Measurement

Using the eye diagram measurement tool in Cadence, we can get the eye diagram measurement summary. Random jitter is 38fs in Design A and 68fs in Design B. Deterministic jitter is 1.86ps in Design A and 835fs in Design B. For Design A the measurement uses the data from 5μs to 30μs(245700 cycles), for Design B the data is measured from 5μs to 20μs(147510 cycles).

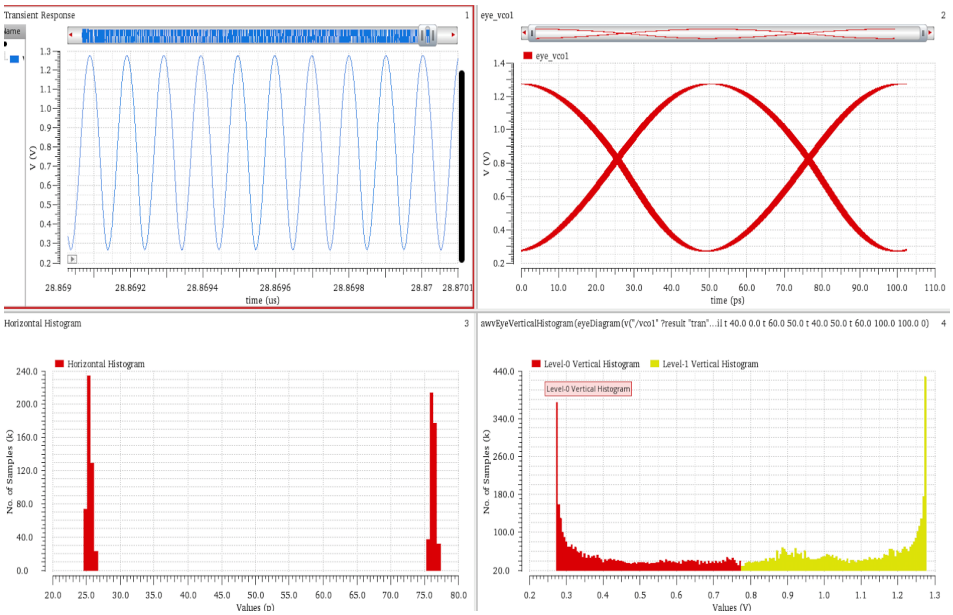


Figure 4.11: Eye diagram and jitter measurement of Design A

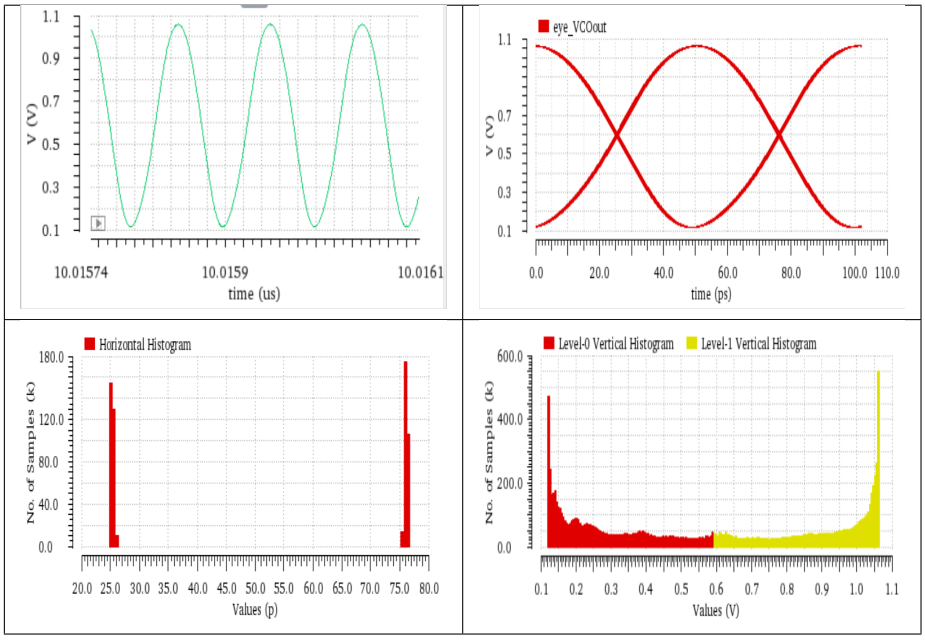


Figure 4.12: Eye diagram and jitter measurement of Design B

4.1.6 Frequency Error and Phase Error

Frequency Error

We define the frequency error as

$$F_{error} = average\{(F_{Div} - F_{ref}) * 60\} \tag{4.1}$$

when the PLL is stable. F_{Div} is the output frequency of divider.

Figures 4.13 and 4.14 present two forms of frequency error. The upper figure is calculated by

$$F = (F_{Div} - F_{ref}) * 60 \tag{4.2}$$

The bottom one is absolute error in log scale.

$$F = log\Big\{abs\big((F_{Div} - F_{ref}) * 60\big)\Big\} \tag{4.3}$$

Static Phase Error

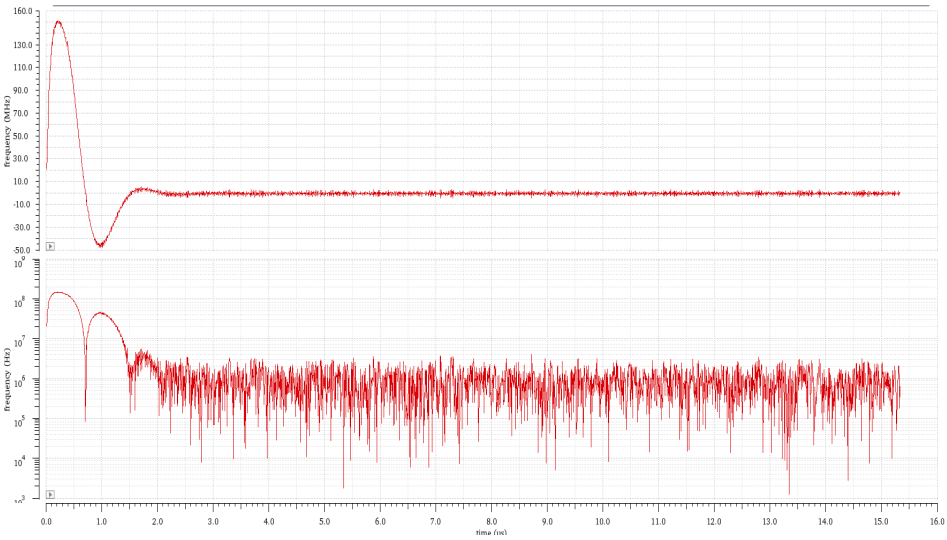


Figure 4.13: Frequency Error of Design A

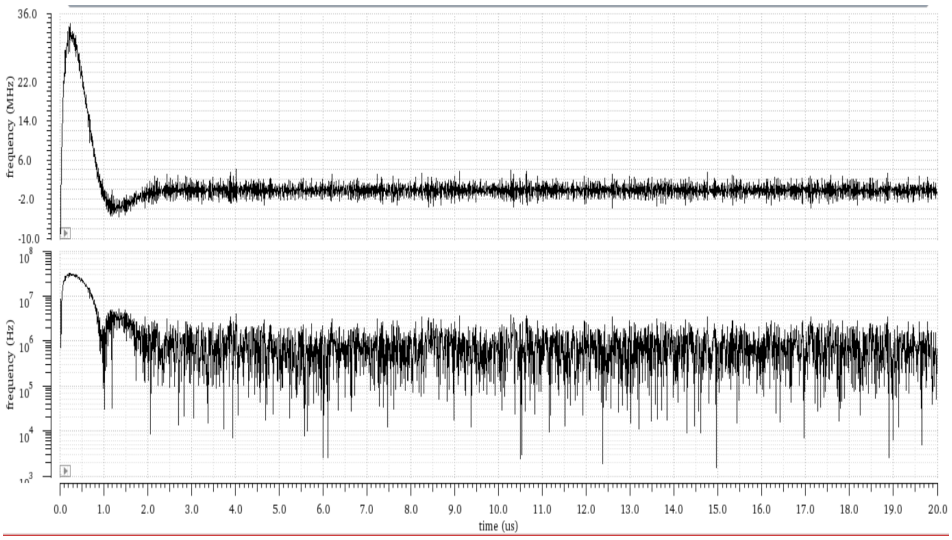


Figure 4.14: Frequency Error of Design B

The fluctuation is caused by noise and the sampling simulation method used in Cadence.

Phase Error can be observed from the Phase difference between Programmable divider output and Reference signal, which are the input signals of PFD. This error is related to the slew rate and mismatch of CP. In an ideal fourth order PLL, there should be no static phase error given enough simulation time.

Figures 4.15 and 4.16 show the static phase error when both PLLs are locked. Input signals of PFD are compared together. The linear one is an ideal Vpulse with a rising time of 10ps. The other one is the output of programmable divider. The delay measured in figure is 150fs and 446fs respectively, however, due to jitter, this value varies slightly even the loop is locked.

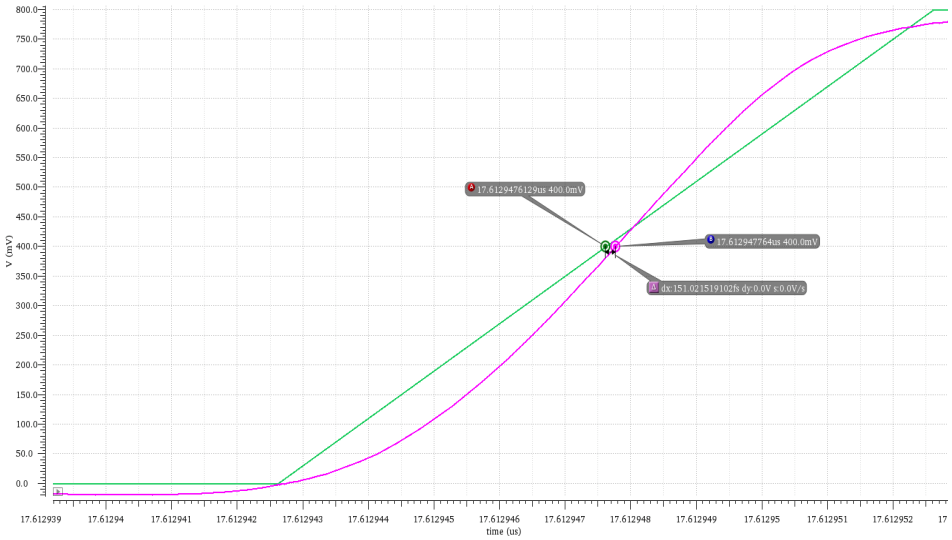


Figure 4.15: Static phase error of Design A

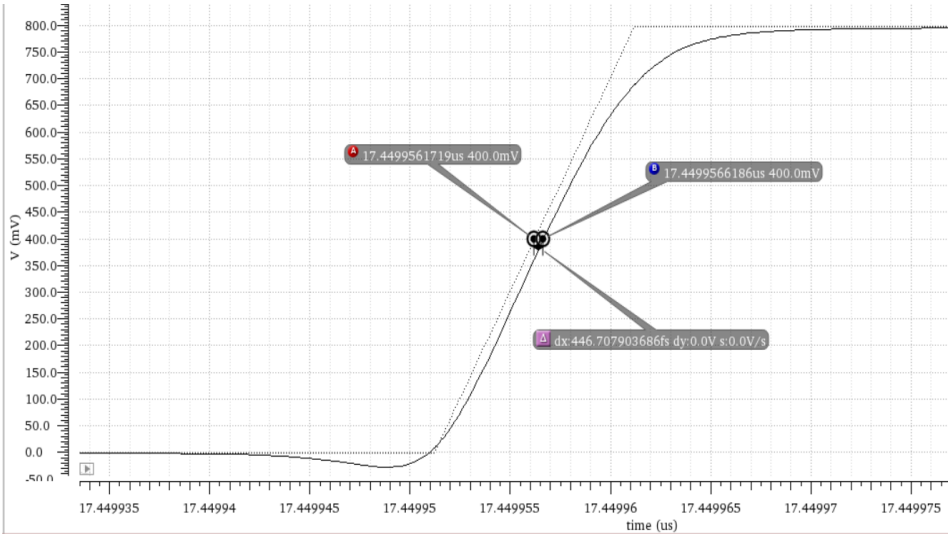


Figure 4.16: Static phase error of Design B

4.1.7 Reference spur

Reference spur level is measured by spectrum analysing tools. In Figure 4.17, the center peak level is -6dB, the reference spurs level is -86dB. A -80dBc reference spur level is achieved. In Design B, the reference spur level is compressed even lower, which reaches -98dBc, Figure 4.18. Thus, there is no such clear and visible side peaks at the frequencies of reference spurs.

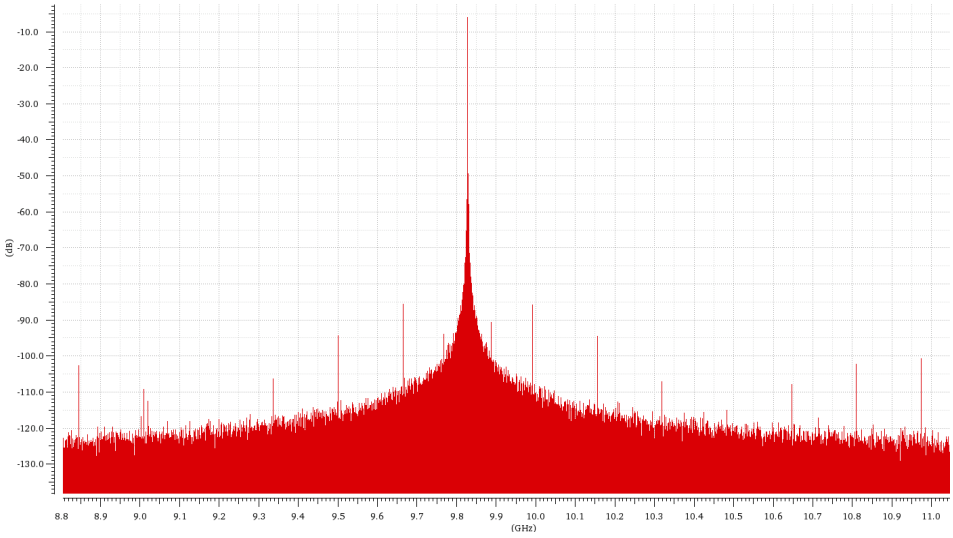


Figure 4.17: Reference spur of Design A

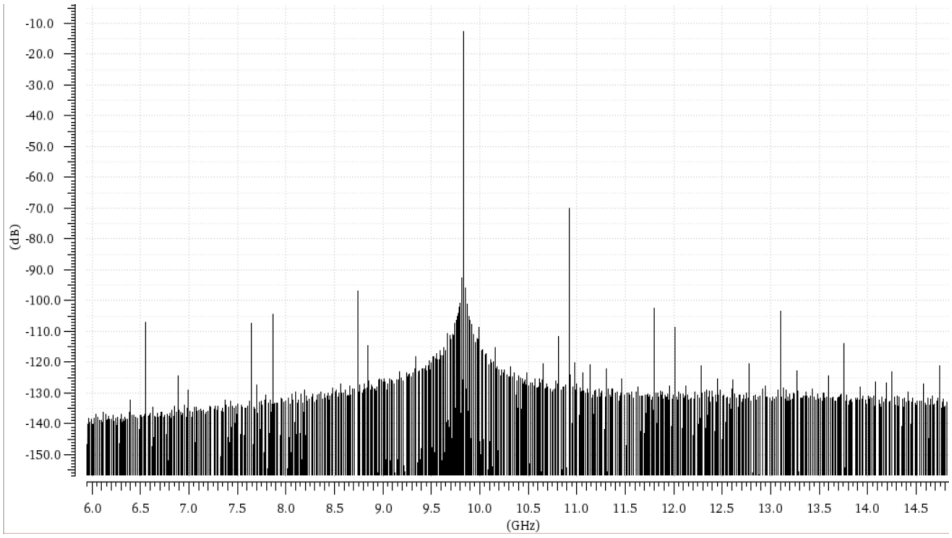


Figure 4.18: Reference spur of Design B

4.1.8 Power Consumption

In Table 4.1 the power consumption of each component used in both designs is shown. As we can see, the main difference between them is the consumption of the VCO. The reason of this is that Design A has a higher gain than Design B, which naturally requires more power. Another high power consumer found in Design A is the pre-scaler which uses the CML topology whereas the pre-scaler of Design B

is a simple dual module divider, which consumes remarkably less power due to its simple digital circuitry.

Component	Design A	Design B
VCO	8.626m	4.817m
Voltage Converter	60μ	45.94
Prescaler	1.28m	50.53μ
Programmable Divider	58.4μ	39.47μ
PFD	1.6μ	1,731μ
Charge Pump	197.6μ	204.3μ
Total power	10.22m	5.16m

Table 4.1: Power consumption (W)

4.2 Chapter Summary

The simulation and measurement results are summarized in Table 4.2. Considering power consumption, Design B would be the clear choice. Otherwise, both structures are quite similar considering the parameters presented in the table, except from the phase noise which is a few dBc lower in Design A.

Parameter	Design A	Design B
Random jitter	38fs	68fs
Deterministic jitter	1.86ps	835fs
Reference spur	-80dB	-98db
Power consumption	10.22mW	5.16mW
Locking time	3.5μ	2.8μ
Static phase error	150fs	446fs
Phase noise @1MHz	-104dBc/Hz	-95dBc/Hz

Table 4.2: PLL system results summarized

Chapter 5

Conclusion

This report presents a design process of Integer-N CP-PLL circuits in the 22nm CMOS technology process to be used for 5G-NR applications. Various architectures of each component were analyzed for use in the final designs. The circuits were simulated and measured in the Cadence Virtuoso environment and two matlab scripts were used to assist calculations considering loop filter and closed loop stability.

Two different designs of a low phase noise PLL with over 20% tuning range were achieved. Random jitters are 38fs and 68fs, reference spur level are -80dBc and -98dBc. Design A and B examine different topologies concerning charge pump, pre-scaler and gain of VCO. The VCO and pre-scaler used in Design B consumes much less power compared with A, which is a great advantage when applied to low power applications.

Some issues were faced in the simulation of closed loop PLL. The main problem is that we could hardly cover all working frequencies when we measure performance parameters such as phase noise and jitter. A 20μs transient simulation (conservative error preset) took 103 hours to complete. As for PSS simulation, it is even harder to obtain a convergence for PLL. Tens of hours, or even days, are needed to obtain an accurate result at a fixed working frequency without any dynamic parameter. In addition, the memory space of the work environment was limited as well. Thereby, dynamic simulations were not carried out in this project, such as changing the control bits of the programmable divider or VCO, or changing the reference frequency. The overall performance would also vary in different cases.

Through all our simulation results, the lowest random jitter (about 20fs) was achieved when the cascoded gain-boosting charge pump was employed and its zero current mismatch point was at the control voltage by which the system was locked. However, at all other points the performance would be tremendously worse. Thus, showing the importance of a wide dynamic range.

If we take a glance toward some future work, there are some performance measures that might be improved. For instance, the VCO power consumption in both design can be considerably optimized, especially in Design A. Similar phase noise

performance could be achieved with only 1/10 power consumption. Naturally, depending on different classes of VCO and processes. Also, control systems should be implemented for both designs, that sets the tuning frequency by tracking the control voltage and adjusting the capacitive switches accordingly. A similar control system should be applied to the programmable divider. Naturally, all sorts of optimizations could be made to almost all the components in the system.

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Appendix A

Extended material

A.1 MatLab Code

A.1.1 Loop filter script

```
%PM=phase margin deg,Kvco= vco gain Hz/V, CP=charge pump
    current A
%Divided by N(integer),crossfreq=crossing frequency Hz,

% Example
% 60deg phase margin
% Kvco = 1120MHz/V
% Charge pump curent is 70uA;
% frequency divided by 60;
% crossing frequency of the filter if 2MHz,

% Type
% Then Fill the ratio of RxCx/R0C0,usually from 0.01 to
    0.1.
% If we fill 0.1
% Then press enter
% Then result comes out
% R0= 1.036101e+04
% C0= 2.866393e-11
% CA= 1.108581e-12
% CX= 1.108581e-12
% RX= 2.678984e+04

function loopfilter(PM,Kvco,CP,N,crossfreq)
syms x;
b=solve(atan(sqrt(x+1))-atan(1/(sqrt(x+1)))-(PM/180)*pi);
R0C0=sqrt(b+1)/(2*pi*crossfreq);
T1=R0C0;
C0=CP*Kvco*2*pi*b/(2*pi*N*sqrt(b+1)*(2*pi*crossfreq)^2);
```

```
R0=R0C0/C0;
r = input('Fill the ratio of RxCx/R0C0,usually from 0.01 to
    0.1. \nThen press enter \n');
T2=r*R0C0;
syms CX;
CA=solve(C0-2*CX*b,CX);
CX=CA;
RX=T2/CX;
%format control
fprintf('R0= %e \n',double(R0));
fprintf('C0= %e \n',double(C0));
fprintf('CA= %e \n',double(CA));
fprintf('CX= %e \n',double(CX));
fprintf('RX= %e \n',double(RX));
end
```

A.1.2 Loop stability measures

```
clear all;
close all;
clc

%Loop Filter
%designed for third order loop filter /fourth order PLL

%-----------------R3-------
%|          |              |
%|          |              |-----Vout
%R1         |              |
%|         C2              |
%|          |              C3
%C1         |              |
%|          |              |
%-----------------GND------

%Change the parameters, then run the script.
%capacitor unit F, Resistor unit ohm.
C1=52.28e-12
R1=9.9e3
C2=4.5e-12
R3=3.44e3
C3=4.5e-12
%-------------
%unit A
Icp=39e-6
%unit rad/V
Kvco=939e6*2*pi
%divider ratio, no unit
```

```
31 N=60
32 %----------------
33 zero=[Icp*Kvco*C1*R1, Icp*Kvco];
34 pole=[2*pi*N*C1*C2*C3*R1*R3, 2*pi*N*(C1*C2*R1) + 2*pi*N*(C1
       *C3*R3) + 2*pi*N*(C2*C3*R3) + 2*pi*N*(C1*C3*R1), 2*pi*N
       *(C1+C2+C3) ,0 ,0];
35
36 closedloop=tf(zero, pole)
37 bode(closedloop)
```

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