Design of Two 28 GHz Doherty Power Amplifier Topologies with Vertical In(Ga)As Nanowire Transistors

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Abstract

In this Master's thesis, two different 28 GHz Doherty power amplifiers (DPAs) are designed, for high power added efficiency (PAE), in the common source (CS) and cascoded topology respectively. The results are analyzed and compared between the two approaches. The DPAs are designed using AWR design environment with virtual source (VS) models of In(Ga)As nanowire transistors and 50 nm gate length. The CS topology achieves a simulated gain of 9.9 dB, a saturated output power (P_{sat}) of 19.7 dBm, and 3-dB bandwidth (BW_{3dB}) from 25.5 to 31.1 GHz. The PAE at 6-dB power back-off (PBO) and PAE at 9-dB PBO are 21.2 % and 15.5 %, respectively. Simulations with a 64-QAM signal were performed. For the highest allowed error vector magnitude, EVM = 5.5 %, output power of 14.8 dBm and a PAE of 23.3 % was achieved. The cascoded topology achieves a gain of 10.6 dBm, P_{sat} of 21.2 dBm and a BW_{3dB} from 26.0 to 30.3 GHz. The PAE at 6-dB PBO and 9-dB PBO is 21.1 % and 15.9 %, respectively. For the highest allowed EVM, output power of 17.1 dBm and a PAE of 24.5% was achieved.

Popular Science Summary

Today more and more devices are connected to the internet, not only cellphones and computers but also your fridge and car stay online around the clock. This may seem unnecessary, however, this constant connectivity allows for better diagnostics and is now being introduced in fundamental functions of society. The internet-of-things, or IoT for short, changes the way we consume data. For home electronics this may only be quality of life improvements, but when looking at work spaces or city planning, IoT could give great results. For example, hospitals could monitor all patients continuously, resulting in faster response in the case of emergencies. Naturally this introduction of IoT leads to a higher demand on the cellular network, as more data is being transferred.

The current 4G network will not be able to support this increase in data rate, so a new generation is being introduced, 5G. This allows for more data to be transferred since, it uses higher frequencies with wavelengths in the range of millimeters, the so called mmWave frequencies. Cellular networks are partly modulated using different transmitted signal powers. 5G uses this to greater extents, which means the hardware must be power efficient over a broad range of power levels. Furthermore, increasing frequencies, while modulating the 5G signal, presents new challenges for power consumption regarding hardware. The most power consuming components in transmitters are the power amplifiers. The efficiency of power amplifiers has been a problem for signal transmission since its infancy. One way to solve this is the now well established Doherty Power amplifier (DPA), which was introduced in 1936. This way of designing power amplifiers is still used today, albeit with modern transistors instead of vacuum tubes, as it increases the efficiency during operation by combining two amplifiers working in parallel designed for high efficiency at different power levels. This comes at the price of a reduced usable frequency span and increased complexity, which may limit the performance.

However, for this technique to be usable for 5G, the two amplifiers comprising the DPA needs to be well suited for high frequency operation. The maximum performance of an amplifier is very much limited by the performance of its transistors. Conventional transistors are reaching their performance limits for high frequency transmission, so new transistor technologies are being suggested

to further push the performance of power amplifiers. One of these transistor technologies is vertical nanowire transistors, which show excellent performance while also being area efficient.

The aim of this thesis is to design two different Doherty power amplifier schematics using nanowire transistors for 5G signal transmission, to evaluate the possible use of the technology for 5G.

Acknowledgements

We would like to express our gratitude towards our supervisor Tobias Tired at NordAmps for his expertise and willingness to explain various concepts throughout the work on this thesis. Also to our supervisor Erik Lind at LTH for his expertise and input on the thesis. Finally we want to thank NordAmps, for the opportunity to write out Master's thesis with them.

Acronyms

5G	5th generation cellular network standard
AWR	Applied Wave Research
BW	Bandwidth
CD	Common Drain
CG	Common Gate
CS	Common Source
DIBL	Drain-induced barrier lowering
DPA	Doherty Power Amplifier
GAA	Gate all-around
IMD	Intermodulation distortion
IoT	Internet of Things
MOSFET	Metal-oxide-semiconductor field-effect-transistor
OFDM	Orthogonal frequency division multiplexing
PA	Power Amplifier
PAE	Power added efficiency
PAPR	Peak to Average Power Ratio
PBO	Power back-off
PLL	Phase locked loop
QAM	Quadrature Amplitude Modulation
QW	Quarter-wave
RF	Radio frequency
RRC	Root raised cosine
SCE	Short Channel Effect
VCO	Voltage controlled oscillator
VS	Virtual Source

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Chapter 1
Introduction

1.1 Background

With the ever growing field of wireless communication, there is a steady increase in demand for faster data rates. The reason behind this is not only the increase in everyday cellular data usage, but also the Internet-of-Things (IoT) and interconnected smart city development. Digital platforms are already found everywhere and future development will set higher bars on not only data speeds but also robustness and latency [1], [2].

The need for higher data speeds can be met using new modulation techniques and higher frequency bands which is why the push from 4G to 5G networks is greater than ever. However, the transition will not be possible without adequate technology supporting it. 5G introduces new requirements on all surrounding hardware that needs to be both high performing and robust. The focus of this thesis is the power amplifier (PA) design for the transmitter, which needs to meet the requirements for 5G picocells and handheld user equipment [3].

Modulation schemes for 5G include 64-QAM and 256 QAM [4], which have a peak to average power ratio (PAPR) of about 9-10 dB. The high PAPR will decrease the efficiency of the power amplifiers, since, generally PAs are designed to be the most efficient at peak output power. Doherty power amplifiers (DPAs) are a well established topology used to increase efficiency of PAs at a lower output power. The Doherty amplifier is therefore suitable for signals with advanced modulation schemes [5]. The power amplifier is one of the most power consuming components in the radio communication signal chain [6]. It is therefore important to have high efficiency amplifiers, to increase the battery life of mobile devices, and also to reduce the environmental impact from high power consumption as well as heat dissipation in basestations.

1.2 Thesis Contributions

This thesis explores the use and performance of In(Ga)As nanowire transistors for high frequency Doherty power amplifiers (DPA) in different topologies. The topologies chosen are the widely used differential common source and cascoded

architectures.

Physical scaling of MOSFET gate length have historically been the drive for the fast improvements in integrated electronics. Scaled devices usually lead to short channel effects, which reduce the efficiency and lowers the operational frequency. Innovative transistor architectures and the shift to III-V materials will improve the electrostatic control [7]. InGaAs nanowire transistors are a promising example of such a novel transistor architecture. The vertical nanowire geometry allows for gate all around (GAA) structures which improves electrostatics. The III-V materials offer high electron mobility and good integration options on silicon [7].

In this thesis, two DPAs are designed to meet the current specifications of the 5G n257-band with center frequency at 28 GHz [3]. The focus is on the efficiency of the amplifier, while still meeting the other requirements such as output power, linearity and bandwidth (BW) of the PA. Comparisons between Doherty amplifier designs of differential common source (CS) and cascoded topologies were made. The goal of the thesis has been to provide amplifier schematics that may be manufactured and verified in a small scale. This has been taken into account in the design of the schematic. The design has therefore been kept relatively simple to simplify the transition to a layout design.

Chapter 2
Theoretical background

2.1 Power Amplifiers

Amplifiers are electric components which increase the power, current or voltage of an electric signal. The signal at the input is amplified using DC power from a power supply to provide a proportionally greater signal at the output. The gain of the amplifier is the ratio of the output signal to the input signal. It can be in either voltage, current or power. In this work, a power amplifier (PA) is considered. PAs are an essential component in RF and mmWave applications, typically needed in transmitters to drive the antennas. Important properties for a PA include gain, output power, energy efficiency, bandwidth and linearity. The efficiency of the amplifier is defined by

$$\eta = P_{out}/P_{DC} \tag{2.1}$$

and is an important property since, for a power amplifier, high output power gives high DC power consumption as well. Improvements in efficiency will therefore have a large impact on the overall power consumption.

To take both gain and efficiency into account the power added efficiency (PAE) is used which is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.2}$$

and rewritten as

$$PAE = \frac{P_{out}}{P_{DC}}(1 - \frac{1}{G}) = \eta(1 - \frac{1}{G}) \tag{2.3}$$

where G is the gain of the amplifier and η is the efficiency. If the gain is high PAE will be almost equal to the efficiency of the amplifier.

2.1.1 Transmitter

The PAs designed for mmWave frequencies are to be used in the transmitter. In Figure 2.1 a block diagram for the transmitter chain is shown. Here the first design choice was made. A differential topology was chosen for the amplifier due to the common-mode rejection of the differential pair. The phase locked loop (PLL) has a voltage controlled oscillator (VCO) at a frequency, usually two times the carrier

frequency. When implementing a PA on the same chip as the PLL there will be some interference between them. A PA has harmonic frequencies that may interfere with the VCO, especially the second order harmonic of the operating frequency. By choosing a differential amplifier design the 2nd order harmonic will therefore be suppressed [8].

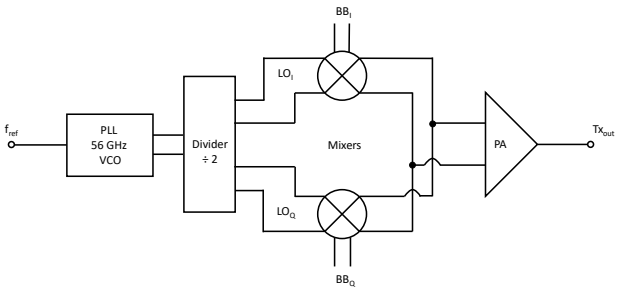


Figure 2.1: Transmitter chain

2.1.2 Linearity

When the input signal increases the transistor will saturate, which means the gain will no longer be linear and the amplifier goes into compression. When the output signal deviates 1 dB from the linear amplification it has reached the 1dB compression point, CP_{1dB}, which marks the end of the linear region. This is illustrated in Figure 2.2.

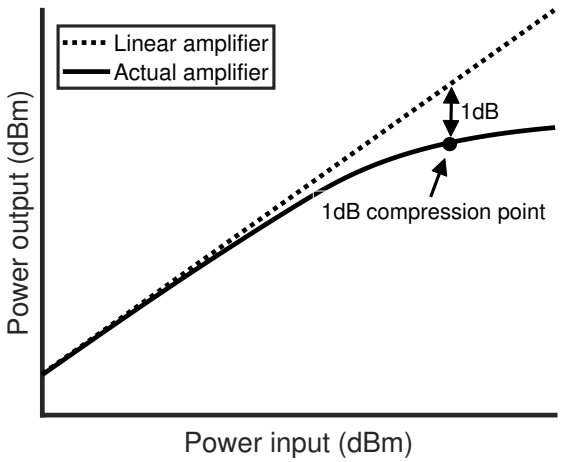


Figure 2.2: 1 dB compression point of amplifier

There are several factors determining when the amplifier reaches compression. Intermodulation distortion and harmonic distortion both affect the linearity by forcing the amplifier into compression earlier due to the added distortion signals [9].

2.1.2.1 Harmonic Distortion

Harmonic distortion is caused by multiples of the fundamental frequency, i.e $2f_0$ and will therefore normally be outside of the bandwidth. Distortion outside the bandwidth is of less importance due to the long distance from the fundamental frequency, and is therefore located where the gain is reduced. However, it may still reduce the linearity of the amplifier. To reduce the effect of harmonic distortion, so called harmonic trap filters can be implemented. A harmonic trap filter is a resonant LC circuit, comprised of a capacitance and an inductance, tuned to the frequency that causes the distortion [10].

2.1.2.2 Intermodulation distortion

Intermodulation distortion (IMD) is signal distortion caused by two or more different frequencies. The intermodulation between the frequencies will cause new distortion products at the sums and differences of the harmonics of these frequencies. The odd ordered intermodulation products, e.g. IM3, at $2f_1 - f_2$ and $2f_2 - f_1$, will be placed close to the carrier frequency within the bandwidth. Higher ordered intermodulation products such as IM5 ($3f_1 - 2f_2$) are also present but have lower amplitude and are at a larger distance to the carrier frequency as seen in Figure 2.3, where the carrier frequency is between f_1 and f_2 [9].

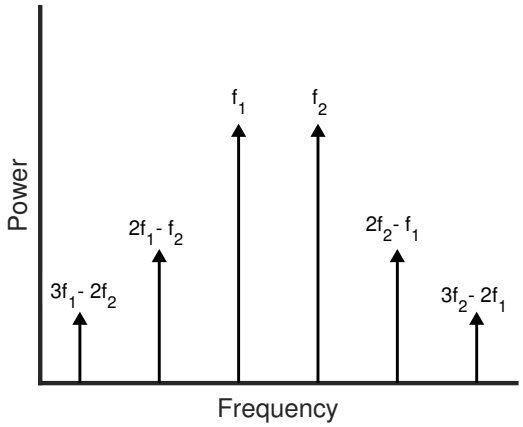


Figure 2.3: Intermodulation products from a two-tone test

The higher order intermodulation products have the largest contribution when operating close to the compression region, but can be ignored at lower output powers. As seen in Figure 2.4, the third order intercept point (IP3) is where the extrapolated output power curve from the fundamental and third order intermodulation (IM3) frequency intercept [9]. In logarithmic scale, the slope of the fundamental is 1:1, while the slope of the IM3 is 3:1 in the low power region.

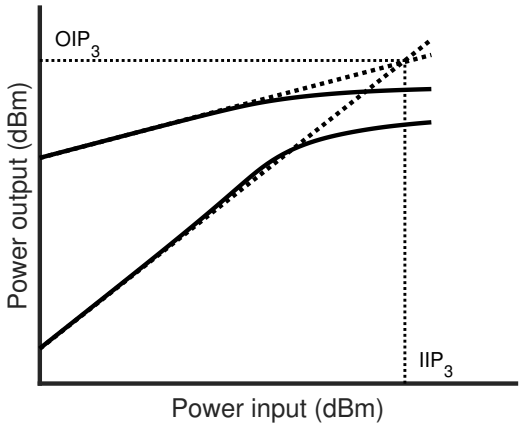


Figure 2.4: Fundamental carrier and third order modulation product P_{out} vs. P_{in} curves

2.1.3 Amplifier classes, A, B, AB and C

There are several different types of amplifier classes. For this thesis, class A, B, AB and C are of most interest. Amplifier classes are defined by the conduction angle of the amplification resulting in different output current waveforms. The conduction angle is set by the bias points which can be extracted with a load line in the IV-curve of the transistors comprising the amplifier, as seen in Figure 2.5a. By increasing the gate bias, the base of the load line will move towards the right, and vice versa, when reducing the gate bias. The position of the load line varies between the different amplifier classes. How the conduction angle affects the output current waveform is illustrated in Figure 2.5b. To restore the output voltage waveform for the class B and C amplifiers a resonant circuit can be used at the output.

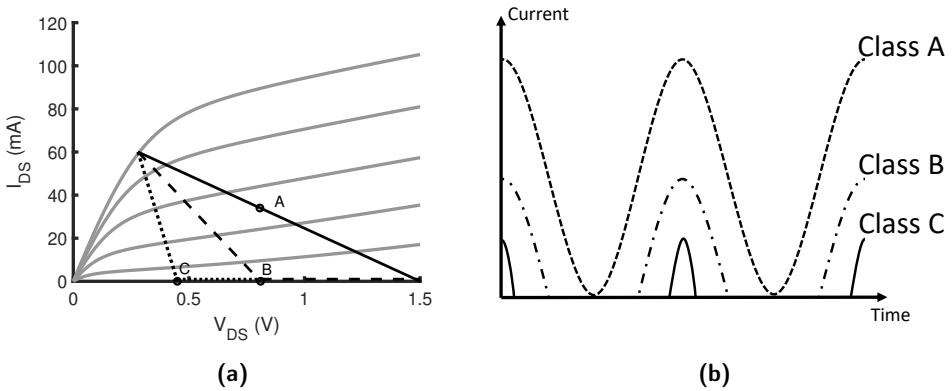


Figure 2.5: (a) IV curve with load lines and biasing conditions for different amplifier classes (b) The output current wave forms of the different amplifier classes

Linearity and efficiency are two conflicting parameters for class A, B and C amplifiers, where A is the most linear but least efficient, and C is the least linear but most efficient, while B is somewhere in between [11].

2.1.3.1 Class A

The class A amplifier is biased so that it operates in the active region at all times, giving the amplifier a conduction angle of 360 degrees. This gives high gain but poor efficiency with a theoretical peak of 50%. Factoring in the need for power back-off to meet linearity requirements, the expected efficiency is degraded further. This renders the class A amplifier too inefficient for use by its own in most wireless systems. Beyond its limitations it still exhibits overall good linearity [9], [12].

2.1.3.2 Class B

The class B amplifier is biased so the active device is only conducting for half of the input waveform, giving it a conduction angle of 180 degrees. The resulting output current is therefore a half-sinusoidal. This is achieved by setting its bias point at the threshold voltage giving it a maximum theoretical efficiency of 78.5%. However, the linearity is degraded for these devices when compared to class A amplifiers [9], [12].

2.1.3.3 Class AB

The class AB amplifier is, as the name implies, a combination of the class A and B amplifiers. The active device is conducting between half and the full input waveform depending on the biasing giving it a conduction angle between 180 and 360 degrees. The linearity of class AB is therefore better than class B but worse than class A and the efficiency vice versa [9], [12].

2.1.3.4 Class C

The class-C amplifier is biased below the threshold voltage to achieve a conduction angle of less than 180 degrees. This gives high efficiency at the cost of low gain and worse linearity. The theoretical efficiency is 100% at zero degrees conduction angle however, in practice this is seldom desired. Due to the sub 180 degrees conduction angle the sinusoidal current is not maintained at the output, only the peaks of the input signal passes the threshold voltage [9], [12].

Amplifier type	Conduction angle
Class A	$\theta = 2\pi$
Class B	$\theta = \pi$
Class AB	$\pi < \theta < 2\pi$
Class C	$\theta < \pi$

Table 2.1: Table of conduction angles for amplifier classes

2.1.4 Topologies

2.1.4.1 Amplifier configurations

Common-source, common-gate and common-drain are the three possible single stage amplifier configurations for MOSFETs and are shown in Figure 2.6 [13]. The field effect transistor (FET) has three terminals, gate, source and drain. The signal will enter in one terminal and exit in another. The remaining terminal is the "common", e.g. if the signal enters the gate and exits in the drain it is a common source configuration. These configurations can be combined to create different types of topologies which improve shortcomings of the single stage amplifiers configurations.

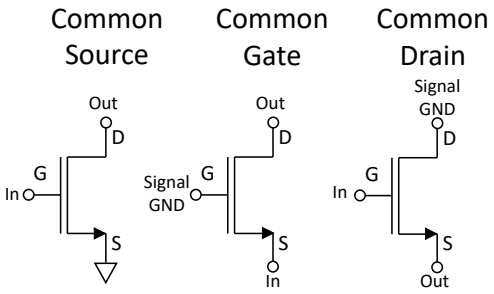


Figure 2.6: Schematics of the different amplifier configurations

2.1.4.2 Differential topology

A differential amplifier has two inputs in opposite phase and amplifies the difference between the inputs. A schematic of the differential topology is shown in Figure 2.7a. Any signal that is common for both inputs, such as noise in the biasing, will not impact the output signal in this configuration if the devices are perfectly matched. An effect of this is that the differential pair will reject even harmonics of the fundamental frequency. This is because the even harmonics are in phase for both differential branches and will thus cancel each other when subtracted [8].

However, the differential topology offers no improvement in signal isolation for the fundamental frequency and odd harmonics compared to the single ended alternative and will thus also suffer from limited signal isolation. In PAs, the transistors are large and thus the parasitic capacitances increase. To improve the isolation and stability of a common source differential amplifier, one can introduce capacitive cross coupling neutralization. This reduces the parasitic effect from the gate-drain capacitance [14]. The cross coupling neutralization is a capacitance between the drain of one transistor to the gate of the other transistor of the differential pair, and vice versa. Choosing an optimal value of this capacitance will cancel the gate-drain capacitance, since, the output voltages of the differential pair are of opposite signs and thus increasing the power gain, reverse isolation and stability [14].

The cross coupled capacitance in Figure 2.7a is not manufactured in the same process step as the transistors, so due to manufacturing variations, the size of the capacitance is difficult to control in relation to the gate-drain capacitance. By instead using an active neutralization component, such as a transistor with the source and gate connected as in Figure 2.7b, the process spread can be mitigated. Then only the mismatch variations will affect how well the gate-drain capacitance is canceled.

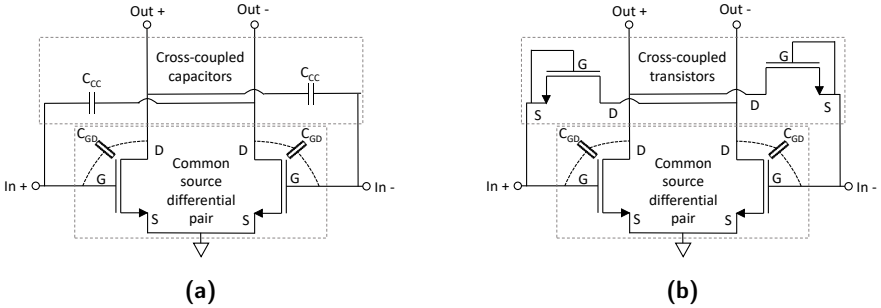


Figure 2.7: Schematic view of common source differential amplifier with capacitive cross-coupling a) Using capacitances (b) Using gate source connected transistor

2.1.4.3 Cascode topology

The cascode topology is a common design choice among PAs, achieved by connecting a common source (CS) and a common gate (CG) transistor in series. This topology can also be combined with the differential topology as seen in Figure 2.8 to achieve common-mode rejection.

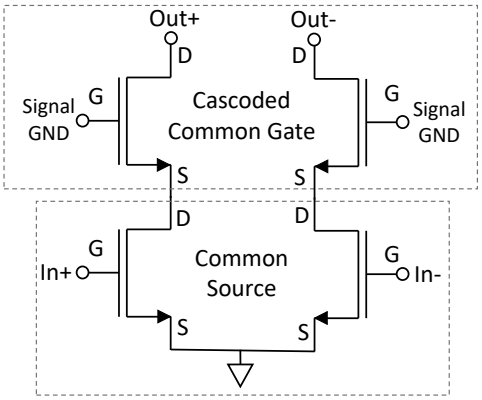


Figure 2.8: Schematic view of a differential cascode amplifier

The main purpose of the cascode is to improve the CS topology with higher output impedance and better isolation between input and output. The higher output impedance derives from the fact that the cascoded CG acts as a current follower, transforming the current driven by the CS from low to high resistance. To further explain this, it is necessary to analyse the resistance of both the CS and CG separately in the topology before combining them. The input resistance of a CG, $R_{in,CG}$, if the CG transistor output resistance, $r_{o,CG}$, is large it can approximately be given by [15]

$$R_{in,CG} \approx 1/g_{m,CG} \tag{2.4}$$

where $g_{m,CG}$ is the CG transistor transconductance. The output resistance of a CS, $R_{out,CS}$, is given as [16]

$$R_{out,CS} = r_{o,CS} = \frac{1}{\lambda I_D} \tag{2.5}$$

where $r_{o,CS}$ is the output resistance of the CS transistor, λ its channel length modulation coefficient and I_D its drain current. Between the transistors, the input resistance of the CG is much smaller compared to the output of the CS, allowing for good current transfer between the transistors. Finally, the output resistance of the cascoded CG, $R_{out,CG}$, is approximately

$$R_{out,CG} \approx g_{m,CG}\, r_{o,CS}\, r_{o,CG} \tag{2.6}$$

giving the cascode higher output resistance compared to the single transistor CS [15]. The cascoded topology also puts the CS stage under less voltage stress,

allowing for higher V_{DD} to be used without damaging the circuit at large voltage swings [9].

One of the inherent problems with CS amplifiers is limited stability, due to low isolation between input and output given by the parasitic capacitance, C_{gd}, allowing reverse feedback [9]. In CS amplifiers with voltage gain, C_{gd}, leads to the Miller effect. The Miller effect increases the input capacitance thus reducing the bandwidth, which is undesirable [17]. The cascode topology helps ease these issues present in the CS amplifier with the addition of a cascoded CG stage. The low load at the CS output removes the voltage gain of the CS, effectively cancelling the Miller effect. The reverse feedback is also decreased improving stability [18], [19], [9].

2.1.5 Modulation

By using different types of signal alterations in phase, amplitude, time and frequency, more data can be transmitted within a certain bandwidth. Modulation schemes used in modern cellular networks are getting more complex with each generation, increasing the modulation order to support higher data rates. 5G for example, uses multiple different modulations where the more complex ones are 64 and 256-QAM OFDM (quadrature amplitude modulation)(orthogonal frequency-division multiplexing) [4].

2.1.5.1 Quadrature amplitude modulation

QAM is a common modulation technique for wireless communication. In QAM, the symbols are represented by both phase and amplitude combinations. This is usually visualized in a constellation diagram, as seen in Figure 2.9, showing all possible symbols for 64 QAM. Each symbol represents a fixed number of bits depending on the modulation order. In the case of 64-QAM, each symbol represents a unique combination of 6 bits. When increasing the modulation order, the symbol density increases in the constellation diagram. The higher density will cause more bit-errors when symbols are poorly defined due to noise or nonlinear amplification. Another effect of higher modulation orders is increased peak-to-average power ratio (PAPR). This is due to the increased difference in the average and highest amplitude component between symbols. The reason to move towards higher modulated schemes are to increase the spectral efficiency which is the information rate in bits per second per hertz, that can be transmitted over a certain bandwidth [20].

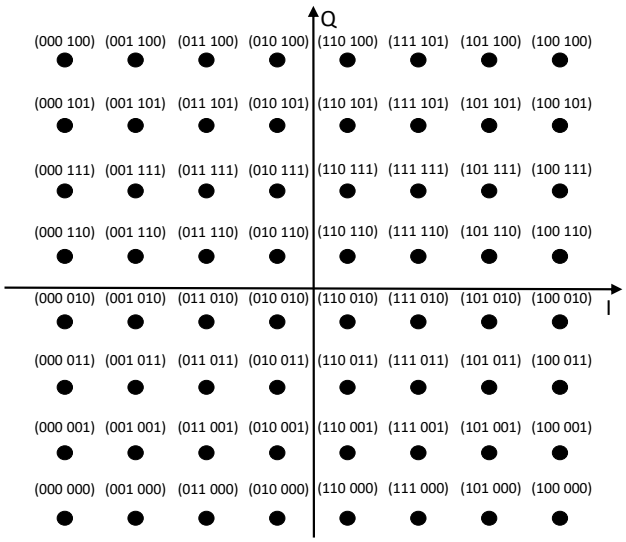


Figure 2.9: 64-QAM Gray constellation diagram

2.1.5.2 Orthogonal frequency-division multiplexing

To send multiple symbols at once, a frequency band can be divided into several subcarriers. The 5G network uses orthogonal frequency-division multiplexing (OFDM). This technique separates the channel into narrow-band subcarriers. Traditional frequency-division multiplexing (FDM) requires guard bands in between the channels to prevent interference. In OFDM however, each subcarrier is orthogonal to the others, i.e. the center frequency of each subcarrier is located at one of the minima of the neighbouring channels. This makes it possible to not use a guard band and OFDM has therefore high spectral efficiency. The presence of multiple subcarriers in OFDM causes the PAPR to increase significantly [21].

2.1.6 Doherty power amplifier

The Doherty power amplifier (DPA) topology is a well established amplifier configuration that William H. Doherty developed in 1936 [22]. Originally it was used to improve efficiency in high power radio transmitters, but fulfills the same purpose in today's cellular transmitters. In order to ensure linear amplification throughout the power range of the modulated signal, the average power during operation is backed-off with respect to the compression point. This is especially important for modulated signals with high PAPR e.g. 64-QAM. Operating at back-off reduces the efficiency for all mentioned amplifier classes, however, the DPA solves this by combining two amplifiers in parallel. These two amplifiers are referred to as the main and the auxiliary amplifier, with the main usually being class A through B, and the auxiliary class C. An overview of the Doherty amplifier concept can be seen in Figure 2.10. The function of the $\lambda/4$ transmission lines is to get proper load modulation at outputs of both amplifiers, a concept which we

will further discuss throughout this section.

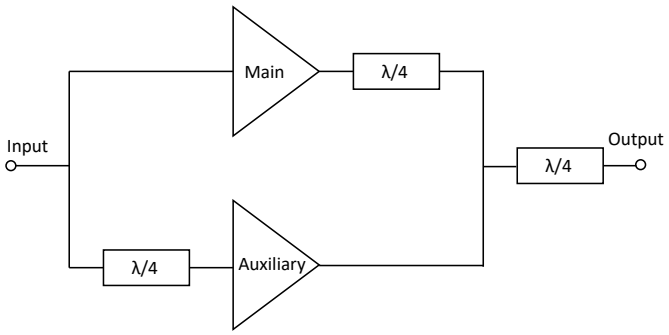


Figure 2.10: Doherty power amplifier concept

The efficiency of a single amplifier is proportional to the output swing voltage, $\eta \propto V_{output}/V_{DC}$ [9]. If the output swing voltage can be kept at its maximum value over a range of input voltages the efficiency will also be at the highest value in that input range. When the input voltage is increased so is the load current, and since, $V_{output} = IR_L$ the resistive load will need to be reduced in order to keep V_{output} constant. This is called load modulation and makes it possible to increase the output power while keeping the output voltage constant [9], [23], [24].

The load modulation begins when the auxiliary amplifier is turned on and starts to inject signal current into the load. While the input voltage is lower than half of its maximum, the auxiliary PA is turned off and ideally has infinite output impedance. When turned on, the output impedance of both amplifiers will be load modulated to an optimum value (R_{opt}) depending on the characteristic impedance of the transmission lines at the output. In Figure 2.11 a simplified schematic of the Doherty amplifier is shown to help illustrate the load modulation concept. The $\lambda/4$ transmission line will provide a 90° phase shift of the current and also transform the impedance as

$$Z_{in} = \frac{Z_T^2}{Z_L} \tag{2.7}$$

where Z_{in} is the new impedance, Z_T the characteristic impedance of the transmission line and Z_L is the load impedance. These characteristics of the transmission line are only valid for signals with wavelengths corresponding to the wavelength the transmission line is designed for. This can affect bandwidth, since, the characteristics change with frequency [11].

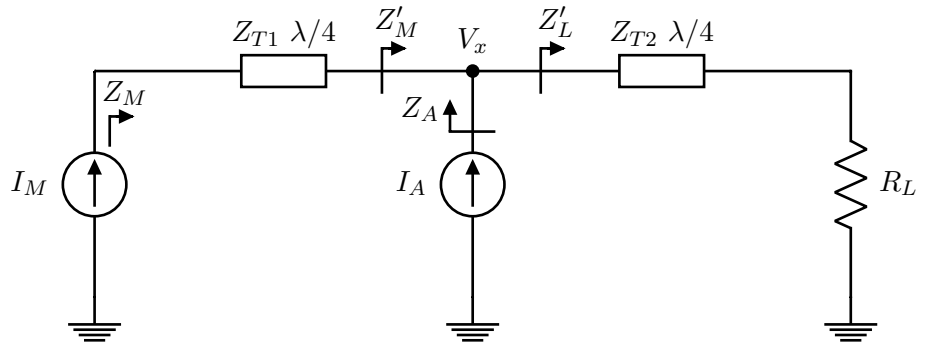


Figure 2.11: Schematic view of the Doherty PA concept

The load impedances of the two amplifiers are described in equations 2.9 and 2.11. To find the expressions for the main and auxiliary amplifiers load impedance in Figure 2.11 we begin by defining the voltage in node x, V_x, given by

$$V_x = (jI_M + I_A)\frac{Z_{T2}^2}{R_L} \tag{2.8}$$

where the imaginary I_M is a result from the phase shift in transmission line T_1. The impedance seen from the auxiliary amplifier, Z_A, can then be written as

$$Z_A = \frac{V_x}{I_A} = \frac{(jI_M + I_A)}{I_A}\frac{Z_{T2}^2}{R_L} = (1 + \frac{jI_M}{I_A})\frac{Z_{T2}^2}{R_L} \tag{2.9}$$

where it is evident that there needs to be a 90° phase shift between I_M and I_A to achieve a real impedance, Z_A. To find the expression for the impedance seen from the main amplifier, Z_M, we start by defining the expression for Z'_M which is

$$Z'_M = \frac{V_x}{jI_M} = \frac{(jI_M + I_A)}{jI_M}\frac{Z_{T2}^2}{R_L} = (1 - \frac{jI_A}{I_M})\frac{Z_{T2}^2}{R_L} \tag{2.10}$$

The expression for Z_M is then

$$Z_M = \frac{Z_{T1}^2}{Z'_M} = \frac{Z_{T1}^2 R_L}{Z_{T2}^2(1 - \frac{jI_A}{I_M})} \tag{2.11}$$

also here it is apparent that a shift of 90° between I_A and I_M is needed for the load impedance to become real. This is achieved in the Doherty amplifier by using a transmission line at the auxiliary input.

As mentioned earlier, the load modulation is tuned by changing the characteristic impedance of the output transmission lines. Using $Z_{T1} = R_L$ and $Z_{T2} = R_L/\sqrt{2}$ for the transmission lines and a 90° phase difference between I_M and I_A, the main amplifier load is modulated from $2R_{opt}$ to R_{opt} and the auxiliary amplifier load from ∞ to R_{opt}. For example if $R_L = R_{opt} = Z_{T1} = 50\Omega$ and $Z_{T2} = 35\Omega$ then

$$Z_A = (1 + \frac{I_M}{I_A})\frac{35^2}{50} = (1 + \frac{I_M}{I_A})25 \tag{2.12}$$

and

$$Z_M = \frac{50^2 \cdot 50}{35^2(1 + \frac{I_A}{I_M})} = \frac{100}{1 + \frac{I_A}{I_M}} \tag{2.13}$$

The main amplifier load is modulated from 100 Ω to 50 Ω and the auxiliary load from ∞ to 50 Ω.

A general example of load modulation is illustrated in Figure 2.12a and the currents for each amplifier is shown in Figure 2.12b. While the auxiliary amplifier is turned off it will not affect the operation of the main amplifier, this is known as the low power region. When the auxiliary is turned on the main amplifier will see the other load resistance, R_{opt}. This is called the Doherty region [25].

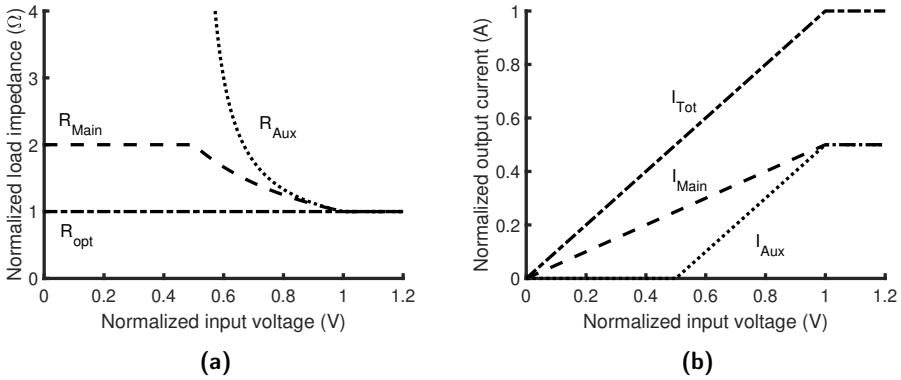


Figure 2.12: (a) Load modulation of Doherty amplifier, impedance vs. input voltage (b) Current vs. input voltage for the main and auxiliary

The efficiency of the Doherty PA in the two regions is shown in Figure 2.13a and 2.13b. The idea is to operate around the "Doherty peak" at back-off were we get a major increase in efficiency compared to a class B amplifier. The ratio in maximum current between the main and auxiliary amplifiers can be tuned to get the efficiency peak at a desired back-off power [9], [25].

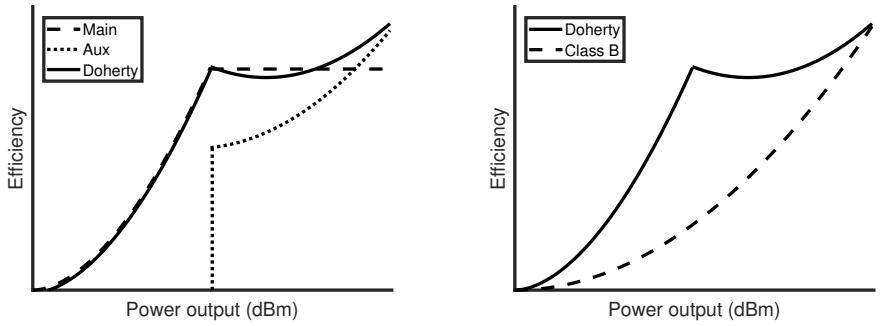


Figure 2.13: (a) Efficiency of Doherty power amplifier (b) Efficiency of Doherty amplifier and class B power amplifier

2.2 Nanowire Transistors

With the transistors being further scaled the voltage tolerance is reduced. Moving towards higher operational frequencies and lower supply voltages, there will be difficulties to achieve high output power. The physical limits of what can be achieved using planar transistor designs and silicon are being reached. To allow for further improvements, innovations with 3-dimensional channel geometry, like nanowire transistors and the introduction of new materials such as III-Vs are necessary. III-V materials are combinations of the elements in column three and five in the periodic table, for example Indium (In) and Arsenic (As). InAs have high mobility but suffers from band to band tunneling due to a narrow bandgap. In order to increase the bandgap InAs may be combined with another III-V with a wider band gap, using so called bandgap engineering. In this case InAs is combined with Gallium (Ga) to form InGaAs at the drain contact [26].

2.2.1 Geometry

In this thesis we have been using nanowire transistors. Nanowires are classified as one dimensional structures, since, the length is much larger than the width of the structure. The nanowires are grown vertically on a silicon wafer.

When scaling devices, various short channel effects (SCEs) are introduced due to the limited electrostatic control of the channel. The electrostatic control is how well the gate can control the channel current. Electrostatic control can be improved by increasing the contact area of the gate or by decreasing the thickness of the isolation layer between gate and channel. Traditionally, planar transistors with a two dimensional contact area between the gate and channel have been used, however, to achieve better electrostatics, three dimensional structures such as FinFET [27] and gate all-around (GAA) [7] have recently been implemented. The vertical nanowire allows for the gate to be all around the channel and achieves

improved electrostatic control compared to other approaches. Figure 2.14 shows the simplified geometry of a nanowire transistor and a planar transistor [7].

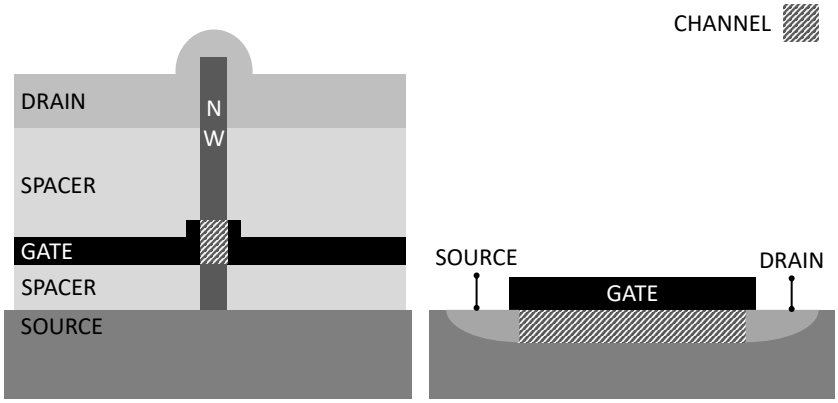


Figure 2.14: Simplified comparison between GAA and planar channel geometry

2.2.2 III-V Materials

Since the limit of how far the scaling of silicon transistors can continue is reaching its end, there is a need for new materials with better electric properties. III-Vs have shown increased conductivity and compatibility with high relative dielectric constant, k, oxides. High k oxides are favorable, since, they provide better coupling between the gate and channel, thus allowing for thicker oxides while keeping the same capacitance. It is beneficial to use thicker oxides since it reduces the gate to channel tunneling. The relation between capacitance and k is given by

$$C = \frac{k\epsilon_0 A}{t} \tag{2.14}$$

where ϵ_0 is the free space permittivity, A the capacitor area and t the oxide thickness [11].

Moving towards III-V materials must be economically viable. Compared to silicon, the III-V wafers are expensive [28]. To reduce the wafer cost it would be beneficial to implement the III-V structures on silicon wafers instead. There are often problems with lattice mismatch when growing on silicon wafers. However, nanowires have due to their small footprint, which reduces the propagation of defects, proven to be a good choice to integrate III-V:s on silicon wafers [28]. In(Ga)As nanowire devices on silicon is an economical way to gain the performance improvements from III-V:s.

Beyond channel scaling, supply voltage scaling is also important for high

efficiency. The electrical properties of silicon, such as injection velocity, hinders further voltage scaling without heavy degradation in on-current levels. Transistors using III-V materials, like In(Ga)As, can match silicon based transistor currents with half the supply voltage due to their higher injection velocity [29].

2.2.3 Model

A proper transistor model is crucial when simulating and designing circuits to get good correspondance with measurement data for manufactured devices. However, the model must not be too complex to get reasonable simulation times without immense computational power. Traditional transistor modeling techniques have historically been a good fit for MOSFETs, but with transistors moving into the nanometer regime, new types of models are needed to efficiently model their properties [30], [31], [32]. This also goes for the nanowire transistor used for this thesis.

The transition to nanometer regime transistors presents new carrier transportation mechanisms that start to dominate its characteristics. More specific, quasi-ballistic instead of purely diffusive carrier transportation [31], [32]. For long channel devices, carriers will collide when moving from source to drain, since, their mean-free path, the average travel length between collision, is much shorter than the channel itself. This is referred to as diffusive transportation, where collisions sets the limits for maximum current throughput. When the channel length starts to approach the same length as the carrier mean-free path, the average amount of collisions decreases until the statistical possibility of collision is negligible. This collision free transportation is referred to as ballistic transportation [33]. Quasi-ballistic transportation is when the current has both a significant ballistic and diffusive part. Carriers approach the ballistic limit for short channel MOSFETs, meaning that the carriers can go through the channel without scattering. For quasi-ballistic FET, there is some scattering which will lower the mean velocity $\bar{v}$ this can be expressed as [30]

$$\bar{v} = \frac{\lambda}{\lambda + L} v_{max} \tag{2.15}$$

where λ is the carrier mean free path, L is the channel length and v_{max} is the maximum carrier velocity [30]. For the transistors used in this thesis, the gate length is 50 nm. The virtual source (VS) model is a well established way of modeling short channel devices, as the nanowire transistor, with good accuracy while remaining easy to compute. The name virtual source derives from the way the device is modeled, by looking at the "virtual source" of the device. The virtual source is defined at the location where the energy barrier is at its maximum between the source and channel, usually referred to as x_0. This can be seen in Figure 2.15 [31].

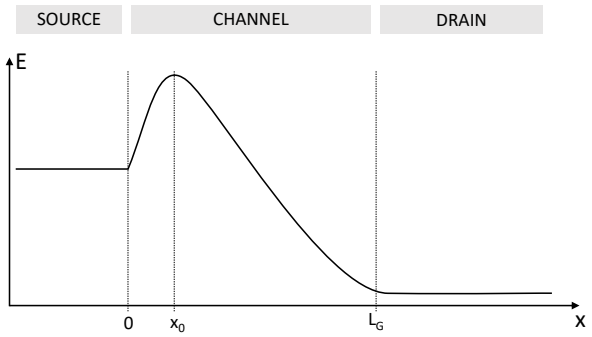


Figure 2.15: Schematic view of energy barrier in transistor channel for virtual source location

In the model the drain current, I_D, at saturation is expressed as [32]

$$I_D = F_s Q_{ix_o} \bar{v}_{x_0} \tag{2.16}$$

where Q_{ix_0} is the charge area density and $\bar{v}_{x_0}$ the average carrier velocity at x_0. F_s is a fitting parameter. Q_{ix_0} is given by equation [30]

$$Q_{ix_0} = C_{inv}(V_{GS} - V_T) \tag{2.17}$$

where C_{inv} is the gate capacitance at strong inversion and V_T is the threshold voltage. F_s is a function dependent on V_{DS} managing non-saturated operation. F_s is given by [32]

$$F_s = \frac{V_{DS}/V_{DS,sat}}{(1 + (V_{DS}/V_{DS,sat})^{\beta})^{1/\beta}} \tag{2.18}$$

where $V_{DS,sat}$ is the V_{DS} at saturation and β is used as a fitting parameter. F_s is present to avoid discontinuity in the model during operation transitions. The next parameter of importance is the threshold voltage, V_T. V_T is dependent on V_{DS} beyond its zero-bias state which is expressed as

$$V_T = V_{T0} - \delta(L_{eff})V_{DS} \tag{2.19}$$

with the effective gate length, L_{eff}, dependent drain induced barrier lowering (DIBL) coefficient being $\delta(L_{eff})$ and V_{T0} the zero-bias threshold voltage [32]. Beyond this, there are some minor dependencies between parameters, most notably $\delta(L_{eff})$ variations affecting v_{x_0}, which is the only one large enough to be considered. These dependencies are technology dependent as they are affected by material and device parameters [32].

To implement a VS-model for a given transistor, the device current-voltage (IV) and capacitance-voltage (CV) characteristics need to be extracted. Additional parasitics need to be added to account for the non-voltage dependent resistive and capacitive parasitics present due to non-ideal device contact. These parasitics surrounding the VS model can be seen in Figure 2.16.

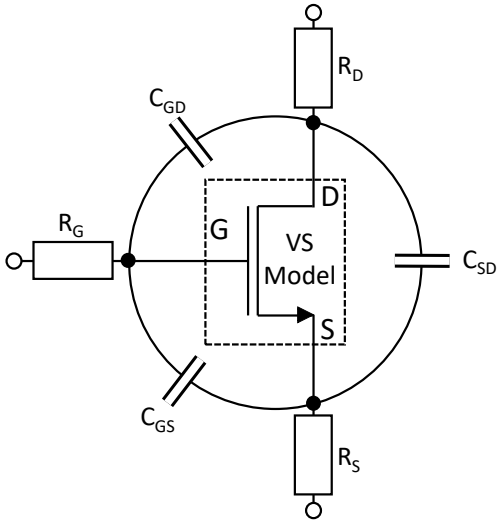


Figure 2.16: Parasitics surrounding the VS model

For the nanowire transistor used in this work, the complete small-signal model is shown in Figure 2.17 [7].

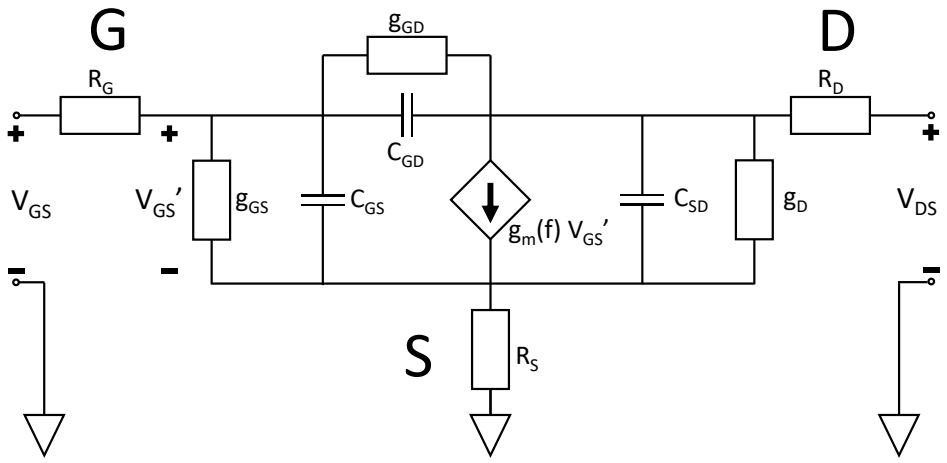


Figure 2.17: Small-signal model of nanowire transistor

2.3 Design specification

The 5G specification is set by the 3rd generation partnership project group (3GPP) which have selected multiple frequency bands for 5G deployment each

with its own specification. The 5G frequency band chosen for this thesis is the n257 band that covers frequencies 26.5 to 29.5 GHz with the center frequency at 28 GHz [3]. The bandwidth of our PA needs to be wider than the intended signal band so the final requirement was decided to be 5 GHz. There are several power classes that determine the specification for each type of equipment, e.g. handheld devices, picocell or femtocell basestations. In this thesis we are limited to a supply voltage of 1.5 V due to the breakdown voltage of the transistors. Power class 3 is the default power class and have the lowest output power demands [3].

The minimum peak equivalent isotropically radiated power (EIRP) demand for power class 3 is 22.4 dBm [3]. From the EIRP the required output power for the amplifier at back-off can be calculated using

$$EIRP = G_{array} + P_{PA} \tag{2.20}$$

where G_{array} is the gain from the antenna array and P_{PA} is the output power for the amplifier at back-off. Assuming 8 antennas per user equipment (UE), no antenna gain and one PA per antenna

$$G_{array} = 20log_{10}(N) = 20log_{10}(8) = 18dB \tag{2.21}$$

where N is number of antennas, and in extension

$$P_{PA} = 22.4 - 18 = 4.4dBm \tag{2.22}$$

There will also be losses due to the connections from the PA to the antenna of about 2 dB[34]. This leaves us with

$$P_{PA} = 6.4dBm \tag{2.23}$$

and since the PAPR of the 64-QAM signal is around 9 dB [5], the requirement for saturated output power is 9 dB higher at 15.4 dBm.

The error vector magnitude (EVM) is related to the bit error rate (BER) and is to the largest extent determined by the linearity of the amplifier. Other sources of EVM are I/Q transmitter imbalance and noise from the phase locked loop (PLL). The average EVM can be no more than -25 dBc which corresponds to 5.5% [3].

Other DPA designs, with a similar supply voltage and output power while operating at 28 GHz, have achieved around 10-20% PAE at 9 dB back-off [24], [35], [36], [37]. The aim is to maximize the PAE, but for reference the requirement was set to 20% PAE at 9 dB back-off.

	Specifications
P_{ave}	6.4 dBm
P_{max}	15.4 dBm
f_0	28 GHz
BW	5 GHz
EVM	-25 dBc (5.5%)
Modulation	64-QAM
Gain	15 dB
PAE@BO	20%

Table 2.2: The specification aim of the amplifiers in this thesis

Chapter 3

Design and Comparison of Amplifiers

3.1 Simulation tools

All design and simulation for this thesis was done using AWR Design Environment which has tools for DC, AC and harmonic balance simulations, but also system simulations for testing with modulated signals. The passive device, i.e. the transformer, was realized with a lumped model with resistors, capacitors and inductors. The transformer model is shown in Appendix (Figure 5.1 and 5.2). The transistor model was supplied as Verilog-A code. For all power gain, output power and PAE measurements, single tone harmonic balance simulations were used. For linearity, two tone tests with a separation of 0.1 GHz were used.

3.2 Verification of the transistor models

Before designing the PAs comprising the DPA, the supplied transistor model was evaluated using DC and AC simulations. Parameters such as transconductance and threshold voltage, but also IV-characteristics play an important role when choosing bias and sizing of the transistors during the PA design.

The devices used in the simulations have 50 nm gate length, L_g, and a diameter, d_{NW}, of 30 nm. The characterization was done using 1000 nanowires, since, initial testing showed that this number of nanowires was able to support the output current needed to meet the output power specification, with a 1.5 V supply voltage and a 50 Ω load. For nanowire transistors, the device width, W, is its channel circumference which is determined by the number of nanowires, N_{NW}, following equation

$$W = \pi d_{NW} N_{NW} \tag{3.1}$$

where d_{NW} is the diameter of the nanowires.

In Figure 3.1a the drain current, I_{DS}, vs. the drain-source voltage, I_{DS}, is shown for different gate voltages. The linear dependence of I_{DS} on V_{GS} as shown in Figure 3.1b is due to the transistor being a short channel device. A conventional long channel device, by comparison, would have a quadratic dependence. From the same figure the threshold voltage, V_T, can be extracted by extrapolating the

linear region, V_T is found to be 0.17 V for our device when using a supply voltage of 1.5 V.

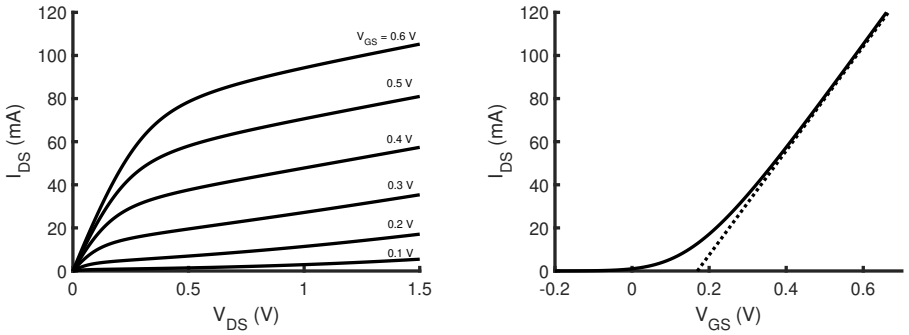


Figure 3.1: (a)I_{DS} vs. V_{DS} characteristics (b) I_{DS} vs. V_{GS}, V_{DS} = 1.5 V

The transfer curve is shown in Figure 3.2, from which the subthreshold slope (SS) is found to be 98 mV/dec.

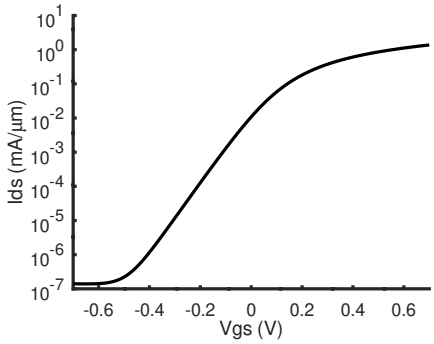


Figure 3.2: Transfer curve of the transistor, V_{DS} = 1.5 V

3.3 Design of amplifier classes

Before designing the Doherty amplifier, a comparative study was made between the implementations of different amplifier classes to get a better understanding of their performance. This is important when choosing which amplifier classes to pair in the Doherty topology as their properties regarding gain, PAE and linearity varies.

Constraints were set limiting sizing and biasing to achieve reliable measurement results in future fabrication. The limits set were 1500 nanowires per transistor

and a maximum of 1.5 V DC voltage across the source-drain of the transistors to allow for headroom during voltage swing. For comparison purposes between the different classes and topologies all PAs have the same number of nanowires, 1000, in their common source transistor.

For proper characterization of the amplifiers, small signal analysis needs to be conducted. However, the class C amplifier is biased by the large input signal which is ignored in the small signal analysis. Even though the small signal analysis loses accuracy when the devices are biased by a large input signal, the simulations still provide information that can be useful especially in comparisons. The large signal bias was compensated for by increasing the gate bias of the class C amplifier while performing the small signal analysis. The bias chosen corresponds to the large signal bias at 9 dB back-off from the compression point, i.e. the start of the Doherty region.

We have decided to keep the matching network simple with just the transformer, a parallel capacitance, and the cross-coupled transistors. This makes the design easier to manufacture and compare with other technologies. The performance of the active nanowire device is the focus of this thesis.

The choice of supply voltage, V_{DD}, has a large impact on PAE and maximum output power. Since, V_{DD} is fixed for all amplifiers in the same circuit, this was one of the key parameters decided from the beginning of the design process. This optimisation was done by mainly looking at PAE at 1dB compression for different V_{DD}, while keeping in mind the 1.5 V limit over each transistor and the saturation output power. For the differential CS amplifier the results can be seen in Figure 3.3a. The chosen supply was $V_{DD} = 1.5$ V. For the cascode, the results can be seen in Figure 3.3b, with respect to both V_{DD} and $V_{GS,CG}$. The variation in $V_{GS,CG}$ is displayed as different traces. The filled in zone shows approximately which conditions that results in a voltage higher than 1.5 V over one of the transistors. The V_{DD} chosen was 2.5 V since it allowed for the highest PAE while remaining in the allowed region.

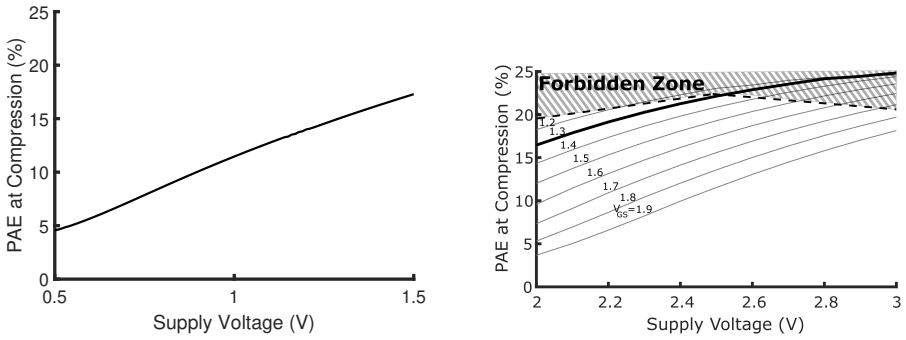


Figure 3.3: PAE at 1dB compression for different supply voltages (a) Differential CS (b) Cascode with traces for CG gate bias, the forbidden zone indicates unpermitted bias conditions

3.3.1 Differential common source

In Figure 3.4, the schematic for the differential common source amplifier is shown. All the amplifier classes use the same schematic but with variations in gate bias and matching capacitances, C_1 and C_2, to achieve the desired conduction angle and center frequency of 28 GHz. To increase stability, capacitive cross-coupling neutralization with gate source connected transistors is used. Voltage bias is supplied through a center tap on the transformers at the input and output. The maximum allowed supply voltage of 1.5 V is used to achieve maximum output power and PAE.

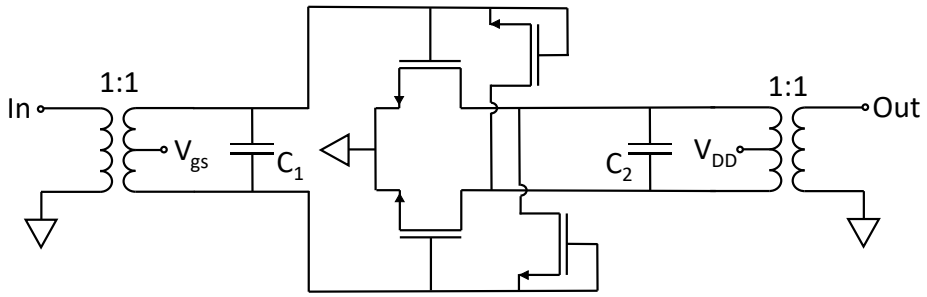


Figure 3.4: Schematic of common source differential amplifier

3.3.1.1 Class A differential common source amplifier

The differential common source amplifier in class A operation has a gate bias of 0.35 V, which corresponds to a high value of g_m. The size of the cross-coupled transistors are 450 nanowires and the capacitanses are, $C_1 = 110$ fF and $C_2 = 90$ fF.

In Figure 3.5a the smith chart with S_{11} and S_{22} is shown. The S-parameters with respect to frequency can be seen in Figure 3.5b. The 3 dB bandwidth of S_{21} is from 24.6 GHz to 32.4 GHz.

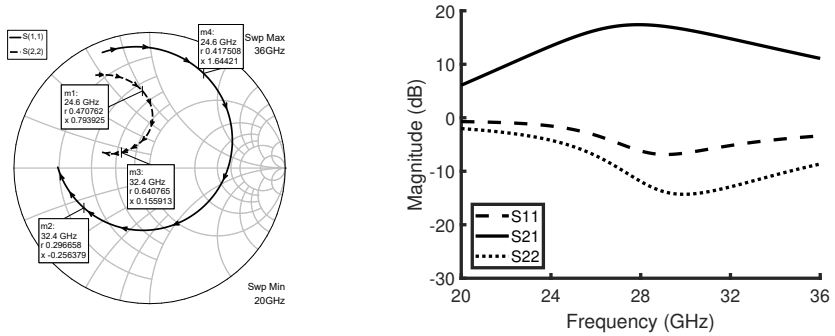


Figure 3.5: Differential CS class A (a) Smith chart S-parameters (b) S-parameter magnitudes

The single tone simulation results for the class A amplifier are found in Figure 3.6. The P_{out} vs. P_{in} curve can be seen in Figure 3.6a, P_{sat} is 17.0 dBm. Figure 3.6b shows the gain and PAE of the amplifier at 28 GHz. The power gain of the amplifier is 17.4 dB and the 1 dB compression point (OCP_{1dB}) is at 13.7 dBm output power. The maximum PAE is 45.2 % and the PAE at OCP_{1dB} is 17.3 %.

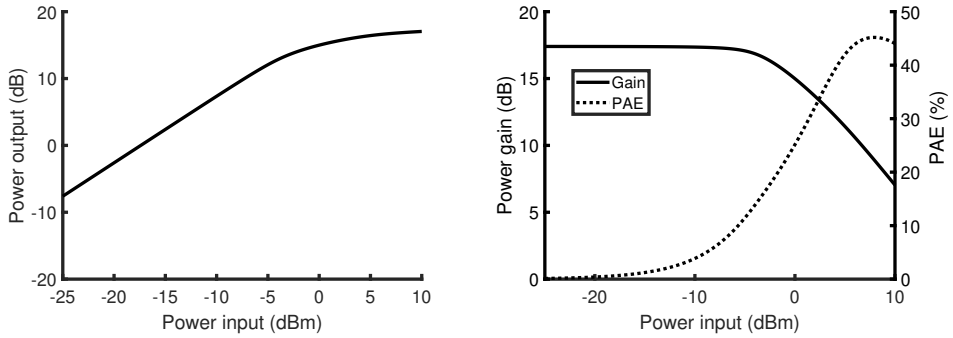


Figure 3.6: Differential CS class A (a) P_{out} vs. P_{in} at 28 GHz (b) Gain and PAE vs. input power at 28 GHz

The results, from two tone simulation with frequencies 28 GHz and 28.1 GHz, are shown in Figure 3.7 where OIP_3 is at 28 dBm.

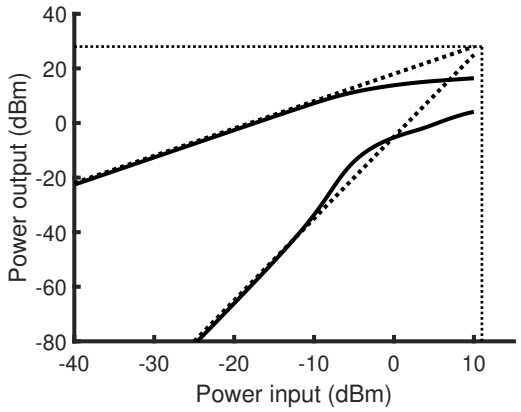


Figure 3.7: Differential CS class A IP3

3.3.1.2 Class AB differential common source amplifier

The differential common source amplifier in class AB operation has a gate bias of 0.2 V which corresponds to a value just above the threshold voltage and will thus ensure the desired conduction angle. The size of the cross-coupled transistors are 450 nanowires and the capacitances are, $C_1 = 110$ fF and $C_2 = 100$ fF.

In Figure 3.8a the smith chart with S_{11} and S_{22} is shown. The S-parameters with respect to frequency can be seen in Figure 3.8b. The 3 dB bandwidth of S_{21} is from 25.0 GHz to 32.3 GHz.

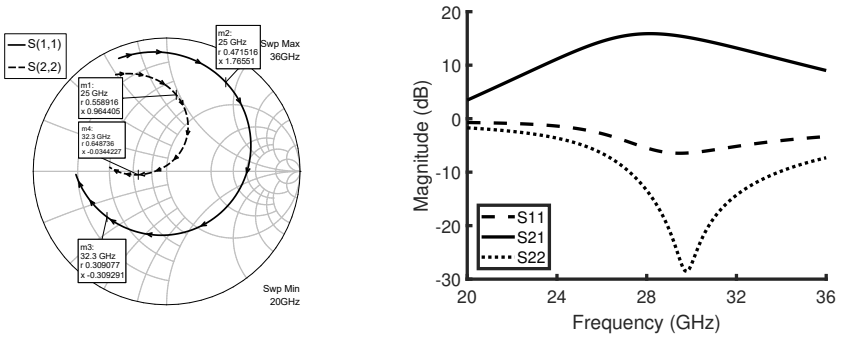


Figure 3.8: Differential CS class AB (a) Smith chart S-parameters (b) S-parameter magnitudes

The single tone simulation results for the class AB amplifier are found in Figure 3.9. The P_{out} vs. P_{in} curve can be seen in Figure 3.9a, and P_{sat} is 16.6 dBm. Figure 3.9b shows the gain and PAE of the class AB amplifier at 28 GHz. The power gain of the amplifier is 15.9 dB and the 1 dB compression point is at 12.9 dBm output power. The maximum PAE is 44.2 % and the PAE at OCP_{1dB} is 26.9 %.

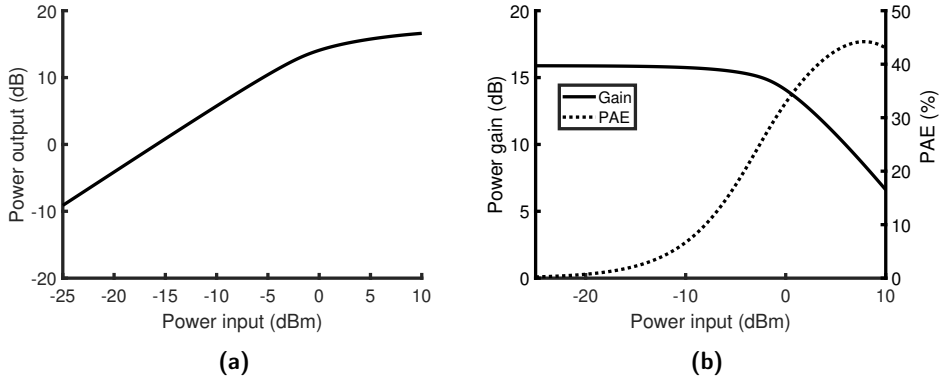


Figure 3.9: Differential CS class AB (a) P_{out} vs. P_{in} at 28 GHz (b) Gain and PAE at 28 GHz vs. input power

The results from the two tone simulation with frequencies 28 GHz and 28.1 GHz, are shown in Figure 3.10 where OIP_3 is at 25 dBm.

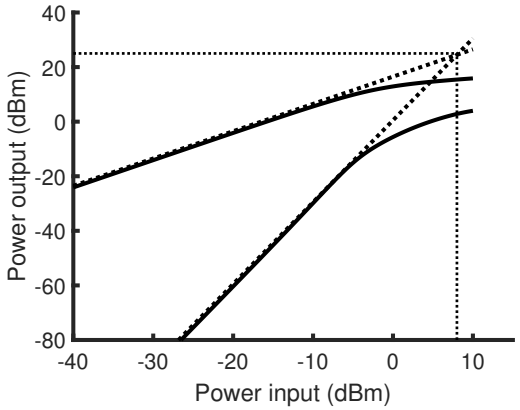


Figure 3.10: Differential CS Class AB IP3

3.3.1.3 Class C differential common source amplifier

The differential common source amplifier in class C operation has a gate bias of 0 V which corresponds to a value below the threshold voltage to ensure a low conduction angle. The size of the cross-coupled transistors are 450 nanowires and the capacitanses are, $C_1 = 110$ fF and $C_2 = 110$ fF.

The S-parameters with respect to frequency have been extracted at 9 dB below the compression point. In Figure 3.11a the smith chart with S_{11} and S_{22} is shown and from Figure 3.11b it can be seen that the 3 dB bandwidth of S_{21} is from 25.7 GHz to 32.4 GHz.

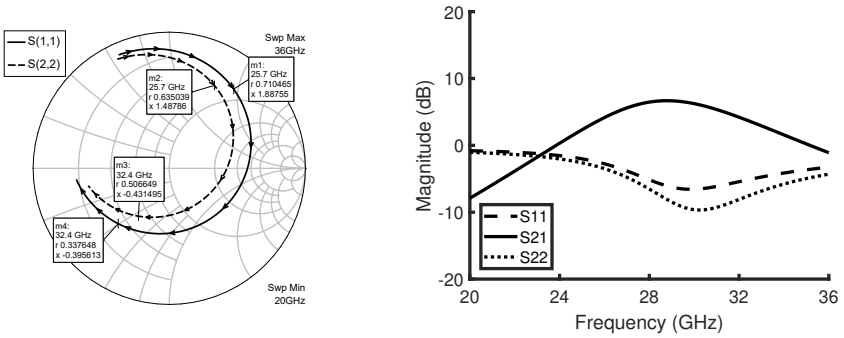


Figure 3.11: Differential CS class C (a) Smith chart S-parameters (b) S-parameter magnitudes

The single tone simulation results for the class C amplifier are found in Figure 3.12. The P_{out} vs. P_{in} curve can be seen in Figure 3.12a, P_{sat} is 16.4 dBm. Figure 3.12b shows the gain and PAE of the class C amplifier at 28 GHz. The maximum

power gain of the amplifier is 9.4 dB and the 1dB compression point is at 14.7 dBm output power. The maximum PAE is 41.8 % and the PAE at OCP_{1dB} is 40.4 %.

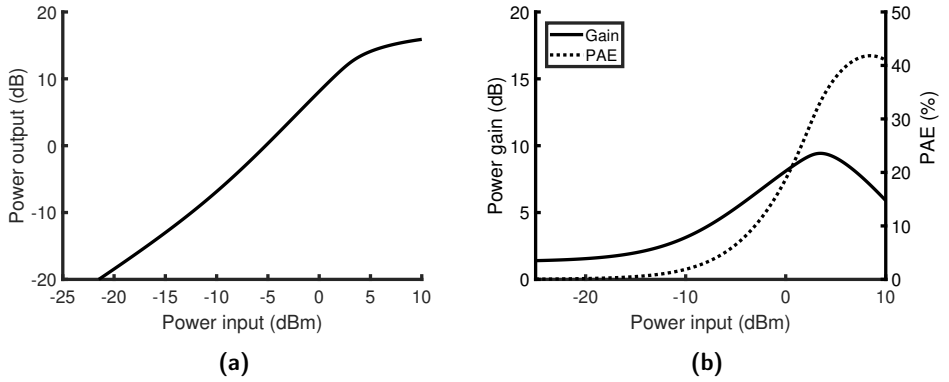


Figure 3.12: Differential CS class C (a) P_{out} vs. P_{in} at 28 GHz (b) Gain and PAE vs. input power at 28 GHz

The results, from two tone simulation with frequencies 28 GHz and 28.1 GHz, are shown in Figure 3.13 OIP_3 is at -1 dBm.

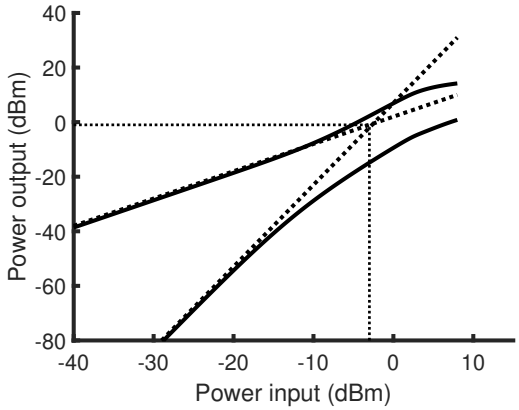


Figure 3.13: Differential CS class C IP3

3.3.2 Differential Cascode Topology Design

The general schematic used for the differential cascode topology can be seen in Figure 3.14. All amplifier classes share this schematic with variation in bias to get the desired conduction angle and matching to tune them for 28 GHz. To drive the differential cascode, a higher supply voltage is needed to reach the same output power compared to the differential CS, since, bias is shared between the CS and CG transistors. After simulations, it was found that the optimal supply voltage to maximize PAE while keeping the desired output power was 2.5 V for all amplifier

classes. However, the cascoded CG gate bias varies between the amplifier classes to match the compression points of both transistors in the cascode chain. All classes have 1000 nanowires in the CG and CS transistors, to balance the amplifier.

To secure stability for all frequencies, every amplifier class has capacitive cross coupling neutralisation like the CS differential amplifiers, albeit to a lesser degree due to the better built in stability of the cascode. The size of the diode coupled transistors was chosen individually for each amplifier class as a compromise between bandwidth, gain and PAE as they increase stability and gain at the cost of bandwidth.

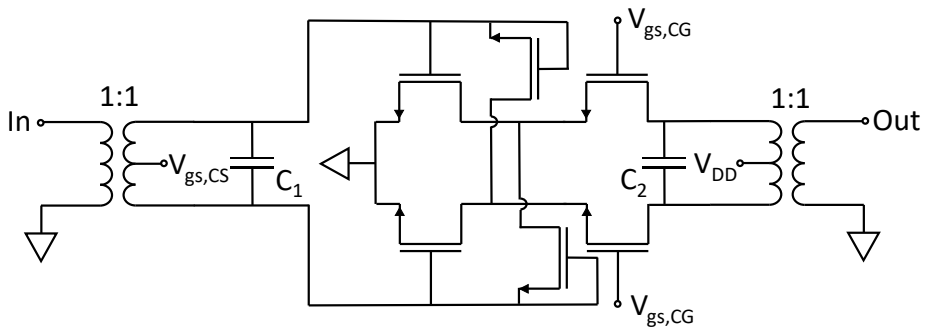


Figure 3.14: Differential cascode schematic

3.3.2.1 Class A differential cascode amplifier

A gate bias of 0.35 V was chosen for the CS transistors to ensure 2π conduction angle with high g_m. The CG gate bias was set to 1.3 V. To ensure stability, the amount of nanowires in the cross coupled transistors was set to 400 nanowires and for matching, the capacitances were set to $C_1 = 110$ fF and $C_2 = 156$ fF.

The small signal simulation results can be seen in Figure 3.15. Figure 3.15a shows a smith chart of the amplifier S_{11} and S_{22}. The S-parameter magnitudes can be seen in Figure 3.15b where S_{21} gives a 3 dB bandwidth between 25.2 GHz and 31.3 GHz.

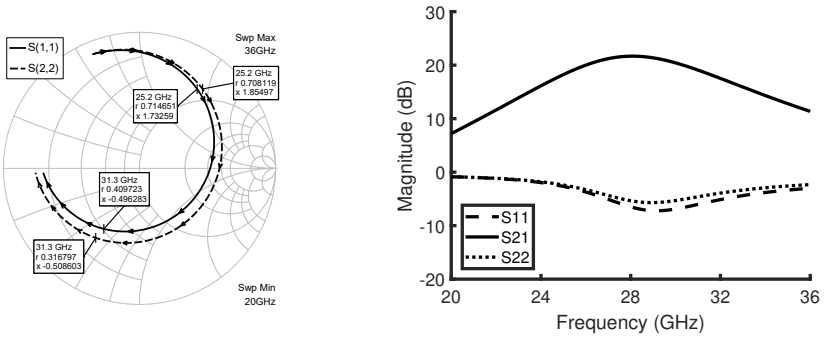


Figure 3.15: Differential cascode Class A (a) Smith chart S-parameters (b) S-parameter magnitudes

The single tone simulations for the class A amplifier at 28 GHz are found in Figure 3.16. The P_{out} with respect to P_{in} can be seen in Figure 3.16a, P_{sat} is 20 dBm. Figure 3.16b shows the power gain and PAE of the amplifier. The power gain of the amplifier is 21.66 dB with the OCP_{1dB} being reached at 17.4 dBm output. The maximum PAE of the amplifier is 38.9% with the PAE at OCP_{1dB} being 22.2%.

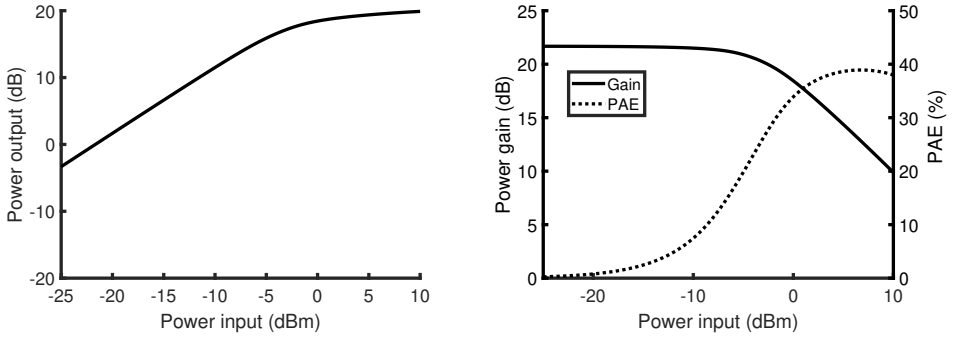


Figure 3.16: Differential cascode Class A (a) Pin vs. P_{out} at 28 GHz (b) Gain and PAE at 28 GHz

The two tone simulation results using frequencies 28 GHZ and 28.1 GHz, can be seen in Figure 3.17 where OIP_3 is extracted to 32 dBm.

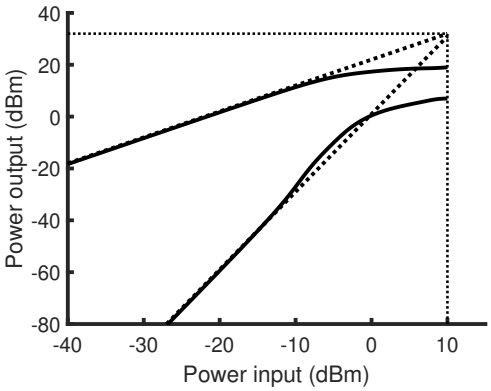
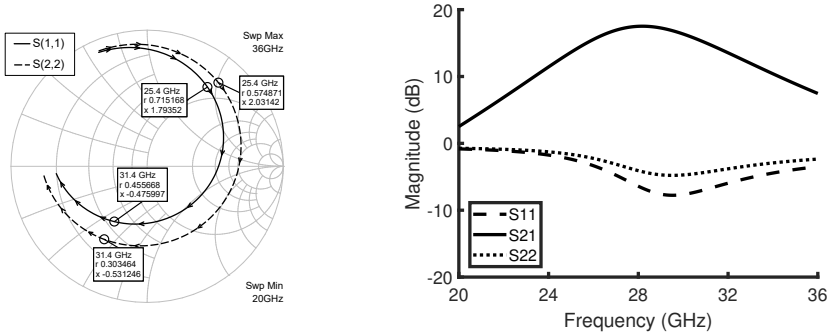


Figure 3.17: Differential cascode class A IP3

3.3.2.2 Class AB differential cascode amplifier

The CS gate bias was chosen to 0.2 V to get the desired conduction angle. The CG gate bias was set to 1.2 V for optimal PAE. The amount of nanowires of the cross-coupled transistors was set to 300 nanowires, and for matching the capacitances were set to $C_1 = 110$ fF and $C_2 = 152$ fF.

The small signal simulation results can be seen in Figure 3.18. Figure 3.18a shows the amplifier S_{11} and S_{22}. The magnitude of the S-parameters can be seen in Figure 3.18b where S_{21} gives a 3 dB bandwidth between 25.4 GHz and 31.4 GHz.



(a) **(b)**

Figure 3.18: Differential cascode Class AB (a) Smith chart S-parameters (b) S-parameter magnitudes

The 28 GHz single tone simulation results for the class AB amplifier are found in Figure 3.19. The P_{out} vs. P_{in} simulation can be seen in Figure 3.19a, giving a P_{sat} of 19.3 dBm. Figure 3.19b shows the power gain and PAE of the amplifier. The power gain of the amplifier is 17.5 dB with the OCP_{1dB} being reached at

16.3 dBm output. The maximum PAE of the amplifier is 40.5% with the PAE at OCP_{1dB} being 29.6%.

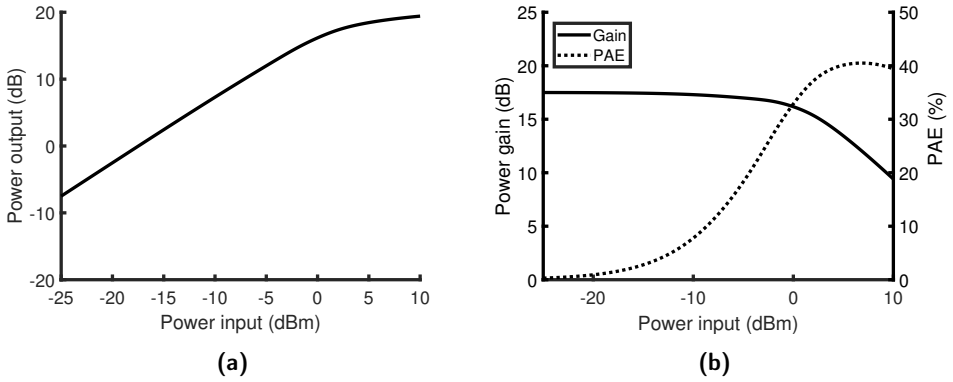


Figure 3.19: Differential cascode Class AB (a) P_{in} vs. P_{out} at 28 GHz (b) Gain and PAE at 28 GHz

The linearity simulation using two tones with frequencies 28 GHz and 28.1 GHZ can be seen in Figure 3.20 where the OIP_3 is extracted to 22 dBm.

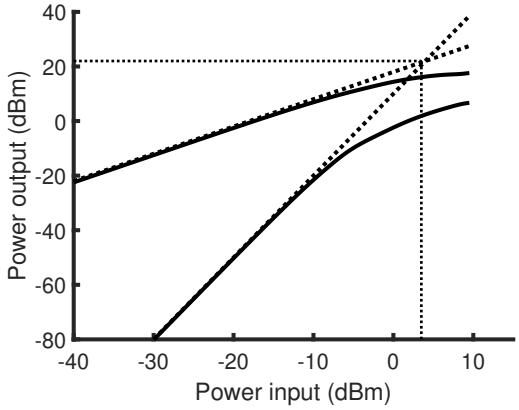


Figure 3.20: Differential cascode class AB IP3

3.3.2.3 Class C differential cascode amplifier

To achieve the desired conduction angle for a class C amplifier, the CS gate bias was placed well below threshold at 0 V. The gate bias of the CG was set to 1.2 V for optimum PAE. Stability was then ensured by setting the amount of nanowires in the cross coupled transistors to 400. For the matching capacitances were set to $C_1 = 110$ fF and $C_2 = 15$ fF.

Figure 3.21a shows S_{11} and S_{22} for the amplifier. The S-parameter magnitudes

can be seen in Figure 3.21b, from S_{21} the 3 dB bandwidth is found to be between 25.9 GHz and 31.9 GHz.

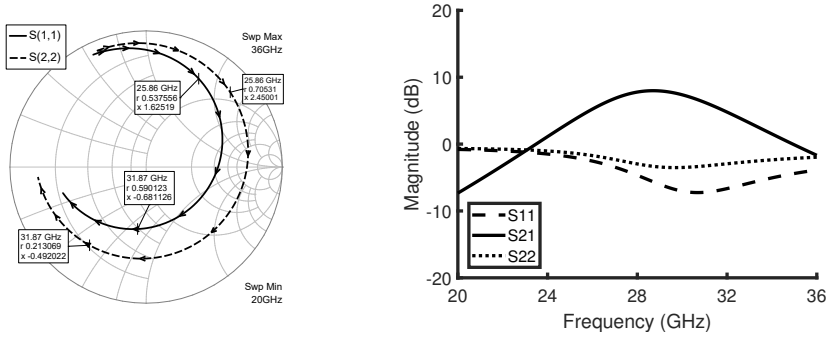


Figure 3.21: Differential cascode Class C (a) Smith chart S-parameters (b) S-parameter magnitudes

The single tone simulations at 28 GHz for the class C amplifier are found in Figure 3.22. The simulation for P_{out} can be seen in Figure 3.22a, P_{sat} is 19.1 dBm. Figure 3.22b shows the power gain and PAE of the amplifier. The maximum power gain of the amplifier is 11.1 dB with the OCP_{1dB} being reached at 19.1 dBm output. The maximum PAE of the amplifier is 40.9 % with the PAE at OCP_{1dB} being 40.8 %.

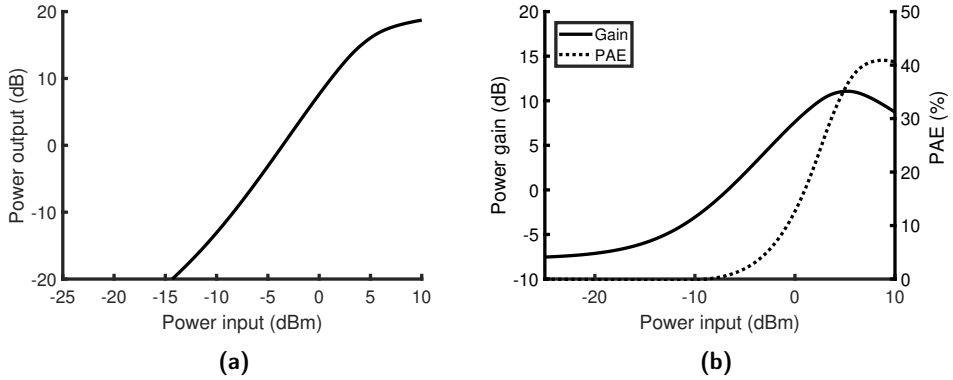


Figure 3.22: Differential cascode Class C (a) P_{in} vs. P_{out} at 28 GHz (b) Gain and PAE at 28 GHz

The two tone simulation with frequencies 28 GHz and 28.1 GHz, can be seen in Figure 3.23 where the OIP_3 is extracted to -9 dBm.

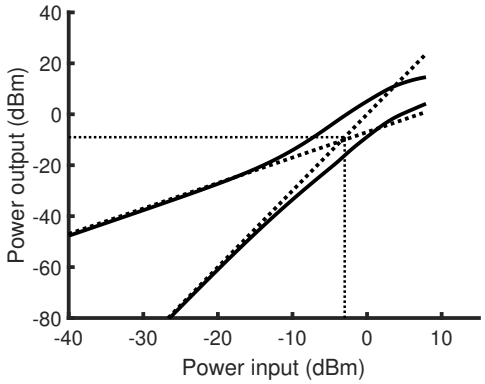


Figure 3.23: Differential cascode class C IP3

3.4 Comparison

With similar schematics and gate bias being the main variable, the results are close to what was expected. For both the CS and the cascoded topology, similar results between the amplifier classes were obtained and will be commented together. A comparison between the two topology implementations for each class will also be presented.

The class A amplifiers exhibit good linearity, OIP_3, and high gain, G, however, the efficiency, PAE, at OCP_{1dB} is low. The class AB amplifiers shows almost as much gain as class A and a slightly higher PAE at OCP_{1dB}, however, at the loss of linearity. The class C amplifiers have much lower gain and worse linearity but the PAE at OCP_{1dB} is higher.

The gain of the class C amplifier is clearly dependant on the power of the input signal. This is expected due to the low conduction angle. The class C amplifier relies on the input signal to raise gate bias and thus achieve gain. The trade-off between efficiency and linearity is obvious when comparing the class C amplifier with the other amplifier classes.

A comparison of the amplifier classes are shown in Table 3.1.

	G (dB)	BW (GHz)	PAE@CP1 (%)	OIP_3 (dBm)
CS class A	17.4	7.8	17.3	28
Casc. class A	21.7	6.1	22.2	32
CS class AB	15.9	7.3	26.9	25
Casc. class AB	17.5	6	29.6	22
CS class C	9.4	6.7	40.4	-1
Casc. class C	11.1	6.0	40.8	-9

Table 3.1: Comparision of Properties of the amplifiers

All the amplifier classes have shown their ability to deliver enough current to achieve the output power requirement of 15.4 dBm in the proposed Doherty topology. For the class A amplifiers, the cascoded topology shows significantly more gain, higher PAE at OCP_{1dB} and better linearity, while the CS have wider bandwidth. The cascoded class AB amplifier shows higher gain and PAE at OCP_{1dB}, the CS achieves wider bandwidth and better linearity. For the class C amplifiers, the cascoded have higher gain while, the CS have wider bandwidth and better linearity.

The choice of supply voltage and $V_{GS,CG}$ for optimal PAE seems to have degraded the cascode linearity. This can be explained by looking at the voltage over the transistors in the cascode chain. With the supply voltage chosen, the V_{DS} over the CG is 1.5 V and 1 V over the CS. Due to the DIBL effect this means that the threshold voltage of the cascode CS is higher than in the differential CS. This means that the cascode topology in this work is biased deeper in class AB and C which explains the lower linearity and higher PAE compared to the differential CS. This effect is not seen in class A since, the gate voltage is significantly higher than the threshold voltage.

The simulations of the CS generally show a wider bandwidth than the cascoded topology. The bandwidth is set by the Q-factor of the resonant circuit at the output according to

$$BW_{3dB} = \frac{f_0}{Q} \tag{3.2}$$

where f_0 is the center frequency and Q the quality factor. Considering a parallel resonant circuit at the output, the smallest resistance will determine the quality factor. This is either, the device small signal output resistance r_o or, the resistance of the transformer inductance. In case of the CS, r_o is much smaller and thus the device determines the bandwidth. For the cascode the output resistance is significantly higher due to two transistors being cascoded, thus the bandwidth is not determined by the device but the resistance of the transformer.

3.5 Doherty PA design

Two Doherty power amplifiers were designed, one using the differential common source topology and the other using the differential cascode topology. For each

Doherty design, two amplifiers are required, one main and one auxiliary. For the auxiliary, the linearity requirement is low and emphasis is on the efficiency. Based on the previously presented results, the class C is the better option. Regarding the main amplifier, the requirement is a more linear but still efficient amplifier. Both class A and AB are viable options where the former is the more linear choice and the latter is the more efficient. In our case, the goal is high PAE and thus the class AB was chosen as it showed better PAE and sufficent linearity.

The ratio between the main and auxiliary PA saturation current will affect at what output level the Doherty region will start. This was kept in mind when sizing the transistors. We aim for 9 dB back-off average power and thus the auxiliary amplifier should be larger than the main amplifier to supply more current [25]. The sizing was the same for both topologies at 1200 nanowires for the auxiliary amplifier and 600 nanowires for the main amplifier.

For both topologies, the input and output looks similar, the input is supplied through a 3 dB splitter followed by a 90° phase shift from the quarter wave (QW) transmission line at the auxiliary amplifier input. At the output, there is a 90° phase shift at the main amplifiers output to match the phase of the two amplifiers before combining the signal. At the output there is another transmission line for load transformation.

3.5.1 Differential Common Source

The schematic for the common source differential amplifier is shown in Figure 3.24. The sizing of the cross-coupled transistors are 100 nanowires for the main amplifier and 300 nanowires for the auxiliary amplifier. The capacitances are, $C_{1M} = 0.15$ fF, $C_{2M} = 0.11$ fF, $C_{1A} = 0.09$ fF and $C_{2A} = 0.04$ fF, to ensure 28 GHz resonance at both input and output. Gate bias are, for the main amplifier 0.2 V and for the auxiliary amplifier 0 V.

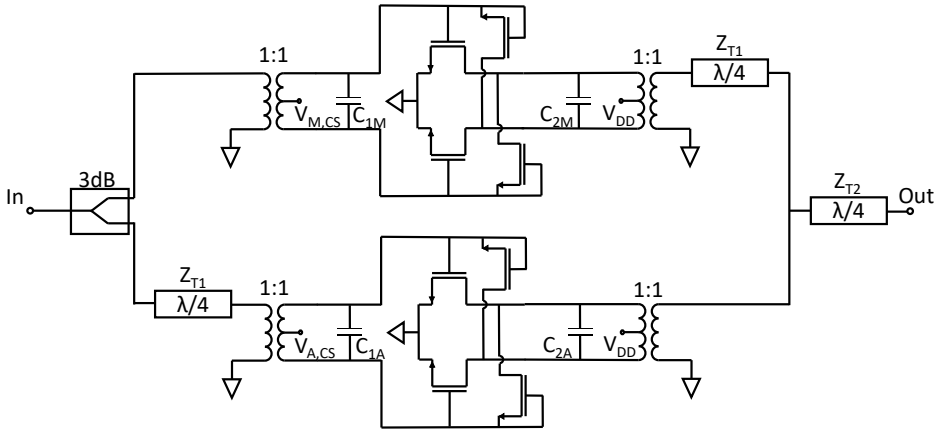
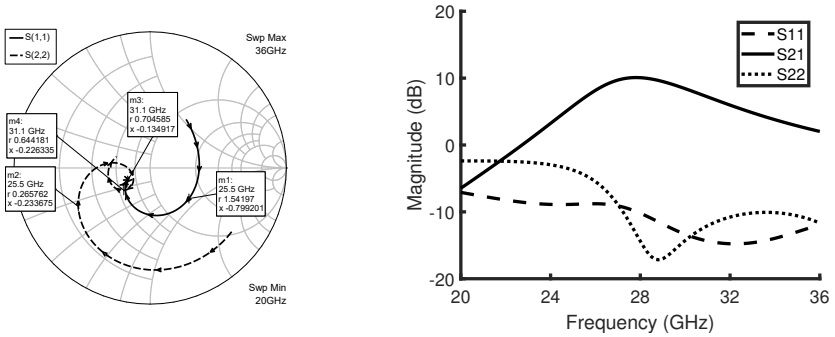


Figure 3.24: Schematic of the CS Doherty power amplifier

In figure 3.25b the frequency dependant gain and the bandwidth at 9 dB back-off is shown, the 3 dB bandwidth is from 25.5 GHz to 31.1 GHz.



(a) **(b)**

Figure 3.25: CS Doherty PA (a) Smith chart S-parameters (b) S-parameter magnitudes

The P_{out} vs. P_{in} curve can be seen in Figure 3.26a, showing P_{sat} equal to 19.7 dBm. In Figure 3.26b the gain and PAE of the amplifier is shown. The power gain of the amplifier is 9.9 dB with the OCP_{1dB} at 18.0 dBm output power. The PAE of the amplifier is 30.5% at P_{sat} and the PAE at 9 dB output power back off is 15.5%.

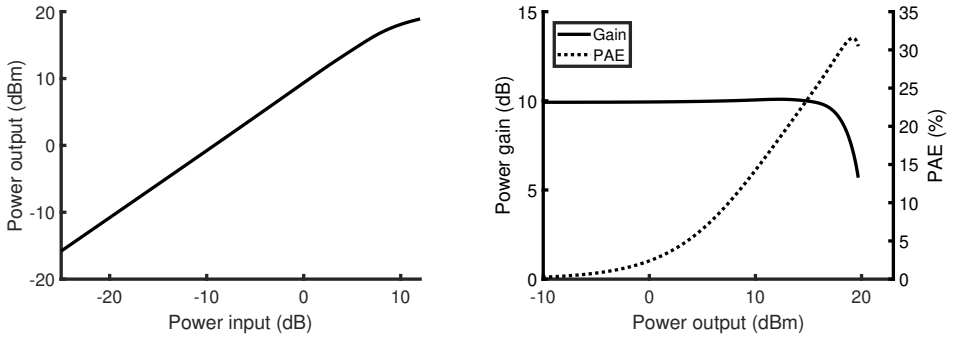


Figure 3.26: CS Doherty PA (a) P_{in} vs. P_{out} at 28 GHz (b) Gain and PAE at 28 GHz

In Figure 3.27 the linearity of the CS DPA is shown, the OIP_3 is found at 19 dBm.

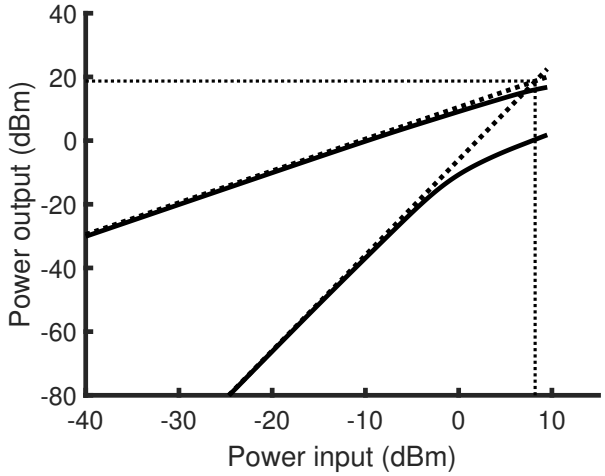


Figure 3.27: Two tone simulation of CS Doherty PA using 28 and 28.1 GHz

The modulated signal performance was simulated using a gray coded 64-QAM signal with 800 MHz BW and without OFDM. A root raised cosine (RRC) filter was used with $\alpha = 0.35$. The 64-QAM constellation diagram from simulations with 2048 symbols and EVM of 5.5 % is shown in Figure 3.28a. The PAE and EVM against P_{out} is shown in Figure 3.28b. The CS DPA achieves 23.3 % PAE and 14.8 dBm output power at 5.5 % EVM.

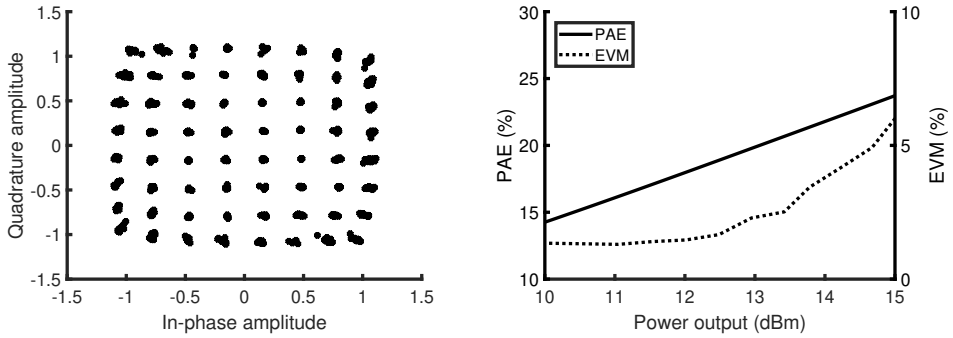


Figure 3.28: CS Doherty PA (a) 64-QAM constellation diagram (b) PAE and EVM vs. P_{out} at 28 GHz center frequency

3.5.2 Cascode

The schematic used for the differential cascode Doherty amplifier can be seen in Figure 3.29. The supply voltage, V_{DD}, was set to 2.5 V following previous testing. The different gate biases were set to $V_{M,CS} = 0.2$ V, $V_{M,CG} = 1.2$ V, $V_{A,CS} = 0$ V and $V_{A,CG} = 1.2$ V.

For matching, the capacitances were set to $C_{M1} = 0.142$ fF, $C_{M2} = 0.155$ fF, $C_{A1} = 0.095$ fF and $C_{A2} = 0.125$ fF. The cross-coupled transistors are not present in this design, since, simulations showed the amplifier to be stable without them. They could still be implemented to increase gain, however, this resulted in the bandwidth being reduced, which could not be sacrificed. The same sizing was kept between the CS and CG transistors for both the main and auxiliary amplifier, as it was found to give better bandwidth and load modulation while balancing the gain between the two amplifiers.

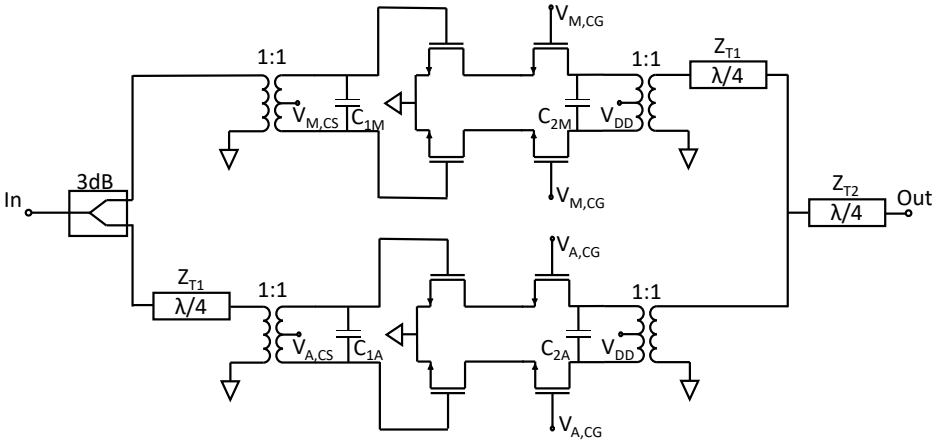
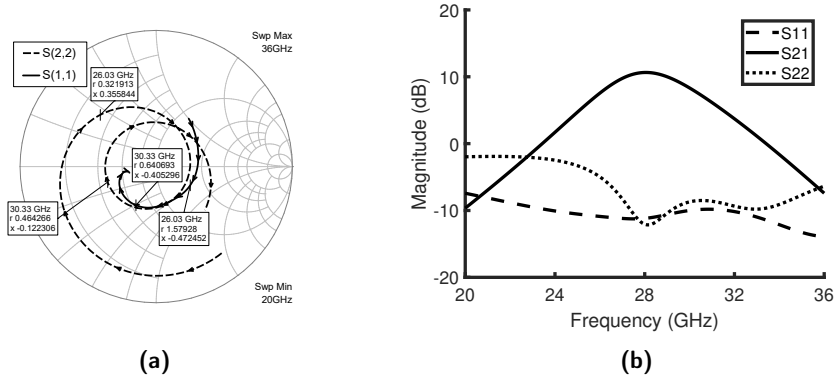


Figure 3.29: Schematic of the cascode Doherty power amplifier

The S-parameter simulations for the cascode DPA can be seen in Figure 3.30. A smith chart representation is found in Figure 3.30a while magnitudes are found in Figure 3.30b. From S_{21} in Figure 3.30b the 3 dB bandwidth is found to be between 26.0 and 30.3 GHz.



(a) **(b)**

Figure 3.30: Cascode Doherty PA (a) Smith chart S-parameters (b) S-parameter magnitudes

The single tone simulations can be seen in Figure 3.31. The P_{out} versus P_{in} simulations are found in Figure 3.31a, giving a P_{sat} of 21.2 dBm. The gain and PAE simulations are displayed in Figure 3.31b giving a gain of 10.6 dB and a OCP_1 of 19.9 dBm. The PAE is 28% at P_{sat} and 15.9% at 9 dB output power back-off.

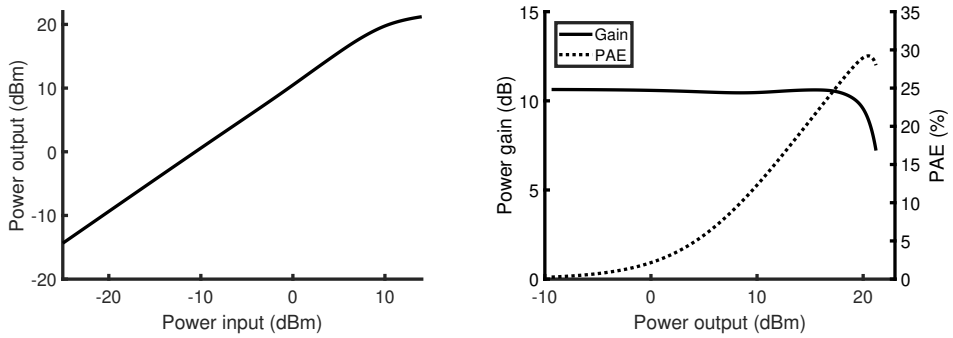


Figure 3.31: Cascode Doherty PA (a) P_{in} vs. P_{out} at 28 GHz (b) Gain and PAE vs P_{in} at 28 GHz

The two tone simulation using 28 GHz and 28.1 GHz for the cascode DPA can be seen in Figure 3.32 giving an OIP_3 of 17 dBm.

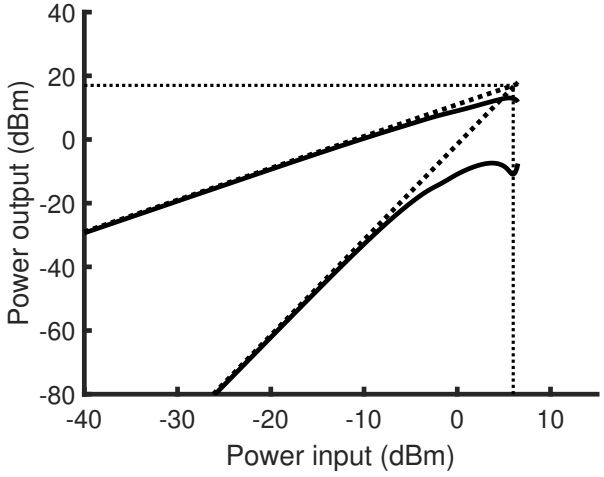


Figure 3.32: Two tone simulation of Cascode Doherty PA using 28 and 28.1 GHz

The modulated signal performance was simulated using gray coed 64-QAM signal with 800 MHz BW and without OFDM. A RRC filter was used with $\alpha = 0.35$. The 64-QAM constellation diagram from simulations with 2048 symbols and EVM of 5.5 % is shown in Figure 3.33a. The PAE and EVM against P_{out} is shown in Figure 3.33b, the cascode DPA achieves 24.5 % PAE and 17.1 dBm output power at 5.5 % EVM.

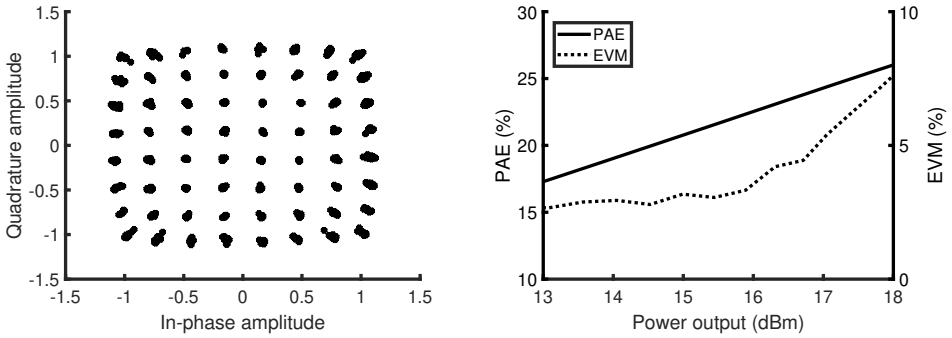


Figure 3.33: Cascode Doherty PA (a) 64-QAM constellation diagram (b) PAE and EVM vs. P_{out} at 28 GHz center frequency

3.5.3 Comparison

3.5.3.1 This work

Both topologies reached the specification of 15.4 dBm output power. When comparing the results from this work, the cascoded topology achieves higher P_{sat} and gain, while the CS achieves better $OIP3$ and bandwidth. Regarding PAE the results are comparable. The 64-QAM modulated signal simulations showed a higher output power and efficiency for the cascode topology at EVM = 5.5 %. A summary of the results of the DPA:s from this thesis can be seen in Table 3.2.

Also in the case of the DPAs, the cascoded topology is operating deeper in class AB and C. This causes worse linearity when looking at OIP_3 compared to the CS due to the DIBL-effect. The bandwidth is again determined by the device for the CS and by the resonant circuit at the output for the cascode.

The third order intermodulation of the cascode, however, exhibits IM_3 cancellation when the auxiliary amplifier turns on. One possibility is that the third order derivative of the transconductance, g_{m3}, of the main and auxiliary amplifiers cancel, due to their difference in V_{GS}, resulting in them being out of phase before combining. This is has previously been observed for DPAs [38]. The effect seems to be most prevalent around 28 GHz, which improves EVM around saturation, for carriers using this frequency. To see how the cancellation improves the EVM throughout the entire 5G frequency band would require further testing, preferably using many subcarriers.

The PAE at 9 dB back-off for both topologies was improved compared to their main amplifier which was the aim with the Doherty topology. However, the shape of the PAE curve does not show the characteristic Doherty peak in efficiency around the targeted back-off as can be seen in DPAs operating at lower frequencies. This is the case for most DPAs at mmWave frequencies.

The bandwidth of the DPA was reduced for both topologies which was expected since, the Doherty topology uses transmission lines to achieve the load modulation. When using transmission lines, the bandwidth is dependant on the operating frequency, this is a general problem with DPAs. There are various examples on how to improve the bandwidth of Doherty PAs using novel circuit designs [39], however this was beyond the scope of the thesis and was left for future work.

	Gain (dB)	BW (GHz)	PAE (%) @6dB/9dB	P_{sat} (dBm)	Mod. Sim. 64-QAM 5.5 % EVM
CS	9.9	5.6	21.2/15.5	19.7	14.8 dBm 23.3 % PAE
Casc.	10.6	4.3	21.1/15.9	21.2	17.1 dBm 24.5 % PAE

Table 3.2: Comparison of the Doherty amplifiers designed for this work

3.5.3.2 Other works

The results for the DPAs in this work can be seen in Table 3.3 compared with other Doherty PAs implemented in other technologies. Our Doherty power amplifiers show better linearity properties than other technologies, which means that the required back-off from saturated power can be small. With less back-off also good efficiency is achieved. However, the saturated output power is lower than some of the alternatives, especially GaAs and other bipolar devices can achieve higher output powers.

	CS/Cascoded (this work)**	[24]	[35]	[36]	[37]
Technology	In(Ga)As nanowire	130 nm SiGe	45nm SOI CMOS	E-mode 0.15 um GaAs	28nm bulk CMOS
Topology	Diff. CS/Cascode	Diff. CE	2-stack	2-stage 2-stack	Diff. 2-stage 2-stack
F_0 (GHz)	28	28(/37/39)	28	28	32
Supply (V)	1.5/2.5	1.5	2.4	4	1
Gain (dB)	9.9/10.6	18.2	10	12	22
Bandwidth	5.6/4.3	16.4	-	7.5	6
PAE@6dB (%)	21.2/21.1	13.9	28	29	9*
PAE@9dB (%)	15.5/15.9	-	20*	21*	-
$OCP_{1dB}(dBm)$	18.0/19.9	15.2	21.5	23*	16
P_{sat}	19.7/21.2	16.8	22.4	26	19.8
Modulated results Power (dBm) PAE (%)	64-QAM 5.5% EVM 14.8/17.1 23.3/24.5	64-QAM -27 dB 9.2 18.5 CE	64-QAM 5.5 % EVM 13 16.8	- - - -	64-QAM 5.5 % EVM 11.7 5.75

*Extracted from figures, **Simulated results

Table 3.3: Comparison between the DPAs designed for this work and other published DPA works

Chapter 4
Conclusions

In this Master's thesis, two Doherty power amplifiers using the differential common source and the cascode topology, have been designed and compared. The amplifiers were designed around the n257 frequency band, between 26.5 and 29.5 GHz, for 5G transmitters. The simulations throughout this work have been conducted using the AWR design environment with virtual source models of In(Ga)As nanowire transistors supplied by NordAmps.

The designed Doherty amplifiers used a class AB main amplifier and a class C auxiliary amplifier. Both Doherty amplifiers reached the output power goal and achieves improved back-off PAE when compared to the main amplifier. System simulations with 64-QAM signals show high output power and PAE at 5.5 % EVM. Linearity was good for both topologies. This contributed to the small back-off in order to meet the EVM requirements, which allows operation close to compression and thus achieving high PAE.

The main goal of this thesis was to design DPAs using vertical In(Ga)As nanowire transistors. However, in the designed DPAs there are also other components, e.g. transformers, which may have limited our ability to reach conclusions with regard to the transistor technology. Furthermore, choosing a simple topology limited this work, as novel and more complex designs have shown improvements upon the typical Doherty topology.

To conclude, it has been possible to achieve the goal of the thesis, designing two efficient Doherty PAs. The simulation results from this thesis suggests, that the technology used could achieve exceptional output power and PAE at 5.5 % EVM.

4.1 Future work

Even though we have achieved to goal of this thesis there are multiple areas of interest to look further into. Future work may include the following:

- Both topologies in this thesis have resulted in a Doherty amplifiers with low gain, therefore requiring a high input power to reach the saturated output power. It would be desirable to have a gain of at least 15 dB, since, the

input signal strength often is low. To achieve this a driver stage could be implemented to the Doherty topology.

- The Doherty amplifiers showed reduced bandwidth, which is expected for the topology. There are alternative Doherty implementations which show increased bandwidth over the one used for this thesis. However, this was beyond the scope of the thesis but could be further explored [39].
- Performing Monte-Carlo simulations for process variation and also manufacturing the DPAs for verification measurements would be interesting to better benchmark the design. Due to time constraints it was not possible in the scope of this thesis.
- Further simulations using 64-QAM OFDM modulated signals would be of interest, as it would better benchmark the amplifiers for 5G operation. Within the time frame of the thesis this was not possible, so it is left for future work.

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Chapter 5
Appendix

5.1 Transformer

In this work the transformer model used are presented below. It is based on the previous work from [40]. The model have one path for the DC biasing, which is separated with and inductive RF-choke, and one for the RF signals.

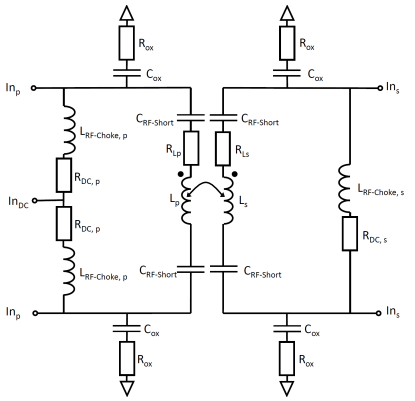

Figure 5.1: Schematic of the transformer

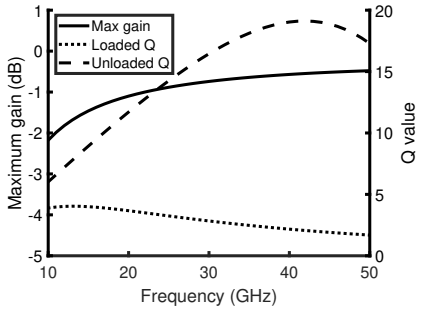

Figure 5.2: Maximum gain and Q values for the transformer

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