Nanowire based mm-wave LNA and switch design

for 5G & Satellite Communications

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Master's Thesis

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By

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Abstract

In this work, two LNAs operating at a frequency around 83 GHz and 110 GHz, for satellite- and 5G applications respectively, have been designed, using vertical InGaAs nanowire transistors. In addition, a switch operating at a frequency around 110 GHz has been designed. The topology has consisted of a common source as a first stage, and a cascode as a second stage. The design and simulations of the design have been performed in National Instruments (NI) AWR. The results from the simulations of the 5G LNA show a noise figure less than of 2.6 dB for a bandwidth of 16.4 GHz from 103.6 to 120.0 GHz with a peak gain of 24.5 dB. For the satellite LNA, the noise figure is less than 2.8 dB and the gain is more than 21.8 dB for the full uplink E-band from 81 to 86 GHz, and achieves a total 3-dB bandwidth of 8 GHz, with a peak gain of 23.2 dB. The transmitter to receiver isolation of the switch is more than 22 dB and the insertion loss less than 2.2 dB from 97.5 to 120.0 GHz.

Popular Science Summary

Today, more and more people use internet, and it is just not the number of internet users that is rapidly changing. People use it for more things now than just to search for information, as was the main use of internet for a long time. Today, wireless internet with high data speed finds applications in various things such as self-driving cars and sensors that monitors people, agriculture, and forests. To achieve the high data speeds necessary for these tasks, the frequency of operation have to increase, but this requires transistors with good high frequency characteristics. Transistors can be made from Indium-Gallium-Arsenide nanowires that operates at these high frequencies. For the receiver to be able to function properly, a switch must guide the received signals to the right low noise amplifier. The low noise amplifier then amplifies the signals without adding to much noise. Both the switch and the receiver are generally more difficult to design the higher frequencies they operate. In addition, the linearity performance has to be good enough, while the power consumption cannot be too high, otherwise the batteries will be drained to fast. This can be accomplished by selecting the right bias point for the transistors, match the transistors to the right passive elements etc.

Acknowledgments

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Andreas Grenmyr

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CHAPTER 1

1 Introduction

1.1 Concept

For the upcoming fifth-generation mobile communication systems, there is a desire to be able to transmit large amounts of information from base stations that are connected to many users. Sometimes, this concerns base-stations that are not connected to other base stations through optic cables and therefore wireless transmission of information is the only option. At higher frequencies, there is significant potential to increase the data transfer speed. One frequency band is the D-band (around 110 GHz). This is largely due to the relatively low atmospheric absorption at these frequencies [1]. On the other hand, base stations far out in rural areas that are neither connected to other base stations through optic cables, nor are in proximity to other base stations for efficient wireless transmission, could use satellite communication instead. For this purpose, the E-band (from 81 GHz to 86 GHz), which possesses large amounts of available bandwidth, is an interesting option to use [2]. The design at these frequencies requires high performance and high frequency device and circuit environment. One such example is vertical InGaAs nanowire MOSFETs, that can provide excellent RF characteristics at mm-wave frequencies. One reason is that they can achieve large g_m and low intrinsic capacitances at short channel lengths [3]. This thesis will focus on designing and evaluating performance of E-band and D-band low noise amplifiers and radio-frequency (RF) switches, using vertical nanowires MOSFFETs. As vertical nanowires are a feasible option for future high frequency device implementation, this work is of interest from circuit performance aspects, as it demonstrates the current technology limit. Therefore, it could be a feasible option to use models of these transistors in the design of the low noise amplifiers and switches.

1.1.1 Wireless communication systems

In modern communication systems, in order to increase the amount of information sent or received, the digital information is converted into high-frequency analog signals that propagate in free space. These modulated signals that a receiver antenna receives must be amplified before they can be efficiently processed by different receiver stages. The initial signal amplification is done by a circuit called a low noise amplifier (LNA). The LNA operation ensures that signal is amplified, while minimum amounts of noise is added to it. The term signal to noise ratio (SNR) is used to describe the ratio between the power of the signal to the power of the noise and should be as large as possible, the noise factor (F) and noise figure (NF) are given by equation [4]:

$$F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \qquad (1a)$$

$$NF = 10 \log F \qquad (1b)$$

where $S_{in/out}$ and $NF_{in/out}$ are the power of the signal and the noise at the circuit input/output, respectively. The noise figure can therefore be described as the degradation of the signal to noise ratio between the input and output. Therefore, the characteristics of the LNA are of huge importance in maintaining good SNR, as its purpose is to amplify the signal without introducing to much noise [4].

The LNA is the first active stage in a receiver, after the antenna and switch. The antenna is the element receiving the electromagnetic wave and transforming it into a current and voltage wave which continues into the receiver as seen in figure 1. The switch after the antenna selects where the signal path will go, and if the LNA is active, the signal continues there. The total system noise figure is described by Friis formula [4]:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \qquad (2)$$

where $F_n$and G_n are the noise factor and gain of the nth stage [4]. For the case of the receiver, the LNA is the first stage, followed by the mixer that is the second stage, then comes the third stage, the transimpedance amplifier, and so forth. From this formula, we see that it is crucial that the LNA needs

a high gain and low noise figure in order to supress the noise of the succeeding stages. The stages are relatively noisy and includes a mixer, that down converts the signal to an intermediate frequency (IF) by using a local oscillator, and a demodulator that demodulates the IF signal and retrieves the information stored in the signal. These steps are outlined in Fig. 1. In Fig. 1, RX is the receiver, DR is the dynamic range, and BER is the bit error rate of the analog-to-digital converter.

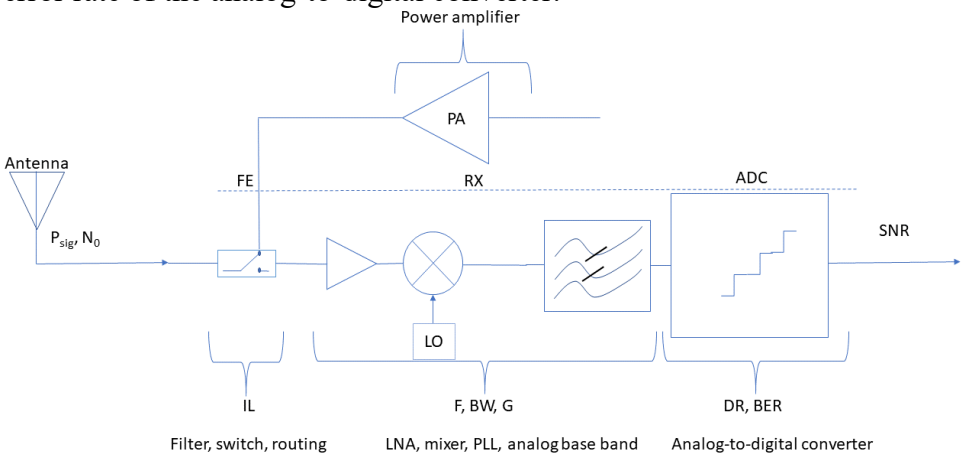

Figure 1: Schematic of a receiver. Each stage deteriorates the SNR.

The date rate that is transferred is not only limited by the SNR of the signal when it has reached the demodulator but also the number of channels and the bandwidth of the individual channels limits the data rate [5]. Both are, in turn, limited by the total bandwidth of the full receiver, which is initially set by the bandwidth of the RF stage, namely the LNA. Since there is more bandwidth available at higher frequencies, there is a demand to increase the frequencies of the carrier signal. For example, the frequencies of the upcoming fifth generation of wireless communication technologies have thus far been determined to include frequency bands of up to at least 40 GHz [6].

The receiver sensitivity is defined as the minimum signal power required for the receiver to be able to demodulate it correctly without that too much information is lost (normally around 95% of the transmitted data). Some challenges with increasing the frequency of operation are the increased atmospheric absorption at mm-wave frequencies which results in a demand for increased transmitting power and/or a demand for improved receiver sensitivity. Alternatively, the problem could be addressed by increasing the number of base stations. Other challenges for operation at mm-wave

frequencies include difficulties in providing enough gain in amplifiers, since, the frequency of operation of active devices is closer to the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}), i.e. the frequency where the maximum current- or power gain is unity, respectively. Also, a problem specifically for the receivers is that the noise figure increases with the frequency of operation, mainly due to increase in losses in transistors.

1.1.2 Active components – transistors

A transistor can be described as a three-terminal device. For a metal-oxide-field-effect-transistor (MOSFET) the third terminal, the gate, controls the current flow between remaining two terminals (drain and source), as shown in Fig.2. The gate is capacitively coupled and introduces an energy band shift in the semiconductor channel opposite to the gate, with a thin insulating oxide in between which enables this capacitive coupling. When the energy barrier is lowered, charge carriers can travel from source to drain, when a voltage bias between these terminals is applied. The amplification in MOSFETs amplifier is designed for a small voltage shift in the gate to cause a relatively large shift in the drain-source current.

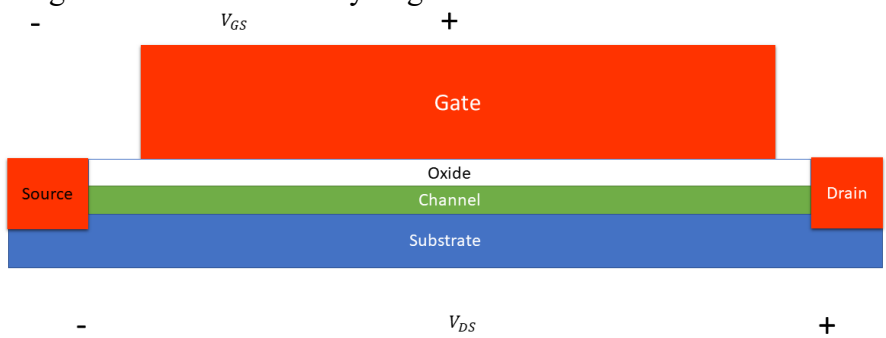

Figure 2: Picture of a traditional planar MOSFET.

The characteristics of the transistors define the LNA performance. For a transistor to be able to operate at high frequencies, the channel length (L_C) needs to be short, while the speed of the carriers (v_c) needs to be large, as given by [7]:

$$transit\ time, t = \frac{channel\ length,\ \ L_C}{carrier\ velocity, v_c} \qquad (3a)$$

$$v_c = \mu E, \qquad (3b)$$

where v_c is the carrier velocity, L_C is the channel length, t is the transit time, the time needed for the charge carriers to be swept from the source to the drain, μ is mobility, E is the electric field between source and drain, and

$$E = \frac{V_{DS}}{L_c} \qquad (3c)$$

where V_{DS} is the voltage between drain and source. If v_c in (3a) is substituted by (3b) and (3c), (3a) can be rewritten as:

$$t = \frac{L_c^2}{\mu V_{DS}} \qquad (3d)$$

From $(3d)$, because t is proportional to the square of the channel length, it can be seen that reducing the channel length and increasing the carrier mobility greatly improves the transit time from source to drain, hence improving the cut-off frequency. Although, the small channel effect velocity saturation causes the velocity to be independent on the electric field, and thereby the transit time becomes only proportionate to the channel length.

However, if the gate length reduces, then the impact of the drain potential on the channel increases which can result in drain induced barrier lowering, (DIBL). This is unwanted, because it makes the transistor more difficult to switch off at high drain bias. One way to improve the electrostatics of the transistor is to have the gate-all-around (GAA) structure. This can be accomplished if the channel is made of a nanowire around which a gate is wrapped. Aside from superior electrostatic control, nanowires are a cost-effective way of using high mobility materials, such as Indium Gallium Arsenide, InGaAs, as a channel material, thus improving carrier velocity, and as a result, the high frequency operation. In Fig. 3a, a SEM image of a vertical InGaAs nanowire MOSFET is shown, which reveals that one MOSFET typically consists of many nanowires, and an illustration of the basic structure of a nanowire MOSFET with gate, source and drain as contacts is shown in Fig. 3b.

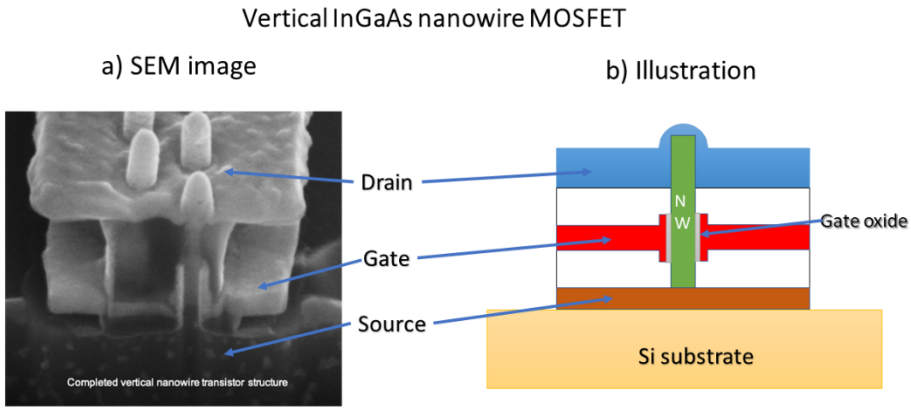

Figure 3: a) SEM image of a vertical nanowire MOSFET, and in b) is an illustration of the basic structure of the MOSFET in a).

1.2 Thesis contributions

The aforementioned discussion shows the need for the design of an LNA with acceptable NF and gain but operating at very high frequencies and with a large total bandwidth. This thesis is contributing with insight of how to design an LNA together with an antenna switch for 5G or 6G applications at frequencies around 110 GHz and also how to design an LNA for satellite communication applications at up-link frequencies around the new satellite band at 83 GHz. Vertical InGaAs nanowire transistors will be used for all circuits. Because of the excellent RF characteristics of nanowire transistors, this gives an opportunity to design high frequency receiver circuits with improved performance compared to current state-of-the-art.

CHAPTER 2

2: Theory

2.1 S-parameters. Gain, Noise

High frequency current and voltage waves can also be seen as power waves. The relation between incident and reflecting power waves can be described by scattering parameters (S-parameters), as shown in Fig. 4. The values of reflection (S_{11}, S_{22}) and transmission (S_{12}, S_{21}) parameters in a 2-port network describes gain, stability/feedback and how well a network is matched to a reference impedance. This makes S-parameters very powerful in evaluating device and circuit performance and allows for a direct conversion to impedance values [4].

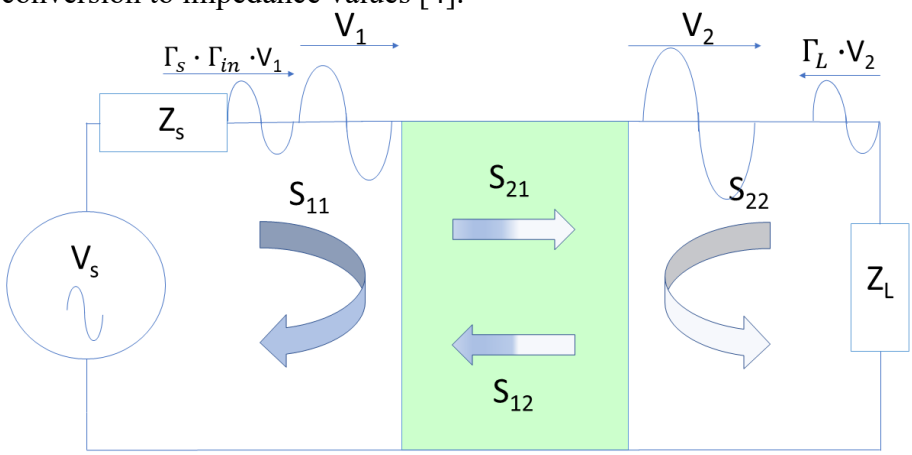

Figure 4: S-parameters and the source and load reflection coefficients Γ_s and Γ_L respectively. Z_S and Z_L are the source and load impedance and V_1 and V_2 are the incoming and outgoing voltage wave, respectively.

There are many ways S-parameters can be utilized. For example, the reflection parameters describe how good the matching is, where a low value is indicating a good match. [8]. A good match with the lowest possible value of the reflection S-parameters is achieved through having the load impedance the complex conjugate of the input impedance [4]. This condition is called simultaneous conjugate match. Figure 4 illustrates the S-parameters, as well as the source- and load reflection coefficient, Γ_s and Γ_L. The reflection coefficient is defined as the ratio between the incident

voltage wave, and the reflected voltage wave. If conjugate matched, then $\Gamma_s = \Gamma_{in}^*$ and $\Gamma_L = \Gamma_{out}^*$, where Γ_{in} and Γ_{out} are the reflection coefficients at the input and output of the 2-port network, respectively. This results in cancellation of the reflecting waves, and no power is reflected at the device.

The transmission S-parameters define gain (isolation) of the 2-port network. There are several gain expressions exploited in this thesis, from which following two are selected: [4]

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{|S_{21}|^2\left(1 - {\Gamma_S}^2\right)}{|1 - S_{11}\Gamma_S|^2(1 - |\Gamma_{out}|^2)} \qquad (4a)$$

$$G_T = \frac{P_L}{P_{avs}} = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|^2}\frac{|S_{21}|^2(1 - |\Gamma_L|^2)}{|1 - \Gamma_{out}\Gamma_L|^2} \qquad (4b)$$

Where G_A is the available power gain and G_T is the transducer power gain. The available power gain is defined as a ratio between power available from the network to power available from the source. The transducer power gain is defined as the ratio between power available at load to power available from the source. The expressions in Eq. 4a and 4b are equal in case of simultaneous conjugate match. Additionally, gain values for a specific Γ can be plotted in a complex impedance plane, or Smith Chart. For a specific set of Γ there is a constant available gain circle, as shown in Fig. 5 [4].

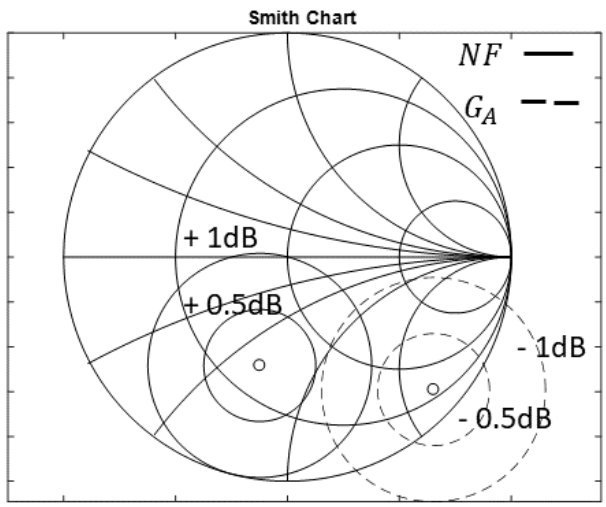

Figure 5: Smith Chart with available gain and noise figure circles.

Fig. 5 also shows a noise circle given for a specific reflection coefficient. In general, all the noise from a 2-port network can be summarized into just one ideal voltage and current source, as shown in Fig. 6, while the rest of the 2-port network is noiseless. This voltage source models all the corresponding noise at the output when the input is short circuited, while the current source models all the corresponding noise at the output when the input is open. For all other cases, both sources at the input are necessary to model the noise generated in the circuit [9].

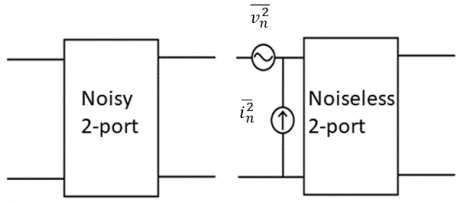

Figure 6: Noisy general 2-port network and a noiseless 2-port network circuit with equivalent input-referred noise sources.

Using input-referred noise sources, $\overline{v_n^2}$ and $\overline{i_n^2}$, the total noise factor is [9]:

$$F = 1 + \frac{\left(\overline{v_n^2} + |Z_s|^2\overline{i_n^2} + 2\mathrm{Re}(\overline{v_n i_n^*}Z_s^*)\right)}{4k_B T R_s} \qquad (5)$$

where $Z_s = R_s + jX_s$ is the source impedance, k_B is Boltzmann constant, and T is temperature. Using this formula, an optimum value of the source impedance that corresponds to a minimum value of the noise factor, and thereby the noise figure can be derived. This means that the source can be matched for an optimum noise figure. An equation describing how the noise factor increases if the source is not matched for an optimum noise figure is given by:

$$F = F_{min} + \frac{4R_n}{Z_0}\frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{(1 - |\Gamma_s|^2)\left|1 + \Gamma_{opt}\right|^2} \qquad (6)$$

where R_n is the resistance corresponding to a resistance with a thermal noise equal to $\overline{v_n^2}$, Z_0 is the characteristic impedance (usually 50 Ω), Γ_S is the reflection coefficient at the source, F_{min}, is the minimum noise factor when the source is matched for optimum noise, and, Γ_{opt} is the reflection coefficient for minimum noise figure [9].When looking at the Smith Chart showing the value of Γ_S, a constant value for noise figure is given by a circle around the value of Γ_{opt} as seen in Fig. 5.

The equivalent voltage source, $\overline{v_n^2}$, corresponding to the thermal noise generated by a resistor with a resistance, R, is given by:

$$\overline{v_n^2} = 4k_B TBR \qquad (7)$$

where B is the bandwidth. The thermal noise originates from the random distribution of thermal energy for different charge carriers. The origin of many noise sources in a transistor can be explained by thermal noise [10], and for short channel MOSFETs, the channel thermal noise is most significant [11]. Other noise sources for MOSFETs include shot noise from the gate leakage current and flicker noise from charge trapping defects at low frequencies [10].

For low noise amplifiers, there is a figure of merit (FOM) that concludes how good a LNA is in general, by considering its performance in terms of noise, gain, bandwidth and power consumption [4]:

$$FOM = \frac{G \cdot B[GHz]}{(F-1) \cdot P_{dc}[mW]} \qquad (8)$$

Where G, is the gain, B is the bandwidth, F is the noise factor, and P_{dc} is the power consumption of the LNA.

2.2 Linearity and Stability

Linearity is an important property of the LNA. A good linearity for the amplifier means that if it can be driven with a large-magnitude signal without affecting the small signal gain or result in significant intermodulation products. The distortion that is the most critical for an LNA is the third order intermodulation products, IM_3. The third order intermodulation products have the frequencies $2f_1 - f_2$ and $2f_2 - f_1$ where f_1 and f_2 are the frequencies of two input signals, as seen in Fig. 7. Harmonics and other intermodulation products, such as the second order intermodulation products, generally have frequencies further from the frequency band of interest, therefore this distortion is not considered critical.

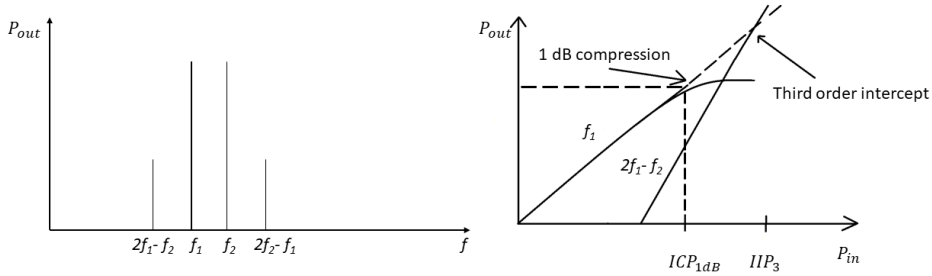

Figure 7: The location of the intermodulation products with respect to the fundamental tones (left) and the location for the 1dB compression point and third order intercept point for two signal sources with frequencies f_1 and f_2 (right).

Two important performance metrics when it comes to linearity for the LNA are the 1 dB-compression point and the third order intercept point (IP_3). The 1 dB-compression point is occurring when the input signal power has reached a high enough value so that the gain has been reduced by 1dB. The third order intercept point is when the third order intermodulation products would have the same amplitude as the desired output signal if no gain compression would occur. [4] In Fig. 7, the 1dB compression point and third order intercept point is illustrated. The input referred 1 dB compression point, ICP_{1dB}, is defined as the input signal power for which the gain has been lowered by 1dB. The input referred third order intercept point, IIP_3, is the input power where the extrapolated signal power and extrapolated third order intermodulation products power intercept [10]. The intercept occurs because the power of the third order intermodulation products increase faster with increasing input power than the output power of the signal, which can be explained by intermodulation products being a product of the interfering signals.

Stability is an important parameter for the LNA. All transistors and amplifiers have some amount of feedback. This means that the amplifier can potentially oscillate for certain load and/or source impedances if it is not designed to be unconditionally stable. The S-parameters can be used to calculate the stability factor, k, according to [4]:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1 \qquad (9)$$

where Δ is the determinant of the 2×2 S-parameter matrix. For the circuit to be unconditionally stable, k >1, |Δ|<1. In a multi-stage circuit design, it is

not enough to check that the whole circuit has a k>1, but each individual stage must also have k>1 [4].

2.3: Modulation techniques and Link Budget

The information is stored in the signal by modulating the signal waveform. This can be done through different types of modulation, but one modulation technique is quadrature amplitude modulation, QAM. In this technique, both amplitude and phase shift are used to modulate the signal. There are different types of QAM depending on how many bits of information each symbol contains. The more bits that can be represented by one symbol, the faster the data speed becomes. One downside though with having more symbols in the constellation diagram is that the required SNR, becomes higher and thereby the requirements on the performance of the LNA increases [4].

The minimum required SNR, furthermore, together with the bandwidth, noise figure of the receiver and temperature, corresponds to a minimum required input power to the receiver, the receiver sensitivity. The input power to the receiver is affected by the distance between the receiver and the transmitter, the performance of the receiving and transmitting antennas, absorption of the signal by the atmosphere and the output power of the transmitter. The equation for calculating the requirements of the noise figure for the receiver, and output power for the transmitter, involving the addressed variables, is called a Link Budget [12].

2.4: Transformers

A transformer is made up of two inductors that are in proximity to each other. Because of their magnetic coupling, the transformer will block DC signal, but AC signal will be transmitted. A transformer can be used to transform a single ended circuit to a differential circuit, for impedance transformation or as an added inductive component that will resonate with the rest of the circuit. It is possible to model the transformer into a lumped circuit model [13]. Fig. 8 shows circuit schematic of a transformer, where Z_{In} is the input impedance, Z_{Out} is the output impedance, L_1 , L_2 is the inductance of the two inductors respectively and k is the coupling coefficient between the two inductors. The coupling coefficient is computed from the ratio of the actual magnetic coupling to the maximum magnetic coupling [13].

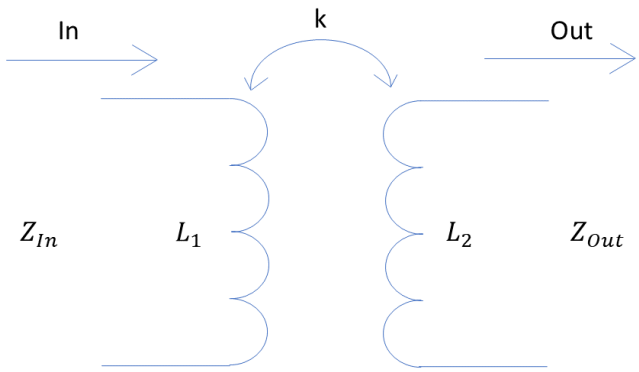

Figure 8: Circuit schematic of a transformer.

A real transformer is not an ideal element. It has ohmic losses caused primarily by the skin effect at high frequencies, while dielectric losses are the reason for conductive loss. There are also parasitic capacitances, which originate mainly from the capacitance between the two inductive metal sheets and between the inductive metal sheets and the ground plane [13].

2.5: RF switches

An RF switch, much like a regular switch, is a device that has two states, it is either in on-state and passes the input RF signal to the output, or it is in off-state and is blocking the input RF signal. For a switch in the on-state, the most critical parameter is the insertion loss. Insertion loss can be described as the ability of the switch to transfer the signal from the input to the output without losses. Lower insertion loss indicates better performance. For a switch in the off-state, the most relevant parameter is the isolation. Isolation is related to the ability of the switch to block the signal, and higher isolation demonstrates better performance. In general, a switch is realized as a MOSFET device, which, in essence is a high-frequency performance switch. A transistor with infinitely high ratio between the on-impedance and off-impedance constitutes an ideal transistor for a switch. A switch can for example be a shunt switch, a series switch or both [14]. In Fig. 9a, 9b, a series switch and a shunt switch are described, respectively.

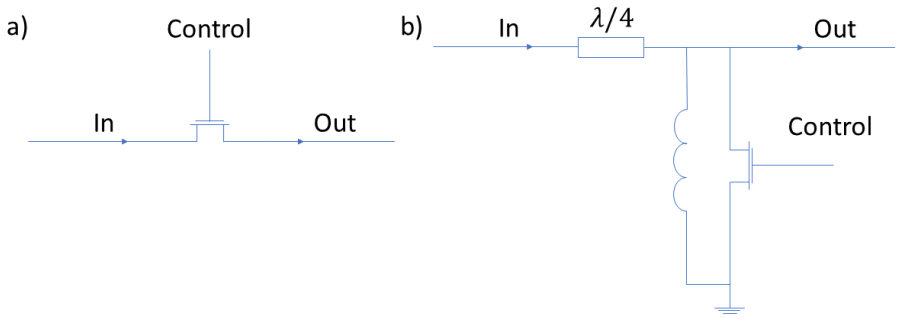

Figure 9: The series switch, a), and the shunt switch, b).

In a series switch, when the switch is turned on, so does the transistor and when the switch is turned off, the transistor is turned off as well. In a shunt switch, the opposite applies were the transistors are always in the opposite state compared to the switch. In a shunt switch it is important that there is an inductive element in resonance with the shunted transistor at the frequencies of interest, to resonate transistor parasitic capacitance and mitigate leakage of the RF signal to ground when the transistor is turned off. In a shunt switch, it is a good idea to use a quarter wavelength transmission line before the shunted transistor so that when the switch is in the off state, and the transistors are on, the signal sees a large real input impedance and when the switch is in the on state, and the transistors are off, it will see a small real input impedance [14].

For a shunt switch with transmission lines and a resonating inductive element, the insertion loss, $S_{21_{ON}}$, and isolation, $S_{21_{OFF}}$ and ratio between insertion loss and isolation $D_{ON/_{OFF}}$, can be approximately calculated using [14]:

$$S_{21_{ON}}(R_{ON}, Z_{int}) \approx \frac{1+\frac{R_{ON}}{Z_{int}}}{1+\frac{3R_{ON}}{2Z_{int}}}, R_{ON} \ll R_{OFF} \qquad (10a)$$

$$S_{21_{OFF}}(R_{ON}, Z_{int}) \approx \left(\frac{3}{2}+\frac{Z_{int}}{R_{ON}}\right)^{-1}, R_{ON} \ll R_{OFF} \qquad (10b)$$

$$D_{ON/_{OFF}}(R_{ON}, Z_{int}) \approx 1+\frac{Z_{int}}{R_{ON}}, Z_{int} \ll R_{OFF} \qquad (10c)$$

Where R_{ON} is the on-state resistance of a transistor, Z_{int} is the characteristic impedance of the transmission lines and R_{OFF} is the off-state resistance of a transistor. Furthermore, Eq. 10c shows that if the quarter wave transmission

line has a characteristic impedance of more than 50 Ω, this will result in a larger ratio between the insertion loss, and isolation.

2.6: MOSFET modelling

One way to model a transistor is by using the virtual source model [15]. The virtual source model is adapted to include quasi-ballistic transport. A quasi-ballistic transistor is a transistor where the carriers can travel through the transistor channel without scattering, which means that the mean free path for the electrons in the channel is longer than the channel length. In a quasi-ballistic case, some fraction, T, of the carriers is passing through the transistor while the other is being reflected back to the source or scattered in the channel. The current through a transistor in the virtual source model is therefore described by [15]:

$$I_D = W \cdot F_S \cdot Q_{ix_0} \cdot v_{x_0} \qquad (11)$$

where I_D is the drain current, W is the width of the channel, F_S is a factor describing output (velocity saturation) behaviour of the transistor, Q_{ix_0} is the inversion charge density, and v_{x_0} is the speed of the electrons at the source (virtual source velocity), that is scaled by carrier ballisticity (transmission, T) [15].

A transistor is a nonlinear device, but if the bias is fixed, then for small signals using first order Taylor expansion, a transistor can be assumed to operate as a linear device and can be modelled through a lumped circuit model. In Fig. 10, the lumped circuit model, called the small signal model of a transistor is shown.

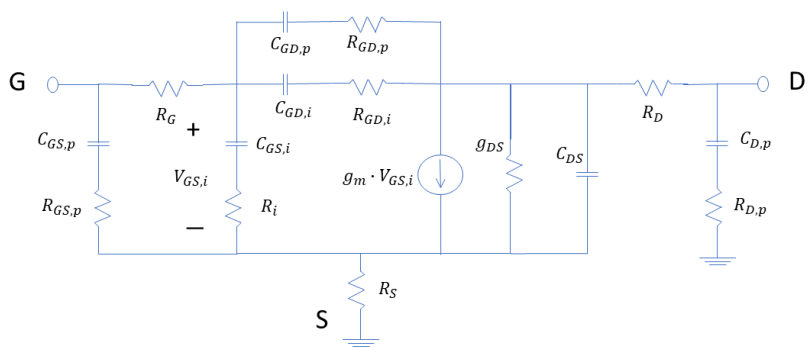

Figure 10: Small signal model of a transistor.

Many of the circuit's elements in the small signal model have both a parasitic component and an intrinsic component. For example, the gate

source capacitance C_{GS} in Fig. 10 has both an intrinsic component, $C_{GS,i}$ and a parasitic component $C_{GS,p}$. The origin of the intrinsic component is the capacitance between the substrate and the gate, while the origin of the parasitic component is the capacitance between the source and the gate. The resistance R_i originates from the latency of the charge carriers in the channel. The resistances seen in Fig. 10, e.g. the gate resistance, R_G, contributes a significant portion of the total noise generated by the transistor, since they generate thermal noise. From the values of the components in the small signal model, important high frequency parameters for the transistors can be calculated, such as f_T, which is the frequency at where the current gain is unity, and f_{max}, which is the frequency at where the power gain is unity [16]. If R_S and R_D can be neglected, then f_T and f_{max} are approximately calculated by [17]:

$$f_T \approx \frac{g_m}{2\pi(C_{GS}+C_{GD})},\ C_{GS} = C_{GS,p} + C_{GS,i} \quad (12)$$

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi C_{GD} R_G \left(1 + \frac{2\pi f_T}{C_{GD}}\Psi\right)}}, \quad (13a)$$

where $\Psi \approx \frac{g_d}{{g_m}^2}\left(\left(C_{GS,i} + C_{GS,p} + C_{GD}\right)^2 + \frac{R_i}{R_G}{C_{GS,i}}^2\right)$ (13b)

Using f_T, R_i, and the gate resistance, R_G, an approximative value of F_{min}, can be calculated for a MOSFET [18]:

$$F_{min} = 1 + 2\left(\frac{f}{f_T}\right)\sqrt{\left(\frac{\gamma}{\alpha}\right) g_m R}\ , R = R_G + R_i \quad (14)$$

where f is the frequency, and α and γ are dimensionless factors. The parameter α is less than 1 for transistors that suffers from short channel effects, otherwise it is equal to 1, while γ is bias dependent and varies roughly between $\frac{2}{3} \leq \gamma \leq 2$.

CHAPTER 3

3: Method

3.1 General

In this work, the circuits have been simulated in National Instruments (NI) AWR. AWR is a simulation program for simulating schematics, layouts etc, in RF and mm-wave environment. First, DC simulations for an individual transistor were performed and key parameters were obtained. Then, an ideal single ended amplifier was designed for the frequency of interest. Next, a differential design concept was laid out and optimized with components with a finite q-factor. The first stage of the LNA for 5G applications were initially designed. During the design, an ideal non-frequency dependent output matching for the center frequency was used as the output load, followed by completion of the design of the second stage, following a procedure similar to that of the first stage, but with where the output impedance of the first stage were modeling the source impedance of the second stage. After the individual stages of the LNA had been designed, the two stages were merged and further optimized to meet the 5G specifications around 110 GHz. The LNA for satellite applications was then designed in a similar way, but for the different frequency requirements.

3.2 Vertical NW MOSFET performance evaluation

First, a DC evaluation of device performance is needed. For this purpose, we use an RF-optimized vertical nanowire MOSFET, comprising of 180 wires, organized into 3 gate fingers. Fig. 11-12 shows the transfer and output curves of a nanowire transistor. In Fig. 11, for a drain voltage of 1.5V, a peak transconductance, g_m, is achieved for a gate voltage at around 0.5 V. For a gate voltage of 0.4 V, the transconductance is only deterred slightly, while power consumption is lowered significantly. In Fig. 15, a gate bias of around 0.4 V achieves a minimum noise figure for a single transistor with 180 nanowires. The voltage gain of a transistor can be estimated by the product of the transconductance and output impedance. Since a voltage bias of 0.4V results in a high transconductance for a

relatively low power consumption, optimum noise figure, and since the output impedance do not vary much with bias, 0.4V gate bias seems to be an optimum bias point. In Fig. 11, a drain current of 10.3 mA and a transconductance of 41.5 mS is highlighted for a gate bias of 0.4 V.

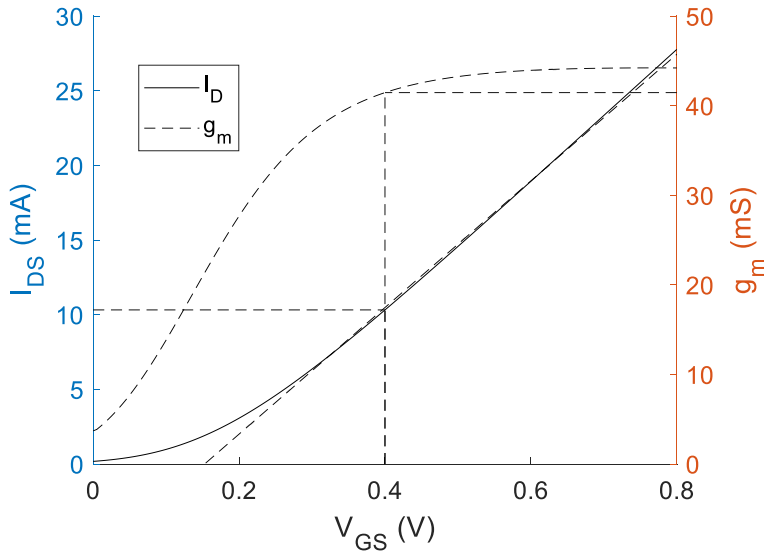

Figure 11: The drain current and transconductance versus the gate voltage, for set drain voltage, $V_{DS} = 1.5\ V$.

In Fig. 11, a line has been fitted to the drain current curve and extrapolated to the x-axis, in order to estimate a value on the threshold voltage for a drain bias of 1.5 V. The obtained value of the threshold voltage is approximately 0.16V. In Fig. 12, the drain current versus drain bias is shown for different gate biases is shown. For a gate bias of 0.4 V and a drain bias of 1.5 V, the drain current is 10.3 mA. If the drain bias is lowered by half, to 0.75 V, the drain current is lowered to 7.7 mA, a 25% decrease. A threshold voltage of around 0.16 V seems to conform with the results from Fig. 12, where for a drain bias of 1.5 V, there is almost no drain current for a gate bias of 0.0 V, although there is a drain current for 0.2 V.

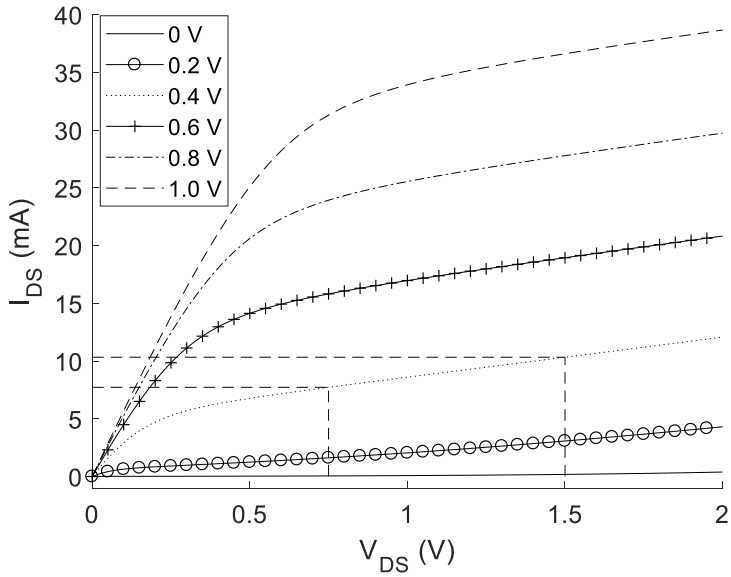

Figure 12: The drain current versus the drain voltage for different gate biases.

In Fig. 13, the gain and noise plots are illustrated. In Fig. 13a, the value of the minimum noise figure versus the gate bias is shown for the frequencies 83.5 GHz and 110 GHz, at a drain bias of 1.5 V for a transistor with 180 wires divided into 3 fingers. With a gate bias of around 0.4 V, the minimum noise figure is 0.35 dB at a frequency of 83.5 GHz. When the frequency is increased to 110 GHz, the minimum noise figure also increases to 0.47 dB. In Fig. 13b, the available gain- and noise figure circles are shown in a Smith chart for a transistor with 3 fingers and 180 wires at a frequency of 83.5 GHz. The available gain at optimal impedance match is 10.7 dB. Since the location for maximal available gain is close to the edge of the chart, it indicates that optimal matching will result in low bandwidth and stability issues.

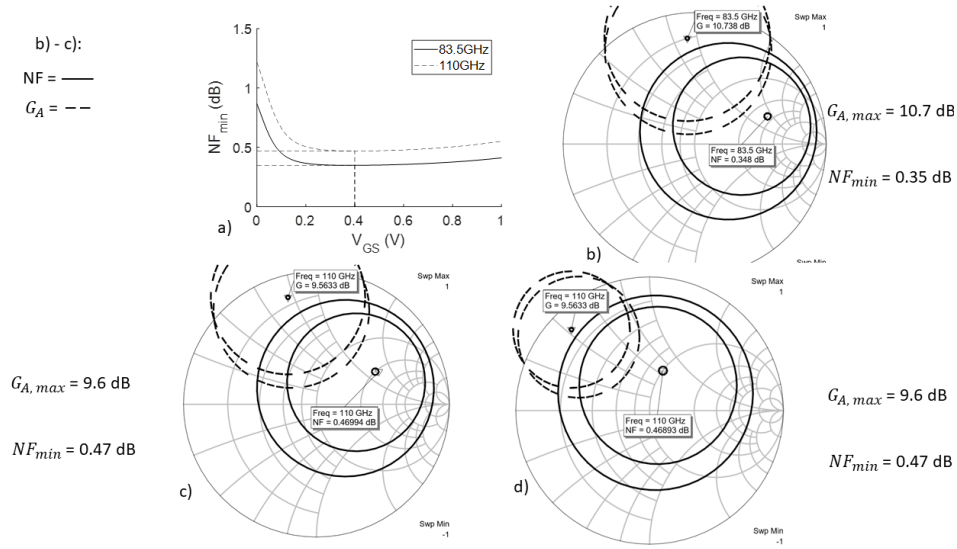

Figure 13: a) The minimum noise figure versus gate bias for a transistor with 3 fingers and 180 nanowires with a drain bias of 1.5 V. b) A Smith chart with available gain- and noise figure circles for a transistor with 3 fingers and 180 nanowires at the frequency 83.5 GHz, and c) 110 GHz. d) A Smith chart with available gain- and noise figure circles for a transistor with 6 fingers and 360 nanowires at 110 GHz.

In Fig. 13c, the location of the maximum available gain and optimum noise figure in the Smith chart has not changed noticeably from the lower frequency. The most significant change is that the minimum noise figure has increased, and that the maximum available gain has decreased, from 10.7 dB to 9.6 dB. In Fig. 13d, the value of the maximum available gain and minimum noise figure have not changed noticeably from the smaller transistor, but the location of both optima has been shifted. The location of the maximum available gain has remained close to the edge of the chart. For the Smith Charts in Fig. 13c-d, the inner circle corresponds to 0.5 dB from optimum available gain or noise, while the outer circle is 0.5 dB from the value given by the inner circle.

3.3 Sub-circuit design

There are many different amplifier stages, three examples of the most common are the common source stage, the common gate stage and the cascode stage. The common source and common gate stage are both consisting of a single transistor, if single ended design, or two transistors if differential, as shown in Fig. 14. The difference between them is the terminal where the input signal is applied, and which terminal is grounded. The cascode stage consists of a combination of the common source- and gate stage, where the input signal is sent into a common source stage, the output of the common source stage is the input for the common gate stage, as shown in Fig. 14a [10]. The common source stage has generally a lower gain than the cascode stage. The reason for the high gain of the cascode stage origins from that the voltage gain is proportional to the output impedance of the stage, and the cascode stage has generally a high output impedance [4]. Fig. 14 shows a schematic of various device implementations in the LNA design.

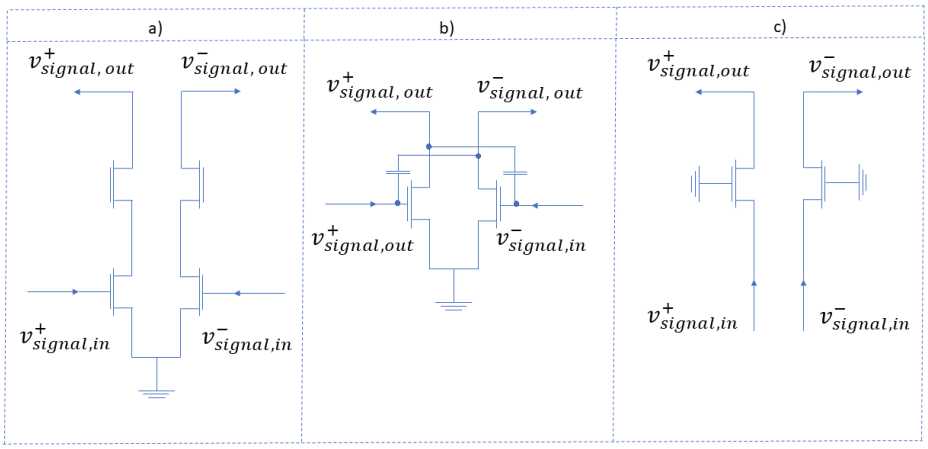

Figure 14: Three common amplifier stages: a) differential cascode stage, b) differential common source stage with cross-coupling and c) differential common gate stage.

As observed in Fig. 13, the transistor is not stable when optimizing for maximum gain. Therefore, the feedback responsible for the instability has to be reduced. This was implemented through adding cross-coupled capacitances, which reduced the effective feedback capacitance (C_{GD}), responsible for the instability. In Fig. 14b, the cross coupled capacitances are shown. They were also implemented for the cascode stage, although not shown in Fig. 14a. This is normally not done for a cascode stage, since the common gate neutralise part of the C_{GD} of the common source but was

required to ensure stability for this work. Both LNA were implemented using differential design. Differential design has many advantages compared to single-ended design. It is not affected by common mode noise from the circuit environment, the supply and ground. Furthermore, it is not depending on the impedance in the ground connection. The stages biased were separated from the small signal path either through having a DC bias feed to the transformer that is connected to the stage or by using quarter wave transmission lines.

A lumped circuit model of the transformer and the values of the elements within the model, has been used from previous work [13], and is shown in Fig. 15. In the model, each inductor is modelled with a certain inductance and parasitic resistance in series corresponding to the ohmic losses caused primarily by the skin effect. There is also a capacitive element modelling the capacitive coupling between the inductor and the ground plane. In between the capacitive element and the ground there is also a parallel RC-element modelling the substrate effects of the substrate beneath the ground plane. The model also takes into consideration the parasitic capacitance in between the two inductors. The mutual inductance of the two inductors is modelled through a coupling coefficient, *k*. The inductors in series with the resistances shown in Fig. 15 are ideal RF-blocking elements, and the capacitances in series with the inductors in the centre are ideal DC-blocking elements [13]. In this work, the inductance values for the primary- and secondary side is roughly the same, corresponding to an impedance transformation ratio 1:1 and the inductors have a Q factor of 18 at the carrier frequency.

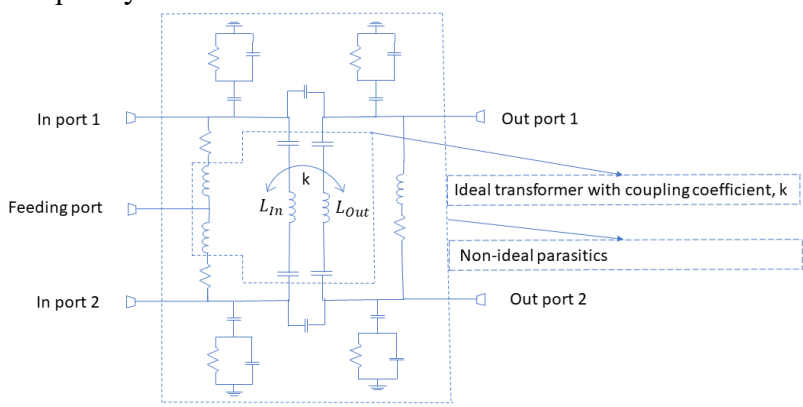

Figure 15: The transformer lumped circuit model.

In Table 1, the insertion loss, inductance at the primary- and secondary side, coupling factor, Q factor at the input, and resonance frequency of the transformer. The same model was implemented twice, with different lumped circuit elements values, depending on the frequency of operation for the LNA. The values of the inductances and the capacitances for the capacitive coupling are in the same order as that of [13]. The values of the coupling factor and series resistances are taken directly from the same work. The values of the capacitances and RC-element that are modelling the substrate effect were chosen so that the total insertion loss for the transformer for the transformer used at 110 GHz would be close to 0.7 dB, so that the transformer model would have realistic performance. For the transformer operating at 83.5 GHz, the values of the lumped circuit model were modified in order to lower the resonance frequency in order to find an optimum Q factor, and insertion loss, since, lower insertion loss can be expected at lower frequencies. The LNA design intended for satellite uses two different transformers for the LNA with the difference in the model being the inductance for one of the inductors.

Location	Frequency (GHz)	IL (dB)	$L_{Inductor}(pH)$	k	Q_{In}
Input stage	83.5*	0.64	≈30	0.81	12.44
All stages	110	0.68	≈30	0.81	12.05
Inter-stage, output stage	83.5**	0.67	≈30	0.81	11.67

Table 1: The insertion loss, inductance at primary, secondary side, coupling factor, and Q factor for the different transformer models at the frequencies 83.5 GHz and 110 GHz for satellite- and 5G application respectively.

The main purpose of the transformer at the input is to transform the circuit from single-ended to differential and are located in front of the gate inductors as shown in Fig.18-19. The transformer together with the gate inductors are used to resonate the parasitic capacitances of the transistors, in order to achieve optimal power transfer. Since achieving the minimum noise figure of the first stage is crucial to accomplish a close to minimum noise figure for the full LNA as shown in Eq. 2 (Friis formula), the input of the transformer has been matched for a trade-off between a high available gain and a low noise figure. In Fig. 16a and 17a, the available gain- and noise figure circles are shown for the input of the transformer connected to the gate inductors of the common source stage before they are matched for available gain-and noise.

The transformer at the interstage that is connecting the two differential amplifier stages, the drain inductors of the first stage and the gate inductors of the second stage resonate together with the parasitic capacitances of the transistors at the output of stage 1 and at the input of stage 2 in order to achieve optimal power transfer. Since achieving the maximum available gain and a large bandwidth of the second stage is crucial to accomplish a close to maximum available gain of the full LNA, the input of the transformer has been matched for a trade-off between a high available gain and a high bandwidth. The bandwidth is further increased by optimizing the available gain of the cascode stage for a slightly higher frequency than that of the common source stage because the gain peak of the two different stages becomes located at different frequencies. This leads to a flat frequency response for the gain in between the two peaks. Fig. 16b and 17b corresponds to the available gain- and noise figure circles for the input of the transformer connected to the gate inductors of the cascode stage before they are matched for available gain and a large bandwidth.

Fig. 16 corresponds to the LNA for 5G applications. It can be observed that the minimum noise figure for the common source LNA at 110 GHz is 2.56 dB and the available gain is 9.8 dB. These values are worse than for the values shown in Fig. 13 for the corresponding transistor. This is probably due to losses in the transformer, in addition to resistive parasitics in reactive elements. The losses will contribute to a lower available gain and an increase of the noise floor, since resistive parasitics in reactive elements are also generating thermal noise. Since the location for maximum available gain is further away from the edge of the Smith Chart, the cross coupled capacitors have been reducing the capacitive feedback and increased the stability. The matching network for the input of the transformer located at the input of the first stage consists of a shunted capacitor. The maximum available gain of the second stage is 10.5 dB and the minimum noise figure is 3.0 dB, an increase compared to the available gain and noise figure of the common source stage. The matching network for the input of the interstage transformer consists of a L-network consisting of a shunted capacitance and a series inductor.

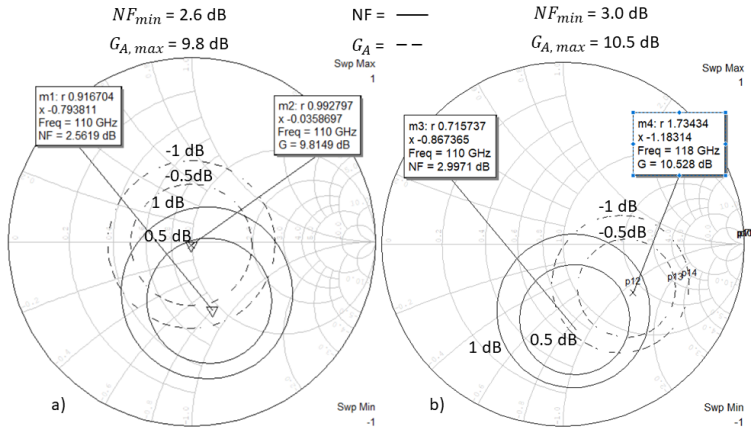

Figure 16: The available gain (dashed line)- and noise figure (full line) circles for the 5G LNA before matching: a) First stage, common source b) cascode stage

Fig. 17 corresponds to the LNA for satellite applications. Similar conclusions can be made as for D-band LNA, but the maximum available gain for the common source stage at 83.5 GHz is higher than for 110 GHz and is now 10.1 dB. The minimum noise figure of the common source stage has also increased slightly compared to the corresponding stage at 110 GHz and is now 2.57 dB. The matching network for the input of the transformer located at the input of the first stage consists of a shunted capacitor.

The cascode at 83 GHz has a higher minimum noise figure compared to the corresponding stage at 110 GHz and is now 2.8 dB. The maximum available gain for the cascode at 83 GHz is 11.2 dB, an increase compared to the corresponding stage at 110 GHz. To summarize what has been observed, the available gain and noise figure are higher for the cascode stage than the common source at the corresponding frequency. The matching network for the input of the interstage transformer consists of a L-network consisting of a shunted capacitance and a series inductor.

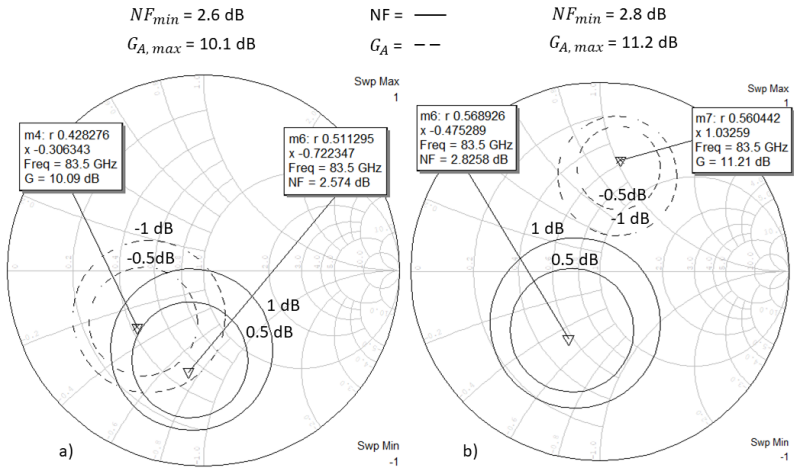

Figure 17 : The available gain (dashed line) and noise figure (solid line) circles for the satellite LNA before matching. a) common source b): cascode stage

In Table 2, the matching networks at the input and interstage of the LNA at the frequencies 110 GHz and 83.5 GHz are shown. The matching networks includes all elements in between the input of the LNA and the active devices of the first stage for the input matching network and in between the active devices of the first and second stage for the interstage matching network.

Matching network	Network	Values
$Input_{110}$	Shunt C-Tr*-series L	12 fF-60 pH
$Interstage_{110}$	Series L-Shunt C-Tr-series L	90 pH-35 fF-75 pH
$Input_{83.5}$	Shunt C-Tr*-series L	37 fF-133 pH
$Interstage_{83.5}$	Series L-Tr*-series L	85 pH-91 pH

Table 2: The matching network for the input of the transformers at the input and interstage of the LNA at 110 GHz and 83.5 GHz.

***Tr = Transistor.**

3.4 LNA and switch design

3.4.1 LNA design

Fig. 18 shows the schematic of the LNA for 5G applications. The first stage is a common source stage, and the second stage is a cascode stage. The purpose of the first shunt capacitor, C_1, is to resonate with the transformer and to transform the source impedance which corresponds to an impedance

in the Smith Chart well within the 0.5 dB available gain and noise circles in Fig. 16. A series capacitor could replace the shunt capacitor but that will result in less bandwidth. To conclude, the shunt capacitor is creating a wideband input matching that is optimized for low noise. The purpose of the L_G inductors is to resonate with the parasitic capacitances in the transistor at the operating frequencies. Shunt inductors could similarly be used to resonate the parasitic capacitances, which would provide a wider bandwidth, although this could result in a higher noise figure for the amplifier [4].

A degeneration inductor of 10 pH is located at the source of the input transistor, M1 and M2. Similarly, as for L_G, these transistors also resonate with the parasitic capacitances. The reason why inductors are required at both the source and the gate terminal is, since, a real input impedance at the gate will be created by L_S. Therefore, the value of the inductance of L_S will be chosen for an optimum noise match. Since, the value of the real part for the optimum noise match determines which inductance L_S should have, L_G provides an additional degree of freedom in order to both acquire an optimal input impedance for noise performance and resonating the parasitic capacitances at the operation frequency. In summary, the main purpose of L_S is to increase the real part of the input impedance which improves the input matching.

The input transistors, M1 and M2, are divided into three gate fingers, with 60 wires on each finger. This is to reduce the gate resistance, R_G, which will result in a reduced noise figure. This is because R_G is generating thermal noise at the input of the gate, which in turn will be amplified by the circuit. There are also cross-coupled capacitances C_{c1} and C_{c2} with a capacitance of 6 fF each. These are connected in such a way that the effective C_{gd} of the transistors will be reduced, which improves stability. For certain values of cross-coupled capacitance, it was also noticed that this could result in a smaller distance between the optimum noise and maximum available gain in the Smith Chart which was used to improve gain and noise performance. The small distance between the noise and gain circles is shown in Fig. 16-17. Therefore, a close to optimum noise and gain match was achieved at the input.

At the output of the first stage, the drain inductances, L_{D1} and L_{D2}, which are also part of the matching network, are resonating together with the parasitic capacitances at the output of the stage, thereby tuning the output

stage, and providing maximum gain at the operating frequencies. Moreover, they affect the second stage, as shown in Fig. 16b, moving the maximum available gain closer to the center of the Smith Chart. Since, $L_{D1}$and L_{D2} in Fig. 18 have a large inductance, 80 pH each, only 10 pF are required in the interstage matching network to match for maximum available gain. The interstage matching network further moves the point of maximum available gain in the Smith Chart to the center, while simultaneously providing sufficiently effective power transfer, by minimizing the reflection coefficient.

The second stage can be described in a similar way, but there are some differences. This stage is a cascode stage, where the transistors M3, and M4, are in common source configuration, consists of 3 fingers with 60 wires on each, while M5, and M6, are in common gate configuration, are twice as large and consists of 6 fingers with the same amount of wires on each finger. The reason for having larger transistors in the common gate than the common source part of the cascode is to achieve a smaller impedance as seen from the drain of the common source transistors into the source of the common gate transistors. This is due to a larger transistor having a larger transconductance, and the impedance is roughly the inverse of the transconductance. This results in a larger small signal current which results in a higher gain.

The second stage has resistive feedback from the drain of the common gate to the gate of the common source transistors in order to increase bandwidth [4]. The downside of the resistive feedback is that the gain and linearity performance reduce. Furthermore, they generate thermal noise, but since the gain of the first stage suppresses the noise generated in the second stage, the degradation of the total noise figure from the resistive feedback was small.

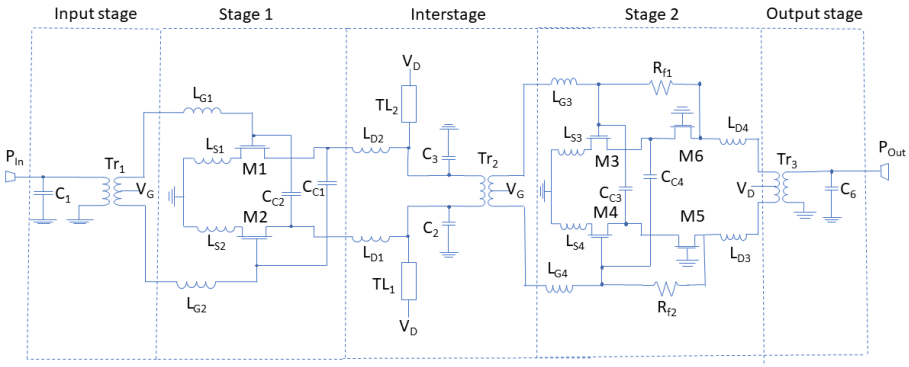

Figure 18 :The schematic of the LNA for 5G applications.

Fig. 19 shows the schematic of the LNA for satellite applications. This amplifier also has a common source as a first stage, and a cascode stage as a second stage. This amplifier shares a lot of similarities with the amplifier in Fig. 17. There are however some differences. First, the matching network for the interstage is different, as shown in Table 2. This was in order to match the network for the E-band frequency range. Since the requirements for bandwidth was not as strict as for the 5G LNA, no resistive feedback was required which resulted in a higher gain than otherwise would have been achieved. For an LNA operating in a satellite, the received signals from earth are typically very weak, therefore large gain and low noise figure are probably very crucial in order for the LNA not to degrade the SNR of the received signals. The bias point for the first stage in Fig. 17 and where $V_{GS} = 0.4\ V$ at $V_{DS} = 1.5\ V$ since it was considered as a good trade-off between noise, gain performance and power consumption, as described in section 3.2, while in Fig.18, $V_{GS} = 0.37\ V$ at $V_{DS} = 1.5\ V$ to reduce power consumption. The second stage in Fig. 18 had a bias point at $V_{GS} = 0.49V$ and $V_{DS} = 0.79\ V$, for the common source device, with a total supply voltage of $V_{DD} = 1.75\ V$, in order to increase linearity performance, at the cost of higher power consumption. The linearity performance increases, since, a higher V_{DS} increases the voltage swing and a higher gate bias results in less third order intermodulation products [10]. In a satellite, the total power consumption is limited by the power generation of the solar panels. Therefore, the second stage had a lower bias point at $V_{GS} = 0.4\ V$ and $V_{DS} \approx 0.75\ V$. Both transformers and quarter wave transmission line, TLs, was used to separate the bias from the signal path, as shown in Fig. 18-19. For both amplifiers, the output port had an impedance of 20 Ω, corresponding to the low input impedance of a current driven passive mixer followed by a transimpedance amplifier. The input port had an impedance

of 50 Ω, corresponding to the impedance of the antenna. This means that the output is matched for 20 Ω, while the input is matched for 50 Ω.

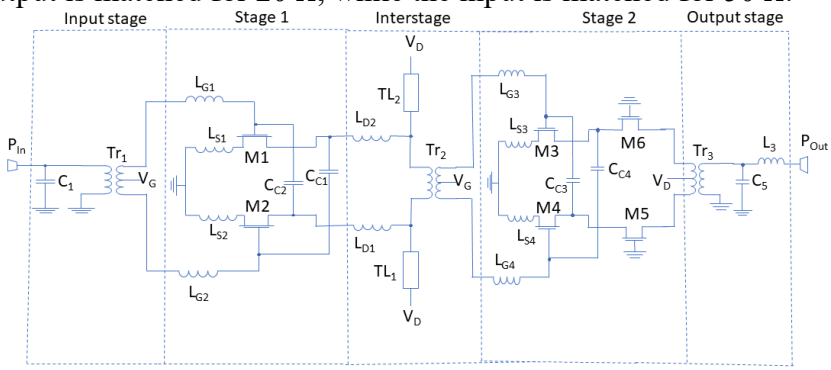

Figure 19: The schematic of the LNA for satellite applications.

3.4.2 Switch design

A schematic of the switch can be seen in Fig. 20 [14]. According to Eq. 8, the isolation and insertion loss of a switch can be calculated using the on-state resistance of the transistor and characteristic impedance of the quarter wave transmission lines, $TL_{1,2,5,6}$, if the off-state resistance of the transistor is assumed to be much larger than the characteristic impedance and the on-state resistance. The characteristic impedance and the size of the transistor where adjusted with the goal of achieving an insertion loss less than 2 dB and an isolation more than 20 dB. For the full operating frequency range. Two parallel transistors with a size of 405 wires divided into 5 fingers were finally used. The on-resistance of each transistor was 7.0 Ω. The characteristic impedance was approximately 75 Ω while the maximum off-state resistance was 348 Ω when the transistor was in resonance with a transmission line with a length of 228 μm, and a characteristic impedance of 50 Ω, noted as $TL_{3,4}$ in Fig. 20.

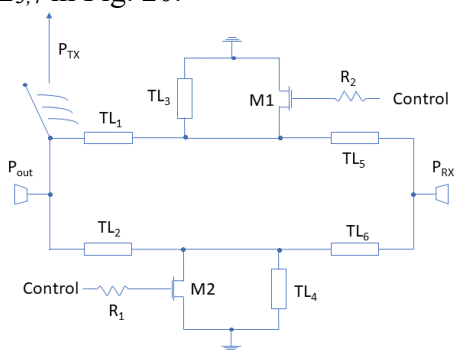

Figure 20: Schematic of the switch.

Two resistive elements, $R_{1,2}$, were used in order to decrease the effect of C_{GD} on the off-state resistance, lowering the impedance by providing a small signal ground through the control gate bias. $R_{1,2}$, have a resistance of 1 $k\Omega$. Two transistors were used in parallel, in order to ensure the condition that the off-state resistance is much larger than the characteristic impedance. Since each transistor can be made smaller while still achieving the same isolation. In addition, optimal control biases where investigated. It was found that the on-resistance did not decrease significantly with a control bias of more than 1.5 V, simultaneously, the off-resistance did not increase with a control bias of -0.25 V. Therefore, it was determined that these control biases resulted in optimum performance. This RF switch is based on the switch in [14].

CHAPTER 4

4 Results

4.1 Results for LNA

4.1.1 Satellite LNA results

In Fig. 21, the S-parameters and noise figure for the LNA with satellite applications is shown. A peak gain is achieved at 83 GHz with $S_{21} = 23.2\ dB$. The 3-dB bandwidth is 8.0 GHz, from 79.5 GHz to 87.5 GHz, with a $S_{21} > 21.8\ dB$ within the uplink E-band, from 81 GHz to 86 GHz. The noise figure is less than 2.8 dB from 78.9 GHz to 86.6 GHz, i.e. for the full E-band uplink frequency, with a minimum noise figure of 2.66 dB at 83 GHz.

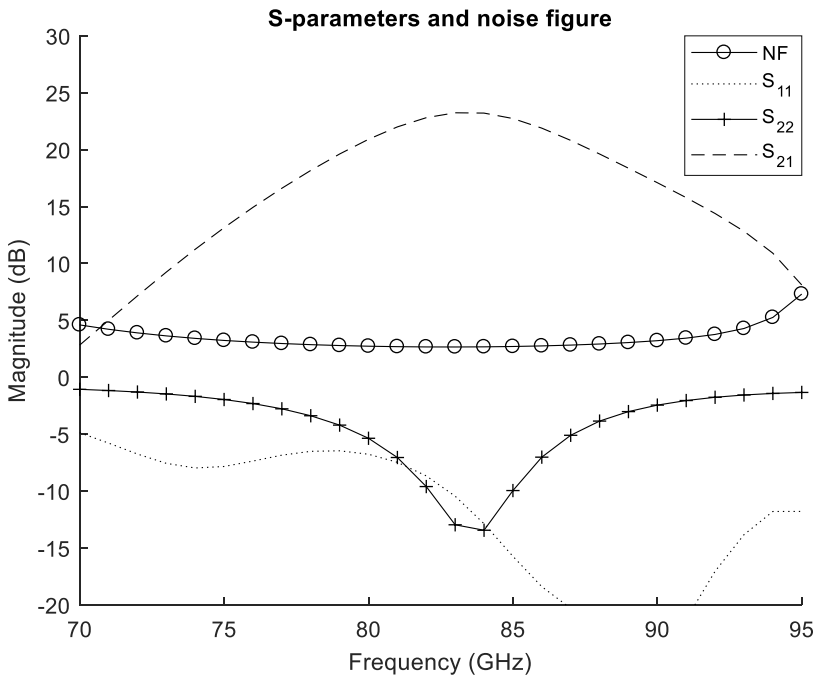

Figure 21: S-parameters and noise figure for the satellite LNA.

For the input matching, $S_{11} < -7.0\ dB$ from 81 GHz to 86 GHz, with a very good input match of $S_{11} < -10\ dB$ for frequencies over 82.1 GHz, with a minimum $S_{11} = -18.4\ dB$ at 86 GHz. For the output matching, $S_{22} < -7.0\ dB$ for the full uplink E-band frequency range, with an optimal match at 84 GHz with $S_{22} = -13.4\ dB$. The output match is quite narrowband since the output of the cascode has high impedance and the input to the mixer has low impedance. Therefore, the output matching network is optimized for a small frequency range. The gain peaks of the two stages is relatively close in frequency, since bandwidth requirements are less stringent for this LNA, which results in a peaking frequency response for the gain of the full LNA.

4.1.2 5G LNA results

In Fig. 22, the S-parameters and noise figure for the LNA for 5G applications is shown. Maximum gain is achieved at 113 GHz with $S_{21} = 24.5\ dB$. The 3-dB bandwidth spans from 103.6 GHz to 120.0 GHz resulting in a total 3-dB bandwidth of 16.4 GHz. From 106.9 to 118.1, $S_{21} > 23\ dB$, which is a frequency range of 11.2 GHz. The noise figure is less than 2.5 dB for a frequency range of 6.3 GHz, from 111 GHz to 117.3 GHz. For the full 3-dB bandwidth, the noise figure is less than 2.6 dB.

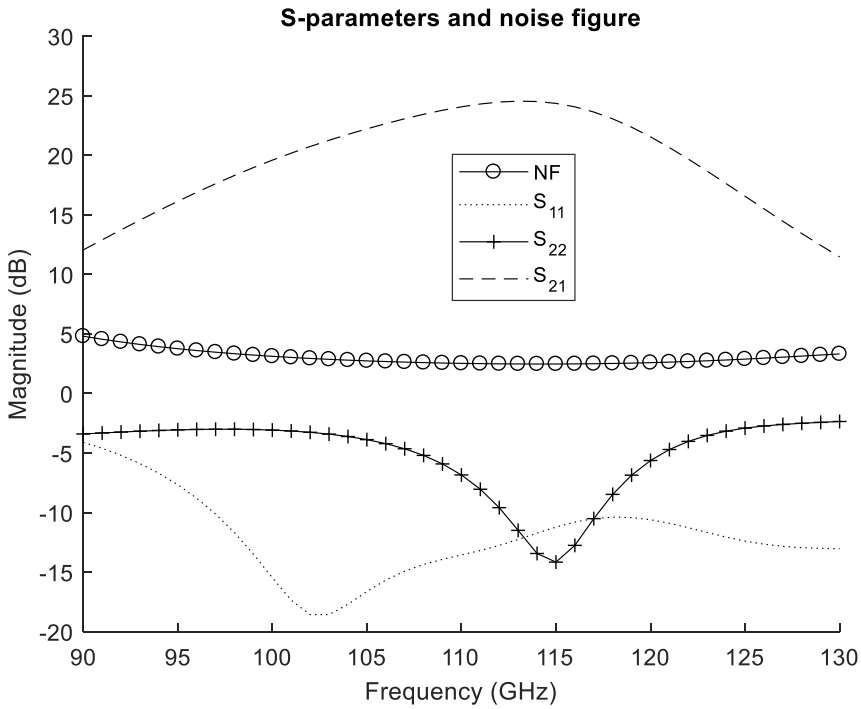

Figure 22: The S-parameters and noise figure for the 5G LNA.

The input matching achieves an $S_{11} < -10\ dB$ for the full bandwidth, with minimum input reflection achieved at 103.6 GHz with $S_{11} = -18.0\ dB$. The output matching achieves only $S_{22} < -3.5\ dB$ for the full 3-dB bandwidth. The output matching is good from 111.0 GHz to 117.3 GHz with $S_{22} < -10\ dB$ and lowest output reflection at 115 GHz with $S_{22} = -14.2\ dB$. The frequency response for the gain of the full LNA is relatively flat since the gain peaks at different frequencies for the two stages, which results in a higher bandwidth.

A study on alternate input stage topology has been done. In Fig. 23, the difference between the first stage used in the 5G LNA, the common source stage, and a corresponding common gate stage are highlighted for gain and noise figure. The common source stage has clearly both a higher gain and a lower noise figure compared to the common gate stage for the frequency range of interest. The common gate stage has a maximum gain of 2.6 dB at 111 GHz while the common source stage has a maximum gain of 9.18 dB at 108 GHz. The common source stage has a 3-dB bandwidth of 28.7 GHz between 96.9 GHz and 125.6 GHz while the common source stage has a 3-dB bandwidth of 35.5 GHz between 96.6 GHz and 132.1 GHz.

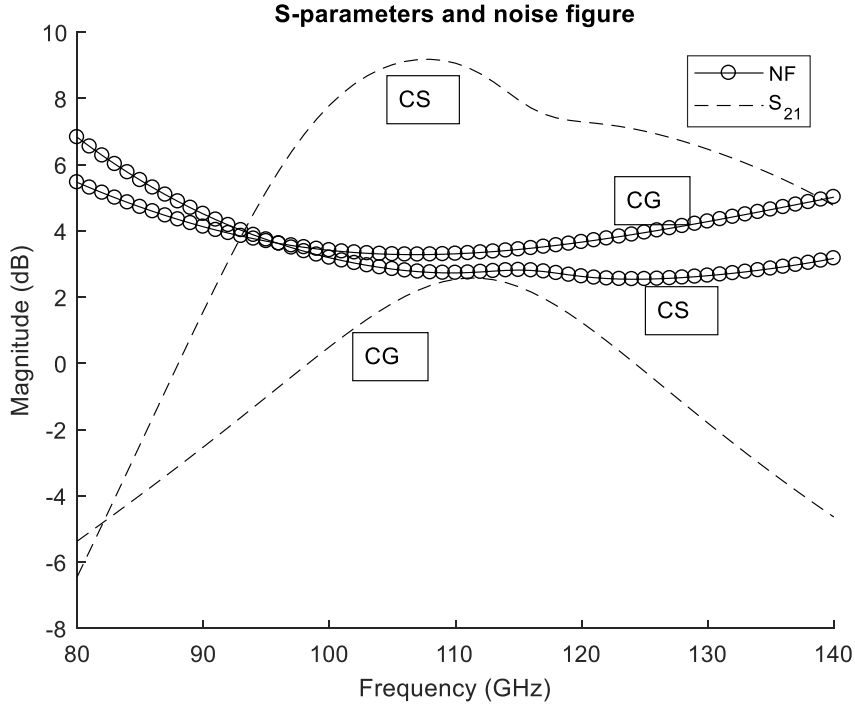

Figure 23: The difference between the common source stage and a common gate stage.

The common gate has a noise figure less than 3.5 dB between 98.0 GHz and 116.6 GHz, while the common source stage has a noise figure of less than 3 dB between 102.4 GHz and 137.5 GHz. The common gate stage never achieves a noise figure lower than 3 dB and the minimum noise figure for the common gate is 3.28 dB at 107 GHz.

4.1.3 Linearity of the LNA

Fig. 24 shows the linearity performance for the satellite LNA at 83 GHz. For high enough input powers, the output goes into compression. The 1-dB compression point is outlined at an input power of -21 dBm and an output power of 2.1 dBm. The third-order intercept point is also outlined at an input power of -12.7 dBm and an output power of 10.4 dBm. The distance between input referred compression point and third-order intercept point is therefore 8.3 dBm.

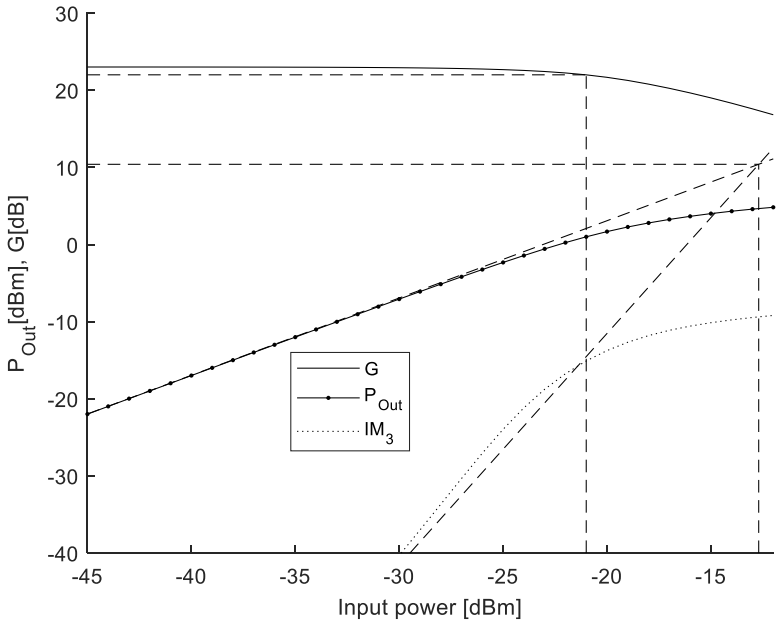

Figure 24: Linearity performance of the satellite LNA at 83 GHz.

In Fig. 24, the third-order intermodulation product is less than -40 dBm for interfering signals, with signal strength of -30 dBm power or less. At an input power of -30 dBm, the output power is -7.1 dBm. If the wanted signal power equals the interfering signal power, this results in a more than 30 dB ratio between the output signal power and the output power of the spurious signals.

Fig. 25 shows the linearity performance for the LNA for 5G applications at 114 GHz. The input referred 1-dB compression point is obtained at an input power of -23.4 dBm and an output power of -2.0 dBm. Furthermore, the input referred third-order intercept point is outlined at an input power of -17.4 dBm and at an output power of 6.5 dBm.

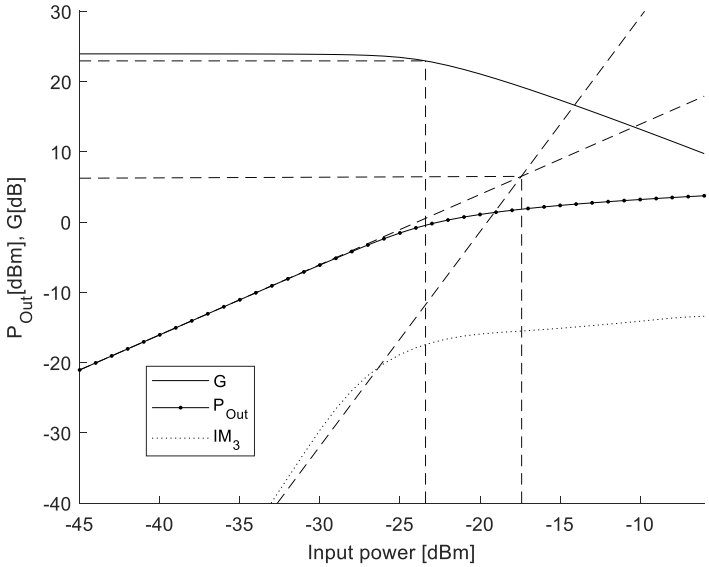

Figure 25: Linearity performance of the 5G LNA at 114 GHz.

In Fig. 25, the third order intermodulation product is less than -40 dBm when the interfering signals have a signal strength of less than -33.6 dBm. If the wanted signal power equals the interfering signal power, this results in a more than 30 dB ratio between the output signal power and the output power of the spurious signals.

4.2 Results for the switch

In Fig. 26, the S-parameters for the switch are shown. Including both S_{21} in the on- and off-state of the switch, i.e. insertion loss, and isolation between the antenna and the receiver. The isolation between the transmitter and the receiver is also shown, S_{23}. Both S_{11} and S_{22} are measured in the on-state. The insertion loss is less than 2 dB from 97.5 GHz to 111.2 GHz, a bandwidth of 13.7 GHz and has increased to 2.15 dB at a frequency of 120 GHz. The lowest insertion loss achieved is -1.96 dB at a frequency of 104 GHz. The isolation between the antenna and receiver is more than 20 dB for a bandwidth of 31.65 GHz, from 97.4 GHz to 129 GHz with maximum isolation for the bandwidth of interest at 110 GHz with an isolation of 20.33 dB. The isolation between the transmitter to the receiver is equal to the insertion loss and the isolation between the antenna and the receiver and is more than 22 dB for the frequency range of interest.

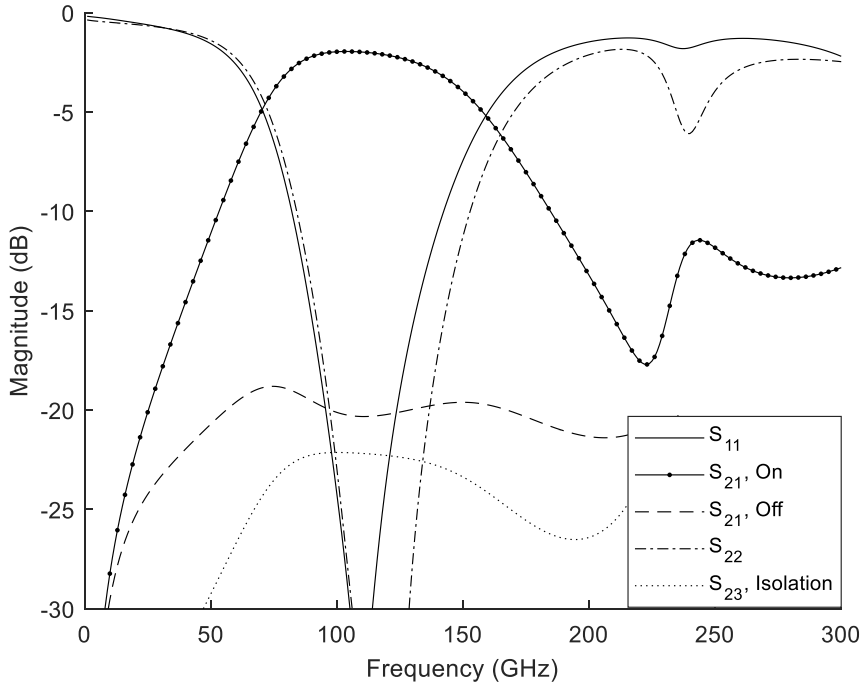

Figure 26: The S-parameters for the switch.

For the input matching, $S_{11} < -10\ dB$ from 82.1 GHz to 142.4 GHz, corresponding to an impedance input matching bandwidth of 60.3 GHz, with minimum reflection at 110 GHz with $S_{11} = -34.2\ dB$. The achieved output matching was excellent too, with $S_{22} < -10\ d$B between 84.1 GHz to 152.9 GHz with minimum output reflection achieved at 122 GHz with $S_{22} = -52.6\ d$B.

In Fig. 27, the linearity performance for the switch is shown. The switch does not show any signs of compression for input power levels lower than 10 dBm, and the input-referred 1 dB compression point for the insertion loss is 14.5 dBm. The third order intercept point is located at an input power of 21.5 dBm and an output power of 19.5 dBm.

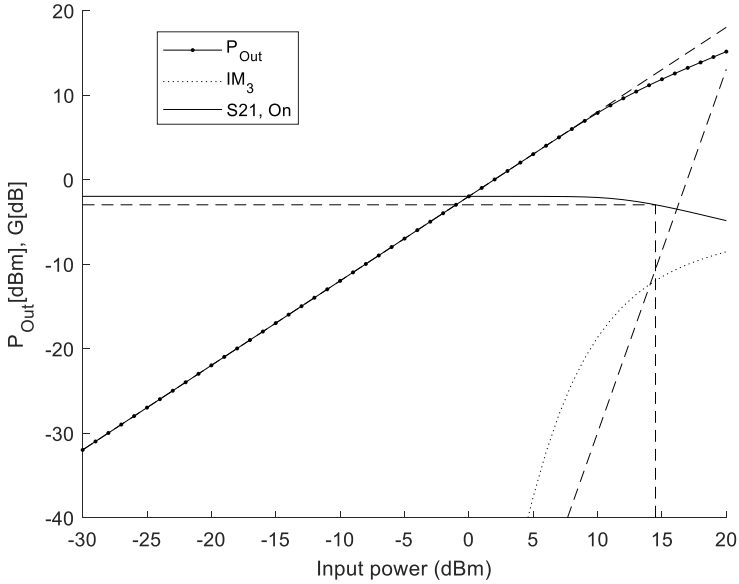

Figure 27: Linearity performance for the switch.

4.3 Performance comparison: LNA with and without RF switch

Fig. 28 shows the change in performance for the S-parameters and the noise figure when a switch is connected to the LNA for 5G applications at 110 GHz. The gain has dropped 2 dB for the LNA connected with the switch in comparison to the single LNA, approximately equal to the insertion loss of the switch. Simultaneously, the switch has increased the noise figure by approximately 2 dB to between 4.5-4.6 dB for the frequency range 106.6-116.6 GHz. The input matching has improved for the LNA that is connected to a switch compared to the single LNA, but there is no change for the output matching. The RF switch is matched for 50 Ω at the input and output. If a differential interstage matching network would be made to match the RF switch with a differential input to the LNA, perhaps would result in less complexity and better performance.

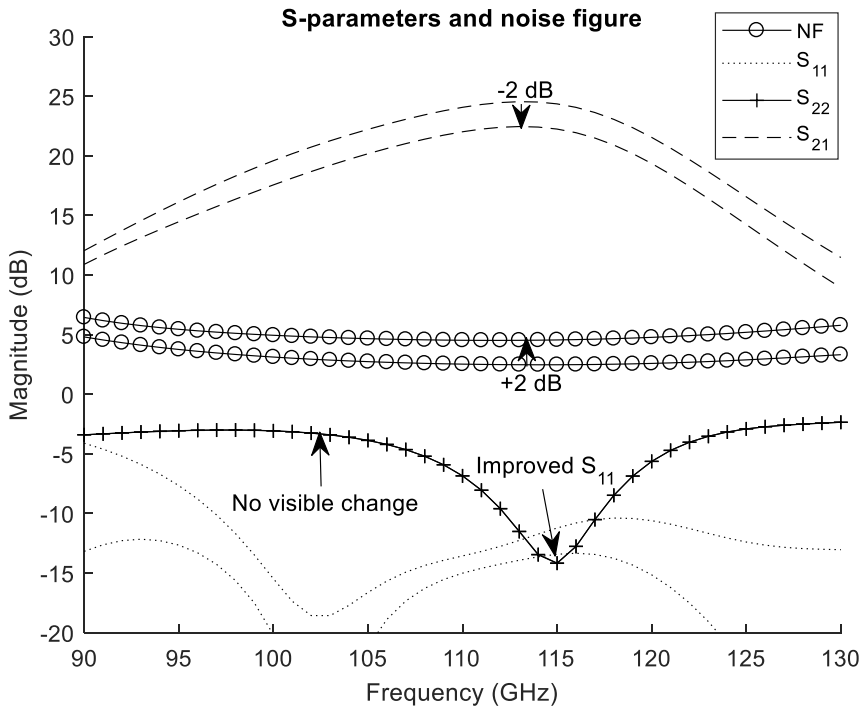

Figure 28: Change of the performance for the S-parameters and noise figure when a switch is connected to the LNA.

4.4 Comparison

4.4.1 Comparison to other LNAs

Table 3 shows a comparison between the LNA for satellite- and 5G applications regarding important parameters. The noise figure is around 0.2 dB higher for the satellite LNA compared to the 5G LNA. According to Eq. 14, increasing frequency increases the minimum noise figure. Although, the slightly higher noise figure for the satellite LNA can be explained when comparing Fig. 16 and Fig. 17, where it can be observed that it is more difficult to match the input to the first stage for both optimum gain and noise for the satellite LNA. The 5G LNA also has around 1 dB more gain than the satellite LNA. This can be explained by the higher bias of the second stage of the 5G LNA, which increases the power consumption. The bandwidth of the 5G LNA is around twice as that of the satellite LNA, this is due to both the higher operation frequency, and the resistive feedback of the 5G LNA. The combination of no resistive feedback and the lower gain results in better input-referred linearity performance for the satellite LNA.

LNA	NF (dB)	G (dB)	BW (GHz)	ICP_{1dB} (dBm)	IIP_3 (dBm)	P_{dc} (mW)	FOM (GHz/mW)
5G	2.5	24.5	16.4	-23.4	-17.4	73.1	81.2
Sat.	2.7	23.2	8	-21	-12.7	51.8	37.4

Table 3: Comparison of the satellite- and 5G LNA.

4.4.2 Comparison to other work

In Table 4, the LNA for 5G applications is compared with LNAs, operating at similar frequencies. This work used similar channel lengths to that of many of the compared works. The noise figure for the LNA of this work is lower or similar to that of the compared works, while reaching similar gain. Although, the bandwidth was similar or lower, meanwhile the power consumption was average. To conclude using FOM in Eq.8, the LNA of this work had better overall performance than all except for two compared work. The high value of FOM in [19] can be explained by their given bandwidth not being the 3-dB bandwidth but the 4.5-dB bandwidth, and their high gain.

Comparison with previous work: LNA for 5G					
	This work: *	[20]	[1]	[19]	[21]
Technology	InGaAs VNW-MOSFETs	InP HEMT	mHEMT	mHEMT	mHEMT
L_G (nm)	50	100	120	50	50
NF (dB)	2.5	5.6	4.5	2.6	4*
G (dB)	24.5	20	24	28.5	21
BW_{3dB} (GHz)	16.4	15	≈ 23	64***	30
IIP_3 (dBm)	-17.4	N/A**	N/A**	N/A**	N/A**
ICP_{1dB} (dBm)	-23.4	-16	N/A**	N/A**	N/A**
P_{DC} (mW)	73.1	120	90	50.2	28.9
f (GHz)	103.6-120.0	117.5-132.5	100-115	60-124	126-156
FOM (GHz/mW)	81.2	4.8	35.3	1101	86.4

Table 4: Comparison with previous works for low noise amplifiers operating in a similar frequency range but using different technologies.

***Results obtained from simualtions.**

****N/A indicates that no data was presented for the specific parameter.**

*****This value is not the 3-dB bandwidth, but the 4.5-dB bandwidth.**

In Table 5, the LNA for satellite applications is compared with LNAs operating at similar frequencies. The LNA of this work had lower noise figure than the compared works, while having similar or slightly higher gain. The bandwidth was lower than two out of three, furthermore the linearity was worse than two out of three compared work. The power consumption was average except for one other work that achieved a lower power consumption. To summarize, this work average performance using FOM outperformed the compared works.

Comparison with previous work: LNA for satellite					
	This work: *	[22]	[23]	[24]	[25]
Technology	InGaAs VNW-MOSFETs	CMOS	CMOS SOI	SiGe	CMOS RFSOI
L_G (nm)	50	90	45	120	45
NF (dB)	2.7	8.8	4.8	4.5	4.9
G (dB)	23.2	20.2	16.8	>22	12
BW_{3dB} (GHz)	8.0	4	15	15	25
IIP_3 (dBm)	-12.7	N/A**	0.4	N/A**	N/A**
ICP_{1dB} (dBm)	-21	-27.4	-9.2	-6.5	-21
P_{DC} (mW)	51.8	15.4	46	67	4.7
f (GHz)	81-86	66-70	76-88	81-86	80-95
FOM (GHz/mW)	37.4	4.1	7.7	19.5	40.3

Table 5: Comparison with previous works for low noise amplfiers operating in a similar frequency range and applications but using different technologies.

***Results obtained from simulations.**
****N/A indicates that no data was presented for the specific parameter.**

In Tab. 6, the switch of this work was compared to switches of other works, operating at similar frequencies. The isolation of this work was average, or

lower compared to that of other works, while the insertion loss was higher than all except one compared work. The compression point was also lower than that of other works. Further optimization is required to produce better numbers.

Comparison with previous work: Switch					
	This work: *	[26]	[27]	[28]	[29]
Technology	Vertical InGaAs nanowire MOSFETs	SiGe BiCMOS	GaN-HEMT	GaAs pHEMT	mHEMT
L_G (nm)	50	90	100	100	50
S_{32}(dB)	>20	>20	20.4	28	28-31.4
IL (dB)	2	<2	1.3	4.8	1-1.9
ICP_{1dB} (dBm)	14.5	>24	>25	22	19
f (GHz)	97.5-120	79-129	75-110	75-96	72-120

Table 6: Comparison with previous works for switches operating in a similar frequency range.

***Results obtained from simulatons.**

CHAPTER 5

5 Conclusions

Vertical InGaAs nanowire transistors have been used for the design in this work to show their potential as transistors in LNAs and switches. Two LNAs have been designed using AWR, one for 5G applications operating around 110 GHz with 16.4 GHz bandwidth, and one for satellite applications operating around 83 GHz with 8 GHz bandwidth. The achieved noise figure was less than 2.8 dB for the full frequency range of interest for both LNAs, and if compared to LNAs of other work operating at similar frequencies, the achieved noise figure is low for both amplifiers. The low noise figure at high frequency operation when using these transistors can be explained as a consequence of the high g_m for the bias point of the first common source stage. The second stage consisting of a cascode stage have provided a total gain for the full satellite LNA of 23.2 dB and 24.5 dB for the full 5G LNA. This gain will probably be enough to suppress significant noise addition from the preceding circuit elements and keep the total receiver noise figure close to 5 dB.

For the linearity performance, the input referred 1-dB compression point was -23.4 dBm, and -21 dBm for the 5G- and satellite LNA respectively, moreover, for the switch it was 14.5 dBm. For spurious emissions, the input-referred third order intercept point was -17.4 dBm, and -12.7 dBm for the 5G- and satellite LNA, respectively. The relatively low power consumption of the satellite LNA of 51.8 mW, although providing high gain and low noise figure, will be useful for satellite applications in the E-band, since it can compare with LNAs used in similar applications [12]. Furthermore, link budget calculations for the satellite LNA is shown in appendix 2. Since there are no strict defined specifications for receivers operating around 110 GHz, it is not possible to yet determine if the 5G LNA together with the switch will meet future specifications. It is shown in appendix 3, that the 5G LNA together with the switch, has low enough noise figure to meet the specification for receiver sensitivity defined at lower frequencies. The transmitter to receiver isolation the switch is more than 22 dB up to 220 GHz and the insertion loss is less than 2.2 dB from 97.5 to 120.0 GHz.

CHAPTER 6

6 Future Work

- The input transformer affects the noise performance to a large extent, since it contributes with noise before the signal has been amplified. It would be valuable to use different models of the transformer with different properties to explore what properties the optimum transformer would have and still be feasible to realize.
- This work has focused on two-stage LNAs, with a first stage as a common source and a second stage as a cascode. It would be relevant to design LNAs using the same transistors for similar frequencies but using different topologies or more stages.
- This work has been using only transistors with a channel length of 50 nm. It would also be relevant to explore more in depth how different channel lengths affects the performance of the LNAs.
- Finally, this work could be continued by designing a layout of this design, use it to realize a prototype, and measure its properties to see how it compares to the values extracted from the simulations performed in this work.

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List of Acronyms

CMOS	Complementary Metal Oxide Semiconductor
LNA	Low noise amplifier
InGaAs	Indium gallium arsenide
NF	Noise figure
SNR	Signal to noise ratio
CS	Common source
CG	Common gate
BER	Bit error rate
RF	Radio frequency
5G	Fifth-Generation Mobile communications
DIBL	Drain-induced barrier lowering
QAM	Quadrature Amplitude Modulation
PLL	Phase locked loop
GAA	Gate all-around
BW	Bandwidth
FOM	Figure of merit
SEM	Scanning electron microscope

Appendix

A.1 Modulation techniques and Link Budget

The minimum required SNR, furthermore, together with the bandwidth, noise figure of the receiver and temperature, corresponds to a minimum required input power to the receiver, the receiver sensitivity. The input power to the receiver is affected by the distance between the receiver and the transmitter, the performance of the receiving and transmitting antennas, absorption of the signal by the atmosphere and the output power of the transmitter [12].

The information is stored in the signal by modulating the signal waveform. This can be done through different types of modulation, but one modulation technique is quadrature amplitude modulation, QAM. In this technique, both amplitude and phase shift are used to modulate the signal. There are different types of QAM depending on how many bits of information each symbol contains. An example of the modulation scheme for the 16-QAM is given in Fig. 29. The number in front indicates how many ways the waveform can be modulated and the number of bits for each symbol is given by $\log_2 N$ where N is the number in front. This is because there are $2^{\log_2 N}$ different ways that the waveform can be modulated. As an example, for 16-QAM there is 4 bits per symbol [4].

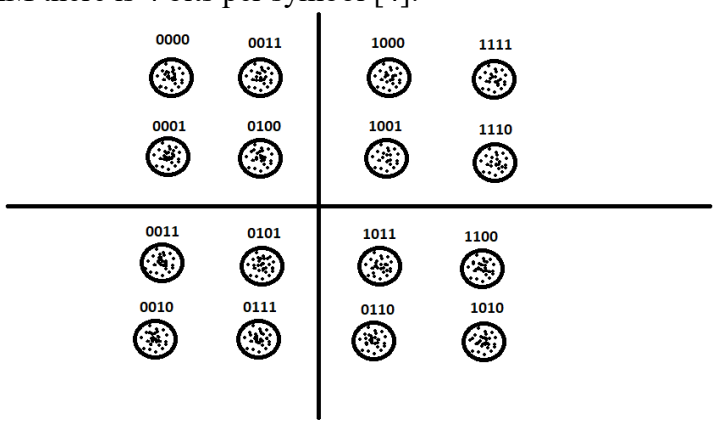

Figure 29: Modulation scheme for 16-QAM.

The more bits that can be represented by one symbol, the faster the data speed becomes. One downside though with having many bits per symbol is that the required signal to noise ratio, SNR, becomes higher and thereby the requirements on the performance of the LNA increases, for example the LNA must have a very low noise figure to be able to receive 128-QAM. In the modulation scheme, noise and nonlinearities makes it more difficult to distinguish what symbol it belongs to, i.e. the dots get further away from the circles in Fig. 29, where each circle represents a symbol. For large enough noise and nonlinearities, the dots belonging to different symbols begin to overlap, and some bits are lost as a result [30].

$$BER \approx \frac{1}{\log_2 M} 4\left(1 - \frac{1}{\sqrt{M}}\right) Q\left(\sqrt{\frac{3}{M-1} SNR}\right) \text{ [30]} \qquad (15a)$$

Where $Q(z) = p(X \geq z) = \int_z^{\infty} \frac{1}{\sqrt{2\pi}} e^{-x^2/2}\, dx$ [31] (15b)

(15a) shows the bit error rate, BER, for M-QAM as a function of SNR. Q is the Q function. When having decided a minimum acceptable value of BER and M, a minimum acceptable value of SNR can be calculated [30]:

$$rx_{Sensitivity} = 10\log_{10}(k_B T) + 10\log_{10}(BW) + NF_{RX} + SNR_{min} \quad (16)$$

From this value of SNR_{min}, the receiver sensitivity, $rx_{Sensitivity}$, can be calculated when knowing the noise figure of the receiver, NF_{RX}, and bandwidth of the channel, BW, as shown in Eq. 16. In Eq. 16, k_B is Boltzmann's constant and T is the antenna temperature in Kelvin.

The fifth-generation mobile communication systems, 5G, has a specification sheet [6], were the required specifications for a receiver designed for 5G is specified. There are 4 different power classes with different specification requirements. The power class that is used depends on application and output power of the transmitter in the corresponding wireless network. Power class 1 is for fixed wireless access user equipment. Power class 2 is for vehicular user equipment. Power class 3 is for handheld user equipment. Power class 4 is for high power non-handheld user equipment. [6]

There are also 4 different frequency bands to operate within in the FR2 frequency range. This is so far the frequency range for 5G applications yet

specified that includes the highest frequencies and covers a frequency range from 24.25 GHz to 52.6 GHz. It is specified that for a receiver of power class 3 and a channel bandwidth of 400 MHz in the n260 band, that includes the frequencies from 37-40GHz, the maximum receiver sensitivity should be -76.7 dBm, for a 4-QAM modulation. The n260 band is the highest frequency band within the FR2 frequency range yet specified. The maximum input power level should be -25 dBm for all channel bandwidths. The in-band blocking requirements states that for the n260 band, the interference signals should have a power level of 34.5 dBm over the receiver sensitivity and be at a distance 400, 800 MHz from the wanted signal. The wanted signal should in turn have a power level 14 dBm over the reference sensitivity, but the receiver should still be able to demodulate the wanted signal. Regarding all these requirements, a minimum acceptable throughput defined as 95 %, which means that the data transfer rate is 95 % of the maximum data transfer rate. The requirements are made for this frequency band, but it can be assumed that similar requirements can be used at higher frequencies [6].

Link budgets are useful for determining the requirements for the different devices in the full transmitter to receiver wireless system and takes into consideration the distance between transmitter and receiver etc [12].

$$P_{RX} = P_{TX} + G_{A,Tx} + G_{A,Rx} - FSPL - L_{atm} \quad (17)$$

A formula useful for link budget calculation for satellite communication and 5G networks etc, can be found in Eq. 17. There the received power at the receiver, P_{RX}, is a function of the power transmitted from the transmitter, P_{TX}, the antenna gains at the transmitter and the receiver, $G_{A,\,Tx}$, $G_{A,\,Rx}$ respectively [12].

$$FSPL = 10\log_{10}\left(\frac{c}{4\pi r f}\right)^2 \quad (18)$$

The free space propagation loss (FSPL), given by Eq.18, where f is the frequency, r is the distance between transmitter and receiver and c is the speed of light in vacuum [12]. Eq.18 is also a function due to the loss of the signal from attenuation caused by the atmosphere, L_{atm} [12].

$$P_{RX,min} = 10\log_{10}(k_B\,TB) + NF_{RX} + SNR_{min} \quad (19)$$

The minimum SNR for a certain BER and modulation technique is given by Eq. 15a. That could be used to calculate the receiver sensitivity, $P_{RX,min}$, according to Eq. 19. T is the temperature of the receiving antenna, k_B is Boltzmann's constant, B is the channel bandwidth, NF_{RX}, is the receiver noise figure and SNR_{min} is the minimum SNR. [30]
The E-band uplink band frequency is between 81-86GHz. For these frequencies, a total antenna gain of 88dBi is realistic. [12] The total power from the transmitter can be assumed to be around 30 W and the antenna temperature is equal to 270 K [32]. The satellites that are using the E-band for communication are normally located 400-550 km above the sea level. [2] L_{atm} is varying heavily depending on the current weather but can be assumed not to be more than 20 dB for the E-band [12], this value does not depend on the distance between the satellite and the sea level, since the atmosphere absorption above approximately 30 km is neglectable [32].

A.2 Calculations of BER for satellite LNA:

By using Eq. 17 for the link budget and Eq. 18 for the free space propagation loss, the received power at the satellites communicating in the E-band can be calculated, using $L_{atm} = 20\ dB, P_{TX} = 30\ W, G_{A,Tx} + G_{A,Rx} = 88dBi$ [12], $f = 86GHz, r = 550\ km$:

$$P_{RX} = P_{TX} + G_{A,Tx} + G_{A,Rx} + FSPL - L_{atm} = 10 \cdot (\log_{10} 30 \cdot 10^3\ mW) + 88\ dBi - 10\log_{10}\left(\frac{c}{4\pi r f}\right)^2 - 20\ dB = 10 \cdot (\log_{10} 30 \cdot 10^3\ mW)\ + 88\ dBi + 10\log_{10}\left(\frac{c}{4\pi \cdot 550\ km \cdot 86\ GHz}\right)^2 - 20\ dB = -73.2\ dBm$$

Then equation 12 can be used to calculate what SNR this corresponds to when assuming the noise figure in figure 21 of around 2.7 dB and a bandwidth of 5 GHz from the uplink E-band between 81-86 GHz:

$$P_{RX,min} = 10\log_{10}(kTB) + NF_{RX} + SNR_{min}$$
$$SNR_{min} = P_{RX,min} - 10\log_{10}(kTB) - NF_{RX}$$
$$= -73.2\ dBm - 10\log_{10}(1.38 \cdot 10^{-23} J/K \cdot 270\ K \cdot 5 \cdot 10^9\ Hz) - 2.7\ dB$$
$$= 9.9\ dB$$

If the used modulating technique is QPSK, using equation 8a and SNR = 8.6 dB results in the following BER:

$$BER \approx \frac{1}{\log_2 M} 4\left(1 - \frac{1}{\sqrt{M}}\right) Q\left(\sqrt{\frac{3}{M-1} SNR}\right) = Q\left(\sqrt{SNR}\right)$$
$$= 8.3 \cdot 10^{-4}$$

Using the same equation with PSK results in a $BER \approx 1.6 \cdot 10^{-7}$

A.3 Calculations of BER for 5G LNA:

If the channel for instance has a bandwidth of 400 MHz in the operating band n260 in the Fr2 frequency range, the temperature is 300 K, for a power class 3, then the minimum required receiver sensitivity, $RX_{Sensitivity}$ = -76.7 dBm. From Eq. 9 and with a noise figure of 4.6 dB as shown in figure 28:

$$RX_{Sensitivity} = 10\log_{10}(K_B T) + 10\log_{10}(BW) + NF_{RX} + SNR_{min}$$

$$SNR_{min} = RX_{Sensitivity} - 10\log_{10}(K_B T) - 10\log_{10}(BW) - NF_{RX} =$$
$$= -76.7 \text{ dBm} - 10\log_{10}(1.38 \cdot 10^{-23} J/K \cdot 300\ K)$$
$$- 10\log_{10}(400 \cdot 10^6\ Hz) - 6\ dB = 5.1\ dB$$

According to 3GPP, the specification requires that for a minimum input power of -76.7 dBm, the data rate throughput should be minimum 95% when using 4-QAM [6]. By using $SNR_{min} = 5.1\ dB$ in equation 8a for 4-QAM:

$$BER \approx \frac{1}{\log_2 M} 4\left(1 - \frac{1}{\sqrt{M}}\right) Q\left(\sqrt{\frac{3}{M-1} SNR}\right) \approx 0.036.$$

A.4 Noise sources in LNAs:

In Table 7 and 8, the noise source contributions for the 5G- and satellite LNA is shown. The noise power is measured at the output of the LNA. It can be concluded that the three most significant sources in both LNAs are from the transistor model, the transformer at the input of the LNA, and the gate inductors of the common source.

5G LNA:

Element*	Noise contribution at 110 GHz (10^{-18} W/Hz)
$M1$ and $M2$	5.8
Tr_1	3.5
L_{G1} and L_{G2}	1.8
L_{S1} and L_{S2}	1.3
C_1	0.34
Tr_2	0.33

Table 7: Noise sources for the 5G LNA.

***Refer to Fig. 18.**

Satellite LNA:	
Element*	Noise contribution at 83 GHz (10^{-18} W/Hz)
$M1$ and $M2$	2.1
L_{G1} and L_{G2}	2.0
Tr_1	0.95
C_1	0.29
$C_{c1}$and C_{c2}	0.24
Tr_2	0.061

Table 8: Noise sources for the satellite LNA.

***Refer to Fig. 19.**

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