A Quadrature Frequency Generation Chain for Direct-conversion Phased-array 5G Transceivers

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Abstract

The 5th generation (5G) has recently specified a new spectrum range, FR2- 5G New Radio (5G-NR), to provide higher spectral efficiency and channel capacity for ubiquitous cellular connectivity where the user ends can be in various types such as picocell stations, sensor nodes, cloud servers, hand-held devices, and so on. Due to the advantage of phased array antennas in performing beam-forming, and improving SNR at higher spectra, multi-antenna systems have gained an inevitable role in developing such radios. However, attributed to their multi-path feature, their corresponding silicon solutions are often complex, power-hungry, and bulky which all together limit their practicality for low power and compact solutions. This introduces an additional hurdle to the RFIC units of 5G radios which already is challenged by strict cellular requirements.

During the recent years, the developing short channel silicon-on-insulator (SOI) CMOS technology has provided distinguished characteristics for CMOS transistors. Thanks to the smaller scale and the isolated substrate, the CMOS transistors provide a considerable improvement in power efficiency. Also, they provide a highly controllable characteristic promising novel architectures and circuits. All the merits considered, short channel SOI technology has taken an indisputable role in developing advanced RFIC units.

This thesis benefits from Global Foundries' 22-nm fully depleted silicon-on-insulator (FD-SOI) process, and presents a power-efficient LO phase shifting RFIC unit for direct conversion phased array transceivers. The proposed solution covers the sub-30 GHz bands including n257, n258, and n261 (24.25 GHz- 29.5 GHz). The chain supports the required frequency range with a single VCO by providing a 31.5% tuning range. The VCO occupies 0.025 mm^2, and consumes 5.1 mW on average and its phase noise at 1 MHz offset varies between -95 dBc/Hz to -98 dBc/Hz. Accordingly, its FOM and FOMt at 1 MHz offset is -177.8 dBc/Hz and -187.7 dBc/Hz respectively. Furthermore, the chain provides a tunable quadrature LO generation that consumes 15.8 mW and provides at least 40 dBc image rejection ratio (IRR) over the targeted bandwidth. As the last stage, for accomplishing the array steering, a low power active phase shifting unit is proposed. The proposed phase shifter occupies 0.01 mm^2, and provides 93-110 degree phase-shifting for each of the quadrants within the specified bandwidth. The phase-shifting unit and its following output buffer consume 2.8 mW and 2.7 mW respectively For each quadrature paths.

Table of Contents

1 Introduction **1**
- 1.1 Thesis organization . . . 1
- 1.2 Objective and motivation . . . 1

2 Architecture **5**
- 2.1 Multi-antenna systems . . . 5
- 2.2 Frequency conversion . . . 7
- 2.3 LO generation and distribution . . . 8

3 FD-SOI short-channel CMOS technology **11**
- 3.1 Impact of SOI . . . 11
- 3.2 Impact of short channel . . . 12

4 Tunable CMOS resonance circuits **17**
- 4.1 Varactor . . . 18
- 4.2 Capacitor bank . . . 18
- 4.3 Cascode load . . . 19

5 Phase shifter **23**
- 5.1 Phase shifting techniques . . . 23
- 5.2 Phase shifting block . . . 24

6 IQ generation **31**
- 6.1 LO quadrature generation techniques . . . 31
- 6.2 Quadrature generation block . . . 32

7 Voltage controlled oscillator **39**
- 7.1 Challenges and limitations . . . 39
- 7.2 VCO and performance evaluation . . . 40

8 Conclusion and future work **45**
- 8.1 Conclusion . . . 45
- 8.2 Future work . . . 45

References 47

List of Figures

2.1 Array of N antennas with identical spacing. 6
2.2 Conventional architectures for phased array systems. (a) RF phase shifting. (b) baseband phase shifting. (c) LO phase shifting 6
2.3 Popular transceiver architectures. 8
2.4 Various frequency generation and distribution strategies 9
2.5 Proposed frequency generation chain for LO phase shifting receivers. 9
2.6 LO distribution arrangement for an array of 4 antennas. 10

3.1 Cross section of an FD-SOI CMOS transistor. 11
3.2 Body biasing Global Foundries for 22nm FDX process [14]. 12
3.3 Small signal model of a MOSFET 13
3.4 f_{max} compression for different technology node of NFET by Global Foundries [14]. 14

4.1 Parallel lumped model of an LC tank with parasitic resistance. 17
4.2 A CMOS varactor and its equivalent distributed lumped model[4]. . . 18
4.3 Switch capacitor bank and its simplified lumped model. 18
4.4 Cascode circuit for N and P channel transistors. 19
4.5 Small signal model of the NMOS cascode topology. 20
4.6 Operation regions of transistors Mn and Mcn when gate bising of the Mcn is regulated. 21
4.7 Intrinsic C_{gs} and C_{gd} variation for PMOS and NMOS cascode transistors. 21

5.1 Multi-phase oscillator. 24
5.2 Phase shift by injection locking. 24
5.3 Maximum achievable phase range for 1.8 times tuning ratio for capacitor and different Q-factor values. 25
5.4 Amplitude modulation due to the phase shift (AM-to-PM). 26
5.5 proposed LO phase shifting unit. 27
5.6 (a) proposed differential phase shifter (b) following differential buffers. 27
5.7 small signal gain of the phase shifting chain. 28
5.8 Maximum achievable phase shift versus frequency. 28
5.9 Maximum AM-to-PM error within the band of interest. 29

5.10 Output power over the load capacitor. 29
5.11 Layout view for the differential pair of the proposed phase shifter and its following buffers 30

6.1 Quadrature generation block. 32
6.2 a) Constant gain PPF b) Buffer 33
6.3 Small signal model of the IQ chain. 34
6.4 Small signal model an active buffer loaded by a coupled resonator. . 34
6.5 Small signal gain of the IQ chain 36
6.6 IRR with and without calibration with calibrating voltage. 36
6.7 Output power level of the IQ unit after calibration, loaded by the consequent phase shifitng block. 37

7.1 Negative feedback system. 39
7.2 Lumped model of a cross coupled LC oscillators. 40
7.3 Schematic of the designed VCO. 41
7.4 Layout view of the VCO and its consequent buffers. 42
7.5 Phase noise of the VCO at 1 MHz and 10 MHz offset. 43
7.6 DC power consumption of the designed VCO. 43
7.7 FoM and FoMt at 1 MHz and 10 MHz for the designed VCO. 44

List of Tables

1.1 5G-NR frequency ranges. 2
1.2 Specified bands for FR2 5G NR. 2
1.3 Channel bandwidth for different bands of FR2. 2

5.1 Performance comparison with state-of-the-art designs. 30

7.1 Performance comparison with state-of-the-art VCO designs. 44

Chapter 1
Introduction

1.1 Thesis organization

This work is a result of an internship at the Department of Microtechnology and Nanoscience (MC2) of Chalmers University of Technology, Gothenburg, Sweden. The purpose was to investigate novel techniques for multi-antenna phased array receivers. Therefore, targeting the form factor and power consumption, a sub-30-GHz frequency generation chain for low power and small scale 5G phased array transceivers was proposed. All simulations are done by using Cadence Virtuoso. The utilized design kit is a 22 nm, fully-depleted silicon-on-insulator (FD-SOI) CMOS process provided by Global Foundries. The used supply voltage is 850 mV. All the inductors and transformers are provided by the same design kit. The report includes eight chapters covering as follows:

- Chapter 1: Presents a brief discussion of the objective and motivation.
- Chapter 2: Discusses the phased array architectures.
- Chapter 3: Elaborates upon advantages of ultra-low scale SOI CMOS technology and how this work benefits from those features.
- Chapter 4: Discusses tunable CMOS resonance circuits, and proposes an alternative technique to improve tuning range.
- Chapter 5: Presents the phase shifting unit.
- Chapter 6: Presents the IQ-generation block.
- Chapter 7: Covers the voltage controlled oscillator block.
- Chapter 8: provides a conclusion for the proposed solution and discusses future works.

1.2 Objective and motivation

Recently, the 3rd Generation Partnership Project (3GPP) has specified a new spectrum ranges for $5th$ generation of wireless cellular connectivity, 5G-NR [1]. As shown in Table.1.1 [1], its spectrum includes two separate regions where FR1

is an improved model of the former standard 4G, and FR2 is the new spectrum designated to provide higher channel capacity and spectral efficiency for cellular user ends. As shown in Table.1.2 and Table1.3 [1], so far, four bands have been announced which each offers 50 MHz, 100 MHz, 200 MHz, and 400 MHz channel bandwidth. These bands are partially or fully licensed across the world.
5G-NR provides various carrier aggregation strategies for both inter-band and intra-band use cases [1]. This feature comes with placing three bands (n257, n258, and n261) adjacently, and granting 5.25 GHz bandwidth in total. Compared to the unlicensed 60 GHz band, such a bandwidth is provided at relatively lower spectra. Therefore, the RFIC unit can support higher orders of modulation with lower complexity and power consumption. The communication type of FR2 is limited only to the time division duplex (TDD) scheme leading to great simplicity in the RFIC unit. Since, firstly, the self-interference is not a concern and the front-end can operate without additional filters, and secondly, the TX and RX can share the same LO chain without mutual pulling. The second advantage works best for LO path phase-shifting architectures since it reduces LO complexity to half.

Spectrum designation	Spectrum range GHz
FR1	0.41 – 7.125
FR2	24.25 – 52.6

Table 1.1: 5G-NR frequency ranges.

Operating bands	UL (GHz) & DL (GHz)	Duplex mode
n257	26.5 - 29.5	TDD
n258	24.25 - 27.5	TDD
n260	37 - 40	TDD
n261	27.5 – 28.35	TDD

Table 1.2: Specified bands for FR2 5G NR.

Bands	SCS KHz	50 MHz	100 MHz	200 MHz	400 MHz
n257	60	Yes	Yes	Yes	-
	120	Yes	Yes	Yes	Yes
n258	60	Yes	Yes	Yes	-
	60	Yes	Yes	Yes	Yes
n260	60	Yes	Yes	Yes	-
	60	Yes	Yes	Yes	Yes
n261	60	Yes	Yes	Yes -	
	60	Yes	Yes	Yes	Yes

Table 1.3: Channel bandwidth for different bands of FR2.

Among various transceiver architectures, direct conversion topology provides

a notable simplicity, lower form factor, and less overall power consumption. Although its LO distribution at higher spectra requires additional gain and phase adjustment, for UE devices which carry smaller arrays, direct conversion LO phase shifting architecture [2], [3] can provide an optimal performance .
Considering the explained merits, this design concentrates on bands n257, n258, and n261 and presents a quadrature phase-shifting LO chain for direct conversion transceivers. In the following part, a brief discussion of the related challenges is presented.
Oscillator: To cover the sub-30 GHz bands with a single VCO, the oscillator must provide at least 23% of tuning range. As a well-known fact, tuning range, power consumption, and phase noise of an oscillator are mutually in a trade-off with each other[4]. Therefore, providing such a wide span while keeping the phase noise and power consumption at a reasonable level is challenging. On the other hand, the use of an additional oscillator, not only increases the power consumption and area, but also, it introduces mutual pulling between oscillators which consequently leads to more complex calibration and synchronizing units.
Quadrature generation: The first challenge in this unit is to provide a sufficient IQ accuracy including amplitude and phase over the bandwidth. The second issue is to provide harmonic purity and produce fewer spurs. The third challenge which is a great concern with PPFs is to provide a wide bandwidth with a low power dissipation.
Phase shifting unit: Phase shifting unit deals with three major challenges. The first problem is the amplitude to phase modulation error (AM-to-PM) by which the gain transfer function of the phase shifter varies for different phase adjustments. This problem is less critical in the LO path since the amplitude of the signal does not carry any information and the rendered loss can be compensated by afterward buffer stages providing a reliable but power hungry solution. The second problem is to provide wideband phase-shifting functionality by which at least 90-degree phase shift for each quadrant is provided within the bandwidth. The third important challenge is to provide wideband gain performance.

Chapter 2
Architecture

2.1 Multi-antenna systems

Use of available wider bandwidth at higher frequencies has been a challenge for ubiquitous cellular connectivity. This is majorly due to the lossy link path at such spectra which in turn results in a lower SNR levels. According to Friis formula, the power level of the received signal can be quantified as Eq.2.1:

$$P_{RX} = P_{TX} G_{TX} G_{RX} (\frac{\lambda}{4\pi d}) \tag{2.1}$$

Where $P_{TX}$is the power level of the transmitted signal, G_{TX} is the antenna gain of the transmitter, G_{RX} is the antenna gain of the receiver, λ is the free-space wavelength, and d is the distance between RX and TX. Based on Eq.2.1, the power level of the received signal is proportional to the signal wavelength. Therefore, naturally, electromagnetic waves undergo a higher link attenuation as their wavelengths get smaller. Additionally, due to the atmospheric absorption, the transmitted waves experience an additional loss [5]. To overcome this problem, directional antenna solutions could be utilized [6]. Despite the Omni-directional class, directional antennas concentrate the wave energy into a specific direction. Therefore, in a specific physical angle, a higher signal to noise ratio (SNR) can be achieved.
A single directional antenna requires a mechanical rotation which is not a practical solution for cellular applications. Therefore, later on, by the development of phased array antennas, it is shown that the SNR can be improved by an alternative way where the beam of radio waves are steered electrically [6]. In this technique, the transmitter feeds the same wave to an array of antennas where the waves are with a relative propagation delay to each other. In the receiver side, as shown in the Fig.2.1, another array receives the transmitted waves. Considering the free-space condition, If the plane-wave beam is incident on the array at an angle of θ_{in} to the normal direction, each beam will experience a time delay equal to $\Delta(\tau) = \frac{d \sin(\theta_{in})}{c}$ [7] where d is the physical distance between antennas and c is the speed of light in free space. In this case, the signals received by each of the antennas can be quantified by Eq.2.2 [7]

$$S_i(t) = A \cos(\omega(t - (i-1)\frac{d \sin(\theta_{in})}{c})) \tag{2.2}$$

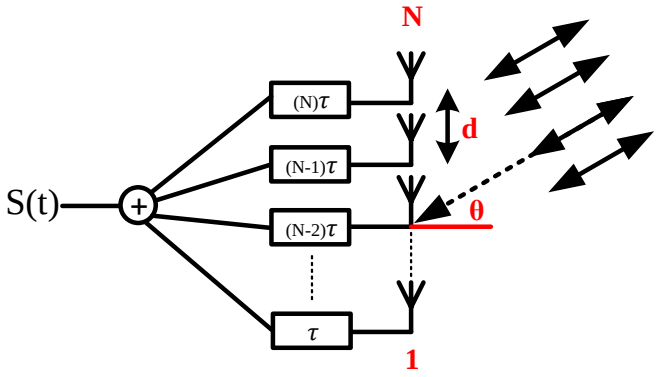

Figure 2.1: Array of N antennas with identical spacing.

By assuming a linear propagation delay between antennas, applying an additional delay equal to $(N-i+1)\frac{d\sin(\theta_{in})}{c}$ for i_{th} antenna, would provide zero relative phase difference between received signals, and the waves can be summed constructively. In this case, the array achieves a power gain of N^2 over that of a single antenna. If we assume that noise added by each antenna is uncorrelated, the antenna array would gain N times more noise as well. Therefore, in total use of antenna arrays would improve the SNR by a factor of N [7]. Since the wave construction is a selective process for a specific relative delay, the use of the array improves the selectivity after the construction node. By assuming a linear relationship between time delay and phase shift, the transceiver requires to provide at least 180° for differential and 90° for quadrature signals respectively.

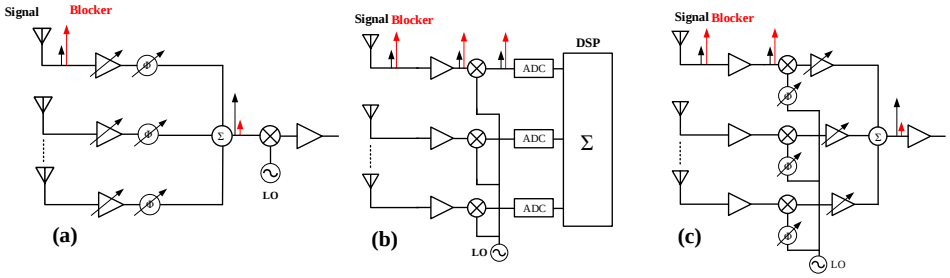

Figure 2.2: Conventional architectures for phased array systems. (a) RF phase shifting. (b) baseband phase shifting. (c) LO phase shifting

Fig.2.2, demonstrates the most commonly used architectures for phased array systems. RF phase-shifting requires a less complex frequency synthesizing and LO distribution network. Also, since the summation is done before the frequency conversion, the linearity requirements on mixers and the rest of the receiver is relaxed. However, its requirement on the phase-shifting unit is strict since the phase shifter must provide a high input dynamic range, otherwise, in the existence of

strong blockers, it would get saturated and consequently, it would fail to provide beamforming. Besides, since the phase shifter stands at the beginning of the chain, its noise performance becomes critical.
Baseband phase-shifting relies on DSP operations to adjust the amplitude and phase of each antenna. This technique is highly flexible and provides accurate beamforming however since each antenna requires a separate down-conversion and mixed-signal chain, it requires a high power consumption. Moreover, as the combining happens in baseband, both RF and baseband chains require a higher dynamic range. Through the literature, a variation and combination of these two methods have been tried. Hybrid [8] and IF [9] beamforming are few to name.
As an alternative technique, the phase-shifting function can be accomplished through the oscillator. This can be shown by the use of the linear model of a mixer as it is provided in Eq.2.3.

$$\begin{aligned} S_{out}(t) &= \cos(\omega_{RF}(t) + \phi_{RF}) \cos(\omega_{LO}(t) + \phi_{LO}) \\ &= \frac{1}{2} \left[\cos\left((\omega_{RF} \pm \omega_{RF})(t) + (\phi_{RF} \pm \phi_{LO})\right)\right] \end{aligned} \tag{2.3}$$

This architecture provides more relaxed requirements on phase shifters which in turn, leads to a simpler RF circuitry. However, since the summation happens only by the frequency conversion, the linearity requirement on the mixer is strict. Additionally, it renders a complex LO distribution due to the fact that each of the antenna elements requires a separate frequency conversion chain. The latter issue is more problematic in larger arrays.

2.2 Frequency conversion

Fig.2.3, shows two popular architectures. In the first architecture which is called zero-IF, the RF/IF signal is translated directly to DC/RF level. This architecture provides a superior performance in rejecting image harmonics, and producing lower mixing spurs [4]. However, linked to its higher LO frequency, its LO distribution requires additional adjustment. In the second architecture which is known as sliding IF, the frequency translation is done by two steps through an intermediate frequency. This architecture requires a single frequency synthesizer and the second conversion happens by a fraction of the first one. Therefore, the IF slides over the same bandwidth of RF signal. In sliding IF architecture, the first LO frequency can be calculated by Eq.2.4.

$$\omega_1 = \omega_{RF}(\frac{N}{N+1}) \tag{2.4}$$

where N denotes the number of down conversions. For example, for N=2, $\omega_1 = \frac{2}{3}\omega_{RF}$ and $\omega_{IF} = \frac{1}{3}\omega_{RF}$. Therefore, compared to zero-IF architecture, in the sliding-IF, the LO distribution happens at lower frequencies by which lower amplitude and phase error is achieved. However, this does not necessarily gives an upper hand in overall power efficiency and simplicity. First of all, sliding-IF requires an additional mixer and a frequency divider which both add to power consumption

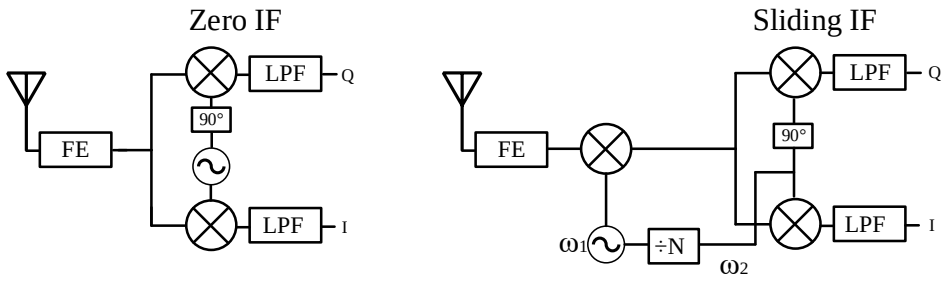

Figure 2.3: Popular transceiver architectures.

and complexity. Secondly, it introduces more non-ideality to the chain. A common case is the additional spurs and harmonic aliasing in the base-band which is the result of image signals, multiple LO harmonics, and non-linear mixers.

2.3 LO generation and distribution

Three common types of LO distribution are shown in Fig.2.4. In the local PLL architecture, every antenna element is fed by a local PLL [10]. These PLLs are synchronized to an external oscillator which is a low frequency and low phase noise source. Therefore, the LO distribution is low power and simple. However, since it requires a separate PLL for each antenna, its LO generation occupies more space and consumes more power. In the central PLL architecture, the synchronized frequency is produced by a single unit and distributed to all channels. This architecture provides a simple generation. However, its distribution requires additional gain and phase adjustment to ensure its LO accuracy. In the distributed architecture, the PLL generates only an integer fraction of the required LO, and consequently, it is up-converted by a local sub-harmonic injection locking multiplier [11][12]. By the use of this architecture, LO can be distributed with less power consumption. However, it comes with a spurs penalty. As the lower sub-harmonic frequency, the higher level of spurs are generated [12].

As it is discussed earlier, due to the TDD modulation scheme defined by 3gpp for 5G-NR FR2 range, RX and TX chain can share the same LO chain efficiently. This motivates opting for LO phase shifting topology. Especially, for UE devices that carry smaller antenna arrays and do not require a complicated LO distribution. In addition, the advantage of direct conversion architecture in providing less spurs and lower power consumption over the sliding IF topology is explained. Considering all the facts, this design provides a phase-shifting quadrature LO chain for direct conversion transceivers. As linearity of the mixer is an important factor, the chain can be used to drive a linear quadrature passive mixer directly.

The design follows the central PLL solution. Therefore, as it is shown in Fig.2.5, it includes a wide tuning range VCO, a tunable quadrature generator, and a phase shifter providing at least a 90-degree phase shift within the targeted spectrum. Additionally, for compensating the AM-to-PM and distribution loss, two buffers are provided. This work does not include the distribution network for multiple

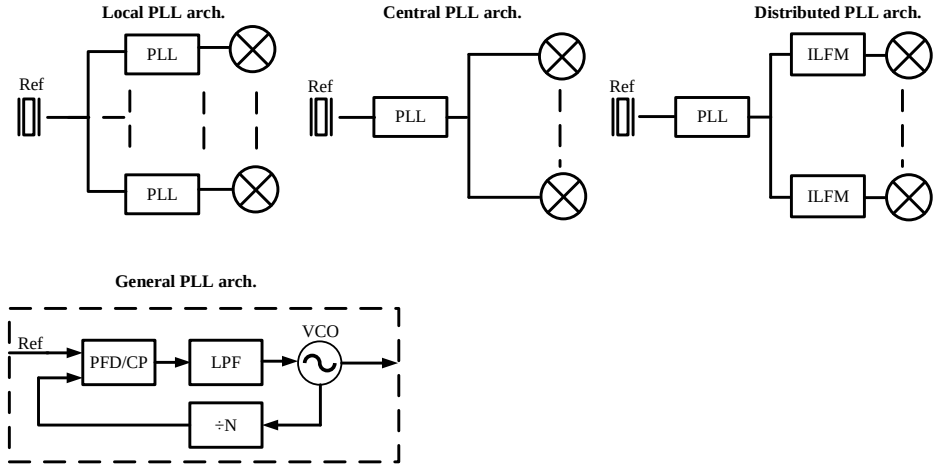

Figure 2.4: Various frequency generation and distribution strategies

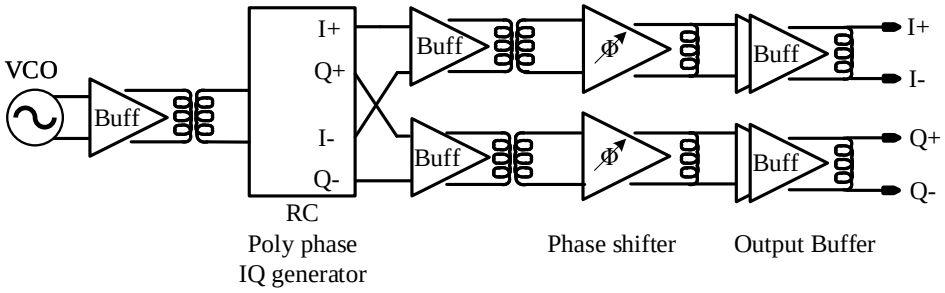

Figure 2.5: Proposed frequency generation chain for LO phase shifting receivers.

antennas. However, an example arrangement for 4 antennas is shown in Fig.2.6.

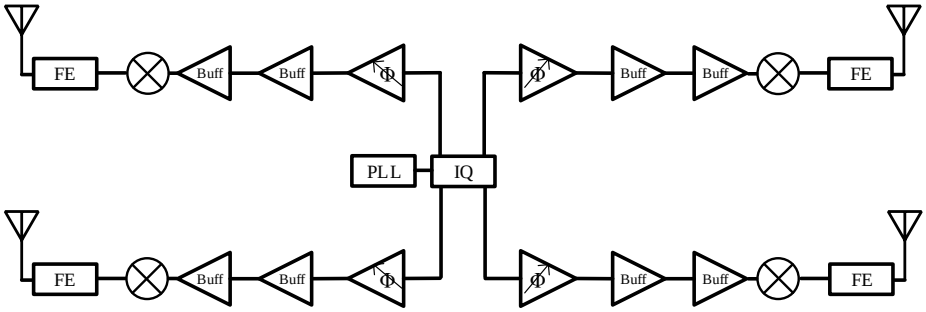

Figure 2.6: LO distribution arrangement for an array of 4 antennas.

Chapter 3

FD-SOI short-channel CMOS technology

Fig.3.1 shows a cross-section of an SOI transistor where the substrate is isolated by the buried oxide layer (BOX). Producing a thin film of single-crystal silicon and placing it on top of the amorphous silicon dioxide layer (SO_2) without applying any mechanical stress or electrical active defects kept researchers busy for a long time that it was only after the year 2000 that high-quality SOI wafers became available [13]. In this chapter, a brief discussion of the impact of short channel lengths, and SOI technology on CMOS is provided.

3.1 Impact of SOI

3.1.1 Power efficieny

The power consumption of a single CMOS transistor can be expressed in the simplest form as Eq.3.1

$$P = I_{leakage}V_{dd} + CV_{dd}^2 f \tag{3.1}$$

where C is the load capacitor, f is the operating frequency, V_{dd} is the supply voltage, and $I_{leakage}$ is the leakage current of the transistor. The first term of Eq.3.1 is static and the second part is the dynamic power dissipation. Despite the bulk technology in which the substrate and channel are connected, in SOI technology, the buried oxide layer isolates the channel and terminals from the substrate. Therefore, less DC leakage current and lower static power is dissipated. The dynamic power consumption is proportional to the value of the load capacitor which in this case, we assume that it includes only parasitic capacitors to substrate. A comparison between a typical 1-um bulk process to SOI shows that the

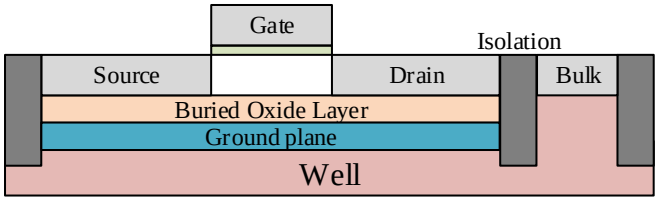

Figure 3.1: Cross section of an FD-SOI CMOS transistor.

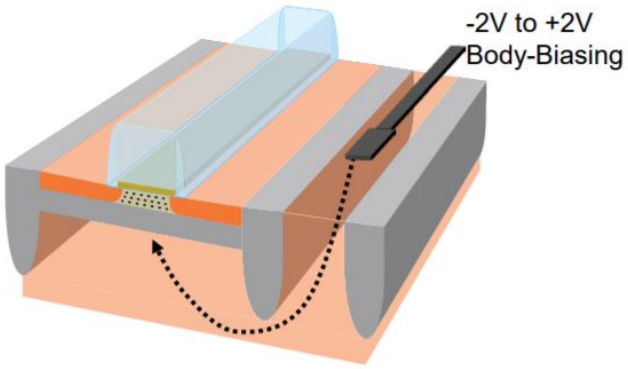

Figure 3.2: Body biasing Global Foundries for 22nm FDX process [14].

drain/source capacitor to the substrate of the SOI process is 4 to 7 times smaller [13]. Similarly, the same comparison shows that metal 1 to substrate capacitor in SOI is 40 % less which in turn, promises a lower capacitor per area.

3.1.2 Flexibility

Reducing parasitic capacitors not only contributes to a power-efficient system, but also, it provides a wider span of tunability for intra-terminal capacitors such as C_{gd} and C_{gs}. These capacitors can be tuned by regulating the biasing point of the transistor.
Additionally, SOI provides a flexible body biasing strategy for each transistor. As shown in Fig.3.2[14], by applying voltage potential over bulk terminal, the substrate can be highly polarized. Depending on the doping of the well for NMOS and PMOS transistors, the polarization can be either forward or reversely set. Forward body-bias (FBB) enables low voltage operation and the reverse body-bias (RBB) enables low leakage operation [14].

3.2 Impact of short channel

3.2.1 Power efficiency

By shrinking the parasitic capacitors, down scaling plays an indisputable role in reducing dynamic power dissipation as it is shown in Eq.3.1.

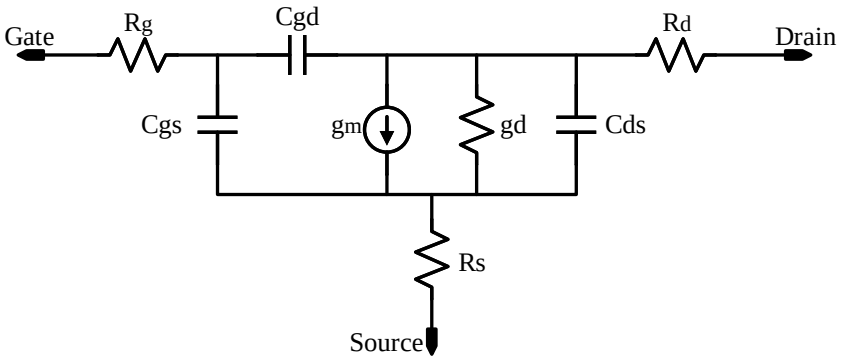

Figure 3.3: Small signal model of a MOSFET

3.2.2 Lower g_m/g_d and C_{gs}/C_{gd}

As described in Eq.3.2[15], by scaling down a CMOS transistor by factor of α, the total terminal capacitor experiences a reduction by the same factor.

$$\begin{aligned} C_{S/D} &= \frac{WE}{\alpha^2}(\alpha C_j) + 2(\frac{W}{\alpha} + \frac{E}{\alpha})C_{jsw} \\ &= \frac{1}{\alpha}\left(WEC_j + 2(W+E)C_{jsw}\right) \end{aligned} \tag{3.2}$$

where Cj is the bottom plate and $Cjsw$ is the sidewall capacitance. Considering the small signal model of a CMOS transistor provided in Fig.3.3, we can conclude that scaling down improves the intrinsic cut-off frequency proportionally, as it is elaborated in Eq.3.3. However, on the other hand, as the channel gets shorter the coupling between drain and gate becomes stronger and results in a lower ro and a larger C_{gd} which in turn causes a considerable decrease in g_m/g_d and C_{gs}/C_{gd} ratio occurs [16]. On the other hand, since the access resistances (rc, rg, and rd) do not decrease proportionally [16], according to the Eq.3.4. and Eq.3.5, a proportional drop in unity current and power gain cut-off frequency (f_T and f_{max}) occurs. Fig.3.4 shows the experimental investigation of this phenomena by Global Foundries for bulk process transistors[14] by which the f_{max} is extracted for different channel lengths. As it is shown, f_{max} makes a peak level for channel lengths between 40 nm to 60 nm and drops abruptly in shorter dimensions.

$$f_c = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{3.3}$$

$$f_T \approx \frac{f_c}{1 + \frac{C_{gd}}{C_{gs}} + (R_s + R_d)(\frac{C_{gd}}{C_{gs}})(g_m + g_d) + g_d} \tag{3.4}$$

$$f_{max} \approx \frac{f_c}{1 + \frac{C_{gd}}{C_{gs}} + \sqrt{g_d(R_s + R_g) + 0.5(\frac{C_{gd}}{C_{gs}})(R_s g_m) + (\frac{C_{gd}}{C_{gs}})}} \tag{3.5}$$

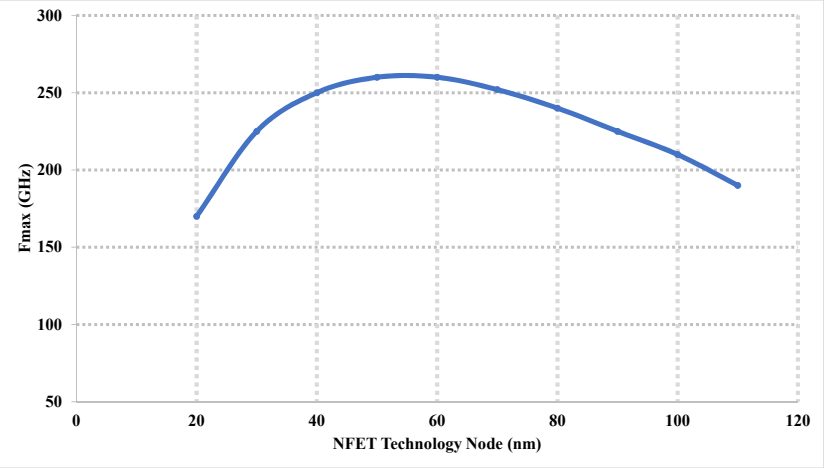

Figure 3.4: f_{max} compression for different technology node of NFET by Global Foundries [14].

3.2.3 Velocity saturation

Another important feature of shorter channel lengths is the velocity saturation effect by which the required Vds potential to maximize the charge acceleration, and accordingly, to saturate the drain current is lower than the known overdrive (pinch-off) point in long channel transistors [15]. Therefore, the Vds range by which the transistor stays in saturation mode is wider in short channel transistors.

Chapter 4

Tunable CMOS resonance circuits

Tunable LC resonance circuits are one of the main building blocks of any RF system. Fig.4.1 shows a parallel LC resonance tank where R_p illustrates the total resistance of the inductor and capacitor in parallel lumped model. Oscillation frequency of this circuit is calculated by Eq.4.1 and its Q-factor is quantified by Eq.4.2.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4.1}$$

$$\frac{1}{Q_t} = \frac{1}{Q_c} + \frac{1}{Q_L} \tag{4.2}$$

where, Q_c and Q_L are Q-factors of the capacitor and inductor in parallel model, and their values are calculated by Eq.4.3 and Eq.4.4 respectively.

$$Q_c = CR_C\omega_c \tag{4.3}$$

$$Q_L = \frac{R_L}{L\omega_c} \tag{4.4}$$

By assuming an equivalent parallel resistor as R_p, the Q-factor of the resonance circuit can be obtained by Eq.4.5.

$$Q = R_p\sqrt{\frac{C}{L}} \tag{4.5}$$

Frequency tuning can be done by adjusting both of the inductor and capacitor. However, due to the technical and area limitations, frequency tuning is majorly

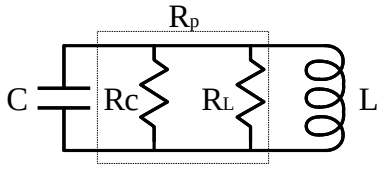

Figure 4.1: Parallel lumped model of an LC tank with parasitic resistance.

accomplished by adjusting the capacitive element. In the following, various tunable capacitors are discussed.

4.1 Varactor

Fig.4.2 shows a CMOS varactor and its distributed RC lumped model. Higher tuning range is achieved by increasing the length of the transistor. This results in a Q-factor degradation as for m-fold increase in channel length, m^2 fold drop in Q-factor is expected.[4]

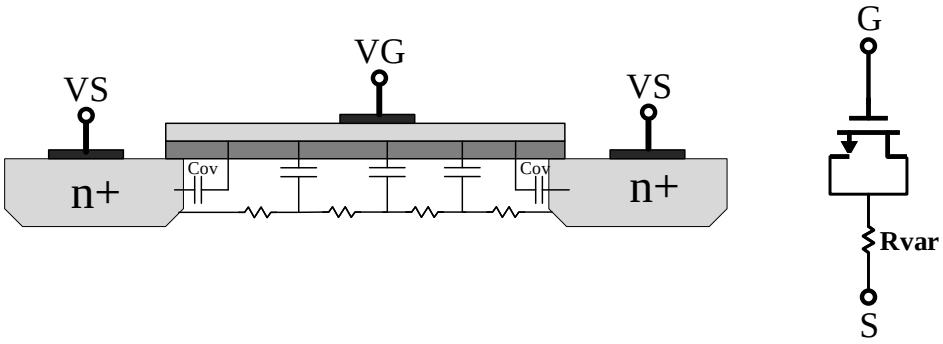

Figure 4.2: A CMOS varactor and its equivalent distributed lumped model[4].

4.2 Capacitor bank

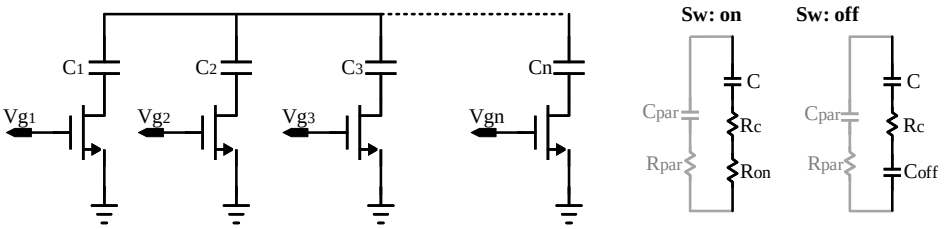

Figure 4.3: Switch capacitor bank and its simplified lumped model.

Fig.4.3 shows the schematic view of a common switched capacitor bank and its equivalent lumped model for each of "on" and "off" states where R_{par} and C_{par} model the substrate path loss, R_c is the resistance of the capacitor, R_{on} is the switch resistance, and C_{SWoff} is the parasitic capacitor of the switch which is equal to $C_{gd} + C_{gs}$. As shown in Eq.4.6 and Eq.4.7, the tuning range is limited by the equivalent parasitics. Q-factor of the capacitor bank is provided in Eq.4.8[4] which

indicates that increasing the tuning range results in wider range of Q variation .

$$f_{max} = \frac{1}{2\pi\sqrt{L(C_{min} + m(C_{PAR} + C_{SW,off})}} \tag{4.6}$$

$$f_{min} = \frac{1}{2\pi\sqrt{L(C_{max} + m(C_{PAR} + C_{SW,off})}} \tag{4.7}$$

$$\frac{1}{Q_t} = \frac{1}{Q_L} + \frac{1}{Q_1}\frac{C_1}{C_t} + \frac{1}{Q_2}\frac{C_2}{C_t} + ... + \frac{1}{Q_n}\frac{C_n}{C_t} \tag{4.8}$$

4.3 Cascode load

The intrinsic capacitors of a MOS transistor including C_{gd} and C_{gs} are bias dependent. As discussed in Chapter 3, in shorter channel lengths, C_{gd} takes more dominant stance in characterizing the frequency response of CMOS transistors. Despite its negative effect on gm stage, its contribution to load regulation is beneficial. One way to benefit from aforementioned advantage is to use of the cascode topology as shown in Fig.4.4.

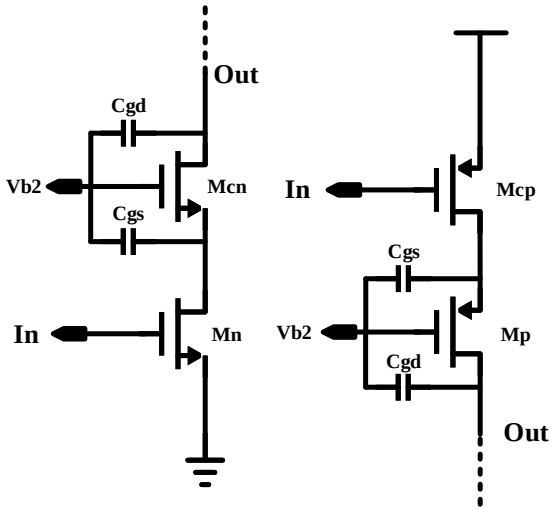

Figure 4.4: Cascode circuit for N and P channel transistors.

In this case, depending on the operation region of the cascode transistor, the output capacitance can be tuned. Fig,4.5, shows the small signal model for an NMOS cascode topology. the equivalent output impedance can be calculated by Eq.4.9.

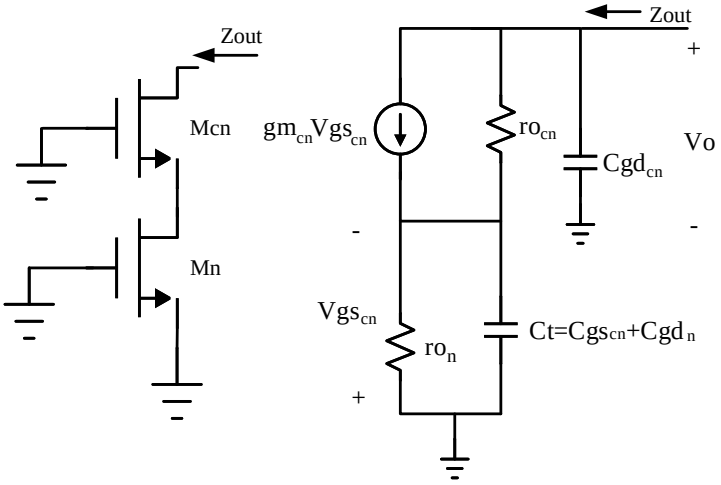

Figure 4.5: Small signal model of the NMOS cascode topology.

$$Z_{out}(\omega) = \frac{1}{j\omega Cgd_{cn}} || \left((ro_n || \frac{1}{j\omega C_t}) + ro_{cn} + gm_{cn}(ro_n || \frac{1}{j\omega C_t}) ro_{cn} \right) \qquad (4.9)$$

When the operation region of the cascode transistor moves from saturation to the Ohmic region. The intrinsic C_{gd} abruptly changes from WC_{ov} in saturation to $(0.5)WLC_{ox} + WC_{ov}$ in resistive region. Also, C_{gs} changes from $(2/3)WLC_{ox} + WC_{ov}$ in saturation to $(1/2)WLC_{ox} + WC_{ov}$ in the Ohmic region[15].
Ideally, it is not desired to have any change in operation region of the gm transistor (Mn). However, with a restricted power budget and lower supply voltage, Mn can exit the deep saturation region and cause a current reduction. Fig.4.6 shows the I-V plot of the input (Mn) and cascode (Mcn) transistors for this case. It is worth noting that thanks to the velocity saturation effect, the range by which Mn stays in saturation region is higher than long channel transistors.

To investigate the span of this variation, a test simulation is presented. In this setup the same circuits shown in Fig.4.4 are used, and the maximum allowed degraded DC current is set to 20 % of the nominal current. It is determined to keep the input transistor close to the saturation region while swapping the operation region of the cascode from deep triod to saturation. For this purpose, the supply voltage is set to 850 mV. |Vgs| of the input transistors and Drain of the cascode transistor both are set to 452 mV. Also, the maximum allowed Vgd is determined as 1.2 V. The simulation is repeated for different scaling of Mcn. As shown in Fig.4.7, after a certain width, NMOS and PMOS cascode transistors can provide Cgd_{max}/Cgd_{min} of 3 to 1 and 2.25 to 1 respectively.
In order to have more control over the Q-factor and tuning resolution, complementary architecture is used. According to the post-layout simulations, the proposed solution, provides $Cout_{max}/Cout_{min}$ of 1.8 with average Q-factor of 10.

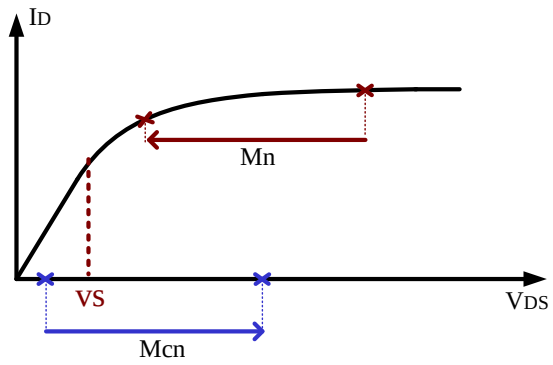

Figure 4.6: Operation regions of transistors Mn and Mcn when gate bising of the Mcn is regulated.

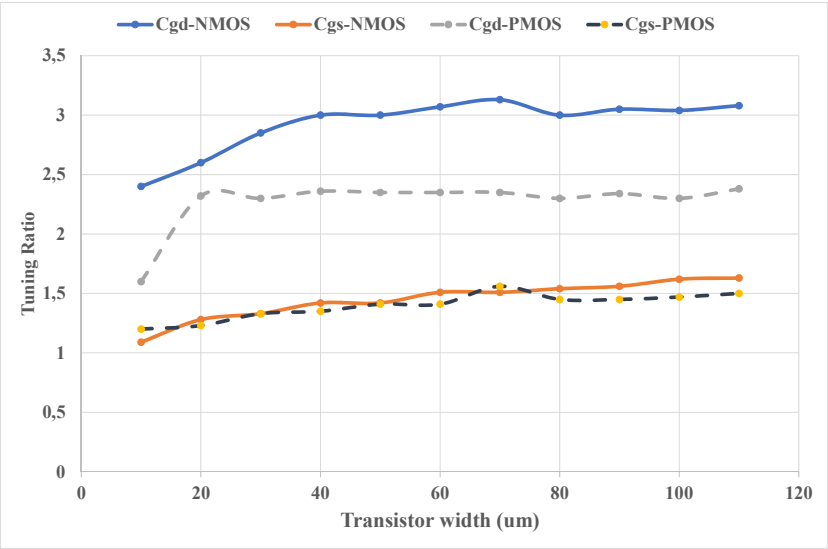

Figure 4.7: Intrinsic C_{gs} and C_{gd} variation for PMOS and NMOS cascode transistors.

Chapter 5
Phase shifter

As explained in Chapter 2, to accomplish constructive wave summing, phased array receivers require the phase steering procedure. In this chapter, the common architectures, and the proposed design are discussed. The simulated results include post-layout RC extraction and electromagnetic (EM) views for individual inductors by Momentum Keysight. This excludes the mutual coupling effect between inductors.

5.1 Phase shifting techniques

There are various ways to generate quadrature signals. As the most straightforward approach, the phase can be generated within the frequency synthesizer. For instance, as shown in Fig.5.1, by applying a ring connection between multiple amplifiers[17][18], multiple phases are generated. Although the power consumption of this approach is high, it provides all phases in a synchronized loop. In an alternative approach, the phase of the oscillator is adjusted by locking an additional oscillator to the main one. A simplified model of this technique is provided by Fig.5.2. In this case, the phase shift can be quantified by Eq.5.1[19].

$$\Phi \approx \arcsin\left(\frac{2Q}{\omega_0}\frac{I_{osc}}{I_{inj}}(\omega_0 - \omega inj)\right) \tag{5.1}$$

where Q is the quality factor of the tank circuit, I_{osc} is the current of the main oscillator and I_{inj} is the current of the injected oscillator. Also, the ω_0, and ω_{inj} are resonance frequencies of the main and injection oscillator respectively. The output frequency is determined by injecting oscillator and the desired phase shift can be achieved by changing resonance of the main oscillator in range of $\omega_0 \pm \omega_L$ called as locking range [20]. By doing so, a phase shift in the range of $(-\pi/2, \pi/2)$ for single output, and 2π for differential output can be achieved. For example, in [12], this solution is implemented on a sub-harmonic injection locking multiplier to accomplish the LO generation of a distributed PLL architecture and phase-shifting together. This solution provides unwanted spurs [12]. Vector modulation is another technique by which, first, the quadrature of the signal is generated and after weighing each quadrant they are summed together. This technique requires

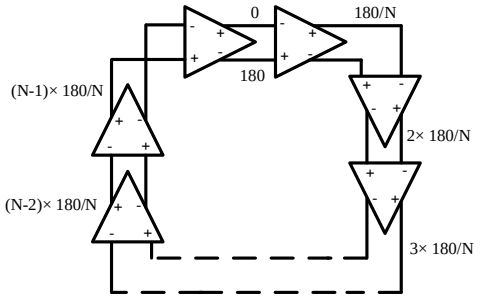

Figure 5.1: Multi-phase oscillator.

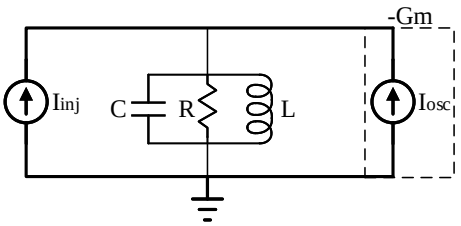

Figure 5.2: Phase shift by injection locking.

a quadrature input, and provides only differential output. An example of the implementation of this method on the LO path can be found in [21]. The phase shift can be achieved by adjusting the electrical length of the transmission line in the signal path. For example, in [22], phase shifting is implemented by transmission lines and switched capacitors. The problem in this case is the large form factor. An alternative way is to use lumped reflection type phase shifters (RTPS) which provides a compact solution for phase-shifting where, by tuning the lumped companent, the input reflection coefficient of the load, and consequently, phase of the output signal is adjusted. For example in [23], the 360-degree phase shift is achieved by cascading π networks. Or, in [24], a tunable LC tank provides a 100-degree phase shift.

5.2 Phase shifting block

Among various topologies, reflection-type phase shifters (RTPS) can provide a compact and spurs free phase shifting. A single-pole LC tank shown in Fig.4.1 is the simplest topology for this purpose. In this case, the impedance function of the tank is calculated by Eq.5.2.

$$Z(f) = \frac{R}{1 + jQ(f/f_0 - f_0/f)} \tag{5.2}$$

where f_0 is the resonance frequency of the tank provided in Eq.4.1, and Q is the quality factor of the tank calculated in Eq.4.5. The phase of the impedance can be

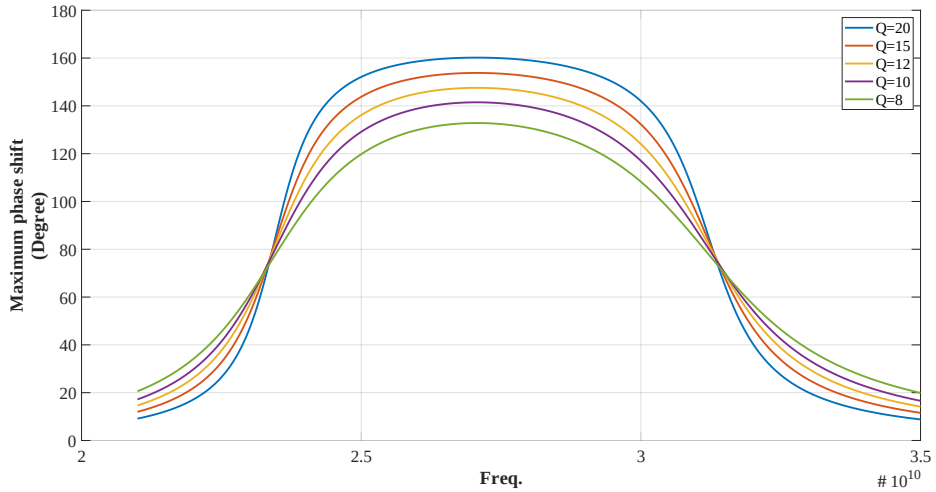

Figure 5.3: Maximum achievable phase range for 1.8 times tuning ratio for capacitor and different Q-factor values.

derived by Eq.5.3. Ideally the phase shift can range from $(-\pi/2, \pi/2)$. However, for limited Q-factor and tuning range, the phase shift range becomes limited.

$$\Delta\Phi = \frac{\pi}{2} - \arctan\frac{L\omega_0}{R(1 - LC\omega_0^2)} \tag{5.3}$$

Fig.5.3, shows the mathematical simulation for maximum achievable phase shift by an LC tank for different Q-factors when the inductor is 200 pH and the capacitive element varies from 130 fF to 230 fF (ratio of 1.77). Based on Fig.5.3, for a given tuning range, minimum Q-factor of 8 is required to achieve at least 90 degree phase shift within the targeted bandwidth. Fig.5.4 shows the produced AM-to-PM of the same setup. According to the Fig.5.4, up to 8 dB amplitude error can be expected. Therefore, the consequent buffers should provide at least 8 dB gain to compensate the amplitude variations.

The block view and lumped model of the proposed LO phase shifting unit and their schematic circuits are shown in Fig.5.5 and Fig.5.6 respectively. the tunable resonance is accomplished by the cascode transistor as it is explained in chapter 4. The scaling of the input transistors for the NMOS pair is 12um/18nm and for PMOS is 20um/18nm. Also as cascode pairs, scaling for the NMOS is 80um/32nm, and for PMOS it is 60um/32nm. In order to provide sufficient bandwidth, an additional resonance is placed at the load of the second buffer. Therefore, the acquired transfer function can perform a band-pass characteristic. The first resonance has an inductor value of 200 pH and its tunable capacitor varies from 130 fF to 230 fF (ratio of 1.77). In order to calculate the second pole, and consequently, to obtain the value of the second inductor and capacitor, the transfer function of the provided lumped model shown in Fig.5.5 is simulated. Therefore, the $L_2 = 190pH$ and $C_{Load} = 70fF$ is determined. Fig.5.7 shows the AC gain of the proposed

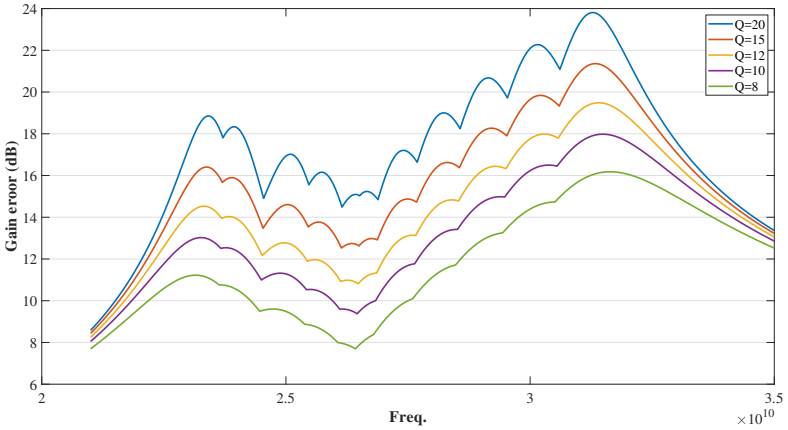

Figure 5.4: Amplitude modulation due to the phase shift (AM-to-PM).

chain by which approximately 7 dB is provided by the phase shifter and 8 dB by the consequent buffers. the differential phase shifter consumes 5.6 mW and the consequent differential buffers consume 5.4 mW in total. The maximum achieved phase shift of the chain is provided by Fig.5.8. Compared to the Fig.5.3, the obtained phase range is narrower. This is mainly due to the effect of the additional resonance (C_{Load} L_2) which is used for bandwidth enhancement. The AM-to-PM error is calculated by Eq.5.4, and is shown in Fig.5.9. The chain is terminated by the C_{load} which can be merged by the mixer input capacitor. In this case the delivered power is provided by Fig.5.10. Fig.5.11 shows the layout view of the phase shifter and its consequent buffers. The occupied area for the differential phase shifter and the consequent buffers are 0.019 mm^2 (210 um × 90 um), and 0.017 mm^2 (210 um × 80 um) respectively. Table.5.1, provides a performance comparison to some of the state-of-the-art designs.

$$AM_{error} = 20\log(\frac{Amp_{max}}{Amp_{min}}) \tag{5.4}$$

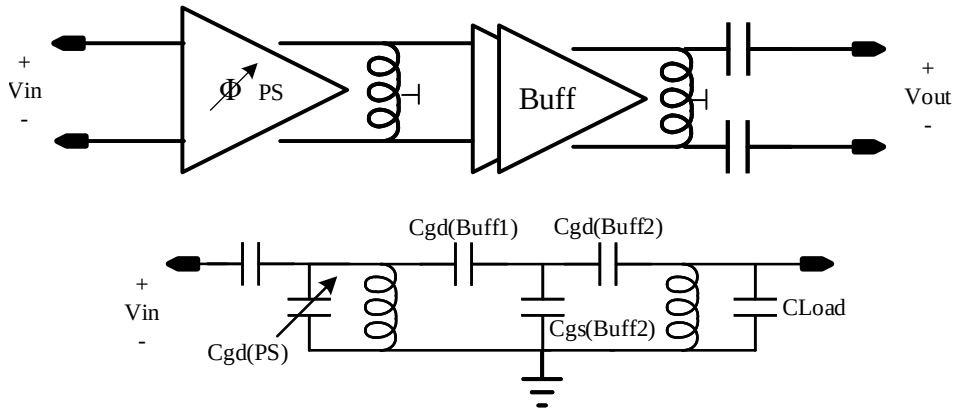

Figure 5.5: proposed LO phase shifting unit.

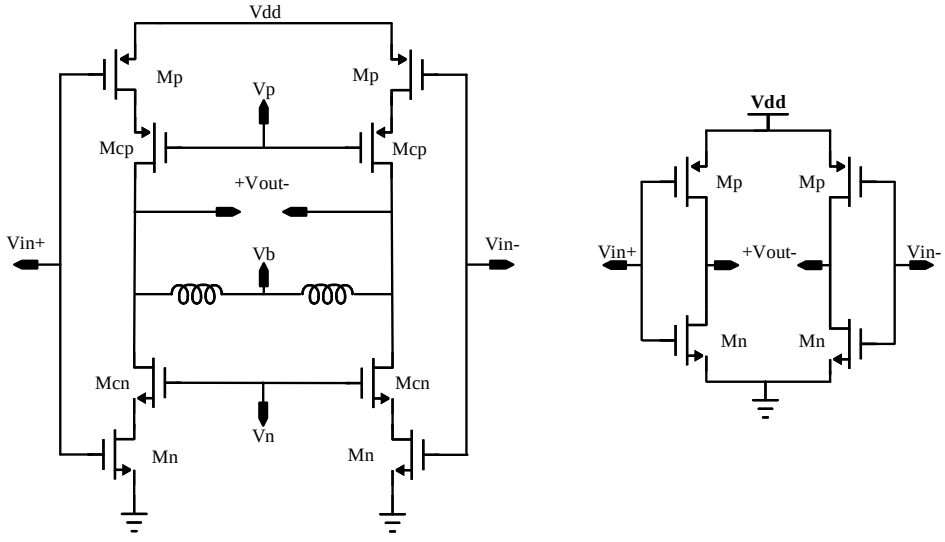

Figure 5.6: (a) proposed differential phase shifter (b) following differential buffers.

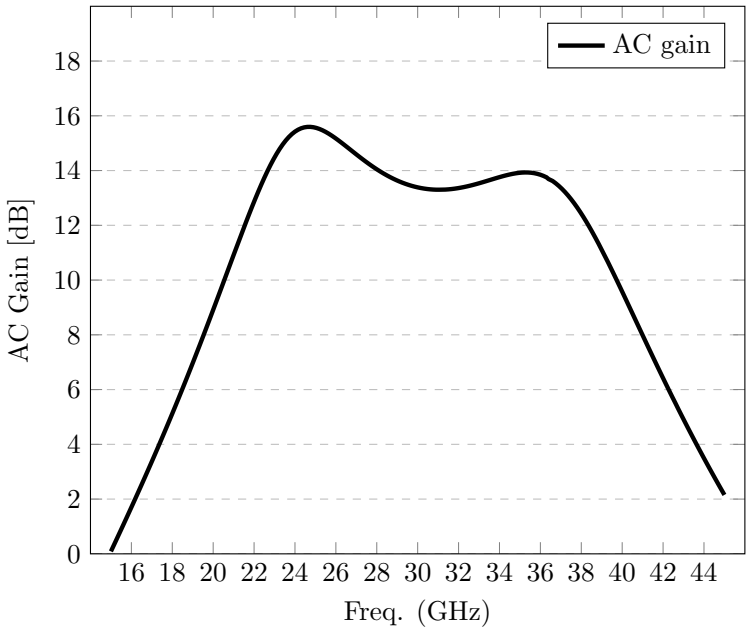

Figure 5.7: small signal gain of the phase shifting chain.

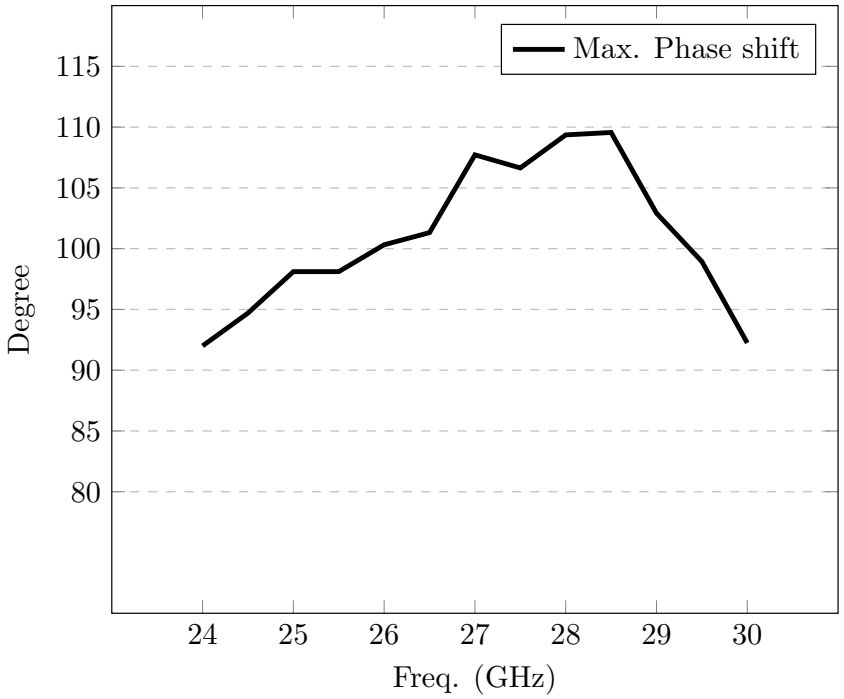

Figure 5.8: Maximum achievable phase shift versus frequency.

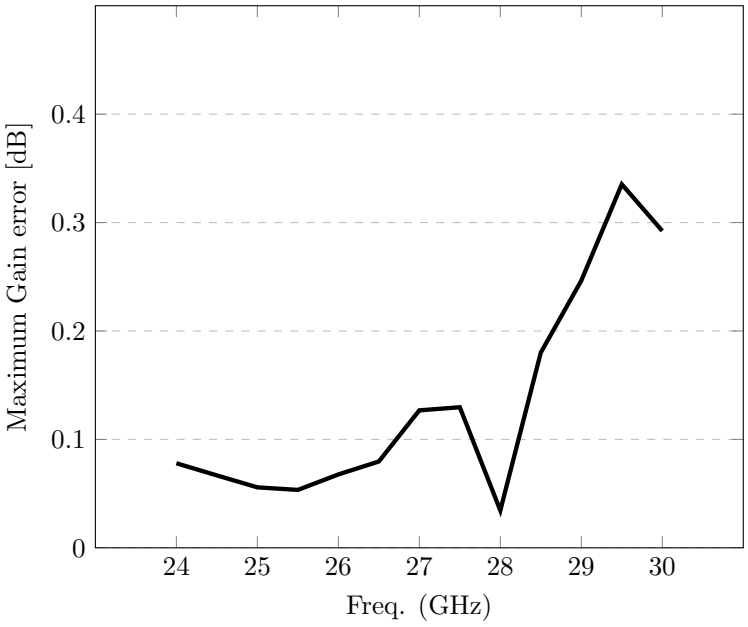

Figure 5.9: Maximum AM-to-PM error within the band of interest.

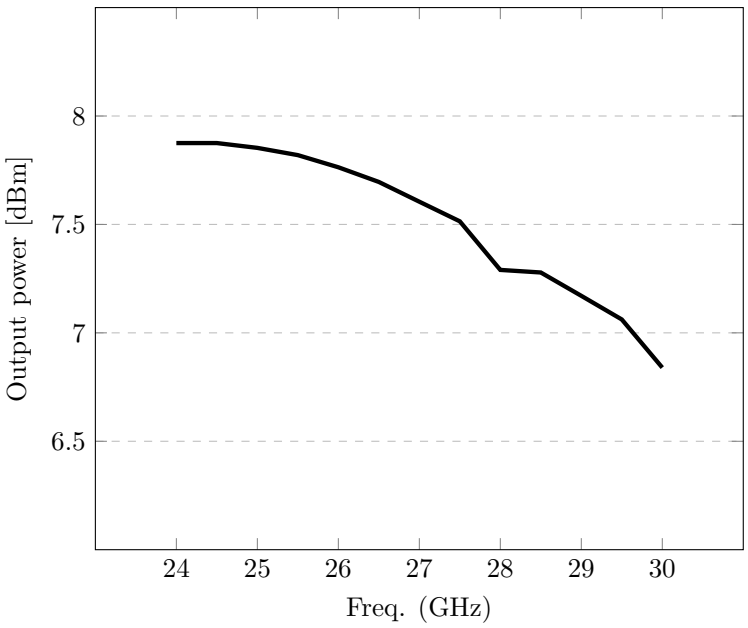

Figure 5.10: Output power over the load capacitor.

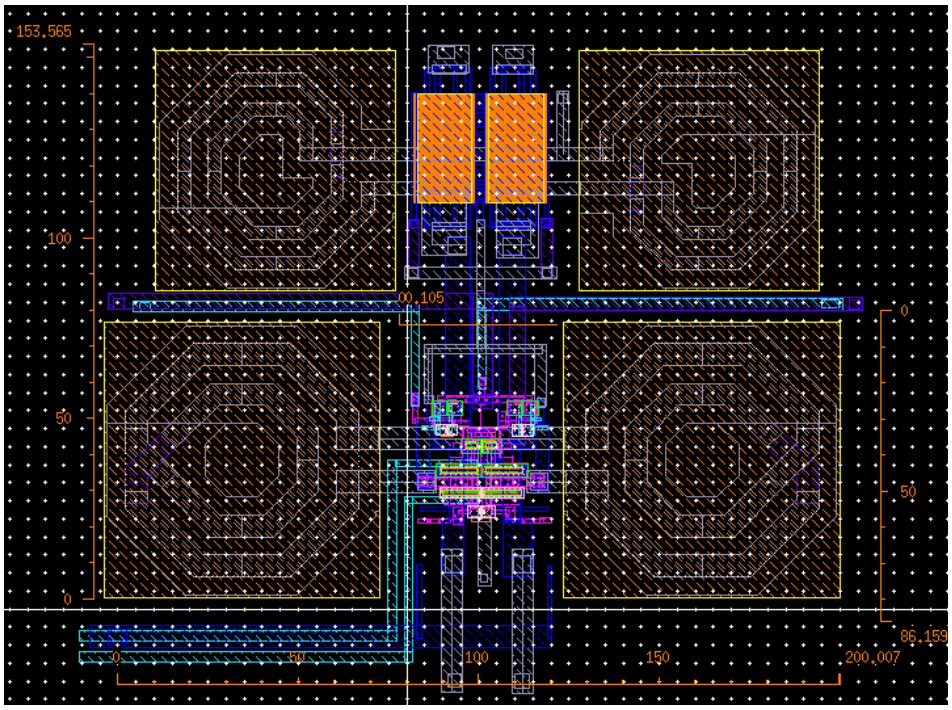

Figure 5.11: Layout view for the differential pair of the proposed phase shifter and its following buffers .

Ref.	[20]	[23]	[22]	[24]	**This work**
Tech.	CMOS 65nm	CMOS 65nm	CMOS 40nm	CMOS 65nm	CMOS 22nm FD-SOI
Topology	IL + tripler	RTPS $\pi - network$	Transmission Lines+ divider	Resonance tank	Resonance tank
Freq (GHz)	42.75 - 49.5	28	44-54	28	24.25 - 29.5
Range (Degree)	± 30 $\times$ 3	360	360	± 50	93-110 Per quadrant
Amplitude Error (dB)	± 0.4	0.3 RMS	-	0.04/0.15 RMS/Amplitude	0.25 Amplitude
Phase Resolution	22.5°	11.25°	5.4°	2+3+10 bit/0.3 ° SWcap+Varactor	Continuous
Insertion Loss (dB)	-	7.45 - 8.05	-	-	-
Power (mW)	55 4 cores Differential	-	16.9 Differential	PS: 10.3 Buffer: 16.6 Differential	PS: 2.8 Buffer:2.7 Per quadrant
Area (mm^2)	-	0.16 RTPS	0.143 TLine+Divider Differntial	0.25 Buffer+PS Differential	PS: 0.019 Buffer: 0.017 Differential

Table 5.1: Performance comparison with state-of-the-art designs.

Chapter 6

IQ generation

Ideally, in-phase and quadrant signals are expected to have the same amplitude with a 90 degree phase difference. Any degradation of quadrants either in magnitude or phase is known as I/Q mismatch. Image rejection ratio (IRR) is a standard term to quantify the quality of quadrature generation. IRR is calculated by Eq.6.1 [4]

$$IRR(dB) = 10\log\left(\frac{(1+\epsilon)^2 + 2(1+\epsilon)\cos\Delta\theta + 1}{(1+\epsilon)^2 - 2(1+\epsilon)\cos\Delta\theta + 1}\right) \tag{6.1}$$

where ϵ denotes the relative gain error, and θ is in radians. The rendered I/Q mismatch leads to BER and limits the maximum achievable data rate. For example, based on [25], at least 35 dBc IRR is required to achieve BER = 0.001 for 64-QAM modulation.

6.1 LO quadrature generation techniques

Quadrature LO can be generated in various ways. The most straightforward method is to use a quadrature voltage-controlled oscillator (QVCO)[26][27]. Although the use of QVCO reduces the power consumption remarkably, its phase accuracy shows a strong trade-off with its tuning range which similarly holds the same trade-off with its phase noise. As an alternative approach, the quadrature generation can be accomplished by injection locking dividers (ILFD) [28]. This method comes with phase noise penalty since the Q-factor of the passives at its input and output frequencies do not hold the same value and the output quadrature provides higher phase noise compared to that of a VCO at the divided frequency. In another approach, the quadrature wave is generated by placing poly-phase filters on the LO path. Such filters can be constructed in various ways. Resistive capacitive (RC) PPFs [29][30][31] are among the most common architectures, such filters provide low form factor, but, a narrowband solution. Increasing their bandwidth requires either use of higher-order of the filter which in turn, imposes a great power loss or to use lower orders with dynamic calibration [32]. Inductive-capacitive (LC) topology is another type of PPFs which can enhance the quadrature bandwidth with a lower power penalty. However, such improvement comes with a form factor price. Transformer [33] and coupler [34][35][36] based solutions are other alternatives which almost share the same shortcomings as LC PPFs provide.

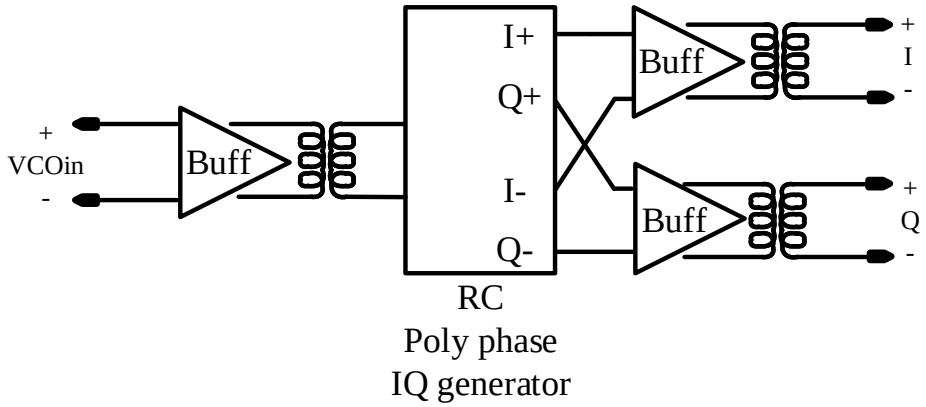

Figure 6.1: Quadrature generation block.

The advanced silicon solution has shown great potential in developing agile calibration units by which the electrical parameters of circuits can be dynamically adjusted to meet a wider span of specifications. This paves the way for simpler and more power-efficient solutions.

6.2 Quadrature generation block

The provided results in this chapter do not cover the layout. However, transistors are provided by foundries practical models, and passives include their EM extracted views. Also, the chain is loaded by the phase shifters provided in the previous chapter.
Fig.6.1 shows the proposed quadrature generation block including a single-stage tunable RC-PPF, and active resonance units at its input and output to improve LO isolation, and to compensate for the power loss of the PPF. The use of transformers provides an easier inter-connection between stages, and enhances the bandwidth.
RC-PPFs are placed in two categories: (a) Constant gain (b) constant phase [30]. In this design, As shown in Fig.6.2, a constant gain PPF has been designed. The transfer function for I and Q path to the input can be calculated by Eq.6.2 and Eq.6.3. Also, the transfer function of I path to Q path can be obtained by Eq.6.4.

As shown in Eq.6.4, the filter provides a constant gain for all frequencies and 90° phase difference at the pole frequency ($\omega = 1/(RC)$). In order to maintain the same phase for the entire bandwidth, the dominant pole must be tuned. Therefore, a tunable resistor is created by channel resistance of NMOS transistors which can be adjusted under different biasing. Also, simple complementary buffers shown in Fig.6.2 have been used at the input and output of the PPF to compensate the gain, and to provide a flat frequency response.

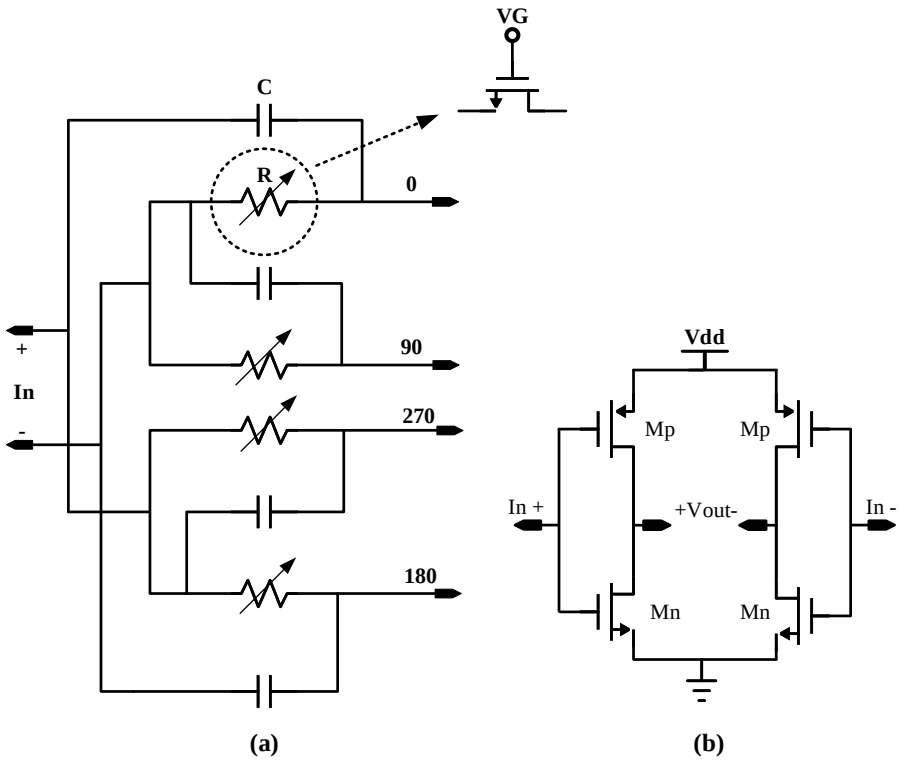

Figure 6.2: a) Constant gain PPF b) Buffer

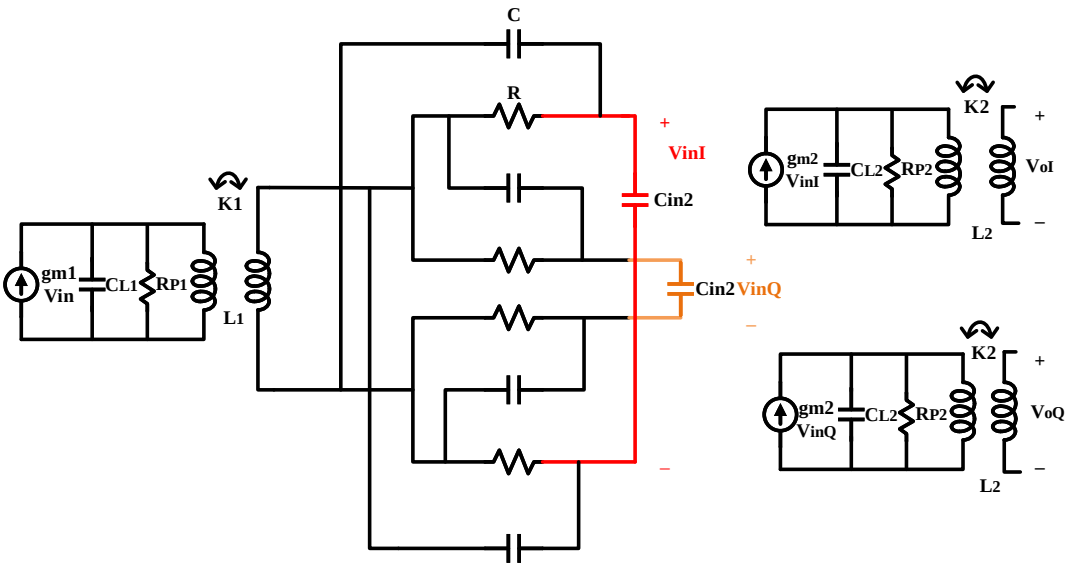

Figure 6.3: Small signal model of the IQ chain.

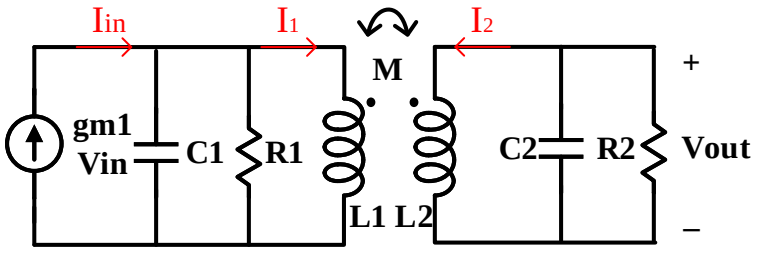

Figure 6.4: Small signal model an active buffer loaded by a coupled resonator.

The design procedure starts with specifying the single pole of the PPF. In this design, we set the resonance frequency at 28 GHz. Therefore, 40 fF and 140 ohm for capacitor and resistor are achieved. The resistor is created by channel resistance of an NMOS transistor with dimension of 3um/22nm. Then by use of buffer stages, the bandwidth is enhanced. Small signal model of the combination is shown in Fig.6.3. If we neglect their mutual loading effect, the transfer function of each of I and Q path can be obtained by multiplying gain transfer function of cascaded stages. Transfer function of the stand alone PPF for both I and Q paths is provided by Eq.6.2, and Eq.6.3[31]. Also, for buffers which are loaded by transformers, a model of Fig.6.4 is used. In this case, the transfer function can be

derived by Eq.6.5-Eq.6.8.

$$\Delta H_{I(j\omega)} = \frac{Z_L}{R + Z_L + (jw)RCZ_L}(1 - j\omega CR) \tag{6.2}$$

$$\Delta H_{Q(j\omega)} = \frac{Z_L}{R + Z_L + (jw)RCZ_L}(1 + j\omega CR) \tag{6.3}$$

$$\frac{\Delta H_{I(j\omega)}}{H_{Q(j\omega)}} = \frac{(1 - j\omega CR)}{(1 + j\omega CR)} \tag{6.4}$$

$$V_{out}(s) = I_2(L_2 s) + MI_1 s \tag{6.5}$$

$$I_2(s) = -\frac{V_{out}(R_2C_2 + 1)L_2 s}{R_2} \tag{6.6}$$

$$I_1(s) = \frac{R_1 L_1 s}{R_1 + L_1 s(R_1 C_1 s + 1)} I_{in} \tag{6.7}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = gm\frac{Q_2 Q_1 M L_1 s}{(Q_2 + \frac{s}{\omega_{02}} + \frac{Q_2}{\omega_{02}^2}s^2)(Q_1 + \frac{s}{\omega_{01}} + \frac{Q_1}{\omega_{01}^2}s^2)} \tag{6.8}$$

where M is a function of mutual coupling factor and is calculated by Eq.6.9[4].

$$M = k\sqrt{L_1 L_2} \tag{6.9}$$

Based on the model, the first transformer is set to be 2:1 with an inductance of 200 pH and the second transformer is 1:1 with an inductance of 230 pH. Both of the transformers are generated by the design kit and their EM extracted views have been used. Fig.6.5, shows the small-signal gain of the chain. The tuning gate voltage ranges between 1 V to 1.23 V with a step size of 30 mV. Fig.6.6, shows the IRR value before and after calibration, and the calibrating gate voltage for NMOS transistors of PPF. After calibration within the bandwidth, the gain response undergoes a variation. Fig.6.7 shows the output power of the IQ chain after calibration when it is loaded by the phase shifter. The IQ buffers together consume 15.8 mW.

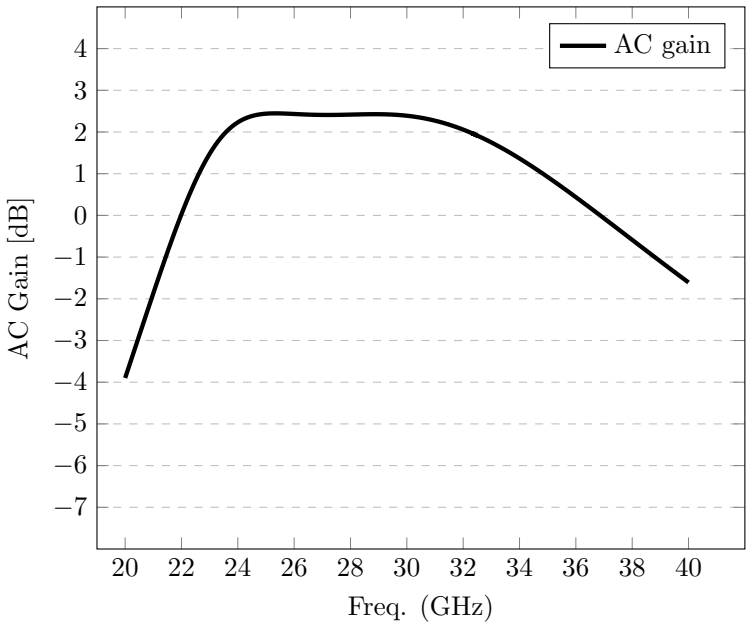

Figure 6.5: Small signal gain of the IQ chain

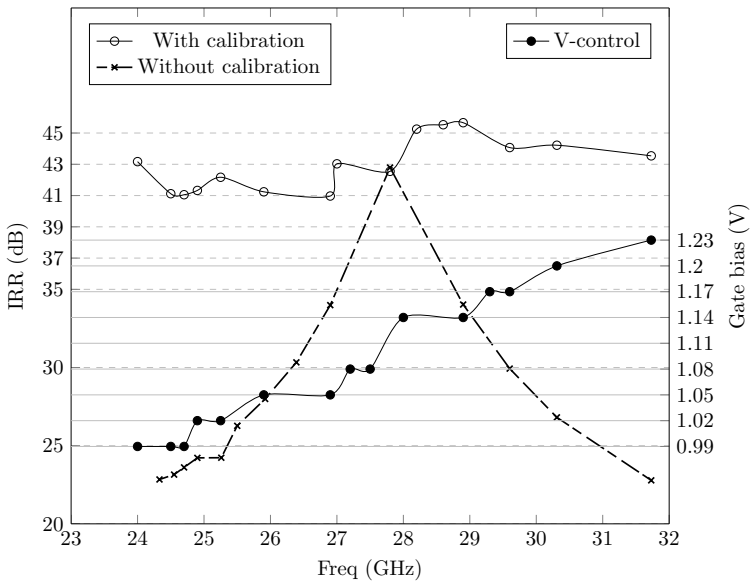

Figure 6.6: IRR with and without calibration with calibrating voltage.

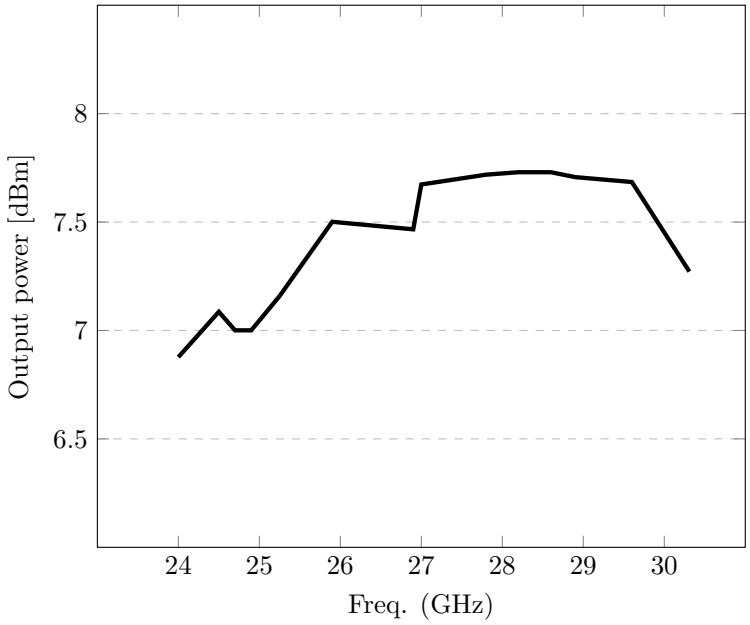

Figure 6.7: Output power level of the IQ unit after calibration, loaded by the consequent phase shifitng block.

Chapter 7

Voltage controlled oscillator

7.1 Challenges and limitations

According to Barkhausen theorem, any negative feedback shown in Fig7.1. which can provide conditions of Eq.7.1 and Eq.7.2 can produce an oscillation.

$$|H(s = j\omega)| = 1 \tag{7.1}$$

$$\angle H(s = j\omega) = 180^\circ \tag{7.2}$$

where, $\angle H(s = j\omega)$ is the frequency dependent phase shift [15]. LC cross-coupled oscillators are among the most popular solutions for frequency synthesising. As shown in Fig.7.2, in such oscillators, the resonance frequency is determined by a passive LC tank circuit and the loss of the tank is cancelled by a negative transconductance to provide the oscillation condition in Eq.7.1. There are various ways to implement such VCOs. However, amongst topologies, complementary push pull VCOs are known to be the right candidate for low-power operations. This is due to the fact that NMOS and PMOS pairs re-use the same DC current in a push pull way, and provide twice of the transconductance as those of only NMOS or PMOS VCOs[37] [38].
To tune the oscillation frequency, the dominant pole of the transfer function in Eq.7.1 must be tuned which translates to adjusting the resonance tank of the oscillator. Similar to the phase shifter design, the cascode load is used to create the equivalent capacitor. This implementation is shown in Fig.7.3 where the dimensions for each transistor setermines as following: Mn= 15um/18nm, Mcn= 60

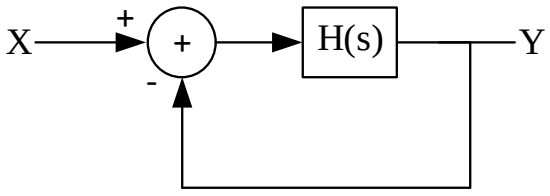

Figure 7.1: Negative feedback system.

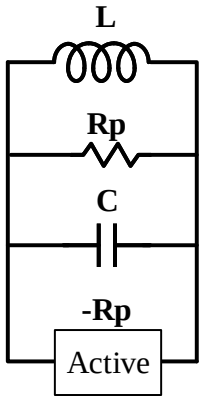

Figure 7.2: Lumped model of a cross coupled LC oscillators.

um/32nm, Mp= 22um/18nm, Mcp= 70um/32nm. Also the inductors L and Ls are 220 pH, and 160 pH respectively.

The generated phase noise at the output of the PLL can crucially undermine the SNR of the transceiver and deteriorates its spectral efficiency [39]. In LC oscillators, the phase noise at $\Delta\omega$ away from the oscillation frequency (ω_0) can be calculated by Eq.7.3 [40].

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{2FkT}{P_{Sig}}\left(1+(\frac{\omega_0}{2Q\Delta\omega})^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right) \tag{7.3}$$

where, P_{sig} is the power level of the signal, k is the Boltzmann constant, T is the temperature in Kelvin, Q is the quality factor of the LC tank, F includes white noise, and $\Delta\omega_{1/f^3}$ includes the flicker noise of the active device. Wider tuning range comes with the price of higher phase noise variation. This shortcoming stems from the fact that the tuning element which mostly is either a varactor or a capacitor bank, fails to provide the same Q-factor over the tuning range. As a result, the phase noise which is inversely proportional to the Q-factor of the tank undergoes a consequent degradation. In order to enhance the quality factor of the VCO, the tail nodes of the oscillator shown in Fig.7.3 are loaded with inductors to provide a high impedance node for its second harmonic current signal.

7.2 VCO and performance evaluation

All the presented results include the post-layout effects which are modeled by RC-extraction and EM views of the inductors. Fig.7.4 shows the layout view of the oscillator and its consequent output buffer. The design occupies 0.025 mm^2.

By the use of periodic steady-state (PSS) analysis, the phase noise values at 1 MHz and 10 MHz are obtained as shown in Fig.7.5. Also, the DC power consumption is presented in Fig.7.6. In order to include all the trade-offs, oscillators are often evaluated by standard units known as figure-of-merit (FOM). FOM can be calculated by Eq.7.4. Furthermore, to include tuning range and area FOMt and

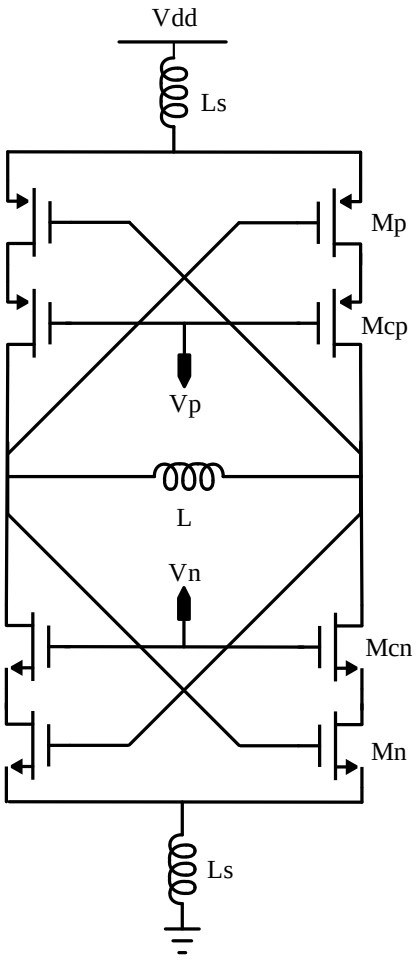

Figure 7.3: Schematic of the designed VCO.

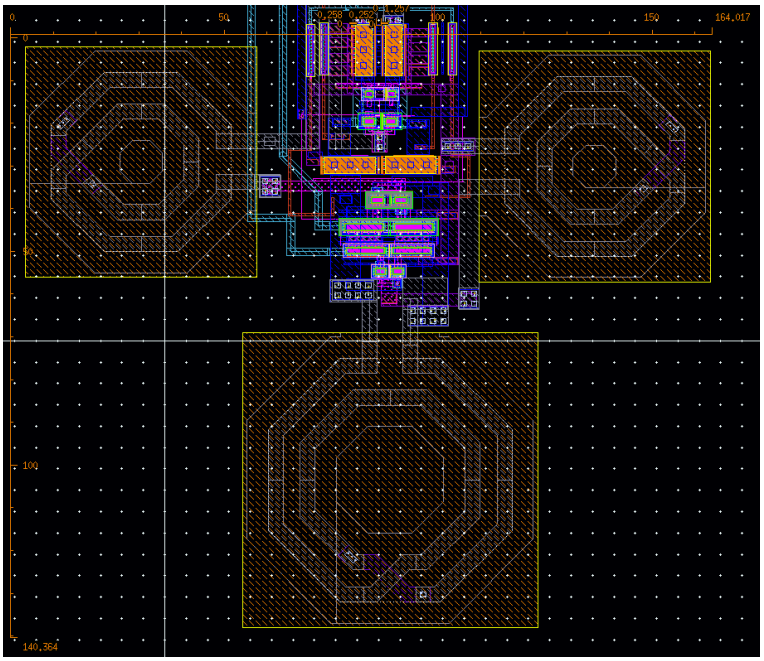

Figure 7.4: Layout view of the VCO and its consequent buffers.

FOMa are often reported. FOMt, and FOMa is provided by Eq.7.5-7.6 respectively.

$$FoM = PN - 20\log\left(\frac{f_0}{\Delta f} + 10\log(\frac{Pdc_{mW}}{1mW})\right) \tag{7.4}$$

$$FoM_t = PN - 20\log\left(\frac{f_0}{\Delta f}\frac{TR}{10} + 10\log(\frac{Pdc_{mW}}{1mW})\right) \tag{7.5}$$

$$FoM_A = FOM + 10\log(\frac{Area(mm^2)}{1mm^2}) \tag{7.6}$$

Table.7.1, provides a performance summary and comparison of the designed VCO and state-of-art designs.

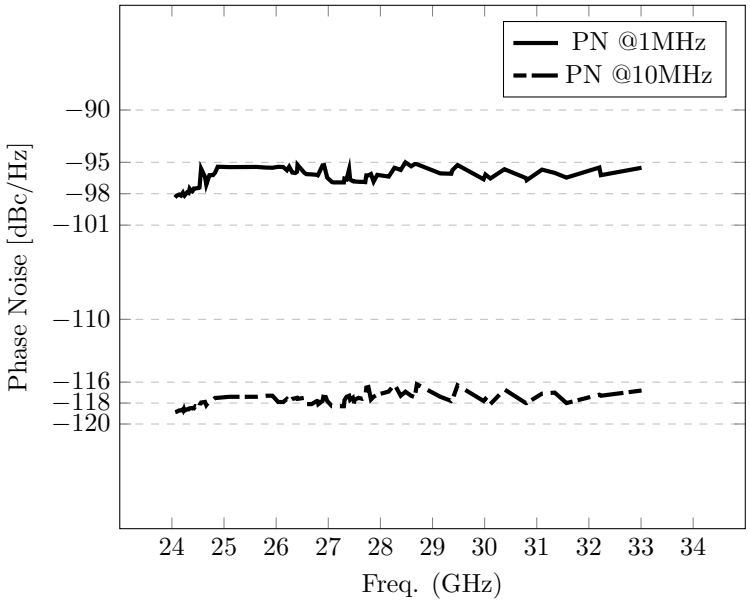

Figure 7.5: Phase noise of the VCO at 1 MHz and 10 MHz offset.

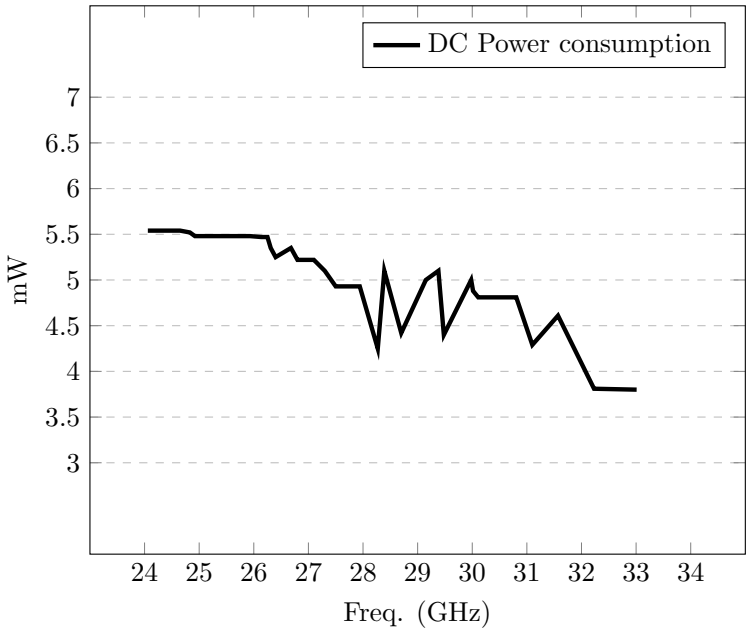

Figure 7.6: DC power consumption of the designed VCO.

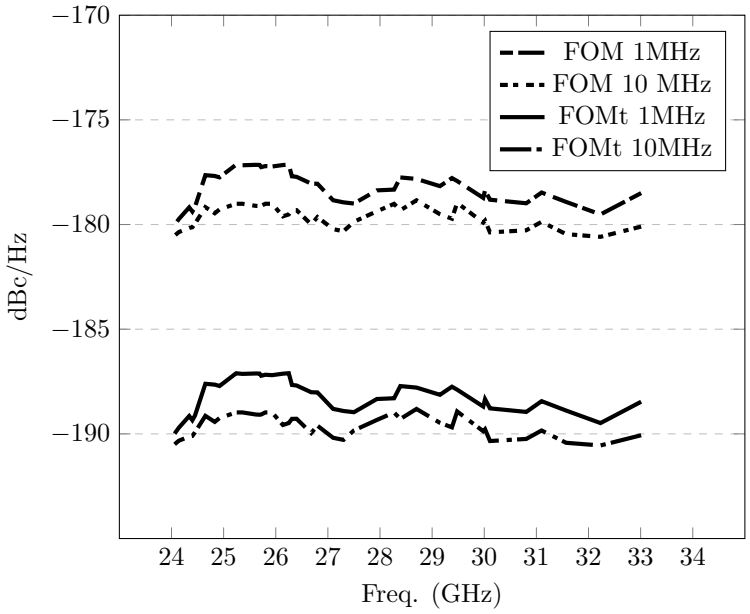

Figure 7.7: FoM and FoMt at 1 MHz and 10 MHz for the designed VCO.

Ref.	[41]	[42]	[43]	[44]	[45]	**This work**
Tech.CMOS	32nm- SOI	65nm	28nm	65nm	65nm	22nm-SOI
Freq (GHz)	29.24-31.56	26	27.3-31-2	26.3	26.5	24-33
PN (dBc/Hz)	-128 @10 MHz	(-115.4)-(-122.8) @10 MHz	-126 @10 MHz	-121 @10 MHz	-105.8/-130 @1/10 MHz	(-117)-(-119) @10 MHz
TR (%)	7.6	40.3	14	20.1	14	31.5
Power (mW)	4.56	4.3±0.3	11.58	2.3	10.8	5.1
Area (mm^2)	0.3	0.05	0.15	0.22	0.022	0.025
FOM (dBc/Hz)	-190.9	-180±2.5	(-177) -(-181)	-185.8	-184/-188 @1/10 MHz	(.178)-(-181) @10 MHz
FOMt (dBc/Hz)	-188.5	-192.1±2.5	-187.55	-191.8	-186/-191 @1/10 MHz	(-187.8)-(-196.6) @10 MHz
FOMA (dBc/Hz)	-196.12	-193±2.5	(-185.23) -(-189.23)	-192.4	-200.6	-197.62

Table 7.1: Performance comparison with state-of-the-art VCO designs.

Chapter 8

Conclusion and future work

8.1 Conclusion

By developing the cellular network to mm-wave ranges, power consumption and form factor have become a great challenge in developing their corresponding UE devices. This is partially due to the multi-path architecture of phased array topologies, and partially, due to the parasitic of the technology. 5G-NR-FR2 operates in TDD modulation scheme. Therefore, the LO chain can be shared between RX and TX. This makes the LO path phase shifting architecture an optimum candidate for smaller arrays. In this regard, this work benefited from Global foundry's 22nm-FD SOI CMOS technology and presented a compact and low-power LO phase-shifting chain for direct conversion phased array transceivers operating in sub-30 GHz bands including bands n257, n258, and n261.
The design presented an LO chain including phase shifters, IQ generation, and a VCO. The phase shifter block provides 93-110 degree phase shift for each quadrant, and consumes 2.5 mW and occupies only 0.01 mm^2. The PPF provides at least 40 dBc of IRR, and consumes 15.8 mW. Also, the VCO provides 31.5 % tuning range, consumes 5.1 mW and produces -98 to -95 dBc/Hz phase noise at 1 MHz, and -117 to -119 dBc/Hz at 10 MHz offset. The VCO occupies 0.025 mm^2.

8.2 Future work

As it is presented, the quadrature generation unit consumes the major portion of the chain's power budget. By the use of QVCOs, the power can be considerably reduced. However, the challenge is to maintain the quadrature accuracy for the target tuning range (5.25 GHz). In this case, a QVCO in conjunction with the phase correction loop can provide the required IQ accuracy. Such phase correction can be done either in the PLL loop or in the LO signal chain.
As it was discussed, SOI technology provides a great flexibility in terms of regulating the DC and small-signal characteristics of each CMOS transistor by regulating its body and terminal biasing. This facilities the calibration process in terms of simplicity and power efficiency, and paves the way for simpler calibration circuits.

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