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Industrial Electrical Engineering and Automation

DC-DC capacitor precharger

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Master thesis: DC-DC capacitor precharger

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Abstract

This study evaluates the possibility of charging large capacitors to high voltages within short time frames. The system is designed to charge a capacitor of 4 mF from 0 to 850 V in one second by connecting a 24 V lead acid car battery to a flyback converter. Simulation has shown that this is possible using as little as four transistors as long as proper cooling is provided. The charge sequence could then be executed multiple times per minute. Simulation results based on three different control algorithms are presented.

A prototype based on the simulations has been built and tested. The prototype managed to charge a 0.5 mF capacitor from 0 to 600 volts in one second without generating excessive heat. Noise in the circuit and lacking lab equipment hindered testing with higher power and higher voltages.

Contents

Acknowledgements

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Chapter 1

Nomenclature

1.1 Variable names

B_{max}	Saturation value for magnetic fields
l_g	Inductor core air gap
l_c	Inductor core length
L_p, L_s	Magnetising Inductance on the primary, secondary side
A_L	Inductance factor
I_{max}	Maximum current through the coupled inductor to avoid core saturation
I_{rms}	The root mean square of the current
I_{peak}	Peak current determining the switching points
(MLT)	Mean length per turn in the transformer windings
n_p, n_s	Number of winding turns on primary, secondary side
N	Turns ratio
A_c	Cross sectional area of the transformer core
W_A	Window area of the transformer core
A_W	Cross sectional area of copper conductors
A_{Fe}	Cross sectional area of the inductor core
μ_0	Magnetic permeability of vacuum
μ_c	Relative magnetic permeability of the inductor core material
R_{Vout}	Resistance value that sets the output target voltage
V_{out}	Output voltage from the flyback converter, the voltage that the capacitor is charged to
V_{target}	Target voltage of the capacitor, 850 V according to the specification
I_{sense}	Measured current through the power transistor
R_{sense}	Resistor used to measure I_{sense}
E_{max}	Maximum energy in the output capacitor according to the specification.
I_p, I_s	Primary inductor current and secondary inductor current respectively

V_p, V_s	Voltage across the inductor primary, secondary side winding
C_{out}	Capacitance of the output capacitor
EMC	Electromagnetic compability
E_{mag}	Magnetic energy in the inductor core
V_{diode}	Diode forward voltage drop
T_{sw}	Time of one switching cycle
l_g	Inductor core airgap
R_g	Magnetic reluctance in the air gap
R_c	Magnetic reluctance in the core material
$R_{reluctance}$	Total magnetic reluctance in the inductor core
ρ_r	Resistivity
c	Specific heat capacity
K_u	Inductor fill factor
τ	Time constant
ω	Angular frequency. $\omega = 2 \cdot \pi \cdot f$
q	Heat flux
$\dot{Q}$	Heat energy transfer rate
k	Thermal conductivity
R_{th}	Thermal resistivity
η	Efficiency

1.2 Abbrevations

Volvo	Volvo Trucks
CCM	Continous conduction mode
DCM	Discontinous conduction mode
FC	Flyback converter
DC-DC	Direct current to direct current
PCB	Printed circuit board
PCFF	Peak primary current fixed frequency control
PCDC	Peak primary current discontinuous control
HCMD	Hysteretic current mode control
HVB	High voltage battery
LVB	Low voltage battery
IGBT	Insulated gate bipolar transistor
MOSFET	Metal oxide semiconductor field effect transistor
IC	Integrated circuit
ASIC	Application specific integrated circuit

Chapter 2

Introduction

2.1 Background

Inside an electric vehicle two batteries are typically present, one high voltage battery (HVB) to power the driveline and high-power systems and one low voltage battery (LVB) that supplies low power systems such as control systems, lights, infotainment etc.

In order to stabilise the current from the high voltage battery, large capacitors are needed at the connection points to the power electronic loads such as the traction machine converter. These capacitors are located in the various power electronic converters in the high voltage circuit. When the vehicle is turned off the capacitors will be discharged through bleeding resistors for safety. The problem arising from this is that if the high voltage battery is connected to the capacitor when it is discharged it will sink a large inrush current to charge up the capacitor. This inrush current could damage the capacitor and the battery as well as other components and compromise the high voltage isolation in the vehicle. In order to avoid this the capacitor must be charged before the battery is connected. The current solution to this problem is to let a relay connect a resistor in series with the capacitor, blocking the inrush current. Using this method the voltage across the capacitor, V_c, will follow function 2.1.

$$V_c = V_{HVB}(1 - e^{\frac{-t}{RC}}) \tag{2.1}$$

Where V_{HVB} is the voltage of the HVB.

The exponential nature of this function means that a lot of the charging current flows in the beginning and then trickles down to zero as t approaches infinity. Since the capacitor is precharged for a finite amount of time there will always be a gap between actual voltage and target voltage when the HVB is connected and there will still be an inrush current. Eliminating this inrush current could reduce the stress on other components in the circuit.

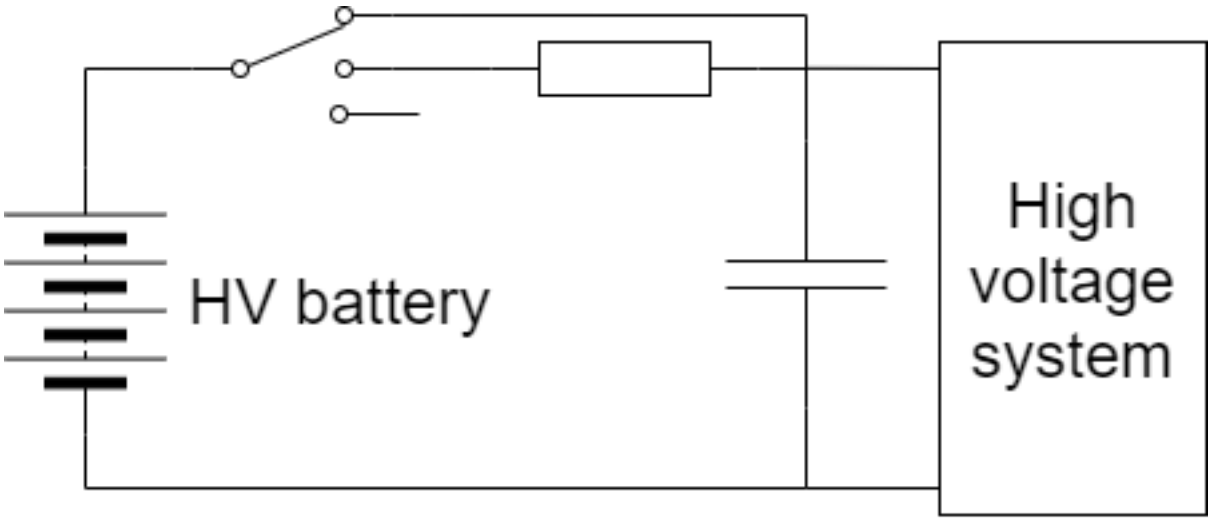


Figure 2.1: Conventional precharge circuit in an EV. The switch is set to the lowest when the EV is turned off. Before the HV battery is connected to the rest of the HV circuitry the capacitance is charged through a resistor in series.

2.2 Goal

The aim of this master thesis is to eliminate inrush current described in the previous sections. This will be done by designing a DC-DC converter which uses the LVB to precharge the capacitor to the same voltage level as the HVB. Eliminating that current will reduce wear and tear on other electronic components in the car and the cabling required to conduct that current.

Doing this requires some sort of precharge of the capacitor that must be fast, energy efficient and cost efficient. The final design should cost less than the resistor and relay prevalent in most electric vehicles today combined with the cost reduction of lowered inrush current rating on surrounding electronics.

2.3 Specification

If a product is to be placed in a vehicle then it has to meet a lot of requirements regarding performance, size and safety. No formal specification has been written by Volvo but the following bullet points defines the basic frames of the project.

- Charging the capacitor should be done within one second to ensure switf startup of the vehicle
- The system must handle a capacitor as big as 4 mF
- The target voltage must be able to vary between 600 and 850 volts
- The converter should be optimised for 24 volts and the converter must be functional with supply voltages between 18 and 36 volts

- The finished product should be the size of a tinderbox, roughly 120x70x30 mm
- The high voltage and low voltage must be galvanically isolated
- The system must be able to run in an ambient temperature as high as 60°C

Chapter 3

Theory

3.1 System Requirements

The energy that is stored in a capacitor varies with the voltage V and the capacitance C according to:

$$E = \frac{1}{2}C \cdot V^2 \tag{3.1}$$

With $C = 4\ mF$ and $V = 850\ V$ for the largest capacitance and target voltage in the specification, the energy of the fully charged capacitor is

$$E_{max} = \frac{1}{2} \cdot 0.004 \cdot 850^2 = 1445J \tag{3.2}$$

Since the capacitor is to be charged from 0 to 850 V in one second the average power output, $\overline{P_{out}}$, of the converter over the full precharging cycle is

$$\overline{P}_{out} = 1445W \tag{3.3}$$

Since the converter is to be optimised for a 24 V supply, the charge time is allowed to be longer for lower voltages. Ignoring all losses, i.e. $P_{out} = P_{in}$ gives the lowest theoretical average input current for the converter.

$$\overline{I}_{in} = \frac{P_{in}}{V_{in}} = \frac{1445}{24} = 57.8A \tag{3.4}$$

Galvanic isolation between the high voltage and the low voltage sides is needed and provided by a coupled inductor, which is essentially a transformer which is being used in a charge-discharge fashion. Measurement signals on the high voltage side can be passed to the low voltage side through opto-isolators or hall effect sensors but each such component introduces a potential source of failure and should be kept at a minimum. Similar to a transformer, a coupled inductor with a voltage drop V_p across the primary side will have a voltage drop V_s on the secondary side according to the number of winding turns on each side.

$$V_s = V_p \frac{n_s}{n_p} \tag{3.5}$$

Meanwhile, the effect on current on either side is the opposite:

$$I_s = I_p \frac{n_p}{n_s} \tag{3.6}$$

This means that the number of windings will be important for the rating of components that are connected to the transistor. The relationship between the number of turns on each side is called the turns ratio, N.

$$N = \frac{n_s}{n_p} \tag{3.7}$$

3.2 Selection of topology

Several topologies were considered at an early stage. According to [1], a half bridge series resonant converter can have a more even output current over the charge cycle. It is also found that the operating conditions for the output diode are less harsh compared to a flyback topology. Rotman and Ben-Yaakov [2] have had success with charging a capacitor with a resonant topology using input and target voltages similar to those in the specification, although with a much smaller capacitor. Ultimately, a flyback topology was selected for the capacitor precharger. The reasons for this are that there are known control circuits for this topology, that the design is familiar to the authors, and the low number of components necessary on the high voltage output side.

3.3 Functionality of the flyback converter

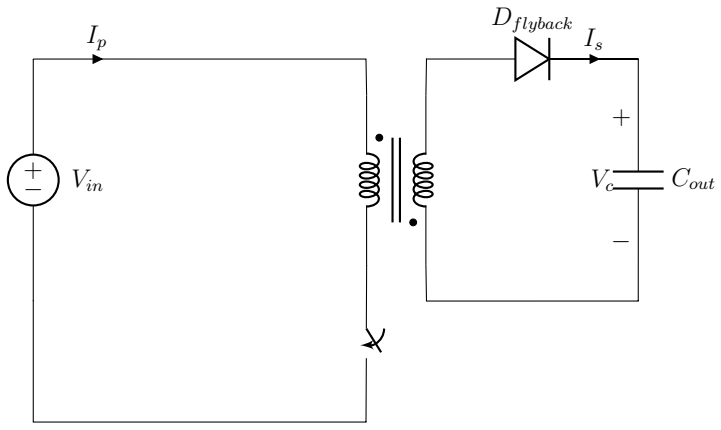


Figure 3.1: A simple flyback converter topology

3.3.1 Charging and discharging

In the following explanation all resistive and threshold voltage drops are ignored.

The flyback converter (FC) is a galvanically isolated DC-DC converter which uses power transistors and a coupled inductor. The FC has two states: primary side magnetising and secondary

side demagnetising. During primary side magnetising (or simply: "magnetising") the power transistor is in its conducting state, t_{on} and current is allowed to flow through the magnetising inductance on the primary side. At this time the current on the primary side increases linearly according to

$$\frac{dI_p}{dt} = \frac{V_{in}}{L_p} \tag{3.8}$$

which increases the strength of the magnetic field in the coupled inductor. This magnetisation continues until a peak current value, $I_{p,peak}$, is reached.

Secondary side demagnetising (hereafter: "demagnetising") begins when the power transistor is turned off (t_{off}). At this point the magnetic field present inside the coupled inductor induces a current through the winding of the secondary side. This makes the diode on the secondary side, called the flyback diode, forward biased and the current is allowed through to charge the capacitor. The initial current, right after the switching event, can be calculated according to equation 3.9 and the current will decrease according to equation 3.10.

$$I_s(0) = I_{p,peak}\frac{{n_1}^2}{n_2} \tag{3.9}$$

$$\frac{dI_s(t)}{dt} = \frac{V_{out}(t)}{L_s} \tag{3.10}$$

$$\frac{dV_{out}(t)}{dt} = \frac{I_s(t)}{C_{out}} \tag{3.11}$$

The voltage across the capacitor V_{out} will increase according to equation 3.11. If C_{out} is sufficiently large and L_s is sufficiently small, $V_{out}(t)$ can be estimated to be constant for any one switching cycle. This continues until the current has decayed to zero (at which point the flyback diode blocks the capacitor from driving a current back in the other direction) or until the power transistor on the primary side switches to its conductive state again.

The ratio between transistor on-time t_{on} and off-time t_{off} is known as the duty cycle, T_d, as defined by equation 3.12.

$$T_d = \frac{t_{on}}{t_{off}} \tag{3.12}$$

The power input to the FC depends on the primary side voltage, average current during magnetising, and the duty cycle according to equation 3.13.

$$P = V_{in} \cdot T_d \cdot (\frac{\Delta I_p}{2}) \tag{3.13}$$

The FC can operate in two distinct modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In continuous conduction mode the FC switches from magnetising back to demagnetising before the current on the secondary has decayed to zero as seen in figure 3.2. In discontinuous conduction mode the secondary side current has completely decayed before magnetising is resumed, and the discharging time t_{off} has two parts, the time it takes to demagnetise t_{demag} during which the flyback diode is conducting current from the secondary winding, and the dead time t_{dead} during which the current is zero. These timestamps are illustrated in figure 3.3.

During t_{dead} neither the primary nor the secondary side conducts any current and thus the transmitted power during this time is zero.

The total time T_{sw} of one switching cycle is set by t_{on} and t_{off} which also sets the switching frequency of the power transformer.

$$T_{sw} = t_{on} + t_{off} \implies f = \frac{1}{T_{sw}} \tag{3.14}$$

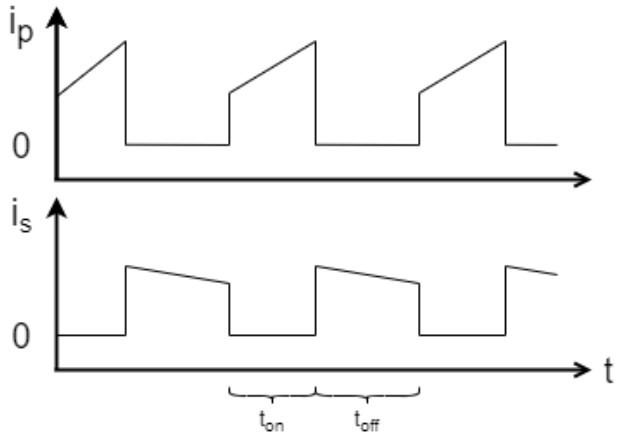


Figure 3.2: Currents in continuous conduction mode of operation

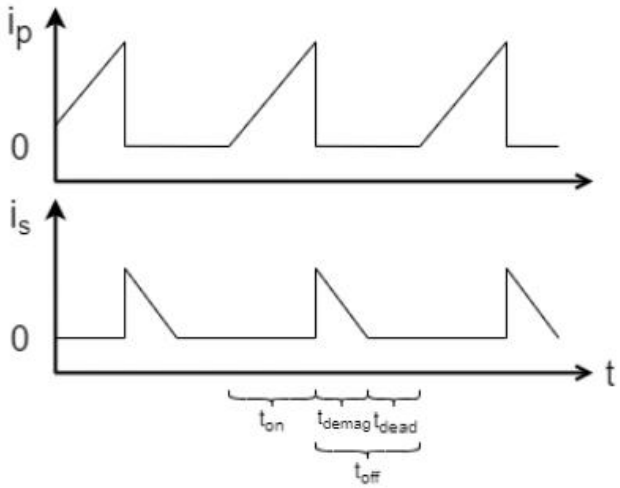


Figure 3.3: Currents in discontinuous conduction mode of operation

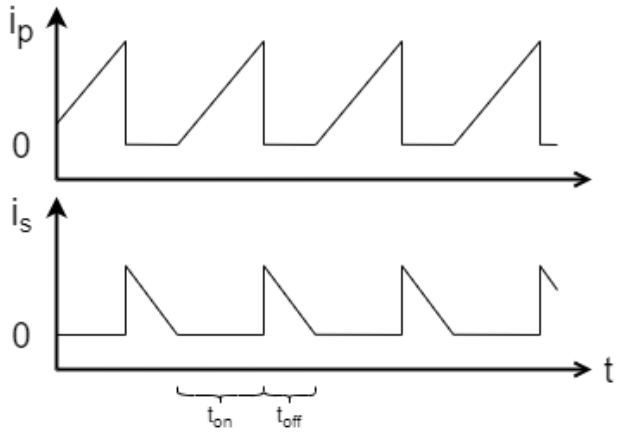


Figure 3.4: Currents at the border of continuous and discontinuous conducton mode of operation

3.3.2 Energy transfer

Energy is transferred from the primary side to the secondary side via a shared magnetic field. This field is carried by a core material that keeps the magnetic flux localised to the coupled inductor. The field is induced by drawing current through the primary winding. Normally this would induce a current in the secondary winding since it is also inside the magnetic field. In this case however, the flyback diode blocks the secondary current. Once the induced field is strong enough the current path through the primary circuit is closed, forcing the field to collapse into the secondary winding. This makes the flyback diode forward biased and the energy stored in the field is passed to the secondary side of the coupled inductor.

Since the coupling is purely magnetic the galvanic isolation is maintained through the charging sequence. This is highly desirable since power flows from the LVB to the HVB, a short circuit between these systems is potentially catastrophic.

The energy E_{mag} which is stored in the magnetic field of the coupled inductor is proportional to the current i which flows through it according to:

$$E_{mag} = \frac{1}{2} L_p \cdot i^2 \tag{3.15}$$

Where L_p is the magnetising inductance of the primary winding, the magnetising inductance of the secondary winding is denoted L_s. Since the magnetic coupling is not perfect the inductance can broken down to L_{mag} and L_{leak}. In this regard L_{mag} is useful inductance that is coupled with the other inductor whereas L_{leak} is a parasitic inductance that remains in the winding.

The magnetising inductance is not the same on both sides, it depends on the number of winding turns according to:

$$L_p = L_s \cdot \left(\frac{n_p}{n_s}\right)^2 \tag{3.16}$$

where n_p is the number of turns on the primary winding and n_s is the number of turns on the secondary winding. This means that if a certain magnetic energy corresponds to a current I_p on the primary side, it will induce a current $I_s = I_p\left(\frac{n_p}{n_s}\right)$ on the secondary side.

3.3.3 Snubber circuits

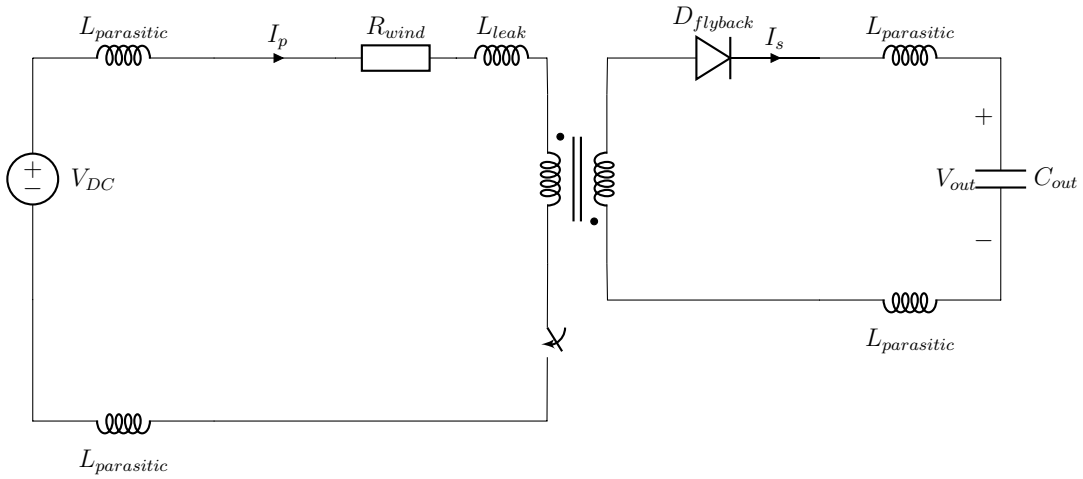


Figure 3.5: Flyback circuit with parasitic inductances

In addition to the leakage inductance there will be stray inductance present in the circuit. The fast switching of the FC is problematic because these unwanted inductances will continue to drive current on their respective sides even after switching. This could create voltage spikes that would easily break the switching components and must thus be handled in some way. RCD snubber circuits, see figure 3.6, provide an alternative path where the current is allowed to flow into a capacitor which is then discharged through a resistor. A diode prevents the current from oscillating back to the stray inductance. The snubber must be designed in such a way that the current from the parasitic inductances is absorbed into the snubber capacitors without exceeding the rated voltage of the snubber capacitor. Using equation 3.15 with the leakage and parasitic inductance to find the energy, the voltage across the snubber capacitor after one switch can be found using equation 3.1. It must be ensured that the voltage rating of the capacitor is higher than this value.

$$V_{snubbercap} = I_{peak}\sqrt{\frac{L_{leak} + L_{parasitic}}{C_{snubber}}} \tag{3.17}$$

The snubber capacitor then starts to discharge through the resistor, and the voltage follows equation 3.18. The size of the resistor and capacitor sets the discharge time of the snubber. The time constant τ is the time it takes to discharge the capacitor voltage to $\frac{1}{e}$ of the initial value:

$$V(t) = V_0 \cdot e^{-t/\tau} \tag{3.18}$$

$$\tau = R \cdot C \tag{3.19}$$

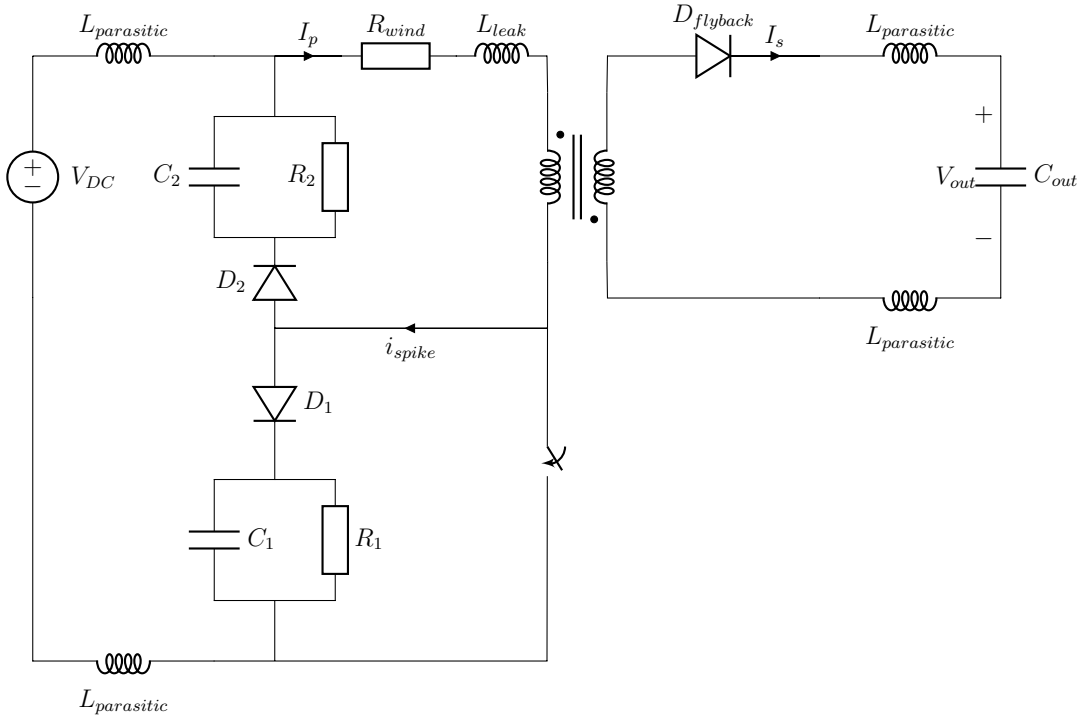


Figure 3.6: Flyback circuit with primary side snubbers and parasitic inductances

It is important to note that when the snubber diode is forward biased, the snubber voltage will be visible on the node between the coupled inductor and the switch. Since this is the node where the reflected voltage is measured as well, this can cause problems if the reflected voltage is used to calculate the output voltage. Just like the flyback diode the snubber diode is forward biased for a shorter time if the snubber capacitor voltage is higher as the discharging of the leakage inductance also follows equation 3.20. That makes it difficult to sample the reflected voltage unless the snubber capacitor is fully discharged between switching cycles. The secondary current does not reach its peak value until the primary leakage inductance is fully discharged. The models include up to three snubber circuits, two on the primary side and one on the secondary side. One snubber on the primary side sits across the winding terminals and is there to absorb the voltage spike from the leakage inductance and the parasitic inductance on the positive connection. The second snubber is connected across the power transistors and protects them from the voltage spike caused by the parasitic inductance on the negative connection. The snubber on the secondary side is connected across the flyback diode and protects it from voltage spikes caused by switching to charging state before the secondary side current has decayed completely. See section 4.1 for snubber selection in the simulation and section 5.1.4.

3.4 Control Algorithms

Control of a capacitor charger is not straightforward. The reason is that the output voltage level increases throughout the charging. Recall that the current through an inductor changes

according to:

$$\frac{di}{dt} = \frac{V}{L} \tag{3.20}$$

Where V is the voltage across the inductor. For the flyback secondary side, V is the capacitor voltage plus the forward voltage of the flyback diode, V_{diode}:

$$\frac{di}{dt} = \frac{V_{out} + V_{diode}}{L_s} \tag{3.21}$$

Thus, in the beginning of the charging when $V_{out} = 0$ the only voltage across the inductor is the forward voltage of the flyback diode and the current decays slowly, which means that the capacitor also charges slowly since the output energy is low. The energy which is stored in the magnetic field can be found by combining equation 3.15 and 3.16. When the capacitor voltage is near the target voltage, equation 3.21 is dominated by the capacitor voltage and the current derivative is very steep, so the secondary side is demagnetised quickly.

On the primary side the voltage (ignoring voltages across parasitic resistances and the power transistor) across the inductor winding is constant. V in equation 3.20 is the input voltage. The result is that the power during t_{on} is constant throughout the charging of the capacitor, while the power during t_{off} increases with the capacitor voltage.

If the FC is run at a constant switching frequency f_{sw} and a constant duty cycle T_d, one can choose between two scenarios. The first is that the frequency and duty cycle is chosen such that the secondary side has time to completely decay during the first switch cycle. This will result in dead-time for the remaining switch periods as the current decay time gets gradually shorted when the output voltage increases. Since the target voltage is much larger than the voltage resulting from a single magnetization cycle, the FC will be in t_{off}, see figure 3.3, most of the time. The second scenario is that f_{sw} and T_d are selected to allow the inductor to completely demagnetize at some later switch cycle when the output voltage has increased and the demagnetization is faster. One may be tempted to select this to be the final switch cycle where $V_{out} \approx V_{target}$. Then the FC will never have any dead-time during the charge cycle. However, since t_{on} is constant and the secondary side is not allowed to completely demagnetize the core during the first part of the charge cycle, it will be more and more magnetized and will eventually saturate and cause excessive currents on the primary side. To avoid this, the core must be allowed to discharge as much energy as it is charged with for every switch cycle during the charging process.

To avoid a situation where the magnetic field saturates the core, the current in the inductor can be measured. This can be done by measuring the current on the primary side and stopping the current when it reaches a peak value, I_{pk}. Another way is to measure the current on the secondary side and ensure that it decays enough to avoid saturation of the core. t_{on} could then be set to a constant value low enough to ensure that the core is never saturated. The disadvantage of this method is that it requires measurement of the secondary side current to be

transferred to the primary side without compromising the galvanic isolation between primary and secondary. It is more convenient to measure the primary side current and turn the power transistor off before the current becomes too large.

3.4.1 Primary peak current control with fixed frequency (PCFF)

The first control algorithm for the FC that was investigated is the primary peak current control with constant switching frequency. The algorithm begins by turning on the power transistors and allowing the current through the inductor to increase until a peak value, I_{max}, is reached. At I_{max} the power transistor is switched off and the primary inductor can be demagnetised through the secondary side. After a fixed amount of time the power transistors are switched on and the magnetic field is induced again. Doing this at a fixed frequency can result in the FC starting the charging sequence in CCM and ending it in DCM. This is because the demagnetisation is faster when the secondary voltage is higher. This phenomenon can be observed in figures 3.7a and 3.7b where the capacitor voltage is at 10 and 600 volts respectively.

Since demagnetisation takes less and less time as the output voltage increases, the duty cycle increases as the capacitor becomes more and more charged. This means that the power of the FC also increases until DCM is reached at which point the duty cycle reaches it's maximum and plateaus. One can choose to design the FC so that DCM is reached at the same time as the target voltage. The magnetising inductance of the secondary winding is called L_s and it's value is $L_s = L_p \cdot N^2$ where N is the turns ratio of the coupled inductor. Since $V_{cap} = L_s \frac{di}{dt}$ we can write:

$$\frac{di}{dt} = \frac{V_{target}}{L_s} = \frac{V_{target}}{L_p\left(\frac{n_s}{n_p}\right)^2} \tag{3.22}$$

Assuming that the switching frequency is high the following approximation for the differential can be made:

$$\frac{di}{dt} = \frac{\Delta i}{\Delta t} \tag{3.23}$$

where the delta values can be known. Approximating that the voltage across the capacitor is constant for the last charging cycle, $U_{final} = 850\ V$, the following will hold for the primary side: $\Delta i = I_{peak}$ and $\Delta t = T_d \cdot T_{sw}$.

For the secondary side the following equations apply: $\Delta i = \frac{I_{peak}}{N}$, $L_s = L_p \cdot N^2$ and $\Delta t = (1 - T_d) \cdot T_{sw}$

The inductance equation can now be rearranged to

$$L\frac{\Delta i}{\Delta t} = V \iff \Delta t = \frac{L \cdot \Delta i}{V} \tag{3.24}$$

The charging and discharging times can now be calculated according to

$$\begin{cases} t_{on} = \frac{I_{peak} \cdot L_p}{U_{in}} \\ t_{off} = \frac{I_{peak} \frac{1}{N} \cdot L_p \cdot N^2}{U_{final}} = \frac{I_{max} \cdot L_p \cdot N}{U_{final}} \end{cases}$$

This means that for the final switching cycle the duty cycle, T_d, is

$$T_d = \frac{t_{on}}{t_{on} + t_{off}} = \frac{\frac{I_{peak} \cdot L_p}{U_{in}}}{\frac{I_{p,pk} \cdot L_p}{U_{in}} + \frac{I_{peak} \cdot L_p \cdot N}{U_{final}}} \tag{3.25}$$

With $N = 10, U_{in} = 24\ V$, $U_{final} = 850\ V$, the duty cycle becomes

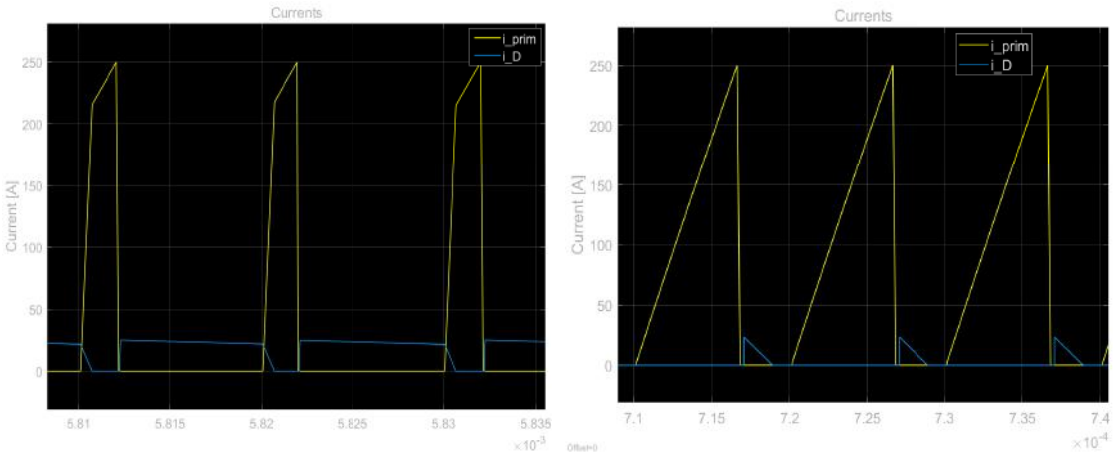
$$T_d = \frac{\frac{1}{24}}{\frac{1}{24} + \frac{10}{850}} \approx 0.78 \tag{3.26}$$

In other words the inductance is selected such that the current can reach I_{max} in 80 % of one charging cycle. This means that the converter enters DCM in the final cycle and no cycle has any dead time. This gives the following equation for the inductance:

$$L = U_{in} \cdot \frac{t_{on}}{\Delta i} = U_{in} \cdot \frac{T_d \cdot T_{sw}}{I_{peak}} = U_{in} \cdot \frac{T_d}{f \cdot I_{peak}} \tag{3.27}$$

It then follows that the frequency for a given inductance becomes:

$$\frac{1}{f} = T_{sw} = t_{on} + t_{off} = \frac{L_p \cdot I_{peak}}{U_{in}} + \frac{L_p \cdot I_{peak} \cdot \frac{N_2}{N_1}}{U_{final}} = I_{peak} \cdot L_p \cdot \frac{U_{in} + U_{final} \frac{N_1}{N_2}}{U_{in} U_{final} \frac{N_1}{N_2}} \tag{3.28}$$



(a) Early stage of the charging process. Capacitor voltage at around 10 volts. FC operates in CCM with f = 100kHz.

(b) late stage of the charging process. Capacitor voltage at around 600 volts. FC operates in DCM with f = 100kHz.

Figure 3.7: Peak primary current control with constant frequency

This is a simple but inefficient control algorithm because of the shift in conduction mode. As soon as the current reaches zero the power transistors should be switched on again in order to minimise t_{dead}. The dead time caused by this control algorithm can be observed in figure 3.7b. The early stage of the charge cycle is also inefficient since very little of the energy is transferred to the capacitor before primary side magnetising resumes. This can result in unnecessary turnoff losses without much energy having been transferred.

3.4.2 Peak primary current with discontinuous current mode detection (PCDC)

This algorithm is similar to the one above but instead of switching on the primary side power transistors at fixed time intervals it remains off until the current on the secondary side has ceased. This can be detected by measuring the reflected voltage and once it reaches zero the power transistors are turned on. Since the primary side current starts at 0 A and increases linearly during t_{on} the power of the converter, ignoring any losses and switching times, depends on the peak current and the duty cycle according to:

$$P(t) = \frac{1}{2} I_{peak} \cdot V_{in} \cdot T_d \tag{3.29}$$

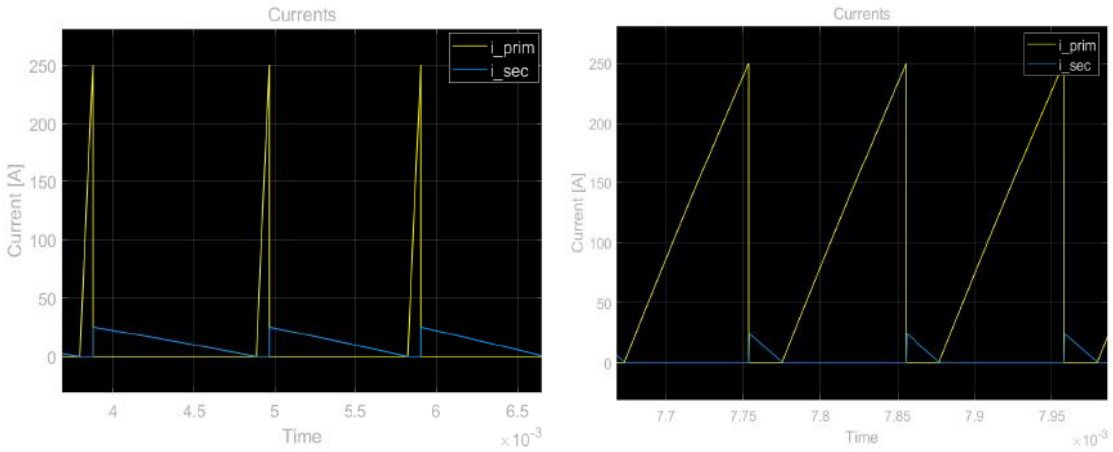
Figure 3.8 shows that the duty cycle increases as the output capacitor becomes more and more charged. The peak current can be roughly approximated by using the average power acquired from equation 3.3

$$I_{peak} = \frac{2 \cdot \overline{P}}{V_{in} \cdot T_d} \tag{3.30}$$

This algorithm guarantees that the FC is always in DCM and without dead time as seen in figures 3.8a and 3.8b. These graphs can be compared to figure 3.7a and 3.7b, in the beginning of the charging sequence the power is still properly transferred and at the end of the sequence there is no dead time. Since the peak current on the primary side is constant and always increases from zero, t_{on} is constant throughout the sequence. However, t_{off} is reduced significantly as V_{out} increases, thus the switching frequency of the power transistors increase during the sequence. If the FC is always in DCM then the FC never cuts an inductive current on the secondary side which eliminates the need for a snubber on the secondary side.

3.4.3 Hysteretic current mode control (HCMC)

According to Nathan O. Sokal and Richard Redl [2], a more efficient FC can be constructed by staying in CCM. The optimal control algorithm would be to let short current pulses with flat tops pass through the FC. This is due to the fact that the power dissipation is proportional to the RMS current and the component current rating depends on the peak current. The charge



(a) Early stage of the charging process. Capacitor voltage at around 10 volts. Switching frequency just over 1 kHz.

(b) late stage of the charging process. Capacitor voltage at around 750 volts. Switching frequency approximately 10 kHz.

Figure 3.8: Peak primary current control with discontinuous conduction mode

delivered to the capacitor on the other hand is proportional to the average current. The highest possible average current, given RMS and peak current, is achieved by sending a square current waveform. However, the current will have to vary according to $\frac{di}{dt} = \frac{V}{L}$. By keeping dt low, di can be kept low as well, but this comes at the price of increased switching frequency and thus switching losses. A compromise is sought where di is kept low and dt is not too small. Meanwhile, the value of V will increase on the secondary side as the capacitor voltage increases. The solution is to specify a value for di that the system must ensure for every switch. The value of di will vary on the primary side and the secondary side depending on the turns ratio, but the deviation from the peak value in percent will be the same for both sides. We call this deviation a:

$$a = 1 - \frac{i_{peak} - i_{min}}{i_{peak}} \tag{3.31}$$

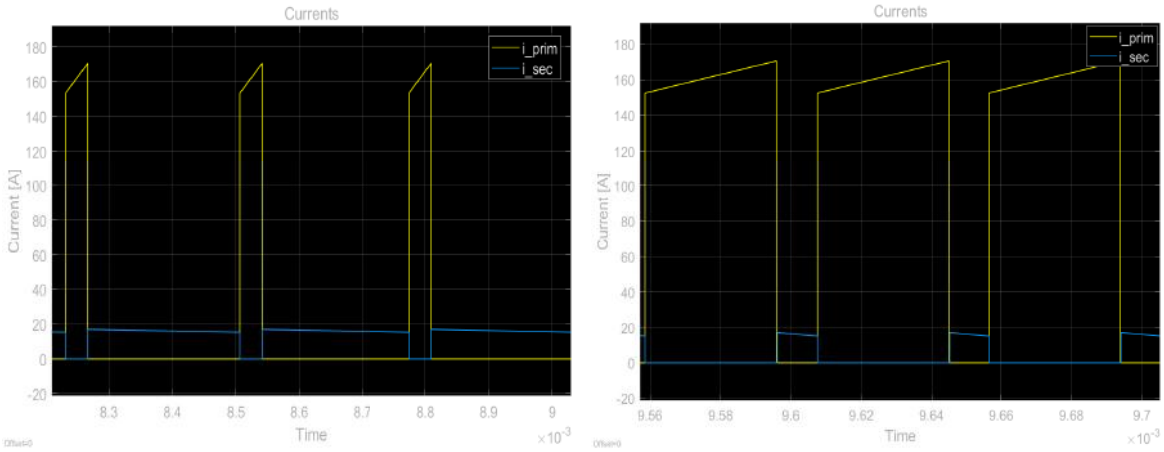
$$i_{min} = a \cdot i_{peak} \tag{3.32}$$

The FC was simulated with a varying between 0.2 and 0.8 and the results can be seen in 4.2

This approach requires some way of measuring the current on the secondary side. This can be done algebraically by looking at the reflected voltage but would require accurate and continuous measurement as well as exact knowledge of the turns ratio, magnetising inductance, voltage drops etc. Some practical approaches are proposed in [2]: measuring the current on both sides of the transformer; measuring the current on either side and using knowledge of the magnetising inductance or one could measure the voltage levels to calculate how long the current should be allowed to flow on the opposite side, i.e. feed-forward control. This requires voltage measurement on the output capacitor in case t_{off} is to be calculated.

The first approach might jeopardise the galvanic isolation since it requires measurement on the secondary side. The second approach demand accurate knowledge about system parameters

that might be difficult to attain. The authors of [2] advice against the third approach since using feed-forward control for both t_{on} and t_{off} may result in I_{peak} either growing or fading uncontrollably if there are any inaccuracies in the model.



(a) Early stage of the charging process. Capacitor voltage at around 10 volts. Switching frequency just over 1 kHz.

(b) late stage of the charging process. Capacitor voltage at around 700 volts. Switching frequency approximately 10 kHz.

Figure 3.9: Peak primary current with secondary side tolerance band

3.5 Coupled inductor design

When designing a coupled inductor there are many factors that need to be considered and there are many design methods. In this project the area product method is used to identify suitable cores.

The area product is achieved by putting five equations together. The first one, equation 3.33, describes the relationship between maximum current, I_{max}, winding turns, n, magnetic saturation, B_{max}, air gap, l_g, and magnetic permeability, μ_0. The geometrical variables are illustrated in figure 3.10.

$$n \cdot I_{max} = B_{max} \frac{l_g}{\mu_0} \tag{3.33}$$

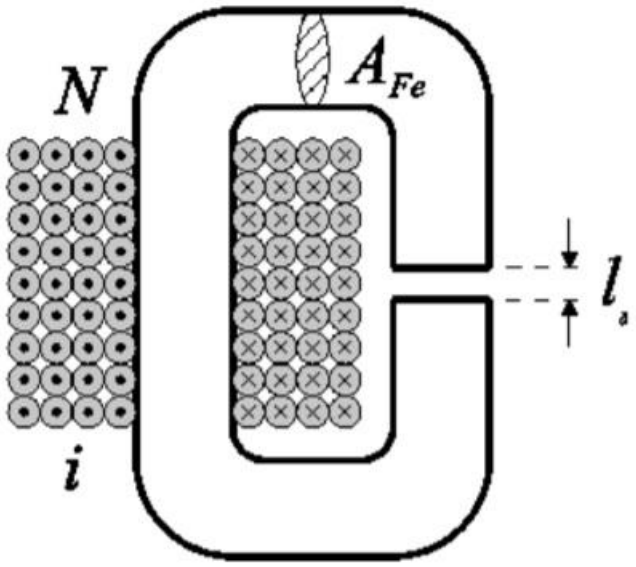


Figure 3.10: Illustration of an inductor core window area [3]

The current that passes through an inductor induces a magnetic field that is carried through the core material and the air gap. There is, however, a limit to how great the magnetic flux density can become in a given material. This puts an upper boundary on how strong the magnetic field can become, i.e. how big B_{max} can be. With this in mind equation 3.10 is rearranged to the difference 3.34, it is then necessary to make sure that the core material can satisfy this condition.

$$B_{max} \geq \frac{nI_{max}\mu_0}{l_g} \tag{3.34}$$

The inductance of the coupled inductor is different when seen from the primary and secondary side. If only one side is considered then the inductance only depend on the number of winding turns and the reluctance of the core material and the air gap. This is shown by equation 3.35 where the reluctance is broken down to air reluctance and core reluctance. Due to difficulties in manufacturing where it's hard to guarantee precise gaps and permeability, most manufactures specify an inductance factor, A_L instead of air gaps and reluctances.

$$L = \frac{n^2}{R_{reluctance}} = \frac{n^2}{R_g + R_c} = \frac{n^2}{\frac{l_g}{\mu_0 A_{Fe}} + \frac{l_c}{\mu_c \mu_0 A_{Fe}}} = A_L n^2 \tag{3.35}$$

Notice that the reluctance and thus the inductance factor is set by the cross sectional area of the inductor core and that a larger core area gives a lower reluctance and a higher inductance factor. By finding the number of turns from equation 3.34 and plugging it into equation 3.35 it can bee seen that a higher current requires a lower reluctance and thus a larger core size for the same air gap.

$$n = \sqrt{L \cdot R_{reluctance}} \iff B_{max} \geq \sqrt{L \cdot R_{reluctance}} \cdot \frac{I_{max}\mu_0}{l_g} \tag{3.36}$$

The LT3750 controller that is used for experimental implementation and discussed in section 5.1, puts a demand on the system inductance in order to guarantee reliable performance, this demand is expressed in micro Henrys according to inequality 3.37.

$$L_p \geq \frac{V_{target}}{n \cdot I_{peak}} 10^{-6} \tag{3.37}$$

If the cross sectional area of the copper used in the windings is too small then too much energy will be dissipated in the copper. The losses are directly proportional to the resistance as calculated by equation 3.38. Where ρ_r is the resistivity of the material, n is the number of turns and (MLT) is the mean length per turn.

$$R = \rho_r \frac{n(MLT)}{A_w} \tag{3.38}$$

With a known resistance R, geometry and heat capacity c, and operating time t, the temperature rise can be calculated according to equation 3.40. This calculation returns the required cross sectional area of the conductor given the current and acceptable temperature rise. The heat energy in the winding is:

$$E = c \cdot m\Delta T = c \cdot n(MLT)A_w \cdot \rho_r \Delta T = R \cdot I_{RMS}^2 \cdot t = \rho_r \frac{n(MLT)}{A_w} I_{RMS}^2 \cdot t \tag{3.39}$$

Rearranging equation 3.39 gives the minimum winding area:

$$A_w = \sqrt{\frac{\rho_r \cdot I_{RMS}^2 \cdot t}{c \cdot \Delta T \cdot \rho_m}} \tag{3.40}$$

The inductor core selected to pass the energy must be able to accommodate the windings, they have to fit inside the core window W_A. Since the windings are round and isolated the entire window area can't be filled with copper. To adjust for this a fill factor K_u is used in inequality 3.41.

$$K_u \cdot W_A \geq A_W n \tag{3.41}$$

Putting equations 3.33, 3.35 ,3.38, 3.40 and 3.41 together will result in the inequality 3.42.

$$A_{cA}^2 \geq \frac{A_l^2 \cdot n^3 \cdot I_{max}^2 \sqrt{\frac{\rho_r I_{RMS}^2}{c\Delta T \cdot \rho_m}}}{B_{max}^2 \cdot K_u} \tag{3.42}$$

Inequality 3.42 must hold for the selected core. Most of the values are specified in the datasheets of the cores or derived from simultaions as discussed above. The K_u value however, is estimated to be 0.4. This accounts for the thickness of the isolation and the fact that the transformer is wound by hand, meaning that some gaps between the bobbin and the coil is to be expected. B_{max} is typically specified for each individual core but manufacturers are prone to exaggerating their performance, thus B_{max} has been set to 0.3 T in calculations which could be reasonably expected from most ferrite cores.

One crucial aspect of the inductor design is the turns ratio on the windings. In a transformer the turns ratio is selected in order to produce the correct voltage level on the output. In the design of a FC the reflected voltages are of greater concern since they pose a greater strain on the components. As such it is the component that dictate what turns ratio can be used, a more thorough discussion of the turns ratio can be found in section 5.1.

The current will appear as a saw-tooth wave with a maximum duty cylce of approximately 80 %, see section 4.2. The I_{RMS} value of such a current is calculated according to equation 3.43.

$$I_{RMS} = \sqrt{\frac{1}{T}\int_0^T I_{RMS}^2 dt} = \sqrt{\frac{1}{T}\frac{I_{max}^2}{(0.8T)^2}\int_0^T t^2 dt} = \sqrt{\frac{I_{max}^2 0.8}{3}} \tag{3.43}$$

With I_{max} equal to 250 A as disscussed in section 4.2 the I_{RMS} value becomes 129 A.

3.5.1 Inductor measurements

The inductance of an inductor can be identified in multiple ways. In this project two methods are used, measuring the step response when applying a voltage step and measuring the frequency response when applying a voltage sine wave.

When applying the voltage step the current through the inductor will increase asymptotically. The exponential nature of the curve will make the voltage follow the function in 3.44. Identifying the time constant for this curve will yield the inductance according to 3.45. In this case the desired inductance will give time constants in the order of magnitude of picoseconds. No equipment was available that could measure such a short duration accurately.

$$V_L = V_o - V_o e^{-\frac{L}{R}t} \tag{3.44}$$

$$\tau = \frac{L}{R} \iff L = R \cdot \tau \tag{3.45}$$

The frequency response is measured by applying sinusoidal voltage across the inductor. The impedance of the inductor depends on the frequency of the sine wave according to equation 3.46. The current will also have a 90°phase lead compared to the voltage.

$$Z_L = j\omega L \tag{3.46}$$

The magnitude of the inductance L can be determined by connecting a resistor of known resistance in series with the inductor. the angular frequency and the frequency of the sine wave can then be adjusted until the voltage across both components has the same magnitude, thus $Z_L = R$. Equation 3.47 is then used to find the inductance.

$$L = \frac{Z_L}{j\omega} = \frac{R}{j2\pi f} \tag{3.47}$$

This method is used to find the inductance of the coupled inductors that were wound by hand in this project.

The turns ratio of the transformer can be verified by rearranging equation 3.5 into equation 3.48 by applying a sinusoidal waveform across the secondary winding and observing the voltage across the primary.

$$\frac{n_s}{n_p} = \frac{V_s}{V_p} \tag{3.48}$$

3.6 Losses

All conduction of electricity dissipates some amount of heat. These losses must be identified and handled with proper cooling or the circuit will break. Some components such as power transistors and power resistor are prepared with a cooling tab and can be fastened to a heat sink which absorbs the heat energy from the component. For continuous operation, the heat sink needs to be cooled either passively or actively e.g. with a fan. Since the FC is designed for intermittent operation, the heat sink does not require any active cooling but needs to have enough thermal mass to absorb the losses without heating up too much.

The electrical simulations as discussed in section 4.2 yield an estimate off how much energy the system will dissipate as heat which is useful when designing the size and placement of heat sinks. PLECS allows for building thermal models in the form of thermal networks, which resemble electrical circuits. In a thermal network heat flux is modelled as current, thermal mass as capacitance and thermal paths as resistance. The following equations shows the analogy between heat transfer and Ohms law that thermal networks build on.

3.7 Heat transfer

The heat flux q is proportional to the temperature difference ΔT, the thermal conductivity k, and the length of travel L according to equation 3.49.

$$q = -k\frac{\Delta T}{L} \tag{3.49}$$

The heat energy transferred through a medium, $\dot{Q}$ is also proportional to the surface area A that is in contact according to equation 3.50.

$$\dot{Q} = A \cdot q = -A \cdot k\frac{\Delta T}{L} \tag{3.50}$$

solving for ΔT gives the first part of equation 3.51, a heat transfer equation analogous to Ohm's law.

$$\Delta T = \frac{L}{A \cdot k}\dot{Q} = R_{th}\dot{Q} \iff U = R \cdot I \tag{3.51}$$

From this analogy thermal networks can be constructed. The model can be improved by adding thermal capacitance m_t, calculated from specific heat capacity and mass according to equation 3.52.

$$m_t = c \cdot m \tag{3.52}$$

Thermal networks can have two structures, Foster-networks or Cauer-networks. The main difference between the two is how the thermal impedances are connected, in Cauer networks all components are connected in series whereas Foster networks connect them in parallel. In these models Cauer-networks have been used, in which all thermal impedances are connected in series. In figure 4.1 the thermal model of the system can be seen.

3.8 Method

The theory as explained above shows that a system that meets the specification can be built. This is verified in two ways: the first method is simulation as described in chapter 4, where all the control algorithms are modelled and simulated. With those results the best algorithm can be selected for implementation.

The second method is to actually build the system as detailed in chapter 5. Here the true capabilities of the system will become apparent and the limitations of reality will impose themselves on it.

Chapter 4

Simulation

4.1 Simulation method

In order to better understand the operation of the flyback converter, simulations with each control algorithm have been preformed. The following parameters were examined:

- How the losses vary with the switching frequency
- How the losses vary with component parameters and where those losses occur
- Whether the losses vary over the charge sequence
- Which components have a greater impact on the losses and operation. (sensitivity analysis)
- How the power output varies over the charge sequence
- How the efficiency and power vary depending on the settings of the controller
- For how long the FC is idle
- Ensuring that the rating of the components is not exceeded during operation. This includes both thermal, voltage and current ratings.

A flyback topology as shown in figure 4.1 was constructed in PLECS, a plugin for Matlab/Simulink. The PLECS model contains two networks: one electrical network (including the magnetic coupling of the inductor) and one thermal network. Every iteration simulates one second of operation during which the output capacitor is charged from 0 V. If the target voltage of 850 V is reached before the second has passed the circuit turns off and the capacitor is not charged any further. The model includes the primary side magnetic inductance, leakage inductance and winding resistance. Voltages, currents, losses, temperatures and states of switching devices can be sampled and saved at each integration step of the numerical analysis

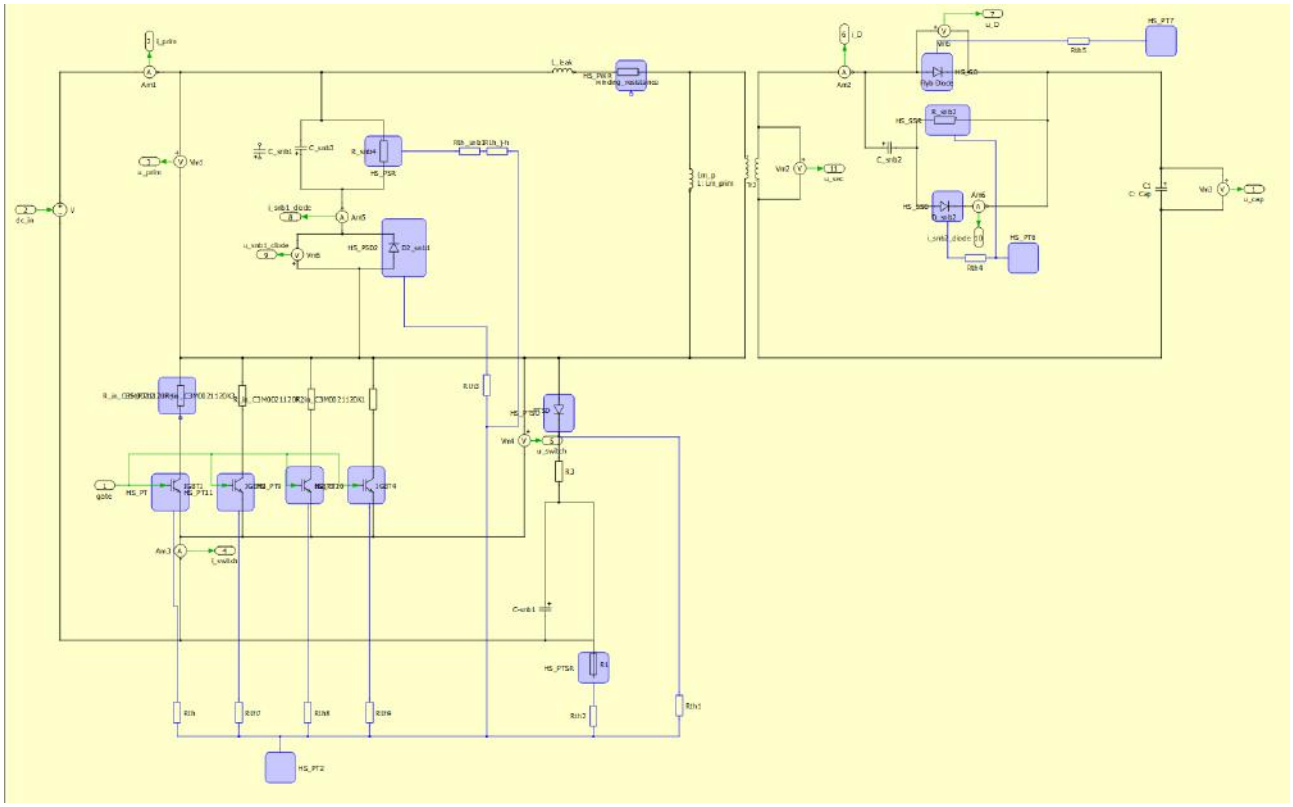


Figure 4.1: Electrical and thermal image from the simulation environment. The power transistors snubber diodes and snubber resistors on the primary side are connected to a common heat sink.

but due to the uneven step sizes and the high number of steps they were instead sampled and saved with 1000 Hz frequency.

The conduction losses in the switches are part of the thermal model but do not show up in the electrical model. For this reason a small resistor was added. The size of the resistor was selected by iterating simulations until the thermal and electric losses of the transistor were within 10 % of each other.

Simulations were carried out with the same components, parasitic resistances, input voltage and output target voltage for the three control algorithms. The settings of the algorithms were swept over in order to understand how this would affect some key parameters, namely:

- Input power
- Output power
- Output capacitor voltage
- Duty cycle
- Switching frequency
- Losses in each component (switching and conductive)

- Temperatures of transistors and diodes
- Temperatures in snubber resistors

The results can be seen in section 4.2.

Three similar models were used for the three control algorithms. For each algorithm, the following key variables were swept. For each iteration, six to ten values were used in the sweep.

- Peak primary current control with constant frequency (PCFF)
  - Frequency
  - Primary side inductance
  - Peak current

  For the frequency sweep the inductance was changed for each iteration according to equation 3.27. The smallest inductance was 640 nH and the largest was 3.84 μH. The peak current was calculated using the current from equation 3.4, an average duty cycle T_d of 0.58, an efficiency η of 80% and using the fact that the primary current is a saw tooth wave, i.e. the peak value is twice the average value.

  For the inductance sweep a switching frequency of 80 kHz and a peak current I_{peak} of 250 A were selected. Notice that the frequency in this case was not changed according to equation 3.28. The frequency corresponds to the third value in the sweep, 840 nH, found with equation 3.28.

  For the current sweep the 80 kHz frequency was used again together with the 840 nH inductance.

$$I_{peak} = 2 \cdot \frac{\overline{I}_{in}}{T_d \cdot \eta} \approx 250 \tag{4.1}$$

  The value of the inductance was then calculated according to equation 3.27 using the duty cycle of the last switches which was of 80 %. The calculated inductance was $L_{calc} = 842nH$. The circuit was simulated with six inductance values: 0.4, 0,6, 1, 1.5, 2, and 4 times the size of L_{calc} For the current sweep equation 3.27 was used with $T_d = 0.8$ and $I_{peak} = 250A$ which gave a primary winding inductance of 842 nH. The switching frequency was set to 80 kHz. Six different currents from 100 to 350 A in steps of 50 A were used in the sweep.

  For the frequency sweep six equidistant frequencies from 20 kHz to 120 kHz were used. Equation 3.27 was used to calculate a new inductance for each frequency. $I_{peak} = 250A$ and $T_d = 0.8$ was used in the calculation and simulation.

- Peak primary current with discontinuous conduction mode (PCDC)

  - Primary side inductance
  - Peak current
  - Turns ratio

  For the primary side inductance sweep, four inductances were selected because they are the theoretical values of the primary side magnetising inductance from the selected cores according to the data sheets[4][5][6], see Table 5.1. The two larger inductance values show how the performance is affected if a larger core would be used instead.

  For the peak current sweep an inductance of 520 nH was used.

  The turns ratio affects the selection of components and a turns ratio of around 1:10 was regarded as realistic, see section 5.1.3 for further discussion on turns ratio. Primary side inductance of 500 nH was used for the sweep.

- Hysteretic current mode control (HCMC)
  - Size of the tolerance
  - Frequency/inductance
  - Peak current

  The size of the tolerance band makes the difference between this algorithm and PCDC. Primary side inductance of 450 nH was used together with a peak primary side current of 170 A.

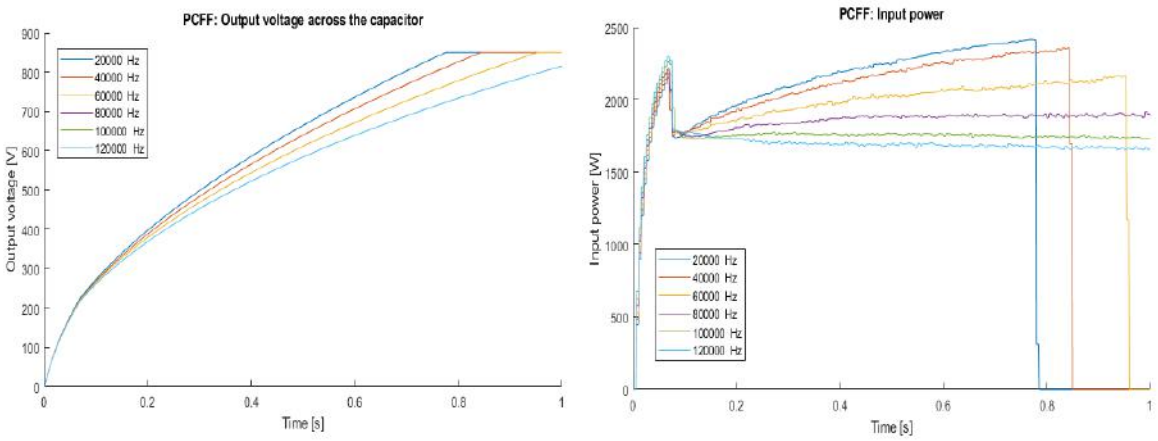
  For the inductance sweep more values were swept than for the other algorithms. This is because the smaller peak current allows for a larger inductance for the same core before it becomes saturated so a larger range of inductances can be used with the same cores.

  For the peak current sweep an inductance of 450 nH was used.

4.2 Simulation results

4.2.1 PCFF

Figure 4.2 shows how the output voltage and input power varies over the charging cycle.



(a) Capacitor voltage over time

(b) Input power over time

Figure 4.2: Sweep over multiple frequencies

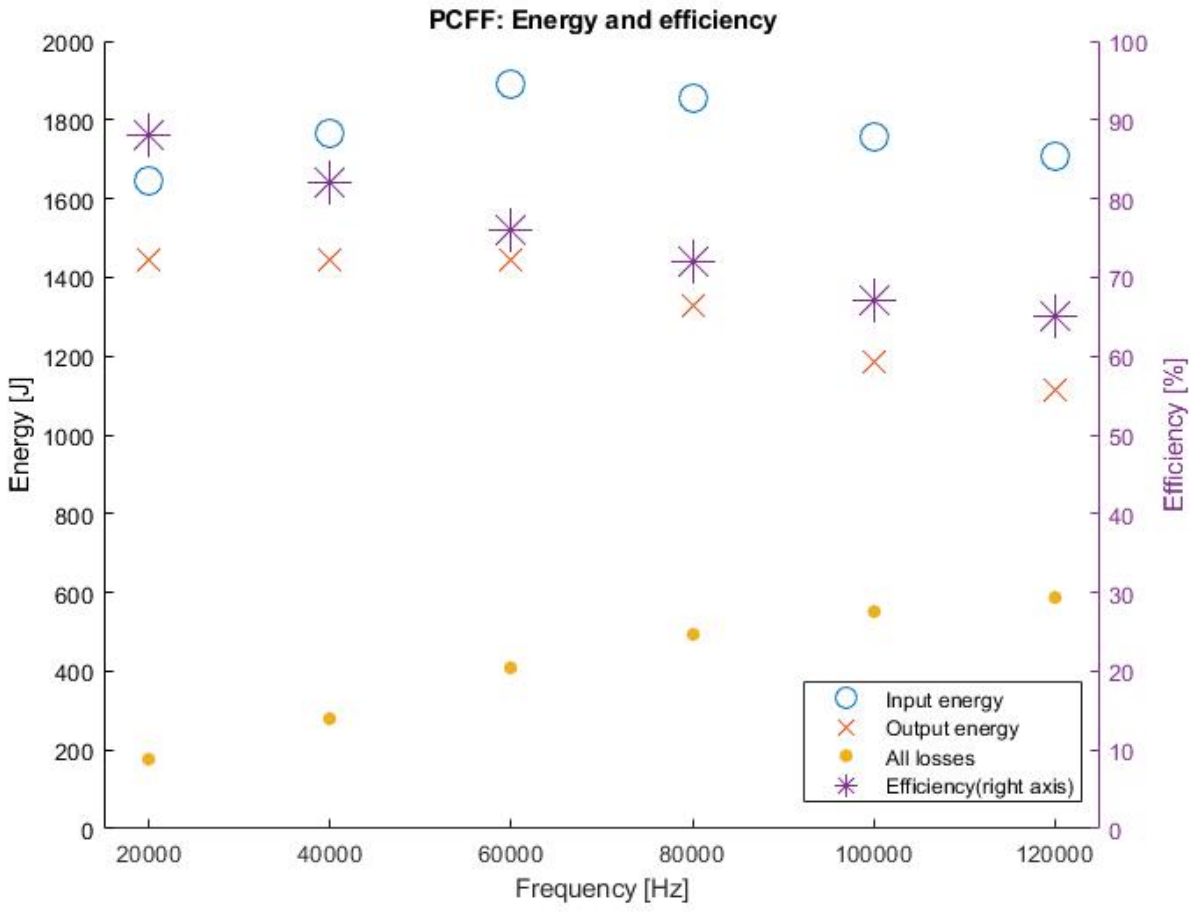


Figure 4.3: Inductance optimized using equation 3.27 at 80 kHz

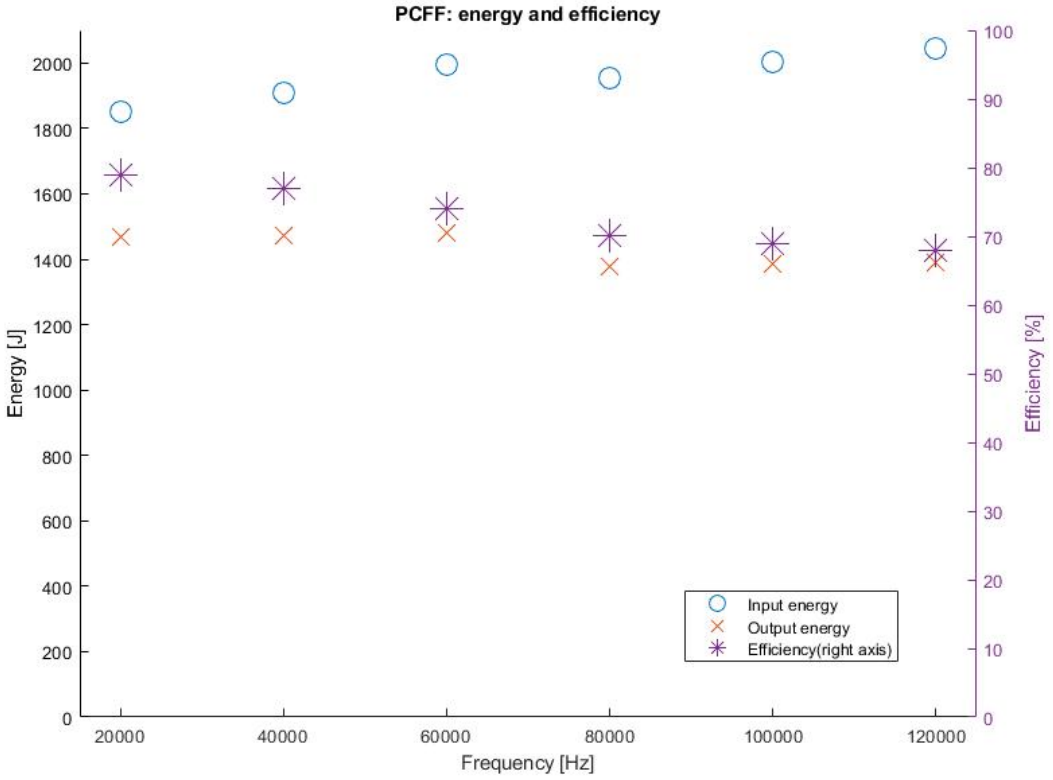
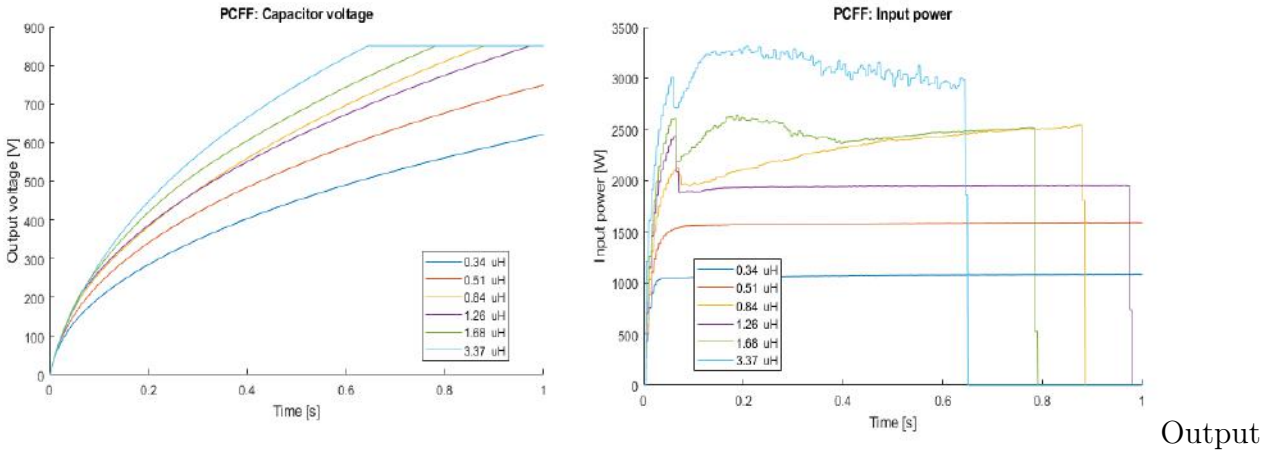


Figure 4.4: Inductance optimized using equation 3.27 for each frequency

The inductance sweep illustrated in figure 4.5 shows that this algorithm requires to much time if the inductance is to high. For this sweep the frequency is optimised for the $0.84\mu H$ primary inductance using equation 3.28.



(a) Capacitor voltage over time

(b) Input power over time

Figure 4.5: Sweep over multiple inductance values

Output

The I_{peak} value has also been swept across and as can be observed in figure 4.7 it must remain high for the algorithm to work.

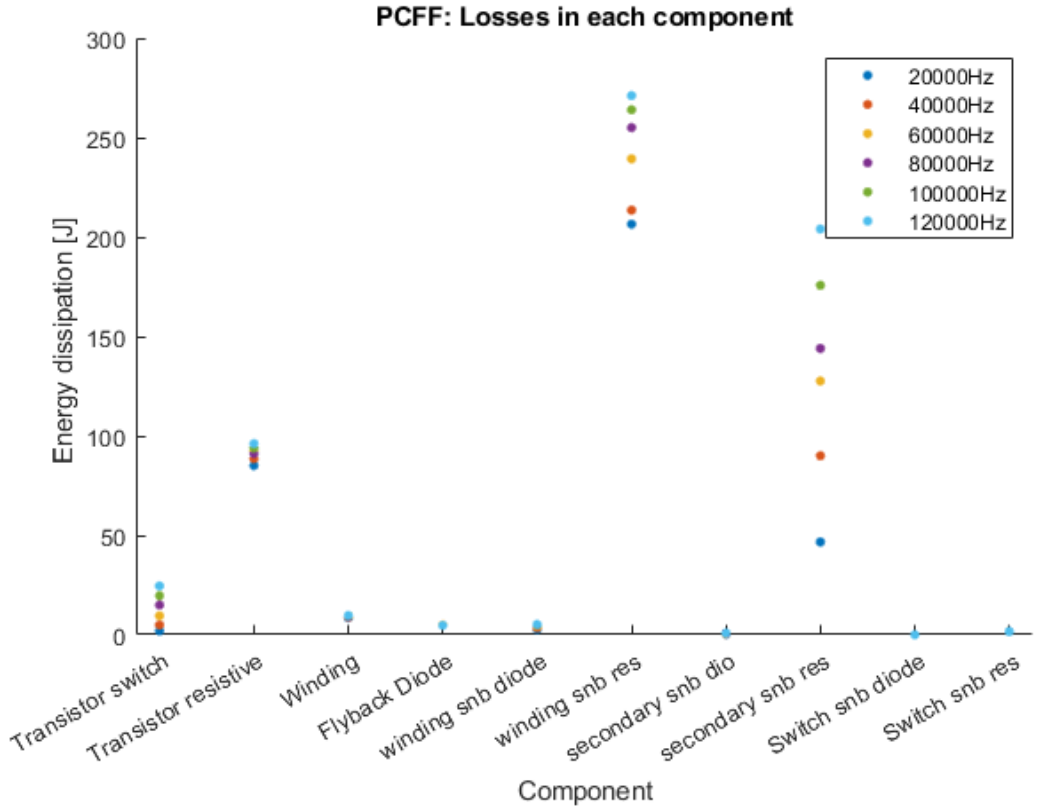
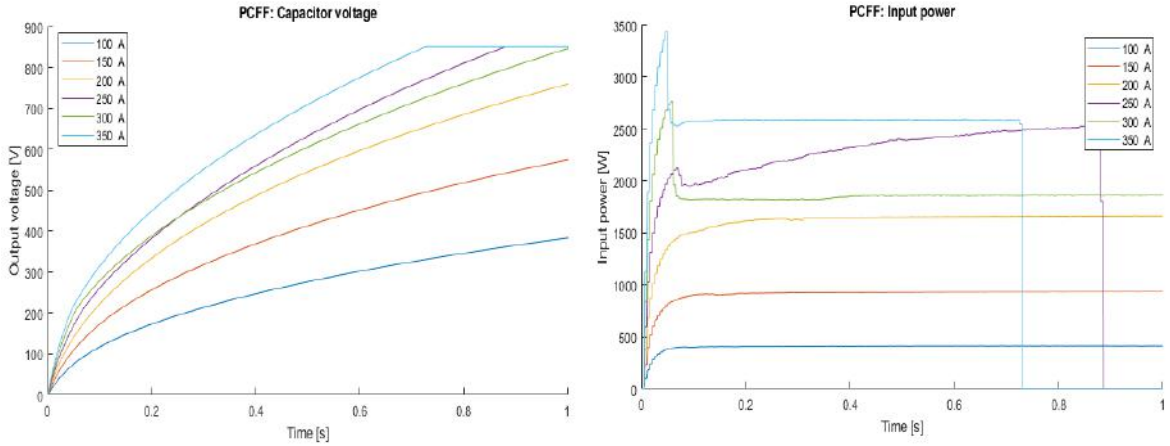


Figure 4.6: Losses in each component when varying the frequency



(a) Capacitor voltage over time

(b) Input power over time

Figure 4.7: Sweep over multiple I_{peak} values

The simulation shows that frequency has an effect on both the input power and the efficiency of the converter when controlled with the PCFF algoritm.

4.2.2 PCDC

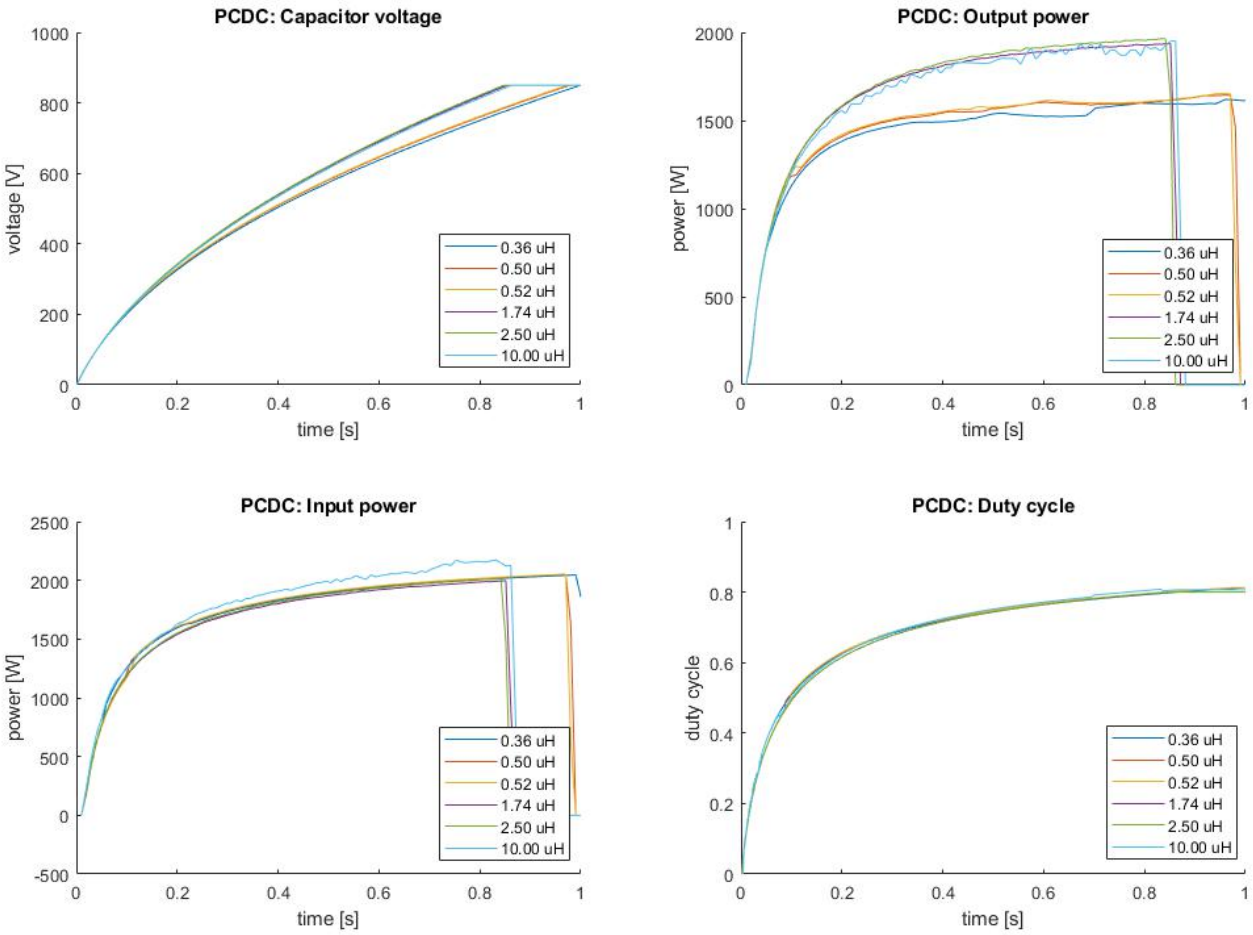


Figure 4.8: Capacitor voltage, input power, output power and duty cycle over one charging cycle for six primary inductance values.

Figure 4.9 shows the losses in each component according to the inductance. In these figures, each snubber is regarded as one component, although the snubber actually consists of three discrete elements, a resistor, a capacitor and a diode. The losses are restive losses in the resistor.

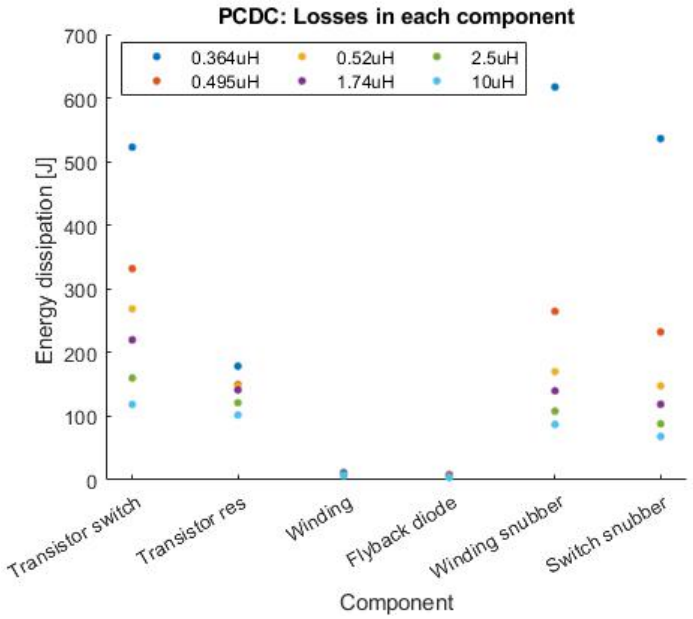


Figure 4.9: Losses in each component when varying the primary side inductance. The turns ratio is kept at 1:10 primary:secondary.

Input and output energy and the resulting efficiency for six values of i_{pk} are presented in figure 4.11

The losses in each component are shown in Figure 4.10. Since three of the values of I_{peak} did not reach the target voltage, the simulated losses are much lower for those. To make the comparison fair the losses for values of I_{peak} have been scaled by dividing the energy in the fully charged capacitor (1445 J) by the output energy of the simulation.

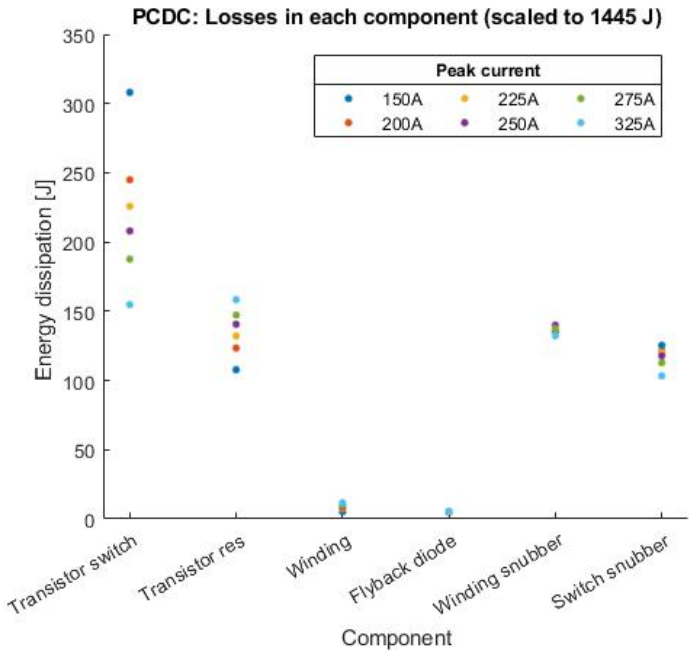


Figure 4.10: Losses in each component for varying values of I_{peak}. Losses have been normalized to a full charge cycle for $I_{peak} = 150, 200, 225A$ since they did not meet the target voltage in one second. For this simulation a model of the MOSFET transistor was used which results in the higher switching losses compared to the resistive losses.

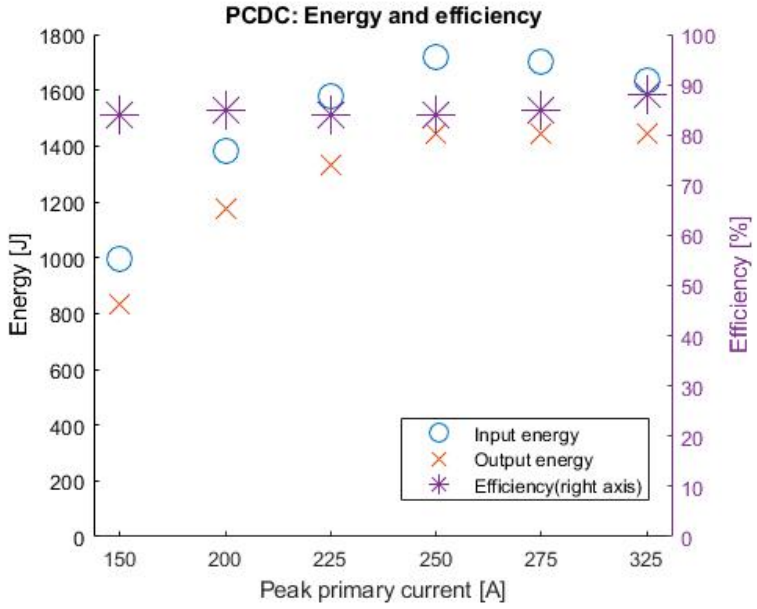


Figure 4.11: Input, output and efficiency for a full charging cycle for fix values of i_{pk}

Figure 4.12 shows how the turns ratio effects the energy and efficiency of the FC and figure 4.13 shows how the output voltage and the duty cycle is effected.

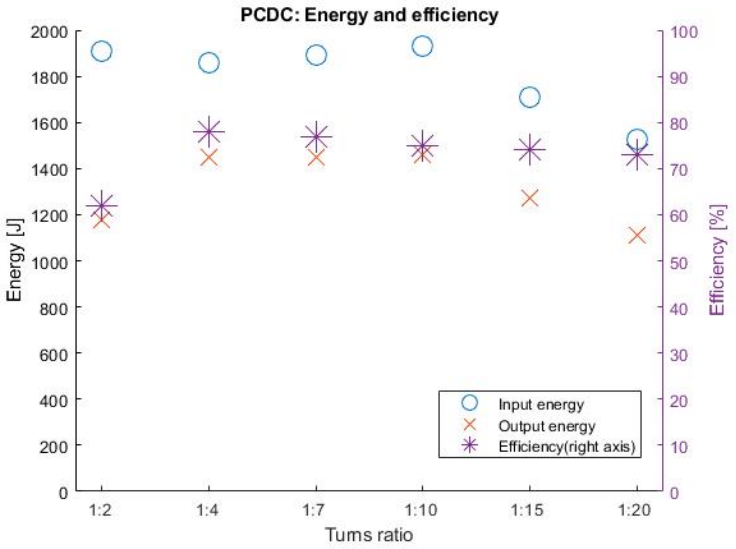
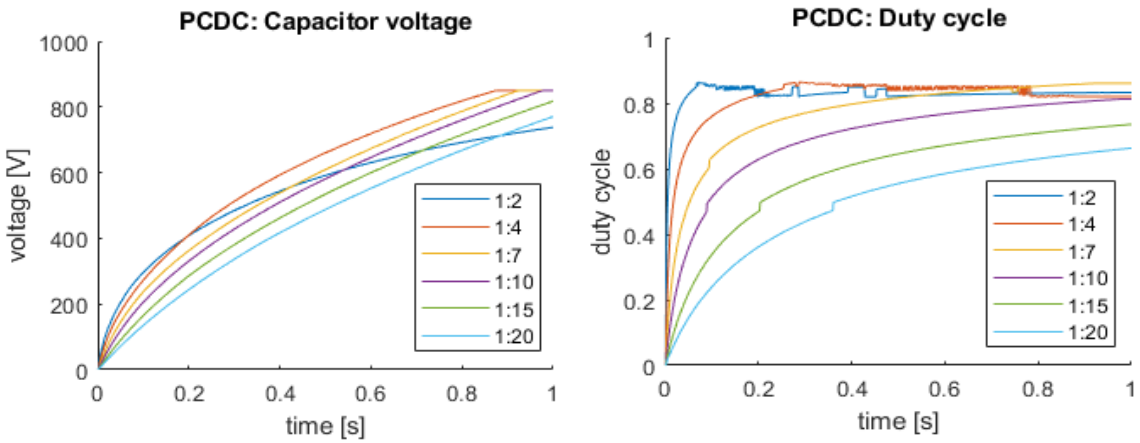


Figure 4.12: Input, output and efficiency for a full charging cycle for different turns ratios



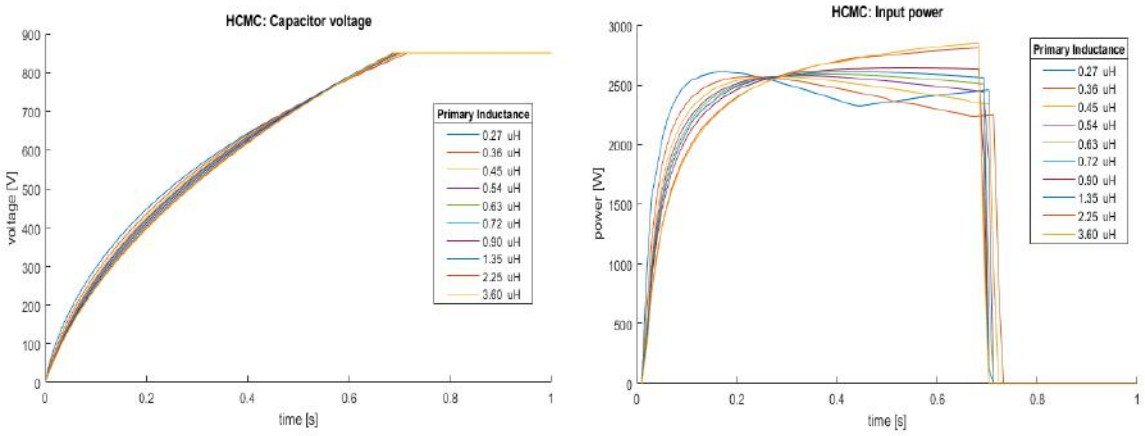
(a) Capacitor voltage over time

(b) Input power over time

Figure 4.13: Sweep over multiple coupled inductor turns ratios

4.2.3 HCMC

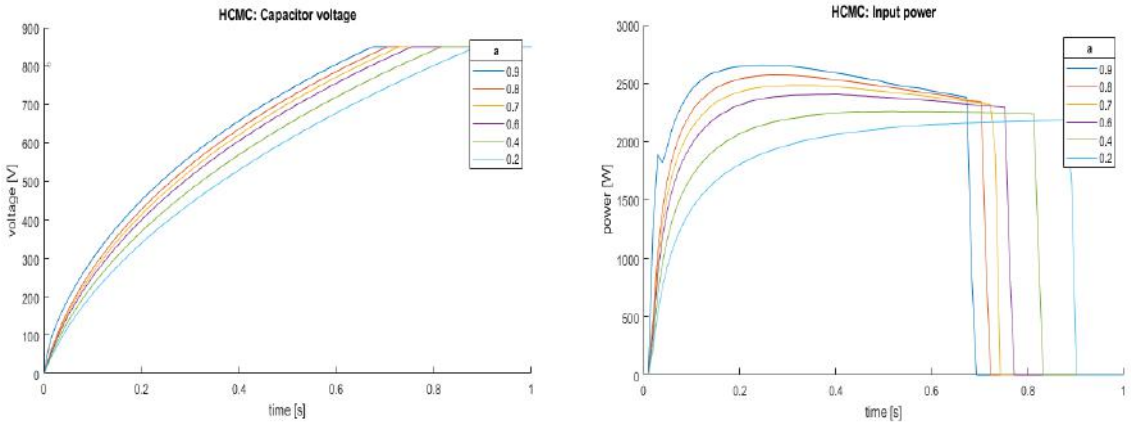
In simulations the HCMC algorithm works, as can be seen in figure 4.14 the capacitor voltage rises until the target voltage is reached at which point the power input drops to zero. It can also be observed that the inductance has little effect on the duration off the charging sequence but might affect the power that the system draws.



(a) Capacitor voltage over (b) Input power over time

Figure 4.14: Sweep over multiple inductance values

as can be seen in figure 4.15 the a parameter has a significantly higher effect on the performance than the inductance. From the charging duration and power inputs it seem as though a higher a is better. Looking at figure 4.16 it becomes clear that there is a drawback, the losses also increase with a.



(a) Capacitor voltage over time (b) Input power over time

Figure 4.15: Sweep over multiple a values $i_{pk} = 170A$

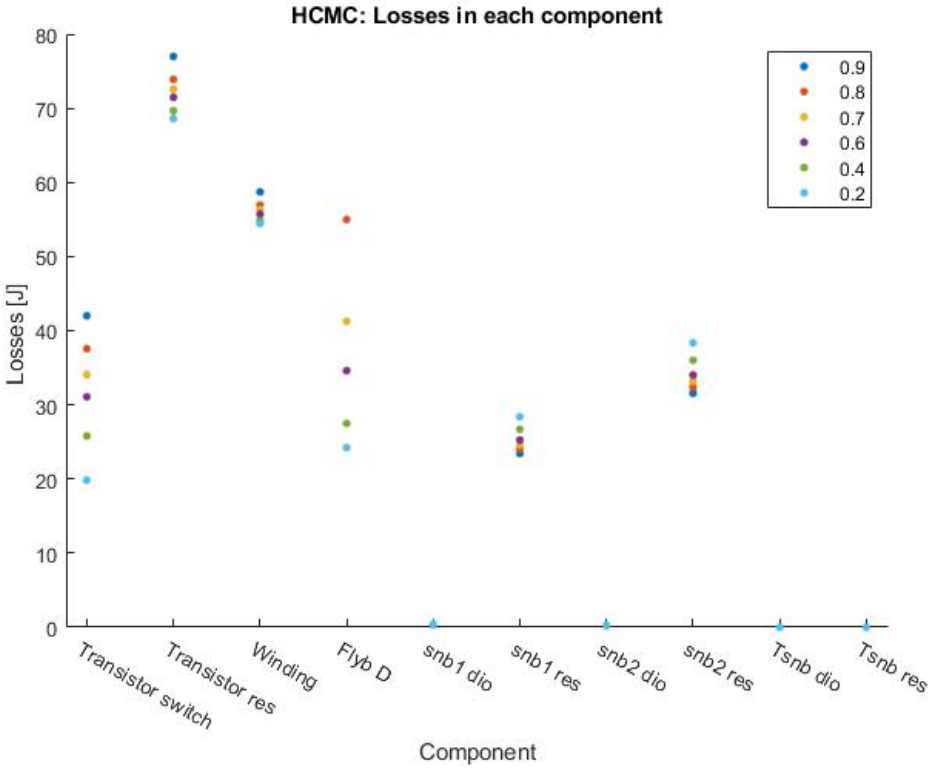


Figure 4.16: Losses in each component when a is swept from 0.2 to 0.9. A bug in the simulations causes the diode losses to be abnormally high. Snubber 1 is the snubber across the primary winding. Snubber 2 is the snubber across the flyback diode.

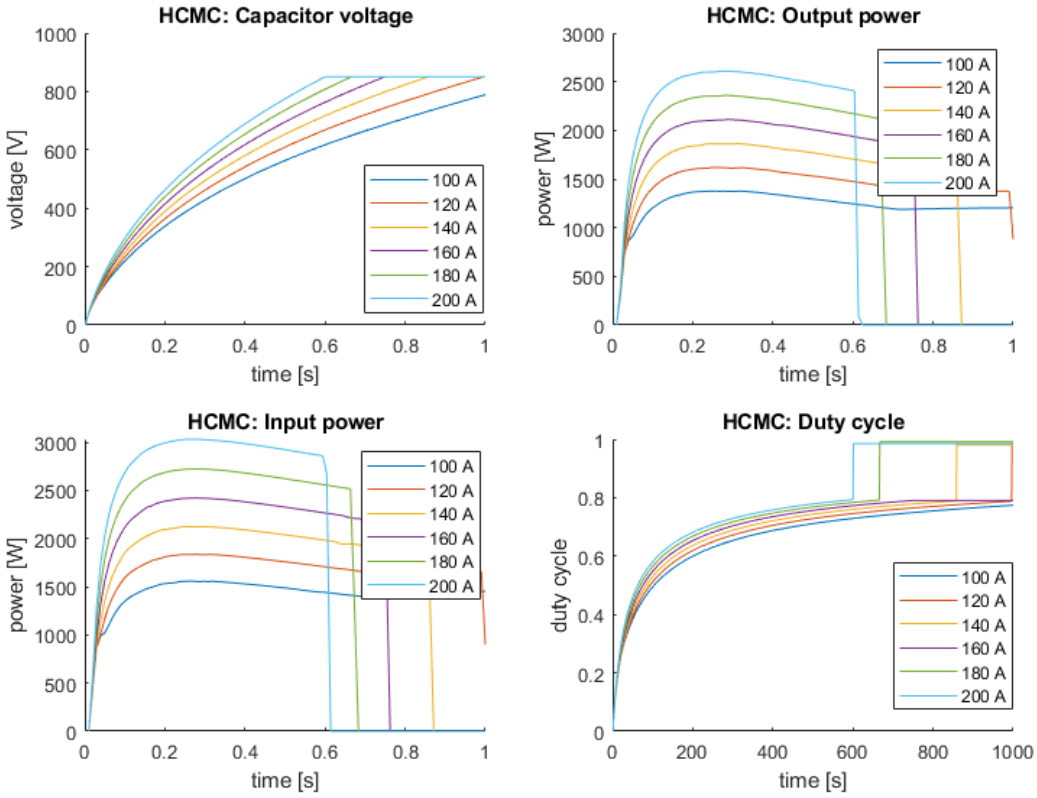


Figure 4.17: Capacitor voltage, input power, output power and duty cycle from the peak current sweep.

4.2.4 Simulation discussion

The simulation results show that the inductance value does not matter much for the charging capabilities of the PCDC and HCMC control algorithms, which can be seen in figures 4.14a and 4.8. However, for the PCFF algorithm the inductance must be high.

As can be seen in figure 4.2 the frequency of the PCFF mostly affects the end of the charging sequence. The algorithm fails to charge the capacitor when the frequency is too high. Comparing figure 4.3 and 4.4 it can be seen that using equation 3.28 gives a higher efficiency compared to using a too high frequency, but that a too low frequency actually has higher efficiency than what is found using 3.28.

The peak primary current sets the input power and the simulations show that a peak current of 250 A or more is needed for the PCFF and PCDC algorithms. However, HCMC can deliver the necessary power with a peak current value of only 120 A. This is because the primary side current does not have to start from 0 in every switch cycle, thus the average current can be kept high enough even with a much smaller peak current. This is good for a tight design because the size of the inductor core increases with the peak current according to equation 3.36.

Sweeping the value of a in the HCMC algorithm shows how the compromise between switching often, switching with higher currents and the average power all vary with a. Higher values of

a give a higher average power but the losses also increase since more switches are needed and the turn-on losses of the transistor increase when the current through the inductor is higher at turn-on.

The turns ratio is important to the requirements on the components as discussed in section 5.1. It also affects the efficiency of the converter when the PCDC algorithm is used. A ratio that is too low is ineffective and a ratio that is too high reduces the input power. The 1:10 ratio has both high power and acceptable efficiency.

The losses appear mostly in the transistor and the snubber resistors. This reduces the number of components that need to be connected to a heat sink.

Chapter 5

Implementation

5.1 Selection of components

5.1.1 Control circuit

The selected control algorithm, PCDC, can be preformed by the LT3750 integrated control circuit from Linear Technology [7]. This circuit uses a current sensing resistor R_{sense} in series with the transistor to determine when the current through the transistor has reached I_{peak} and it's time to switch off the power transistors. The voltage across R_{sense} is compared to a fixed voltage of 78 mV in an internal comparator, thus:

$$I_{peak} = \frac{0.078}{R_{sense}} \tag{5.1}$$

When the secondary side current has decayed to zero, the flyback diode becomes reverse biased and no reflected voltage is seen across the transformer. Thus the voltage at the point between the power transistors and the transformer, V_{switch} is the same as the input voltage when no current is flowing through either side of the transformer. The LT3750 uses this fact to determine when the secondary side current has decayed to zero and a new switching cycle is to begin. V_{switch} is compared to the input voltage V_{in} plus an additional 36 mV bias.

$$DCMdetected \iff V_{switch} \leq V_{DC} + 0.0036[V] \tag{5.2}$$

This means that in order to detect DCM, the reflected voltage must drop below this bias. The lowest reflected voltage occurs when the output voltage is zero, and the only reflected voltage comes from the forward voltage drop across the flyback diode, V_{diode}. This effectively puts a limit on the transformer ratio:

$$N \leq \frac{V_{diode}}{0.036} \tag{5.3}$$

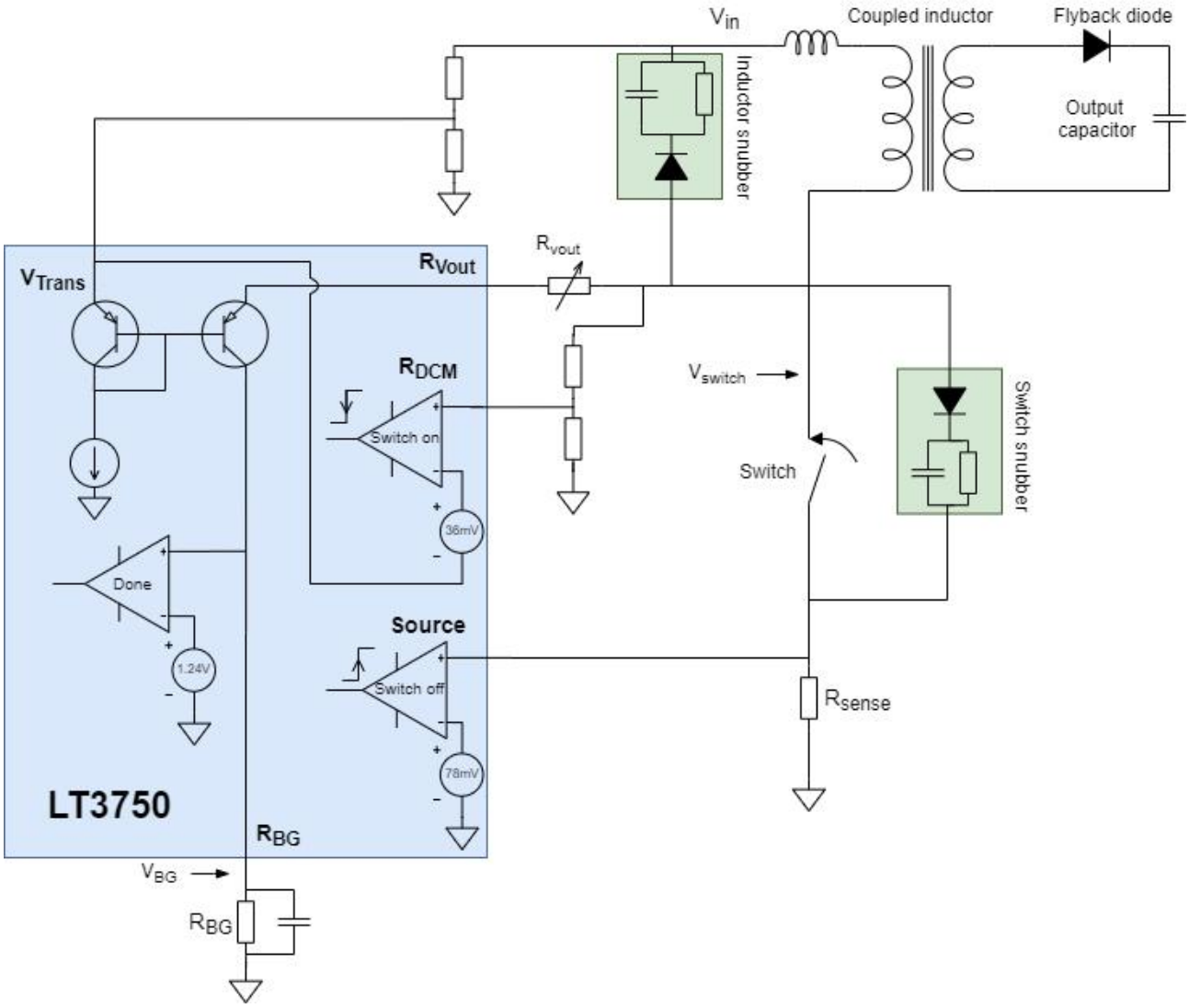


Figure 5.1: The measurement points in the control circuit and their connection to the rest of the FC.

For a diode with a forward voltage drop of 1.5 V this means that the winding ratio has to be less than 41.

The reflected voltage is used to determine when the charging has finished. V_{switch} is connected to the LT3750 via a resistor, R_{Vout}, and the signal passes through an internal current-mirror and another resistor, R_{BG}, before connecting to ground. The voltage V_{BG} that appears across R_{BG} is fed to an internal comparator with a reference voltage of 1.24 V. The target voltage is set by R_{Vout}, R_{BG} and the turns ratio.

$$V_{target} = \left(1.24 \cdot \frac{R_{vout}}{R_{BG} \cdot N}\right) - V_{diode}[7] \tag{5.4}$$

5.1.2 Voltage blocking semiconductors

The reflected voltages puts high requirements on the semiconductors in the circuit and forces a careful selection of turns ratio. The goal is to get the secondary side capacitor to 850 V, if the turns ratio is too low then this voltage, reflected to the primary side, can break the power transistors. Likewise if the turns ratio is too high the 24 V that feeds the primary side might reflect a voltage high enough to brake the flyback diode. If the turns ratio is 1:10 then the expected voltage on the primary side will be the 24 V supply plus the 85 V reflected voltage which sums up to 109 V. For the secondary side the flyback diode must be able to withstand the 850 V from the capacitor plus the 240 V reflected from the primary, a total of 1090 V. Components that are able to block these voltages are available and are usually produced in brackets where the voltage ratings are seperated by about a few hundred volts. Meaning that the transistors and diodes can be selected with ratings of 600, 1200 or 1700 V. Since the system is an SMPS and prone to voltage spikes the rating of the components should be a couple of hundred volts higher than the calculations suggest. Thus 1700 V in blocking voltage is selected for the flyback diode

For the power transistors 600 V blocking voltage is deemed sufficient. Given the large currents that will pass, an IGBT is the most suitable transistor type due to its low forward voltage drop. The forward voltage drop and the switching losses are the two biggest factors influencing the performance of a power transistor. Typically an IGBT has lower forward voltage drop than a MOSFET and thus has lower conduction losses. The MOSFET on the other hand typically has shorter turn on and turn off times reducing the amount of switching losses. When optimising a balance between the two kinds of losses must be found and thus it was decided to try this FC with both types. Two IGBTs with suitable rating were identified, AIKW50N60CT [8] and STGW30H60DFB [9]. Finding a MOSFET with an acceptable forward voltage drop was difficult but the silicon carbide C3M0065090D [10] had the appropriate ratings.

The flyback diode requires a significantly higer blocking voltage rating and silicon carbide was the only real option in an appliction like this. The Schottky diode structure was selected due to its reverse recovery time being virtually zero. The GB05MPS17 diode [11] was selected.

5.1.3 Inductor core

Selecting the inductor core was a difficult task and needs to take all of section 3.5 into consideration. Given inequality 3.34 the number of turns n had to be kept low, and given inequality 3.37 in combination with equation 3.35, the number of turns should be kept high. Balancing this trade off poses some challenges but three ferrite E-cores that fulfil the demands were identified. The geometrical E shape was selected for three reasons, it is cheap, readily available and is the simplest core type to wind and mount on a PCB.

Three different core sizes were selected as can be seen in table 5.1. The three different sizes were selected to account for uncertainties in the calculations and the idea is to test all three and see which ones work. The largest one was selected to guarantee that the core does not saturate, the medium one satisfies all conditions and the small one is the smallest E-core that could feasibly avoid saturation.

Core	n	Inductance [nH]	3.42 holds [yes/no]	$B_{max}at250A$ [T]
E55/28/21 [4]	1	496	Yes	0.314
E65/32/27[5]	1	526	yes	0.209
E70/33/32 [6]	2	2620	no	0.419
E70/33/32	1	655	yes	0.209

Table 5.1: The most important values for each core under consideration

5.1.4 Snubber components

Two snubbers are used in the design, one across the primary winding and one across the power transistors. No snubber on the secondary side is necessary because the current is allowed to decay to zero before the power transistor is turned back on. The resistor value was small enough to allow the snubber capacitor to fully discharge before each switching event.

5.1.5 Electrical design

Figure 5.2 illustrates the schematics of the PCB that was built. Notice that some electrical nets are not drawn in the circuit, ground and supply appear in multiple places.

The LT3750 cannot deliver enough current to turn on the four power transistors, thus a darlington connection is used where the controller only needs to turn on one MOSFET. The IGBT gates are only rated for 20 V and thus a voltage divider was used between the supply and ground giving the gates 14 V each.

The LT3750 is rated for a maximum of 24 V, since this is the intended supply voltage and the actual supply might be higher, voltage divider and regulators are used to guarantee that the

rating is not exceeded. This can be seen on the RDCM pin, the Vtrans pin and Vcc. Remaining pins are either outputs or can handle higher voltages.

The target output voltage can be determined by dividing the reflected voltage going into R_{vout}. This voltage division can be seen in the top left corner of figure 5.2. Since the system must be able to change the output voltage between 600 V and 850 V potentiometers have been used here. The IC is a digital potentiometer that can be set by a microcontroller, this IC in series with resistor R8 allows the vehicle to set the output voltage anywhere in the specified range. The digital potentiometer is connected in parallel with regular turn potentiometers, these were added to the circuit to make testing easier.

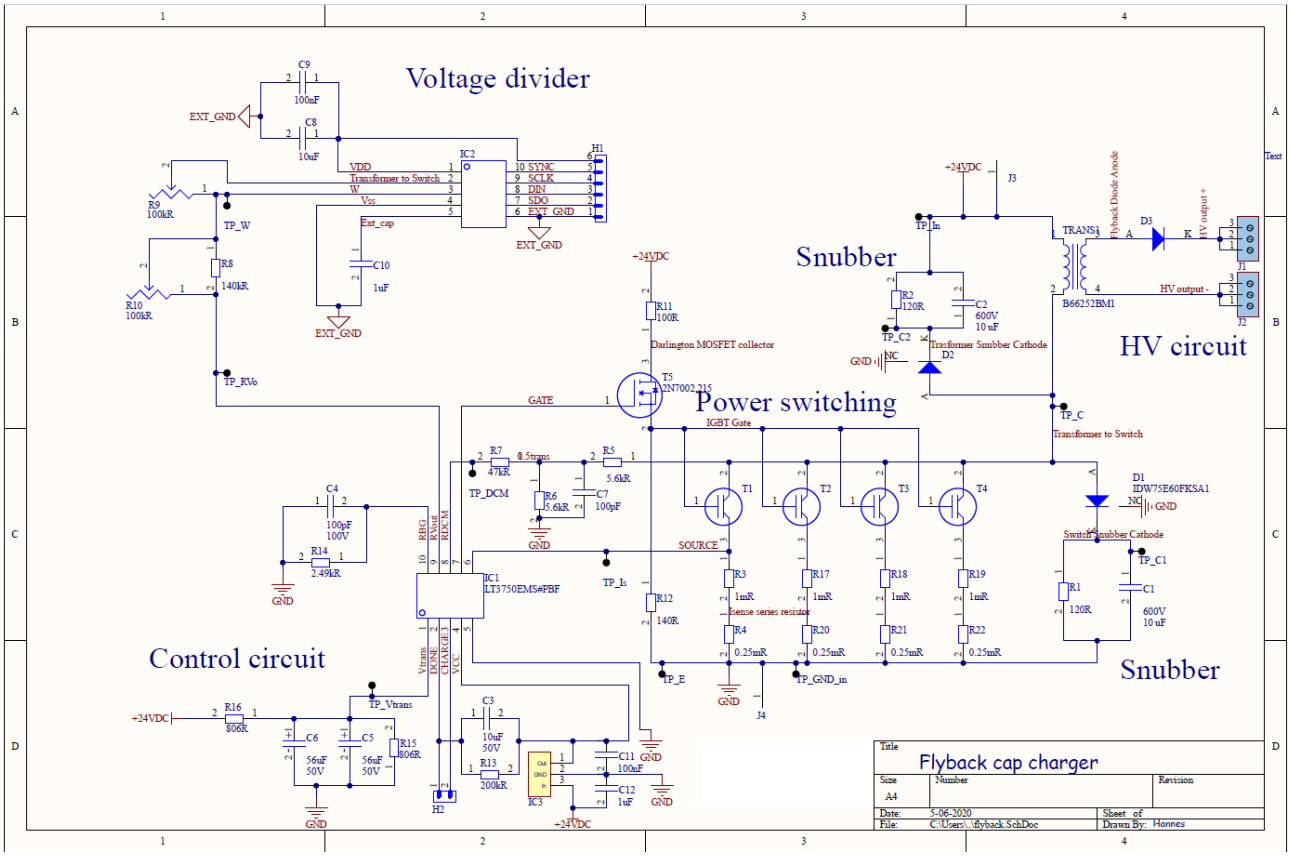


Figure 5.2: Electrical schematic used for the PCB

5.2 Physical design

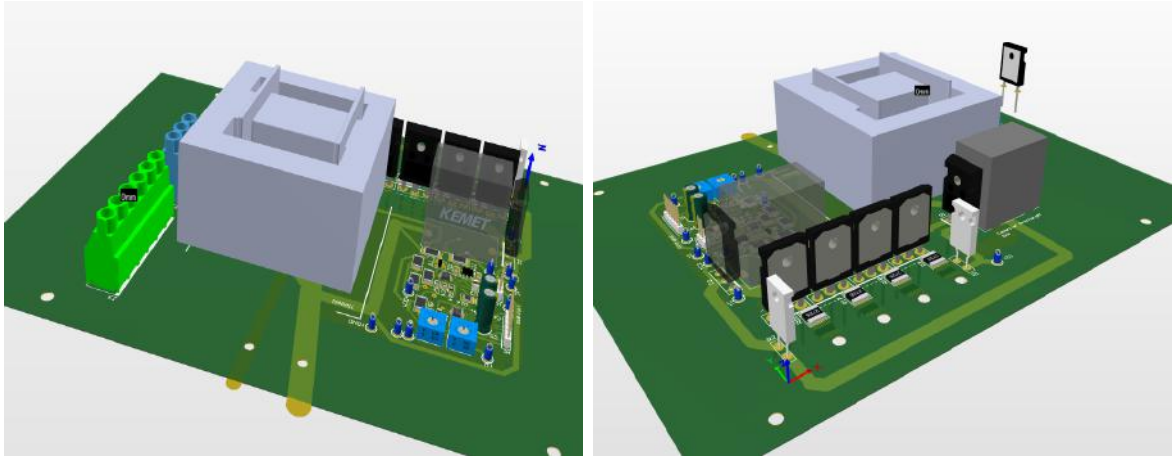
Before the design of the PCB begun, a few preconditions were established:

- The PCB should be rectangular
- The high current path should be as short as possible
- The return high current path should be directly underneath the input high current path
- The footprint of the transformer should be the same for all three sizes of inductor cores

- The bottom layer should be a large ground plane with few traces in it
- The secondary side with high voltage traces and components should be separated and have sufficient distance to the low voltage primary side
- The traces from the driving MOSFET to the power transistors should be equidistant for all four transistors
- The current sense path from the source/emitter leg to the control circuit should be kept short
- Rotary potentiometers, headers, and test points should be easy to access

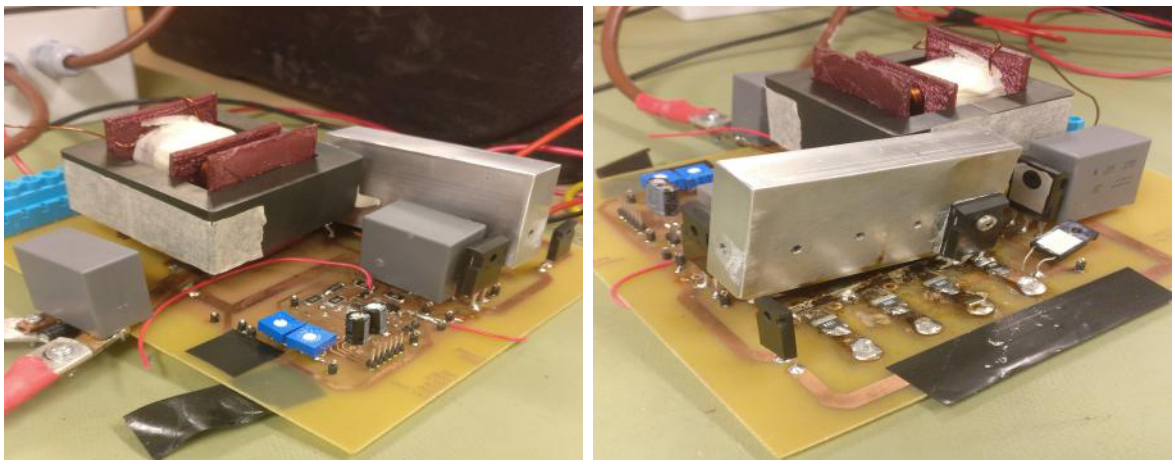
The first design iteration had a straight copper sheet from the transformer primary output with the transistors in a row sticking out from the transformer. This design left a lot of unused space on the PCB, and it was reckoned that a 90°turn on the copper sheet could be made in order to fit the transistors closer to the transformer. This bend would be placed right underneath the inductor core as seen in figure 5.3a. Initial placement of the components with the first six points above in mind resulted in a much smaller design than the original layout. Problems arose when it came to placement of the primary side winding snubber. The spatially large capacitor was difficult to fit on the PCB, it can be seen as large grey component in figure 5.3b and 5.4b. Fitting it near the low voltage input would result in high spike currents running around the control circuitry. Instead it was fitted near the power transistors. This has the added benefit that the snubber resistor can share a heat sink with the transistors.

The high currents used in the FC puts demands on the current path that an ordinary PCB can't satisfy. With an I_{max} of 250 A and a copper trace thickness of 0.1 mm, a very wide trace would be needed. Instead copper sheets where cut and soldered together to get a high current trace of around 3x5 mm^2. This trace can be seen going in under the core in figure 5.3a and 5.4a, the trace then continues to the transistors.



(a) Control circuit to the right (b) Power Transistors without heat sink

Figure 5.3: 3D render of the PCB design.



(a) Control circuit to the right (b) Single Power transistor mounted

Figure 5.4: Actual circuit built for testing

5.3 Construction

5.3.1 Coupled inductor measurements

The measurements were carried out using banana plugs and lab style cables. The impedance of the oscilloscope probes was a 1 MΩ resistor connected in parallel with a 15 pF capacitor. The theory is described in section 3.5.1.

The inductance of the coupled inductor was measured on the secondary side by connecting a waveform generator with a sine wave output in series with a radial resistor $R_{measure} = 2.4\ \Omega$ and the coupled inductor secondary winding. The voltage across the resistor and the voltage across the inductor were measured with oscilloscope with the common node used as reference. The waveform generator produced a sinusoidal signal and it's frequency was increased until the voltage across the resistor was equal in magnitude to the voltage across the inductor, which means that equation 5.5 holds.

$$R_{measure} = |Z_{inductor}| = |j \cdot L_{inductor} \cdot \omega| \tag{5.5}$$

It was ensured that the voltage across the resistor lagged behind the voltage across the inductor by 90°.

The same measurement was attempted on the secondary side but the phase shift between resistor voltage and inductor voltage was not 90°in these measurements.

The turns ratio was measured by connecting the secondary side directly to a waveform generator using a sine wave with a frequency of 1 MHz. The voltage was measured on both sides using oscilloscope probes from the same oscilloscope which means that both sides of the coupled inductor were connected to the same reference point. Additional turns were added or removed

on the secondary side until the oscilloscope showed a voltage gain of 0.1 from secondary to primary side.

5.3.2 Rework

As soon as the first circuit was built it became clear that there were some shortcomings in the design. Fortunately the PCB was designed in a way that could easily accommodate changes, the most essential ones are shown in figure 5.5. The current measurement turned out to be very noisy and would trigger on a very low voltage, so a third order filter was placed at the 'Source' of this pin. The ringing at transistor turnoff was excessive and thus the transistor snubber was altered to a RC-snubber in order to deal solely with that ringing.

The controller could not measure when the reflected voltage was high enough to end the charging sequence. It would always output a done signal after a couple of switches when the output was still only between 20 V and 30 V. This was bypassed by cutting the trace to R_{Vout} and charging the capacitor at R_{BG} from an external micro controller. Doing this allowed for exact control of the duration of the switching sequence but leaves the system blind to the output voltage.

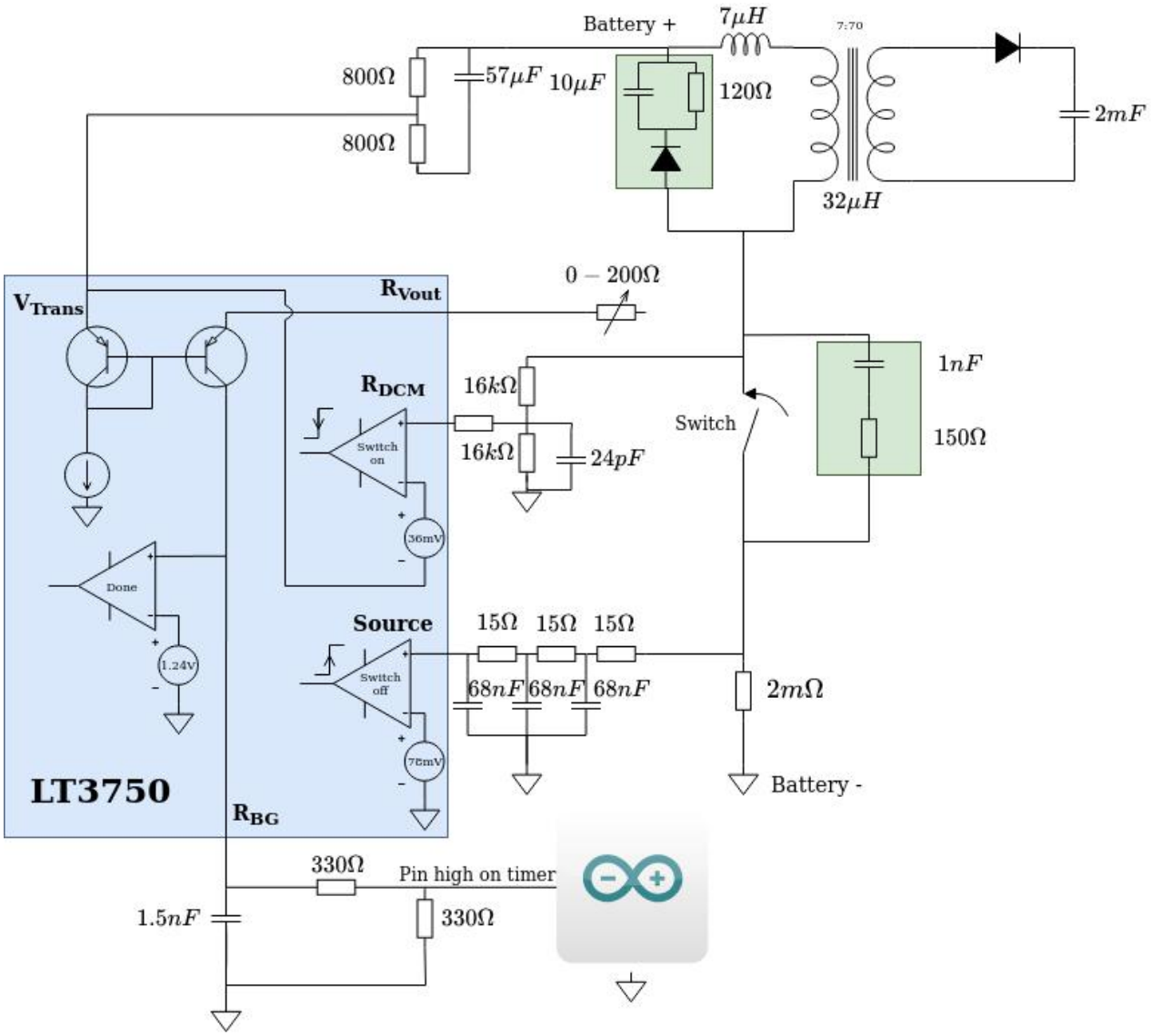


Figure 5.5: Essential rework of the control circuit

Making one more tweak to the system as shown in figure 5.6 allows the system to run in PCFF. This is accomplished by putting a diode at the R_{dcm} pin and connecting the capacitor to the cathode. This makes sure that the capacitor is charged to the reflected voltage level at transistor turnoff but it has to discharge through the voltage divider resistors. The controller will start a new switch cycle when the capacitor is discharged to 12.036 volts. This means that the switching frequency will be determined by the time constant of the RC-circuit and a fixed switching frequency is achieved. The time constant was selected so that the FC enters DCM after only a few switches and has a long dead-time at the end of the charging sequence.

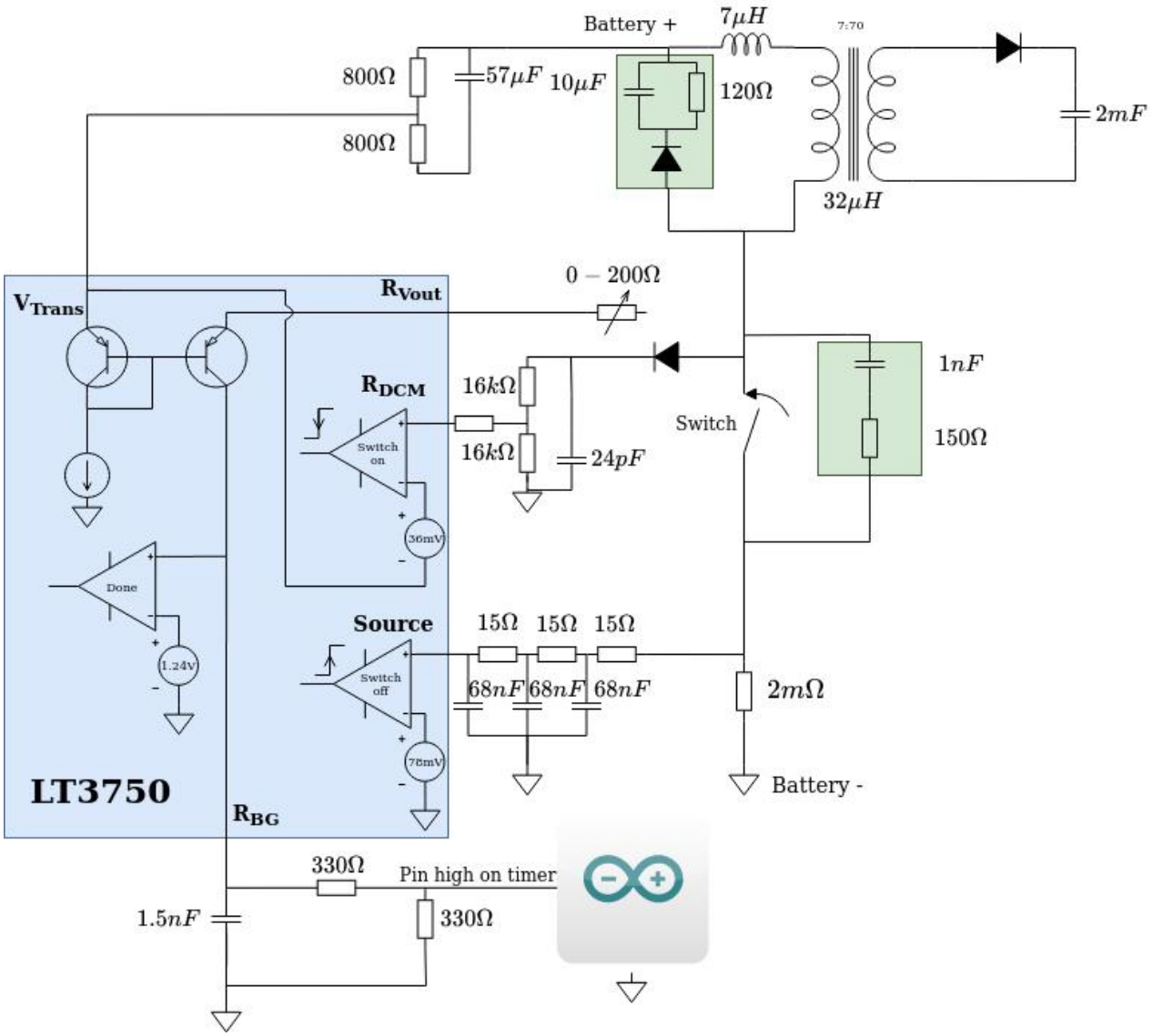


Figure 5.6: Rework that allows for PCFF control

Chapter 6

Results

6.1 Laboratory Results

6.1.1 Coupled inductor measurements

The measurement of the turns ratio shows a voltage gain of approximately 0.1 from secondary to primary side for all three inductors. The actual number of turns on the secondary side was nine for the smallest inductor core and ten for the medium and large cores.

Measurement of the secondary side inductance can be seen in table 6.1 below. The cores can be found in table 5.1

Core size	Sine frequency	Z_L	L
Large	7.2 kHz	2.4 Ω	53 μH
Medium	16.7 kHz	2.4 Ω	23 μH
Small	12.0 kHz	2.4 Ω	31 μH

Table 6.1: Results from coupled inductor measurements on the cores that were not successful in the experiments.

Due to oscillations at the battery input another bobbin was wound in order to reduce the switching frequency. It had seven turns on the primary side and 70 on the secondary. The inductance was measured on both sides using the same methodology as described in section 5.3.1. The results are listed in table 6.2

Side	Sine frequency	Z_L	L
Primary side	11.9 kHz	2.4 Ω	32 μH
Secondary side	1.2 kHz	2.4 Ω	318 μH

Table 6.2: Results from coupled inductor measurements on the core used in the successful experiments. The large core was used with 7:70 turns.

6.1.2 Flyback converter measurements

Figure 6.1 illustrates the typical switch curves attained in the lab. Here the Miller plateau of IGBT and the subsequent charging of the internal capacitor is apparent.

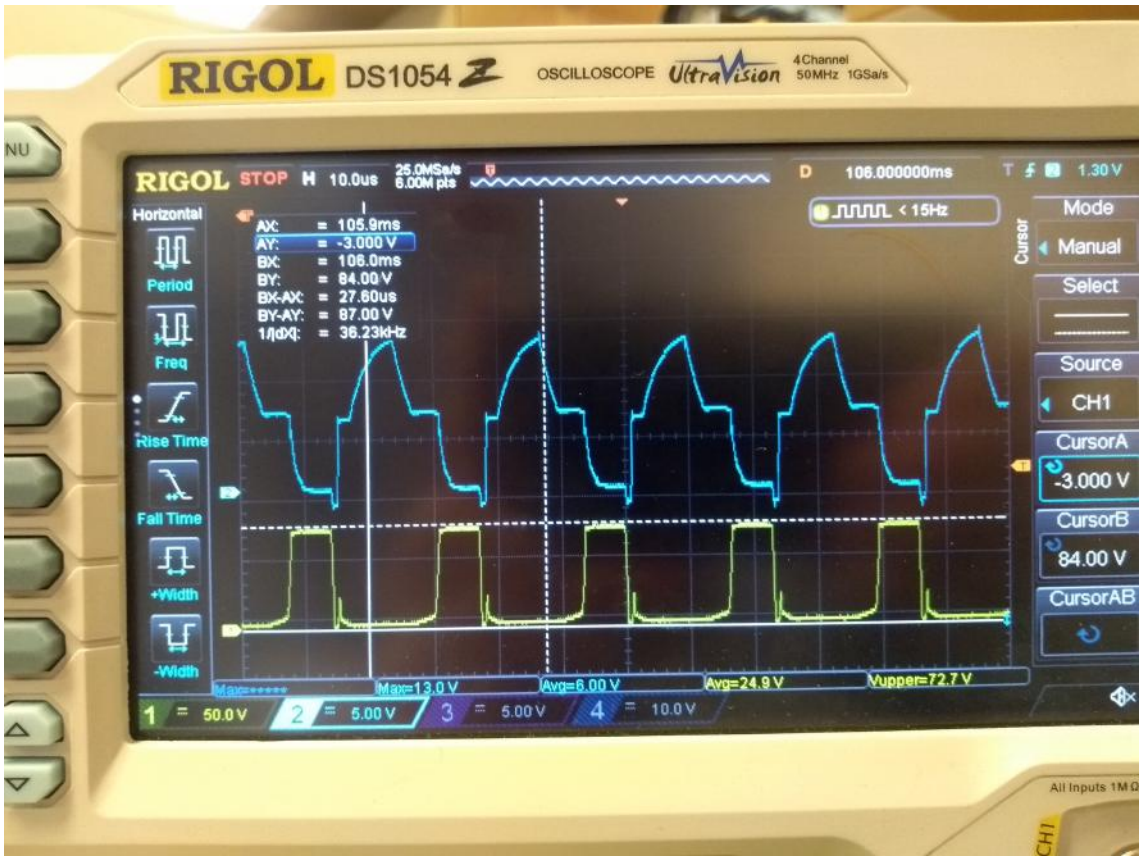
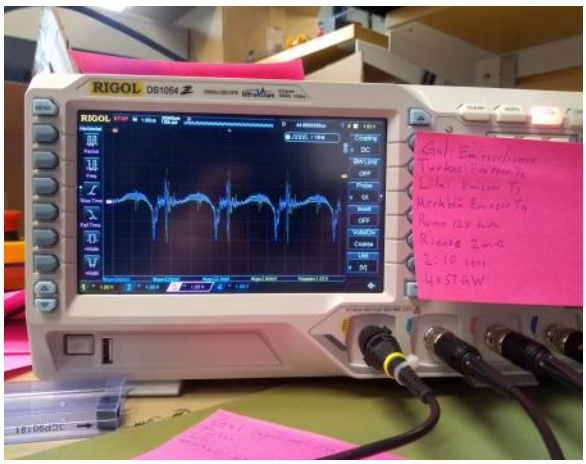
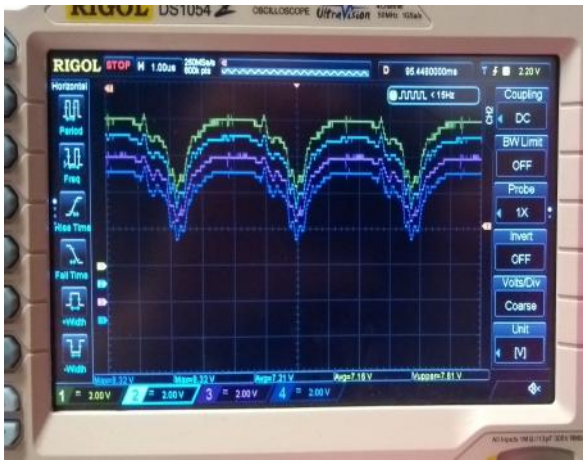


Figure 6.1: typical switch curve attained in the lab. Blue: Gate-emitter voltage. Yellow: Collector-emitter voltage.

Figure 6.2 shows the synchronisation of the power transistors when four of them are connected. It can be seen that they all receive the same gate signal at the same time and that the current is distributed equally.



(a) Current measurement through all four power transistors using 2 $m\Omega$ emitter resistance



(b) Gate signals of the four IGBTs, notice the ground offset

Figure 6.2: Behaviour of four power transistors.

PCFF with a turns ratio of 7:70

The following measurements where achieved using a coupled inductor with seven turns on the primary winding and 70 turns on the secondary winding. Only one power transistor was used.

Putting the system in PCFF the following results where attained. Figure 6.3 shows how the voltage, i.e. energy, in the capacitor increases over time. This is a typical graph with a rapid increase in the beginning and then a plateau. This plateau appears at roughly 380 V after four seconds.

Figure 6.3: Output capacitor voltage

In figures 6.4 and 6.5 one can see the system start in CCM and slowly transition into DCM. Once DCM is reached the dead time of the switches slowly increase. With this approach the output voltage reaches roughly 380 V with an average power of 36.1 W.

(a) Cyan: secondary current. Yellow: V_{DCM}

(b) Cyan: secondary current. Yellow: V_{DCM}

Figure 6.4: early and mid stages of a PCFF switch cycle

(a) Cyan: secondary current. Yellow: V_{DCM}

(b) Cyan: secondary current. Yellow: V_{DCM}

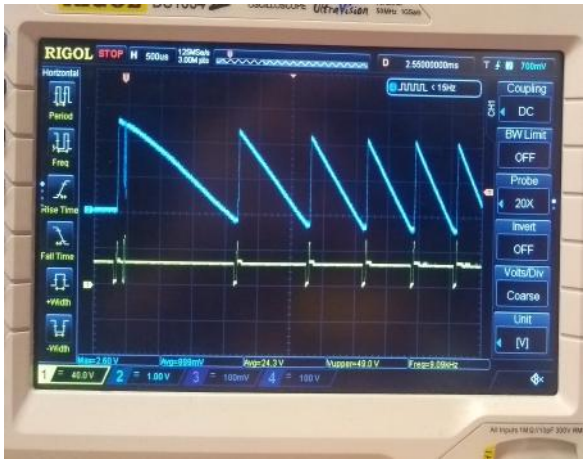
Figure 6.5: Later stages and entire switch sequence in PCFF

PCDC with a turns ratio of 7:70

Putting the system in PCDC the following results where attained. Figure 6.6 shows the output voltage, in this case the voltage does not plateau but the FC is shut down at 600 V in order to stay safely below the capacitor rating.

Figure 6.6: Output capacitor voltage when in PCDC

Figures 6.7a and 6.7b show the early stages of the switching sequence and the later stages can be seen in figures 6.8a and 6.8b. In these switching curves it can be seen that the systems maintains DCM and has almost no dead time.



(a) Cyan: secondary current. Yellow: Power transistor collector voltage

(b) Cyan: secondary current. Yellow: Power transistor collector voltage. Purple: primary current measurement.

Figure 6.7: early stages of PCDC switch sequence

(a) Cyan: secondary current. Yellow: Power transistor collector voltage

(b) Cyan: secondary current. Yellow: Power transistor collector voltage. Purple: primary current measurement.

Figure 6.8: Later stages of the switching sequence in PCDC

6.2 Discussion

6.2.1 Problems with the circuit

One of the performance issues stems from the ground reference and its oscillations. The FC is a noisy system with regards to EMC and the equipment used forced some ground loops into the system. The oscilloscope needs a ground reference from the circuit, the processor that sends and receives charging signals needs a ground reference that follows through to the laptop powering it. These loops in combination with the converter noise made the ground reference unstable.

The current sensor used in this system is resistive, it determines the current by measuring the voltage drop across a low impedance resistor placed on the current path. This measurement became reliable after heavy filtering but it had a large offset. It is believed that there was to much resistance on the high current path due to the multiple large solder points.

6.2.2 Problems with the LT3750 controller

It was decided early on to get an off the shelf controller for the FC. Such a decision always forces the designer to compromise and make a trade off between the desired properties and the properties of the controller that is available. In this case the LT3750 was selected to implement the chosen control algorithm. Unfortunately this circuit suffers from some problems. The biggest one being its rating, When the component was selected it was thought to have a rating of 24 V which could reasonably satisfy the specification. It later turned out that 24 V was its absolute maximum rating meaning that all input pins had to be placed behind the protection of voltage regulators or dividers. Although this worked to some extent it did

cause some undefined behaviour in the circuit. The controller uses the inputs as reference levels for certain measurements and if the voltage reduction on the measurement pin does not match the reduction on the reference pin the measurement is botched. The most sensitive measurement pins were theV_{out}/R_{BG} pins. oscillations on the V_{cc} pin could trigger the done signal prematurely.

This offset problem in combination with a very noisy environment and an oscillating ground reference made all external measurements difficult. After heavy filtering the LT3750 could measure all signals except for one, the done signal. The controller could never identify when the charge sequence was done and thus a workaround was implemented using the micro controller as detailed in section 5.3.2

6.2.3 Problems with the lab setup

During the spring of 2020 when this thesis project was carried out the COVID-19 pandemic struck the world. This forced Volvo into a company wide furlough leaving this project largely without supervision and equipment. The biggest impact of this is that no 24 V truck battery has been used in testing, instead two 12 V batteries were connected in series. The intended 4 mF capacitor has not been used, instead the experimental setup used two 1 mF capacitors connected in series, the performance of which might differ significantly from the ones Volvo would use. The capacitors where rated for 400 V each making it unsafe to charge them higher than about 600 V.

The safety equipment used consisted of one large plastic box shielding the circuitry, two large relays for connecting and disconnecting the batteries and a discharge path for the capacitor. These relays where however sub-optimal and only rated for about a quarter of the current needed. The main problem caused by the relays was that they sent current spikes down the circuit when connecting. At some instances these spikes where strong enough to activate the system and initiate an unintended charge sequence.

No Volvo truck battery was available during testing, instead two 12 V motorcycle batteries where connected in series. These batteries where not capable of delivering the power needed to run the system properly. Setting the peak current to 40 A caused significant supply problems and could trigger under voltage lockout on the controller.

6.2.4 Comparison to resistor relay

As mentioned in section 2.2 this system competes with an existing solution, namely the resistor and relay. There are three fundamental problems with the current solution that the FC can solve; actually reaching the target voltage, doing it within in an acceptable time frame and making it work even if the HVB is dead.

The LVB is an incredibly reliable voltage source and one can safely assume that if the vehicle

works at all, then the LVB works. The same cannot be said about the HVB, lithium ion batteries are fickle and it is crucial that they are not discharged below a certain point. Thus having a reliable low voltage system that can create the bridge to the HVB could prove useful.

At the time of writing this report it was not possible to contact Volvo and ask what resistance they use or the time it currently takes to charge their capacitors. What is known is that the target voltage is not reached and that once the HVB is connected to the capacitor an inrush current spike occurs. At this point it is difficult to say if the elimination of this spike will make it a financially sound idea to replace the resistor and relay with the FC. The extra weight that the FC would add must be considered as well.

6.3 Conclusions

Looking at the performance of the FC a couple of conclusions can be drawn directly. By looking at the switching action in figure 6.8b it can be seen that the timing is very precise, the primary current looks noisy but this is because the probe is placed before the passive filters. This shows that both primary side current measurements and reflected voltage measurements work well. However, the target output voltage measurements does not work in the test circuit which leaves the system blind and possibly dangerous if the output voltage gets too high. This needs to be resolved and could possibly be done by use of external voltage measurements on the car if they are sufficiently fast.

Looking at the secondary side current it is consistently decaying to zero and no spikes are observed, this confirms that no secondary side snubber is needed just as the simulations showed. The ringing between the power transistor and the coupled inductor was worse than anticipated and required an RC snubber across the transistors, initial fears of having the snubber capacitor oscillate with the coupled inductor proved unwarranted.

Given that neither the coupled inductor windings nor the heat sink has any excessive heating it can be determined that the heat dissipation is close to what was predicted. The heat sink used in the circuit is slightly larger than the one in the simulations and the power throughput is lower than anticipated. With this in mind it can still be concluded with confidence that heating will not be a major problem.

6.3.1 Meeting the specification

The most important part of the specification is whether or not the capacitor can be charged by the FC. The lab results has clearly shown that this is possible. Looking at figure 6.6 the voltage trajectory is still clearly headed upwards as it reaches 600 V and the FC is turned off. Keeping in mind that this was with only a quarter of the systems full power there is no doubt that the system can reach 850 V before it plateaus.

Again, looking at figure 6.6 one can see that 600 V is achieved within one second of charging.

Increasing that voltage to 850 V would require twice as much energy. If the output capacitor is increased to 4 mF then the output energy must increase eight fold. This means that the output power must increased by a factor of 16 if the time requirement is to be maintained. If a peak current of 250 A is used then the input power can be increased by a factor of six meaning that it will most likely take 2.6 seconds to charge instead of one second.

In order to assess the temperature rise in the system human senses were used. After running the system multiple times there was a perceivable but low temperature difference in the heat sink. Since the system is intended to be used once and then be in rest for multiple minutes before it is used again this is deemed satisfactory.

The high voltage and low voltage systems are galvanically isolated from each other. The bobbin design makes sure that the primary and secondary windings are isolated from each other and kept apart. The remaining test of the galvanic isolation is to connect 3 kV across the coupled inductor and look for any current leaks.

Testing the functional supply voltages of the system has not been possible. The ratings of almost all components allows the system to run on 36 V except for the power transistors. The voltage after the voltage divider on the power transistor gate should not exceed 20 V meaning that the supply voltage should not exceed 34 V.

The size requirement has not been met. Choosing a ferrite E-core breaks this requirement since the core itself is bigger than the specification demands. The complete system with coupled inductor and control circuitry is roughly 260x290x80 mm^3.

At this point there is no way to accurately change the output target voltage. It can be done but would require mapping of what timers yield what voltage, in the lab this has shown reliable results.

6.4 Further work

Due to time restrictions there is some work left to be done on the current implementation, once that has been done one should take a critical look at the system. The work that still remains relies on fixing the done signal instead of working around it as descried in section 5.3.2. If this can be fixed then the digital potentiometer can be implemented and the entire system could be made to function as intended.

If the problems with the done signal can be resolved and the digital potentiometer can be implemented, the next step is to connect all four power transistors and increase the power. At this point it seems plausible that the power throughput could be quadrupled, the power transistors can handle up to 62.5 A each meaning that it might be possible to increase the power sixfold. Drawing the current that this requires will amplify the noise that has been causing so many problems, thus the EMC issues might become the limiting factor keeping the

design from working properly.

If it turns out that the *done* signal cannot be fixed then a new control circuit needs to be developed. It is tempting to build the entire controller with operational amplifiers and discrete components but such a design causes two problems. One being that the space specification cannot be met, such a design would require too much PCB surface. The second problem is that having all discrete components laid out increases the susceptibility to noise, something that has been shown to be of great concern.

The noise concern requires as much as possible of the controller to be fitted in an IC. There are other control circuits available, UCx84x control series from Texas Instrument is one option. The problem with the UCx84x is that it implements the PCFF algorithm, the results of this project indicate that this algorithm might not be able to deliver enough power to fulfil the specification. The second option is to implement the PCDC algorithm with other trigger levels in an ASIC. Altough this approach is costly it is the most likely way to build a functioning controller given the noise levels.

The next target for improvement is the coupled inductor. In order to meet the space requirement the inductor core must be made smaller. In this project there was no time to investigate the limit of the ferrite cores but most likely a ferrite E-core can't be made small enough. Ferromagnetic materials typically saturates at low magnetic flux densities which forces the designer to bring down the inductance and the number of windings. If a nanocrystaline or an amorphous material with a much higher saturation point was selected instead then these design issues would go away. It would allow the inductance to increase which would create a more stable system with a somewhat lower frequency. It would also allow for more turns on each winding which would strengthen the magnetic coupling. It should be possible to get a significantly smaller coupled inductor if the core material was changed.

Another area of improvement is to utilise the fact that the cooling tab on the power transistors are connected to the collector. This means that the transistor heat sink could be made of copper and be a part of the high current path, the collector leg could simply be cut off. The emitter leg could then connect directly to a resistor on the bottom side of the PCB and then connect to the high current return path. A design like this would allow the high current paths to be placed directly on top of each other, reducing the EMC issues.

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.1 Appendix A

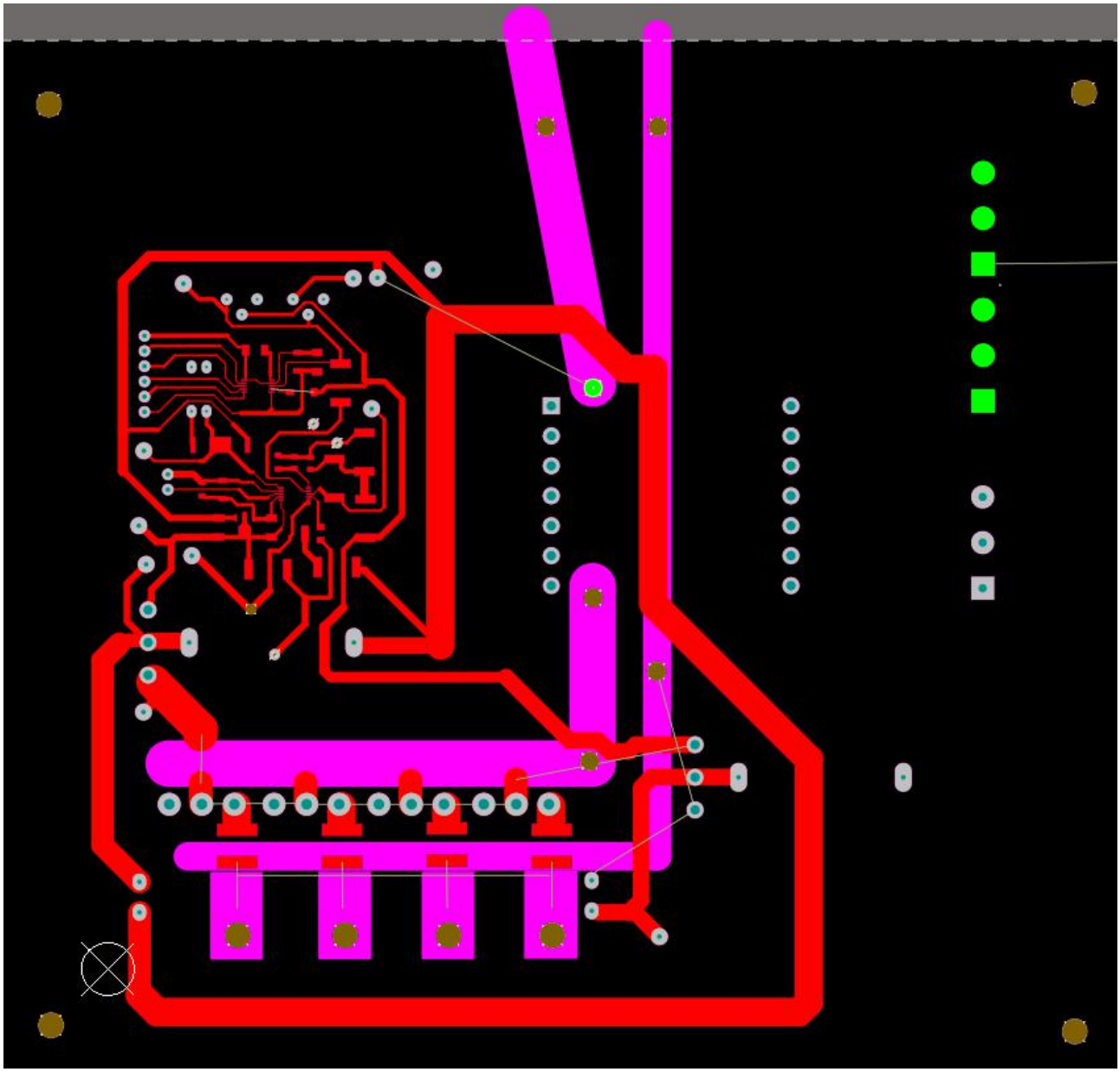

Figure 9: Top layer of PCB design

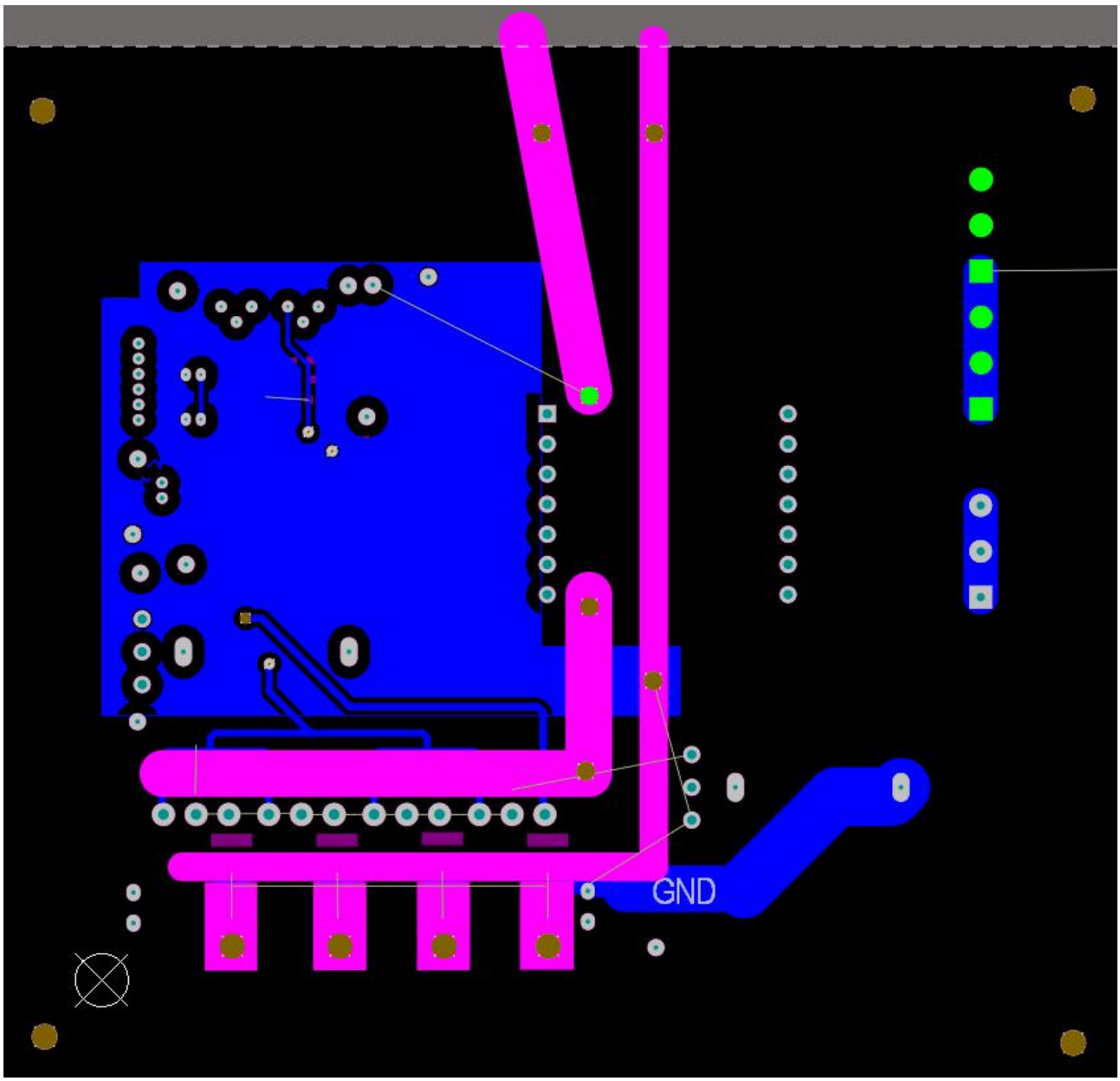

Figure 10: Bottom Layer of the PCB design