Master's Thesis

III-V Nanowire MOSFETs for mm-Wave Switch Applications

by

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Abstract

RF-switches are key components in many electronic devices as they enable routing of higher frequency signals. Increasing demands on device performance requires new technologies as well as new approaches to designs of circuits.

III-V nanowire MOSFETs are a promising device technology well suited for implementation of switches. This work investigates the design trade-off's for III-V nanowire MOSFET technology for mm-wave switch circuits. In the thesis, simulation results for three different switch designs are compared. These are a standard single-pole double throw, with one respectively two resonant pairs, and a switch that uses high internal impedance to improve the isolation.

The results show figures of merits that are comparable to state-of-the-art designs and indicates the need for further work in this area as to validate the simulations with measurements on processed devices.

Populärvetenskaplig sammanfattning

Dagen samhälle blir allt mer digitaliserat, såväl inom industri som vanliga hushåll. Som en del av detta växer även behovet av snabb och energisnål elektronik som utan fördröjning kan kommunicera med varandra, så kallat Internet of Things (IoT). Detta medför enorma effektiviseringsmöjligheter för industri såväl som hushåll men även för infrastruktur då det leder till självkörande bilar och så vidare. För att detta ska fungera så måste signaler kunna skickas mellan enheter utan fördröjningar och med en stabil sammankoppling. Aktuellt idag är 5G som just skickar enorma mängder data med mycket låg fördröjning. Det som möjliggör detta är att 5G använder frekvenser som är högre än tidigare.

I motsats till den digital elektroniken i exempelvis en dator använder analoga applikationer en oscillerande signal. Förenklat kan det förklaras med att signalen ligger inom ett frekvensband och ju högre detta band ligger i frekvens, desto mer information kan skickas. En viktig del i att hantera dessa analoga signaler är möjligheten till att kunna välja hur den ska hanteras. Till exempel kan en signal som fångas upp av en antenn behöva förstärkas medan nästa signal behöver filtreras. För att lösa detta kan en Radio-Frekvens omkopplare användas.

I detta arbete har omkopplare designats och simulerats med nanotrådsbaserade transistorer som, på grund av sin geometriska form, har mycket goda elektrostatiska egenskaper. Med detta menas att de är mycket effektiva i att leda respektive blockera signalvägar. Traditionella planära transistorer kan påverka ledningsförmågan i kanalen från en sida medan för nanotrådstransistorns kanal utgörs av den smala nanotråden vilket ger möjligheten att påverka kanalen från alla håll. Dessa trådar utgörs även av indium-gallium-arsenid, ett material som möjliggör högre rörlighet hos elektroner, vilket leder till mindre förluster.

Utöver en standarddesign så har ytterligare två applikationsspecifika designer tagits fram, vars fokus varit bandbredd respektive isoleringsförmåga.

Resultatet av arbetet visar att omkopplare designade med nanotrådstransistorn kan mäta sig med moderna lösningar på högsta tekniska nivå genom små förluster, bra bandbredd och bra isoleringsförmåga.

Acknowledgements

I remember, sitting in the large lecture hall in building E during my first year of study, as the professor recommended us electronic engineering students to take a course in quantum physics. It sounded strange at that time, but it started me of on a path which has led to this work.

First, I would like to take the opportunity to thank my supervisor Lars Ohlsson Fhager for your explanations regarding circuitry, structuring and the always useful feedback. Additionally, a great thanks to my assistant supervisor Stefan Andric for all your support given during these last months and for always talking time and answering my questions. Even though it is not included in the report, the practical tutoring in the lab by my assistant supervisor Adam Jönsson has benefited me greatly by connecting theory with practical work.

Finally, I would like to express my gratitude to Carolin, for your never ending support and the believe you have in me.

Contents

1

Introduction

An increase of information and data transfer is putting higher demands on the performance of electronic devices. They need to be smaller, more power-efficient and able to handle ever increasing amounts of data. In analog applications more data means moving up in frequency, into the mm-Wave spectrum and beyond.

1.1 Background

The RF-switch is a key building block in wireless communication systems, radar systems, and integrated control electronics for quantum computers. When benchmarking the operation of the RF-switch one usually looks for a low ON resistance and a low leakage current in the OFF-state of the transistor. Nanowire transistors are shown to have very good electrostatic properties with very low ON resistance giving them a high dynamic range. This also enables nanowire transistors to have good scalability.

Today's electronics are dominated by devices made from silicon (Si). But in order to meet the future demands on electronics the introduction of high mobility compounds such as indium-gallium-arsenide (InGaAs), commonly called III-V due to their position in the periodic table, is needed. In essence, the material enables better performance than Si but at a cost. They are much rarer and more expensive than Si. It would therefore be desirable to decrease the amount of material used by integrating III-V on top of a Si substrate, but this results in material defects due to lattice mismatch between III-V and Si. The geometry of nanowires has shown good results in containing defects close to the substrate interface when the III-V nanowires are growing on a silicon substrate.

These performance potentials in millimeter wave circuit application, with a focus on RF-switches, can make nanowires RF devices a competitive alternative to existing devices.

1.2 Aim and Scope

This project investigated the design trade-offs in III-V nanowire MOSFET technology for mm-wave circuit design. The main objective was to identify and benchmark critical performance metrics in basic circuit topologies, with a focus on device design and size selection.

The work was started with literature studies of state-of-the-art switch designs and nanowire MOSFET devices. Circuit simulation workspaces were set up in *Keysight ADS* to create designs with the goal of increasing performance metrics relative standard switch design.

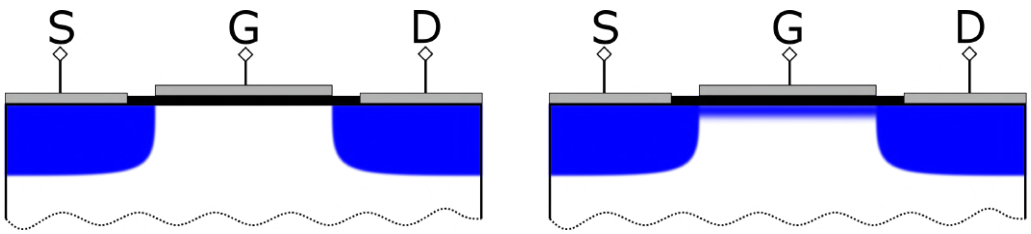
Work connected to this thesis have been cleanroom and processing training as well as participation in the development of related process technologies, such as coplanar waveguide circuits implemented with vertical nanowire MOSFETs. The process technology development will not be included in the scope of the thesis, partly because it is not finished and partly due to the need to keep the thesis outline focused and of reasonable length.

2

Theory

2.1 Metal–Oxide–Semiconductor Field-Effect Transistor

The metal–oxide–semiconductor field-effect transistor (MOSFET) is the key component in modern electronics. The name gives an idea of the basic physics behind the operation of these devices. In short, the basis consists of a semiconductor substrate, originally silicon (Si) with doped contact regions called source and drain. Between these regions is the gated channel region where a metal electrode is placed on top of an isolating oxide. Depending on the type of transistor and the direct current (DC) bias, electrons or holes, called charge carriers, will pass from source to drain. The channel has few free charge carriers but by applying a potential at the gate, free carriers will be attracted to the channel and thus enabling a transport current. The differential voltage over the source and drain contacts creates an electrical field that accelerates the carriers thus creating a current of charges. Figure 2.1 shows a cross section of an electron carrier MOSFET, n-MOS, biased to operate in cutoff and linear mode.



(a) *Cutoff mode* ***(b)*** *Linear mode*

Figure 2.1: *Basic planar n-MOSFET. The drain, D, and source, S, contact regions contain free electrons indicated by blue and the gate is isolated from the substrate by an oxide. When no potential is applied to the gate, G, the transistors is biased in cutoff mode (a). A positive potential applied on the gate creates an electric field in the substrate that attract electrons to form a channel (b).*

2.1.1 Metrics of the MOSFET

The drain current is given by the amount of charges and the velocity of which they pass through the channel. For n-MOS with a positive gate voltage, V_{GS}, that is larger than the threshold voltage, V_T, results in a large current. For the linear operation region, see Figure 2.2b, the drain voltage, V_{DS}, is small and the change of potential in the channel region between the drain and the source can be approximated as linear. The electric field in the channel can then be approximated as V_{GS}. For this linear region the drain current is given by

$$I_D = \frac{W}{L} \cdot C_g \mu_n \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{2.1}$$

where W and L is the channel width and the channel length respectively and μ_n the effective mobility of the carrier charge. C_g is the gate capacitance which consists of the oxide capacitance, C_{ox}, the quantum capacitance, C_q, and the charge centroid capacitance, C_C in series. In (2.1) the last term ($\frac{V_{DS}^2}{2}$) is included to modulate the non-linear behavior when V_{DS} approaches $V_{GS} - V_T$, that is the limit of the linear region. The effective mobility is material related and it is defined as $\mu_n = q\tau/m_n$, where q is the electron charge, τ is the mean free time between carrier collisions inside the structure and m_n is the effective electron mass. But when the current moves in to the saturated region, see Figure 2.2b, and the channel length is small the electric field becomes strong and the velocity of the carriers will start to saturate [1, 2]. The saturation current will then be given by

$$I_D = W C_{ox} \upsilon_{sat} (V_{GS} - V_T) \tag{2.2}$$

where υ_{sat} is the saturation velocity of the carriers.

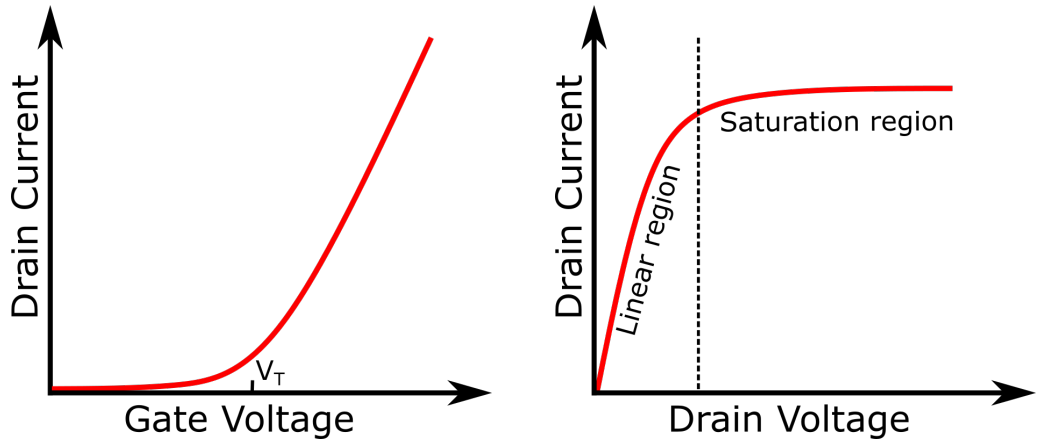
But with a short channel length it is important to note that, if the length is much shorter than the mean free path, λ_0, then there will be some ballistic transport which change the expression for the current. In a fully ballistic transistor the current is independent of the mobility inside the material and the current can be expressed as

$$I_{D,ballistic} \approx W C_{ox} \upsilon_{inj} (V_{GS} - V_T) \tag{2.3}$$

The difference between long devices and short is that the mobility is replaced by injection velocity, υ_{inj}, and that there is no gate length dependence for the ballistic devices [1]. However, real devices always have scattering and an ideal ballistic transistor is hard to realize. Thus leading to that short gate lengths and high mobility increases the likeliness of ballistic transport as seen in equation 2.4, where the ballistic transmission, T, is defined by the gate length and the mean free path, which in turn is defined by the mobility of the carriers [3].

$$T = \frac{\lambda_0}{\lambda_0 + L_G} \tag{2.4}$$

So the drain current in quasi-ballistic devices can be approximated with $I_D = T \cdot I_{D,ballistic}$.



(a) Transfer Characteristics *(b) Output Characteristics*

Figure 2.2: *The characteristics of ideal long channel n-MOS. The threshold voltage can be approximated by extrapolating the drain current in (a) as can be seen in (2.2) and (2.3). In (b) the operating regions, linear and saturation, are shown.*

Another important metric regarding transistors is the transconductance, g_m. This represents the change of I_D with regard to the change in V_G, and can be expressed as

$$g_m = \left.\frac{\delta I_D}{\delta V_{GS}}\right|_{V_{DS}=constant}. \tag{2.5}$$

At high bias the potential at the drain contact will effect the electric field inside the channel region. For long channel devices this introduces channel length modulation while for ballistic devices it leads to a lowering of the gate barrier, so called drain induced barrier lowering, DIBL. In both cases this results in V_{DS} effecting the current levels even when the transistor is operating in saturation. This is denoted the *output conductance* (g_d) and is expressed as

$$g_d = \left.\frac{\delta I_D}{\delta V_{DS}}\right|_{V_{GS}=constant}. \tag{2.6}$$

However, in circuit design it is more common to use the *output resistance* $r_o = 1/g_d$. The product of the transconductance and the output resistance gives the intrinsic gain of that transistor and is an important metric in amplifier design [4]. How much the electrical field effects the channel is expressed by the geometry and expressed by the natural length, λ_n. DIBL in cutoff mode results in a parallel shift of the sub-threshold current which in turn will lead to a V_T shift, making it a good parameter for the electrostatic performance of a device. Thus a low DIBL means good electrostatic control [2].

As V_G approaches V_T the current starts to increase. How fast the transistor turns on is defined by the sub-threshold swing, SS, and it represents the change in I_D as a function of V_{GS} below the threshold voltage. The carriers in the conduction band of semiconductors follow the Fermi-Dirac distribution, this results in a theoretical minimum for MOSFETs which is 60 mV/decade at room temperature. Meaning, it takes 60 mV on the gate to increase I_D a decade. As this metric is correlated to V_T it also effects demands for biasing voltage, which means that a low SS leads to decreased power consumption. It also effects g_m as can be see in equation 2.5.

2.1.2 Transistors in Radio-Frequency Operations

In analog applications the large signal currents, $i_D = I_D + i_d$, where I_D is constant biasing current and i_d a sometimes small signal current. The biasing sets an operation point in 2.2b on which the a frequency signal creates small variations. These notations are given in the time domain and the Laplace/Fourier equivalent for the signal current is I_d. These RF signals are usually defined to the GHz regime. The wavelength is defined as

$$\lambda = \frac{v_g}{f} \tag{2.7}$$

where $v_g = c/\sqrt{\epsilon_{eff}}$ in which ϵ_{eff} is the effective relative permittivity of the propagating mode and c is the speed of light in vacuum. So as an example the wavelength for 28 GHz, used in 5G, in air is around 10.7 mm. This can be compared to when the signal is transferred in a coplanar wave guide, see Section 2.2.3, on top of SiO_2. In this case, the relative permittivity of the dielectric is 3.9 the resulting wavelength is approximately 6.8 mm.

As the impedance, Z, of reactive elements is frequency dependent there is a need for modeling transistors in a way that includes these parasitics effects. These models can range from basic to extremely elaborate and detailed, depending on the needs. The *small-signal model* includes the parasitics and it is a powerful tool when analyzing transistors. A schematic for a RF small signal equivalent circuit is shown in Figure 2.3. In the model the resistances R_g, R_s and R_d are the extrinsic elements and consists of resistive paths seen for each contact. R_s and R_d derive from the access resistance between the metal and the semiconductor and the resistance in the semiconductor in the path to the channel. The resistance in the channel is usually smaller than R_d and R_s, especially in quasi-ballistic devices. If the channel resistance is in fact much smaller than the access resistances and $V_{GS} \gg V_T$ the total resistance can be approximated as

$$R_{ON} = \left.\frac{1}{g_d}\right|_{V_{DS}=0, V_{GS}\gg V_T} \approx R_S + R_D. \tag{2.8}$$

The capacitive elements originates from the difference in potential between different regions. The capacitance for overlapping regions is given by

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \tag{2.9}$$

where ϵ_r is the relative permittivity of the medium, ϵ_0 is the permittivity in free space, A the overlapping area and d the distance between them[5]. Thus, it is dependent on geometry, ratio between the overlap area and the distance between as well as the permittivity of the material in which the electric field propagates. There are also contributions from fringing effect, but these are generally small compared to the those from overlap [6].

The impedance of a capacitive element is given by $Z_C = \frac{1}{j\omega C}$, where ω is the angular frequency, shows a linear scaling with the frequency. The effect of these elements on the transistor therefore increases in high frequency [5]. At some frequencies the current gain and the unilateral power gain will reach unity and they are denoted as the transition frequency, f_T, and the maximum oscillation frequency,

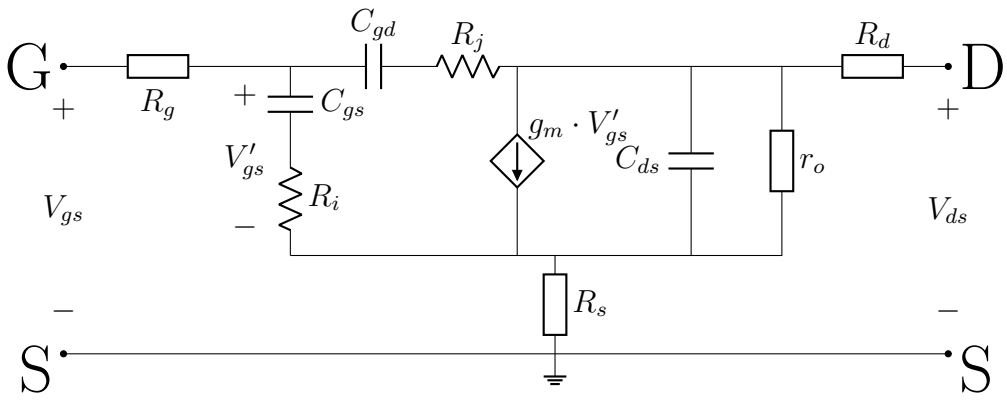


Figure 2.3: *Small signal equivalent circuit for a RF transistor. The geometry of the device effects the parameter sizes. A well designed transistor has small capacitances and resistances while the maximizing the intrinsic gain, $g_m \cdot r_o$.*

f_{max} respectively. They are approximated as

$$f_T \approx \frac{1}{2\pi}\left(\frac{C_{gs}+C_{gd}}{g_m} + C_{gd}(R_S+R_D)\right)^{-1} \tag{2.10}$$

and assuming $g_d = 0$

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi(R_g C_{gd})}}. \tag{2.11}$$

If R_{ON} is small then 2.10 can be simplified as

$$f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{2.12}$$

which clearly show the importance of a high transconductance and small capacitive elements [7]. These metrics are also very useful because they can set the performance limit of the device.

The limit frequencies, f_T and f_{max}, of a device are also easy to measure by utilizing scattering, S, parameter measurements. S-parameters for a two-port system uses the reflected and transmitted power to create a 2x2 scattering matrix. By looking at Figure 2.4 it can be seen that total voltage and current in each port is the superposition of the input and the reflection. Definitions of the incident, a, and reflected, b, power wave amplitude can be

$$P^+ = \frac{|V^+|^2}{2Z_0} = |a|^2 \Rightarrow a = \frac{V^+}{\sqrt{2Z_0}} \tag{2.13}$$

$$P^- = \frac{|V^-|^2}{2Z_0} = |b|^2 \Rightarrow b = \frac{V^-}{\sqrt{2Z_0}} \tag{2.14}$$

if Z_0 is the characteristic impedance of 50Ω. The reflection coefficient at each port is then given by $\Gamma = b/a = V^-/V^+$. From this the S-matrix can be created as

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \qquad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0}$$

By converting S-parameters to admittance and hybrid-π parameters it is then possible to derive f_T, f_{max}, but also the components of the small signal model as has been shown in [8].

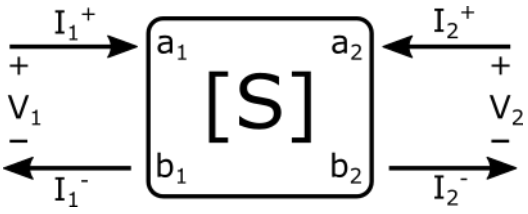


Figure 2.4: *Scattering parameters for a two port system. A power input is sent at each port separately and then the power of each signal is measured by each port thus giving the reflected and transmitted power in a 2 x 2 matrix.*

2.1.3 Silicon and III-V Materials

Si is a cheap material that is easy to work with and has a high quality native oxide, SiO_2, which can be thermally grown. This has resulted in Si being the main semiconducting material used in industries. As mentioned in the section 2.1.1 the mobility has an effect on the drain current, see equation 2.2 for long channel devices, but also for semi-ballistic short channel devices due to the mean free path and mobility correlation. Being able to push more current through a device will also have a positive affect on the transconductance. The mobility itself is correlated to the material and the bandgap of that material. It is possible to improve mobility by, for example, introducing strain in the lattices of the material [9], but a more effective approach is to change material from Si to III-V compound semiconductors, see table 2.1. Material containing arsenic (As) and antimon (Sb) have smaller bandgap and greatly increase the mobility of electrons and holes respectively [10]. This work will focus on electron transport MOSFETs (n-MOS) and compounds commonly used for these are InAs, InGaAs and GaAs and they have electron mobility as high as 10 times that of Si [11].

The arguments against using high mobility compounds instead of Si are the relative low density of states and that they are much more expensive. This can be solved to some degree by using silicon as the main substrate with structures consisting of III-V compounds. Alternatively one can grow a thin layer of III-V on the Si. However by having III-V on Si one will have to consider the lattice mismatch. The mismatch between Si and InAs is 11.6% and it will lead to unwanted strain and lattice dislocation in the structure and thus risks decreasing the performance of the device. The dislocations tend to propagate diagonally through the structure. This fact has given rise to several methods of solving this problem, such as optimizing growth of the III-V layer [12], shallow trench isolation [13] and vertical nanowires. The latter is the method used in this work.

Table 2.1: *Part of the periodic table*

III	IV	V
B	C	N
Al	Si	P
Ga	Ge	As
In	Sn	Sb

2.1.4 Vertical III-V Nanowire MOSFETs

There are different ways of growing nanowires, NW, on silicon. In this work only one will be addressed, namely growing them using seed particles. The wire growth for this work was done by utilizing metal-organic vapor-phase epitaxy (MOVPE) to create a thin layer of a n-doped InAs on a p-doped silicon substrate. Gold particles are defined by electron beam lithography (EBL) and act as catalytic seeds for another MOVPE which grows the wire on the InAs surface [14].

The vertical nanowire transistor consists of thin wires that protrudes vertically from the substrate surface. These wires consist of III-V compositions that may vary along the length of the wire. As discussed in Section 2.1.3, the defect that comes from lattice mismatch when growing different material and compounds on each other, usually self-terminate along the bottom of the wire. This fact makes NW a good candidate when it comes to implementing III-V's on silicon. Most common for the NW transistor is to have the source contact at the substrate surface, the drain at the top and the gate in between. A simple illustration is shown in Figure 2.5.

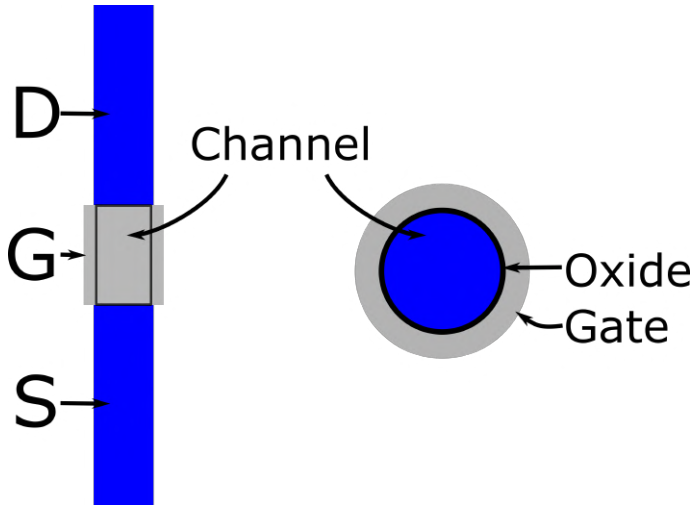


Figure 2.5: *Basics of the NW MOSFET. Showing a vertical nanowire with source, drain and gate. To the right is a cross-section of the channel region.*

As NW transistors have a gate all around, GAA, the electrostatic control of these devices are improved significantly compared to planar devices. This enables more aggressive gate length scaling of devices, which in turn will enable a higher performance and increase the ballistic transmission, as stated in equation 2.4. The drain and source contacts will still effect the potential in the channel region, but not at the same degree as planar or 2-D devices. This means that λ_n is shorter for GAA. Equation 2.15 states an approximate expression for λ_n for a cylindrical device such as the NW. Here ϵ_s and ϵ_{ox} is the relative permeability of semiconductor and of the

oxide respectively, r_{nw} the radius of the NW and t_{ox} the thickness of the oxide[3, 15]. This equation holds for when the oxide thickness and the radius are of similar size, which is the case in this work.

$$\lambda_n = \sqrt{\frac{2\epsilon_s r_{nw} \ln(1 + \frac{t_{ox}}{r_{nw}}) + \epsilon_{ox} r_{nw}^2}{4\epsilon_{ox}}} \tag{2.15}$$

It has also been confirmed in [15] through numerical simulations that, in order to prevent short channel effects such as DIBL the gate length must be larger than five times the natural length. As can be seen the thickness of the wire, the oxide and the channel length must all be scaled in order to scale down the device size.

As previously mentioned the GAA geometry of NW transistors enables for aggressive scaling while maintaining good electrostatic control. This in combination quasi-ballistic current and a low leakage current gives NW transistors a good dynamic range regarding current and good transconductance, as has been shown in [16] with $g_m > 3mS/\mu m$.

However, the scaling of the wire leads to a smaller access interface for the contacts, which in turn could lead to an increase in access resistance and subsequently R_{ON}. As resistances introduce thermal noise and gives a power loss, the desire is to have as low R_{ON} as possible. For NW transistors it has been shown that the access resistance in the source and especially the drain account for the majority of the actual R_{ON} [16, 17]. A difference between the drain-access resistance and source-access resistance is that one is connected to the substrate and the other has a metal contact. But due to the vertical structure it is possible to increase the length of the drain region without increasing the area used on the substrate and it has been shown to be possible to have a good resistance matching as well as low R_{ON} at 190 $\Omega\mu m$ [16].

2.2 Circuits in Radio-Frequency Operations

The impedance of a circuit is defined as $Z = R + jX$, where R is the resistance and X the reactance. When designing circuits for RF operation the frequency dependence of reactive components, such as capacitors and inductors, will lead to them contributing more to the impedance as the frequency is increased. A way to solve this is to use resonant circuits which will be discussed later.

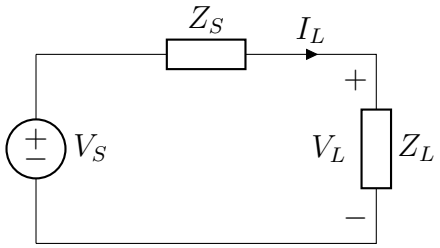


Figure 2.6: *The maximum power transfer from source to load is achieved when $Z_L = Z_S^*$.*

Using peak value a input power, P_S, the power transferred to the load, P_L, is

given by

$$P_L = \frac{V_L I_L}{2} = \frac{V_S^2}{2}\frac{R_L}{|Z_S + Z_L|^2} \tag{2.16}$$

where V_L is the load voltage, I_L is the load current, Z_L the load impedance and Z_S the source impedance. To maximize the power transfer at the load $Z_L = Z_S^* => R_L + \mathrm{j}X_L = R_S - \mathrm{j}X_S$. If this is fulfilled then V_L and I_L will have the same phase and thus maximizing the power transfer from source to load. The available power from the signal generator is thereby

$$P_{av} = \frac{V_S^2}{8R_S} \tag{2.17}$$

and it generally requires a matching network to transfer the load [18].

2.2.1 Resonant Circuits

As mentioned, a circuit usually contains both resistive and reactive elements. As purely reactive elements do not dissipate energy it should be possible to eliminate the effects of these around a designed frequency. This is done by creating resonant pairs.

By analyzing the circuit in Figure 2.7 the equivalent admittance can be derived as

$$Y_p(\omega) = \frac{1}{Z_p(\omega)} = \frac{1}{R_p} + \mathrm{j}\underbrace{\left(\omega C_p - \frac{1}{\omega L_p}\right)}_{B} = \frac{1}{R_p}\left(1 + \mathrm{j}Q\left(\frac{\omega}{\omega_c} - \frac{\omega_c}{\omega}\right)\right) \tag{2.18}$$

where Q is the quality factor. By setting $B = 0$ and solving for ω the resonant frequency relates as

$$\omega_c = 2\pi f_c = \frac{1}{\sqrt{LC}}. \tag{2.19}$$

The relation to the circuit bandwidth in (2.18) is $BW = 1/(RC) = \omega_c/Q$. The same analysis can be done for RLC circuit in series, which will give the same expression for ω_c. By adding reactive elements to the paracitics it is possible to use these relations to create a resonant circuit that effectively cancels the reactive impedance close to the operating frequency.

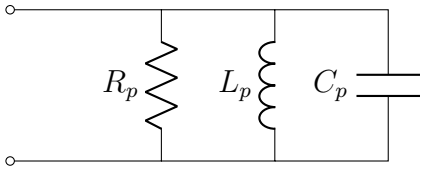


Figure 2.7: *A simple parallel resonant circuit.*

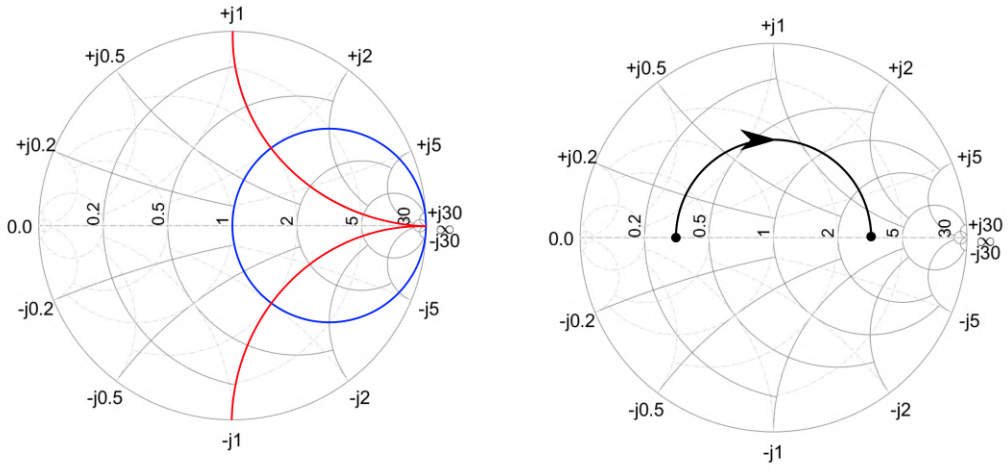
The quality factor, Q, of the circuit is defined as the ratio between the maximum stored energy, E_{tot}, and the energy dissipated per cycle, ΔE_{cycle}, which for practical circuit means, the ratio between size of reactive and resistive elements. General expression for the Q factor is

$$Q = 2\pi\left(\frac{E_{tot}}{|\Delta E_{cycle}|}\right) = \frac{\omega_c}{BW}. \tag{2.20}$$

This relation shows that with an increased BW there must be loss in form of power dissipation for a fixed system [5].

2.2.2 Smith Charts

The Smith Chart is a tool used in designing of RF circuits. It maps the rectangular coordinated for the reflection coefficient, Γ, and the normalized impedance, $z = Z/Z_0$. Conventionally, the impedance is normalized with 50Ω, but this can differ depending on design factors and needs. The Smith Chart consists of constant resistance circles and constant reactance lines as shown in Figure 2.8a. The working principle is that adding a resistive element will change the impedance along the constant reactive line while reactive elements will have a change along the constant resistive circle.



(a) *(b)*

Figure 2.8: *The impedance Smith Chart. In (a) the constant resistance circle for '1' is marked by blue and the constant reactance line by red. A lossless phase shift of π is shown in (b). This corresponds to a $\lambda/4$ transmission line.*

An ideal transmission line, without attenuation and disregarding possible parasitic reactances, will still have a phase shift that is dependent of the travel distance of the signal [18]. This will result in a clockwise rotation in the Smith Chart that is centered at the characteristic impedance of the transmission line. This ideal case is shown in Figure 2.8b for a phase shift of π radians, which translates to a quarter of the wavelength, $\lambda/4$. In reality there will be some attenuation in the line that will result in a shortening of the radius, making the circle spiral towards the origin. However, these are generally small and a lossless TL can in many cases be a valid approximation, which simplifies the expression for the input impedance to

$$Z_0 = \sqrt{R_S R_L} \tag{2.21}$$

for the $\lambda/4$ TL, where R_S is the source resistance and R_L the load resistance. This expression is commonly used for impedance matching and can be generalized for matching between arbitrary impedances if the line length is used as a parameter [19].

2.2.3 Coplanar Waveguides

There are different methods for implementing planar transmission lines, TL, for integrated circuits. One such way is Coplanar Waveguide, CPW, that has ground planes on each side of the transmission line as can be seen in Figure 2.10. By having the ground plane close to, and level with, the TL the isolation of the signal is increased. Regarding processing it enables a possibility to simplify the processing by co-integrating front-end and back-end.

By having a thick dielectric substrate that is at least $h > (2S + W)$, the effects of the height will be negligible. And with $h \gg (2S + W)$ the approximation can be concluded that the dielectric is of infinite dimensions due to the field penetration to the bottom being very small. This results in that the line impedance being only dependent on the ration $W/2/S + W/2$. Also, the effective permittivity can in this case be approximated to

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} \tag{2.22}$$

where ϵ_r is the relative permittivity of the substrate. In order for the CPW to work well the ground plane, which is divided by the TL, must have a uniform potential [18]. Therefore, the ground plane must regularly be coupled. One way of doing this is to connect the ground planes with a bridge-structure that goes under or over the transmission line.

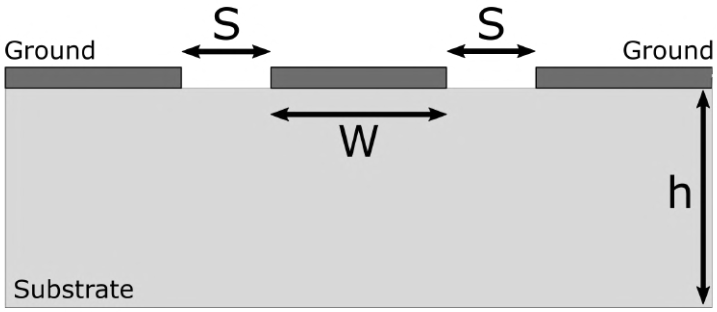


Figure 2.9

Figure 2.10: *Coplanar waveguide. Shows a schematic cross-section of a coplanar line.*

The downside of CPW is that it has a larger area footprint due to the ground plane and TL being on the same layer. CPW are therefore mostly used for high frequency applications.

3

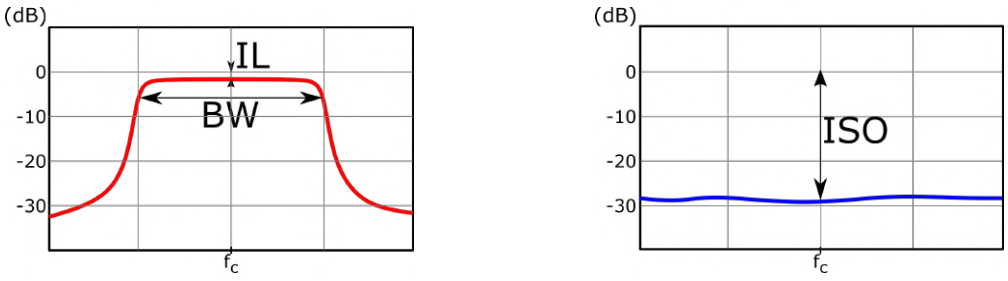
Method

This work consisted of the design and simulations of three single-pole double throw, SPDT, RF switches. The designs are denoted as (A) for the standard SPDT circuit, (B) for the second order SPDT switch and (C) for the high internal impedance circuit, HZ SPDT.

For simulating the circuits *Keysight Advanced Design System*, ADS, was used together with component definitions developed by the Nanoelectronics group, see Section 3.1.

To start designing a circuit, the device performance of different transistor sizes were evaluated by simulating transfer and output characteristics to derive $R_{ON,OFF}$ and then using (2.6). S-parameter simulations were used in determining C_{OFF} and C_{ON} at f_c by connecting a 50Ω port to the drain and a voltage source to the gate of the transistors. The resulting capacitances were then used to get starting approximations for the indutances needed to creating the resonating pairs. This will be explained later in more detail.

Figure 3.2 shows A, the standard SPDT. It will be explained in more detailed later, but as can be seen the switch has two outputs. These are in either ON or OFF state. The ability of the switch to isolate the signal in OFF state, ISO, and how large the insertion loss, IL, at the output branch that is in ON state, are used for benchmarking. The merits originate from the S-parameter forward transmission for both and are defined as IL $= 1/S_{21,ON}$ and ISO $= 1/S_{21,OFF}$, see Figure 3.1.



(a) *(b)*

Figure 3.1: *(a) show the forward transmission of the ON branch ($S_{21,ON}$) with notations for related key metrics. (b) show the ISO which is related to the forward transmission of the OFF branch ($S_{21,OFF}$).*

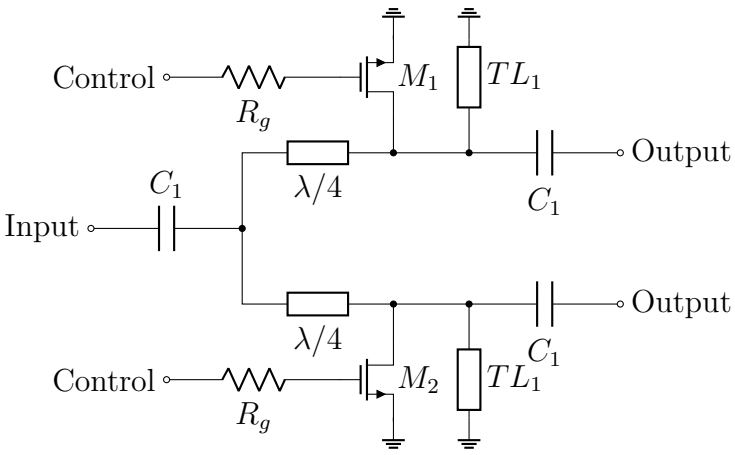


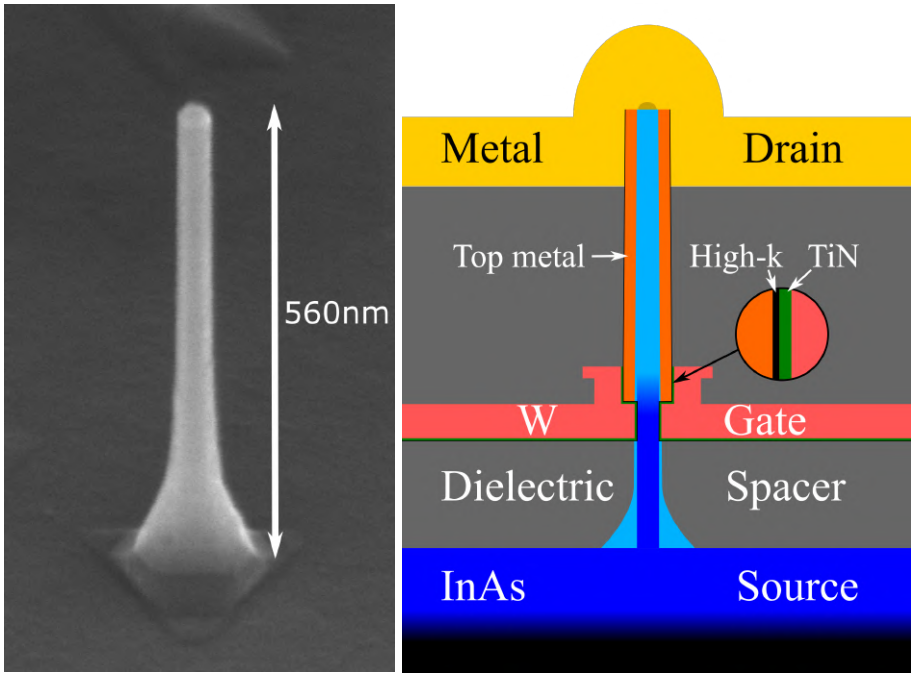
Figure 3.2: *Schematic of A, the standard SPDT. The transformers, which are the $\lambda/4$-lines have impedance of 50Ω while the stubs, TL_1, have 75Ω. Capacitances are added to the input and output as to block DC signals. The details of the circuit will be discussed in Section 3.2.*

3.1 Circuit Technology

In this work the III-V vertical nanowire transistors on top of a silicon substrate developed by the Nanoelectronics group at Lund University were used.

Work on processing NW MOSFET's have been conducted under Adam Jönsson (Nanoelectronics group) parallel to this work. This has, as mentioned, been excluded from this thesis partly out of a need to confine, but also because that work is not finished at the time of writing. However, an overview description of the processing flow will here be described. First, the wires are grown on a highly doped InAs on top of a Si substrate using seed particles. A scanning electron microscope (SEM) picture of a wire is shown in Figure 3.3a. Then a sacrificial HSQ layer is defined using electron beam lithography (EBL), on which the top metal is sputtered. An anisotropic dry etch then removes the metal from the surface of the HSQ, which is in turn removed. Then a bottom HSQ spacer is added and the thickness decides the gate length, in this work 50nm. The exposed wire intended as the gated region, is thinned with digital etching to a diameter of 28nm. A high-k dielectric is then deposited using atomic layer deposition (ALD). The gate metal stack is added, consisting of TiN and W. Lastly a top spacer and drain contact is added. A general cross-section of the device is shown in Figure 3.3b.

In order to reduce the number of layers needed on the chip CPW was used instead of microstrip. A model for CPW TL was created in ADS and other essential structures such as bridges, resistors and capacitors were provided by Stefan Andric (Nanoelectronics Group). The passive structures were in this work placed on the Si substrate, after a removal of the thin InAs layer, and the top metal layer was used for TL and contacts.



(a) *(b)*

Figure 3.3: *Nanowire MOSFET. A SEM picture of a grown InGaAs NW is shown in (a) and a complete gate-last layer cross-section of a NW MOSFET is shown in (b). The NW transistors in this work has a diameter of 28nm and a gate length of 50nm.*

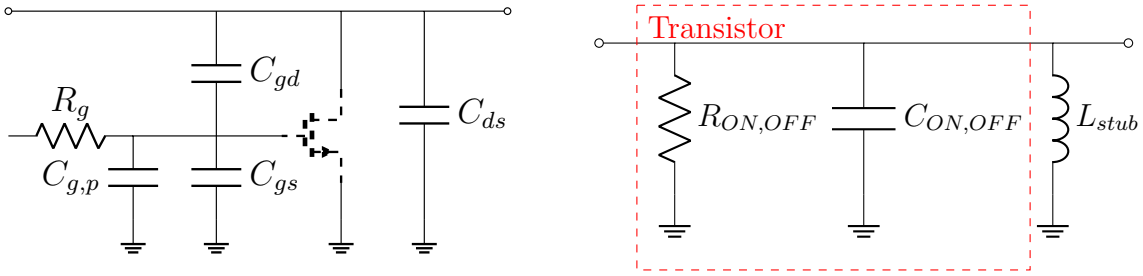
3.2 Circuit Design

As mentioned before, the standard SPDT switch consists of one input and two output branches as seen in Figure 3.2. Each branch has a $\lambda/4$-line and a transistor in shunt configuration which will have a control bias at the gate making it operate in cutoff, OFF, or the linear region, ON, due to the lack of drain biasing. As a control signal on the gate turns the transistor ON, the signal path in that branch will be shorted to ground. The $\lambda/4$-line then transforms the short from a low to a very high impedance. This reflects the input power and the branch will, ideally, have no output signal. Meaning that if the shunted transistor is ON the branch output is set OFF. If, on the other hand, the control signal set the transistor to OFF state the transistor will ideally act as an open circuit and the signal will go to the output, rendering the branch output to ON. A large R_{ON} in this case will result in the impedance to be that of the output the $\lambda/4$-line will transform the impedance around the characteristic impedance at the center of the smith chart. In the following text ON and OFF settings refers to the branch setting and not the transistor unless the contrary is stated.

The $\lambda/4$ TL was designing as a CPW TL of 50Ω and a 90 degree phase shift with *Controlled Impedance Line Designer* in ADS. However, R_{ON} in the transistor will add a small resistance to the short circuit, which will transform to a finite resistance in the open circuit.

In order to avoid low impedance termination and block out any additional reactive elements at the gate of the transistor, a large resistance (R_g) was needed at the gate, see Figure 3.4a. This enables the capacitive contribution to C_{ON} and C_{OFF} to consist of C_{gs} and C_{gd} in series, which will result in a capacitance lower than

C_{gs}. In the OFF state R_{OFF} limit the admittance of the transistor. But as the



(a) *(b)*

Figure 3.4: *The contributions to $C_{ON,OFF}$ is shown in (a). A large resistance R_g was added to the gate. In (b) a simplified model of a transistor in shunt configuration is shown with an added inductor to create a resonant pair with the transistor capacitance, $C_{ON,OFF}$.*

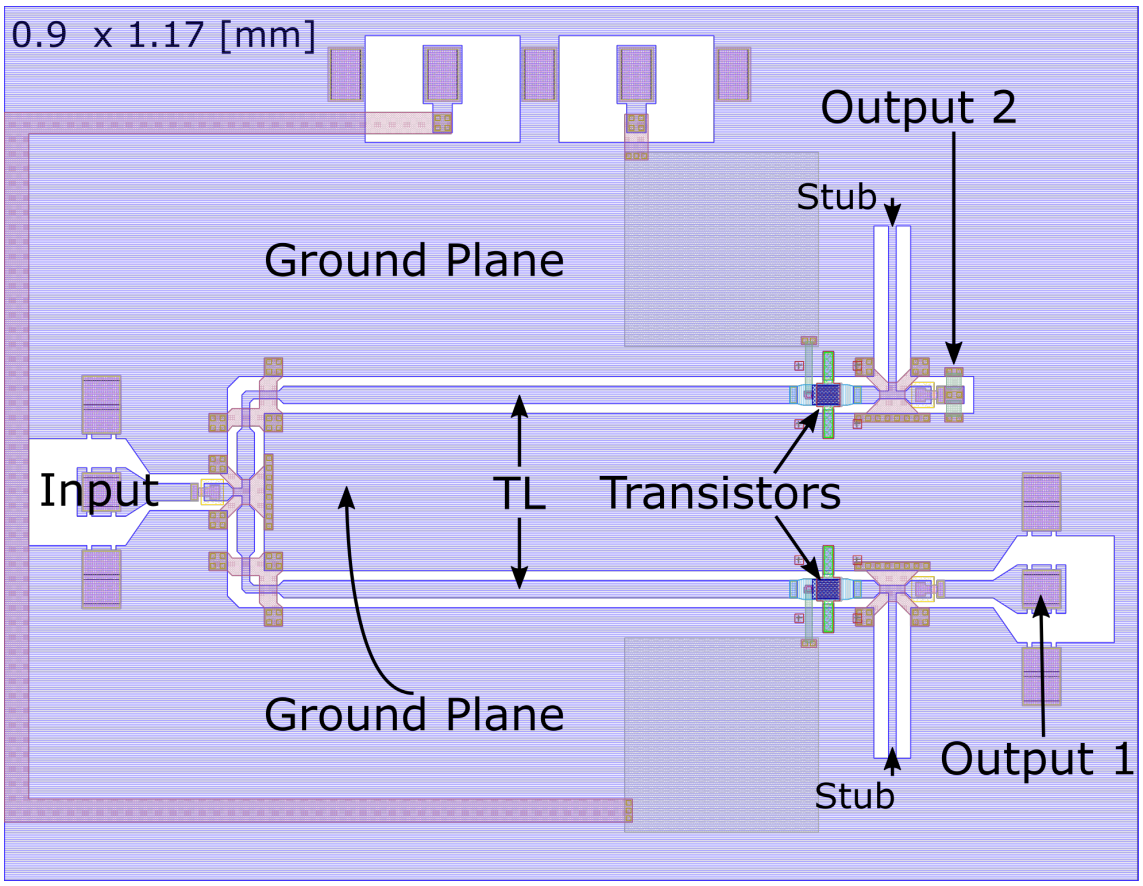


Figure 3.5: *The layout of SPDT switch A in CPW technology. The main components are marked. The input and output 1 have pads for measurement, while output 2 is terminated by a 50 Ω resistor.*

frequency increases so will also the admittance due to the product of frequency and C_{OFF}. This needs to be compensated by adding a parallel inductance, thus creating a resonating pair as shown in Figure 3.4b. By doing this the transistor admittance consist ideally of just the real part when operating close to the set center frequency,

f_c. The simplified model of a transistor in shunt configuration with a compensating inductance is shown in Figure 3.4b. The value of C_{OFF} was derived by doing S-parameter analysis of the transistor in ADS while $R_{ON,OFF}$ was derived through sweeping V_{DS}, as stated in (2.6).

The size of the inductance was derived by using (2.19) for resonating pairs. A shorted stub with a length $l < \lambda/4$ was then used to realize the inductance needed. The relation

$$l_{stub} = \frac{\lambda}{2\pi f L_{stub}} \approx \frac{\lambda}{2\pi} \arctan\left(\frac{\omega L_{stub}}{Z}\right) \tag{3.1}$$

gave a start length. As this do not include all elements ADS needed to be used to tune the response. Choosing a Z that is larger than 50Ω meant that l could be scaled down, while maintaining the same inductance. So for the stubs the line impedance was set to 75Ω by varying S and W according to Section 2.2.3. The schematic of SPDT A is shown in Figure 3.2 and Figure 3.5 shows the layout made by Stefan Andric.

3.2.1 Second Order SPDT

In SPDT B a second resonant pair was introduced. This was done in series and by utilizing the DC blocking capacitance and a TL as an inductor. The capacitance still also functions as a DC block, but it needed to be much smaller. Therefore, the notation was change to C_2, see Figure 3.7. Again (2.19) was used to determine the relation of the resonating pairs as

$$\omega_c = \frac{1}{\sqrt{L_1 C_{OFF}}} = \frac{1}{\sqrt{L_2 C_2}} \tag{3.2}$$

where $L_2 = L_1 \cdot s$ consisting of TL_2 and $C_2 = C_{OFF}/s$. By introducing the scaling factor, s, it was possible to move the poles while keeping the resonant frequency constant, thus increasing bandwidth. First of all $s \neq 0$. Secondly, having $s \neq 1$ will split the poles into conjugates pairs while keeping the same center frequency. The other circuit elements determine if s should be larger or smaller than 1 in order for this to happen. The effect of introducing a second resonating pair is shown in Figure 3.6.

Equation 3.1 also applies to the series resonating pair, even though the TL will be in the signal output path the added impedance will have a very small effect on the attenuation due to the shorter length of the line.

The schematic of SPDT B is shown in Figure 3.7 where the second resonating pair consists of TL_2 and C_2.

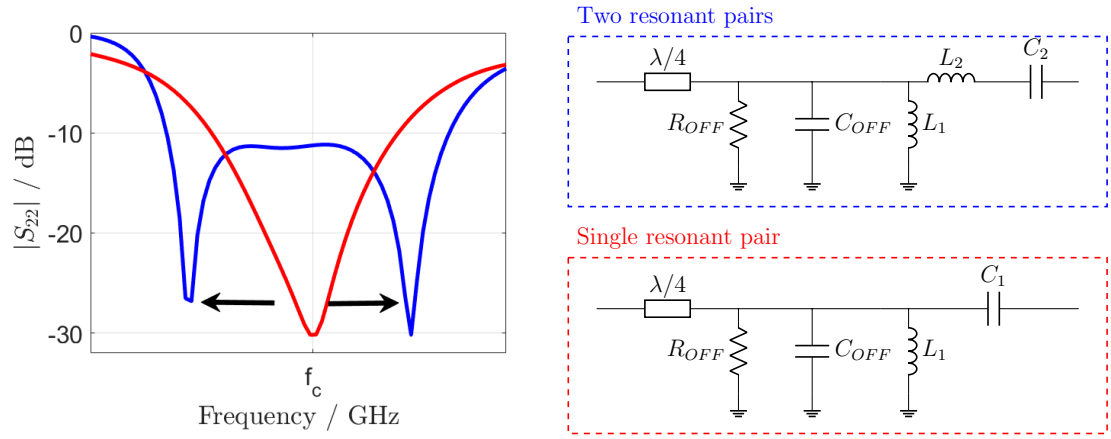


Figure 3.6: *ÄNDRAD FIGUR! An example of how the output reflection, S_{22}, changes when $s \neq 1$. The blue line shows the output reflection behavior of the system with two resonating pairs. These are C_{OFF}, L_1 and C_2, L_2. The simplified branch equivalent to this is marked by blue. The red line show the standard system with one resonating pair. The black arrows indicate that the reflection peak divides into two peaks and moves apart.*

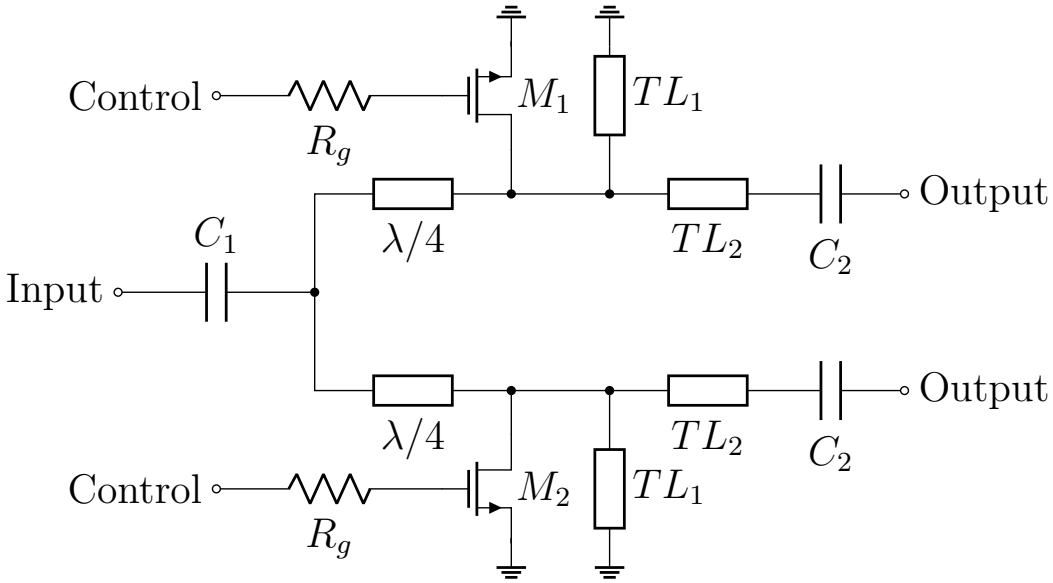


Figure 3.7: *Schematic of B, the second order SPDT. The second resonating pair consist of the inductance of TL_2 and C_2.*

3.2.2 HZ SPDT

The high internal impedance SPDT, named C, utilizes the work presented in [20]. Here the internal impedance is the impedance seen at the drain-nodes of the transistors, see Figure 3.8. By using the $\lambda/4$-transformers, here noted as Z_1, to transform the impedance at the internal node to a higher value it is possible to improve the ISO up to 10dB while the degradation of the IL is about 0.6dB. The internal impedance is given by $Z_{int} = Z_1^2/Z_0$, where Z_0 is the input impedance. In the standard switch implementation the R_{ON} has a small impedance that will transform into a large, but finite, impedance with the help of the $\lambda/4$-line. To improve the reflection in the OFF branch R_{ON} needs to be decreased, which is commonly done by increasing the

width of the transistor. This will degrade other figures of merit such as the bandwidth. But with the high impedance implementation the transformer will rotate around a point in the smith chart that is higher in resistance than the characteristic impedance and the transformed impedance will consequentially be larger, thus increasing the reflection and the ISO.

This behavior can be seen in the forward transmission, which can be approximated as

$$S_{21,ON}(R_{ON}, Z_{int}) \approx \frac{1 + \frac{R_{ON}}{Z_{int}}}{1 + \frac{3R_{ON}}{2Z_{int}}} \tag{3.3}$$

$$S_{21,OFF}(R_{ON}, Z_{int}) \approx \left(\frac{3}{2} + \frac{Z_{int}}{R_{ON}}\right)^{-1}. \tag{3.4}$$

From the dynamic ratio of the system,

$$D_{ON,OFF}(R_{ON}, Z_{int}) = \frac{S_{21,ON}}{S_{21,OFF}} \approx 1 + \frac{Z_{int}}{R_{ON}}, \tag{3.5}$$

it can be seen that the options for improving this is to have a smaller R_{ON} or increasing Z_{int}. To avoid a mismatch between the internal impedance and the output impedance a second $\lambda/4$ line is needed between the transistor and the output. This line will transform internal impedance back to Z_0, which here is the output impedance.

An increase of the internal impedance will at the same time decrease the bandwidth, creating a trade-off with the increased ISO. They are both also heavily dependent on the transistor size. A small transistor will have a smaller capacitance and a larger bandwidth, but at the same time a higher R_{ON}, than a larger transistor. In the end the application demand on the switch will determine what is most needed, keeping bandwidth or having a good ISO. In this work the focus lays in improving the ISO as much as possible while still having a comparable bandwidth to the other models, A and B.

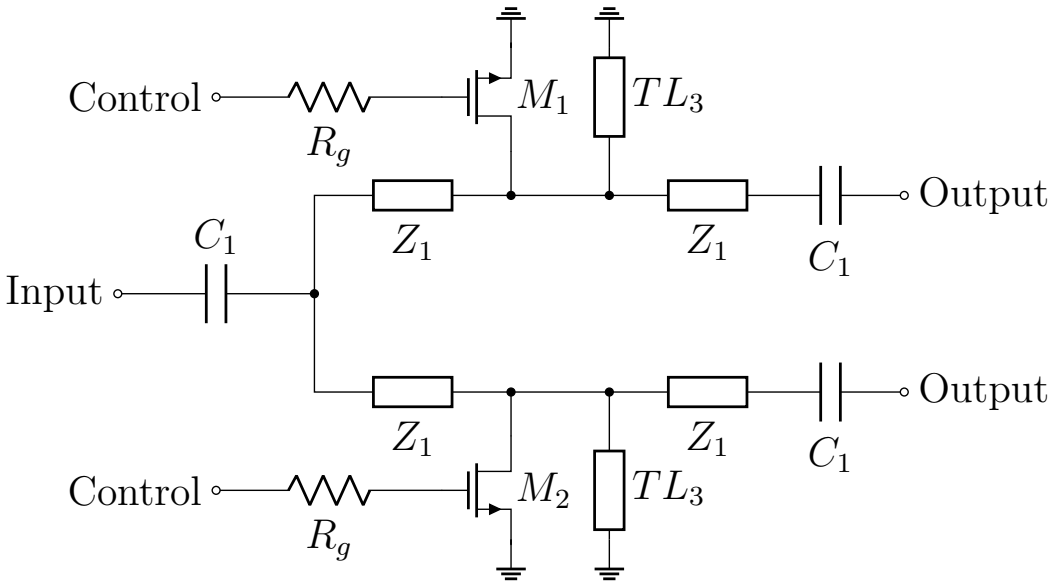


Figure 3.8: *Schematic of design C, a SPDT with higher internal impedance.*

3.3 Simulation setup

Chosen f_c in the design was 50 GHz which gave a $\lambda/4 = 670\mu$m. The dimensions of the $\lambda/4$ TL, 50Ω, and the stubs, 75Ω, are shown in table 3.1.

Table 3.1: *The TL dimensions for $\lambda/4$ TL, 50Ω, and the stubs, 75Ω.*

TL (Ω)	Width (μm)	Clearance (μm)
50	18	10
75	8	15

The simulations of the transistor characteristics show a normalized R_{ON} of 0.375 Ωμm and R_{OFF} of 3.1 kΩμm. Table 3.2 shows the resulting $R_{ON,OFF}$, C_{OFF} and calculated L_{stub} for transistors of 500, 1200, 1600 and 2000 NWs. The choice of transistor size was taken based on already available NW array sizes grown in the lab. Also shown in the table is the product of the transistor parameters $R_{ON} \cdot C_{OFF}$ which is a well-known figure of merit for switches. Both should be as low as possible to improve the performance of the switch.

Table 3.2: *The different transistor metrics and an approximation of the required stub inductance.*

Transistor (NW/NF)	R_{ON} (Ω)	R_{OFF} (kΩ)	C_{OFF} (fF)	$R_{ON} \cdot C_{OFF}$ (fs)	L_{stub} (nH)
500/5	8.5	70	27.4	165	0.37
1200/6	3.6	30	51.4	165	0.20
1600/8	2.7	22	64.7	165	0.16
2000/10	2.1	18	77.6	165	0.13

The methodology was to derive some approximate values for capacitances by S-parameter sweep simulation and inductances for the compensation based on theory. From these, simulation setups based on ideal components, inductors, were created in ADS to verify the approximations. These simulations consisted of S-parameters sweeps with one input port and two output ports. The frequency was swept from 1 GHz to 120 GHz with step size of 1 GHz. Then the inductors were replaced with CPW lines acting as stubs, or TL in the case of SPDT (B). At this point some tuning was needed to get the desired matching. This was done by tuning the variables shown in Figure 3.9 and observing the reflection and transmission changes, in order to match the output reflection to the characteristic impedance. The table also gave some figure of merits which will be discussed later. The simulations of the switch performance were set up in ADS. For details on the TEE structure and the lumped network on the transistor gates in Figure 3.9, see Appendix A.

As C_1 is a DC block it is kept at 1pF for all designs. To isolate the gate from possible parasitics and enabling the approximation that C_{gs} and C_{gd} is in series without additional contributions R_g needs to be large enough to be dominate that impedance. Therefore, it is also kept fixed at R_g =1kΩ for all designs. Remaining parameters are presented in table 3.3.

Table 3.3: *This table shows the sizes and dimensions of the components used. For references see Figures 3.2, 3.7 and 3.8.*

Transistor (NW/NF)	TL_1 length (μm)	TL_2 length (μm)	TL_2 impedance (Ω)	TL_3 length (μm)	Z_1 impedance (Ω)	Z_1 width (μm)	Z_1 clearance (μm)
500/5	330	360	75	310	60	12	10
1200/6	230	370	75	210	68	10	14
1600/8	170	260	75	155	68	10	14
2000/10	155	260	75	150	68	10	14

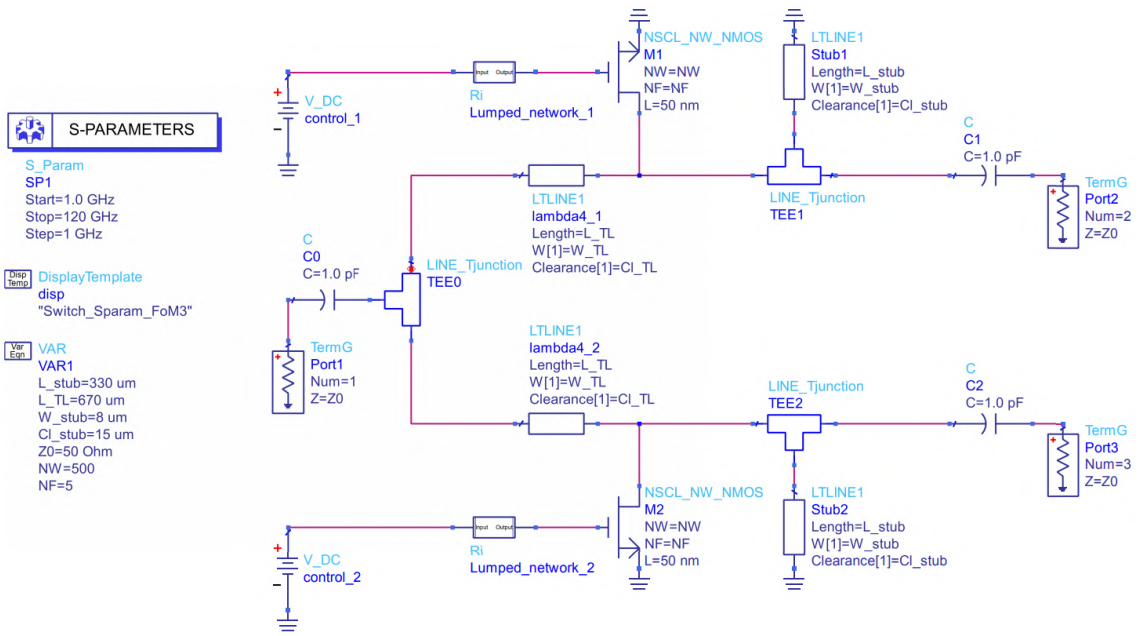


Figure 3.9

Figure 3.10: *The schematic setup of the standard SPDT in Keysight ADS. It shows the variables used and the simulation that was performed, S-parameter.*

4

Results

The resulting simulations from different device sizes in number of nanowires per transistors will here be presented based on the IL, ISO, f_c and the relative bandwidth, $\mathrm{BWr} = \mathrm{BW}/f_c$. These performance parameters are then compared in the *Figure of Merit*, which is defined as

$$FoM = \frac{f_c \cdot \mathrm{BWr} \cdot \mathrm{ISO}}{\mathrm{IL}}. \tag{4.1}$$

The definition of BW used is the -3dB, which means that limits of the bandwidth is defined by the frequencies at which the forward transmission has decreased 3dB from the transmission at f_c.

4.1 Simulation Results

The response of simulation on the 500 NW standards switch is shown in Figure 4.1. There are some deviations between the input reflection (S_{11}) and the output reflection (S_{22}). This is to be expected for all due to the difference in seen impedance for each of them.

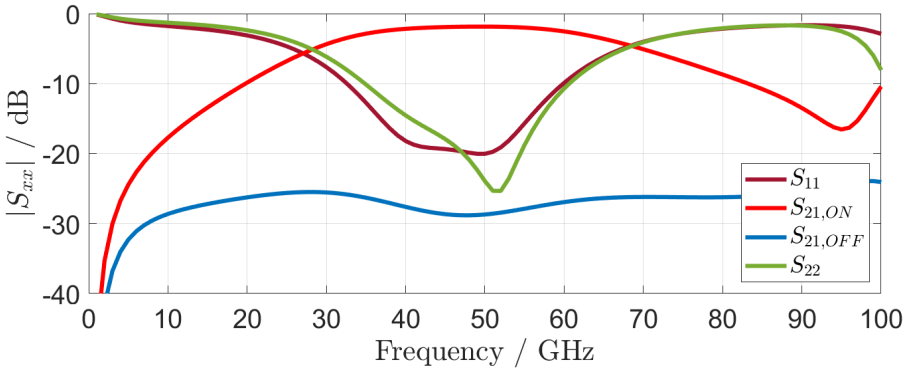


Figure 4.1: *Simulation results for the 2000 NW switch A.*

As the transistor size and R_{ON} is directly correlated it can be concluded that a larger transistor will lead to a higher reflection in the OFF branch because of the

transformation will lead to a higher impedance. The OFF branch should therefore be better isolated the larger the transistor is. Additionally, a large transistor will have better transfer properties, meaning that the ISO would also be expected to increase. Even though R_{OFF} decreases for the larger transistors, it is still large relative other resistances in the circuit, thus this should not degrade the IL.

From Figure 4.2 it can be seen that the ISO improves significantly with size and also that the improvement is somewhat linear in relation to the number o wires. Information about the differences in peak IL is hard to determine from these plots. But by observing the changes in IL it seems that C_{OFF} is the dominate factor regarding bandwidth, see Section 2.2.1, as it decreases for the larger devices. Detailed plots of each size and type configuration can be found in Appendix B.

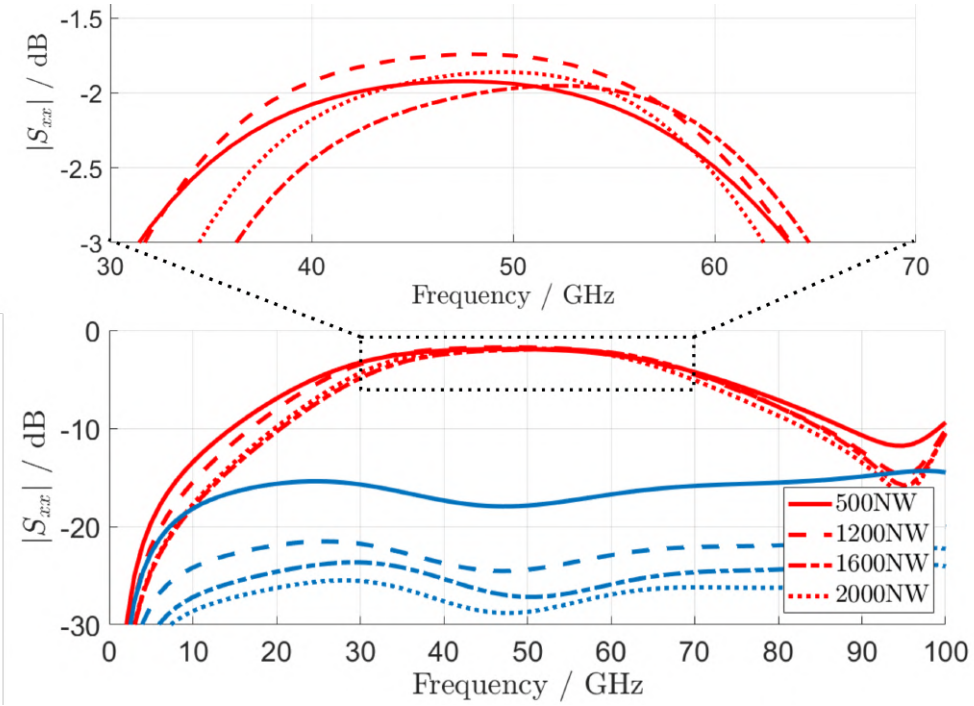


Figure 4.2: *Comparison plots for $S_{21,ON}$ (red) and $S_{21,OFF}$ (blue) for switch A with different transistor sizes. ÄNDRAD BILD*

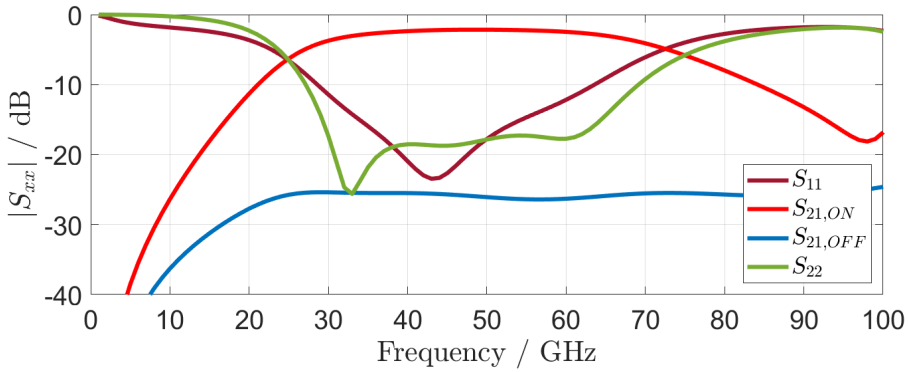
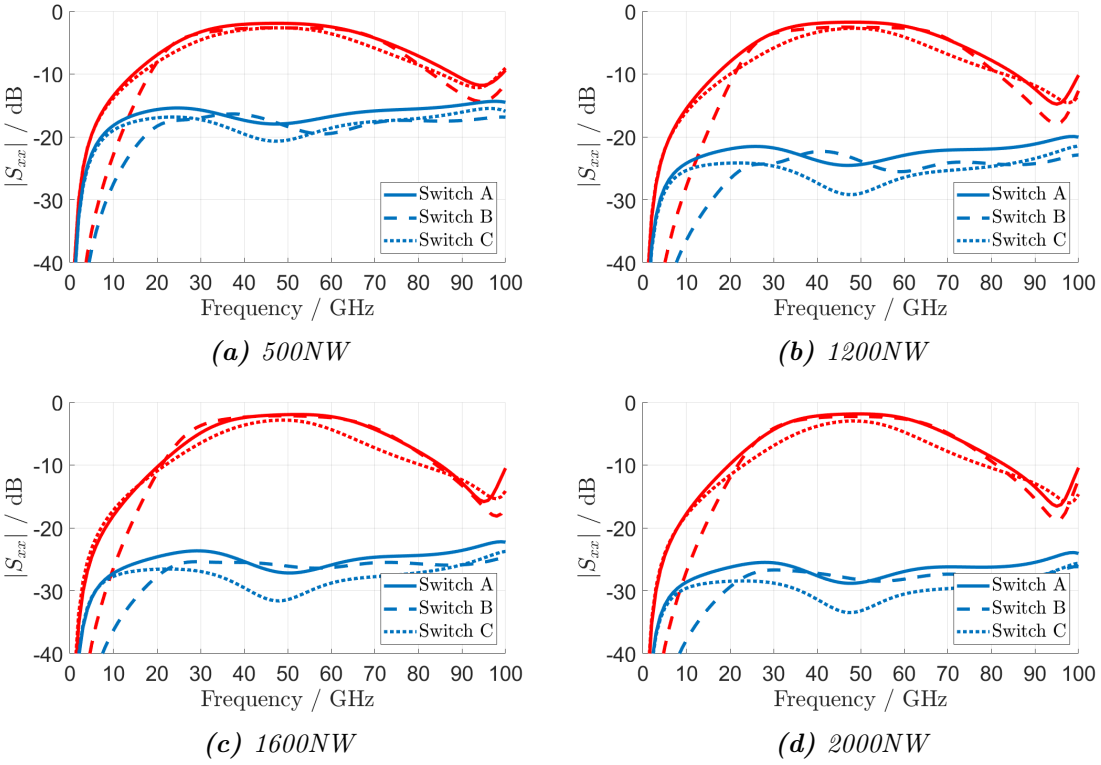


Figure 4.3: *Simulation results for the 1600 NW switch B.*

Figure 4.4 compares the different switch types for fixed transistor sizes. The standard $\lambda/4$-shunt transistor design (A) has a single resonating peak. To increase

the bandwidth and to flatten the forward transmission in the operating band a second resonating peak was introduced in switch B. These can be observed from S_{22} in Figure 4.3 . Because B introduces more reactive elements it can therefore also result in a higher IL. From Figure 4.4 it is possible to see that the bands actually are flattened in B and the bandwidth increase is between 5-12% compared to A.



(a) 500NW *(b) 1200NW*

(c) 1600NW *(d) 2000NW*

Figure 4.4: *Comparison plots for the different SPDT types. Each plot shows the three different switch types for a set transistor size, (a) 500 NW, (b) 1200 NW, (c) 1600 NW and (d) 2000 NW.*

To benchmark the different designs, one must look at the metrics and the FoM. These are all presented in table 4.1. The highest performing types regarding the FoM are marked with bold letters and it shows that the 1600 NW second order SPDT has the highest performance. But it also shows that the standard design performs better than the second order in all other transistor sizes. This is mainly due to the difference in IL. Regarding the transistor size and the IL there seems to be no apparent correlation while the switch design clearly effects the IL. The HZ and second order SPDT both have an additional TL in the signal path. This should result in a higher IL which is supported by the result. As the added TL in the HZ SPDT is longer, $l = \lambda/4 = 670\mu m$, compared to the second order SPDT, $l < 370\mu m$, it also have a higher attenuation and thus an increased IL.

The table also seems to validate the linear dependence on the number of wires regarding the ISO that was mentioned before. In relative terms the improvement between the 500 and the 1200 NW transistor is 38% while in the next size steps the increase is 11% and finally 6%. The purpose of the HZ SPDT was to increase the ISO while only having a small effect on the IL. From the table it can be concluded that the improved ISO is not as high as the theoretical derivation made by [20]. However, the dynamic range improvement as $\Delta ISO/\Delta IL$ is between 2.75-3.64 which is to be

considered as high.

Table 4.1: *The table shows all the simulated setups. NF indicates the number of gate fingers. Numbers presented here for ISO and IL are mean values.*

Transistor (NW/NF)	Topology	fc (GHz)	BW (GHz)	BWr (%)	ISO (dB)	IL (dB)	FoM (GHz)
500/5	Switch A	49	25-72	97	16.7	2.8	284
500/5	Switch B	48	23-73	104	17.8	3.3	271
500/5	Switch C	48	27-69	88	18.9	3.6	220
1200/6	Switch A	49	27-70	89	23.1	2.5	391
1200/6	Switch B	49	26-72	94	24.0	3.1	355
1200/6	Switch C	48	31-65	71	27.2	3.7	250
1600/8	Switch A	51	30-72	82	25.6	2.8	381
1600/8	Switch B	50	27-73	92	25.8	2.9	**410**
1600/8	Switch C	49	32-65	68	29.6	3.9	**250**
2000/10	Switch A	49	29-69	82	27.2	2.7	**401**
2000/10	Switch B	49	28-70	86	27.6	3.0	390
2000/10	Switch C	49	33-64	64	31.5	4.0	242

4.2 Benchmarking

As the result of this work is based on simulations without validating measured results one must be careful in concluding too much regarding comparison to measured data. However, these simulations were design using models that are created based on device measurements.

Table 4.2 shows the best performing devices in regards to the FoM compared to the measured results made by [20]. This work shows comparable results the state-of-the-art a lower IL, good BWr and a high FoM.

Table 4.2: *State of the are comparison*

Technology	Topology	BW (GHz)	BWr (%)	ISO (dB)	IL (dB)	$R_{ON}C_{OFF}$ (fs)	FoM (GHz)
50nm InGaAs mHEMT [20]	$\lambda/4$-shunt	52-168	105.5	42.1	3.1	110.3	796
50nm InGaAs mHEMT [20]	HZ $\lambda/4$-shunt	75-170	77.6	56.4	4.5	110.3	792
(This work)	Switch A	29-69	82	27.2	2.7	165	401
(This work)	Switch B	27-73	92	25.8	2.9	165	410
(This work)	Switch C	32-65	68	29.6	3.9	165	250

5

Conclusion

This work investigated the feasibility of implementing III-V Nanowire MOSFETs in three different RF switch designs. The foundation is the $\lambda/4$-shunt single-pole double throw switch. The focus of the study was to analyze the effects of different transistor sizes as well as investigating three possible circuit designs, 'A' the standard SPDT, 'B' the second order switch for flattened band and increased bandwidth, and 'C' the switch with high internal impedance for increased isolation.

In regard to the size it has been shown that when using the NW transistors the performance benefits heavily by an increased device size. For very large devices the relative improvement is decreasing and at the same time the device will experience larger capacitance and lower ON-resistances making a trade-off between bandwidth and isolation. Additionally, the possibility to realize the components might differ in difficulty. This is a topic for future studies.

The second order switch design has been shown to improve the bandwidth, slightly improved isolation while maintaining a low insertion loss of somewhat larger than the standard design. The 1600 nanowire size for this design was also shown to be the best performing in the simulations. Being simple in that it only needs an additional transmission line compared to the standard design makes for relatively small area footprint.

The high internal impedance design was able to reach an isolation of >31dB. The insertion loss is higher in this design but that can probably be compensated in a full circuit implementation with amplifier. The problem with this design is the degradation of the bandwidth.

Summarizing the result, all the switches show promise, and they all have a strong side. The best switch design is ultimately decided by the demands of the application in which it is implemented.

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Appendix A - ADS Components

TEE junction

In the simulations of the circuits the TEE junctions had some parasitic. These were derived by Stefan Andric through layout simulations and the model shown in Figure A.1 was added to each junction in the schematic in order to account for and compensate the effects from said parasitics.

The shunt transistors connect directly to the TL signal line and the ground plane and the parasitics of these are already considered when matching the stub and $C_{ON,OFF}$.

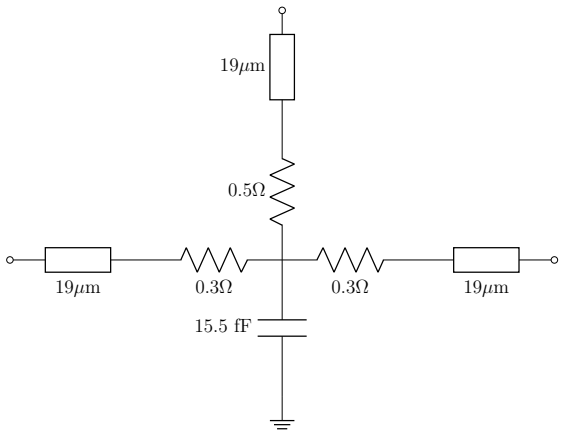


Figure A.1: *The TEE junctions used in the simulations.*

Lumped network

As addressed in Section 3.2, there was a need to isolate the gate of the transistors with a resistance, R_g. For the simulations a lumped network was designed to add all the potential contributions. This lumped network is shown in Figure A.2.

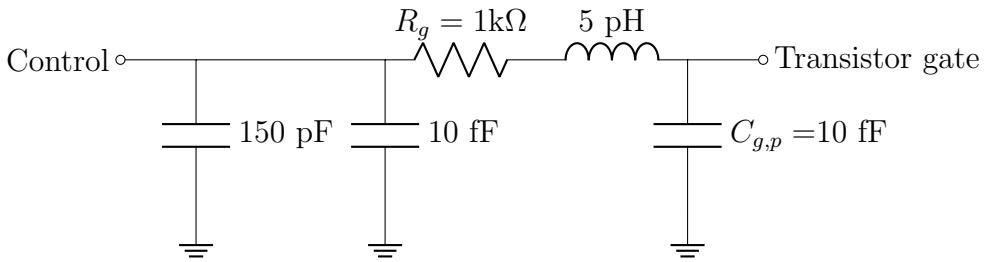
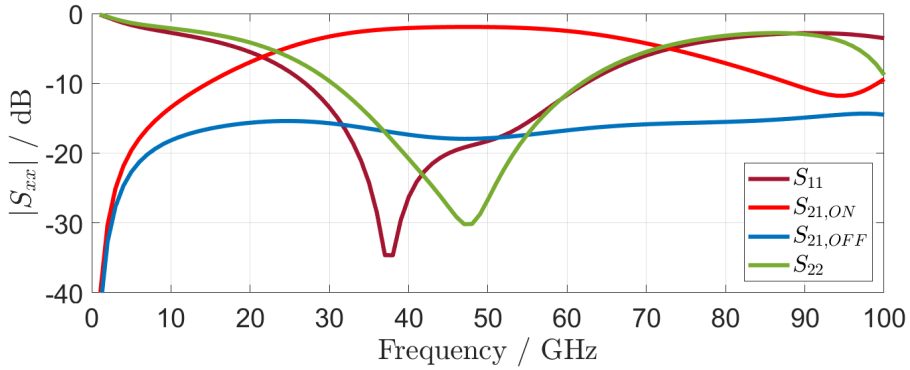


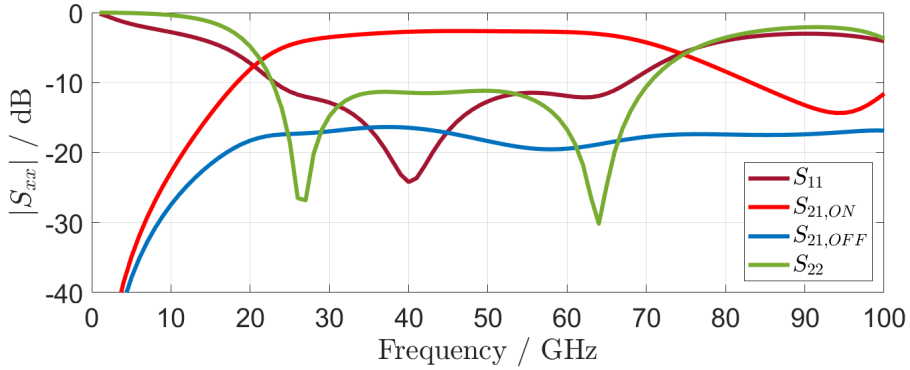
Figure A.2: *The lumped network added to the gate of the transistors in the simulations.*

Appendix B - S-parameter Plots

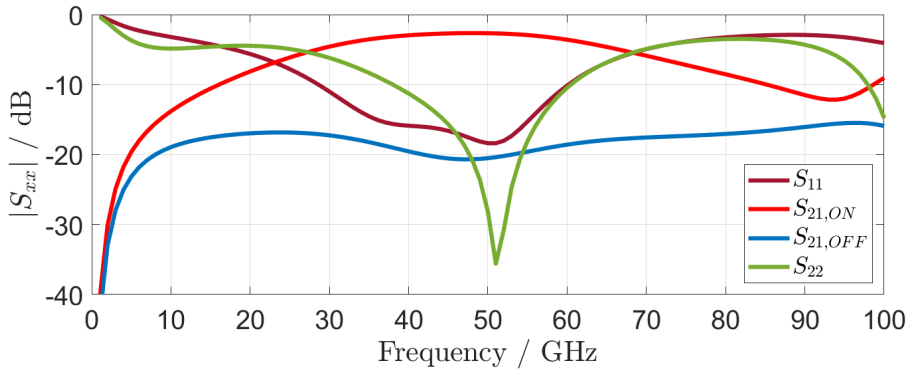
This appendix show detailed simulation results for the switch types and sizes.



(a) The standard SPDT

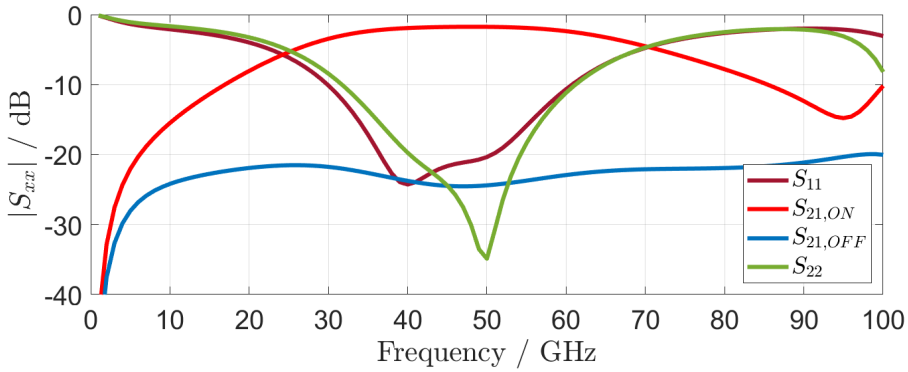


(b) The second order SPDT

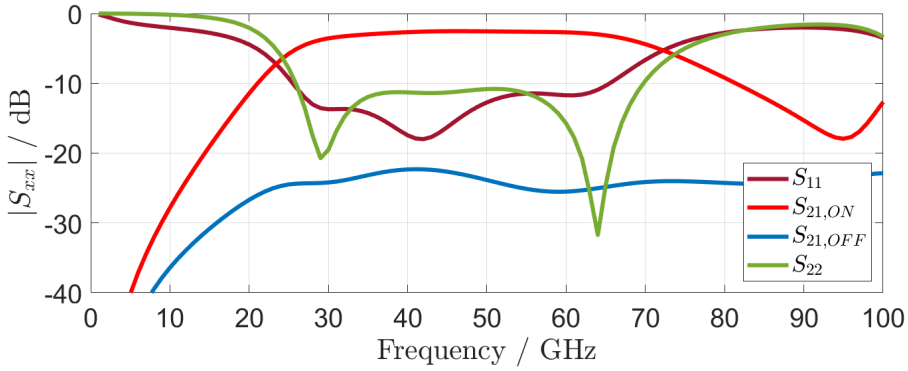


(c) The HZ SPDT

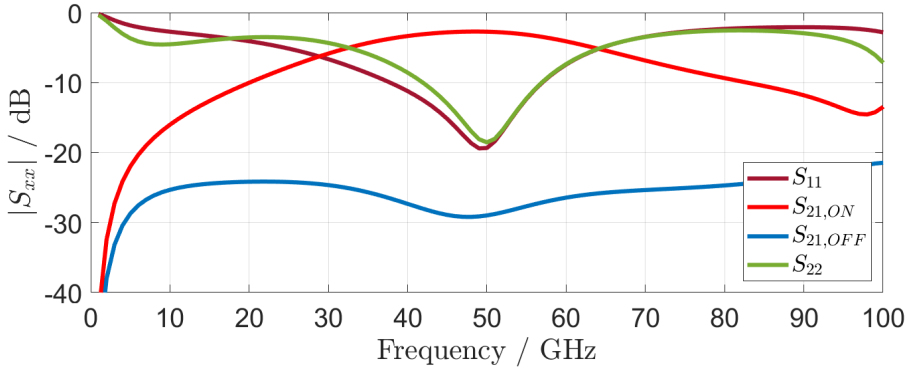
Figure B.1: *Plots shows the S-parameters from the simulated switch using 500 NW/5 fingers transistors.*



(a) *The standard SPDT*

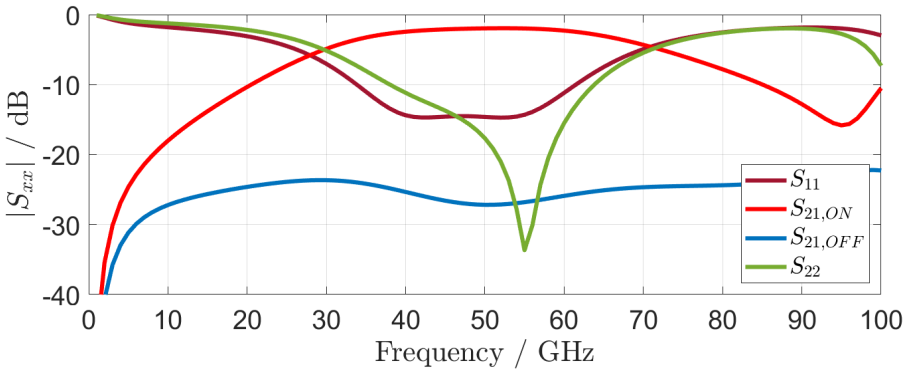


(b) *The second order SPDT*

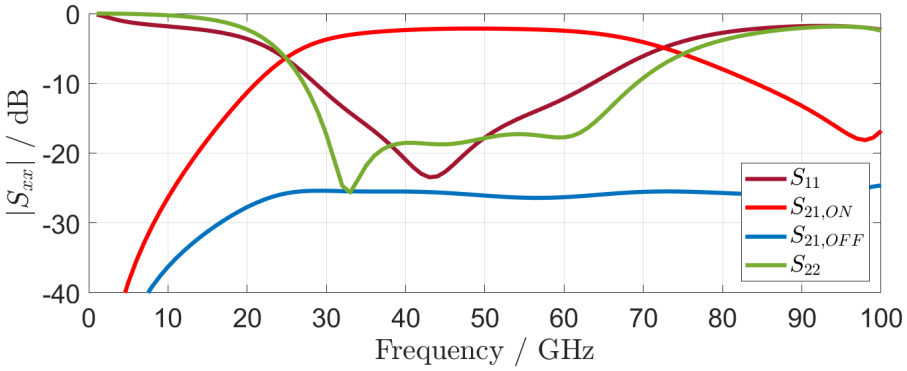


(c) *The HZ SPDT*

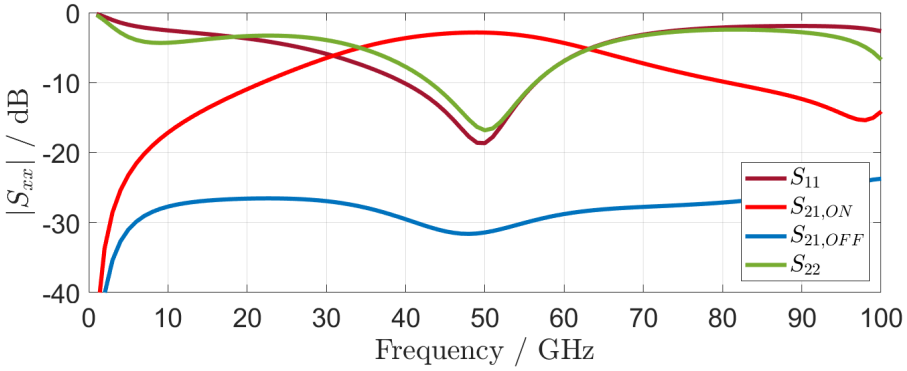
Figure B.2: *Plots shows the S-parameters from the simulated switch using 1200 NW/6 fingers transistors.*



(a) *The standard SPDT*

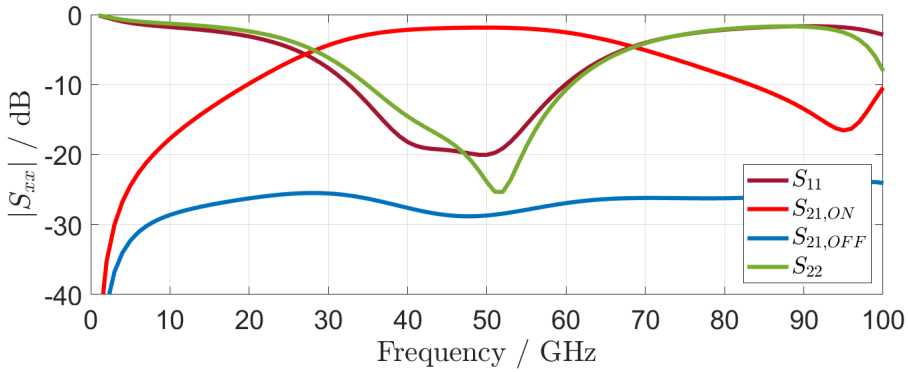


(b) *The second order SPDT*

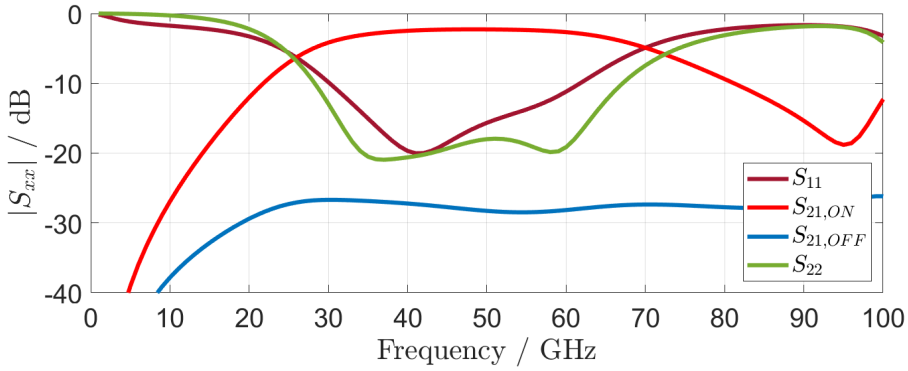


(c) *The HZ SPDT*

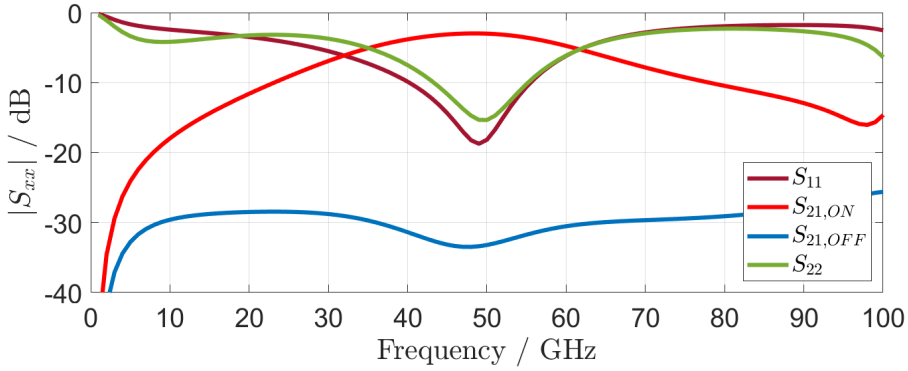
Figure B.3: *Plots shows the S-parameters from the simulated switch using 1600 NW/8 fingers transistors.*



(a) *The standard SPDT*



(b) *The second order SPDT*



(c) *The HZ SPDT*

Figure B.4: *Plots shows the S-parameters from the simulated switch using 2000 NW/10 fingers transistors.*