A design of a 100 MS/s, 8-bit Pipelined ADC in CMOS

Master's Thesis

By

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Abstract

The thesis focuses on designing and simulating an 8-bit high-speed fully differential pipelined Analog to Digital Converter (ADC) in the 65nm Complementary Metal-Oxide-Semiconductor (CMOS) technology by using the software Cadence Virtuoso. The aim is to increase the operation speed of the ADC for communication systems without reducing the performance, in the meantime, the low power consumption and the low complexity should also be required when considering future implementation.

The ADC works on 200mV to 800mV with 1.2V supply voltage and consists of six 1.5-bit stages, one 2-bit stage, and a series of digital correction circuits in the end. A Flash ADC, and a Multiplying Digital to Analogue Converter (MDAC) have been designed for each 1.5-bit stage, while the MDAC is not included in the 2-bit stage. SHA is designed at the beginning but not included in the final schematic since the sampling function is included in the MADC and the Flash ADC. The design also includes a bootstrapped switch to increase the linearity of the switches, a dynamic latch comparator to increase the speed of the Flash ADC, and a fully differential Operational Amplifier (OpAmp) to reduce the impact of the external noise, decrease the second-order harmonic distortion and increase the dynamic range.

Simulation results illustrate the SNDR reaches 48.64dB when the sampling rate is 100MHz, and it remains 47.3dB when the sampling rate increases to 200MHz.

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Popular Science Summary

In the integrated circuit field, the Analog to Digital Converter (ADC) is used to convert the analog signals to binary digital signals. I will let you know why it is important, and I will start with a background introduction.

Nowadays, with the rapid development of electronic technology, we can see electronic devices everywhere, which brings convenience and enriches our lives. The core of all the electron devices is a processor, which can be regarded as the brain created by integrated circuits. This brain is only using binary digital signals to do complex calculations. The binary number only includes 0 and 1, which build a complex digital world. However, the real world is analog, it requires a translator to translate the analog signals in our real world to the digital signals in the digital world. That translator is the ADC, it is used in most electronic devices. For example, when we are using a mobile phone, our voice is an analog signal, the ADC converts it into a digital signal, then the mobile phone can recognize it and use it to realize different functions and applications. Without the ADC, most of the electronic devices in our life will stop working.

It is obvious that the high-speed and high quality of the ADC is important to electronic devices. And my thesis focus on designing a high-speed 8-bit pipelined ADC. I will explain this title step by step. The speed of the ADC is called sampling rate, which represents how fast the ADC can sample the analog signals and convert them into digital signals. Usually, a sampling rate higher can 10MHz can be regarded as high-speed, and my ADC reaches 200MHz without conspicuous degrade of performance. 8-bit is the resolution of my ADC, it shows how accurate the ADC can be. For an 8-bit ADC, the analog signals are divided into 256 levels, and each of them is corresponding to a binary code. The pipelined structure is the key for the ADC can reach high-speed and high quality at the same time. Imagining the pipelined ADC is a large factory that includes several machines, and each machine process part of the material and gets some semi-finished products, and then sends them to the next machine until the end. Finally, all these semi-finished products are collected and processed to become final products. Here, the material is the analog input signal, and the product is the digital

output signal. These machines are the stages in the ADC, using more stages can increase the accuracy but also increase the delay, and vice versa.

The performance is highly dependent on the technology that is using in the integrated circuit. The technology is limited by the accuracy of the stepper, which is used to fabricate the integrated circuits. For example, the technology of this design is 65nm, which means the maximum error in this integrated circuit is ±65nm. With the development of the steppers, this value will decrease gradually. I am looking forward to improving the design with higher technology in the future, it is exciting but also challenging.

Acknowledgments

This Master's thesis would not exist without the support of many people. First of all, I offer my sincerest gratitude to my supervisor Prof. Pietro Andreani and Post Ph.D. Siyu Tan for their guidance and supports during the entire period of my study at Lund University.

Then, I would like to express my gratitude and appreciation to my parents for their love, support, and understanding.

In the end, I want to thank all my friends at Lund University, who supported and helped me throughout my time in Sweden.

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List of acronyms

CMOS	Complementary Metal-Oxide-Semiconductor
ADC	Analog to Digital Converter
DAC	Digital to Analogue Converter
ENOB	Effective Number Of Bits
DSP	Digital Signal Processing
SNR	Signal to Noise Ratio
SNDR	Signal to Noise and Distortion Ratio
SFDR	Spurious Free Dynamic Range
HD	Harmonic Distortion
THD	Total Harmonic Distortion
INL	Integral Non-Linearity
DNL	Differential Non-Linearity
SAR	Successive Approximation Register
OpAmp	Operational Amplifier
SHA	Sample and Hold Amplifier
MDAC	Multiplying Digital to Analogue Converter
VLSI	Very Large Scale Integration
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuits
CM	Common Mode
CMFB	Common-Mode Feedback
RMS	Root-Mean-Square
FoM	Figure of Merit
LSB	Least Significant Bit
MSB	Most Significant Bit
OSR	Over Sampling Ratio
DFF	D type flip-flop
DC	Direct Current

MOS	Metal-Oxide-Semiconductor
NMOS	N-type Metal-Oxide-Semiconductor
PMOS	P-type Metal-Oxide-Semiconductor
DCVSL	Differential Cascode Voltage Switch Logic
UGF	Unit Gin Frequency
PM	Phase Margin

1. Introduction

Recently, digitalization became a tendency of nowadays integrated circuits systems because of its flexibility, feasibility for Very Large-Scale Integration (VLSI), anti-noise ability, etc. [1] In a communication system, digital circuits are widely used to achieve high performance and accuracy, such as Digital Signal Processing (DSP) circuits, digital calibration circuits, etc. On the other hand, the essence of wireless communication is an electromagnetic wave, which is an analog signal. The analog Radio Frequency Integrated Circuits (RFIC) are the fundamental part of a communication system, while all the computation, calculation, and processing are done in the digital core. In this case, the ADC is inevitable that behaves like a bridge between the real world and the digital world, converts analog signals to digital signals [2].

With the rapid development of communication technology, especially nowadays 5G, the speed of the system becomes more and more critical. [3] The ADC with a high speed or high sampling rate has been widely investigated to fulfill the requirements. However, the presumed performance of an ADC also includes low power consumption, high resolution, high accuracy, and a small area with a low power supply. After the consideration and the tradeoff, the thesis aims to increase the speed of the ADC to work on the higher sampling rate without degrading the performance and the resolution. To achieve the low power consumption condition, 1.2V supply voltage is used, and all the transistors are low-power, low-threshold type with the typical corner.

In this thesis, after a brief introduction in the first chapter, some necessary background and theories are presented in the second chapter. In addition, some different type of ADC is introduced and compared with their advantages and limitations. Then, a fully differential 8-bit pipelined ADC of 65nm CMOS technology is designed and simulated in the software Cadence Virtuoso with the performance analysis in the software MATLAB. The design methodology and detailed block structure can be found in the third chapter and the simulation results and performance analysis are illustrated in the fourth chapter. The fifth chapter is the conclusion and discussion. In the end, the last chapter shows an expectation and plan for future work.

2. Background

The thesis presents a 100MS/s 8-bit fully differential ADC. The ADC is used to convert the analog voltage input signal into the digital voltage output signal before the digital core can process and make the calculations. 100M/s is the sampling rate, which limits the speed of the ADC. The pipelined ADC as a Nyquist-rate data converter also determines the highest possible frequency of the input, half of the sampling rate. The 8-bit is the resolution of the ADC, which limits the accuracy. The output can be divided into 256 voltage levels corresponding to the 8-bit resolution. The fully differential structure requires two inverse inputs corresponding to the Common Mode (CM) voltage. It can reduce the impact of the external noise, decrease the second-order harmonic distortion and increase the dynamic range.

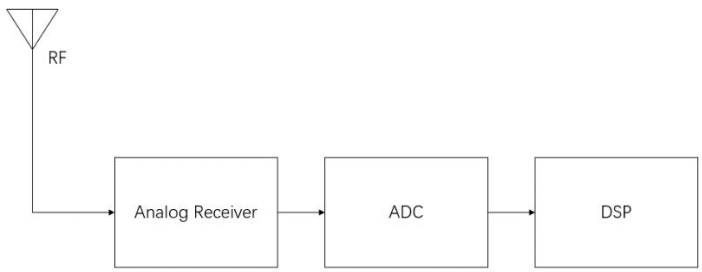


Figure 1. The block diagram of a receiving end.

Fig. 1 shows the block diagram of the receiving end of a communication system. An antenna receives the Radio Frequency (RF) electromagnetic wave before the analog receiver produces an analog output. Usually, an anti-aliasing filter will be used between the ADC and the analog receiver to remove the interference frequency out of the desired band. Then, the ADC converts the analog signals into digital signals for the DSP core to make computations and calculations. A pre-distortion filter is often used between the ADC and the DSP core to increase performance and accuracy. As can be seen, the speed and the accuracy of the ADC are critical for a high-speed and high-quality communication system.

2.1. Concept and Principle

It requires several steps to convert a continuous analog signal to a discrete digital output code as an ADC. Fig. 2 shows the block diagram of an ADC. The first step is sampling, which transforms the continuous-time signal or the continuous amplitude to a discretely sampled signal during the sample phase by the sampler and holds the signal during the hold phase by the holder. Usually, the clocks for sampling and holding are non-overlap clocks. Then, the next step is quantization by the quantizer, which transforms the sampled value or voltage in the holder to a corresponding quantization level depends on the resolution and the dynamic range of the ADC. In the end, a coder is used to transform the quantization output into a digital code.

Figure 2. The block diagram of an ADC.

According to the Nyquist condition, the highest input frequency cannot be larger than half of the sampling frequency. As a result, a higher sampling frequency or a higher sampling rate is always what one presumed in a high-speed ADC, especially in a communication system with MHz or even GHz waves. In addition, with the development of digitalization, the accuracy and the capability of DSP also require a higher resolution and accuracy in ADC.

2.2. Specifications and Characterizations of ADC

2.2.1. PVT Conditions

The PVT conditions are the Process corners, the Supply voltage, and the Temperature. A reliable ADC should be trouble-proof in a range of the variations that appear in these three conditions. For example, the ADC should be able to work on all the common process corners for CMOS technology, such as Fast-Fast, Slow-Fast, Slow-Slow, and Fast-Slow. The

ADC should also be stable for a range of temperature and supply voltage when considering the practical implementation and applications.

2.2.2. Performance

To quantify the performance of a designed ADC, some performance specifications have been chosen. For example, the Signal to Noise and Distortion Ratio (SNDR) shows how the noise and distortion impact the performance, while the Signal to Noise Ratio (SNR) and Signal to Distortion Ratio (SDR) represents the noise and distortion part, respectively. The Spurious Free Dynamic Range (SFDR) is the ratio of the Root-Mean-Square (RMS) magnitude of the input frequency and the RMS magnitude of the most significant noise or distortion. All the ADC have a theoretical SNDR corresponding to the resolution as shown in (1).

$$SNDR = 6.02N + 1.76 \tag{1}$$

where N is the resolution of the ADC. For example, the theoretical SNDR for an 8-bit ADC reaches 49.92dB. On the other hand, the Effective Number Of Bits (ENOB) is calculated by the measured SNDR as shown in (2).

$$ENOB = (SNDR - 1.76)/6.02 \tag{2}$$

where the SNDR is the practical SNDR, the ENOB can be used to represent the distance between the performance of the practical circuits and that of an ideal case. Many factors limit the performance of the ADC and make it never reach the theoretical value.

Some other parameters show the performance of an ADC, which is also essential. For example, Harmonic Distortion (HD) is the ratio between the RMS input and the RMS harmonic components of k order, where k is an integer number larger than 1. Total Harmonic Distortion (THD) is always used to represent the impact of HD. Usually, the second and third HD is dominated since the amplitude of HD decays with the growth of k. However, the even order HD can be almost removed in a differential design because of the symmetry.

The bandwidth of the ADC is not only determined by the Nyquist condition of sampling frequency. The performance, usually SNDR, can degrade dramatically before the input frequency reaches the half sampling frequency. In this case, Effective Resolution Bandwidth (ERBW) is defined as the largest input frequency that the ADC can handle until the SNDR drops by 3dB.

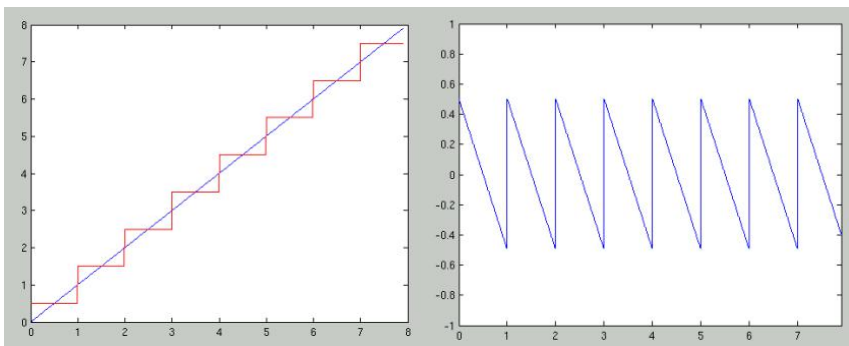
Low power consumption is usually one of the most important features when designing an ADC. The Figure of Merit (FoM) is the parameter that can show the power efficiency as shown in (3).

$$FoM = \frac{P_{total}}{2^{ENOB} \times 2ERBW} \tag{3}$$

where the P_{total} is the total power consumption, the ENOB is the Effective Number of Bits, and the ERBW is the Effective Resolution Bandwidth.

2.2.3. Quantization Error

The quantization error, as the limiting factor of the theoretical SNDR, is an inevitable noise in the ADC because the analog input is a continuous signal while the digital output is a discrete signal. Fig. 3(a) shows a quantization of a ramp signal with an 8-quantization level, while the red line represents the quantized output, and the blue line is the original ramp signal. The corresponding quantization error is shown in Fig. 3(b).



(a) (b)

Figure 3. Quantization error of a ramp signal.

The higher-resolution or the lower Least Significant Bit (LSB) is the lower the quantization error the ADC produces. The range of the quantization error is from $-\Delta/2$ to $\Delta/2$ with an average power of $\Delta^2/12$. Here, Δ is defined as X_{FS}/M, where X_{FS} is the full-scale magnitude of the input, and M is the quantization level (usually 2^N, N is the number of bits). For example, the full-scale magnitude of the input and the quantization level of

the ADC designed in the thesis is 600mV and 256, respectively, then the power of the quantization error is $4\times10^{-7}V^2$.

2.2.4. Jitter

The jitter is also an inevitable noise in the ADC because of the non-perfectly balanced distribution of the clock tree, the internal thermal noise, and external interference, etc. The signal to jitter noise ratio can be calculated by the input frequency as shown in (4).

$$SNR = -20log_{10}(2\pi f_{in}(\delta(nT))) \quad (4)$$

where $\delta(nT)$ is the sampling of a random variable, f_{in} is the input frequency. As a result, the jitter should be less than 5.08ps to reach 50dB SNR at 100M input frequency. The clock jitter is a critical factor, especially with the large magnitude or high-frequency input, limiting the performance of the ADC by making the sampling period inhomogeneous or produce delay among the clock periods.

2.2.5. Thermal Noise

The thermal noise (kT/C noise) always appears in the transistors because of the thermal movement of the electrons as shown in (5). [4]

$$\overline{V_n^2} = 4kTR\Delta f \quad (5)$$

where $\overline{V_n^2}$ is the RMS power of the thermal noise, the k is the Boltzmann's constant approximately equal to 1.38×10-23J/K, the T is the absolute temperature usually assumes to be 300K (room temperature), the R is the resistance in the circuits. The Δf is the bandwidth of the circuits, which produces the thermal noise. However, in an ADC, the thermal noise caused by the Sample and Hold Amplifier circuit (SHA) is inevitable and only depends on the sampling capacitance, not resistance. The power of this type of thermal noise can be calculated as shown in (6).

$$v_{n,c}^2 = kT/C_s \quad (6)$$

where the C_s is the sampling capacitance, the $v_{n,c}^2$ are the power of the thermal noise from the capacitance. In this case, the value of the sampling capacitor in the SHA is determined by the thermal noise, and (6) can be written as (7).

$$C_s = kT/v_{n,c}^2 \quad (7)$$

In addition, thermal noise is a white noise that is independent of the input frequency [5]. That means the thermal noise will remain at the same level when increasing the input frequency. The T is proportional to the thermal noise, while the capacitance is inversely proportional to the thermal noise. It seems that a large capacitor is required to minimize the thermal noise. However, a larger capacitance consumes more time to charge, which will decrease the speed of the circuit, and lead to a critical problem in a high-speed ADC. It is essential to choose a suitable value of the capacitor in the SHA and make a tradeoff between thermal noise reduction and speed enhancement.

2.2.6. Mismatch and Offset

The offset of the ADC is a difference between the practical transform line and the ideal one, which appears in all the bits. Fig. 4 shows the impact of the offset error in an ADC. The dashed lines represent the ideal transform line and the ideal output of the ADC, respectively, while the full lines show the actual ADC output and transform line with an offset. The offset of an ADC derives from the offset in OpAmp or comparators.

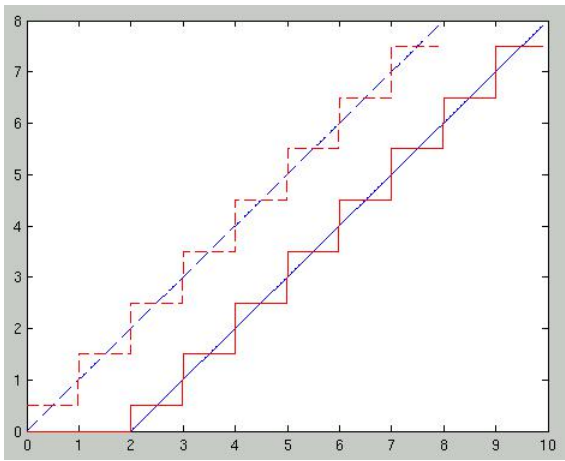


Figure 4. The Offset of an ADC.

The offset in the OpAmp can be divided into two parts: offset voltage and offset currents and can be further divided into input offset and output offset. Usually, the offset occurs when the circuits have a mismatch because of the asymmetry of the structure in the circuits, especially in the differential pair. The offset can shift the CM voltage and lead to a shifting of all the quantization steps. The means all the outputs of the ADC are shifted to higher or lower bits than expected. However, in a fully differential

OpAmp, the CM voltage can be controlled and adjusted by the CMFB's bias voltage, minimizing the impact of the mismatch in the circuits. [4]

The offset in the comparator is often because of the mismatch in the input differential pair. This type of offset can degrade the accuracy of the comparator and the ADC. However, it is not a critical problem as long as the offset is small and a reference voltage is used to compensate for the offset.

2.2.7. Gain Error

The gain error is a percentage number that shows how much the slope of the practical transform line deviates from the ideal one as shown in Fig. 5. [5] The dashed lines represent the ideal transform line and the ideal output of the ADC, respectively, while the full lines show the actual ADC output and transform line with a gain error.

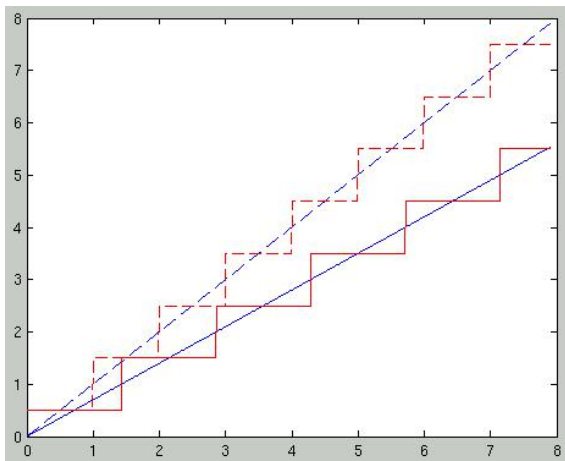


Figure 5. The gain error of an ADC.

The gain error usually occurs in the circuits associate with OpAmp because of the finite gain of open-loop gain of the OpAmp and the Non-Linearity components. The closed-loop gain of the OpAmp with a feedback loop approaches the reciprocal of the feedback factor when the open-loop gain approaches infinite. The gain error can lead to a non-linearity of the ADC and reduce the dynamic range. The gain error can be minimized by increasing the open-loop gain of the OpAmp to a high enough level.

However, the gain and the bandwidth of an OpAmp can never be improved simultaneously in a determined technology. Furthermore, insufficient bandwidth is critical when the ADC is presuming higher speed. The gain error is also because of the mistake in the comparators and the reference voltage.

2.2.8. Non-Linearity

The Non-Linearity includes the Differential Non-Linearity (DNL) and the Integral Non-Linearity (INL). [5] Both of them are important specifications for an ADC. The DNL represents the deviation of the step size from the ideal one at each bit as shown in Fig. 6, while the INL can be regarded as an accumulation of all these deviations as shown in Fig. 7. The INL can increase the noise floor and produce harmonic distortion. Fig. 6 shows the DNL of an ADC; the dashed lines represent the ideal transform line and the ideal output of the ADC, respectively, while the full lines show the actual ADC output.

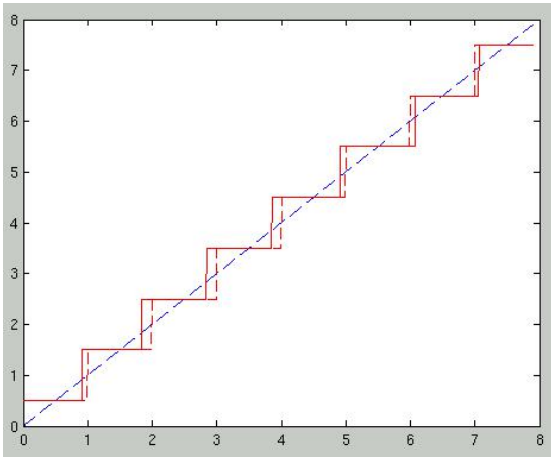


Figure 6. DNL of an ADC.

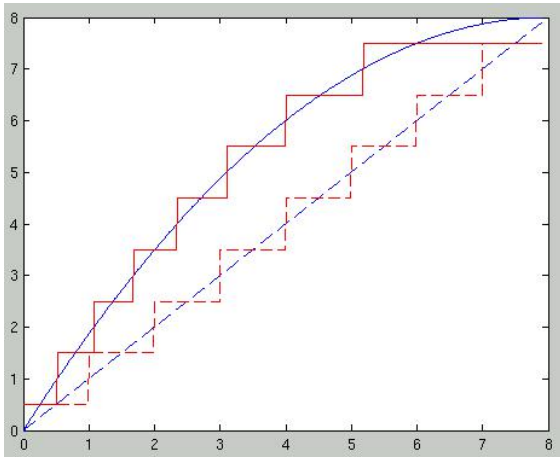


Figure 7. INL of an ADC.

Fig. 7 shows the DNL of an ADC; the dashed lines represent the ideal transform line and the ideal output of the ADC, respectively. In contrast, the full lines show the actual ADC output and transform line. It is measured after the gain error and offset are compensated. Various factors can lead to the non-linearity of an ADC, such as the errors during comparison, gain errors, and the non-linearity of the CMOS transistors. As a reliable ADC with high performance, both INL and DNL should be less than 1 LSB to avoid missing code.

2.3. Different types of ADC

Nyquist rate ADC and Oversampling ADC are the two main families, which have been widely invested and researched. [5] Nyquist rate ADC has more available bandwidth compares to Oversampling ADC with the same sampling rate. On the other hand, Oversampling ADC has less quantization error and higher anti-aliasing ability compares to Nyquist rate ADC with the same frequency range of the input signal.

2.3.1. Flash ADC

Flash ADC is the simplest and fastest ADC that belongs to the Nyquist rate ADC family, can only consist of resistors, comparators, and logic gates. Fig. 8 shows an architecture of a 2-bit Flash ADC.

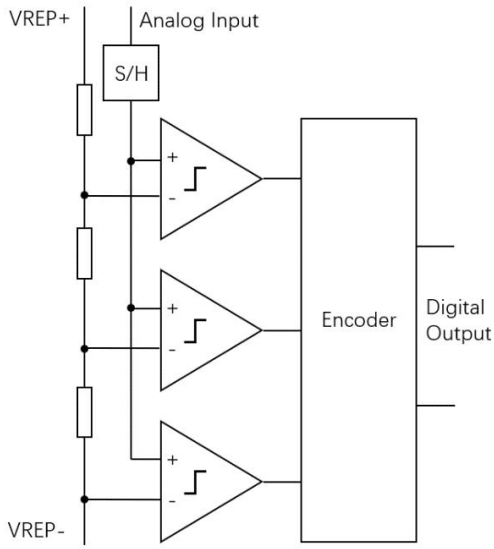


Figure 8. 2-bit Flash ADC architecture.

However, the Flash ADC is suitable for a resolution higher than 6 bits because it requires 2^N-1 comparators, where N is the number of bits. For example, an 8-bit Flash ADC requires 255 comparators. The exponential growth of the hardware and the power consumption with the increasing of the resolution is the critical disadvantage of the Flash ADC. In addition, the comparators have speed limitations, and the resistors in the resistive divider and the capacitance of the sampling capacitor also limit the highest speed of the Flash ADC. As a result, it is impossible to implement a Flash ADC with high resolution with high sampling rate. In a pipelined ADC, the Flash ADC is always used as a sub-ADC in each pipe stage and only responsible for 1.5 bits or 2 bits.

2.3.2. ΔΣ ADC

ΔΣ ADC is a typical Oversampling ADC that enhances the accuracy and resolution by a tradeoff with the input bandwidth. Fig. 9 shows the architecture of a ΔΣ ADC, which consists of an SHA, a DAC, a quantizer, an integrator, and an adder. The core component is the noise shaping modulator, which reduces the in-band quantization error.

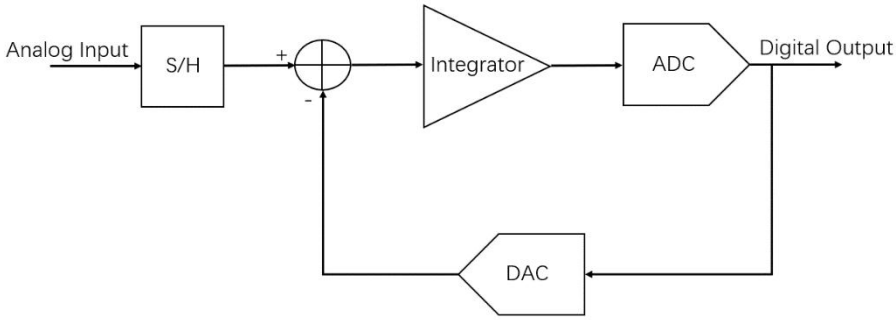


Figure 9. ΔΣ ADC architecture.

Oversampling ADC only uses a small part of the Nyquist band, making it possible to decrease the quantization error, improve the SNR, and increase the ENOB. The oversampling level can be represented by the Over Sampling Ratio (OSR) is shown in (8).

$$OSR = f_s/2f_B \tag{8}$$

where, the f_s is the sampling frequency, and the f_B is the frequency bandwidth. Then, the power of the quantization error becomes

$$V_n^2 = \frac{\Delta^2}{12} \times OSR \tag{9}$$

where the V_n^2 quantization noise power with the oversampling band, the $\Delta^2/12$ is the quantization error, and the OSR is defined in (8). As a result, the ENOB can be calculated as shown in (10).

$$ENOB_{OS} = N + 0.5log_{10}OSR \tag{10}$$

where $ENOB_{OS}$ is the Effective Number of Bits for the Oversampling ADC, and N is the number of the resolution.

2.3.3. Successive Approximation Register (SAR) ADC

Fig. 10 shows the architecture of a SAR ADC consists of a sample and hold circuit, a comparator, a DAC, and a SAR Logic block.

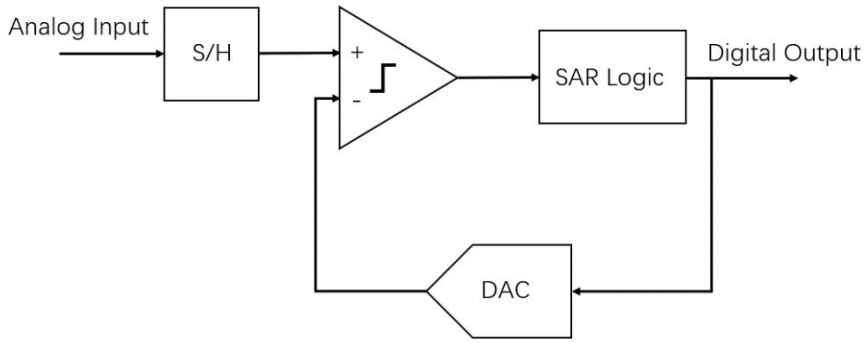


Figure 10. SAR ADC architecture.

The core principle of the SAR ADC is the SAR algorithm that makes the decision by comparing the input to half of the rest reference voltage and store the value into a register, repeat the process until the last bit. Eventually, the binary code can be determined from Most Significant Bit (MSB) to Least Significant Bit (LSB). The SAR ADC consists of an SHA, a comparator, a DAC, a SAR logic block, and a register. The input after SHA compares to half of the current reference voltage in the comparator, and the result stores in the register and determines which half reference will be chosen for the next step. For example, in the first step, the input compares to half of the reference voltage and determines the MSB whether it is 1 or 0, then the value of MSB is used to determine whether 3/4 or 1/4 can be chosen to the comparison in the next step. SAR ADC is a common Nyquist rate ADC relies on its high resolution and high accuracy, which is a tradeoff by speed.

2.3.4. Pipelined ADC

The Pipelined ADC is a popular Nyquist ADC that can be used in many fields for its high-speed and high resolution. Various pipelined ADCs have been designed to work on a sampling rate of MHz to GHz with 8 bits to 16 bits resolution depends on the CMOS technology. [1][6][7][8][9][10][11][12]

Fig. 11 shows a typical architecture of a pipelined ADC consists of several cascade pipelined stages and a digital correction circuit. Each internal stage includes an SHA, a sub-ADC, a DAC, a multiplier, and an adder as shown in Fig. 12.

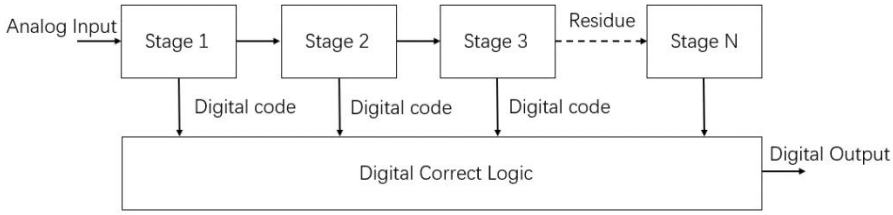


Figure 11. Pipelined ADC architecture.

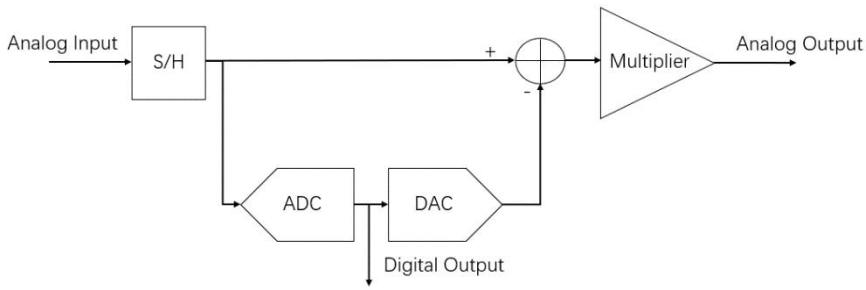


Figure 12. Structure of the internal stage.

The principle of the pipelined ADC is that each stage converts one or more binary bits and generates a residue signal to the next stage. Then, a digital correction circuit is used to compensate for the delay among each stage and correct the binary outputs. The S/H circuit is used to avoid the variation of the signals during the processing. The combination of a sub-ADC and a DAC is used to generate the binary output of the current stage and the compensation of the residue signal for the next stage. For example, for a 1.5bit stage, the input from -Vref to +Vref is divided into three parts: -Vref to -Vref/4, -Vref/4 to Vref/4, and Vref/4 to Vref, while the DAC adds Vref/2 to the first part and subtracts Vref/2 to the last part. After the Multiplication, the range of the residue signal can be compensated into -Vref to +Vref again. Practically, the DAC, the multiplier, and the adder can be designed into one circuit called Multiplying Digital to Analogue Converter (MDAC) or Residue generator circuit. The sub-ADC is usually a FLASH ADC with a 1.5-bit resolution, only requires two comparators. Two non-overlap clocks control all the stages to avoid error between stages. A digital correction circuit includes shift registers, full adders, and N-bit D

type Flip-Flop (DFF) are used to correct the digital output of each stage and convert it into an N-bit binary code.

2.4. Different types of Comparator

2.4.1. Amplifier Comparator

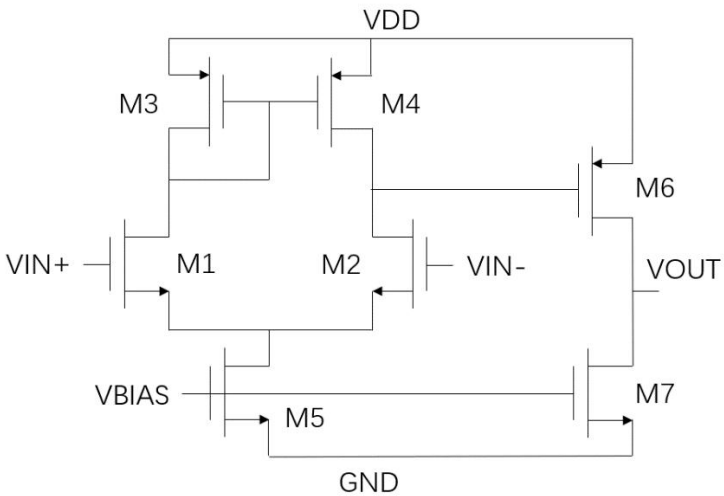


Figure 13. Schematic of an N-type two-stage OpAmp.

An OpAmp without a feedback loop can be used as a comparator. The small difference in the differential pair amplifies to a large enough level for digital circuits. Fig. 13 shows a typical structure of an N-type two-stage single-end OpAmp. A suitable bias voltage in M5 and M7 is required to make sure all the transistor is working in the correct operation region. Usually, a compensation capacitor connects to the outputs between the first stage and the second stage is used to ensure the stability of the OpAmp.

The limitation of the amplifier type comparator can be summarized into two main problems. Firstly, the OpAmp has a speed limitation base on the frequency response and the slew rate. An input with a higher frequency than the bandwidth of the OpAmp is impossible for this type of comparator. In addition, if the full-scale of the input is too large, the OpAmp will be not fast enough to handle. To increase the slew rate, a large bias current is required. However, if a large current is going through to the transistors, power consumption will become a problem, especially the static power consumption from both stages.

2.4.2. Static Latch Comparator

The static latch comparator consists of a pre-amplifier and a regeneration latch. Fig. 14 shows a general schematic of a static latch comparator.

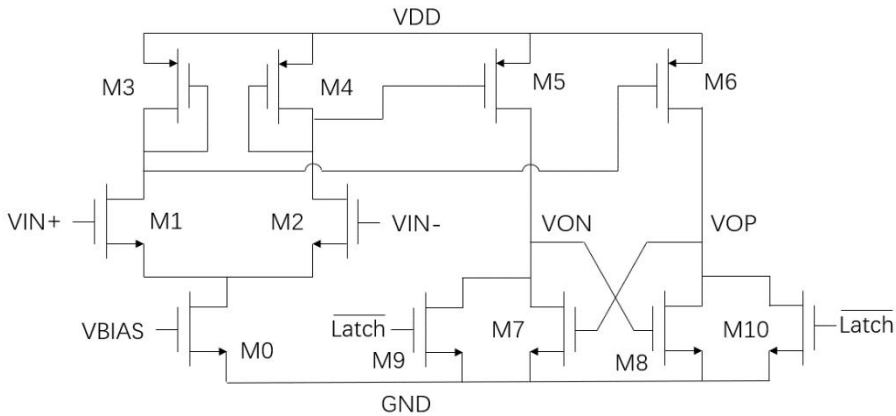


Figure 14. Schematic of a static latch comparator.

The differential pair M0 to M4 is used as a pre-amplifier for the two inputs, a suitable voltage for the VBIAS is required. The regeneration latch consists of two cross-coupled inverters M5, M7, and M6, M8, that compare and regenerate the value with the positive output at VOP and negative output VON. For example, if the voltage at VIN+ is higher than that of VIN-, When the Latch signal is low, the voltage of VON and VOP reset to GND through M9 and M10. The advantage of the static latch comparator is no kickback noise is produced between the regeneration latch and the input pair. As a tradeoff, the speed of the static latch comparator is low, and the power consumption is high due to the static regeneration process.

2.4.3. Dynamic Latch Comparator

Fig. 15 shows a typical schematic of a dynamic latch comparator. During the reset phase, the Latch signal is low, M0 is cut off, and no static current flows from VDD to GND. When the Latch signal is high, the regeneration phase starts. For example, if the voltage at VIN+ is higher than

that of VIN-, the drain voltage of M3 drops faster than M4, which makes VON discharge to 0 through M3 and VOP charge to 1 through M6.

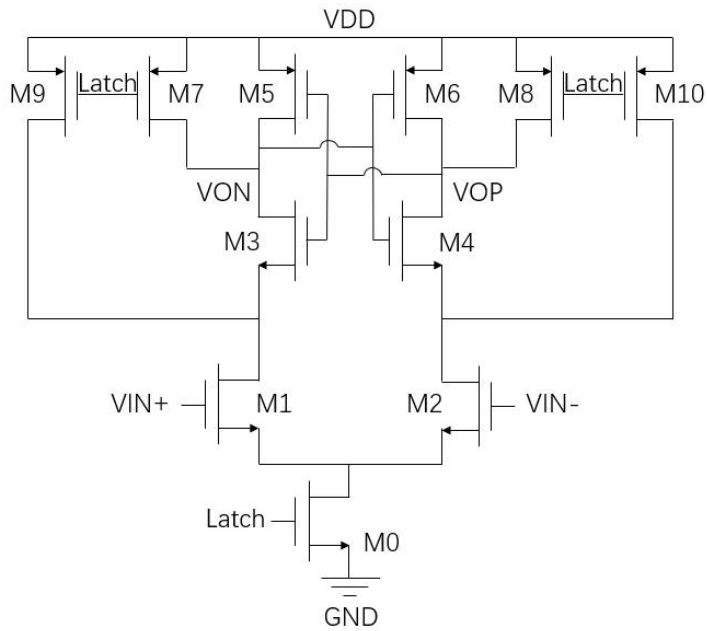


Figure 15. Schematic of a dynamic latch comparator.

The most important feature of the dynamic latch comparator is that the current only exists during the regeneration. No static current during the reset consumes low static power since the differential pair is directly connected to the regeneration latch. However, this dynamic structure increases the speed but also produces kickback noise. A kickback noise reduction circuit is required to minimize the impact of the kickback noise of the input signal.

2.5. Different types of OpAmp

2.5.1. Two-stage OpAmp

The two-stage single-end is a simple and basic OpAmp that only requires eight transistors. The structure is shown in Fig. 16.

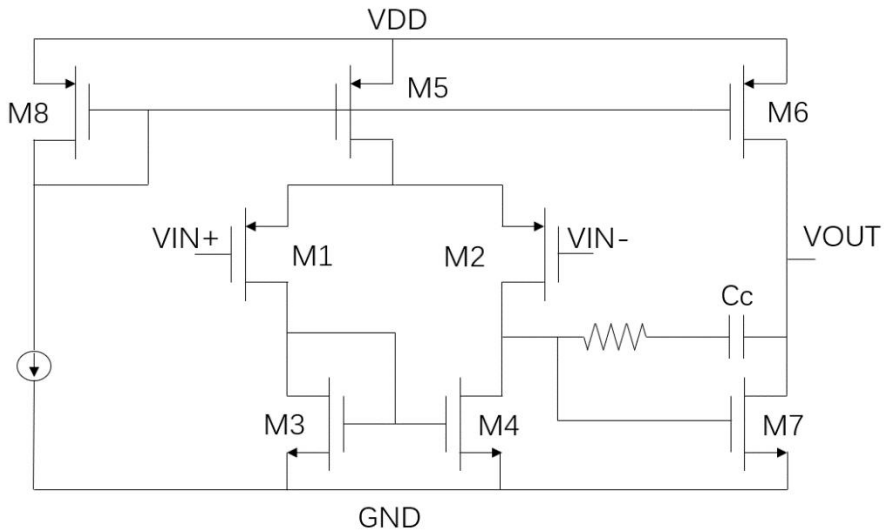


Figure 16. Schematic of a two-stage OpAmp.

The transistors M1 to M5 are the first stage, while M6, M7 are the second stage. The compensation capacitor Cc is used to increase the phase margin and ensure stability. The gain of the OpAmp is

$$G = g_{m1}(r_{o1} \| r_{o3}) g_{m6}(r_{o6} \| r_{o7}) \tag{11}$$

where the G is the open-loop DC gain of the OpAmp. The g_{m1} and g_{m6} are the transconductances of the transistors M1 and M6, respectively. The r_{o1}, r_{o3}, r_{o6}, and r_{o7} are the output resistance of M1, M3, M6, and M7. The dominant pole is

$$p_1 = -\frac{1}{gm_6 R_1 R_2 C_c} \tag{12}$$

where the p_1 is the dominant pole, C_c is the compensation capacitance. R_1 and R_2 is $r_{o1} \| r_{o3}$ and $r_{o6} \| r_{o7}$, respectively. The non-dominant poles are

$$p_2 = -\frac{gm_6}{C_1 + C_2} \tag{13}$$

$$p_3 = -\frac{1}{RC_1} \tag{14}$$

where the p_2 and p_3 are the second pole and the third pole, respectively, C_1 is the parasitic capacitance, and C_2 is the load capacitance, R is the resistance. The OpAmp has three poles because of the three independent capacitors. On the other hand, the OpAmp also has a zero as shown in (15).

$$z = \frac{1}{(\frac{1}{gm_6} - R)C_c} \tag{15}$$

To provide a positive phase shift and increase the phase margin, the resistance R should be larger than $\frac{1}{gm_6}$, and it is usually implemented using a MOS transistor. [4] Equations (12) to (15) are approximations base on the assumption gm_6R_1 and gm_6R_2 >>1, and Cc is large enough. The second stage's output swing is determined by the second stage, making the DC gain of the second stage less than the DC gain of the first stage. To ensure the stability of the OpAmp, a compensation circuit is connected between the two stages. The compensation circuit consists of the capacitor Cc and the resistor R. A self-resonance will occur when the phase margin of the OpAmp is not large enough, which also means the OpAmp is unstable. However, it takes a longer settle time for a larger phase margin. The compensation capacitor Cc can increase the phase margin with a tradeoff of the bandwidth. In addition, the bandwidth and the gain are also opposing, which it is impossible to optimize the gain and the bandwidth at the same time. As a result, in given CMOS technology, making the tradeoff between bandwidth and gain while ensuring the stability to fulfill the design specification is a practical way of designing an OpAmp.

2.5.2. Gain-boosting OpAmp

Fig. 17 shows the technology of the gain-boosting, which is also called the active cascode. The DC gain of a MOS amplifier depends on the transconductance and the output resistance. Increasing the number of cascoding levels increases the output resistance, but it is limited by the supply voltage and signal-swing requirements. [4] Using an active cascode circuit, as shown in Fig.17, increases the output resistance without increasing the number of cascoding levels.

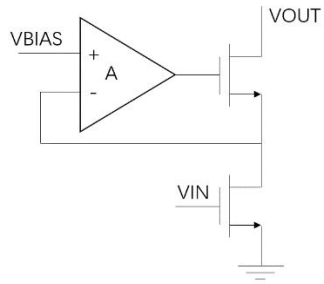


Figure 17. The structure of a gain-boosting technology.

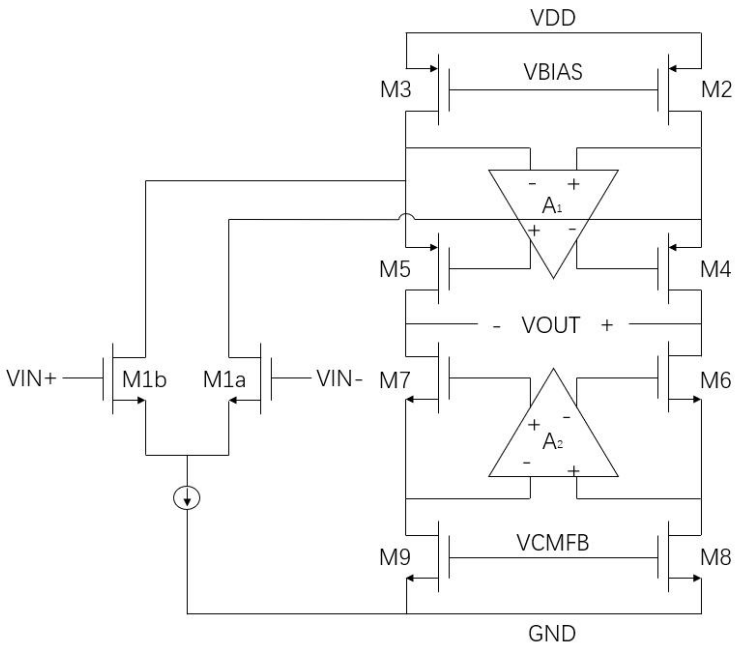


Figure 18. Fully differential folded cascode gain-boosting OpAmp.

Fig. 18 shows the schematic of a typical fully differential folded cascode gain-boosting OpAmp with the gain as shown in (16).

$$G = gm_1[A_1 gm_7 r_{o7}(r_{o1} \| r_{o9}) \| (A_2 gm_5 r_{o5} r_{o3})] \quad (16)$$

where G is the DC gain of the OpAmp, A_1, and A_2 are the gain of two amplifiers. gm_1, gm_5, and gm_7 are the transconductance of the MOS transistors M_1, M_5, and M_7, while r_{o1}, r_{o3}, r_{o5}, r_{o7}, r_{o9} are the corresponding output resistance of the MOS transistors. The advantage of the gain-

boosting OpAmp is the high DC gain because of the gain-boosting structure. However, this structure also consumes more power and produces more noise as a tradeoff.

2.5.3. Two-stage Fully Differential OpAmp

Fig. 19 shows a typical two-stage fully differential OpAmp with the corresponding CMFB circuit shown in Fig. 20 from [4].

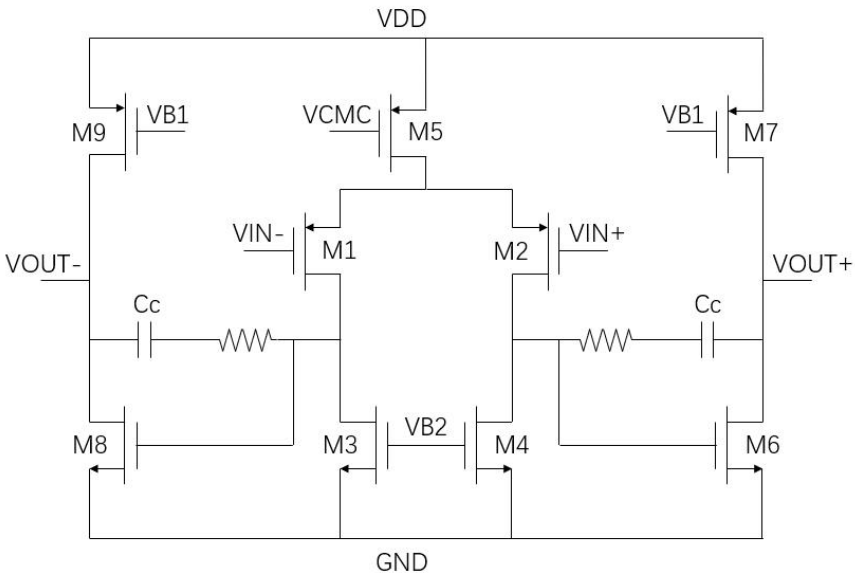


Figure 19. Two-stage fully differential OpAmp.

Two bias voltage VB1 and VB2, are used to ensure all the transistors are working at the correct operating point. VCMC is the compensation voltage from the CMFB to provide the correct CM voltage. In the CMFB circuit shown in Fig. 20, a bias voltage VB3 is used to ensure all the transistors are working at the proper operating point. The MOS transistors M_5 and M_{10} is a current mirror determines the current flow in the OpAmp and the two CM sense differential pair M_{11}, M_{13}, and M_{12}, M_{14}. The gain of the CM sense circuit is negative since the output voltage VCMC is taken from the drain of M_{13} and M_{14}. [4]

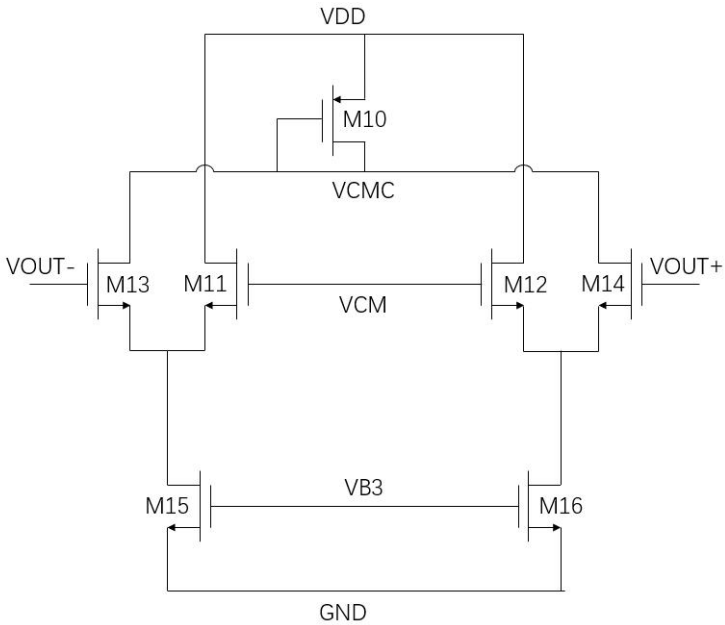


Figure 20. Schematic of the CMFB circuit with two differential pairs.

The gain and the poles are the same as that of a single-end OpAmp, as shown in (11) to (15). The CMFB is used to detect the CM output and compensate it to ensure the correct DC operation point since the two outputs should be fully differential signals. Comparing to the two-stage single-end OpAmp, the fully differential structure has two differential outputs and requires a CMFB circuit. The benefits of the fully differential OpAmp are that the SNR should be 3 dB higher, the impact of the CM interference, and the even-order distortion is reduced due to the fully differential outputs. The CMFB circuit can also use a resistive divider and a CM-sense amplifier as shown in Fig. 21 and Fig. 22. [4]

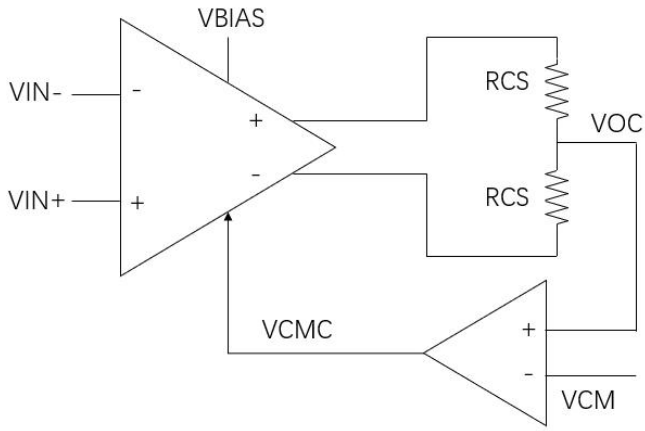


Figure 21. CMFB with resistive divider and CM-sense amplifier.

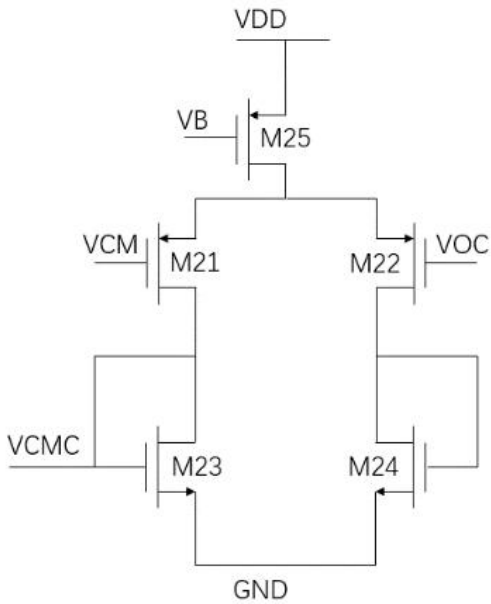


Figure 22. Schematic of the CM-sense amplifier.

3. Modeling and Design

3.1. Overview

The ADC designed in the thesis is an 8-bit fully differential pipelined in 65nm CMOS technology, consists of six 1.5-bit stages, one 2-bit stage, and a digital correction circuit including shift registers, full adders, and an 8-bit DFF. Fig. 23 shows a schematic of the entire ADC. The supply voltage is 1.2V, while the input range is from 200mV to 800mV, with the CM voltage at 500mV. The range of two non-overlap clocks is from 0V to 1.2V. Several digital buffers and inverters are used to generator different clocks to control the comparators in the sub-ADC of each stage. A bias voltage is used to ensure the correct operating points at the CMFB of the fully differential OpAmp, while a bias current is used to control the current flows in both stages of the OpAmp. Three pairs of reference voltages are used for the sub-ADC, comparators, and the DAC, respectively.

The design includes a 1.5-bit Flash ADC, 2-bit Flash ADC, dynamic latch comparator with kickback noise reduction circuit, DAC, MDAC, transmission gate, bootstrapped switch, and several fully differential OpAmp with CMFB circuits. An SHA is also be designed and tested but not included in the final schematic since the resistor type MDAC is replaced by a capacitor type MDAC, which includes the sampling function.

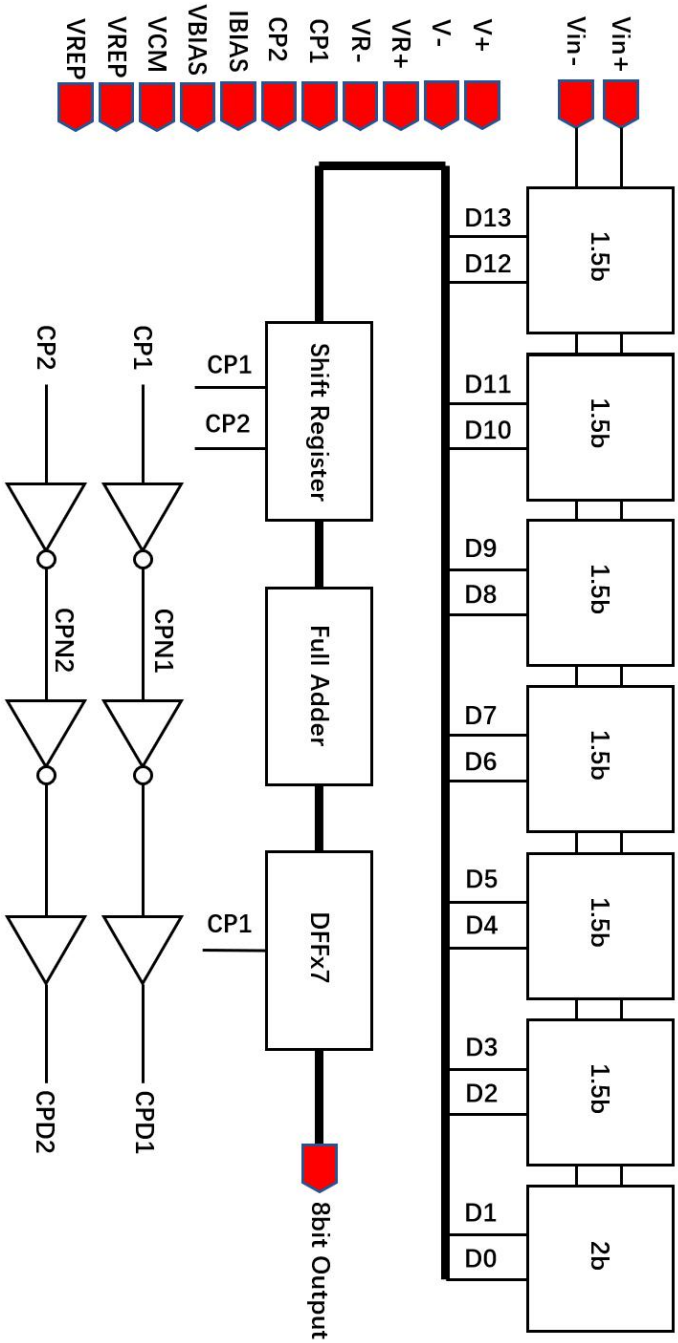


Figure 23. Overview of the 8-bit ADC.

3.2. Pipe-stage

Fig. 24 and Fig. 25 show the structures of the 1.5-bit stage and the 2-bit stage, respectively. Each 1.5-bit stage consists of a sub-ADC to convert two binary bits and an MDAC to generate the residue signal for the next stage. In the end, the 2-bit stage only includes a 2-bit sub-ADC since it is the last stage; no residue signal is required.

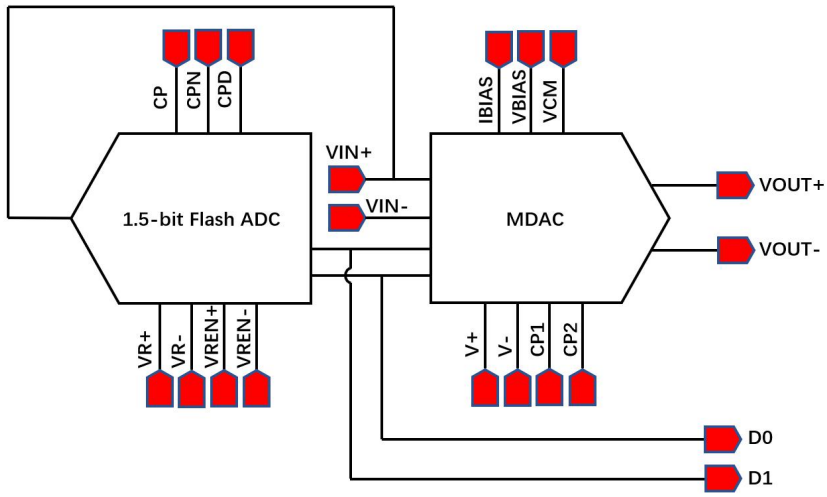


Figure 24. 1.5-bit stage.

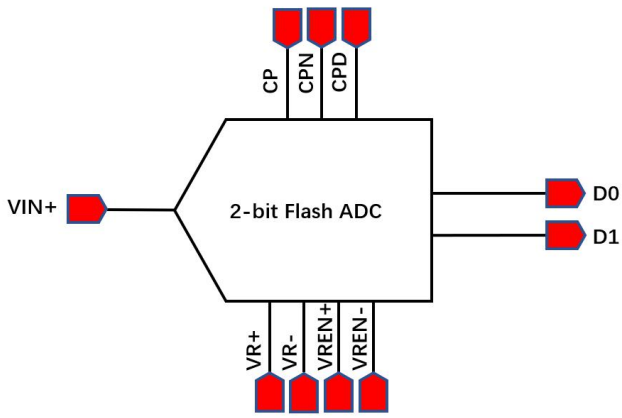


Figure 25. 2-bit stage.

3.3. Transmission Gate and Bootstrapped Switch

In an ADC, many switches are used, especially in the SHA and the capacitor type MDAC. The transmission gate is a straightforward way for switches using MOS transistors. It usually consists of an NMOS and a PMOS in parallel.

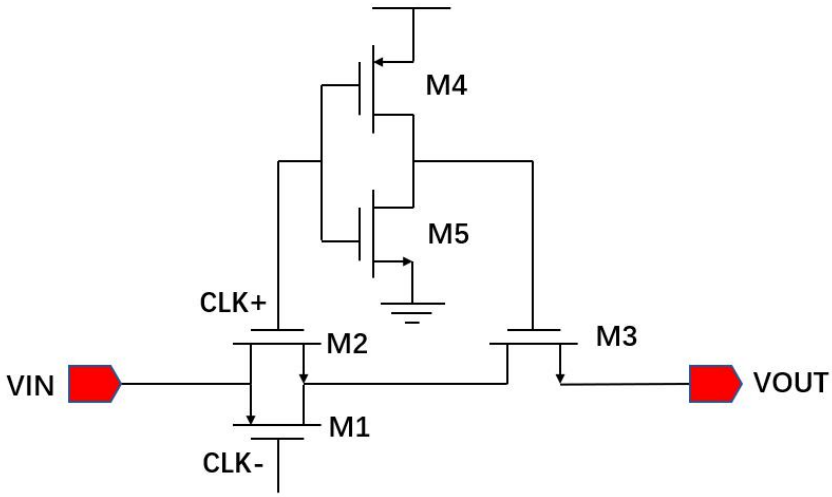


Figure 26. Transmission gate with feedthrough compensation.

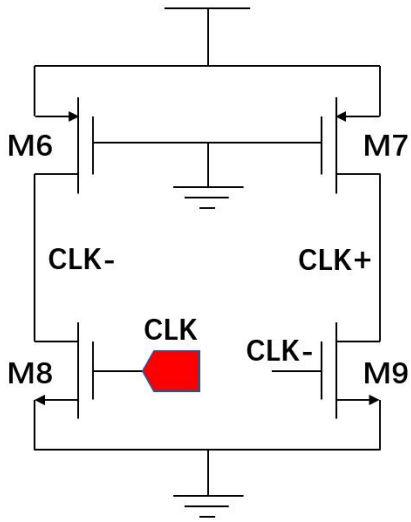


Figure 27. Differential Cascode Voltage Switch Logic (DCVSL).

Fig. 26 shows the schematic of a transmission gate with a dummy MOS transistor to compensate for the clock feedthrough, which makes 50% of the channel charge flows into the sampling capacitor during the switching. [5] But it is not a critical problem for a fully differential design. All the transistors have a minimum length, which is 0.06um. The width of the switch transistors M_1 and M_2 are 30um and 10um, respectively. The width of the dummy transistor M_3 is 5um. The width of the CMOS transistors M_4 and M_5 are keeping the minimum value of 0.135um since they are not important. When the clock signal CLK+ is high and CLK- is low the transmission gate will open, and the input will pass to the output. Since these two clock signals are synchronous inverting signals, both transistors of NMOS and PMOS will open and cut off at the same time. When the transmission gate is off, the dummy MOS transistor M_3 will open, and absorb the feedthrough charges.

The two inverting clock signals are generated by a Differential Cascode Voltage Switch Logic (DCVSL), as shown in Fig. 27. The advantage of this circuit is that it can generate a synchronous inverse clock signal to make sure the PMOS and the NMOS of the transmission gate switching at the same time. This circuit requires two strong NMOS to pull down the output to GND. The widths of the PMOS M_6 and M_7 are 1um, while the widths of the NMOS M_8 and M_{34} are 4um. All the transistors have a minimum length of 0.06um. When the clock signal CLK is high, CLK- will be pull down to GND through M_9. In the meantime, CLK+ will keep a high level since M_7 is open and M_9 is off. The behavior will be the same when the clock signal is low since it is a synchronous design.

The linearity of the switch is important to the ADC to have the same performance at all levels of the full-scale input range. However, the transmission gate will have a linear problem if the input varies when the switch is on. The gate voltage remains at the same level when the clock is high, but the gate-source voltage of the MOS transistor changes with the variation of the input voltage, which produces a variation of the on-resistance that degrades the linearity.

The bootstrapped switch is used to increase the linearity of the switch by maintaining the gate-source voltage of the transistor at the same level to keep the same on-resistance when the input source voltage changes. Fig. 28 shows the schematic of a typical bootstrapped switch with a charge pump. The capacitance in the charge pump should not be too large to charge quickly. Here, the value of the capacitors in the charge pump is 100fp. The gate voltage charges to VDD+VIN when the clock is high, and discharge to GND when the clock is low.

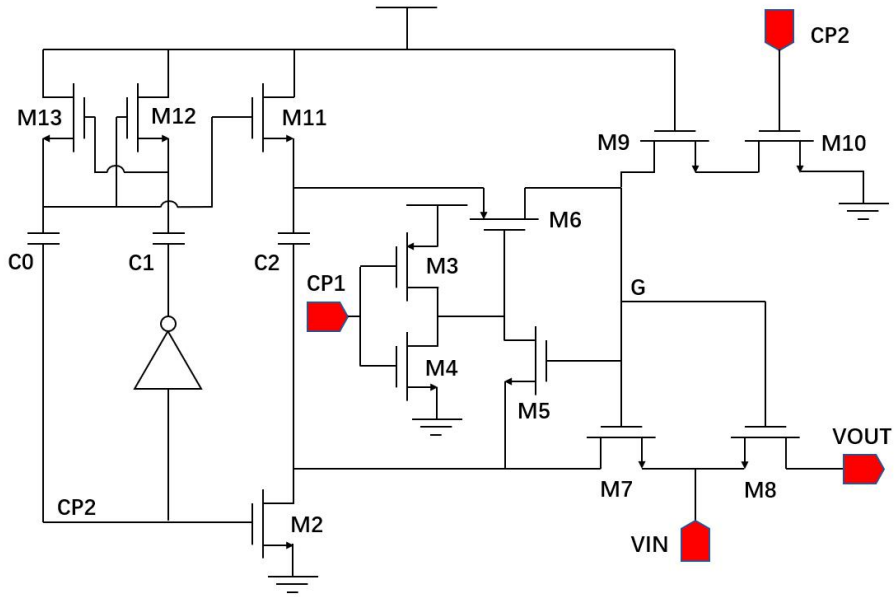


Figure 28. Bootstrapped Switch with charge pump.

All the lengths and widths of the transistors are the minimum value of 0.06um, except for the width of the main switch transistor M_8, which is 2.7um to ensure the switch can handle the full-scale input signals from 200mV to 800mV. When the clock signal CP2 is high, the capacitor C_2 is charged to VDD, the gate voltage of M_8 at node G will be pull down GND through M_9 and M_{10}, then M_5, M_7, and M_8 will be off. In the meantime, CP1 is high, and M_3 is on and M_4 is off. It makes the gate voltage of M_6 is high and close M_6. When the clock signal CP2 is low and CP1 is high, M_6 and M_7 will be on, which makes the capacitor C_2 connecting both the gate and the source of M_8. Then the gate voltage of M_8 will always be VDD+VIN, keeping the on-resistance at the same level during the variation of the input voltage, and increasing the linearity of the circuit.

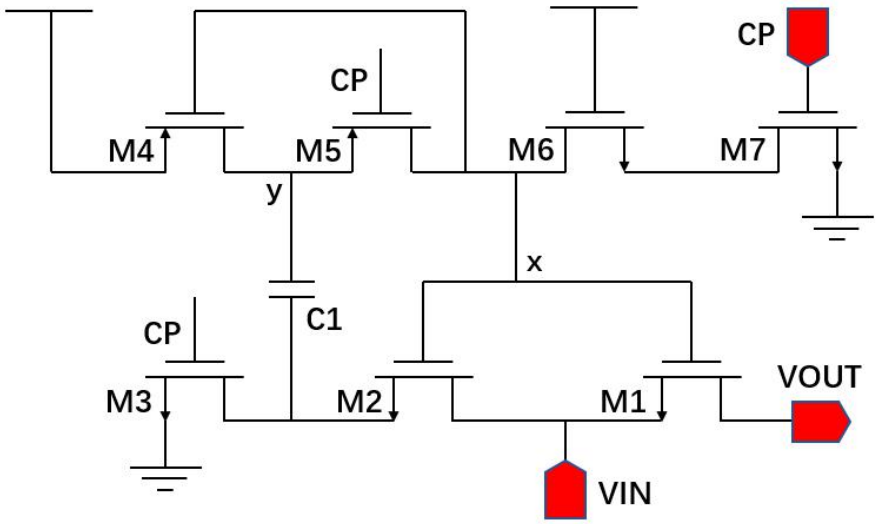


Figure 29. Bootstrapped switch without a charge pump.

However, the charge pump is not necessary, as shown in Fig. 29. [13] The MOS transistor M_1 is the main switch transistor that connects the input and the output. When the clock signal CP is high, M_5, M_7, and M_3 are on, the gate voltage of M_1 at node x discharges to the GND through M_6 and M_7. Then, M_1 and M_2 are off, which turns off the switch. M_4 is on, which charges the capacitor to VDD. When the clock CP signal is low, M_5 and M_2 are on, node x and y is charged to VDD+VIN, ensuring the gate-source voltage of M_1 is always VDD. The gate of M_4 is connected to node x instead of VDD is because node y charges to VDD+VIN and makes the drain of the M_4 become the source and turn on the M_4 when the gate voltage is VDD.

The capacitor C_1 is 100fF, the width of M_2 is 1.35um, and all the other transistors are sized into the minimum size. The width of M_1 is 2.7um, which is dependent on the input range and the load.

3.4. Operational Amplifier (OpAmp)

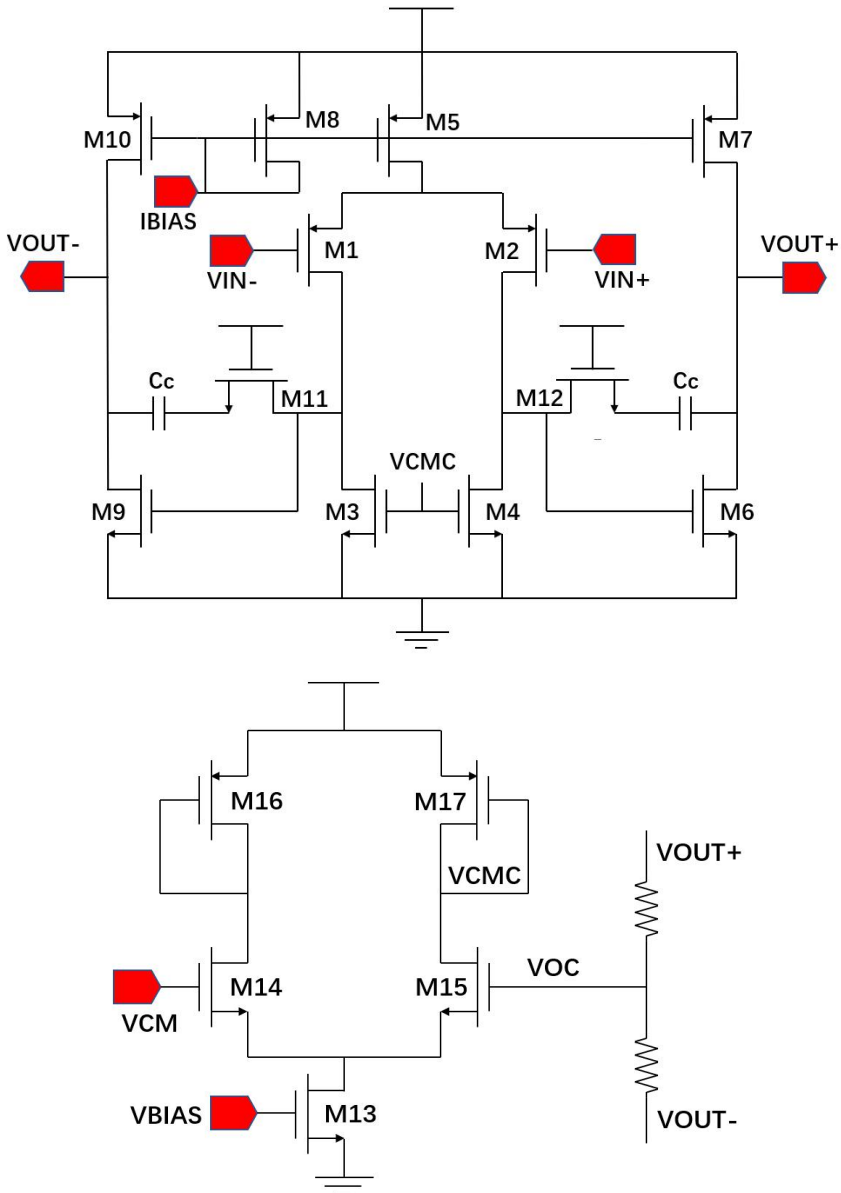


Figure 30. Two-stage fully differential OpAmp with CMFB.

Fig. 30 shows the schematic of the OpAmp, which is one of the most important components in an ADC. The limitation of the speed and the linearity is highly dependent on the OpAmp. Stability is a mandatory specification when designing an OpAmp. The stability is usually dependent on the phase margin; a large phase margin ensures stability and increases the settling time. It is essential to obtain a suitable phase margin. In addition, the tradeoff between the gain and the bandwidth is determined by the design specification and the application. In this thesis, the target is to design a high-speed ADC, which requires a fast-settling time, and large bandwidth. The CMFB circuit in Fig. 30 consists of a resistive divider and a CM sense amplifier. The values of the resistors are 300Ω, which is small enough to avoid a loading issue. In this thesis, four OpAmps have been designed in different sizings as shown in Table 1. The values for the sizings of the transistors are Length/Width, and the units are both um.

Table 1. Sizings for the OpAmps.

	OpAmp 1	OpAmp 2	OpAmp 3	OpAmp 4
M1	400/0.5	1000/0.1	100/0.06	100/0.06
M2	400/0.5	1000/0.1	100/0.06	100/0.06
M3	10/1	480/1.8	300/0.06	300/0.06
M4	10/1	480/1.8	300/0.06	300/0.06
M5	200/1	180/0.06	100/0.06	500/0.06
M6	185/0.5	1300/0.06	400/0.06	400/0.06
M7	800/1	2929/0.52	877.5/0.6	877.5/0.06
M8	200/1	7/0.06	7/0.06	7/0.06
M9	185/0.5	1300/0.06	400/0.06	400/0.06
M10	800/1	2929/0.52	877.5/0.6	877.5/0.06
M11	30/0.06	40/0.06	11/0.06	5/0.06
M12	30/0.06	40/0.06	11/0.06	5/0.06
C1, C2	2p	1p	1p	0.7p

3.5. Comparator

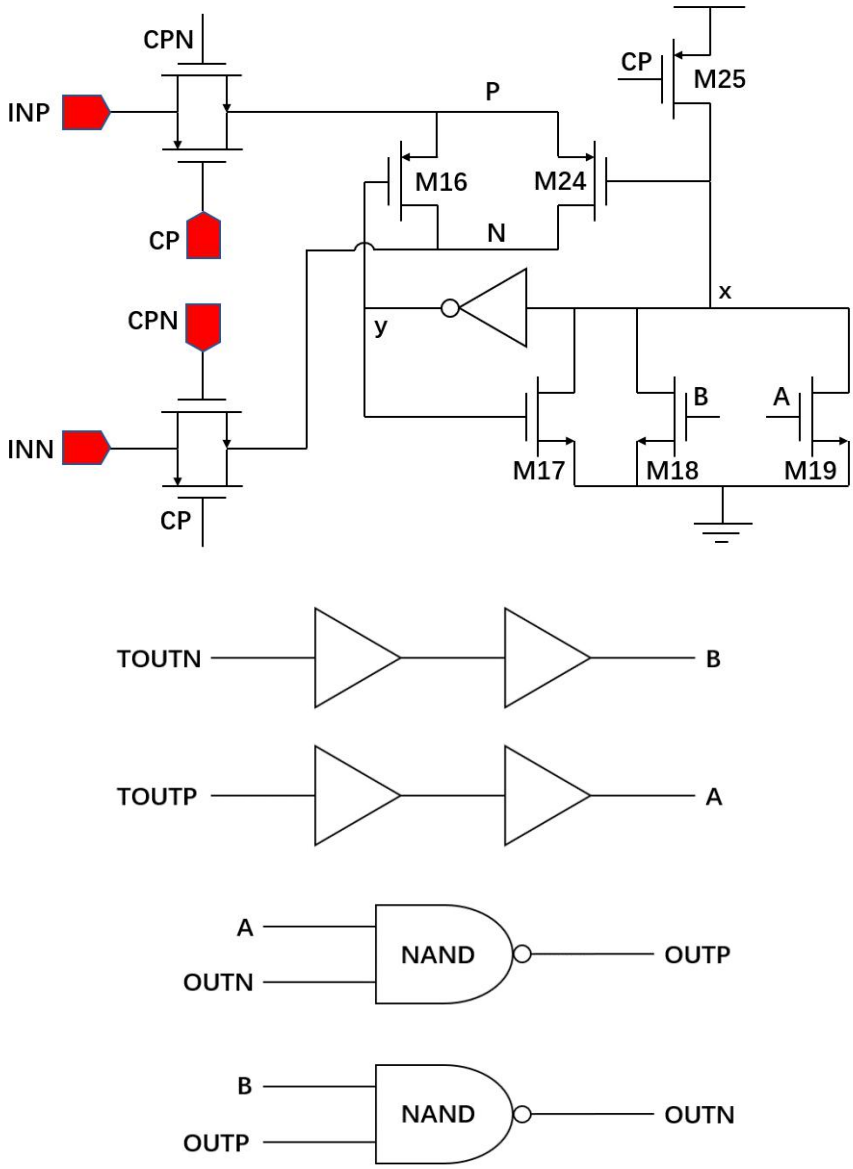


Figure 31. Kickback noise reduction circuit and SR latch.

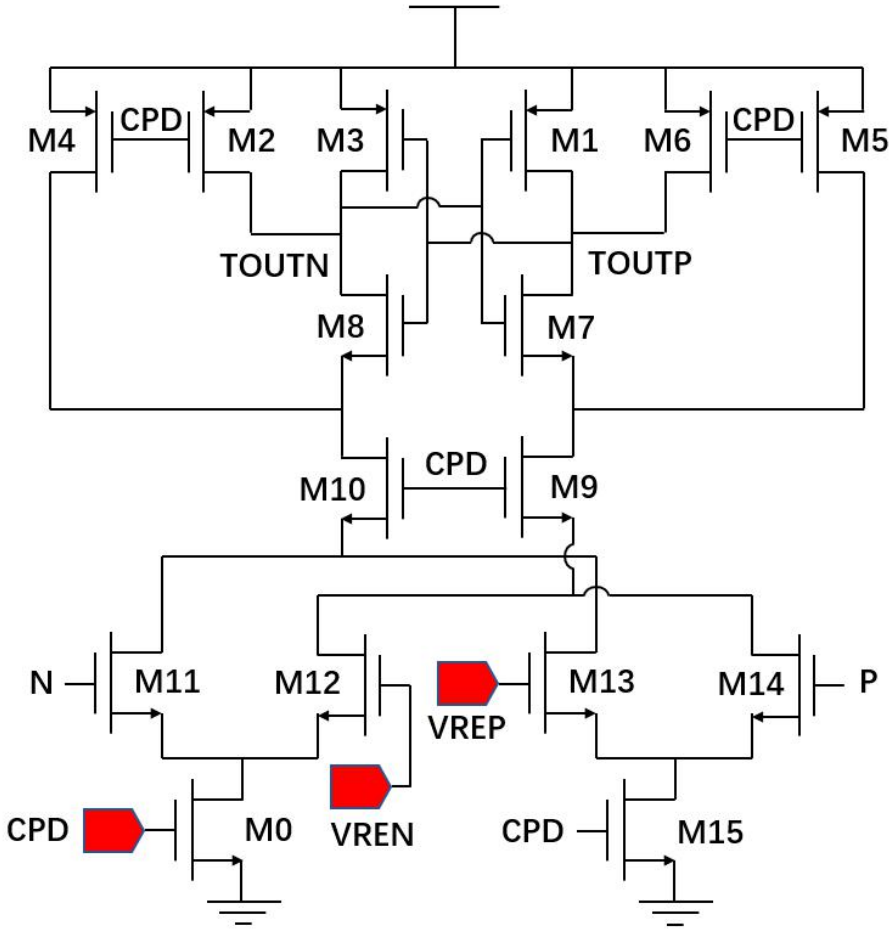


Figure 32. Dynamic latch comparator.

The comparator is also an important component in an ADC, impacting the accuracy and the linearity of the ADC outputs. The dynamic latch type comparator is faster and more power-efficient than the static latch type comparator and the amplifier type comparator. Still, it produces kickback noise at the input node. Fig. 31 shows an SR latch and a typical kickback noise technology bases on [14][15][16][17], which is used to reduce the kickback noise of the dynamic latch comparator, as shown in Fig. 32.

During the reset mode, the clock signal CP is low and CPN is high. The transmission gates are on, passing the inputs to the nodes P and N,

respectively. M_{25} is on and all the other transistors are off. During the regeneration mode, the clock signal CPD is on, the comparator creates outputs bases on the inputs from the nodes P and N. However, in the meantime, the transmission gates are off, which means the regeneration will not impact the input signals. Two reference input signals are used to adjust the thresholds of the comparators. During the reset mode, all the outputs will be reset to zero, and the SR latch is used to keep the output value during the reset mode. All the transistors are using a minimum length. The widths for NMOS and PMOS of the transmission gates are 2um and 5um, respectively. All the other sizings for the transistors are shown in Table 2.

Table 2. Sizings for the comparator.

transistors	Width (um)	transistors	Width (um)
M1, M3	0.2	M13, M14	4
M2, M6	1.1	M0, M15	2
M4, M5	2	M16, M24	35
M7, M8	1.2	M17	1
M9, M10	4	M18, M19	1
M11, M12	4	M25	10

Fig. 33 shows the three-clock signal used in the comparator and the corresponding kickback noise reduction circuit. The clock signal CP is one of the two non-overlap clocks depend on the stage number, while CPN is the inversion of CP, and CPD is a delayed version of CP. CP and CPN are used in the kickback noise reduction circuit, while CPD is used in the dynamic latch comparator since the signal from OpAmp has a settling time, as shown in Fig. 34. Using a delayed clock signal in the comparator can reduce the impact of the settling time and make sure the comparator is processing the correct inputs.

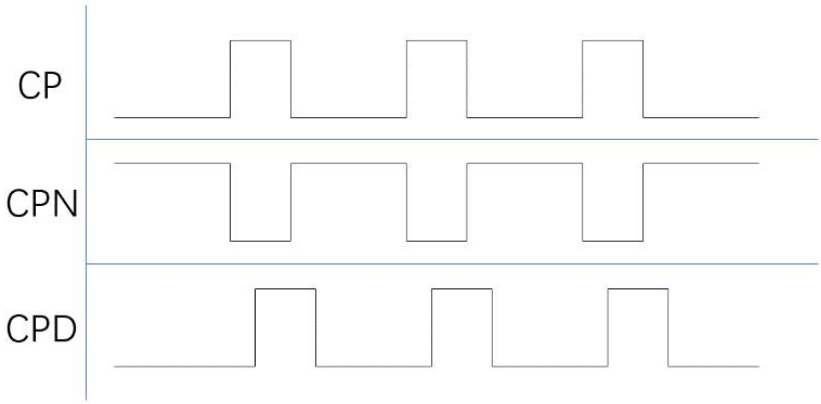


Figure 33. Three clock signals.

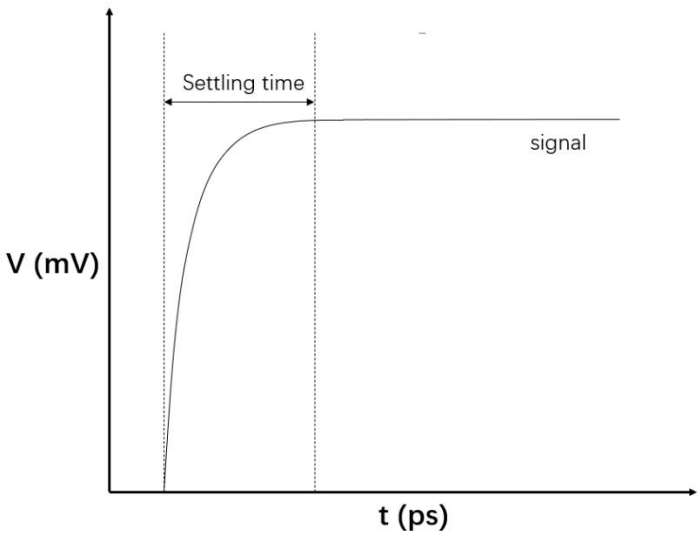


Figure 34. Settling time.

3.6. Flash ADC

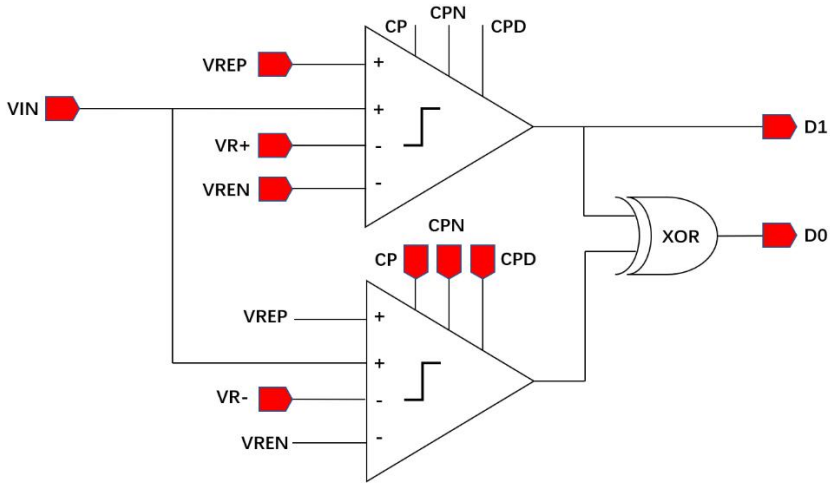


Figure 35. 1.5-bit Flash ADC.

Fig. 35 shows the schematics of the 1.5-bit FLASH ADC. In each 1.5-bit stage, two comparators are used to divide the input into three parts based on these two comparisons. For the full scale of the input, the range is from 200mV to 800mV. The thresholds of the 1.5-bit Flash ADC are 425mV and 575mV. Table. 1 shows the two-bit binary outputs of the 1.5-bit Flash ADC with the corresponding input ranges, while Table. 2 shows the results for the 2-bit Flash ADC.

Table 3. The binary output of the 1.5-bit Flash ADC.

200mV to 425mV	00
425mV to 575mV	01
575mV to 800mV	10

Table 4. The binary output of the 2-bit Flash ADC.

200mV to 350mV	00
350mV to 500mV	01
500mV to 650mV	10
650mV to 800mV	11

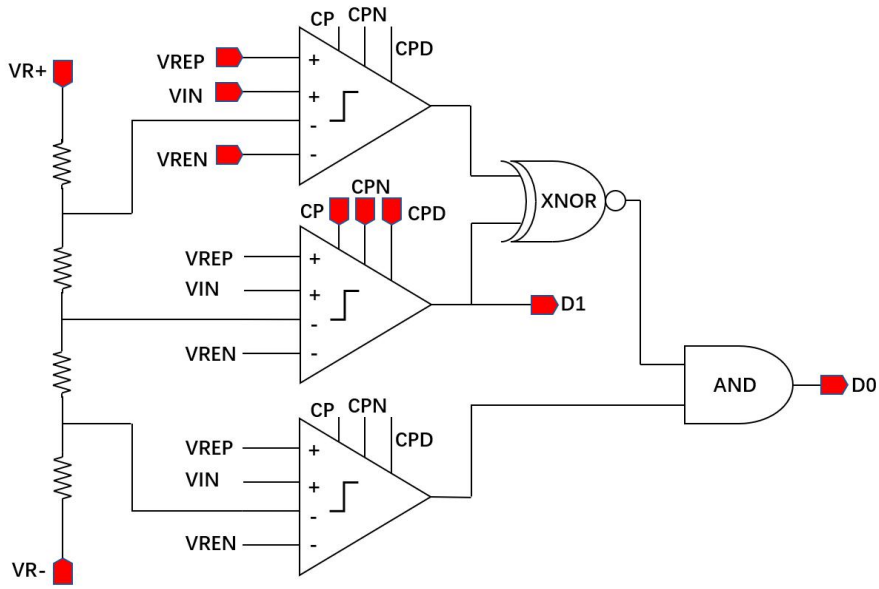


Figure 36. 2-bit Flash ADC.

Fig. 36 shows the schematics of the 2-bit FLASH ADC, which requires three comparators to divide the input signal into four parts with a two-bit binary output. The four resistors should be equal to generate three threshold voltages, which are 650mV, 500mV, and 350mV.

3.7. DAC

In each 1.5bit stage, the DAC is used to generate a compensation voltage for the residue signal to remain in the same voltage range after the multiplication during the operating of the MDAC. The input range is from 200mV to 800mV. When signal voltage is in the range of 200mV to 425mV, the binary outputs are 00; the DAC output should be 650mV. When signal voltage is in the range of 425mV to 575mV, the binary outputs are 01, then the output of the DAC should be VCM, which is 500mV. When signal voltage is in the range of 575mV to 800mV, the binary outputs are 10; the DAC output should be 350mV.

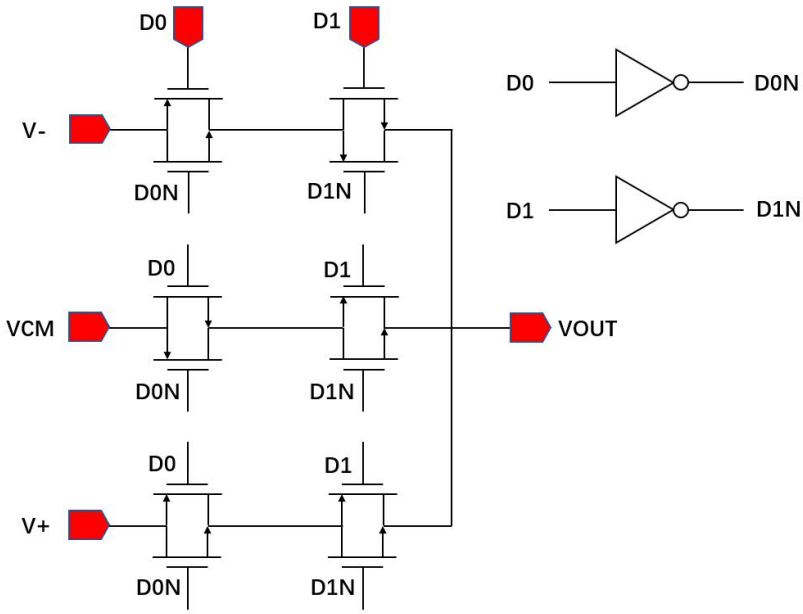


Figure 37. Schematic of the DAC.

Fig. 37 shows the schematic of the DAC consists of six transmission gates controlled by the two binary inputs. Firstly, two invertors are used to generate two inverting digital signals corresponding to the inputs. Two digital inputs and their inverting signals will control these six transmission gates from three roads and make sure only one road can pass the signals to the output. For example, V+ will pass the voltage level to the output if the digital inputs are 00. VCM will pass the voltage level to the output if the digital inputs are 01. V- will pass the voltage level to the output if the digital inputs are 10. All the lengths of the transistors are 0.12um, while the widths are 100um. The sizings are dependent on the load and the input range of the circuits. Usually, the DAC uses a resistive divider to make different voltage levels. However, in this design, the inputs are directly connected to three separate pins. It will be easy to adjust the output of DAC by manipulating the voltage levels in these pins.

3.8. SHA

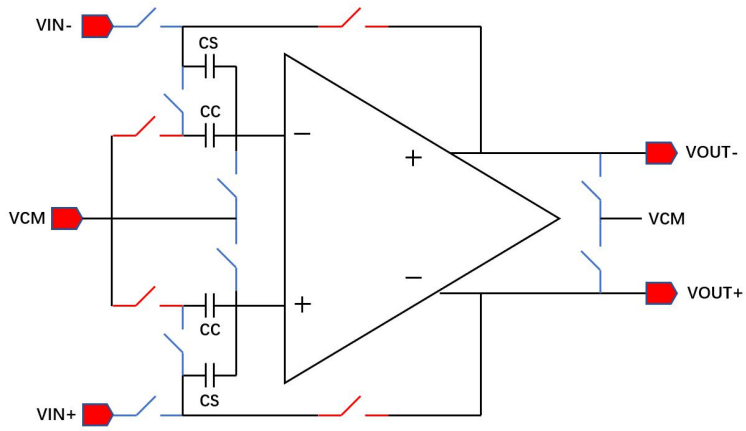


Figure 38. Schematic of SHA.

Fig. 38 shows the schematic of the SHA, which is used to sample the signal and hold the value during the processing. The operation of the SHA can be divided into two-phase. During the sampling phase, the schematic is equivalent to the structure shown in Fig.39, while Fig. 40 shows the structure during the holding phase.

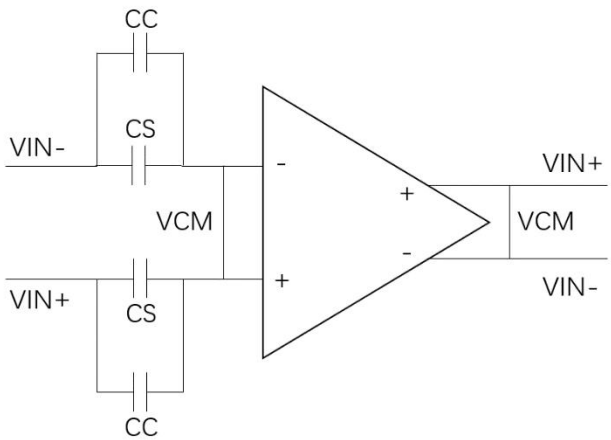


Figure 39. SHA during the sampling phase.

During the sampling phase, The sampling capacitors CS and the compensation capacitors CC are charged to the input voltages. Both inputs and outputs are connected to the CM voltage VCM. CS is connected to the negative feedback loop during the holding phase, while CC is connected to the VCM. The compensation capacitors CC is used to compensate for the gain of the OpAmp. Ideally, without CC the input voltage and the output voltage fulfill (17), which makes the circuit a unit gain buffer.

$$C_S V_{in} = C_S V_{out} \tag{17}$$

But, with the finite gain of the OpAmp, the gain of the circuit is less than 1. By using compensation capacitors, the output voltage is shown in (18).

$$V_{out} = \frac{a}{1 + \frac{aC_C}{C_S + C_C}} V_{in} \tag{18}$$

where $\frac{a}{1+\frac{aC_C}{C_S+C_C}}$ is the closed-loop gain A of the circuit, which is less than 1, a is the open-loop gain of the OpAMp, Cc is the compensation capacitance, Cs is the sampling capacitance, and $\frac{C_C}{C_S+C_C}$ is the feedback factor f. Ideally, the closed-loop gain $\frac{a}{1+a}$ should be 1 to perform as a unity gain buffer with the open-loop gain a is infinite. The compensation capacitor is used to compensate the finite gain of the OpAmp to ensure the gain of the circuit is 1, and the output voltage equals the input voltage stored in the capacitors.

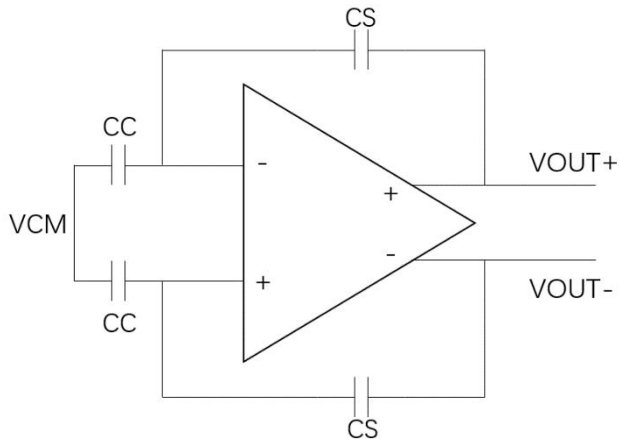


Figure 40. SHA during the holding phase.

However, the SHA is not included in the final schematic. Because the sampling function is included in the capacitor type MDAC, which will be discussed in the next section.

3.9. MDAC

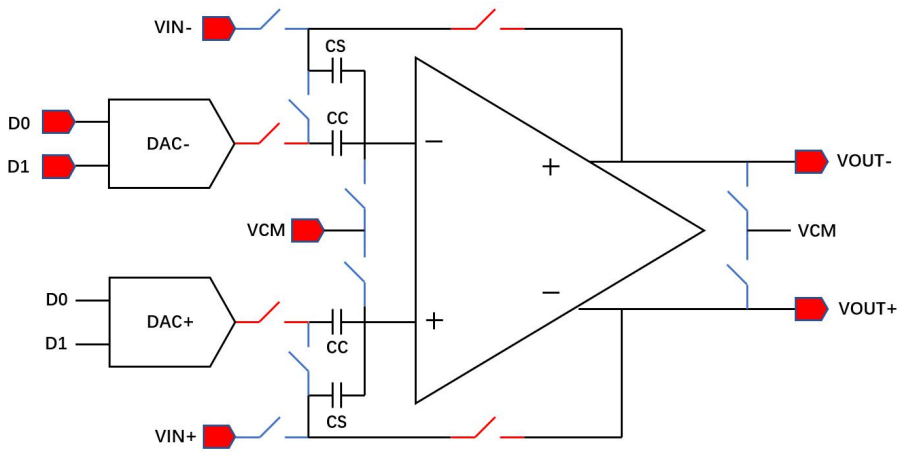


Figure 41. Schematic of the capacitor type MDAC.

In each 1.5-bit stage, the MDAC is used to generate a residue signal to the next stage bases on the input and the binary output of the current stage. Fig. 41 shows the schematic of the capacitor type MDAC, which separates the charging phase and the operating phase. The switches in blue are used for sampling, and the switches in red are used for operating.

During the charging phase, the equivalent circuit is the same, as shown in Fig 39. The sampling capacitors and the compensation capacitors are charged to the input voltages for the sampling.

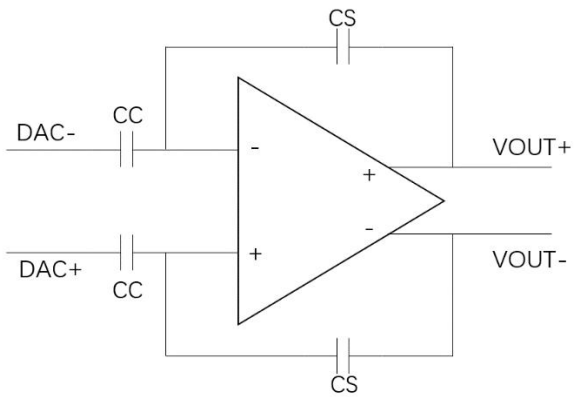
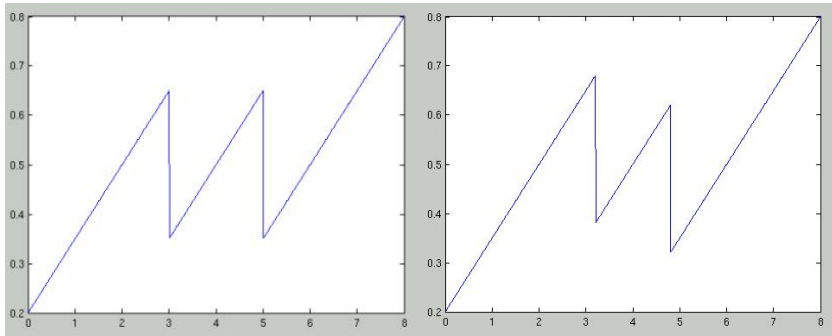


Figure 42. MDAC during the operating phase.

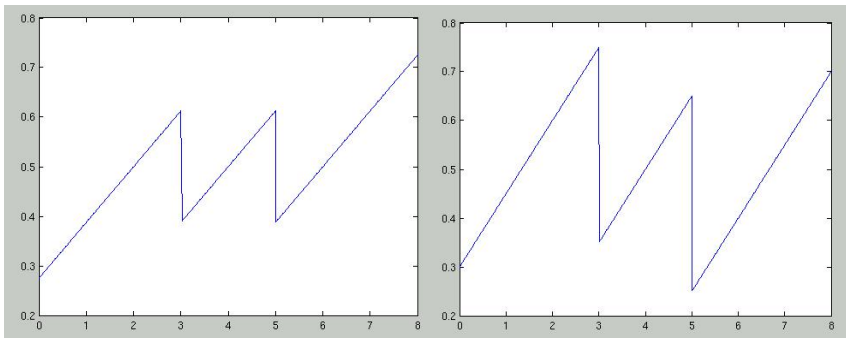
During the operating phase, the equivalent circuit is shown in Fig. 42. Compared to Fig. 39, the inputs are connected to the DAC outputs instead of the CM voltage VCM. Then, (18) should be rewritten as (19), and the output voltage becomes

$$V_{out} \approx \frac{C_S + C_C}{C_S} V_{in} + \frac{C_C}{C_S} V_{DAC} \tag{19}$$

where V_{DAC} is the output of the DAC, ideally, the capacitance of C_C should equal C_S to make a gain of 2. But, to compensate for the finite gain of the OpAmp, C_C should be smaller than C_S. Fig. 43 (a) shows an ideal residue signal of the 1.5-bit stage with a ramp signal from 200mV to 800mV.



(a) (b)



(c) (d)

Figure 43. (a) The ideal transformation of the MDAC in a 1.5-bit stage. (b) Transformation with an error in the comparisons. (c) transformation with a gain error. (d) transformation with an error in the DAC outputs.

Fig. 43(b) shows the transformation of the MDAC with the gain error, Fig. 43(c) shows the transformation with an error in the comparisons of the Flash ADC, Fig. 43(d) shows the transformation with an error in the DAC. These three common errors of the residue signal generated from the MDAC should be avoided for the ADC design.

4. Simulation and Results

4.1. Bootstrapped Switch Test

The testing of the bootstrapped switch is using a 1.2V supply voltage and 100MHz clocks with 500fF capacitors as load. The test signals are two differential 13MHz sinusoidal signals from 200mV to 800mV with a CM voltage of 500mV and two differential ramp signals. The results are shown in Fig. 44 and Fig. 45, respectively. The red and pink curves are the inputs, the green and blue curves are the outputs, and the purple and yellow curves are the gate voltage of the main transistors.

The bootstrapped switch without the charge pump in Fig. 29 has also been tested by the sinusoidal signal, and the result is shown in Fig. 46. The red curve is the input, while the green curve is the output. The blue curve represents the gate voltage of the main transistor. The performance of the two bootstrapped switches is similar, and both keep the gate-source voltage remains at the same level when the input signal varies.

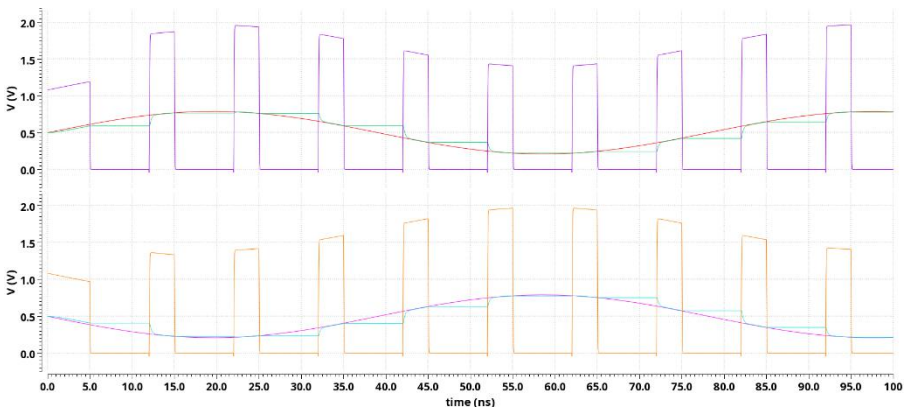


Figure 44. Sinusoidal test for the bootstrapped switch.

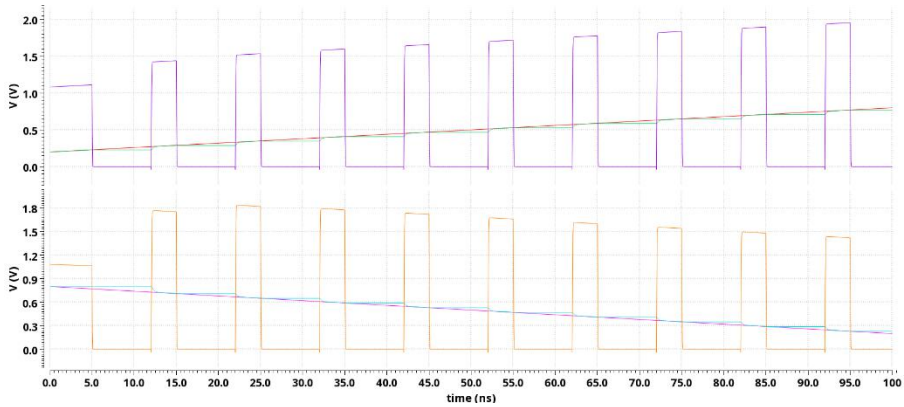


Figure 45. Ramp test for the bootstrapped switch.

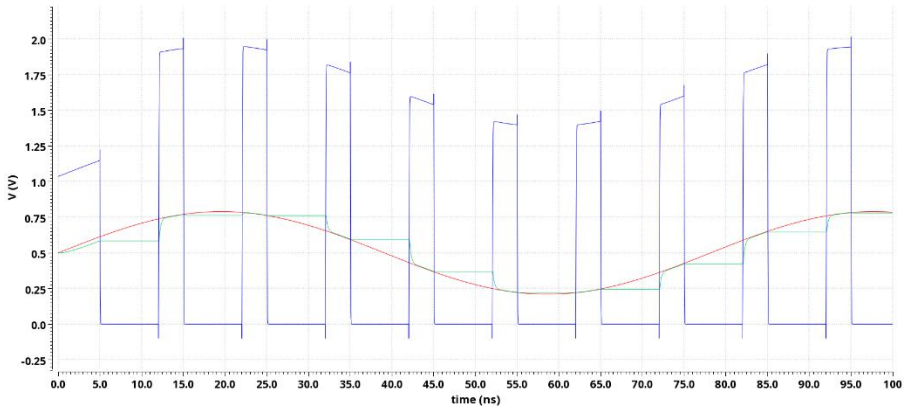


Figure 46. Sinusoidal test for the bootstrapped switch in Fig.29.

For the switch in Fig. 26, the total current consumption is 0.42mA, and the total power consumption is 0.50mW. For the bootstrapped switch in Fig. 28, the total current consumption is 9.68uA, and the total power consumption is 11.62uW. However, for the bootstrapped switch without the charge pump in Fig. 29, the total current consumption is 0.67uA, and the total power consumption is 0.80uW. The performance of these two bootstrapped switches is similar, but the last one consumes less power.

4.2. OpAmp Test

The testing of the OpAmp is using a 1.2V supply voltage. The CM voltage is 500mV; the bias voltage is 404mV, the bias current is 500uA. The inputs are two differential sinusoid signals from 10Hz to 10GHz with two 500fF capacitors as load. Fig. 47 to Fig. 50 show the simulation results of 4 OpAmp with different sizing, while the red curves are the gain, the green curves are the phase. The performance is shown in Table 5 includes gain, bandwidth, Unit Gin Frequency (UGF), and Phase Margin (PM).

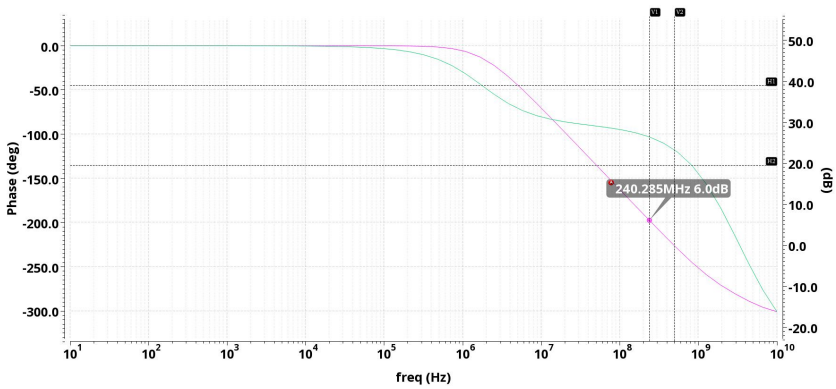


Figure 47. AC test for the 1st OpAmp.

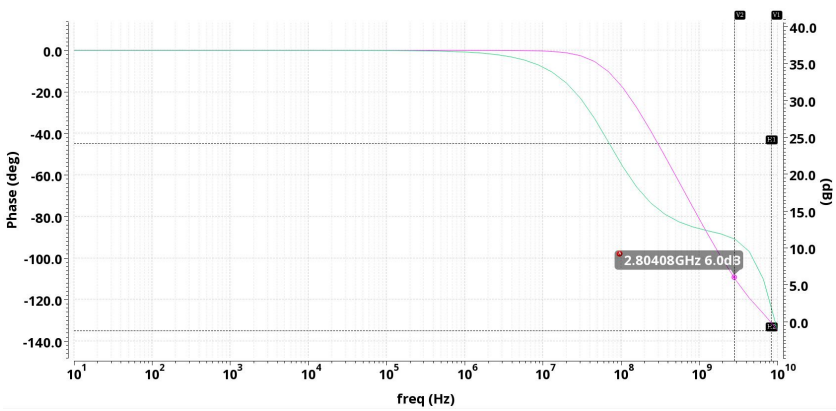


Figure 48. AC test for the 2nd OpAmp.

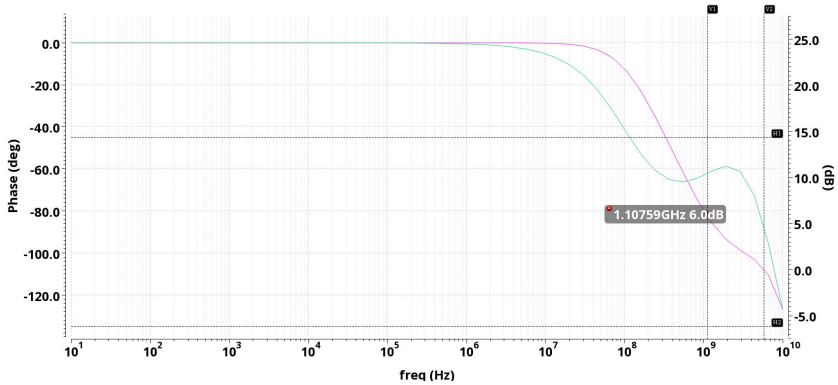


Figure 49. AC test for the 3rd OpAmp.

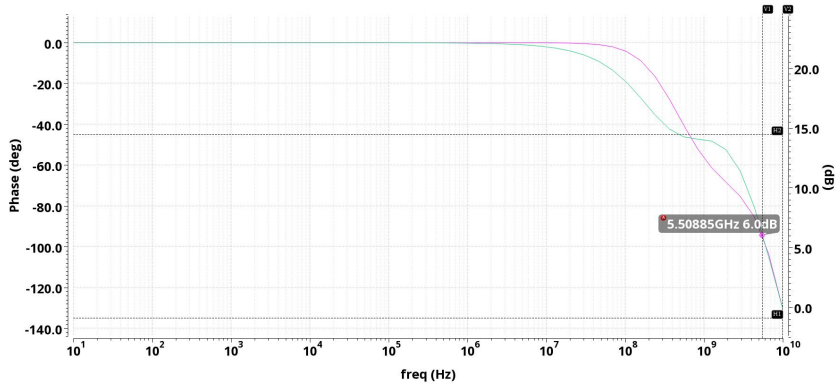


Figure 50. AC test for the 4th OpAmp.

Table 5. Parameter of the OpAmp.

	No.1	No.2	No.3	No.4
Gain (dB)	48.60	36.79	24.59	22.13
Bandwidth(Hz)	1.78M	71.48M	118.20M	497.24M
UGF (Hz)	498.15M	8.32G	5.833G	9.926G
PM (deg)	62.18	57.68	92.37	87.00
Power (mW)	5.68	99.15	29.79	31.13

4.3. Comparator Test

The testing of the comparator is using a 1.2V supply voltage. The clocks are two non-overlapped clock signals; VREP and VREN are used to compensate for the offset voltage. The clock port CPD is used to reduce the impact of the settling time of the OpAmp. It is not used in the test bench since the comparator is not connected to an OpAmp. The total current consumption is 1.98mA, and the total power consumption is 2.38mW for two comparators.

The simulation results are shown in Fig. 51 and Fig. 52, the reds and green curves are the inputs, the pink curves are the positive outputs, and the light blue curves are the clock.

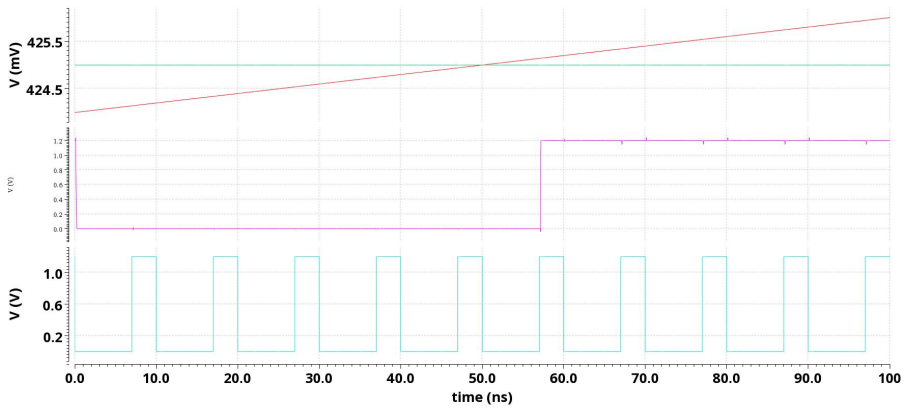


Figure 51. Comparison at 425mV.

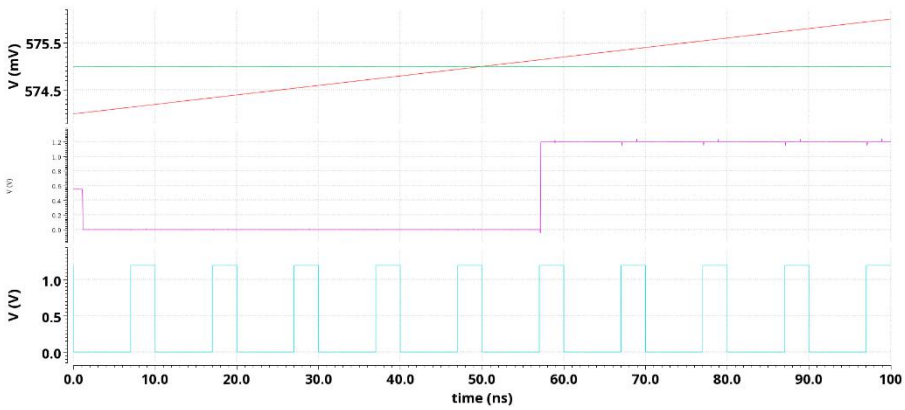


Figure 52. Comparison at 575mV.

4.4. SHA Test

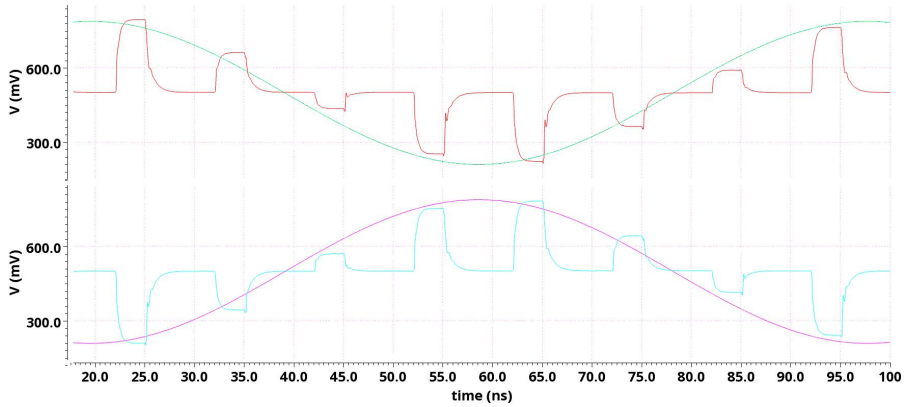


Figure 53. Simulation result of the SHA.

The testing of SHA is using a 1.2V supply voltage, two differential 13MHz sinusoid signals as inputs, and two 500fF capacitors as load; the results are shown in Fig 57. The green and pink curves are the differential inputs, while the red and light blue curves are the differential outputs.

SHA is not included in the final design. The sampling function is included in the MDAC and the comparators. In addition, using SHA the circuits will consume more power, and decrease the speed. It can also produce a gain error and a non-linearity problem because of the OpAmp used in SHA.

However, it is easier to compensate the capacitors in SHA since the gain should be 1, which means the output should equal the sampling input. In MDAC, the gain is 2, and it is difficult to compensate the capacitors. In this design, the sampling capacitances are 100f, while the compensation capacitances are 78f.

4.5. Flash ADC Test

Fig. 54 and Fig. 55 show the simulation results of the 1.5-bit Flash ADC and the 2-bit Flash ADC with a 1.2V supply voltage, respectively. The red curves are the inputs, the pink curves are the first binary outputs, the light blue curves are the second binary outputs, and the yellow curves are the clock. The comparison can only be made when the clock goes up to VDD.

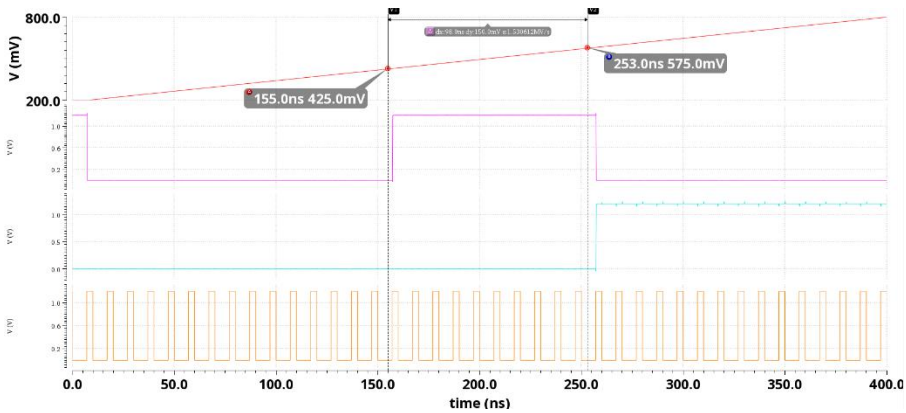


Figure 54. Simulation results of the 1.5-bit Flash ADC.

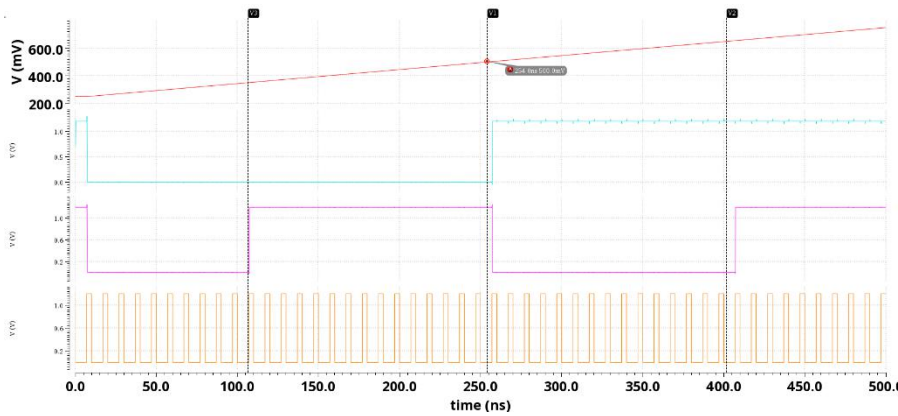


Figure 55. Simulation results of the 2-bit Flash ADC.

4.6. MDAC Test

The error from the MDAC is usually critical to the Pipelined ADC. Only a correct residue signal between one stage to another can ensure the correctness and the quality of the ADC. Fig. 56 shows the simulation results of the residue signals generated by the MDAC of two differential ramp input signals. The red and the green curves are the two differential inputs, while the pink and the blue light curves are the differential outputs. The output is generated during the processing phase and resets to the CM voltage during the reset phase.

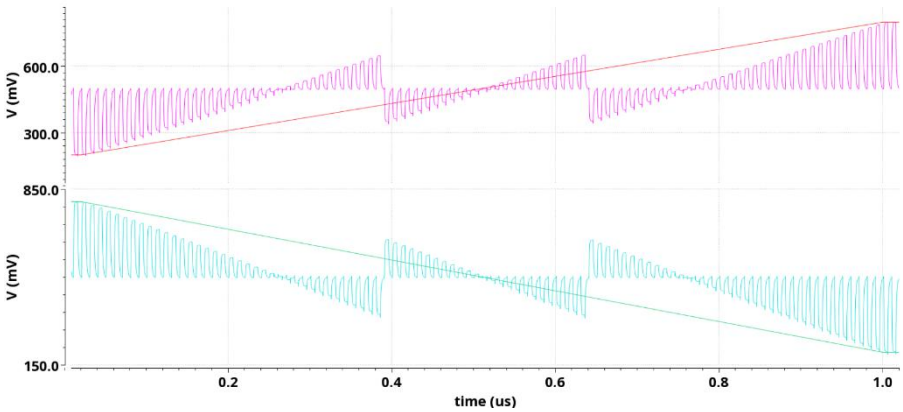


Figure 56. Simulation results of the MADC.

4.7. Ramp Test

Since all the blocks have been tested and all the results are as expected, the test ramp test is used to test the entire pipelined ADC with a ramp signal from 200mV to 800mV within 12.8μs to make sure each output can keep five clock cycles of a 100MHz sampling rate, theoretically. Fig. 57 shows the simulation result of the ramp test with the input in the red curve and the output in the light blue curve. The output signal is converted by an ideal 8-bit DAC of the 8-bit binary code from the pipelined ADC. And the data is recorded and saved in the .dat format for processing of MATLAB.

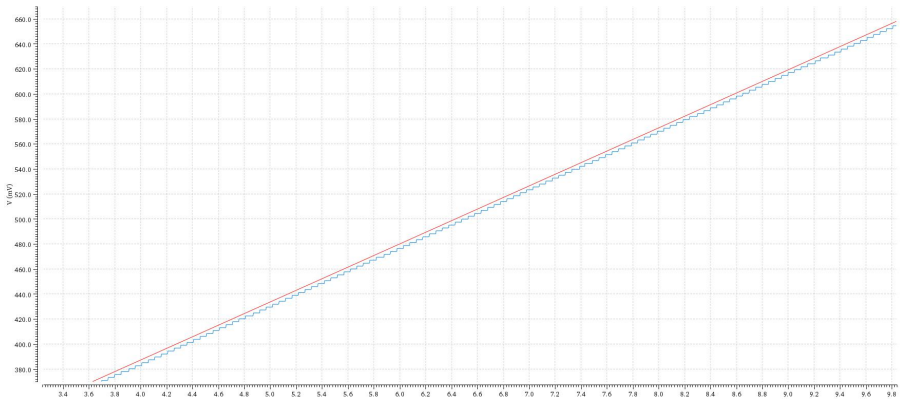


Figure 57. Simulation result of the ramp test.

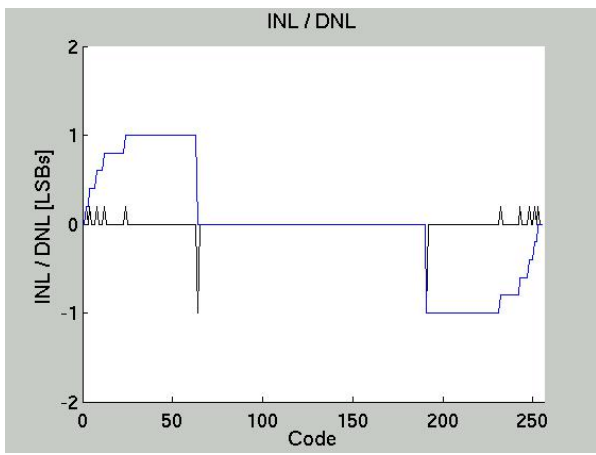


Figure 58. INL and DNL of the ramp test.

Fig. 58 shows the INL and the DNL results of the ramp test by MATLAB. The black curve is the DNL result, while the blue curve is the INL result. The non-linearity is usually inevitable, resulting from the error in the Flash ADC or the MDAC. Fig. 59 and Fig. 60 show the residue signals of the first stage near the breakpoints 425mV and 575mV, respectively. The red curves are the input signal. The blue light curves are the non-inverting output, and the purple curves are the inverted output. The input is marked when the voltage reaches 425mV and 575mV, respectively.

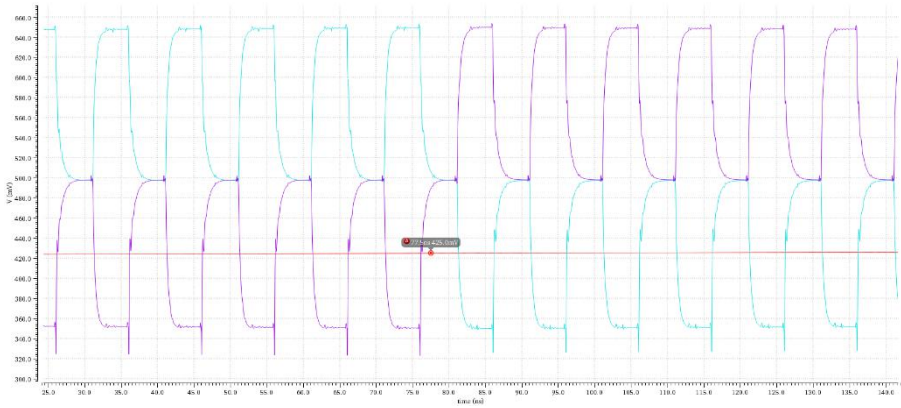


Figure 59. Outputs from the first stage at 425mV.

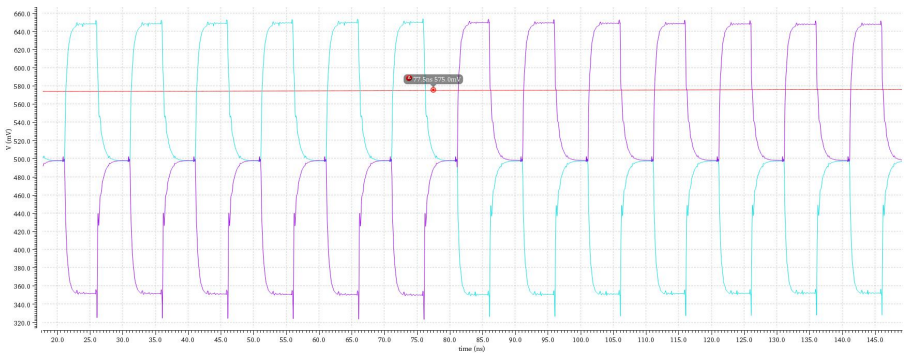


Figure 60. Outputs from the first stage at 575mV.

For a pipelined ADC, the first two stages are usually more important than the others. Fig. 61 and Fig. 62 show the outputs of the second stage near the breakpoint 312.5mV and 387.5mV. The red curves are the input signal. The blue light curves are, and the purple curves are the differential outputs from the first stage, and the yellow curves are the non-inverting output from the second stage. As can be seen, the residue signal from the second stage switches when the residue signal from the first stage reaches 425mV and 575mV. Fig. 63 shows the input of the last stage in a yellow curve and the output of the first stage in the first stage.

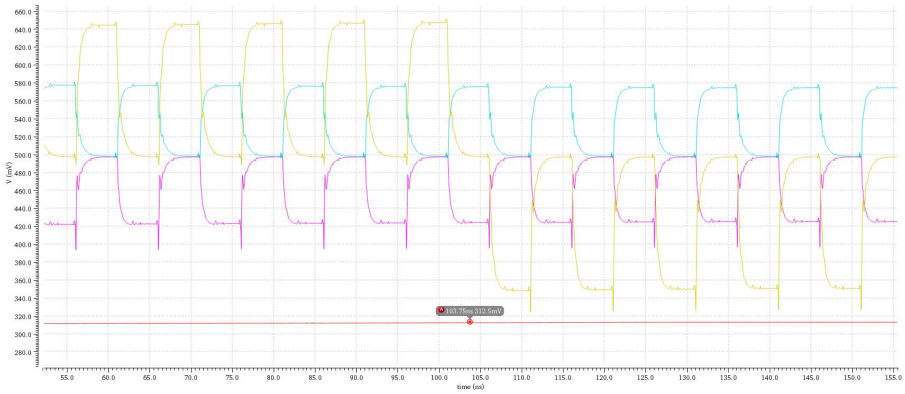


Figure 61. Outputs of the first two stages at 312.5mV.

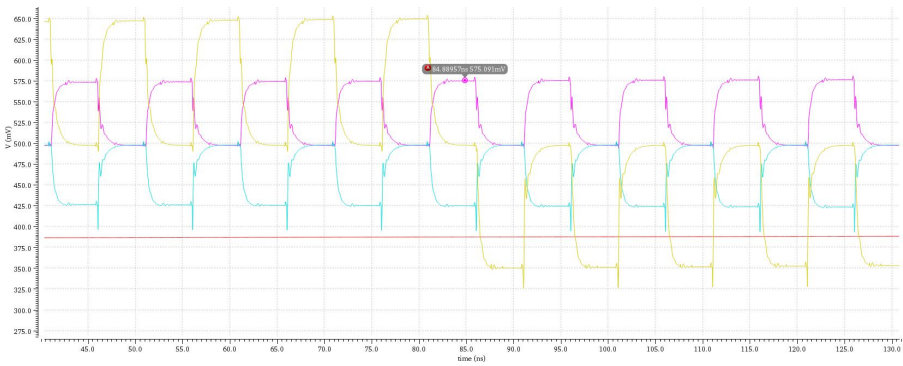


Figure 62. Outputs of the first two stages at 387.5mV.

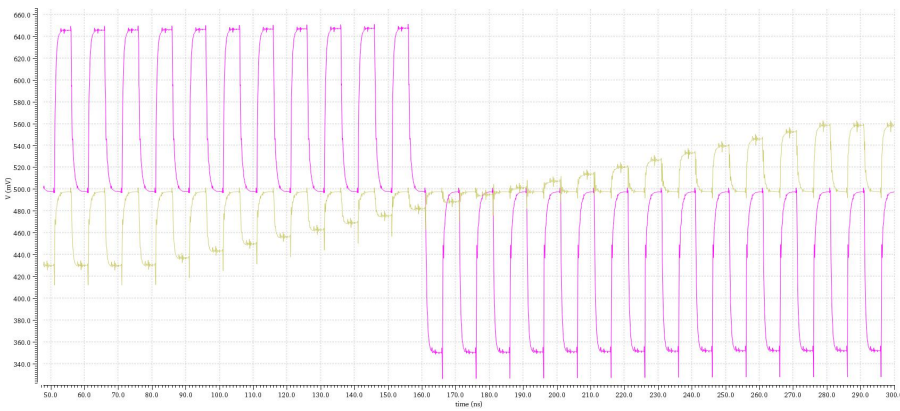


Figure 63. The input of the last stage at 425mV

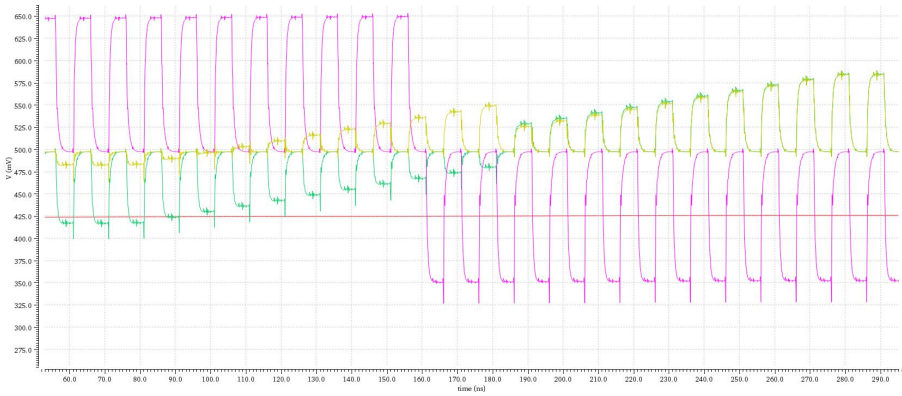


Figure 64. The inputs of the last stage with errors at 425mV.

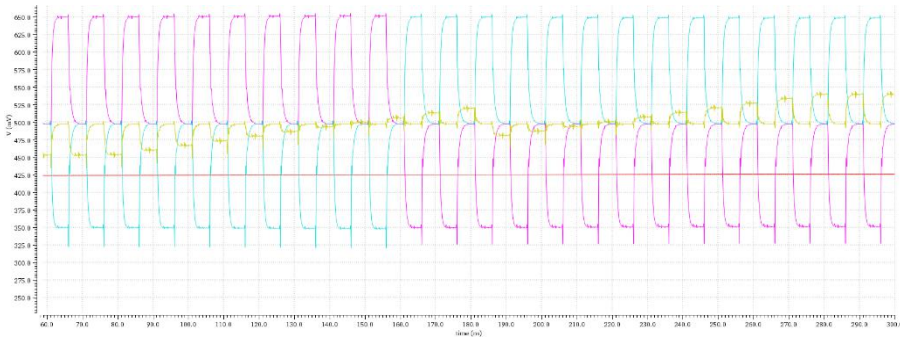


Figure 65. The inputs of the last stage with gain error at 425mV.

Fig. 64 shows the input of the last stage with gain error in the green curve, and the yellow curve represents the input with an error in reference voltage of the DAC, while the red curve is the input, and the pink curve is the output of the first stage. When the gain is too large, it is hard to see in the first two stages, but it is obvious in the last stage, as shown in Fig. 65. The red curve is the input, the pink and the light blue curve are the differential output of the first stage, and the yellow curve is the input of the last stage. It can cause a problem at some breakpoints when the gain is larger than expected, as shown in Fig. 65. The input across the 500mV three times can lead to an error in the last two bits. After fixed these problems in Fig. 64 and Fig. 65, the input of the last stage is shown in Fig. 63.

4.8. Single Tone Test

Fig.66 shows the simulation results of the single tone test, the red curve is the input sinusoid signal of 1.26MHz with a 100MHz sampling rate, and the green curve is the output of the ADC.

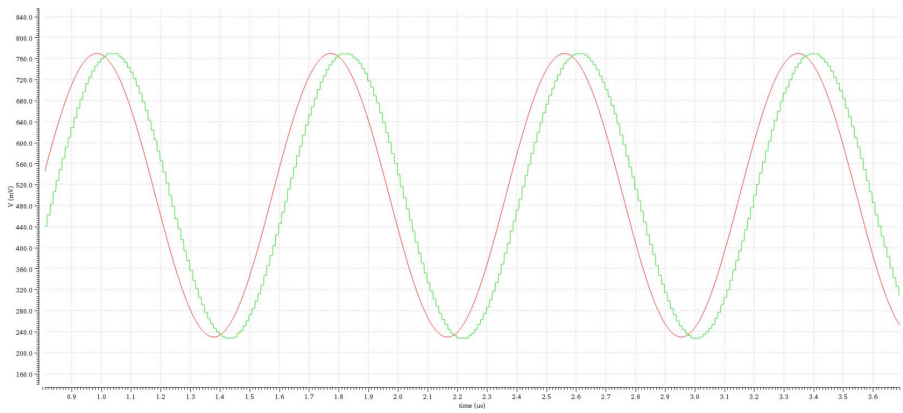


Figure 66. Simulation result of the single tone test with low frequency.

The ADC inputs are all set as 13/1024×FS for different sampling rates, where FS is the sampling frequency. The testing sampling rate includes 100MHz, 200MHz, and 250MHz. The simulation results show that the ADC is not able to work with a sampling rate higher than 300MHz, and the performance degrades rapidly when the sampling rate reaches 250MHz.

According to the simulation and calculation result from Cadence, the total current consumption is 91.79mA, and the total power consumption is 110.15mW. The SNDR reaches 48.64dB, which is corresponding to a 7.78-bit ENOB. The testing also includes a test with transient noise and with higher sampling rates. The results are shown in Fig.67 and Table 6 to Table 9.

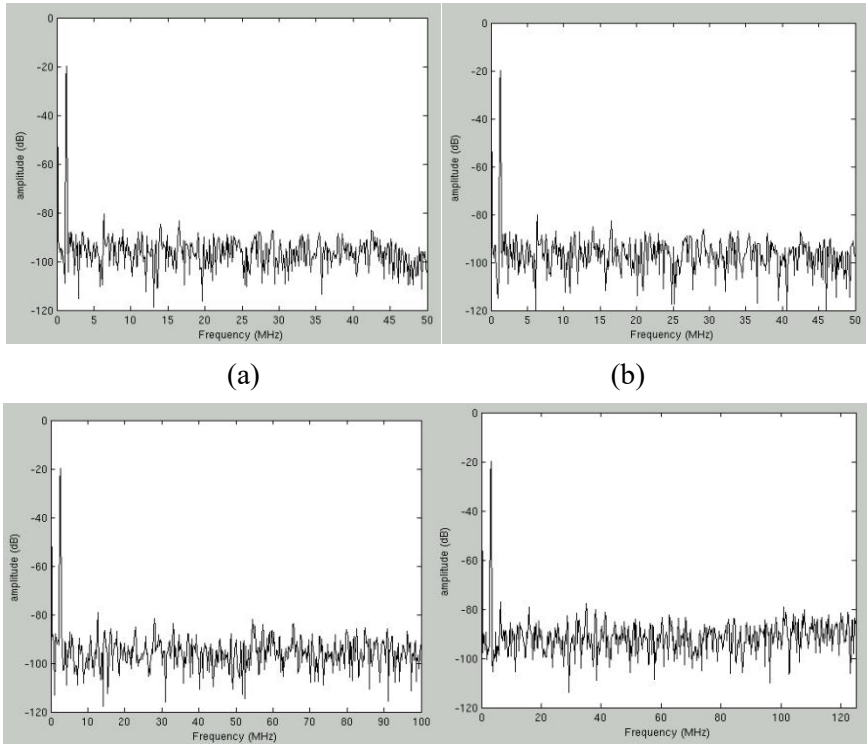


Figure 67. (a) The spectrum of the single tone test at 100MHz.

(b) The spectrum of the single tone test with transient noise.

(c) The spectrum of the single tone test at 200MHz.

(d) The spectrum of the single tone test at 250MHz.

Fig. 67(a) shows the spectrum plot from MATLAB of the single tone test with a 1.27MHz input and a 100MHz clock frequency. Table 6 shows the corresponding performance.

Table 6. The corresponding performance of Fig 67(a).

SNDR	48.64dB
SNR	49.79dB
SDR	54.97dB
SFDR	60.91dB

Fig. 61(b) shows the spectrum plot with transient noise. The input frequency and the sampling rate are the same as in (a), which are 1.27MHz and 100MHz, respectively. Table 7 shows the corresponding performance.

Table 7. The corresponding performance of Fig 67(b).

SNDR	48.50dB
SNR	50.18dB
SDR	53.45dB
SFDR	60.62dB

Fig. 67(c) shows the spectrum plot from MATLAB of the single tone test with a 2.54MHz input and a 200MHz clock frequency. Table 8 shows the corresponding performance.

Table 8. The corresponding performance of Fig 67(c).

SNDR	47.39dB
SNR	49.64dB
SDR	51.33dB
SFDR	59.34dB

Table 9. The corresponding performance of Fig 67(d).

SNDR	43.33dB
SNR	45.43dB
SDR	47.49dB
SFDR	57.22dB

Fig. 67(d) shows the spectrum plot from MATLAB of the single tone test with a 3.17MHz input and a 250MHz clock frequency. Table 9 shows the corresponding performance.

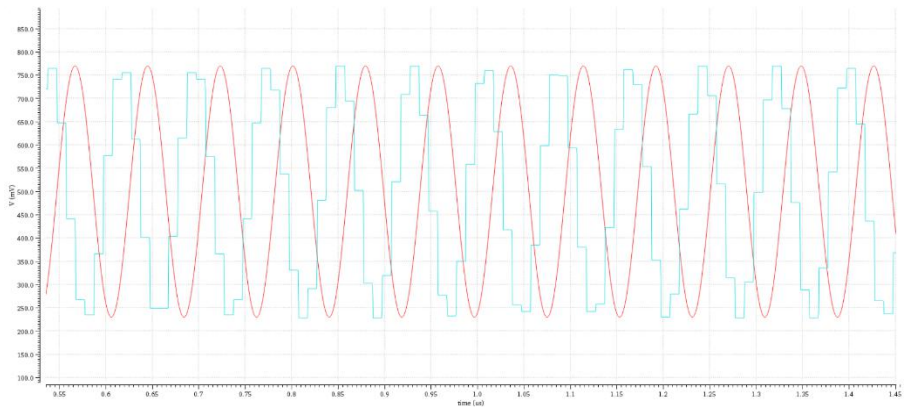


Figure 68. Simulation result for 12.79MHz input.

Then the input is increased to $131/1024 \times F_S$ for both 100MHz and 200MHz sampling rates. Fig. 68 shows the simulation result of the 100MHz sampling rate. Fig. 69and Fig. 70 show the spectrum plots for both 100MHz and 200MHz sampling rates, and the corresponding performances are shown in Table 10 and Table 11, respectively.

Table 10. Performance for 12.79MHz at 100MHz sampling rate.

SNDR	43.17dB
SNR	45.58dB
SDR	46.88dB
SFDR	57.22dB

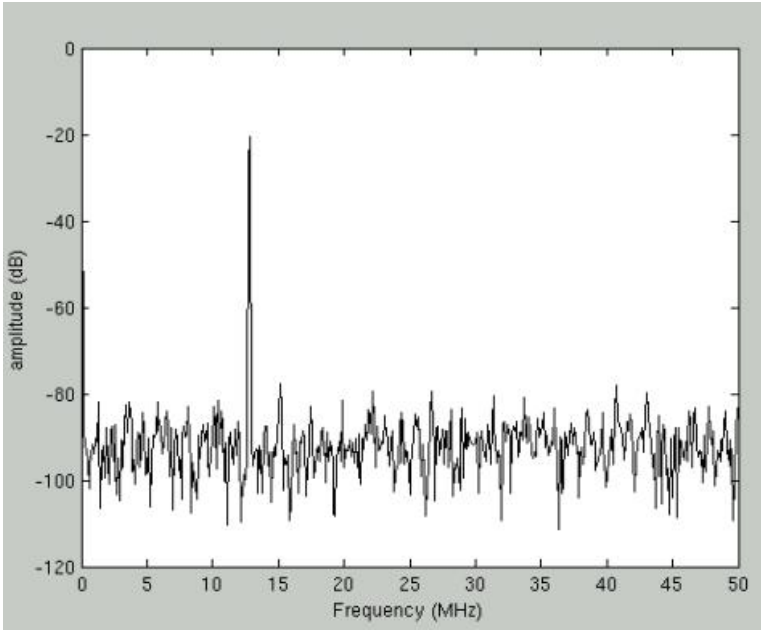


Figure 69. Spectrum plot 12.79MHz at 100MHz sampling rate.

Table 11. Performance for 25.59MHz at 200MHz sampling rate.

SNDR	41.51dB
SNR	45.54dB
SDR	43.70dB
SFDR	53.21dB

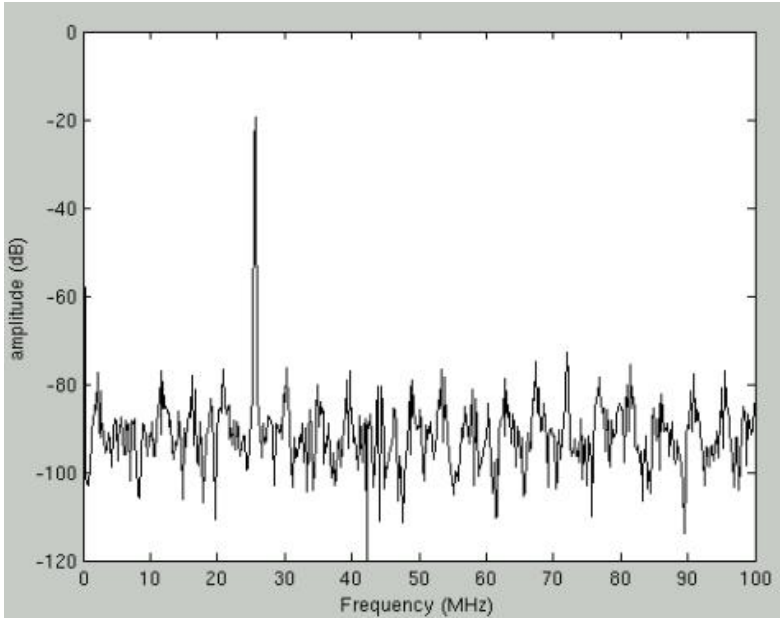


Figure 70. Spectrum plot 25.59MHz at 200MHz sampling rate.

5. Conclusions

The thesis focuses on designing and simulating a high-speed 8-bit fully differential pipelined ADC on 65nm CMOS technology. The ADC works on 1.2V supply voltage and 500mV CM voltage with a full-scale input range from 200mV to 800mV.

All the blocks and the components have been carefully designed and tested to fulfill the high-speed and high-quality requirements. According to the test results in Chapter 4, the ADC can work on up to 250MHz sampling rate with acceptable performance, while the original intention of the speed specification of the ADC is 100MHz. The SNDR reaches 48.64dB at 100MHz clock frequency, 47.39dB at 200MHz frequency, and 43.33dB at 250MHz. Because of the quantization error, the theoretical SDNR of an 8-bit ADC is 49.92dB. Comparing to the ideal SNDR, the performance of the ADC in this thesis is good enough. A transient noise is added in the simulation, and the result shows that the SNDR only reduces 0.14dB, which is enough to prove the reliability and the practicability of the ADC with noise. Table 12 shows the comparison of this work and other similar designs.

Table 12. Comparison with other pipelined ADC designs.

	My	My	[1]	[7]	[10]	[12]	[18]
Resolution (bit)	8	8	10	12	8	6	10
Speed (MHz)	100	200	40	250	100	50	40
Supply (V)	1.2	1.2	3.0	1.2	2.5	1.2	3.0
SNDR (dB)	48.64	47.39	55.00	65.70	48.20	37.10	59.00
Technology(nm)	65	65	90	65	40	130	350
Power (mW)	110.15	112.85	38.10	49.70	8.20	31.62	54.90
FoM (pJ/step)	5.90	3.11	1.10	0.11	0.38	2.10	1.86

6. Future work

A sampling frequency of 250MHz can be regarded as a high frequency of 65nm CMOS technology, but the future speed requirement in communication systems will be far more than that. The CMOS technology limits the performance and the speed of the ADC. It is a promising way to use a higher technology and use smaller transistors to achieve higher speed and better performance. The non-linearity is usually inevitable in the ADC. Although it will not be a critical problem if it is not greater than ±1LSB, the impact of the non-linearity can be minimized.

The thesis is working on a schematic level to ensure the correctness and the feasibility of the theories and equations. To implement a practical ADC system, a layout design and post-layout simulation will be required. Due to the time limitation, this part is not included in this thesis but can be included in future work.

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