Popular Science Summary

Fifth Generation (5G) technology, as a newly flourishing technology, has quickly taken over the market in the past five years. Many survey reports by the telecom companies have shown that the global mobile data traffic is growing significantly in each year. And this data traffic increase is largely due to the expansion of 5G networks. The power consumption introduced by this 5G expansion has shown a rapid increase that leads to a large carbon dioxide dissipation. Therefore, power optimization for 5G products has become one of the major hotspots in recent years. It is also an urgent concern to keep the operating costs and electricity bills under control for the telecom vendors.

For a generic 5G product, the clock-driven power is dominated because of high performance requirements of the product. Ericsson Many-Core Architecture (EMCA) Intellectual Property (IP) block is a block that consists of Ericsson developed digital signal processors. To improve the power efficiency of generic EMCA IP blocks, Clock Gating (CG) is the most commonly used method. CG is a low-power design technique that reduces dynamic power dissipation by removing redundant clock toggles. Ericsson has developed a flow for CG boost. This flow depends on Spyglass power analysis and manual clock gates insertion. This process is normally error-prone and time-consuming. The verification of the optimization needs to run many regressions to cleanup the functional bugs introduced during the optimization. Hence, we need to provide a competent flow that assures a functional error-free optimization with small efforts at the industrial level. Another challenge is that the optimization for generic EMCA IP blocks is usually usecase-specific. This means that the testcase that is used to

optimize an IP block should be more common to the block.

This thesis proposed a flow that can bring together analysis, high-efficient optimization, and formally-verified automatic RTL generation to boost the clock gating efficiency at the late stages of the IP design process. This new flow introduced an efficient Electronic Design Automation (EDA) tool that can automatically implement clock gating in an Application Specific Integrated Circuit (ASIC) design. This EDA tool in-built a functionality equivalence checker that assures error-free optimization. With this tool, the proposed approach guarantees a safe optimization with very little efforts in optimization and verification. In the new flow, we proposed three optional strategies for the testcase selection procedure, which is decisive to the quality of power optimization for an IP block.

Four EMCA IP blocks have been tested and optimized by this new approach. The case study is carried out based on the three strategies developed in the flow. An average reduction of 20% has been achieved for the dynamic power for all tested blocks, which shows that the new flow has performed very well on analyzing and optimizing generic EMCA IP blocks. And, the flow is proved to be very competent for low-power IP design process at the industrial level.