

Evaluation of Discrete-Time Wideband Receivers for NB-IoT

MAGNUS WASTING

MASTER'S THESIS

DEPARTMENT OF ELECTRICAL AND INFORMATION TECHNOLOGY

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Evaluation of Discrete-Time Wideband Receivers for NB-IoT

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Abstract

A receiver that covers several RF bands requires multiple front-end filters which increases the cost in terms of components and/or board/silicon area. Front-end filters assist a receiver to withstand interference at multiples of its down-conversion frequency. Analog discrete-time filters have gained a lot of traction lately, mainly due to their promising architecture, achieving baseband filtering, image and harmonic rejection within the same circuit, allowing a fully integration on-chip. These filters will also scale well with further process shrinking as only switches, capacitors and transconductors are required. The evaluation is performed with a standard 40 nm CMOS technology. This thesis aims to focus on those details that previous papers did not describe in detail, such as different topologies of switches and transconductors, mismatches, non-ideal clock sources, capacitive ratios, intermediate frequency, sample rate, common-mode, noise, on-resistance of switches, power consumption, folding, and simulation aspects with Spectre. To understand these filters a dedicated theory chapter is included, starting from a simple first-order low-pass filter up to the complex $M/2M$ band-pass filter which uses M signals and $2M$ clock phases. All of the above is applied onto a Narrowband Internet of Things (NB-IoT) receiver, as specified in 3GPP release 15. However, a final receiver is not built, only a theoretical one on paper. Discrete-time filters are not suitable for NB-IoT, primarily due to the low requirement on bandwidth (180 KHz), pointing towards a low baseband frequency, which is the opposite of what these filters are suitable for. A high sample rate is required to not degrade the systems performance from folding issues, causing high power consumption. The theoretical receiver is derived to handle all test cases and RF bands, as specified from 3GPP release 15. However, it was not possible to implement a receiver without any front-end filter due to the lack of attenuation of harmonic content over all RF bands. To reduce the power consumption a second-order anti-alias filter was required to reduce the sample rate. The Power consumption was 6.65 mW with a supply voltage of 1.2 V, excluding LNA, mixer, clock dividers and ADC.

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Popular Science Summary

In today's world almost everything is connected by a wireless connection. Given the past history even more will be connected, even for things that no one asked for, perhaps even a can opener. All devices should also be battery powered with several years between any charging. Which can be summarized with other words; how can we create a wireless device that's both cheap and barely consumes any energy? Both of these parts are solved by further integration onto silicon, which is the building foundation of an integrated circuit, namely 'chips' or transistors. You find these transistors in everything from your smart LED lamp to your mobile phone.

The cost aspects can be explained through 'economy of scale', which simplifies to "producing two of the same will always be cheaper than two different things". A real-world example of this would be the dual zone fridge freezer, one could argue that the freezer is integrated into the fridge and thereby making it cheaper to buy then buying the two by themselves.

I think we all have heard about submicroscopic transistors, which year after year shrink in size, mainly due to the science and engineering efforts into this field. As an example, the physical diameter of the COVID-19 virus is $\sim 100 \text{ nm}$ [1] which in comparison to today's transistors is colossal. This thesis is built upon a rather old manufacturing process of 40 nm , in which its mass production started back in 2008. Today you can buy phones in masses that are built upon 5 nm transistors.

In any case, this might sound rather good, which it is! At least for computers and phones as smaller devices means less energy for the same performance, which also goes the other way around. Given the same speed, one can reduce the energy consumption, effectively increase the battery time. But for analog circuits, such as amplifiers, there is not much to gain. There are even aspects where it's worse. Analog discrete-time circuits are supposedly a solution to this, as it scales with the same parameters as computers, but also opens the possibility of more integration onto silicon due to their nature in design, and thereby reducing its cost.

List of Acronyms

5G	The fifth generation technology standard for broadband cellular networks.
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
BB	Baseband
BPF	Band-pass Filter
BW	Bandwidth
CM	common-mode
CMOS	Complementary Metal–Oxide–Semiconductor
CMRR	common-mode Rejection Ratio
CS	Common Source (transconductor)
CSBPF	Charge Sharing Band-pass Filter
DCR	Direct-Conversion Receiver
DR	Dynamic Range
DT	Discrete-Time
E-UTRA	Evolved Universal Terrestrial Radio Access
FB	Feedback (transconductor)
FIR	Finite Impulse Response
FS	Full Scale
g_m -cell	Transconductor
GSM	Global System for Mobile Communications
HB	High Band
IIP	Input-referred Intercept Point

LB	Low Band
FD	Fully Differential (transconductor)
HPF	High Pass Filter
IF	Intermediate Frequency
IMRR	Image Rejection Ratio
IIR	Infinite Impulse Response
IP2	Second-order Intercept Point
IP3	Third-order Intercept Point
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LSB	Lower-Sideband
LTE	Long Term Evolution
MB	Mid-Band
MC	Monte Carlo
MOM	Metal-Oxide-Metal
NB-IoT	Narrowband Internet of Things
QPSK	Quadrature Phase Shift Keying
OFDM	Orthogonal Frequency-Division Multiplexing
OFDMA	Orthogonal Frequency-Division Multiplexing Access
PAC	Periodic AC Analysis
PAR	Peak-to-Average Ratio
PD	Pseudo-Differential (transconductor)
PLL	Phase-Locked Loop
PSS	Periodic Steady State
PXF	Periodic Transfer Function
Q-factor	Quality factor
QPSK	Quadrature Phase Shift Keying
SAW	Surface Acoustic Wave
SNR	Signal to Noise Ratio
STS	Single Transistor Switch
TA	Transconductance Amplifier

TF	Transfer Function
TG	Transmission Gate
UE	User Equipment
ULB	Ultra Low Band
USB	Upper-Sideband

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Introduction

1.1 Background

Modern telecommunications are continuously growing with even more connected devices and higher data traffic every year that passes. The fifth generation (5G) is the latest and was commercially launched at the end of 2018 in several cities [2]. The 5G New Radio standard was developed by the 3rd Generation Partnership Project (3GPP) and first specified in release 13. As with previous generations, the naming scheme is a collection of several different radio bands and protocols.

Narrowband Internet of Things (NB-IoT) can be seen as a subgroup of 5G and it has been designed for massive amount of connected devices that both have low power and throughput. These devices consist of sensors, meters, wearables, and other so called "smart" things. NB-IoT was also developed by 3GPP and first specified in release 13. Cellular IoT connections were one billion in 2018 and are expected to grow to 4.1 billions in 2024, at an annual growth rate of 27 percent, where NB-IoT is expected to have a big market share [2].

A big portion of the NB-IoT market is low cost devices, especially the "smart" IoT as these will be marketed to consumers, and one of the strongest drivers in consumer electronics are the competition of price. These devices also require longer battery life, up to 10 years is a common sales pitch, although its battery life is strongly dependent on how often one sends and receives data.

For a CMOS receiver this means removal of even more off-chip components and integrating these on-chip. Which is a lot easier said than done. For example, if the front-end filters described in chapter 1.2 are meant to be integrated on-chip, more silicon area is required, which makes it more expensive although the end cost would be lower if it would be mass produced. Majority of the cost comes from off-chip components, board space, assembly and verification. Another point is the low Q-factor of on-chip inductors, at least in comparison to off-chip inductors and Surface Acoustic Wave (SAW) filters that are normally used [3]. A lower Q-factor will result in a flatter filter response, hence less attenuation of harmonic content and out of band blockers. This would in turn set higher linearity and filtering

requirements on the whole receiver to not increase the Analog-to-Digital Converter (ADC) bit resolution, as the dynamic range (DR) of the ADC will increase with less filtering.

1.2 A Typical Wideband Receiver

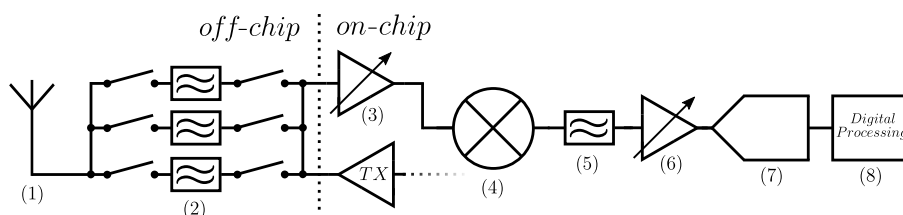


Figure 1.1: Block diagram of a typical wideband receiver.

The building blocks of a typical wideband receiver in CMOS technology can be seen in figure 1.1. The antenna is the first part (1) where radiant energy is absorbed and converted into an electrical signal. The antenna impedance is usually 50Ω .

Next in-line are multiple of switches (2) with their corresponding front-end filter. The switches connect the antenna to either the receiver or transmitter, depending on if it is sending or receiving information. The switches can also route the signal through different front-end filters depending on what frequency band is used. These filters can also be in combination with a balun that convert the signal from single-ended to differential. The filter type in question is typically a band-pass filter and is there to reduce harmonic content and out of band interference.

Now comes the first amplifier (3), which is a special Low Noise Amplifier (LNA) with a moderate to high gain $\sim 25 \text{ dB}$. The amplifier will reduce noise requirement of all forthcoming blocks accordingly to Friis formula for noise. The LNA can either be a true wideband with a flat frequency response over several GHz or have multiple resonant circuits, one for each RF band. The first implementation requires less area and attains close to zero attenuation of unwanted harmonic content, while the other is opposite in both cases.

The mixer (4) performs frequency mixing of the RF signal and the Local Oscillator (LO). Mathematically speaking, a frequency multiplication between the RF and LO are performed and it creates new frequencies, namely the difference between RF and LO and all combinations of their harmonic content. Fourier analysis is a great tool to express the complete transfer. The new frequency from the first harmonic of both RF and LO is called the Intermediate Frequency (IF) and contains the wanted information of the RF signal at a much lower frequency. By using a lower frequency, the forthcoming blocks can thereby be designed with a lower bandwidth, hence they are less sensitive to parasitic capacitance. These blocks are also grouped together figurative as the Baseband (BB) to emphasize

the difference between the high-performance RF side with frequencies up in the GHz range and the BB side with frequencies between DC and a couple of MHz .

The mixer is followed by a BB-filter (5), the filter type is a low-pass in direct-conversion receiver (also known as homodyne or zero-IF receiver) as the IF frequency is centred at DC. If the IF is not centred at DC, the filter is thereby a band-pass and is known as Superheterodyne receiver. In any case, the task of the BB filter is to attenuate frequencies that are close to the carrier, as adjacent channels or in-band interference. The signal strength at this stage is still to low and needs further amplification.

The weak signal is then amplified by the BB amplifier (6) to a level well above the quantization noise floor. This amplifier also needs to have variable gain to maximize the dynamic range of the analog-to-digital converter (ADC) (7), which is the last analog block before the signal is quantified and converter to a digital representation. The ADC should have its own anti-aliasing filter to prevent folding, but it could be integrated into the BB amplifier given that it is normally bandwidth limited. The last stage (8) is post-processing were decoding and further digital filtering are done.

1.3 Thesis Scope

This thesis started as a request from Arm, they were interested in an evaluation of discrete-time receivers and if they are suitable for NB-IoT, without any external front-end filter. This means that the receiver must be able to handle all interference that 3GPP specifies, without sacrificing other key parameters.

However, it must be stated that halfway through the thesis work Arm decided to close their analog department and essentially fired everyone, including me and my mentors. As a result, further thesis work was delayed until Acconeer encouraged me to finalize it. Although this never happened due to personal issues and thereby delayed my work again. Later, I relocated to Nordic Semiconductor where the thesis was finalized.

The filter in question from a discrete-time receiver is known as Charge Sharing Band-pass Filter (CS-BPF) and has gained a lot of traction lately [4–8], these filters are built upon the old N-path filter from 1960 [9] and do no longer suffer from a repetitive frequency response, which effectively means that it is possible to attenuate negative frequencies, or in other words, the image frequency.

The main selling points of CS-BPF are supposedly better performance scaling with a shrinking process node as they can handle the reduction of supply voltage. This comes down to the simplicity of the filters as the building blocks are simple g_m cells, capacitors, and switches (single transistors). These filters are also supposedly stable over Process, Voltage and Temperature (PVT) as the center frequency is only dependent on a capacitive ratio and its sample rate.

The focus will be on; what is needed to fulfill the 3GPP requirements for a NB-IoT receiver with CS-BPF as baseband filters and g_m -cells for amplification. By removing the input front-end filter, the receiver is now susceptible to interference located at a multiple of its LO frequency and thereby harmonic rejection is required and will be looked upon. The power consumption of the whole BB chain is set to max 10 mW and the IF is set to 10 MHz . The low power consumption is needed as NB-IoT devices are intended to be powered from a battery while the rather high IF was requested from Arm with the argument that an IF of 10 MHz would remove all issues caused by intermodulation and $1/f$ noise. No limit on area was set, although capacitors in the nF range is out of the question. The power supply voltage is set to 1.2 V given that this thesis is built upon a typical 40 nm CMOS bulk technology.

Because of time constrains this thesis will only look on the BB side of the mixer. However, the RF side is still needed in several simulation and must therefore be built. The implementation of the LNA was an ideal amplifier while the mixer was with physical models in CMOS, more about this is explained in chapter 4.

1.4 Thesis Structure

A short list of all forthcoming chapters and a brief explanation about them.

- Chapter 2, Theory : A detailed explanation of the mathematics behind analog discrete-time filters and their subcategories.
- Chapter 3, 3GPP NB-IoT Standard and Receiver Specification : What is 3GPP? How are NB-IoT specified from a receiver perspective? A dynamic range mask with filter requirement is also derived from its specifications.
- Chapter 4, Low Noise Amplifier and Mixer : Disclosure of LNA and mixer that was used in several simulations.
- Chapter 5, Discrete-Time Filters : A detailed investigation of the sub-blocks within a discrete-time filter and impacts of different design parameters.
- Chapter 6, Transconductance Amplifiers : Four different, but quite similar topologies, were investigated. What are the trade-offs? Is there any clear winner?
- Chapter 7, Harmonic Rejection : Two different topologies of harmonic rejection are looked upon, one is based on continuous-time while the other is discrete-time.
- Chapter 8, Discussion and a Receiver on Paper : Summary of the whole thesis, comments on what we have learned and own opinions. A theoretical NB-IoT receiver is also derived on paper.
- Chapter 9, Conclusions : A short summary with conclusions, will NB-IoT and discrete-time filter work tougher?

2.1 Intermodulation Products

In a perfect world an ideal amplifier produces an output signal that is proportional to what it is given to its input, no additional information is created or removed. However, in the real-world amplifiers are usually linear at *lower* input levels, to be gradually more and more non-linear at higher levels.

A common way of representing this is seen in eq. 2.1, where A represents the DC component, C_1 the linear gain, C_2 and C_3 the coefficient for the second and third-order products, respectively. With an ideal amplifier only C_1 is non-zero. An important concept from this relationship is that its order is proportional to its growth, second-order products grow by the square while the third with the cube. In terms of power levels, this translates to a slope of one, two and three for the first to third-order respectively.

$$V_{out} = A + C_1 V_{in} + C_2 V_{in}^2 + C_3 V_{in}^3 + \dots + C_n V_{in}^n \quad (2.1)$$

The concept in question is called Intermodulation (IM), which describes the amplitude modulation of at least two different frequencies. IM2 represents the second-order while IM3 the third-order products. The new frequencies that are created comes from a scaled sum and difference, namely $f_1 \pm (n-1)f_2$ and $(n-1)f_1 \pm f_2$, where n is the intermodulation order. This comes for the core concept from amplitude modulation. Although, not all new frequencies will cause trouble. The product of the sum will go up in frequency by approximately a factor of two, and thereby increasing the distance in the frequency domain from our wanted signal.

The difference though, it can fall directly at our wanted signal or close to it. Given its amplitude it could be high enough to obscure our wanted signal or saturate the forthcoming circuit. In particular the IM2 product of $f_2 - f_1$ and the IM3 at $2f_1 - f_2$ and $2f_2 - f_1$ are the cause of most issues and will set requirements on linearity of all amplifiers. In other words, nothing is perfect, new frequencies will always be created. If an amplifier is good enough, in terms of linearity, the level

of these new frequencies will still be below the noise floor and thereby not impact the systems performance.

The question then arises, what is good enough? This is in turn answered by [10] and seen in eq. 2.2 and 2.3, although the M term has been added and represents a margin between the signal and its IM product. IIP stands for Input-referred Intercept Point and is a theoretical point where signal and IM product is equal in strength, the number behind IIP represents the modulation order.

$$IIP2_{min} = 2P_i - P_s + M \quad (2.2)$$

$$IIP3_{min} = \frac{1}{2}(3P_i - P_s + M) \quad (2.3)$$

As an example with two tones, representing an interference and a signal at a power level of $P_i = -20 \text{ dBm}$ and $P_s = -50 \text{ dBm}$, respectively. Given these two levels and a margin of $M = 10 \text{ dB}$, with the equations above, the minimum IIP2 is thereby 20 dBm while IIP3 is 0 dBm , which is the same as the cross-points between signal, IM2 and IM3 in figure 2.1. Furthermore, the signal power, both its input and output, are equal to -50 dBm , as in our example the gain is zero. Its IM products are well below its own signal level and thereby will not cause issues. However, the interferer with its higher level at -20 dBm results in a non-negligible IM2 and IM3 level at -60 dBm . Which is 10 dB lower compared to our signal at -50 dBm . The difference between our wanted signal and IM products from the interference is only 10 dB , which is the same as our given margin of 10 dB .

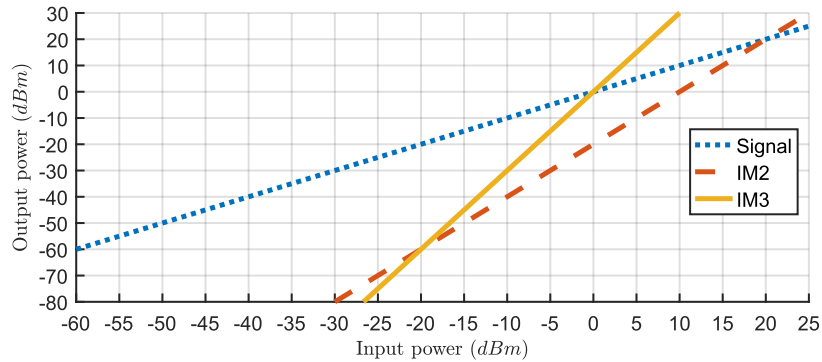


Figure 2.1: Intercept point diagram between signal and intermodulation products two and three. In this example IIP2 is 20 dBm while IIP3 is 0 dBm .

Note that any frequency information is never told. The signal and interferer could have the same frequency, in that case the interference level is already an issue and IM can be ignored. In another case where the interference is *further* from the signal and thereby not an issue per se. But as the amplifier is not perfect, the

IM products from the interferer might fall directly onto the wanted signal with a level difference of 10 dB and thereby cause issues. Calculating intermodulation products will never give the full story, but it is a great tool to have.

2.2 Sampling and Anti-Aliasing

In the world that we all live in, signals are real and continuous (excluding quantum mechanics). This means that you can always find another point between two given points, in fact there is an infinite set of new points between these two adjacent points. A discrete-time signal is the opposite to a continuous one, the signal is defined with a limited set of single points and is undefined between two adjacent points. A discrete-time signal is in a way a lossy compression of a real continuous signal as all information that could be gathered under the limited time frame is approximated into a single point. This process is called sampling and is illustrated in figure 2.2. How many samples one take under one second is called sample rate or sampling frequency, f_s , and its inverse, $1/f_s = T_s$, will be the time between two adjacent samples.

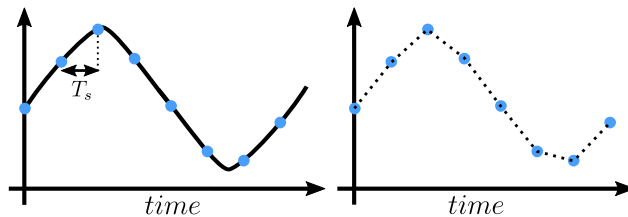


Figure 2.2: A continuous signal and its discrete representation by sampling with a time period of T_s .

A major issue with all discrete-time systems is the unwanted aliasing effect that occur for input frequencies higher than $f_s/2$, commonly known as the Nyquist frequency. Aliasing is also called folding as input frequencies that are a multiple of the sampling rate, $kf_{in} = f_s, k = 1, 2, \dots$, are *folded* back to zero. The folding effect can also be seen as frequency multiplication, or mixing, between the input and sampling frequency as it will down-convert all harmonics of the input signal that are higher than $f_s/2$. Although no up-conversion occurs.

The aliasing effect can be illustrated in the complex plane. Frequency is represented by two rotating vectors, positive and negative frequency. Both vectors starts from (1, 0) and rotate with the same angular velocity, but in opposite directions. Sampling captures a snapshot of the vectors position. A position of (1, 0) represents zero Hz while (0, 1) and (-1, 0) represents $f_s/4$ and $f_s/2$, respectively.

Figure 2.3 shows three different input frequencies, all are sampled with a constant sampling rate of f_s . In a) the input frequency is $f_s/8$ which is lower than $f_s/2$, the sampled signal will therefore correspond to the real input signal, no aliasing

occurs. In b) the input frequency is increased to $\frac{7}{8}f_s$, aliasing will now occur as we have passed $f_s/2$, the sampled signal will be seen to have the same frequency as in a) but with a phase shift of 180° . Information is lost as there is no way to confirm that the actual frequency was $\frac{7}{8}f_s$. In c) the input frequency is yet again increased to f_s , which is as in b) higher than $f_s/2$ and therefore aliasing will occur. The observed frequency from sampling is zero, all information are lost. Not only are information lost in b) and c) but the input frequency are also down-converted below $f_s/2$ and can therefore interfere with signals of interest.

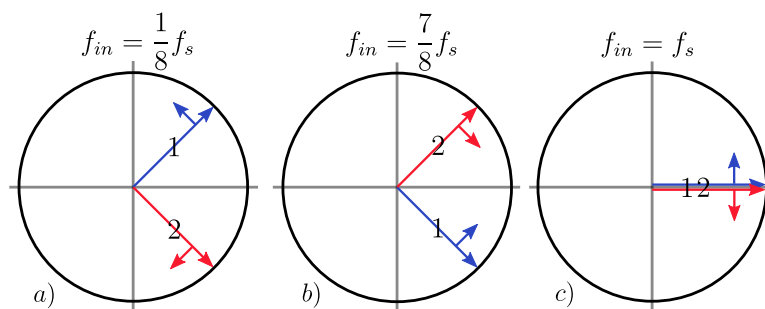


Figure 2.3: Sampling and its aliasing effects within the complex plane. a) is with an input frequency of $f_s/8$, b) with $\frac{7}{8}f_s$ and c) with f_s . In all cases the sample rate is f_s .

To remove these unwanted effects, an anti-aliasing filter is required to attenuate unwanted signal above $f_s/2$ before any sampling occurs. In theory, this filter is a so-called brickwall low-pass filter that removes all frequencies higher than $f_s/2$, but in practice it consist of a high-order active low-pass filter, there is also other solutions such as the sinc filter.

2.3 Sinc Filter

The sinc filter is an effective way of creating an anti-aliasing filter as it comes for free with charge sampling (section 2.5.2). The ideal impulse response from the sinc filter is a sinc function and its frequency response is a perfect rectangular function, it is a perfect low-pass filter, removing all content above its cut-off frequency.

In the real-world however, there is no such thing as a perfect sinc filter. The actual frequency response follows the first-order low-pass filter but with multiple of infinite notches that are located at the inverse of its time window T_s , k/T_s , $k = 1, 2, \dots$, figure 2.4. If the window time is set to the same time as the sample interval the notches from the sinc filter will cancel the repetitions of a discrete-time frequency response, also, all folding that occurs with frequencies higher than $f_s/2$ will be attenuate due to the low pass characteristics. The end result is the removal of all repetitive responses but not the removal of the folding effects, unwanted content is still folded back to zero but with a lower amplitude.

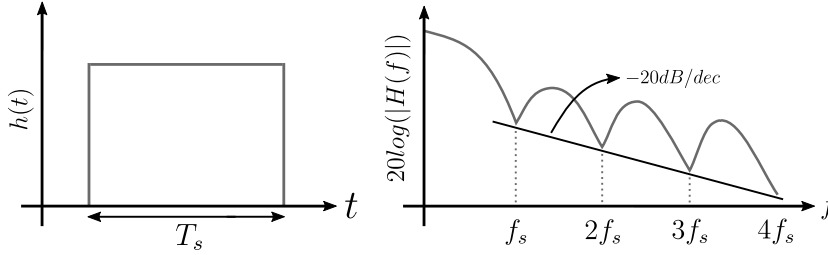


Figure 2.4: Convolution of a time window creates a sinc filter in frequency.

The sinc filter can be implemented in CMOS with a transconductor (g_m), a capacitor, and a switch (transmission gate or a single transistor), as shown in figure 2.5. The switch will clear the previous sample every T_s and thereby convert the continuous-time into a time window.

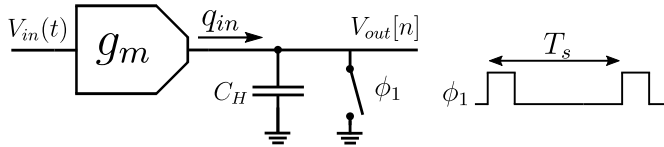


Figure 2.5: General implementation of the sinc filter.

A more formal name of this implementation is called Windowed Integration Sampler (WIS) [11] and works by integrating the output current, or charge, from a transconductor onto a capacitor under its time window. This creates a discrete voltage sample that corresponds to the integrated current and is stored onto the capacitor with a sinc frequency response as seen in eq. 2.4 (assuming $V_{in} = 1$). The level of attenuation depends on how deep the notches of the sinc filter are, which in turn is entirely decided by the output impedance of its transconductor [12]. The combined response of a generic discrete-time system and the sinc filter is illustrated in figure 2.6

$$V_{out}[n] = \frac{g_m}{C} \int_{nT_s}^{(n+1)T_s} V_{in} dt \rightarrow |H(f)| = \frac{V_{out}}{V_{in}} = \frac{g_m T_s}{C} \text{sinc}(f_{in} T_s) \quad (2.4)$$

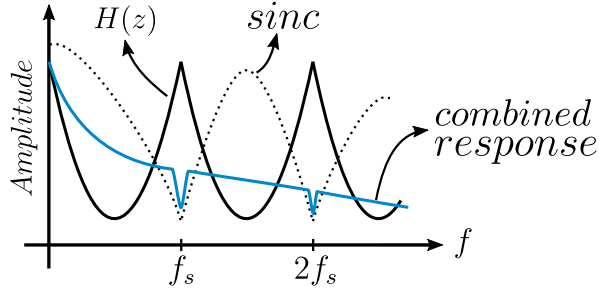


Figure 2.6: Illustration of the combined frequency response of a generic discrete-time system and its sinc filter.

2.4 General Information of Discrete-Time Filters

2.4.1 Common Definitions

Analog discrete-time filters are built upon discrete charge packages that moves from one capacitor to another, and in all forthcoming filters there are two common capacitors and its three related ratios that are recurrent through the thesis.

C_H is the first capacitor and represents the *history*. The stored charge is the integrated current of the present sample and all previous samples, an analogy is a Infinite Impulse Response (IIR). C_H is also the capacitor that creates the sinc filter. The second capacitor is C_R and represents a *rotational* charge between different C_H capacitors, its analogy is more of a Finite Impulse Response (FIR) as its charge is cleared every cycle. There are normally one or two C_H for each signal phase but only one C_R , for one filter circuit. All rotations are controlled by the movement from clock phases ϕ_1 to ϕ_N .

Two ratios are named α_1 and α_2 , expressed in eq. 2.5 and 2.6 where α_1 represents the charge movement from C_H to C_R while α_2 represents the opposite, a charge movement from C_R to C_H . The last ratio is k and represents a capacitive loading factor *seen* by a transconductor, multiplying with its g_m will give the voltage gain of a filter.

$$\alpha_1 = \frac{C_H}{C_H + C_R} \quad (2.5)$$

$$\alpha_2 = \frac{C_R}{C_R + C_H} \quad (2.6)$$

$$k = \frac{1}{C_H + C_R} \quad (2.7)$$

2.4.2 Clock Phases

Any discrete-time filter is always controlled by at least two clock phases, as the example shown in figure 2.7. Given a continuous input signal, the first phase, ϕ_1 , will define the exact moment when the signal is converted to a discrete representation. This exact moment happens when the first switch disconnects $V_{in}(t)$ and $V_{in}[n]$. Therefore, ϕ_1 must meet high requirements, typically very low jitter. If the system has no decimation of sample rate, ϕ_1 will be the only phase that sets the system's performance. In terms of jitter, ϕ_2 can be orders of magnitude worse and it won't degrade the performance.

Furthermore, if the time period T is constant between several samples, then any variations of x_1 and x_2 has zero impact. Even if this generic filter is analog by nature the concept is identical to digital filter, an analogy towards digital filter is, it doesn't matter if the computation time of a digital filter varies, as long as it is done before the next sample and that the sampling is coherent. An analog discrete-time filter acts the same way as the digital representation, but the analog world brings its own aspects such as non-zero ohm switches, leakage, and low output impedance.

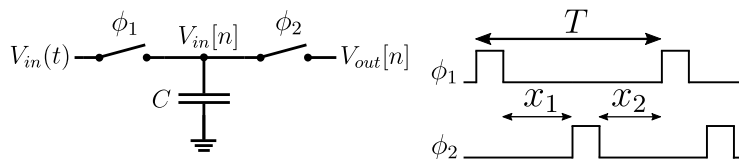


Figure 2.7: A generic discrete-time filter with its two clock phases.

2.4.3 Equivalent Resistance of a Switched Capacitor

Two switches and a capacitor can act as an equivalent resistance, if the switches are controlled in a proper way. Given the schematic in figure 2.8, the charge transfer, q , from V_{in} to V_{out} during one period is equal to the voltage difference multiplied by the capacitance, C , $q = C(V_{out} - V_{in})$. Dividing the charge by the time period gives the current I , $I = q/T$. The resistance, R_{eq} , is then calculated with Ohm's law. Replacing time with frequency gives the final form as seen in eq. 2.8.

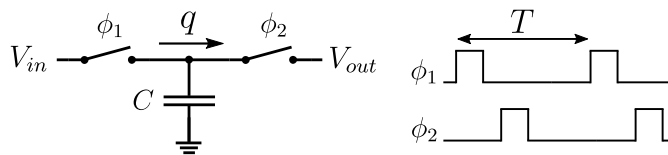


Figure 2.8: Concept of a switched capacitor.

$$R_{eq} = \frac{V}{I} = \frac{V_{out} - V_{in}}{\frac{q}{T}} = \frac{V_{out} - V_{in}}{\frac{C(V_{out} - V_{in})}{T}} = \frac{T}{C} = \frac{1}{f_s C} \quad (2.8)$$

2.4.4 Gain of a Unit g_m -cell

A g_m -cell is short for a Transconductance Amplifier (TA), it takes a voltage as its input and outputs a current. The g_m part comes from its definitions of $g_m = I_{out}/V_{in}$. V_{out} in figure 2.9 is derived directly from ohms law, the load, Z_L , is the parallel impedance of C_H and R_{eq} as described in eq. 2.9.

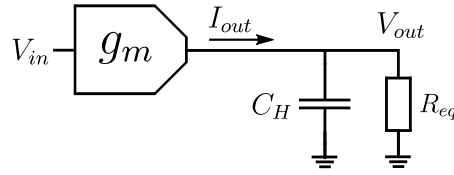


Figure 2.9: A simple g_m -cell with its load.

$$V_{out} = I_{out} Z_L, I_{out} = g_m V_{in} \rightarrow \frac{V_{out}}{V_{in}} = g_m Z_L = g_m (R_{eq} || Z_{C_H}) \quad (2.9)$$

Further expansion with eq. 2.8 and $Z_{C_H} = 1/(2\pi f_{IF} C_H)$, gives the final expression as seen in eq. 2.10. Note that C in eq. 2.8 is changed to C_R to match further equations.

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{C_R f_s + 2\pi C_H f_{IF}} \quad (2.10)$$

2.5 Discrete-time Low-pass Filter

2.5.1 Voltage Sampling

The first-order low-pass filter with voltage sampling is attained with two capacitors and two switches. It is controlled by two phases as depicted in figure 2.10.

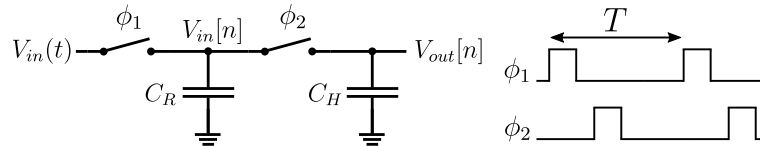


Figure 2.10: Ideal first-order low-pass filter with voltage sampling.

The first switch acts as a typical sample and hold circuit, the voltage onto C_R follows $V_{in}(t)$ continuously given that ϕ_1 is asserted. The exact moment ϕ_1 changes state, the voltage onto C_R are no longer continuous, therefore it is discrete and is now expressed as $V_{in}[n]$. Next, ϕ_1 and ϕ_2 transition from high to low and low to high, respectively. Charges from C_R moves onto C_H , this gives the term $\alpha_2 V_{in}[n]$. As charges of C_H is never cleared, its previous sample $[n - 1]$ also contributes to $V_{out}[n]$. However, the movement of charges are now inverted, charges moves from C_H to C_R and therefore gives the term $\alpha_1 V_{out}[n - 1]$. The cycle repeats with a time period of T and as the system has neither gain or attenuation the voltage gain is always unity. The expression of $V_{out}[n]$ is given by eq. 2.11 and its Z-transform by 2.12.

$$V_{out}[n] = \alpha_2 V_{in}[n] + \alpha_1 V_{out}[n - 1] \quad (2.11)$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\alpha_2}{1 - \alpha_1 z^{-1}} \quad (2.12)$$

2.5.2 Charge Sampling

The charge sampling variant of the discrete-time low-pass filter is quite similar to the voltage sampling circuit in section 2.5.1, the biggest difference is the sampling method. Instead of converting the voltage at an exact moment in time the sampling works by integrating charge from a g_m -cell under a time period T . Other than that, it works identical and uses the same building blocks, two capacitors, two switches and two phases. And as we are integrating the charge, we gain another function, the sinc filter, in which one could argue that the charge sampling is superior to the voltage sampling as it comes with a free anti-aliasing filter. The circuit are shown in figure 2.11.

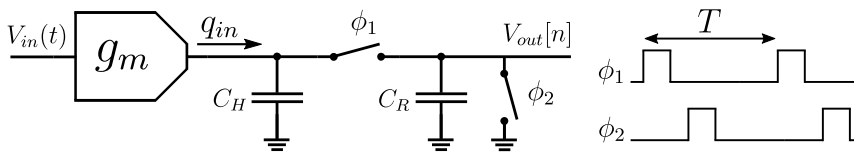


Figure 2.11: Ideal first-order low-pass filter with charge sampling.

When ϕ_1 is asserted, charge of the present sample is stored onto the parallel capacitance of C_H and C_R , which gives the $kq_{in}[n]$ term. The second part when ϕ_1 closes and ϕ_2 opens works identical to the voltage sampling, thereby gives the term $\alpha_1 V_{out}[n - 1]$. The cycle repeats with a time period of T and the expression of $V_{out}[n]$ is given by eq. 2.13. With help from eq. 2.14 the Z-transform of eq. 2.13 is given by eq. 2.15. The voltage gain of the system is obtained from eq. 2.15 with $z = 1$ and gives $\frac{k g_m T}{1 - \alpha_1}$.

$$V_{out}[n] = kq_{in}[n] + \alpha_1 V_{out}[n-1] \quad (2.13)$$

$$q_{in}[n] = g_m \int_{nT}^{(n+1)T} V_{in}(t) dt \rightarrow V_{in}(t) = 1 \rightarrow g_m T \quad (2.14)$$

$$H(z) = \frac{V_{out}(z)}{q_{in}(z)} = \frac{k}{1 - \alpha_1 z^{-1}} \rightarrow \frac{V_{out}(z)}{V_{in}(z)} = \frac{k g_m T}{1 - \alpha_1 z^{-1}} \quad (2.15)$$

2.5.3 Combined Charge and Voltage Sampling

By combining the charge and voltage circuit from section 2.5.2 and 2.5.1 another order on the low-pass filter is gained without doubling the necessary components, only one more of each are needed. The circuit is shown in figure 2.12.

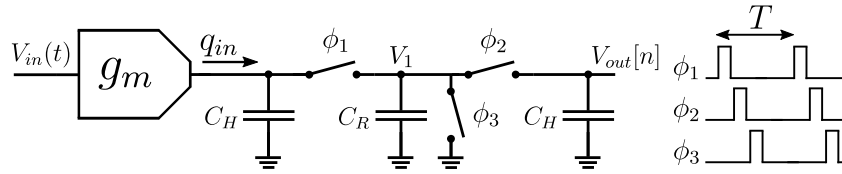


Figure 2.12: Ideal second-order low-pass filter with combined charge and voltage sampling

When dealing with multiple stages the complexity increases substantially, one way of simplifying is to express each node as it is the present sample, $V_x[n]$, and continuing with the Z-transform of each expression individually to be later added together, this works as one of the properties of the Z-transform is linearity. The charge sampling gives $V_1[n]$ while the voltage sampling gives $V_{out}[n]$, as expressed in eq. 2.16, 2.17 and their respective Z-transform by eq. 2.18, 2.19.

$$V_1[n] = kq_1[n] + \alpha_1 V_1[n-1] \quad (2.16)$$

$$V_{out}[n] = \alpha_2 V_1[n] + \alpha_1 V_{out}[n-1] \quad (2.17)$$

$$V_1(z) = \frac{kq_{in}(z)}{1 - \alpha_1 z^{-1}} \quad (2.18)$$

$$V_{out}(z) = \frac{\alpha_2 V_1(z)}{1 - \alpha_1 z^{-1}} \quad (2.19)$$

By combining 2.18 and 2.19, and solving for V_{out}/q_{in} we obtain the transfer function as given in eq. 2.20, which can be expressed in terms of V_{out}/V_{in} with 2.14, and with $z = 1$ the voltage gain is given by eq. $\frac{k\alpha_2 g_m T}{(1-\alpha_1)^2}$

$$H(z) = \frac{V_{out}(z)}{q_{in}(z)} = \frac{k\alpha_2}{(1 - \alpha_1 z^{-1})^2} \rightarrow \frac{V_{out}(z)}{V_{in}(z)} = \frac{k\alpha_2 g_m T}{(1 - \alpha_1 z^{-1})^2} \quad (2.20)$$

2.5.4 M'th Order

The M'th order low-pass filter consist of one charge sampling stage and $M - 1$ voltage sampling stages, the required resources are one g_m -cell, one C_R , M C_H and $M + 1$ switches with its corresponding phase, as shown in figure 2.13. It is possible to switch order of the filter as each order has its own output, the only thing one need is to connect all outputs to an analog multiplexer and control which output one wants.

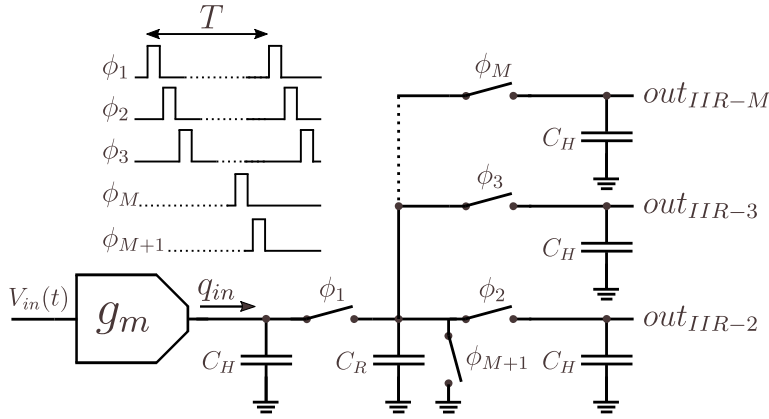


Figure 2.13: Ideal M'th order low-pass filter.

The transfer function is expressed in eq. 2.21 and was derived the same way as in section 2.5.3, the only difference is that each additional stage adds another $\frac{\alpha_2}{1 - \alpha_1 z^{-1}}$, note that the equation is only valid for $M > 1$, and with $z = 1$ gives the voltage gain as seen in eq. 2.22.

$$H(z) = \frac{V_{out}(z)}{q_{in}(z)} = \frac{k\alpha_2^{M-1}}{(1 - \alpha_1 z^{-1})^M} \rightarrow \frac{V_{out}(z)}{V_{in}(z)} = \frac{k g_m T \alpha_2^{M-1}}{(1 - \alpha_1 z^{-1})^M} \quad (2.21)$$

$$A_V = \frac{k g_m T \alpha_2^{M-1}}{(1 - \alpha_1)^M} \quad (2.22)$$

2.6 Complex Band-pass Filter

The complex Band-Pass Filter (BPF), or charge sharing band-pass Filter as many prior papers use, are mainly divided into two groups, the M/M and $M/2M$. The $M/-$ represents the number of inputs and outputs while $-/M$ and $-/2M$ represents how many clock phases are required. Input and clocks must be distinct with its phase, typically by $360^\circ/M$ or $360^\circ/2M$ depending on which filter order is used. This section starts with the $4/4$, continues with M/M and ends with the $M/2M$. A detailed explanation is given with the $4/4$ while the other sections are simplified as they all work in the same way.

2.6.1 Conventional Quadrature $4/4$

The conventional quadrature $4/4$ band-pass filter, has as its name suggest, 4 inputs/outputs ($4/-$) and 4 clock phases ($-/4$). The filter requires an input that are separated into 4 different phases, normally by 90 degrees from each other as 0° , 90° , 180° , and 270° but the absolute values are irrelevant. The same phase difference is required onto the clocks and that they have the same frequency. Furthermore, four g_m -cells, four C_H , four switches, and one C_R are required. The filter is controlled by these 4 clocks, $\phi_1, \phi_2, \phi_3, \phi_4$ and creates the distinct charge packages of q_1, q_2, q_3 , and q_4 that are in turn created by its g_m -cell. Schematics over the ideal filter can be seen in figure 2.14.

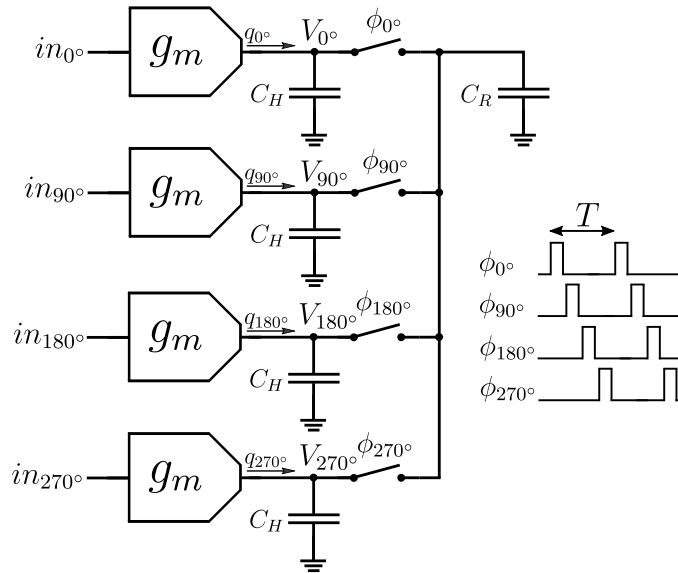


Figure 2.14: Ideal $4/4$ complex band-pass filter.

The voltage of $V_x[n]$ is sampled once ϕ_x transitions from high to low. $V_x[n]$ is described by its previous value, $n - 1$, and the new incoming charge, q_x , during

the time T . The previous value is the sum of two previous samples, its own that is scaled by α_1 and from the prior phase that is scaled by α_2 . Both of these samples follow the principle of voltage sampling while the present sample relates to charge sampling and is therefore scaled by k . Each signal path generates its own transfer function as seen in eq. 2.23, 2.24, 2.25, and 2.26.

$$V_{0^\circ}[n] = kq_{0^\circ}[n] + \alpha_1 V_{0^\circ}[n-1] + \alpha_2 V_{270^\circ}[n-1] \quad (2.23)$$

$$V_{90^\circ}[n] = kq_{90^\circ}[n] + \alpha_1 V_{90^\circ}[n-1] + \alpha_2 V_{0^\circ}[n-1] \quad (2.24)$$

$$V_{180^\circ}[n] = kq_{180^\circ}[n] + \alpha_1 V_{180^\circ}[n-1] + \alpha_2 V_{90^\circ}[n-1] \quad (2.25)$$

$$V_{270^\circ}[n] = kq_{270^\circ}[n] + \alpha_1 V_{270^\circ}[n-1] + \alpha_2 V_{180^\circ}[n-1] \quad (2.26)$$

A simplification can be made by using differential signals as half ($M/2$) the equations are then needed. Let V_{d_1} be defined as $V_{0^\circ} - V_{180^\circ}$ and V_{d_2} as $V_{90^\circ} - V_{270^\circ}$, this gives us eq. 2.27 and 2.28.

$$V_{d_1}[n] = kq_{d_1}[n] + \alpha_1 V_{d_1}[n-1] - \alpha_2 V_{d_2}[n-1] \quad (2.27)$$

$$V_{d_2}[n] = kq_{d_2}[n] + \alpha_1 V_{d_2}[n-1] + \alpha_2 V_{d_2}[n-1] \quad (2.28)$$

Notice how $\alpha_2 V_{d_2}$ in eq. 2.27 has changed sign, one product of $V_{0^\circ} - V_{180^\circ}$ creates an angle subtraction of $270^\circ - 90^\circ$, which is the negative definition of $90^\circ - 270^\circ$ and therefore $-V_{d_2}$.

Further simplification can be made by using a complex definition of our signals. Let q_c be defined as $q_{d_1} + jq_{d_2}$ and V_c as $V_{d_1} + jV_{d_2}$. Why multiple with j one might ask, if one see V_{d_1} as a unit vector with Cartesian coordinate it is $[0, 1]$ and V_{d_2} as $[1, 0]$, the first is pointing to the right while the second one is point up, which are the same as $[1, 0j]$ and $[0, 1j]$ respectively.

With four phases it does not really matter but with higher complexity and more phases it will be a lot easier to express the system with Polar coordinates, or in other words, with complex numbers. With our new definitions we can finally express the relation between the input and output with only one equation as seen in eq. 2.29, and its Z-transform by eq. 2.30. One could express the voltage gain with $z = 1$ into eq. 2.30 but it is a rather lengthy process, a much simpler solution is to use eq. 2.10.

$$V_c[n] = kq_c[n] + \alpha_1 V_c[n-1] + \alpha_2 V_c[n-1]e^{j\pi/2} \quad (2.29)$$

$$\begin{aligned} H_{4/4}(z) &= \frac{V_c(z)}{q_c(z)} = \frac{k}{1 - z^{-1}(\alpha_1 + \alpha_2 e^{j\pi/2})} \rightarrow \\ &\rightarrow \frac{V_{out}(z)}{V_{in}(z)} = \frac{kg_m T}{1 - z^{-1}(\alpha_1 + \alpha_2 e^{j\pi/2})} \end{aligned} \quad (2.30)$$

2.6.2 General M/M

An M/M BPF has M independent single-ended inputs and outputs, phases, g_m -cells, and history capacitors but only one rotational capacitor. The core concept is identical to section 2.6.1 and therefore no detailed explained is given here, the only difference is the share amount of resource and equations. Schematics over the ideal M/M filter can be seen in figure 2.15.

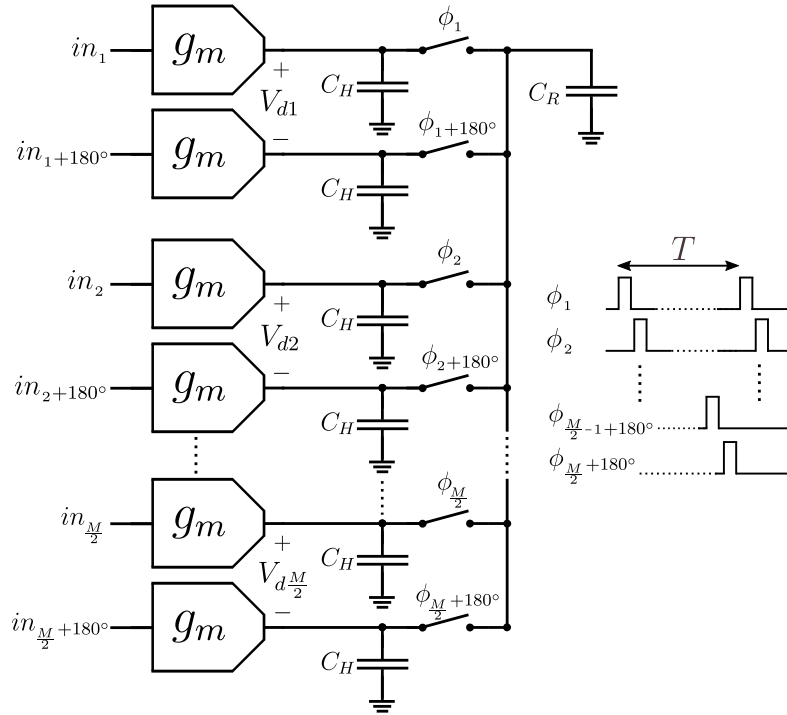


Figure 2.15: Ideal M/M complex band-pass filter.

$M/2$ differential signals are defined, each separated by $360^\circ/M$. Their expression is seen in eq. 2.31.

$$V_{d_x} = \begin{cases} V_{d_1}[n] = kq_{d_1}[n] + \alpha_1 V_{d_1}[n-1] - \alpha_2 V_{d_{M/2}}[n-1] \\ V_{d_2}[n] = kq_{d_2}[n] + \alpha_1 V_{d_2}[n-1] + \alpha_2 V_{d_1}[n-1] \\ V_{d_3}[n] = kq_{d_3}[n] + \alpha_1 V_{d_3}[n-1] + \alpha_2 V_{d_2}[n-1] \\ \vdots \\ V_{d_{M/2}}[n] = kq_{d_{M/2}}[n] + \alpha_1 V_{d_{M/2}}[n-1] + \alpha_2 V_{d_{(M/2)-1}}[n-1] \end{cases} \quad (2.31)$$

To further simplify and solve for the system transfer function we need to define a complex input and output, these are in turn the voltage sum of all differential

voltages, $V_{d_x}[n]$, from eq. 2.31 and multiplied by its corresponding phase shift, $e^{j2\pi(x-1)/M}$, the same concept is also true for all charge packets. This results in eq. 2.32 and 2.33 which together gives 2.34 and its Z-transform by 2.35.

$$V_c[n] = \sum_{x=1}^{M/2} V_{d_x}[n] e^{j2\pi(x-1)/M} \quad (2.32)$$

$$q_c[n] = \sum_{x=1}^{M/2} q_{d_x}[n] e^{j2\pi(x-1)/M} \quad (2.33)$$

$$V_c[n] = q_c[n] + \alpha_1 V_c[n-1] + \alpha_2 V_c[n-1] e^{j2\pi/M} \quad (2.34)$$

$$\begin{aligned} H_{M/M}(z) &= \frac{V_c(z)}{q_c(z)} = \frac{k}{1 - z^{-1}(\alpha_1 + \alpha_2 e^{j2\pi/M})} \rightarrow \\ &\rightarrow \frac{V_{out}(z)}{V_{in}(z)} = \frac{k g_m T}{1 - z^{-1}(\alpha_1 + \alpha_2 e^{j2\pi/M})} \end{aligned} \quad (2.35)$$

As seen in the equation above, higher orders of M do not create more poles and keeps the voltage gain fixed. Only the poles placement is changed, a more details exploration of this are given in section 2.6.4. The Voltage gain is best calculated with 2.10 due to the complexity. For simplicity's sake the transfer function of a 4/4 and 8/8 system are given in eq. 2.36 and 2.37 as they are the most common M/M band-pass filters.

$$H_{4/4}(z) = \frac{k}{1 - z^{-1}(\alpha_1 + \alpha_2 e^{j\pi/2})} \quad (2.36)$$

$$H_{8/8}(z) = \frac{k}{1 - z^{-1}(\alpha_1 + \alpha_2 e^{j\pi/4})} \quad (2.37)$$

2.6.3 General $M/2M$

The $M/2M$ band-pass filter is built upon the M/M and uses the same resources with an additional doubling of switches, phases and C_H capacitors as depicted in figure 2.16. From these extra components an additional low-pass filter is gained, which further helps with filtering as the effective filters Q-factor is increased. The concept of the $M/2M$ filter is more or less a combination of the first order low-pass filter and the 4/4 band-pass filter from section 2.5.1 and 2.6.1 respectively.

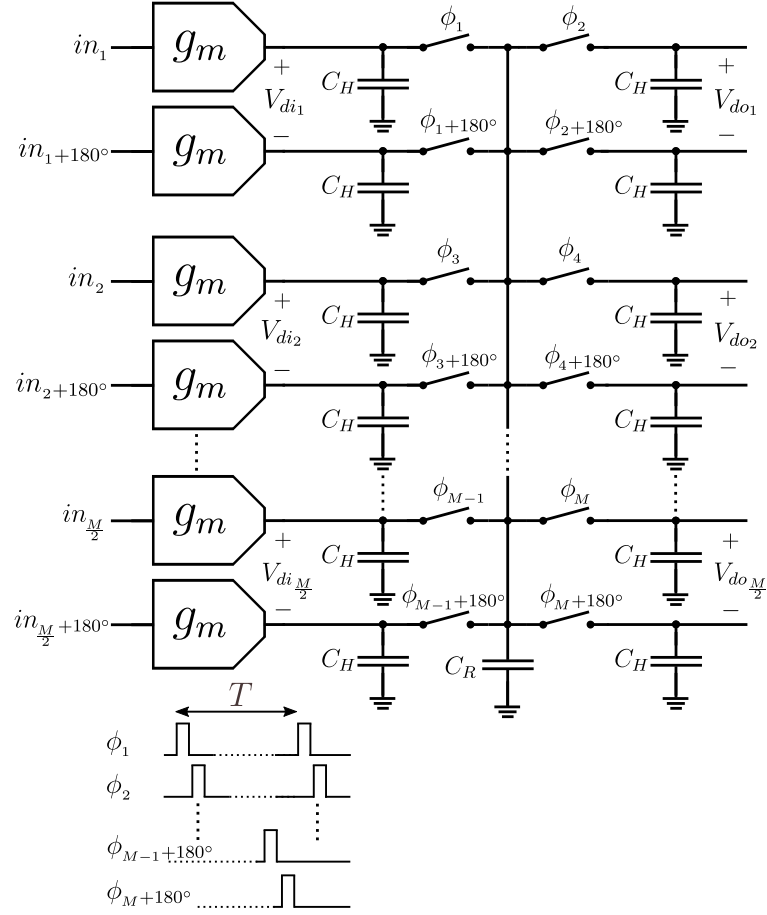


Figure 2.16: Ideal $M/2M$ complex band-pass filter.

Let the differential voltage created by two g_m -cells over its corresponding C_H capacitor be called V_{di_x} and its output by V_{do_x} , $x = 1, 2, 3 \dots M/2$. The input to output relation follows the same principle as given from eq. 2.23-2.26 and 2.11. By following the same concept, we can express the V_{di_x} and V_{do_x} as seen in eq. 2.38 and 2.39.

$$V_{di_x} = \begin{cases} V_{di_1}[n] = kq_{di_1}[n] + \alpha_1 V_{di_1}[n-1] - \alpha_2 V_{do_{\frac{M}{2}}}[n-1] \\ V_{di_2}[n] = kq_{di_2}[n] + \alpha_1 V_{di_2}[n-1] + \alpha_2 V_{do_1}[n-1] \\ V_{di_3}[n] = kq_{di_3}[n] + \alpha_1 V_{di_3}[n-1] + \alpha_2 V_{do_2}[n-1] \\ \vdots \\ V_{di_{\frac{M}{2}}}[n] = kq_{di_{\frac{M}{2}}}[n] + \alpha_1 V_{di_{\frac{M}{2}}}[n-1] + \alpha_2 V_{do_{(\frac{M}{2}-1)}}[n-1] \end{cases} \quad (2.38)$$

$$H_{4/8}(z) = \frac{k\alpha_2}{(1 - \alpha_1 z^{-1})(1 - \alpha_1 z^{-1} - \frac{e^{j\pi/2}\alpha_2^2 z^{-1}}{1 - \alpha_1 z^{-1}})} \quad (2.46)$$

$$H_{8/16}(z) = \frac{k\alpha_2}{(1 - \alpha_1 z^{-1})(1 - \alpha_1 z^{-1} - \frac{e^{j\pi/4}\alpha_2^2 z^{-1}}{1 - \alpha_1 z^{-1}})} \quad (2.47)$$

2.6.4 Pole Placement

The pole placements from eq. 2.36, 2.37, 2.46 and 2.47 are illustrated in the complex plane by showing how the poles move from a big C_H and a small C_R to the opposite of a small C_H and big a C_R , or in other words from $\alpha_1 = 1, \alpha_2 = 0$ to $\alpha_1 = 0, \alpha_2 = 1$ from eq. 2.5 and 2.6. No matter what filter configuration is used the poles are always located at $e^{j0\pi}$ when $\alpha_1 = 1, \alpha_2 = 0$.

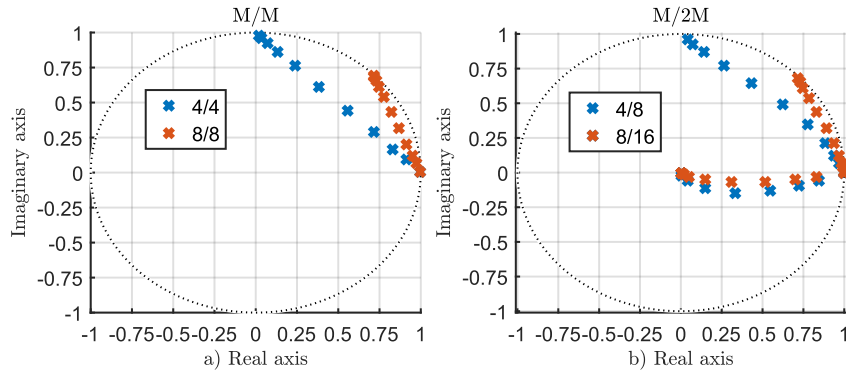


Figure 2.17: Pole movements from $\alpha_1 = 1, \alpha_2 = 0$ to $\alpha_1 = 0, \alpha_2 = 1$, a) shows the poles for a M/M while b) shows the $M/2M$. All poles starts at $e^{j0\pi}$.

As depicted in figure 2.17, both a) and b), the M/M and $M/2M$ following a similar pattern, the 4/4 and 4/8 ends at $e^{j\pi/2}$ while the 8/8 and 8/16 ends at $e^{j\pi/4}$. One important outcome from this figure is the distance between the pole to the unit-circle, as a short distance is equivalent to obtaining a high Q-factor.

From this a conclusion can be drawn, best performance is only attained in the end points. If $C_H \gg C_R$ one is compelled to use a low IF, as increasing the IF one must also increase the sample rate to no lower the effective Q-factor. With $C_R \gg C_H$ the sample rate can be lowered a lot, maybe even too much as for a 4/4 or 4/8 the highest Q is achieved with a IF of $f_s/4$ while $f_s/8$ for a 8/8 or 8/16, the IF are therefore very close to $f_s/2$ and will increase the risk of aliasing issues. Another issue with a low C_H is the degradation of its Sinc filter performance.

2.6.5 Validation

The derivation within section 2.6 was validated by comparing the theoretical AC response from eq. 2.36, 2.37, 2.46 and 2.47 with the frequency response from a PSS + PAC simulation. The same parameters were used in both setups, $C_H = 40 \text{ pF}$ (single-ended value), $C_R = 1 \text{ pF}$ and $f_s = 4 \text{ GHz}$. The center frequency, f_c , of a M/M and $M/2M$ filter can be approximated with eq. 2.48 and 2.49, respectively.

$$f_{c,M/M} \approx \frac{f_s}{2\pi} \arctan\left(\frac{C_R}{C_H} \sin\left(\frac{2\pi}{M}\right)\right) \quad (2.48)$$

$$f_{c,M/2M} \approx \frac{f_s}{2\pi} \arctan\left(\frac{C_R}{C_H} \sin\left(\frac{\pi}{M}\right)\right) \quad (2.49)$$

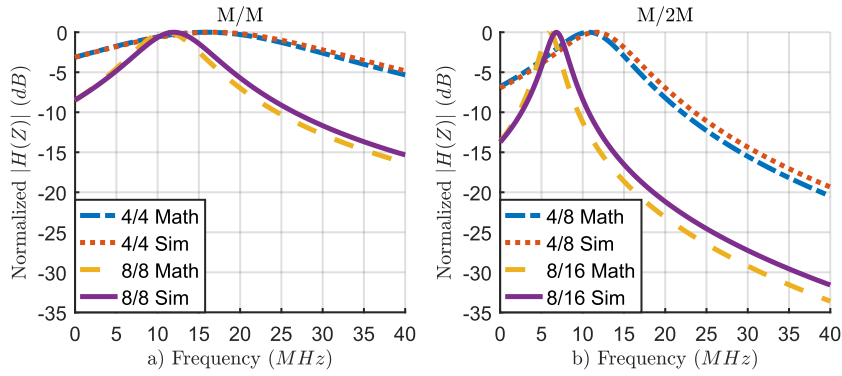


Figure 2.18: Comparison between theory and simulation results, a) shows the M/M while b) shows the $M/2M$.

The overall response from figure 2.18 shows a very good match between theory and simulation, although all filters from simulation shows a minor shift towards a higher center frequency, this is presumably caused by parasitic capacitance in the non-ideal switch which will effectively increase C_R and thus increases the frequency. Non-ideal components were used to ease simulation, perfect switches with PSS introduce strange behaviours.

A comparison between the four filters were concluded by comparing each filters attenuation at an offset of one octave from its center frequency. In order of lowest attenuation, the 4/4, 8/8, 4/8 and 8/16 attains of 3.2, 8.7, 9.6 and 14.8 dB, respectively.

However, this comparison is somewhat flawed as the center frequency is not the same. By tweaking C_R such that each filter has their center frequency at 5 MHz and looking at the attenuation at an offset of one decade, 50 MHz. The order of lowest attenuation is still the same, the 4/4, 8/8, 4/8 and 8/16, but the attenuation is now 19.2, 27.0, 37.4 and 40.1 dB, respectively. All but the 8/8 gives an almost

theoretical response as a first or second-order filter. Which shows that the filter order is not the whole picture, it is also the pole placement that impacts the effective order.

2.7 Pipeline and/or Parallelization

An easy and common way of creating the different clock phases that any discrete-time filter require is to divide a reference clock into several phase, though with a lower frequency. There are several ways of implementing this divider and the point here is not to implement it but rather to highlight that infinite number of phases can be created. However, they will always have a lower frequency than the reference clock, the more one divides, the low the frequency one get.

The reference clock in question is normally created by a Phase-Locked Loop (PLL), which is a versatile frequency generator. The generated clock is created and distributed as a differential-pair as it will suppress common-mode noise [13]. With a differential reference clock, we also gain an additional rising and falling edge under one reference period, effectively doubling the frequency. An example is illustrated in figure 2.19 where a differential reference clock is divided into four phases that will have a frequency of $f_{ref}/2$. The general relation between sample rate and reference clock is given by eq. 2.50.

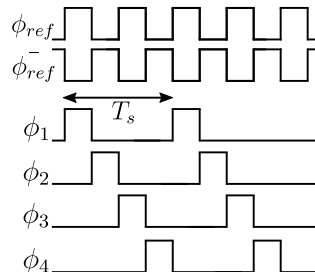


Figure 2.19: Division of a differential reference clock into four phases, its period T_s will therefore be doubled compared to its reference clock.

$$f_s = \frac{2f_{ref}}{M} \leftrightarrow f_{ref} = \frac{Mf_s}{2} \quad (2.50)$$

Where M is the number of phases

As the reference clock will always be higher than the sampling rate an upper limit exist. As an example, a 8/16 DT-BPF running with a sample rate of 8 GHz would require a reference clock of 64 GHz, which is an all too high frequency for a low power device and would increase the complexity substantially to generate such a high frequency.

An easy solution to lower the necessary reference clock is to implement a pipelined version of the discrete-time filter. An illustration of this concept is depicted in figure 2.20 of a generic DT filter that require four phases ϕ_1 , ϕ_2 , ϕ_3 and ϕ_4 . The 1X generic filter samples the input with ϕ_1 and updates the output with ϕ_4 while ϕ_2 and ϕ_3 perform some internal function.

By introducing a copy of the generic DT filter, we can double the sample rate, the key part here is to run the second blocks with ϕ_3 as its first phase, otherwise there is no equal-distance sampling. By yet again doubling the generic filter the sample rate is once more doubled, and to fulfill the equal-distance sampling each block must have a unique starting phase. Note that the history capacitor, C_H , is kept unchanged in both terms of capacitance and unique instances.

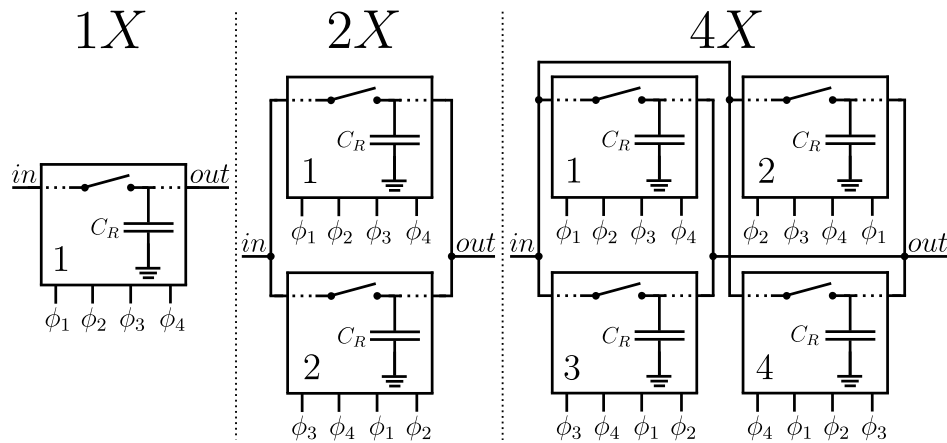


Figure 2.20: Concept of pipelining a discrete system to effectively increase its sample rate, 1X, 2X and 4X will sample at a frequency of f_s , $2f_s$ and $4f_s$ respectively.

2.8 Harmonic Rejection

The mixer in figure 1.1 will down-convert all harmonics of its LO frequency to DC, given that its waveform is a square wave. Only the fundamental frequency is of interest, all other harmonics are unwanted and must be removed or at least attenuated to a negligible level. Otherwise, once the down-conversion has happened, all residual of harmonics is undistinguished from each other.

The first step is to implement a fully differential mixer as it will remove the down-conversion of even harmonics by cancellation. Which leaves us with only the odd harmonics left, the obvious solution is to attenuate frequencies higher than LO before it reaches the input of the mixer. This can either be achieved with a high-order low-pass filter or multiple of notches centred at the unwanted odd harmonics. In practice the implementation of this low-pass filter is not suitable due to the need of active filters, not to degrade the noise figure further, and by

using active filters at GHz the system will consume huge amounts of power due to the need of high bandwidth within the active parts. On the other hand, multiple of notches requires multiple of inductors and capacitors with a high Q-factor, which is in theory plausible but on-chip inductors requires huge amount of area.

Another drawback is the tunability, given the frequency span from table 3.1 with some additional margin, which gives 0.4 to 2.4 GHz , the f_{max}/f_{min} ratio is then equal to 6 which is also the ratio of Q_{max}/Q_{min} as it is proportional to $\sqrt{L/C}$, thereby implies that even with a good Q-factor of 18 it would reach a useless Q-factor of 3 at the lowest frequency.

A more practical solutions is to increase the number of phases that drives the mixer, from the typical four to six or even eight phases. With six phases it is theoretical possible to remove all components of the third harmonic while eight phases can remove the third and fifth harmonics.

This is achieved by combining a scaled sum of a phase and its next two forthcoming phases. For example, with eight phases, ϕ_1 to ϕ_8 , the first phase, ϕ_1 , will combine ϕ_1 , ϕ_2 and ϕ_3 while the last phase, ϕ_8 , will combine ϕ_8 , ϕ_1 and ϕ_2 . The second signal phase in this order are scaled with a factor of $\sqrt{2}$ while the rest stay constant (scaled by 1). This will in turn scale the wanted signals by $1 + \sqrt{2}$ while the third and fifth harmonics cancel each other out as illustrated in figure 2.21.

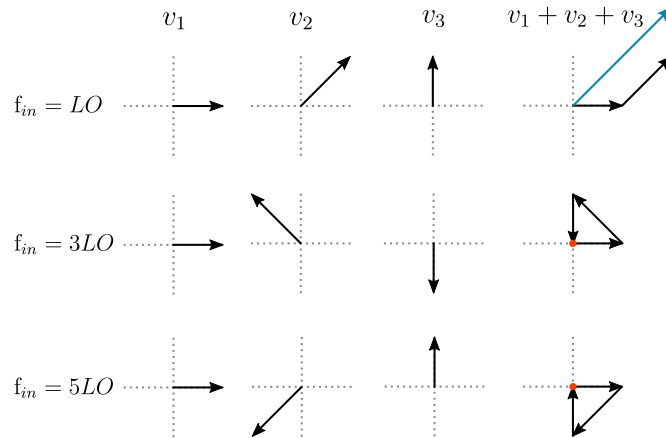


Figure 2.21: Concept of harmonic rejection with 8 phases, v_1 shows the starting positions while v_2 and v_3 shows the forthcoming position. With f_{in} equal to LO the step size is one while with $3LO$ and $5LO$ the step size is three and five, respectively. $v_1 + v_2 + v_3$ shows the sum of these three vectors, f_{in} equal to LO increases the length while $3LO$ and $5LO$ are cancelled.

The illustration above assumes that all phases are scaled perfectly and if any phase shift occurs it happens on all phases, meaning no relative phase error between the phases or that its length differs. In reality a small error will always occur in

both amplitude and phase, thus greatly reducing the performance of a harmonic rejection stage.

Given a scenario of a circuit that performs only 20 dB of harmonic rejection due to mismatches, but the necessary attenuation is 40 dB. One could think that the solution is to add another, identical circuit, after the first one to fulfill the 40 dB. But due to mismatches new vector products could be created from the first stage, in which, interfere with the second circuit and thus reducing the overall performance.

An example of this is illustrated in figure 2.22 where a theoretical perfect 8 phase harmonic rejection circuit are fed with almost perfect vectors, the first vector, ϕ_1 , has an angular error of 1° while the rest are flawless, all has a length of one. a) shows the residual vectors of the third harmonic after the first stage, if no errors were introduced then all vectors should be zero.

However, this is not the case and one can clearly see residuals of ϕ_1 , ϕ_7 and ϕ_8 . These are then the input together with the first harmonic to the second stage in which b) shows the output of the third harmonic, once again there is residual vectors. But the most important aspect here is that there are more content, in both number of phases and amplitude.

By adding a second stage to our scenario one has not improved the situation but rather the opposite, the overall performance is worse. This highlights the need for very low mismatch and a separate calibration scheme for each additional circuit to achieve the required rejection.

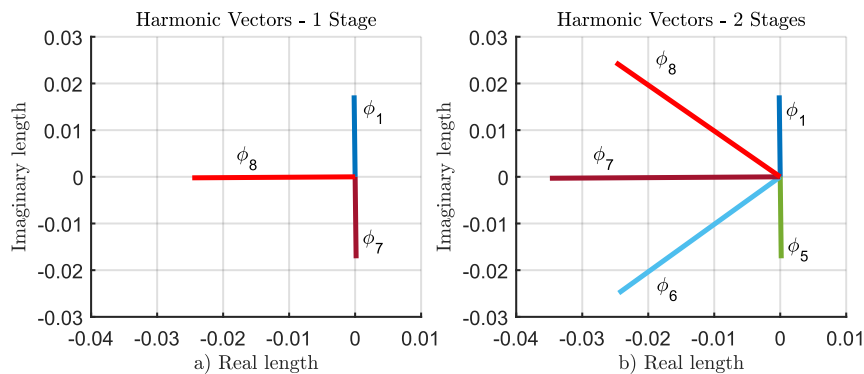


Figure 2.22: Residual of the third harmonic with a theoretical 8 phase harmonic rejection circuit where one phase as an error of 1° , a) shows the content after the first stage while b) shows the second stage.

The problem with harmonics rejection can also be seen as the well-known issue of low rejection of the image frequency, caused by the non-orthogonality between the I and Q channel, or in other words, a phase and/or amplification error of the 0deg

degree vector and the 90deg vector (ϕ_1 and ϕ_3 in our example with eight phases) and will increase the reception to a image frequency. This is known as the Image Rejection Ratio (IMRR) and is given by eq. 2.51.

$$IMRR = \frac{G^2 + 1 - 2G\cos(\phi)}{G^2 + 1 + 2G\cos(\phi)} \quad (2.51)$$

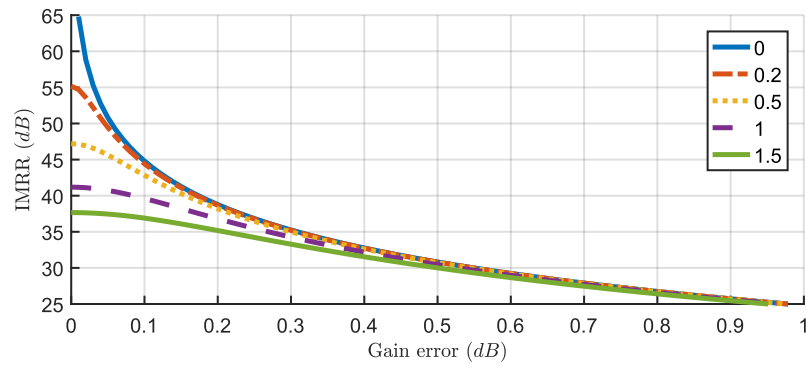


Figure 2.23: Theoretical image rejection ratio with gain error between 0 to 1 dB and a phase error from 0° to 1.5°.

3GPP NB-IoT Standard and Receiver Specification

The 3rd Generation Partnership Project (3GPP) is a collaboration between radio manufactures, mobile network operators and partners working together to standardise the worlds mobile telecommunication. 3GPP is divided into several technical specification groups (TSG) as the Radio Access Network (RAN) that are responsible of the requirements and its interface of, to name a few, the UTRA, E-UTRA and NB-IoT. Each TSG consist of several Work Groups (WG) that are in turn responsible of a smaller part of the TSG responsibility, as the RAN WG1 group that handles the Radio Layer 1 specifications.

All 3GPP standards are structured as *Releases* and as of January 2019, 15 releases have been published. Release 13 contains the first specification of NB-IoT, followed by release 14 and 15 that contain minor changes and further radio bands for NB-IoT. The main focus of NB-IoT is high connection density, low power and long range for mobile communication were high latency and low throughput are of no concern, notably battery powered sensors. NB-IoT reuses nearly all the LTE design, hopefully reducing the time to develop a product that meet its specification.

NB-IoT uses a Quadrature Phase Shift Keying (QPSK) as modulation, Orthogonal Frequency-Division Multiple Access (OFDMA) in the downlink and 200 *KHz* of bandwidth, where 90 percent is signal content (180 *KHz*) while the rest 10 percent (20 *KHz*) as a guard band to the next channel. A NB-IoT channel can be placed as *in-band*, *guard band* or *stand-alone* as illustrated in figure 3.1 The peak theoretical data transfer from a User Equipment (UE) perspective to receive and transmit are 226.7 and 250 *kb/s* respectively [14]. This is of course a best-case scenario and should be compared to the worst case where maximum number of repetitions is used, the data rate is then ~ 25 b/s.

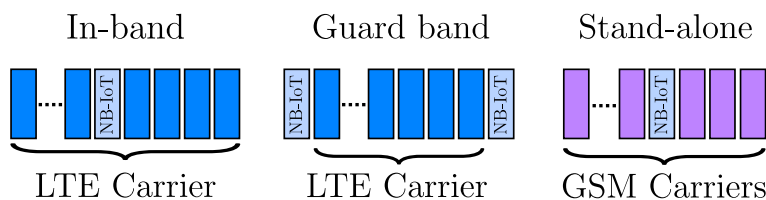


Figure 3.1: Illustration where a NB-IoT channel can be placed, either as in-band, guard band or stand-alone.

In this thesis look at "*LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception (3GPP TS 36.101 version 15.3.0 Release 15)*" [15], and as this thesis only cover the receiver side only chapter 7 (receiver characteristic) in [15] will be covered.

3.1 Frequency Bands

NB-IoT uses several different frequency bands within the air interface of E-UTRA, as in release 13, the whole receiver spectrum can be grouped into two collections of bands that we will call Lowband (LB) and Highband (HB), making the implementation of a front-end filter rather simple as only two filters are needed. However, in release 14 and 15, new bands were introduced that complicates the implementation of this filter as these bands are outside of the LB and HB.

The new bands can be grouped together into what we will call Ultra-Lowband (ULB) and midband (MB). With two more collections of bands, two more front-end filters are needed. Furthermore, the bandwidth in LB was also increased from 231 to 343 MHz forcing the filter to be of a lower Q-factor or variable, if it is a resonant circuit, or even splitting up the band into two smaller bands with different filters that further complicates the implementation. A summary of all bands can be seen in table 3.1.

Table 3.1: A collection of four distinct receiver bands as defined in release 13 and 15.

	Release 13	Release 15
ULB (MHz)	-	461-467.5
LB (MHz)	729-960	617-960
MB (MHz)	-	1475-1518
HB (MHz)	1805-2200	1805-2200

It is worth mentioning that it is not compulsorily for a manufacture to cover all bands. By covering fewer bands, the implementations gets easier and cost less to develop but the receiver now lacks certain bands, thus decreases the market. In

other words, it is arguable of what is better; a single receiver that cost more but covers all bands or several receivers that are cheaper but are limited to a certain band.

3.2 Signal Power and Noise Floor

The weakest signal power, $P_{RF,min}$, that the receiver must be able to translate is -108.2 dBm while the strongest, $P_{RF,max}$, is -25 dBm . At room temperature (290 K) the thermal background noise is -174 dBm , and with a bandwidth of 200 KHz the total noise power, N_{th} , is thereby -121 dBm , as given from eq. 3.1. This means that any NB-IoT receiver will have a theoretical maximum Signal to Noise Ratio (SNR) of 12.8 dB ($121 - 108.2$) at $P_{RF,min}$, this will of course be lower in practice as both analog and digital parts of the receiver will always add noise. Although, at higher signal powers the SNR will increase.

$$kT = -174 \text{ dBm} = 3.98 \text{ aW} \rightarrow N_{th} = kTB = 796.2 \text{ fW} = -121 \text{ dBm}$$

Where k is the Boltzmann constant, T for temperature in Kelvin (3.1)
and B as the bandwidth in Hz

3.3 Receiver Test Cases

A NB-IoT receiver is validated by passing six difference tests, the Adjacent Channel Selectivity (ACS), In-Band Blocking (IBB), Out-of-Band Blocking (OBB), Intermodulation (IM), Spurious Response (SR) and Spurious Emission (SE). However, SR and SE will not be covered in this thesis as SR is covered by the OBB test while SE sets requirement on the LNA which in turn is outside the scope of this thesis. The purpose of these tests is to validate a receiver with scenarios that corresponds to real life situations that typically cause problems. Although, the tests will never cover all possible combination that can happen in the real-world, though they will cover the most probable causes of interference.

In theory, no receiver is needed, as a single channel ADC can receive the wanted signal, to be later filtered in the digital domain, but in practice it makes no sense in terms of cost, complexity and energy consumption. This is due to the share amount of required performance, give or take, one needs a resolution of ~ 20 bits at a sampling frequency higher than 20 GHz to handle the span of input power and frequencies, both in terms of wanted and interference signals.

The minimum resolution, or bit depth, of an ADC depends on the receiver's ability to attenuate interference as less attenuation will demand higher Dynamic Range (DR) of the ADC. The overall goal is to reduce the required resolution as much as possible, as power consumption of an ADC increases with resolution. But in practice there is always a balance between attenuation and resolution. A rough estimate of the minimum resolution, given the DR or vice versa, is given by eq.

3.2 [16], note that this equation assumes a sinusoidal signal and is not valid for a modulated signal, although it gives a good rule of thumb.

The minimum sampling rate of an ADC has the same dependency as any discrete-time filters, although it's not the DR but rather, what is the highest frequency of signal and interference that the ADC should handle? As an example, given an ADC with enough DR, an IF at 2 MHz and an interference at 3 MHz that is impossible to remove, the absolute lowest sampling rate is thereby 6 MHz, although some extra margin is always good to have.

In the forthcoming sections the term f_{Δ} and f_{BW} are shown. Δ is defined as the interference offset from a NB channel edge, or just IF + 0.2 MHz, while BW is its bandwidth. As an example, $f_{\Delta} = f_{BW} = 1$ MHz means that the interference spans between IF + 0.5 to IF + 1.5 MHz.

3.3.1 Adjacent Channel Selectivity

The ACS test validates a receiver to withstand transmissions from a base station at a neighbour channel while still being able to receive a weaker signal of interest. The main point of the ACS is to test a receiver for interference that are very close to the wanted signal and highlights the need of a sharp filter to attenuate this interference. Nonetheless, the power difference between the interferer, P_i , and signal, P_s , is the lowest of all tests as seen in table 3.2.

Table 3.2: Summary of the adjacent channel selectivity test 1 and 2, as defined from 3GPP in table 7.5.1F.

Test	P_s (dBm)	P_i (dBm)	f_{Δ} (MHz)	f_{BW} (MHz)	Type
1.1	-94.2	-66.2	± 0.2	0.2	GSM
1.2	-94.2	-61.2	± 2.5	5	E-UTRA
2.1	-53	-25	± 0.2	0.2	GSM
2.2	-58	-25	± 2.5	5	E-UTRA

3GPP defines the ACS test into two sub-tests, 1 and 2, in which each consist of two separated tests with different type of interference, GSM and E-UTRA. The second test is quite similar to the first test as the relative difference is almost the same, the only difference is the absolute values of the signal and interferer. With figure 2.18 in mind, it is safe to say that a minimum amount of attenuation is possible, thus at least 33 dB (94.2 - 61.2) of DR is required.

3.3.2 In-Band Blocking

The IBB test is quite similar to ACS as the interference is still close to the carrier. However, the interference is stronger while the wanted signal is weaker. This interference represent a transmission from a base station of a E-UTRA channel that allocates 5 MHz of bandwidth.

Table 3.3: Summary of the in-band blocking test 1 and 2, as defined from 3GPP, table 7.6.1.1F-1.

Test	P_s (dBm)	P_i (dBm)	f_{Δ} (MHz)	f_{BW} (MHz)	Type
1	-102.2	-56	± 7.5	5	E-UTRA
2	-102.2	-44	± 12.5	5	E-UTRA

The IBB test is divided into two sub-tests in which both tests the interference type, bandwidth and the signal strength of the carrier are identical, the only difference is the interference strength and offset from the carrier. If no attenuation of these interferer is attained it will result in a DR of 46.2 and 58.2 *dB* for sub-test 1 and 2 respectively.

Although it is possible to get a couple of *dB* of reduction with a 4/8, 8/8 or 8/16 DT-BPF, particularly with sub-test 2 as it is further from the carrier. It is worth mentioning that with an IF of 10 *MHz* the second sub-test is close to the image frequency.

3.3.3 Out-of-Band Blocking

There is a major difference that comes with the OBB in comparison to the other tests, namely the offset frequency of the interference as it is not a single point but a whole span of frequencies, this complicates the test, especially sub-test three as it will included all harmonics that exist under 12.75 *GHz* and hence the need of harmonics rejection.

The OBB test do not particularly correspond to any real transmission from a base station, instead the test is more of a synthetic check to test the receiver of an unknown and unforeseen interferer over the whole spectrum. Furthermore, the OBB test has the strongest interference of all tests, although the type is Continuous Wave (CW) which is easier to handle due to, to name a few, low PAR value and bandwidth.

Table 3.4: Summary of the out-of-band blocking test 1, 2 and 3, as defined from 3GPP, table 7.6.2.1F-1.

Test	P_s (dBm)	P_i (dBm)	f_{Δ} (MHz)	Type
1	-102.2	-44	$f_c - (15 \text{ to } 60)$	CW
			$< f_c <$ $f_c + (15 \text{ to } 60)$	
2	-102.2	-30	$f_c - (60 \text{ to } 85)$	CW
			$< f_c <$ $f_c + (60 \text{ to } 85)$	
3	-102.2	-15	1 to $f_c - 85$	CW
			$< f_c <$ $f_c + 85 \text{ to } 12750$	

The OBB test is divided into three sub-tests, the first is an easier variant to the second IBB test as the interferer type is CW and further away from the carrier. However, because of the span up to ± 60 MHz and with the given IF of 10 MHz the interferer will hit the image frequency. With zero attenuation within the receiver chain a minimum of 58.2 dB (102.2 - 44) of DR is required, although with an I and Q channel within the ADC, 43 dB of rejection is possible with software (figure 2.23, gain error of 0.1 dB and a phase error of 0.5°).

Furthermore, if we assume zero attenuation on all sub-tests the required DR are thereby 58.2, 72.2 and 87.2 dB, although it is possible to greatly attenuate the interference from sub-test 2 and 3.

3.3.4 Receiver Intermodulation

The receiver intermodulation test is the only test that has more than one concurrent interferer. The interference could correspond to two simultaneous transmissions from a base station where one is below while the other is above the wanted signal, although the test is quite synthetic as it is implemented to test the receiver's linearity with a basic two-tone test.

Table 3.5: Summary of the receiver intermodulation test 1 and 2, as defined from 3GPP, table 7.8.1F-1

Test	P_s (dBm)	P_i (dBm)	f_{Δ} (MHz)	f_{BW} (MHz)	Type
1	-96.2	-46	± 2.2	NA	CW
2	-96.2	-46	± 4.4	1.4	E-UTRA

The test is yet again defined into two sub-test, both of these have the same signal and interference strength, however the type and offset are different. The interference in the first sub-test is of type CW and are very close to the wanted signal.

The second sub-test is further from the wanted signal and its type is now a modulated E-UTRA interferer. But as the strength is the same the two sub-test will give the same DR of 50.2 dB (96.2 - 46), with the assumption of zero attenuation.

3.4 Summary

To summarise the four tests and the requirement it will set on a receiver a DR mask was created as seen in figure 3.2. The mask starts relative from the IF and is in reality symmetrical around IF, however one side is only depicted. The image frequency is always located at $-f_{IF}$ per definition, which corresponds to $2f_{IF}$ in the figure. Note, by turning the figure upside down, one attains a filter mask on how much attenuation is needed at a given offset from the IF to achieve the same level between signal and interferer.

The goal here is to determine the minimal DR within the ADC, which can in theory always be reduced with more filtering but in practice there is always a trade-off, an equal amount of complexity is general the best solution in both development time, power consumption and performance.

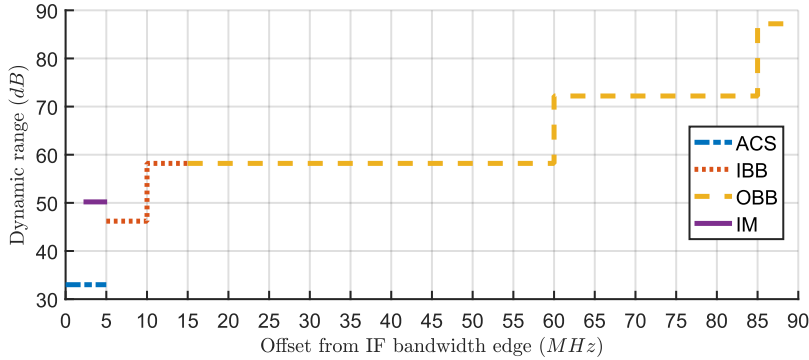


Figure 3.2: Dynamic range mask for NB-IoT with the assumption of zero attenuation within the receiver.

Continuing with DR of an ADC, the highest level it can handle is given by the Full Scale (FS), which is normally the upper limit of its supply. With a supply voltage of 1 V the FS limit is thereby 10 dBm peak (Assuming 2 V_{pp} differential with 50 Ω). The lowest level is set by the quantization noise floor, QN in eq. 3.3, any signal below this level is undistinguished from the conversion rounding errors.

These two limits are of course the theoretical limits, margin is needed on both. Starting with the upper limit, M_{FS} represents a margin to cover all types of variations caused by PVT, 6 dB is a good assumption [11, 17]. Further margin is needed due to power variation of OFDM modulation, also known as Peak-to-Average Ratio (PAR), M_{PAR} of 9 dB will handle the peaks [17].

For the lower limit, 16 dB margin is required to stop further degradation by quantization noise to only 0.1 dB, given by eq. 3.4 [11, 17]. Furthermore, the QPSK coding scheme requires another 10 dB (SNR_{QPSK}) to keep the bit error rate below 10^{-4} [17]. One can of course reduce the SNR and sacrifice data rate, at an SNR of 6 dB the expected error rate is 10^{-3} .

By now the min, max and range of signal levels that the receiver must be able to output to the ADC at any RF power between $P_{RF,min}$ and $P_{RF,max}$ can be calculated from eq. 3.6, 3.5 and 3.7. The receiver min and max gain are also extracted from eq. 3.8 and 3.9.

$$DR = 6.02N + 1.76 \rightarrow N = \frac{DR - 1.76}{6.02} \quad (3.2)$$

$$QN = FS - DR \quad (3.3)$$

$$M_{QN} = 10 \log(10^{0.1/10} - 1) = -16.32 \quad (3.4)$$

$$P_{ADC,max} = FS - M_{PAR} - M_{FS} \quad (3.5)$$

$$P_{ADC,min} = QN + SNR_{QPSK} + M_{QN} \quad (3.6)$$

$$P_{ADC,range} = P_{ADC,max} - P_{ADC,min} \quad (3.7)$$

$$A_{min} = FS - M_{FS} - P_{RF,max} - M_{PAR} \quad (3.8)$$

$$A_{max} = SNR_{QPSK} + M_{QN} - P_{RF,min} \quad (3.9)$$

Given our case with the assumptions above and a bit depth from 8 to 12 bits, the end results are summaries in table 3.6.

Table 3.6: Dynamic range of the receiver with different bit depths of the ADC, from 8 to 12.

N	DR	QN	$P_{ADC,min}$	$P_{ADC,max}$	$P_{ADC,range}$	A_{min}	A_{max}
8	49.9	-39.9	-13.9	-5	8.9	20	94.3
9	55.9	-45.94	-19.9	-5	14.9	20	88.3
10	62.0	-52.0	-26.0	-5	21.0	20	82.2
11	68.0	-58.0	-32.0	-5	27.0	20	76.2
12	74.0	-64.0	-38.0	-5	33.0	20	70.2

There are several way of decoding everything above, one can derive from the signal, interference or with $P_{ADC,range}$, all leads to the same conclusions. In our case we will use $P_{ADC,range}$ and the assumptions that all signals, including interference, are modulated with OFDM (which is not true for CW or GSM). Furthermore, we will assume that zero attenuation is feasible of the ACS tests. This gives a minimum $P_{ADC,range}$ of 33 dB as the ADC must be able to absorb signal and all ACS interference, which points towards a 12 bit ADC in table 3.6. 12 bits will also give the lowest A_{max} of 70.2 dB.

The next question to ask is, what filter order is required to fulfill the other tests? To answer this, a portion of the mask in figure 3.2 was lumped together with four lines that indicates the ideal attenuation of a filter order from one to four at different IF, seen in figure 3.3. If the mask is above the dotted line, one does not fulfill the requirements, more filtering is needed.

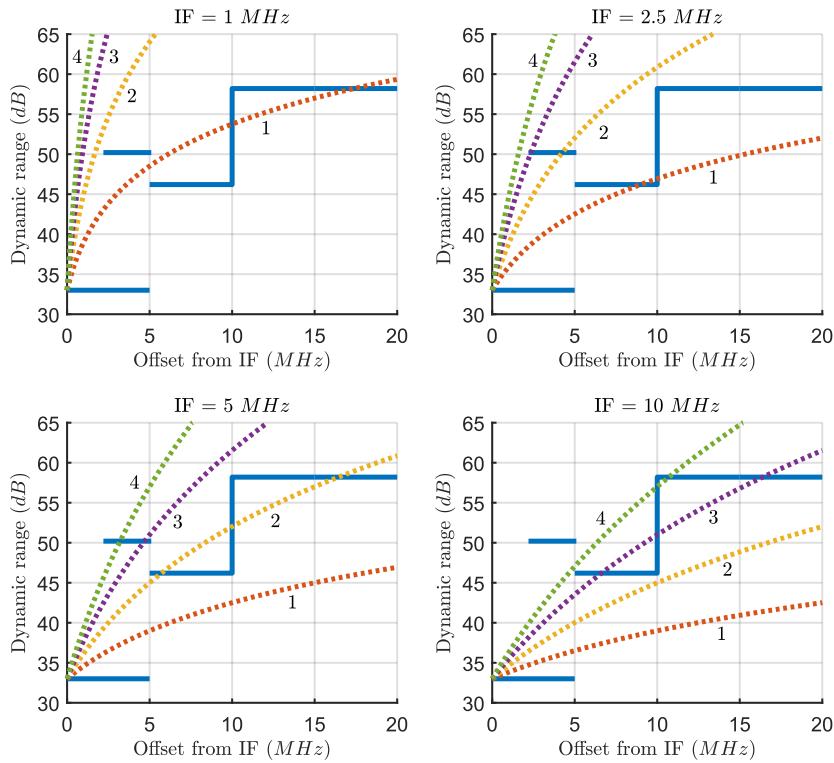


Figure 3.3: Required filter order to fulfill the receiver tests at a IF of 1, 2.5, 5 and 10 MHz, the blue solid line represents the mask while the four dotted lines shows different filter order, marked with 1 to 4.

From the figure above it is clear that the hardest test will be the IM, especially at higher IF. At an IF of 10 MHz only 6.9 dB of attenuation is achieved with a fourth-order filter (IM test at f_{Δ} of 2.2 MHz), if the ADC should also handle this one must increase the resolution by another two bits ($\frac{50.2-39.9}{6} = 1.72$).

Reducing the IF to 1 or 2.5 MHz will make the filters more effective, a fourth-order will be sufficient in both cases. However, with a lower IF the IM2 products might cause issues, given that the linearity is not enough. The highest bandwidth and amplitude product comes from the IBB test, where in theory it will span from 0 to 5 MHz. Once again there is no clear answer, only a choice between two trade-offs.

In any case, given the worst assumption of zero attenuation with IIP calculation from eq. 2.2, 2.3, a margin of 10 dB and zero gain within the receiver chain the requirements on IIP2 and IIP3 are summaries in table 3.7. IIP calculations on all test and their sub-test were performed but only the sub-test that gave the highest IIP requirement is given in the table below.

A word of caution though, eq. 2.2, 2.3 is just an approximation. The given IM level are distributed over several frequencies, which is not accounted for, meaning that one should subtract a few (3-6) dB to obtain the actual require IIP2. Given that a interference is modulated with OFDM the power is spread over its bandwidth, which means that a small portion of its IM products will hit our wanted bandwidth, effectively reducing the IIP requirements by at least 10 dB . However, OFDM has a high PAR value which increases the required IIP. The summarised answer here is that eq. 2.2, 2.3 gives a good approximation but far from the truth.

Table 3.7: Approximate minimum requirements on IIP2 and IIP3, assuming a margin of 10 dB and zero gain within the receiver chain.

	IIP2	IIP3
ACS	18	-3.5
IBB	24.2	-9.9
OBB	82.2	33.6
IM	14.2	-15.9

Low Noise Amplifier and Mixer

As mentioned in section 1.3 both the LNA and mixer are not included in this thesis but is still needed in most simulations to get appropriate results, thus a simple implementation was required.

4.1 Low Noise Amplifier

The LNA was implemented as a differential transconductance amplifier with ideal components, seen in figure 4.1. The single-ended output impedance was 500Ω in parallel with a 200 fF capacitor, creating a LPF at $f_{-3dB} = \sim 1.6 \text{ GHz}$

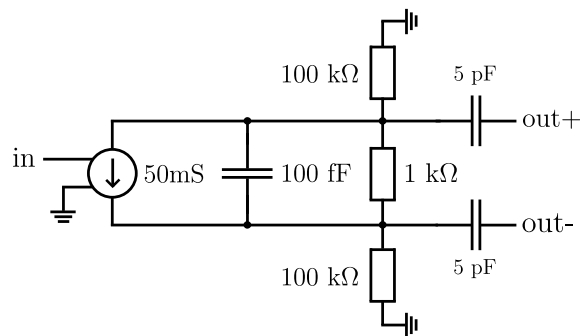


Figure 4.1: Implementation of the ideal differential LNA.

4.2 Mixer

The mixer had to be implemented in CMOS as ideal switches will create deceptive results due to their perfect behaviour. If one simulates with ideal switches, less folding effects appears and down-conversion of infinite harmonics (3rd, 5th, 7th, 9th..) occurs. This is in part caused by the lack of a frequency limit. CMOS

transistors has intrinsic capacitance that creates a upper frequency limit and thus limits the conversion. The mixer is also a core building block of any discrete-time system due to its creation of signal phases.

The mixer was implemented as a fully balanced passive mixer with 4 or 8 phase (depending on which filter was used), working in current mode to achieve better linearity as the voltage swing over the transistors is reduced. The mixer consists of 4 or 8 transistor pairs that creates the same amount of signal phases, respectively. A general implementation of one these pairs can be seen in figure 4.2. The size of M_1 and M_2 were set to $20/0.04 \mu m$, resulting in an on-resistance of $\sim 20\Omega$. The resistance R_{mixer} is not part of the mixer functionality, the sole reason was to ease converges issues with PSS simulations, its value was set high enough to have an negligible degradation of the mixers performance.

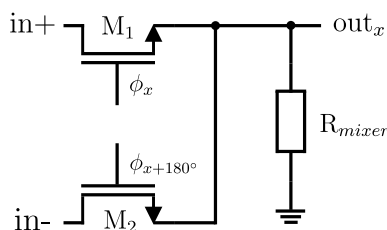


Figure 4.2: Schematic of the Mixer.

In most designs the mixers will have a DC component at its output due LO leakage or an bias network to bias an differential pair of a BB amplifier, this voltage are there to set these transistors in the correct operating region. In this thesis the first BB amplifier is DC coupled with an input capacitor, thus a bias of $0 V$ is possible. This will in turn remove the need to DC-shift the mixers gates as V_{gs} will always be V_{dd} when on and zero when off.

Performance wise the mixer is a critical block and close attention is needed to reduce the impacts of PVT variations. However, nothing is perfect, and a small amount of mismatch will always occur. Figure 4.3 a) shows the mixer response with a LO frequency of $2 GHz$ and no mismatch whatsoever, one can clearly see the theoretical response of only odd harmonics (1st, 3rd, 5th), everything else is suppress by over $140 dB$ (numerical noise floor), While b) shows the same response but with a phase error of 0.4° on one clock phase. The mixer will now down-convert frequencies of all harmonics. The difference between the first and even harmonic is only $48 dB$. This means that an OBB interfeerer around $2LO$, $4LO$ or $6LO$ will be down-converted to the same frequency as the wanted IF and can't be removed with any filter. This highlights the need of a calibration scheme to fix mismatch issues, however, it will not be covered in this thesis.

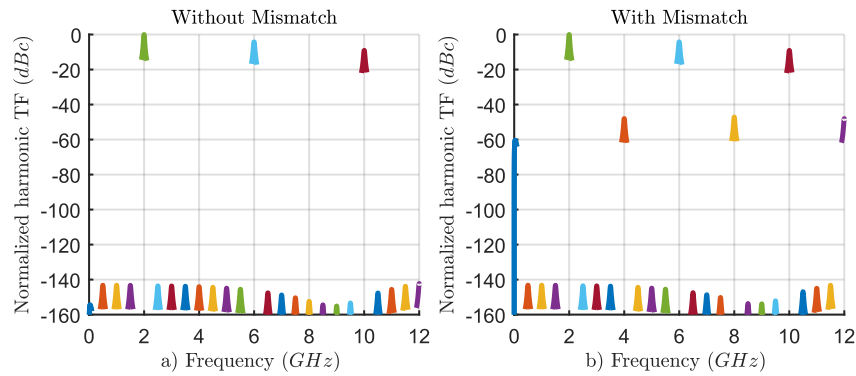


Figure 4.3: Text

4.3 Simulations

The AC response and noise figure were simulated with the LNA and mixer to acquire a reference. A differential capacitor of 7 pF was used as the mixers load on each signal-pair, which creates a LPF with $f_{-3dB} = \sim 20\text{ MHz}$. The result is seen in figure 4.4, the key points are a voltage gain of 28 dB and a noise figure of 1.8 dB at 10 MHz

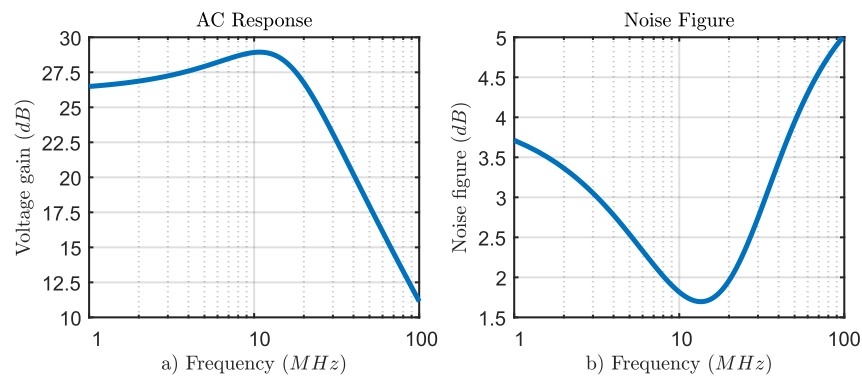


Figure 4.4: Reference figures of the LNA and mixer, a) AC response and b) noise figure.

Discrete-Time Filters

In this chapter a detailed evaluation of the Discrete-Time Band-pass Filter (DT-BPF) is performed by investigating aspects that could have an potential impact on its performance, as switch topology, CM voltage, on-resistance of switches, non-ideal clock sources and sample rate. Furthermore, a short resource overview and a dedicated section on how one should simulate a DT filter are also included. Because of time constrains only results of a 8/8 DT-BPF are shown, although all M/M and $M/2M$ suffers from the same problems, i.e the results should not be viewed as absolute values but rather how the relative performance changes with a certain parameter.

5.1 How to Simulate with Spectre

As with all simulations one will only get answers on what questions are asked and how they are asked, and by asking questions in this context I points towards how the test bench was setup and what you told the simulation-engine to solve for you. With that in mind, discrete-time can be more complicated to simulate compared to continuous-time as they are, in my opinion, more sensitive to the questions being asked and how they are asked. This comes down to the discrete-time, each switch will in a sense act as a sampler, defining a point in time where we go from continuous to discrete. As an example, a discrete-time filter with a sample rate of $f_s = 1\text{ GHz}$ has one of its clocks delayed by as little as 1 ps , this will result in phase shift of 0.36deg ($1/1000*360$) on one of its phases. This small mismatch might degrade the performance significantly but might not be seen due to simplifications within the test bench.

The important thing is, the impact of mismatches and parasitic's will not show its full impact if it is not taken into consideration within the test bench. More than once have I personally been tricked by "too good to be true" results and later realizing when mismatches were taken into considerations the design is more or less useless. This includes, to name a few, reduction in a filters Q-factor, increasing folding effects, diminishing return or even worse when increasing the number of

stages. The impact of the mixer should not be forgotten as it is the block that creates all signal phases. The best way to get the correct result is with multiple of Monte Carlo simulations that includes the mixer.

5.1.1 Without Mixer

At the design start of a DT filter one can reduce the complexity to a bare minimum to a signal source, the filter in question and its load. A good starting point is PSS + PAC and plot the zero harmonic to get the AC response. However, PAC in combination of multiple of signal sources, as one has with any M/M or $M/2M$ filter, will give false impedance. To get correct impedance it is easiest to switch over to PSS + PXF. If PAC is the only choice, then one must remove all but one of the signal sources. The reason for this is still unknown.

5.1.2 With Mixer

If a DT filter is simulated with a mixer, only PSS + PXF is recommended. PXF will show the correct AC response and all folding frequencies. PAC is still possible to work with but frustrating as you need to specify the input harmonic of which the output harmonic relates to, one do only see a small part of the whole picture.

A generic simulation with PSS + PXF was simulated with a beat frequency of 2 GHz , same as the mixers LO frequency, seen in figure 5.1. One can easily see the wanted response, seen as harmonic 1, and the unwanted 3rd and 5th harmonics as 3 and 5. PXF was specified with a frequency range from zero to 2 GHz and are normally a waste of computation time as the region of interest are usually within 50 MHz . Figure 5.2 shows a similar setup with a lower beat frequency of 500 MHz and a shorter frequency range. The dotted line represents the peak values of all harmonics and will be the way of representing the folding effects in forth coming figures, which will be called the harmonic noise floor.

As an example, if the harmonic noise floor is constant at $-120dBc$ over the whole spectrum the receiver won't suffer from any folding issues, only the 1st, 3rd and 5th harmonics will be down converted to the given IF. If one sees a spike of $-60dBc$, let's say at 7 GHz , the receiver will fold content at 7 GHz to the given IF, thus making the receiver vulnerable to OBB. You might ask yourself, OBB? but that's only valid for higher frequencies than our IF within the BB side. Remember that the LNA and mixer are included, what one see is the complete transfer response from RF to IF.

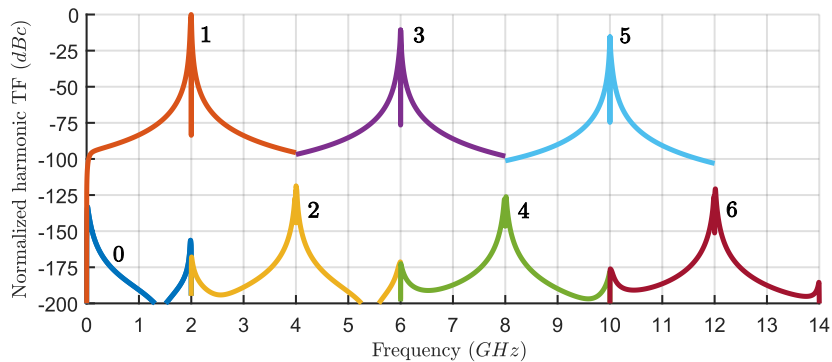


Figure 5.1: Typical response of a PSS + PXF simulation with six harmonics at a beat frequency of 2 GHz and a wide frequency range.

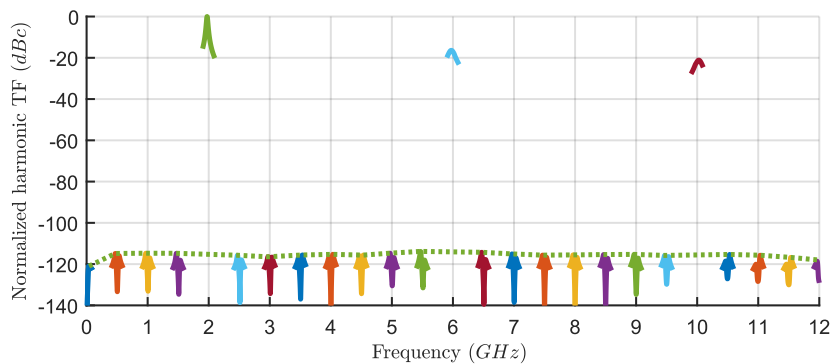


Figure 5.2: Typical response of a PSS + PXF simulation with 24 harmonics at a beat frequency of 0.5 GHz and a narrow frequency range, the harmonic noise floor is depicted as the dotted line.

5.1.3 Tolerance

The tolerance of a simulation will also impact the results. As an example, a PSS + PXF simulation will show the AC response from the output to the input for all harmonics that the user requests. If the whole spectrum is plotted, as in figure 5.1, a lot of harmonics will be shown, however many of these responses are not real and come from numerical errors, which are in turn created by loose tolerance and rounding errors from its floating-point representation. The unreal responses in figure 5.1 are marked as 0, 2, and 6. Validation of real and unreal responses are done by tightening the tolerance, with lower tolerance the unreal responses will decrease in amplitude while correct responses will stay constant. A rule of

thumb for any response that are more than 100 dB lower compared to your signal of interest are unreal.

Another example is given in figure 5.3 of a generic filter and its harmonic noise floor with different tolerance levers, where a higher number means tighter tolerances. a) shows the results without mismatches and one can clearly see that with higher tolerance the lower the harmonic noise floor will be, which means that the noise floor is completely made out of numerical errors and are therefore false. b) are identical to a) beside a minor mismatch within the filter, no matter what setting the harmonic noise floor stays the same. This small mismatch overshadows all numerical errors even at its looses setting, and because of this the response are undoubtedly real.

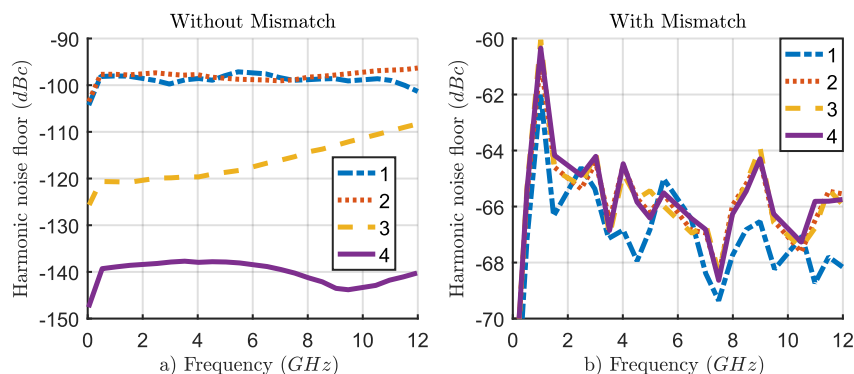


Figure 5.3: A generic simulation of a filter harmonic noise floor with different tolerances, 1 are loose while 4 are tight, a) are without mismatches while b) are with mismatch.

5.2 Resource Overview

Depending on which configuration of DT-BPF one uses, different amount of resources are needed in terms of transconductors, switches and capacitors. Table 5.1 shows an overview of the required resources of a fully pipelined 4/4, 4/8, 8/8 and 8/16, all capacitors are counted as single-ended. C_H can be configured as an differential capacitor as it will reduce the instance count and double the capacitance, both with a factor of two.

An increment in transconductors and switches are equivalent to a higher power consumption and area while capacitors only affect the area. Furthermore, the 4/4 uses fewest switches and capacitors while both the 4/8 and 8/8 uses the same amount, although the 8/8 uses more transconductors. The 8/16 is the most resource intensive, especially the amount of switches. Nevertheless, with figure 2.18 in mind, what one pay in resources one will presumably gain a filter with better performance.

Table 5.1: Resource overview of one stage with different configurations of a fully pipelined M/M and $M/2M$ DT-BPF.

DT-BPF	Transconductors	Switches	C_H	C_R
4/4	4	16	4	4
4/8	4	64	8	8
8/8	8	64	8	8
8/16	8	256	16	16

5.3 Switch Topology

Two different types of CMOS switches are considered, the single transistor switch and the transmission gate. Key characteristics are low on-resistance and simplicity.

5.3.1 Single Transistor

The Single Transistor Switch (STS) is as its name suggest a single transistor of either NMOS or PMOS type, its implementation is seen in figure 5.4 a). Normally the choice falls upon the NMOS due to its higher electron mobility, which will reduce the overall size of the transistor given the same on-resistance.

The NMOS transistor is ON when $\phi_x = V_{dd}$ and OFF when $\phi_x = 0$, although it is dependent on the CM voltage due to the fact that this is also its source and drain voltage, which will in turn reduce V_{gs} and therefore lower the on-resistance. Given a high enough CM voltage it will completely turn off the transistor and thereby no longer work as expected. If one always has a CM voltage close to V_{dd} it is better to use the PMOS transistor. Although, the same problem will occur if the CM voltage is then decreased.

A solution to remove the CM dependence is to DC-shift the gate signal from $[0, V_{dd}]$ to $[V_{CM}, V_{CM} + V_{dd}]$, effectively removing the CM difference between gate and source. A simple and effective implementation of this is achieved with the help of simple RC circuit, depicted in figure 5.4 b).

However, there are three side effects. First, the inverter that drives the switch will see a *higher* load which will in turn decrease the rise and fall times, if one do not increase the driving strength as well. By increasing the size more power will be consumed. Second, the introduction of a resistance at the gate will increase the noise, fortunately the impact of this is minimal. Third, the area will increase by $\sim 100X$ (given $M_2 = 10/0.04 \mu m$, $C_{DC} = 250 fF$, $R_{DC} = 15 K\Omega$), 95% of this area rise comes from, in comparison to the tiny transistor, the huge capacitor of $\sim 8 \times 8 \mu m$ (MOM capacitor). Although, these values should be seen as fixed, the real values of R_{DC} and C_{DC} depends on switch size and clock frequency. The area usage is also compounded as there are many switches in a single DT filter (table

5.1), although this is a bit of a lie as it is possible to only have one DC-shifter for each phase that in turn drives multiple of switches.

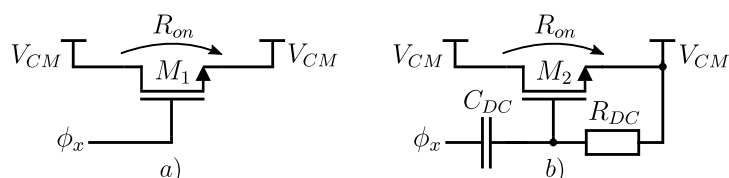


Figure 5.4: Implementation of the single transistor switch, without DC-shift in a) and with in b).

5.3.2 Transmission Gate

A Transmission Gate (TG) consists of two complementary transistors, NMOS and PMOS, that are connected in parallel as depicted in figure 5.5. As the two transistors are opposite to each other the inverse of ϕ_x , $\bar{\phi}_x$, must also be created to drive the switch.

The TG works similar to the STS as with $\phi_x = V_{dd}$ and a CM voltage of zero the NMOS will be ON while the PMOS is OFF. By increasing the CM voltage towards V_{dd} the NMOS will start to turn OFF while the PMOS starts to turn ON. If this continues to a CM voltage of V_{dd} the opposite will occur, the PMOS will be ON while the NMOS is OFF. The lowest on-resistance will occur with a CM voltage close to either zero or V_{dd} while the highest occurs with a CM voltage of $V_{dd}/2$, assuming that both transistors are scaled accordingly.

In term of on-resistances over a wide CM span the TG outperforms the STS as it will always work no matter what CM voltage is applied. However, the PMOS size needs to be scaled by a factor of ~ 3 , increasing the overall size in comparison to the STS. For a DT filter this means a higher power consumption due to the additional capacitive load on its clock drivers.

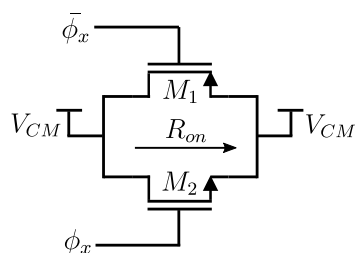


Figure 5.5: Implementations of the transmission gate.

5.4 Sideband Selection

Selection between upper or lower sideband is determined by the relative order of the mixer clocks in comparison to the DT-BPF. If the clock phases of the mixer run in the same order as a DT-BPF, as in direction between phases, then the center frequency of the BPF will be on the lower sideband while inverting the order of either the mixer or the DT-BPF clocks the center frequency will be on the upper sideband. For example, if a mixer has 8 clock phases, ϕ_1 to ϕ_8 , where ϕ_1 is the first phase and ϕ_8 is the last phase. If the clocks to the DT-BPF are running in the same order as the mixer phases the center frequency will be at the lower sideband while inverting the clock phases of the BPF (starting at ϕ_8 and ending at ϕ_1) results in a center frequency at the upper sideband, as seen in the dotted respectively the red line in figure 5.6

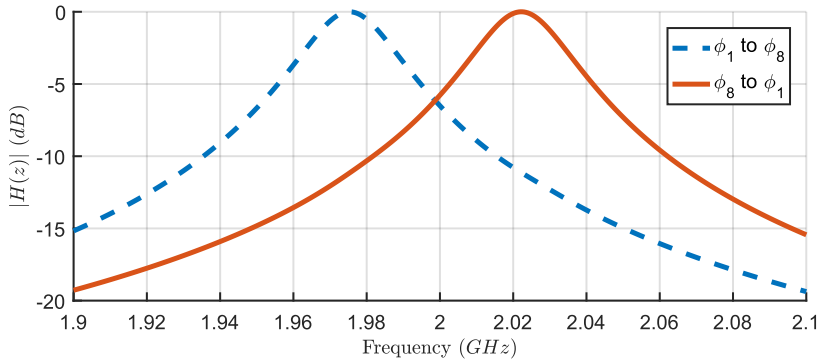


Figure 5.6: Sideband selection from a PSS + PXF simulation. The dotted line represents the response when both mixer and DT-BPF clocks are running in the same order while the other line has its clocks order inverted, either the mixer or filter but not both.

5.5 Relation Between IF, Capacitor Ratios and Sample Rate

By locking the IF and thereby the center frequency of a filter to a fixed frequency, only one variable is left to tweak, the relative scaling of C_H and C_R (eq. 2.48, 2.49). The sampling frequency can of course be seen as another variable but in practise it will be as low as possible due to its linear link to power consumption, but not low enough to cause folding issues.

Best performance is achieved when the capacitive difference between C_H and C_R are large (section 2.6.4). A large C_H and small C_R is the best combination as larger C_H contributes to a overall lower noise and better sinc filter performance while a small C_R increases the equivalent resistance and thus increasing the voltage gain (eq. 2.10). However, this case is not always possible to accomplish given a fixed

IF. Figure 5.7 depicts the relationship of a 8/8 DT-BPF between C_H and C_R with different sample rates of 0.5, 1, 2, 4, and 8 GHz, a) is with a IF of 1 MHz while b) is 10 MHz.

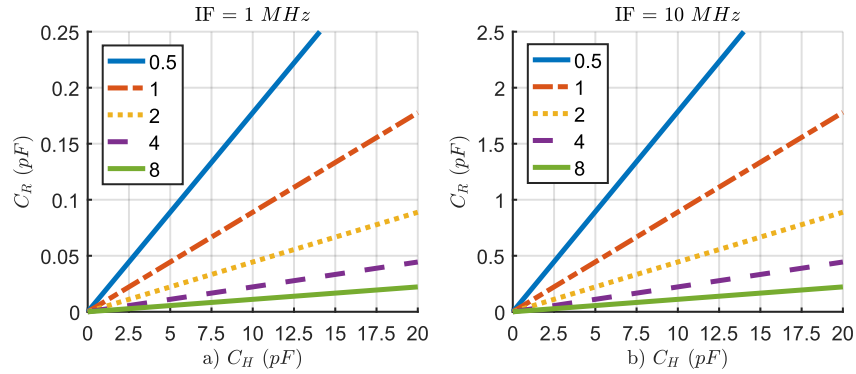


Figure 5.7: Relationship of a 8/8 DT-BPF between C_H and C_R with different sampling rates from 0.5 to 8 GHz, a) is with a IF of 1 MHz while b) is 10 MHz. Note that the scale of the two y-axes are not the same.

The prior figure shows that with an IF of 1 MHz a high ratio of C_H/C_R and low sample rate is possible to attain, ~ 55 with $C_H = 10$ pF and $f_s = 0.5$ GHz, which should be considered high enough and will give a sharp filter. By increasing the IF to 10 MHz this ratio is decreased to ~ 5 , which is very low and will give a flat AC response. To increase the ratio back to 50 the sample rate must be increased to at least 4 GHz, and by doing this one has effectively increased the filters power consumption by a factor of 8.

5.6 Simulations

In all forthcoming simulations the corner setting was typical-typical at 25C, unless otherwise noted. The simulated DT filter in question was always a 8/8 and therefore its input is equal to its output, which is an important aspect on noise simulations. Input-referred noise is equal to output-referred noise.

5.6.1 Effects of common-mode Voltage

The consequence of a CM voltage, V_{CM} , was investigated by simulating the on-resistance of the two different switch topologies from figure 5.4 a) and 5.5. V_{CM} went from zero to V_{dd} with different transistor widths of 10, 20 and 30 μm , the length was kept constant at 40 nm and the PMOS within the TG was sized three times larger to compensate for its lower mobility.

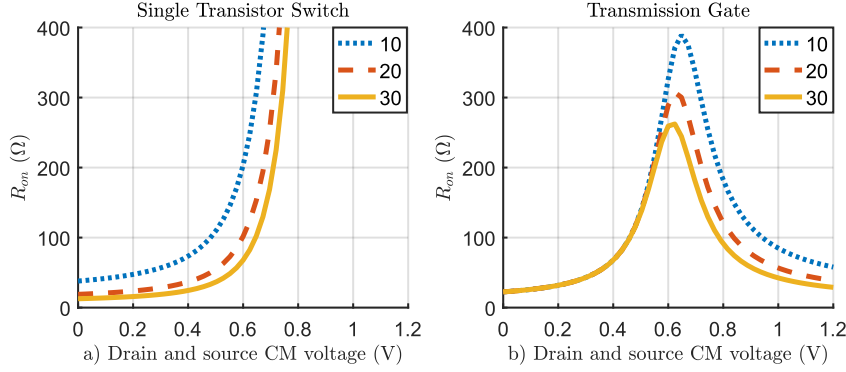


Figure 5.8: Simulation of the on-resistance with different transistor widths from 10 to 30 μm . a) shows the STS with an NMOS while b) shows the TG.

As seen in figure 5.8 both switch topologies perform as expected. The STS works well with a CM voltage of less than $\sim 0.4 V$ while the TG works over the whole span, beside the somewhat high on-resistance at $\sim V_{dd}/2$.

The same simulation was yet again performed with the STS but with the added DC-shift from figure 5.4 b). Values of $C_{DC} = 250 fF$ and $R_{DC} = 15 K\Omega$ were used, creating a HPF with $f_{-3dB} = \sim 42 MHz$. Noise simulation of an 8/8 DT-BPF was also added to see the outcome of R_{DC} , the width of M_2 was kept constant at 20 μm . No g_m -cells were used.

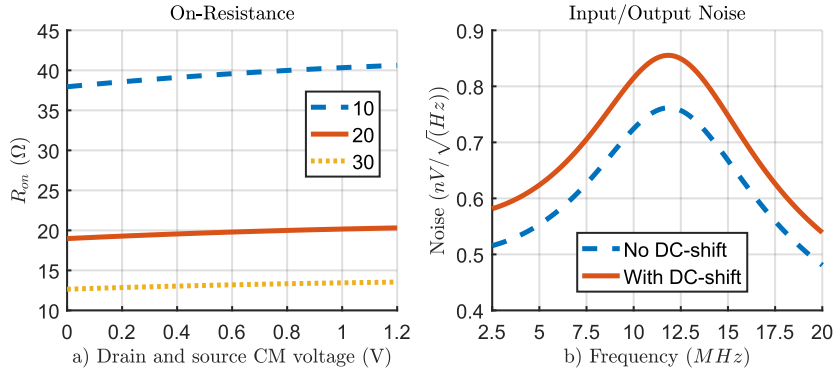


Figure 5.9: a) On-resistance with different transistor widths from 10 to 30 μm of the STS with DC-shift. b) Input/output noise of an 8/8 DT-BPF, due to the design of M/M the input and output-referred noise are equal.

The DC-shift completely solves the CM issue, an almost flat response of the on-resistance is seen in figure 5.9 a). Furthermore, the noise increases as expected,

figure 5.9 b), from its highest point of 0.76 to $0.85 \text{ nV}/\sqrt{\text{Hz}}$, a relative increment of 12%, although it is still negligible in comparison of a transconductors noise (figure 6.7).

The overall winner of these switches is entirely decided by the CM voltage, assuming area is of no concern. Given the typical case of a CM voltage of approximately $V_{dd}/2$ (created by a transconductor) the STS, with a capacitor to isolate the DC level at its source/drain, will deliver the best performance and lowest energy consumption. However, a drawback would be the size of the input capacitor, around 25 pF with the given IF and even larger with a lower frequency. If it is not feasible the STS with DC-shift is the second-best solution, although this implementation still uses more area than a standard STS or the TG. Although, the size of the DC-shift capacitor could probably be less, as long as it is ten times greater than the gate capacitance of the switch, the clock amplitude will be high enough. As a last point, the time constant of the RC filter is also important, with a lower clock frequency the time constant must be increased, otherwise the high state of the clocks will drift towards the CM voltage. A good starting point is a time constant ~ 10 of the clock period. Last comes the TG due to its high resistance at $V_{dd}/2$, it is arguable if an STS with a width of $\geq 30 \mu\text{m}$ is better, although over different corners the TG will be less sensitive.

5.6.2 Effects of On-Resistance

The effects of a non-ideal switch upon a DT filter was explored by simulating the differential impedance of an 8/8 DT-BPF. The switches were implemented as STS with sizes of 5, 10, 20, and $30 \mu\text{m}$, its length and CM voltage were kept constant at 40 nm and 0 V , respectively. The filter parameters were also kept constant with $C_H = 40 \text{ pF}$ (single-ended value), $C_R = 1 \text{ pF}$ and $f_s = 4 \text{ GHz}$. The expected single-ended real impedance is therefore 250Ω (eq. 2.8), hence the differential value will be doubled.

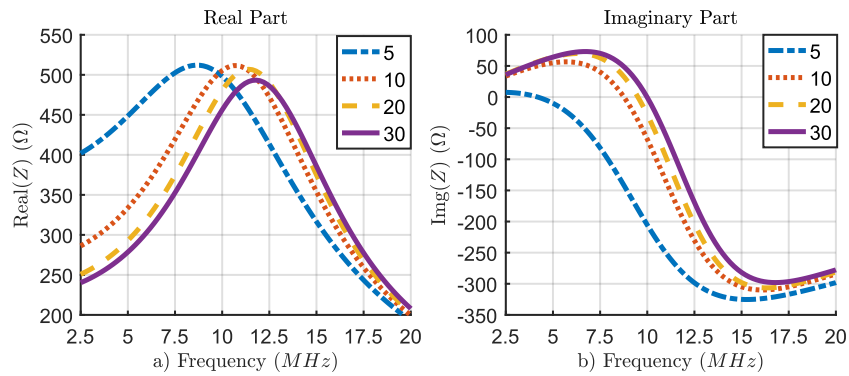


Figure 5.10: Differential impedance simulation of an 8/8 DT-BPF with different transistors widths of 5, 10, 20 and $30 \mu\text{m}$, a) shows the real while b) shows the imaginary part.

All widths in figure 5.10 attains the expected single-ended real impedance of 250Ω , although the center frequency moves quite a bit with wider transistors, this is presumably caused by more parasitic capacitance, effectively increasing C_R and thus increases center frequency. The imaginary part tells another story, with a width of $5 \mu m$ the DT filter barely gives any positive reactance. With $5 \mu m$ the on-resistance is about 80Ω , an all too high resistance in comparison of the filter impedance of 250Ω , in relative terms it is 32%.

The same setup was used to see how the noise and power consumption differs. The widths were 10, 20 and $30 \mu m$. $5 \mu m$ was left out due to its poor performance in the prior figure. During this simulation each switch had its own inverter chain as driver, starting with two inverters ($W_{NMOS} = 0.3, W_{PMOS} = 0.6 \mu m$) which is followed by a bigger inverter (3X) that drives a even bigger inverter (9X). All transistors within the inverters had their length set to $40 nm$, resulting in a rise and fall time of $\sim 15 ps$.

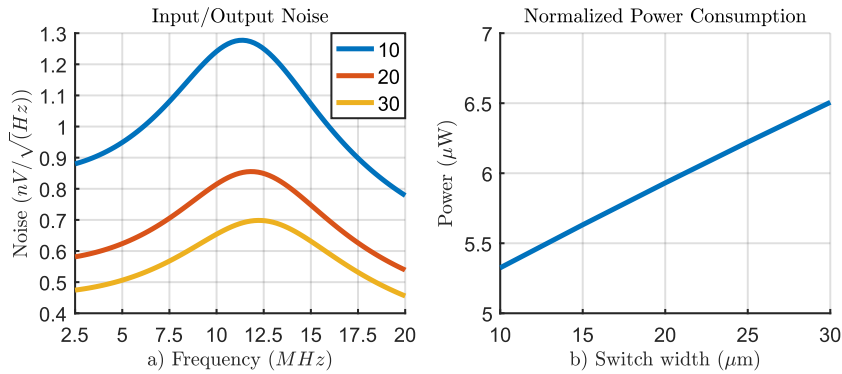


Figure 5.11: Simulation of an 8/8 DT-BPF with different transistor widths of 10, 20 and $30 \mu m$ on a single transistor switch, a) shows the input/output noise, due to the design of M/M the input and output-referred noise are equal. b) shows the normalized power consumption for one switch at $f_s = 1 GHz$.

The noise simulation in figure 5.11 a) gave 1.28, 0.86 and $0.7 nV/\sqrt{Hz}$ for 10, 20, and $30 \mu m$ respectively. Even though the relative increment is quite high, the noise from a transconductor will still be the dominate source (figure 6.7).

An interesting side note is that these noise values are very similar to the theoretical noise of an ideal resistor with corresponding on-resistance to the switches. A resistance of 40, 20 and 15Ω creates noise voltage of 0.82, 0.58 and $0.5 nV/\sqrt{Hz}$ respectively at room temperature. The power consumption in figure 5.11 b) was normalized for one STS at a sampling rate of $1 GHz$, for example with a full pipelined 8/8 DT-BPF at $4 GHz$ one should multiple by 256 ($4 \cdot 8 \cdot 8 = f_s \cdot (\text{pipeline stages}) \cdot (\text{switches in one stage})$).

Folding issues are first seen with the LNA and mixer connected. The harmonic noise floor is simulated with the different width of 10, 20, and 30 μm , all other parameters were kept unchanged from the previous simulation, beside a mismatch of 1° on one clock phase to the mixer, this was in turn done to rise the harmonic noise floor above the numerical noise floor.

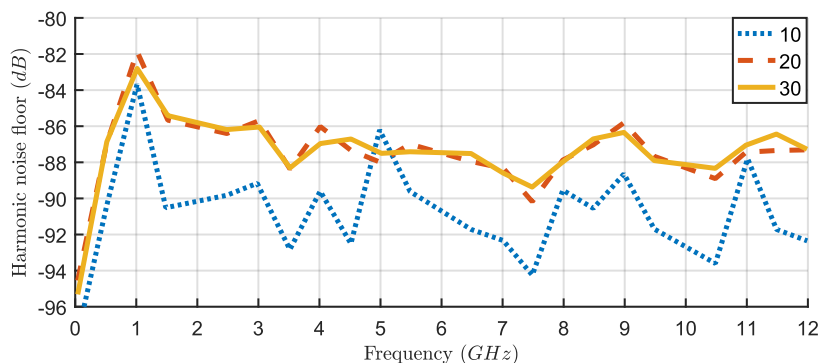


Figure 5.12: Simulation of the harmonic noise floor with different transistors widths of 10, 20 and 30 μm and the LNA, mixer and one 8/8 DT-BPF stage.

The results from figure 5.12 shows a minimal impact of folding with different transistor widths, at least the impact is lower than caused from the mismatch. Lowest folding is attained with 10 μm and are followed by 20 μm and 30 μm at ~ 3 dB higher folding. The better performance with 10 μm is presumably caused by either numerical errors in the simulation or by lowering the effective C_R which in turn gave a sharper filter response.

The somewhat obvious conclusion points to a switch size that is as low as possible, which saves energy and minimizes the influence on C_R from parasitic capacitance. The filter is not limited by noise or folding issues but rather the on-resistance in relationship to the real impedance of the filter, a general starting point is on-resistance of 1/10 compared to the real impedance of the filter.

5.6.3 Non-ideal Clock Sources

The effects of non-ideal clock sources were investigated by simulating the harmonic noise floor of the LNA, mixer and one 8/8 DT-BPF with different rise, fall times and phase errors. The rise and fall time were simulated with 5 to 30 in steps of 5 ps while the phase error had an error on its starting phase, ϕ_0° , with 0° , 0.2° , 0.6° and 1° .

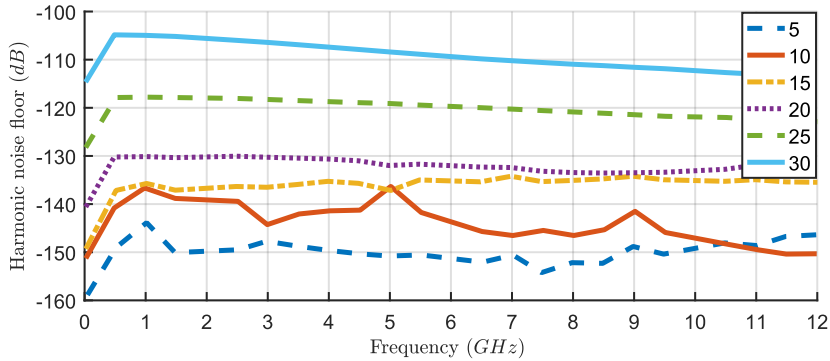


Figure 5.13: Simulation of the harmonics noise floor with different rise and fall times of its clocks, from 5 to 30 ps .

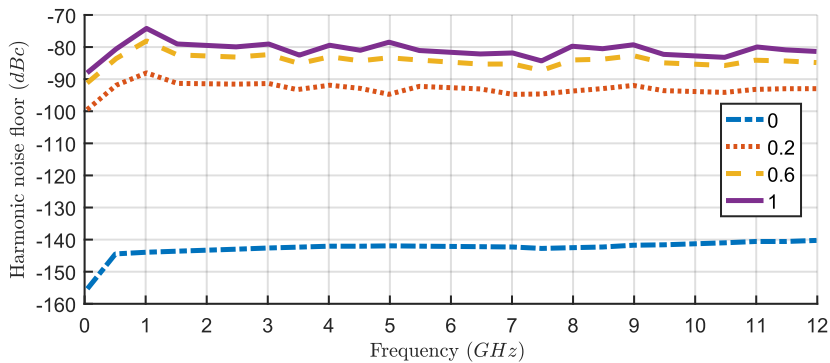


Figure 5.14: Simulation of the harmonics noise floor with different phase error on ϕ_0° , from 0° to 1° .

Figure 5.13 shows an almost flat response over the whole frequency spectrum and approximately linear increment of the harmonic noise floor with slower rise and fall times. Furthermore, figure 5.14 shows a similar flat response over the spectrum, though the folding appears with higher amplitudes when the phase error is non-zero.

The overall results shows a DT filter is highly dependent on its clocks. A close resemblance to that of a frequency mixer which are very sensitive to mismatches, slow rise/fall times on its clock phase. In any case, close attention on the filter clocks are important, one should strive for rise/fall time below 20 ps and phase errors of less than 0.2° on all clocks.

5.6.4 Folding versus Sample Rate

To investigate how the harmonic noise floor behaves with different sample rates and its impact on a wideband receiver, multiple simulation with the LNA, mixer, and three subsequent fully pipelined 8/8 DT-BPF with its transconductance amplifier. Meaning, after the mixer the next block in-line was an 8/8 filter, followed its g_m -cells, which were repeated another two times. C_H was kept constant at 40 pF (single-ended value) while C_R was scaled accordingly to attain a IF of 10 MHz.

As a starting point the effective sample rate was $f_s = 16$ GHz for all stages, or in other words, the decimation of all stages was [1, 1, 1]. As an example, with [1, 2, 4] the first stage will run at $f_s = 16$ GHz while the second and third stage are running with 8 and 4 GHz, respectively. Decimation is obtained by running the forthcoming stage with a lower sampling frequency, this will in turn increase the integration time on C_H such that the first notch from the sinc filter will always hit the first repetition of the DT filter (section 2.3). No mismatch was included on any clocks or signal phases. The highest folding point is given in table 5.2, the complete spectrum is in turn seen in figure 5.15.

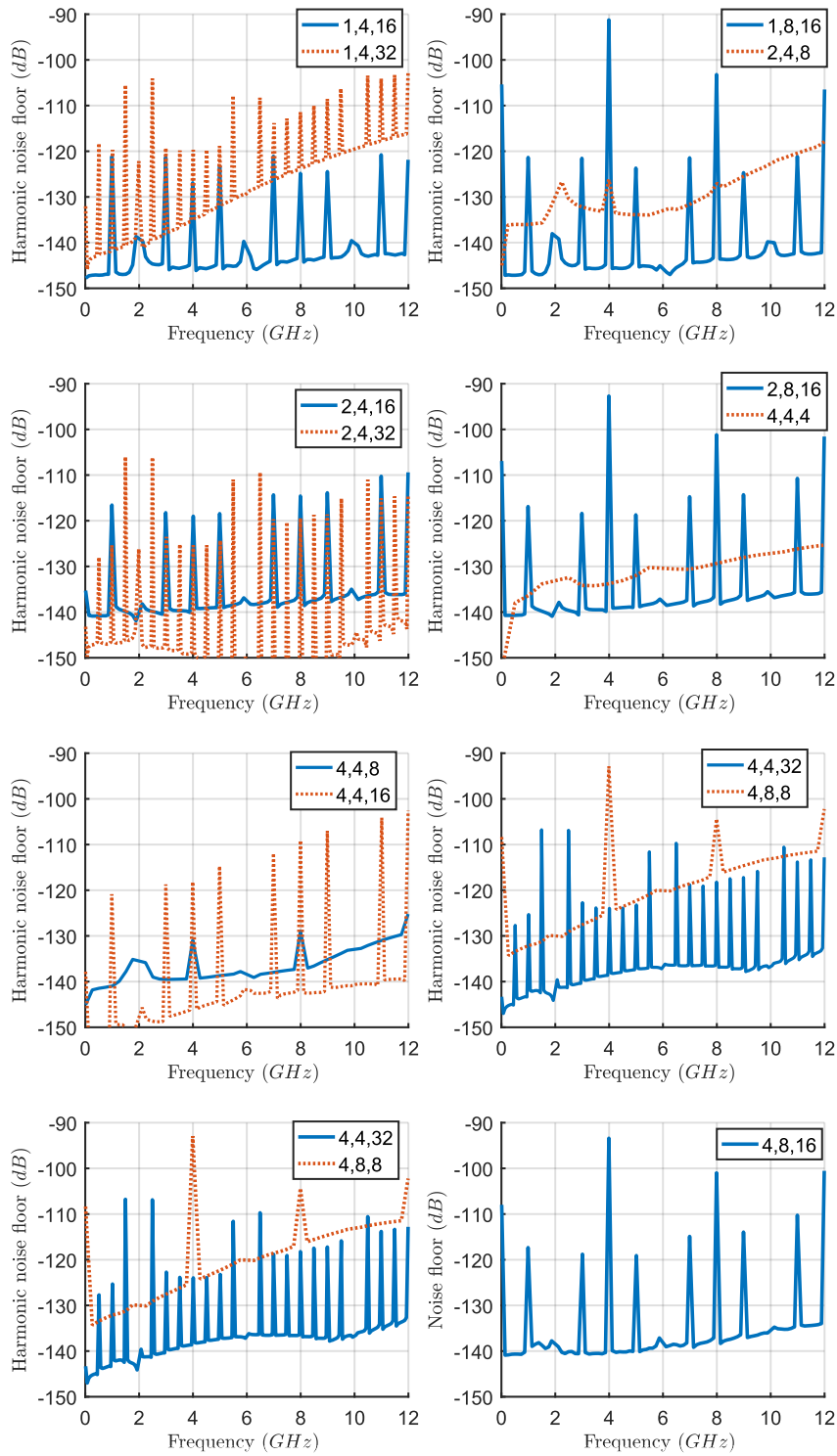


Figure 5.15: Harmonic noise floor spectrum with 15 different samples rates of three subsequent $8/8$ DT-BPF with its transconductor.

Table 5.2: Overview of the harmonic noise floor and the relative power consumption with different samples rates of three subsequent 8/8 DT-BPF with its transconductor, ordered by least folding.

Stage decimation	Peak folding (<i>dBc</i>)	Relative power con.
4, 4, 4	-125.3	0.75
4, 4, 8	-125.2	0.625
1, 4, 16	-120.8	1.3125
2, 4, 8	-119.0	0.875
2, 4, 16	-109.4	0.8125
4, 8, 8	-106.9	0.5
2, 4, 32	-106.0	0.78125
4, 4, 16	-104.1	0.5625
1, 4, 32	-102.5	1.28125
4, 8, 16	-93.4	0.4375
4, 4, 32	-92.9	0.53125
2, 8, 16	-92.7	0.6875
1, 8, 16	-91.2	1.1875

The overall impression from table 5.2 shows that a low sample rate will not work, there is simply too much folding with higher decimation. As this simulation was with perfect phases one can be assured that the real response is much worse. Beside the second-best results with [4, 4, 8] the lowest folding is attained with stages that do not decimate further than 4, hence it will be hard, if not impossible, to achieve a low power solution as three 8/8 DT-BPF stages will consume ~ 4.5 *mW* (excluding g_m stages, figure 5.11), yet more stages are needed to attain enough filtering.

Although, given that one has achieved the required attenuation decimation will save energy, the [4, 4, 8] gives equal performance as the [4, 4, 4] but with 16 percent lower power consumption (0.625/0.75). A relative easy solution to lower the sample rate is to introduce an analog anti-aliasing before any DT filter, however, one could argue that it goes against the concept of a DT receiver, at least in principle.

5.6.5 Scaling of C_H and C_R

Ignoring the sample rate for a while, the relative difference between C_H and C_R sets the center frequency of both the M/M and $M/2M$ DT-BPF (eq. 2.48, 2.49) while the absolute values impact the voltage gain (eq. 2.10) were lower values equal higher gain.

By means of this there is an initiative to lower these capacitors as much as possible. To see the outcome of reduced capacitance the previous simulation with a switch width of $20 \mu\text{m}$ from section 5.6.2 was performed with different absolute values, in each run both C_H and C_R were divided by x where x was 1, 2 and 4 which results in a capacitance of 40, 20 and 10 pF for C_H and 1, 0.5 and 0.25 pF for C_R (all single-ended values). With these settings the theoretical differential real impedance is 500, 1000 and 2000 Ω respectively.

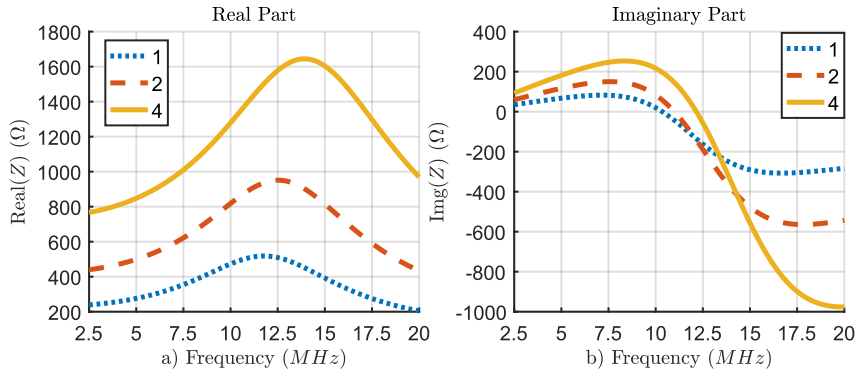


Figure 5.16: Simulation of an 8/8 DT-BPF with different capacitor values, $C_x/1$, $C_x/2$ and $C_x/4$, a) shows the real part while b) the imaginary part.

The highest real impedance, as seen in figure 5.16 a), were 518, 951 and 1644 Ω which relates to a relative deviation of 3.6, -4.9 and -17.8 % from its theoretical value. The difference grows with smaller capacitance and is primarily caused by the change of effective capacitance of C_R due to its already smaller value compared to C_H . The result with 1644 Ω ($x = 4$) is theoretical attained by increasing C_R from 250 to 300 fF . This highlight that with reduced capacitance the filter center frequency is more sensitive to the parasitic capacitance from the switches, therefor making it more receptive to process variations.

Continuing with the same simulation setup and parameters, noise and folding effects with smaller capacitance were also simulated. Nevertheless, the LNA and mixer were also included to see the folding effects.

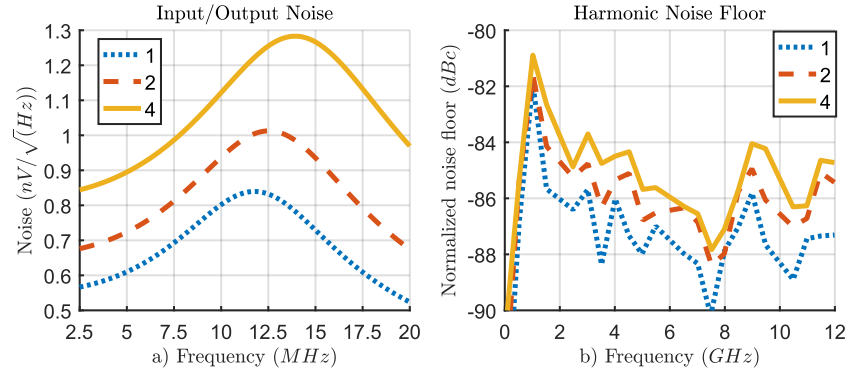


Figure 5.17: Simulation with different capacitor values, $C_x/1$, $C_x/2$ and $C_x/4$. a) shows the input/output noise of an 8/8 DT-BPF, due to the design of M/M the input and output-referred noise are equal. b) shows the harmonics noise floor of the LNA, mixer and one 8/8 DT-BPF stage.

Less capacitance increases the highest noise from 0.84, 1.01 to 1.28 nV/\sqrt{Hz} with $x = 1, 2$ and 4 respectively, seen in figure 5.17 a). This is primarily caused by lower capacitance of C_H (scales with $1/\sqrt{C}$), fortunately it is still lower in comparison to the noise from a transconductor. The harmonic noise floor caused by folding is more or less constant with lower capacitance.

The summary from these simulations concludes that smaller capacitance does in fact work without major issues, one could argue that one should strive to reduce C_H/C_R as much as possible as it will increase the voltage gain and thus increase the SNR, given a constant g_m . The only drawback is C_R sensitivity to parasitic's, where a lower value increases its ratio towards parasitic capacitance and thereby moves the filter center frequency, although this can easily be fixed with a programmable capacitance.

Transconductance Amplifiers

In this chapter four different topologies of a transconductor are investigated. Aspects that are looked upon are g_m efficiency, linearity, required area, simplicity, differential and common-mode voltage gain, noise and impact of process variations.

6.1 Topologies

Four different transconductance amplifiers were considered, the pseudo differential inverter, fully differential inverter, feedback inverter and the common source amplifier. Their names should not be seen as universal but rather simple made-up names for the sake of simplicity. Key characteristics are high g_m/I_d efficiency, low noise and simplicity.

In all forthcoming sections a resource overview are given, although it should not be seen as fixed but rather a rough estimate for the sake of comparison. Increasing W and L by the same amount, the active transistors will increase its output impedance and a minor increment in g_m , but at the same time it will reduce the voltage gain due to the capacitive voltage divider between the input capacitor and the intrinsic gate capacitance, which forces one to increase the input capacitor even more to keep the same gain. Meaning, if two topologies differ with a few dB it does not mean that one is better than the other. Given some extra time it is probably possible to optimize the design such that they are equal.

6.1.1 Pseudo Differential Inverter

The Pseudo Differential inverter (PD) was chosen as the transconductor in several DT receivers and filters [6–8, 18]. It consists of two standard inverters, one for each of the complementary single-ended signals. The gates of one inverter are separated and not connected together as one normally do, each gate has its own bias resistor together with a capacitor to block other DC paths. By doing this it is possible to control the bias current and the output CM voltage independent of each other.

Which transistors that are used for what is left to the designer. In our case the NMOS will set the bias current with a voltage source while the PMOS sets the output common-mode with the help of a simple error amplifier, also known as the common-mode amplifier.

The input capacitor together with its resistor creates a HPF with a cut-off frequency of $1/(2\pi C_{in}R_{in})$ which limits the use of an all too low IF due to the need of large capacitors, one could of course increase the resistance instead, but this will increase the noise. Both resistors and capacitors must have the same value to not give different cut-off frequencies for the two transistors. Assuming $C_{in} \gg C_{gate}$ the input impedance is set by R_{in} and C_{in} and is expressed by $Z_{in} = 1/(2\pi C_{in}R_{in}f_{IF})$. The PD is also highly linear and can almost handle an output swing of its supply voltage.

As this implementation is pseudo differential both differential and common-mode signals will be amplified. Common-mode rejection was achieved in [8] with an active common-mode shunt that decreases its impedance for CM signals. However, this was not considered because of time constraints.

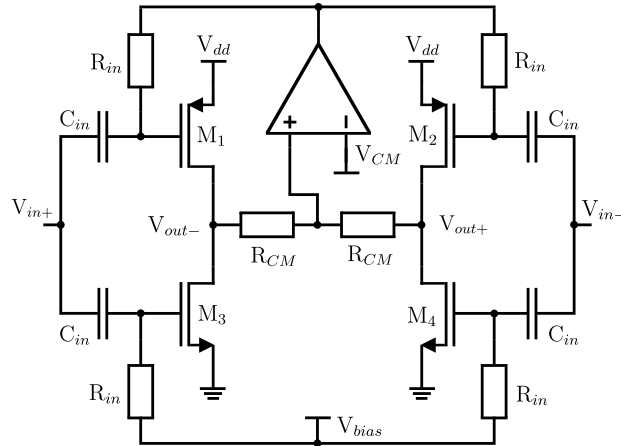


Figure 6.1: Schematic of the pseudo differential inverter.

Sizing and Area

Table 6.1: Approximate resource overview of the PD transconductor.

PMOS (g_m)	60/0.3 μm
NMOS (g_m)	40/0.3 μm
Capacitance	20 pF
Resistance	200 k Ω
Approximate area	5561 μm^2

6.1.2 Fully Differential Inverter

The Fully Differential inverter (FD) is almost an exact copy of the pseudo differential beside that the sources of the two NMOS are connected together to combine their bias currents with a common current source, also known as a tail current. To call this version fully differential is a bit of a lie as the PMOS will not act as a load but rather as another g_m source independent on the NMOS and thereby making it possible to amplify CM signals.

The positive about this version is that the gates can now be connected together, removing two capacitors with its resistors to save area. The cut-off frequency of the HPF remains constant and is set by $1/(2\pi C_{in}R_{in})$, same goes for its input impedance of $Z_{in} = 1/(2\pi C_{in}R_{in}f_{IF})$. Further side effects are the reduction in linearity due to the channel length modulation in the common current source and the reduction of output swing.

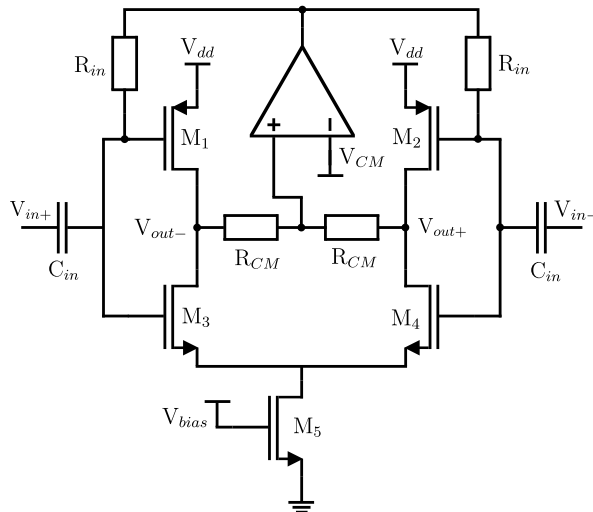


Figure 6.2: Schematic of the fully differential inverter.

Sizing and Area

Table 6.2: Approximate resource overview of the FD transconductor.

PMOS (g_m)	60/0.3 μm
NMOS (g_m)	40/0.3 μm
NMOS (bias)	20/0.3 μm
Capacitance	10 pF
Resistance	170 k Ω
Approximate area	2887 μm^2

6.1.3 Feedback Inverter

A standard inverter with a resistive feedback or simply Feedback inverter (FB) for short. No extra circuitry is needed for bias or common-mode, everything is done by sizing. This simplifies the implementations but also removes several degrees of freedom as it is not possible to set the cut-off frequency of the input HPF independent of the LPF at the output with a given load. This is because the input impedance is dependent on the transconductance, and the output load as seen in eq. 6.1.

On the other hand, if one can set the output load at will, the two filters can be set independent of each other. This inverter required least area as only one resistor and capacitor are needed, also the size of the capacitor can be a lot smaller compared to the other implementations. The FB implementation also lacks any common-mode rejection, amplifying both differential and common-mode signals.

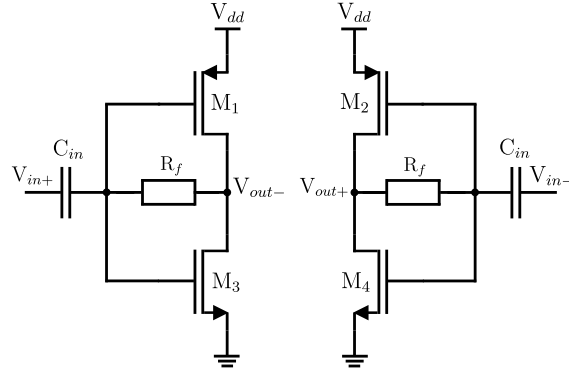


Figure 6.3: Schematic of the feedback inverter.

At low frequencies the input impedance in eq. 6.2 is dominated by C_{in} , as with all transconductors. By ignoring this capacitor for the moment, the impedance differs from other as within its bandwidth it will reduce the impedance due to the local negative feedback, acting more as a current sink. Together as a whole with a load capacitor and a correct setup the lowest impedance can be set at the IF.

The output impedance follows a similar trend, as seen in eq. 6.2, as within its local feedback bandwidth the impedance is low but slowly increases with frequency. Together with a load capacitor and correct parameters the highest point can also be set to the IF, which is better than other transconductors as it will attenuate other frequencies than its IF, but only to a minor degree.

$$Z_{in} = Z_{C_{in}} + \frac{R_f + r_o || R_L}{1 + g_m(r_o || R_L)} \quad (6.1)$$

$$Z_{out} = \frac{R_f + Z_{C_{in}}}{g_m(R_f + Z_{C_{in}}) + 1 - R_f g_m} \quad (6.2)$$

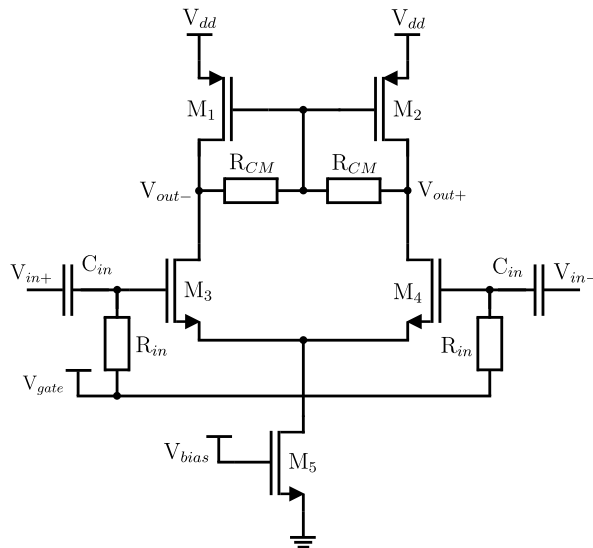
Sizing and Area

Table 6.3: Approximate resource overview of the FB transconductor.

PMOS (g_m)	25/0.15 μm
NMOS (g_m)	30/0.3 μm
Capacitance	1 pF
Resistance	180 k Ω
Approximate area	432 μm^2

6.1.4 Common Source Amplifier

The Common Source amplifier (CS) should not be considered as an inverter, although it is still a good choice for a transconductor. They are regularly found as the input stage of a common two-stage operational amplifier and offers a fully differential operation and attenuation of CM signals due to the PMOS load with its R_{CM} and the common current source. The PMOS do not contribute to any signal transconductance and therefore the CS will have less compared to all previous inverter based transconductors. Beside the absence of a CM amplifier and the new V_{gate} to bias the differential pair it is similar to the fully differential inverter as the bias current is set by the common current source and both the input impedance and HPF are set by $1/(2\pi C_{in} R_{in})$. Although one could use a CM amplifier to further attenuate CM signals and to guarantee a fixed CM at its output.

**Figure 6.4:** Schematic of the common source amplifier.

Sizing and Area

Table 6.4: Approximate resource overview of the CS transconductor.

PMOS (active load)	25/0.15 μm
NMOS (g_m)	30/0.3 μm
NMOS (bias)	12/0.3 μm
Capacitance	10 pF
Resistance	210 k Ω
Approximate area	2856 μm^2

6.1.5 Common-mode Amplifier

As depicted in figure 6.1 and 6.2 the pseudo and fully differential inverter use a CM amplifier to control its output CM. The CM amplifier works as a non-inverting summing amplifier, sensing the sum of a signal pairs output CM voltage and amplifies it.

Differential signals are not *seen* by the amplifier as one side will go up while the other goes down, effectively cancel each other out. The opposite happens with CM signals as both sides will add up. As an example, with a higher CM voltage than desired the sum will increase, raising the output voltage from the CM amplifier and will in turn raise the PMOS gate voltage, hence lower its V_{gs} and therefore the output voltage will go down as the NMOS has now a higher driving force in comparison to the PMOS.

The CM amplifier was implemented with a common source amplifier and an active load as depicted in figure 6.5, biased with a resistor or a transistors for the pseudo and fully differential inverter, respectively. In both cases the size of all transistors was scaled as 1/20 in comparison to its transconductor.

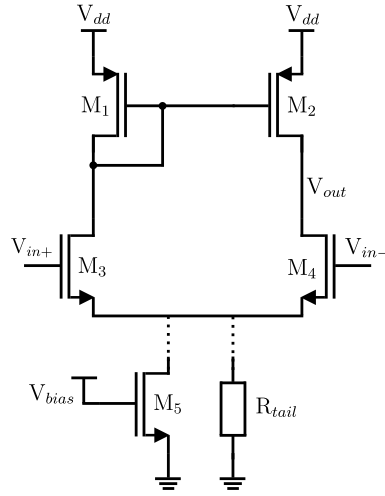


Figure 6.5: Schematic of the common-mode amplifier.

6.2 Simulations

To ease the distinction of the four transconductors in the following figure the pseudo differential inverter will be called PD, fully differential inverter as FD, feedback inverter as FB and the common source amplifier as CS. The simulation of transconductance, AC response, noise and linearity was performed with a bias current of $200 \mu A$ (for a signal pair), the load consisted of a $10 pF$ differential capacitor in parallel with a resistor of $1 K\Omega$. This load represents the loading of a 8/8 DT-BPF and the corner setting was typical-typical at $25C$, unless otherwise noted.

6.2.1 Transconductance

The transconductance was attained with a simple DC simulation and is given in table 6.5, the bias current was $100 \mu A$ for a single side or $200 \mu A$ differential.

Table 6.5: Transconductance and its efficiency at a bias current of $100 \mu A$ (single-ended).

Stage type	g_m (mS)	Efficiency (g_m/I_d)
PD	3.30	33
FD	3.26	32.6
FB	2.21	22.1
CS	1.55	15.5

The results were as expected, those who reuses its current through two active transistors gives approximately twice the g_m and therefore also twice the efficiency. The PD and FD gave the highest g_m and the CS the lowest while the FB is in between.

6.2.2 AC Response

The AC response of the four transconductors were performed of both differential and CM voltage gain. The end goal here is to see which transconductor attains high differential gain while at the same time attenuates common-mode signals. All transconductors had the same load of 10 pF , connected differentially, but their input HPF was adjusted such that the frequency response was centred at 10 MHz .

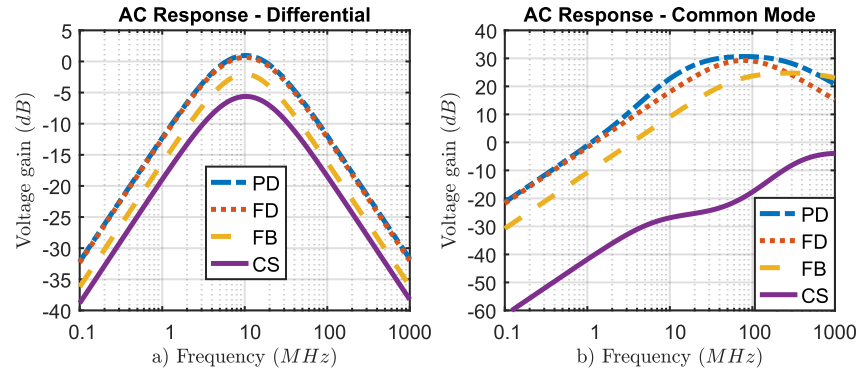


Figure 6.6: AC response of the four transconductors, a) shows differential gain while b) show the common-mode gain.

In figure 6.6 the PD and FD gave the highest voltage gain of 0.95 and 0.65 dB respectively. This is followed by the FB at -2 dB and the CS with -5.6 dB . The opposite occurred for CM signals, lowest gain was attained with the CS of -26.93 dB and was followed by the FB, FD and PD with 9.1, 18 and 22.75 dB respectively. All values of differential and common-mode were taken at a frequency of 10 MHz .

The high CM gain in comparison to differential comes from the lack of CMRR and that the load is only *seen* by differential signals, CM signals will only see the intrinsic output impedance which is a lot higher than the external load ($\sim 15K\Omega$).

There is no overall winner between the four transconductors as the stage that have the highest differential gain also has the highest CM gain. The CS is the only stage that has less CM gain than differential gain, all other have 20 to 30 dB of gain over a span more than 100 MHz . This point towards a conclusion that a differential load capacitor is not the best solution.

6.2.3 Noise

The same test bench for AC response was used to simulate the input-referred noise of the four transconductors, although a second lighter load was also added to see the noise level with a higher gain, the load in question was a parallel capacitor of 200 fF . The first load was kept unchanged at 10 pF .

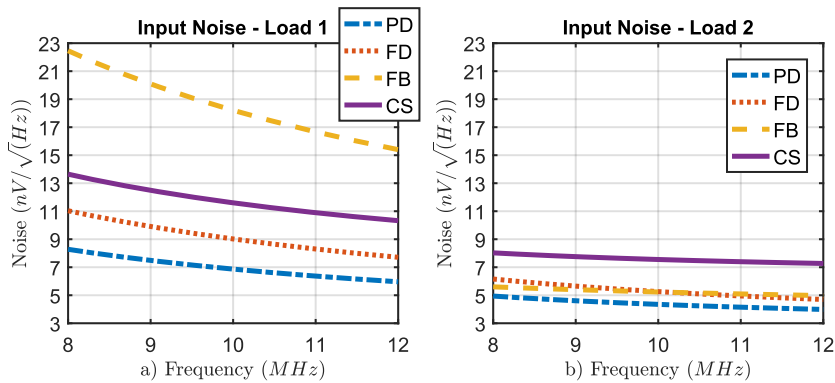


Figure 6.7: Input-referred noise of the four transconductors, a) shows the standard differential load of 10 pF while b) is with 0.2 pF .

The first load in figure 6.7 a) gave similar results from the AC response as lowest noise are attained with the PD, followed by the FD, CS and FB with 6.9 , 9.0 , 11.6 and $18.2\text{ nV}/\sqrt{\text{Hz}}$ respectively. With the second lighter load in figure 6.7 b) the noise decreases to 4.3 , 5.3 , 5.3 and $7.5\text{ nV}/\sqrt{\text{Hz}}$ for the PD, FD, FB and CS respectively. Their voltage gain with the lighter load were, as in the same order as above, 28.8 , 27.6 , 27 and 20.4 dB . All values in both figures were taken at a frequency of 10 MHz .

Lowest noise regardless of load is attained by the PD and is followed closely by the FD. The FB varies the most, depending on which load is used, from worst results with the first load to an almost identical noise level of the PD with the second load. It is arguable if CS has the worst performance as it has the second highest noise with the first load and the highest noise with the second load.

6.2.4 Linearity

Continuing with the same test bench as above, the linearity of the four transconductors were extracted by simulating the input-referred second and third-order intercept point (IIP2, IIP3) with a two-tone test.

IIP2

Without any mismatch the results would be too high, towards the infinite and certainly not realistic. Thereby a mismatch had to be included on one side of the differential signal, in which was attained by increasing the transistor size on one side by 5%.

The frequencies in the two-tone test were $f_1 = 6 \text{ MHz}$ and $f_2 = 14 \text{ MHz}$ and their second-order intermodulation product creates new frequencies at 8 MHz ($f_2 - f_1$) and 20 MHz ($f_1 + f_2$) MHz , 8 is closest to the given IF of 10 MHz and is therefore drawn as the second-order power with a slope of two in the forthcoming figures. For the first-order power with a slope of 1, both 6 MHz and 14 MHz can be used due to the symmetrical AC response around 10 MHz , although 6 MHz was used in the forthcoming figures.

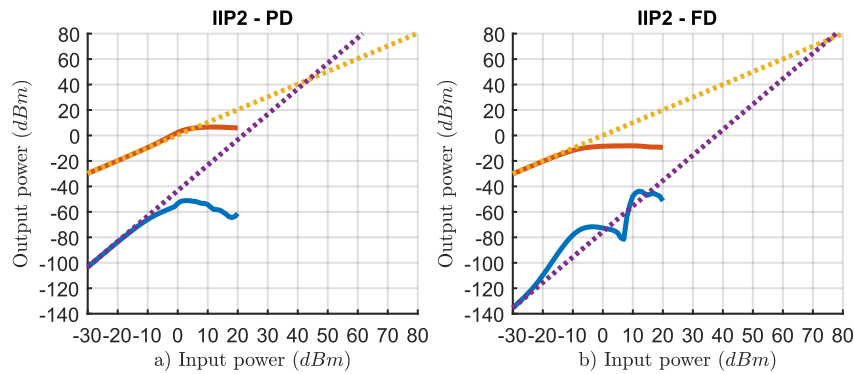


Figure 6.8: Input-referred IP2 of PD in a) and FD in b).

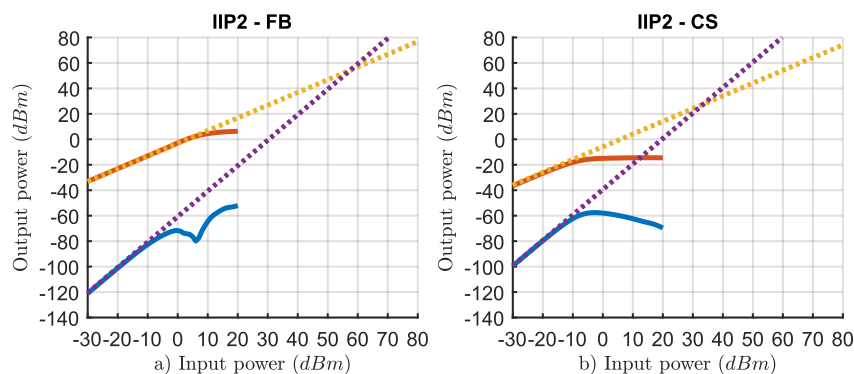


Figure 6.9: Input-referred IP2 of FB in a) and CS in b).

The highest IIP2 was achieved by the FD of 75 dBm and was followed with FB, PD and CS at 57, 44 and 33 dBm respectively, as seen in figure 6.8 and 6.9. Even though the IIP2 result shows a wide span between the four transconductors, a low IIP2 value do not directly mean that the topology is useless, as IIP2 primarily cause problems with an IF close to DC, especially for DCR as one of the second-order modulation products creates a strong product centred at DC and with a modulated interferer this term will span from DC and upwards [19]. The actual requirement is strongly link to what IF one uses.

IIP3

The frequencies for IIP3 in the two-tone test were changed to $f_1 = 10 MHz$ and $f_2 = 10.5 MHz$. The third-order intermodulation products are created at 9.5 MHz ($2f_1 - f_2$) and 11 MHz ($2f_2 - f_1$). Both frequencies are very close to the given IF of 10 MHz , although 10 and 10.5 MHz was drawn for the first-order with a slope of one and the third-order with a slop of three respectively in the forthcoming figures.

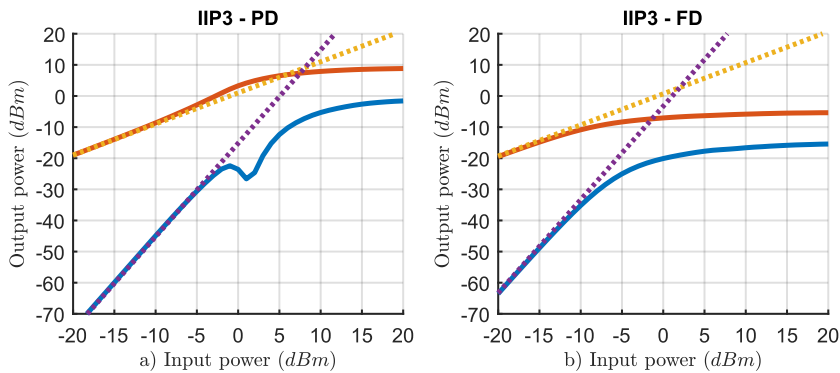


Figure 6.10: Input-referred IP3 of PD in a) and FD in b).

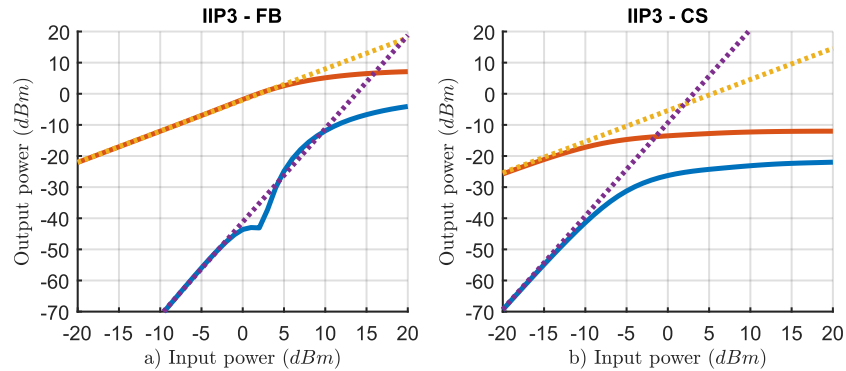


Figure 6.11: Input-referred IP3 of FB in a) and CS in b).

The result from figure 6.10 and 6.11 differs quite a lot in comparison to the IIP2 test as highest IIP3 is achieved with the FB of 19.5 dBm and are followed by the PD with 8 dBm, the FD and CS shares the same results of 2 dBm. With these results in mind the FD and CS suffers from lower linearity compared to PD and FB, especially in comparison to FB as it got an suspicious high IIP3, and because of this a dedicated Monte Carlo simulation of its IIP3 was performed to validate the validity, seen in figure 6.14. In any case, the high IIP3 is probably due to the current-sink characteristics of the FB, effectively reducing the voltage swing at its input.

6.2.5 Stability of Common-mode Amplifier

All systems with feedback suffer from the possibility of unwanted oscillations, this is normally caused by an all too low phase margin. To validate the stability of the system the phase margin at different bias currents were attained by simulating multiple of Bode plots.

This was of course only conducted with the PD and FD as the other do not use a CM amplifier. The point with this simulation is to validate that a CM amplifier can easily be implemented without any issues.

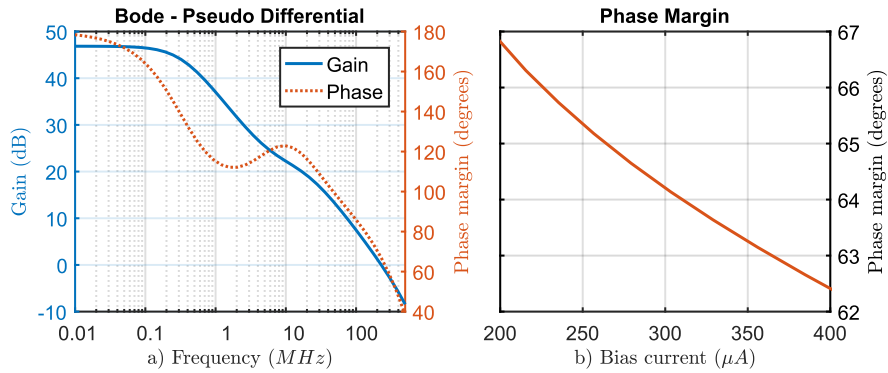


Figure 6.12: Simulation of the CM amplifier controlling the PD inverter, a) shows a Bode plot while b) shows the phase margin over bias current.

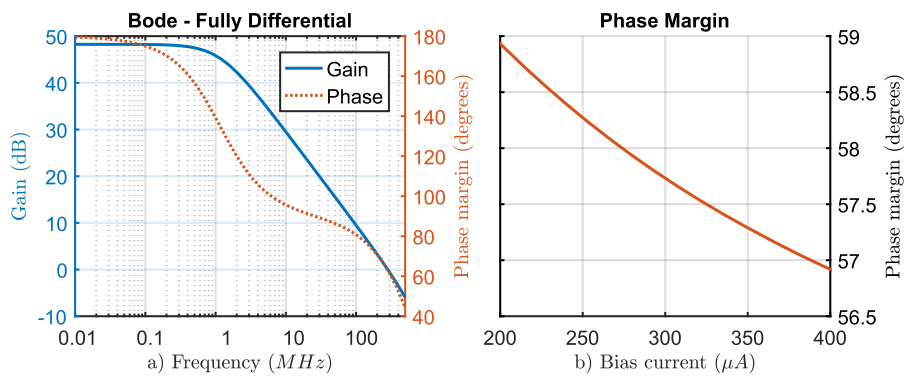


Figure 6.13: Simulation of the CM amplifier controlling the FD inverter, a) shows a Bode plot while b) shows the phase margin over bias current.

Both amplifiers achieve a high DC gain of 46.6 and 48 dB with a gain bandwidth product of 220 and 280 MHz for the PD and FD respectively. The phase margin was on the low side with an average of about 64° and 58° for the PD and FD respectively, although quite stable independent on bias current. By changing C_H as a single-ended load capacitor the bandwidth will be reduce and phase margin will go up as it will be a clear dominating pole (see section 6.2.2).

6.2.6 Process Variations

Resistance and Capacitance

A Monte Carlo simulation was performed of a Metal-Oxide-Metal (MOM) capacitor and a uncalicided poly resistor in three different sizes. These two components are found in all g_m stages as part of its input HPF. All resistors had a value of $10\text{ K}\Omega$ while the capacitors were set to 0.1, 0.5 and 5 pF .

Table 6.6: A Monte Carlo simulation of three resistors and capacitors in different sizes, 8278 runs were performed. Local mismatch represents a difference between two identical devices on the same ASIC while global mismatch are different dies.

	R_1	R_2	R_3	C_1	C_2	C_3
Size (μm)	0.2x2.9	1x15.77	5x82	5.4x5.4	11.5x11.5	35.4x35.4
σ_{local} (%)	1.71	0.32	1.26	0.16	0.05	0.04
σ_{global} (%)	6.37	5.05	4.85	4.80	4.85	4.88

Assuming orthogonality between the resistance and capacitance spread in both local and global mismatch in table 6.6 the worst case $3\text{-}\sigma$ cut-off frequency change of a HPF are then 1.08% and 28.95% respectively.

The results points towards an issue with global mismatch, careful consideration must be done to achieve low spread and possible some type of calibration scheme to level out any die-to-die changes, or a variable IF to use the same IF as the mismatches sets. The positive part is the local mismatch, points towards no sub-block to sub-block calibration.

Transconductors

The frequency response of all transconductors were centred around 10 MHz , just as in figure 6.6. Its gain will vary mainly with its g_m but also due to variation of its input HPF. If its cut-off frequency from the HPF moves up in frequency it will reduce the amplitude.

The absolute gain difference of all transconductors is not of interest as it will not degrade the performance of image and harmonic rejection. On the other hand, the gain difference between different transconductors in the same stage will degrade the performance, or just local mismatch for short. Therefore, two separated Monte Carlo simulations were performed of the gain mismatch between two identical stages. The first test, σ_1 , was with a symmetrical AC response while the other test, σ_2 , was performed with a 3x lower cut-off frequency of the HPF ($f_2 = f_1/3$), this was done to see the impact of this filter.

Table 6.7: Monte Carlo simulation of the four transconductors with only local mismatch to see the gain variations of two identical stages, 10000 runs were performed.

	PD	FD	FB	CS
σ_1 (dB)	0.147	0.182	0.106	0.217
σ_2 (dB)	0.146	0.180	0.114	0.215

All tests had a normal distribution and therefore only the standard deviation is given in table 6.7. Lowest deviation comes with the FB stage, this is followed by the PD, FD and CS stage, respectively. Furthermore, the impact of the HPF is minimal and can be assumed to have zero impact.

IP3

As mentioned in section 6.2.4 a dedicated Monte Carlo simulation was performed to validate its high IP3. The figure 6.14 shows two distributions where the one, which is also the biggest, are centred around the 19.5 dBm mark, the other one is even higher up at ~ 26 dBm. This points towards a correct simulation in figure 6.11, the FB has a fantastic good IP3.

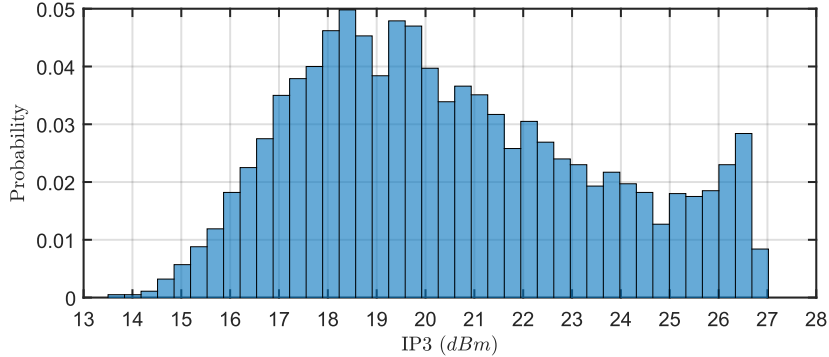


Figure 6.14: Distribution of a Monte Carlo simulation with IP3 of the FB stage, 10000 runs were performed.

Harmonic Rejection

7.1 Topologies

Two different implementations of a harmonic rejection circuit were investigated. The principle of these two are the same and works by cancellation of harmonic content, more about the theory are described in section 2.8. The first implementation is continuous-time based with transconductors and are quite common in receivers with harmonics rejection [8, 20], the second implementation follow the same idea but is realized in discrete-time, the different phases of the signal are sampled and stored on capacitors to later be combined. Both implementations will use eight phases.

7.1.1 Transconductor Based

Any implementations of a transconductor can be configured to achieve harmonics rejection, this is done by combining the transconductance of three signal phases, as seen in figure 7.1. The second transconductor is scaled to produce $\sqrt{2}$ times more transconductance compared to the first and third transconductor. This is then repeated for each of the eight signal phases. In total there is 8 unit-cells for one circuit.

The FB transconductor in section 6.1.3 was chosen for its performance in both linearity, noise and process spread (figure 6.7, 6.11 and table 6.7) but also for the lack of any common-mode circuit that complicates the implementation, multiple of error amplifiers that will try to control a common output is probably a bad idea. However, the main issue is the lack of control, both bias current and common-mode voltage are controlled with sizing. This leaves only the bulk voltage, V_{bulk} , for controllability. The bulk voltage of the NMOS can be directly controlled with V_{bulk} while the PMOS bulk voltage is controlled with $V_{dd} - V_{bulk}$. The effective result by increasing V_{bulk} is higher transconductance and lower output resistance, thus the phase vectors length can be controlled to compensate against process variations.

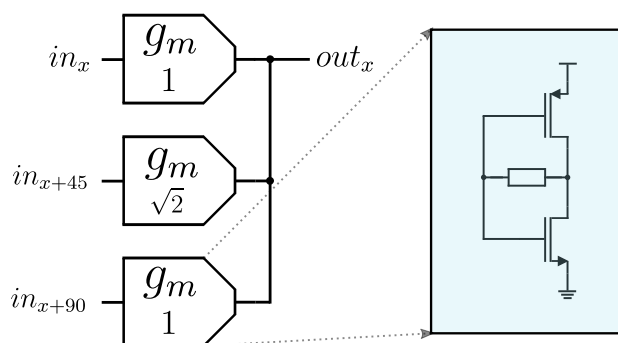


Figure 7.1: Implementations of a g_m -HR unit-cell.

7.1.2 Discrete-Time Based

Harmonics rejection can also be achieved with a discrete-time topology. This is achieved by reconfigure the second-order DT-LPF, as described in section 2.5. The concept is identical to the previous implementation with transconductors, although instead of continuous combining three phases to achieve cancellation each phase is now integrated continuous onto a C_H capacitor over its sampling time T_s to attain the wanted sinc filter, as seen in figure 7.2. Each signal phase is then sampled and stored onto their respective C_R capacitor to be later combined together with another C_H capacitor. The value of the second C_R capacitor is scaled by $\sqrt{2}$ compared to the first and third C_R . This will assure that the second C_R capacitor will transfer $\sqrt{2}$ more charge from its input to the common output capacitor of the three phases. In total there is 8 unit-cells for one circuit.

Beside the harmonic rejection this implementation also comes with a second-order LPF where their cut-off frequency is set by the values of C_{H1} , C_{H2} , C_R and its sample rate. As $C_{R\sqrt{2}}$ differs from C_{R1} the $x + 45^\circ$ path will have another cut-off frequency. The system poles and zeros can be described by eq. 2.20.

To compensate against process variations, it is best suited to implement the $C_{R\sqrt{2}}$ capacitors as a programmable capacitance bank, etc a 150 fF capacitor can be implemented as a fixed capacitor of 130 fF and 32 smaller capacitor of only a few fF .

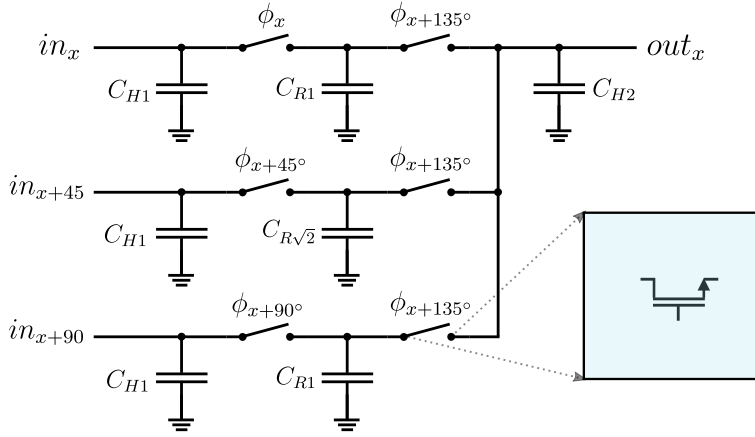


Figure 7.2: Implementations of the DT-HR unit-cell.

7.2 Simulations

Hereinafter in this section the transconductance stage will be called as g_m and the discrete-time stage as DT.

7.2.1 AC Response

As the g_m version was implemented with FB transconductors it will follow the same AC response as a single FB transconductor in figure 6.6, assuming minor adjustment and with the requirement that the load capacitor can independently be set. On the other hand, the DT version is quite different as its AC response follows as a LPF. The AC response were simulated with $C_{h1} = 1.2 \text{ pF}$, $C_{h2} = 500 \text{ fF}$, $C_1 = 100 \text{ fF}$, $C_{\sqrt{2}} = 150 \text{ fF}$ and a sample rate between 0.5 to 4 GHz. Furthermore, no mismatch was introduced, the switch size was set to $10 \text{ }\mu\text{m}$ and its inputs were ideal current sources.

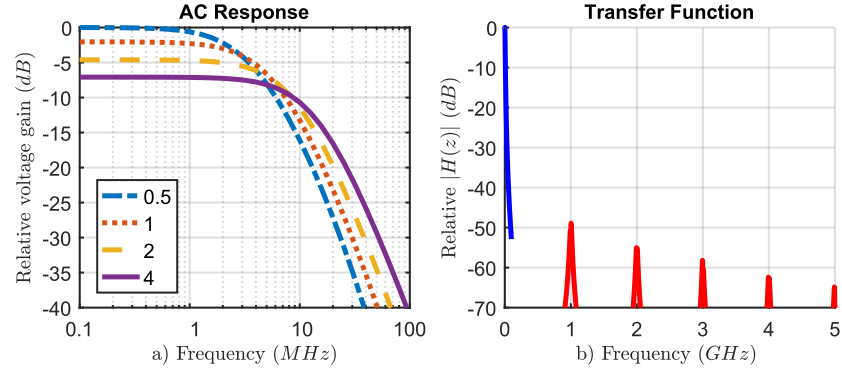


Figure 7.3: a) Relative AC response of the DT-HR with different sample rates, from 0.5 to 4 GHz. b) Relative transfer function of the DT-HR with a sample rate of 1 GHz

The results in figure 7.3 a) shows no surprises, it follows the expected behavior as described in section 2.5.3. In b) the transfer functions with five harmonics are shown, its first harmonics is also where the first folding appears which is suppressed by almost 50 dB, which is far from the theoretical attenuation of 92 dB (assuming f_{-3dB} at 5 MHz)

7.2.2 Harmonic Rejection

The LNA and mixer were included together with a phase error of 1° on one of the mixers clocks. Without any mismatch it is possible to achieve infinite rejection with multiple of stages, this is of course not realistic, and mismatches must therefore always be included to get realistic answers.

Both versions, g_m and DT, were simulated with their respective variable to configure for best performance, bulk voltage for g_m and $C_{R\sqrt{2}}$ for DT. Furthermore, the DT version clocks ran at a sample rate of 500 MHz but were not ideal, although the rise/fall time of its drivers was rather fast of 16 ps.

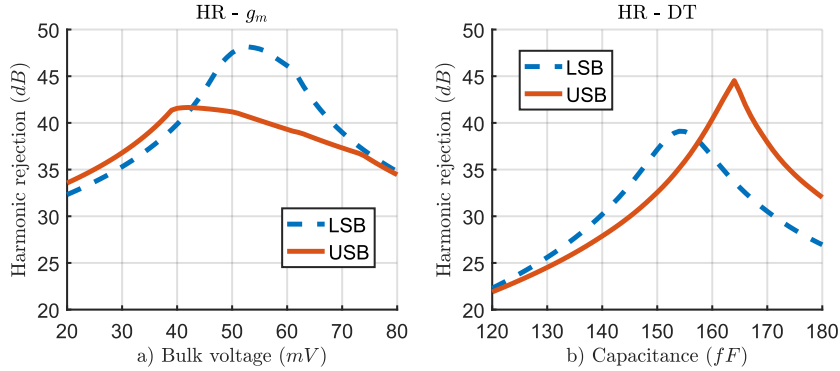


Figure 7.4: Rejection of both upper and lower sideband of the third harmonic, with g_m in a) and DT in b).

The combined results from both upper and lower sideband in figure 7.4 shows 41.7 dB suppression with the g_m stage while the DT only gave 36.5 dB. If one increases the sample rate to 1, 2 and 4 GHz its rejection are then 38, 38.6, 39.6 respectively.

Another simulation with the same test bench but only the DT version and without any mismatches were performed, all other parameters were the same as in section 7.2.1. The point here is to see the impact of driving strength of its clocks and the switch size. The strength was controlled by increasing the size of the buffer chain, a relative linear sweep from 5 to 25 with a fixed switch size of 10 μm . In the other test the switches were varied from 3 to 15 μm and with a fixed strength of 15. Both tests had different sampling rates from 0.5 to 4 GHz.

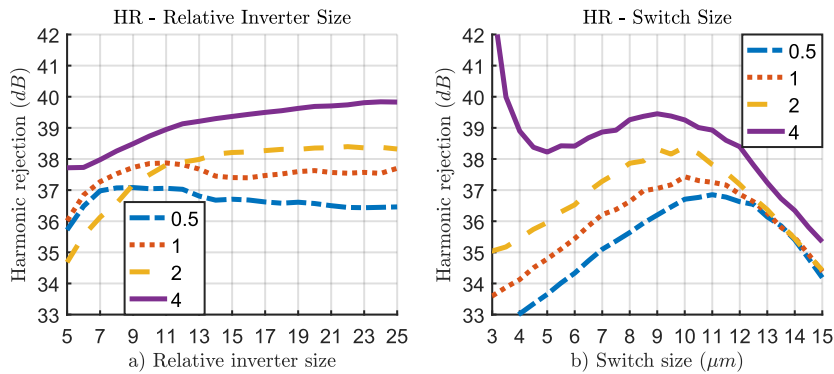


Figure 7.5: Harmonic rejection of only the upper sideband, a) shows the driving strength by increasing the inverters size while b) shows the size of all switches, both at different sampling rates from 0.5 to 4 GHz.

Starting with a) in figure 7.5, more or less the same performance with inverter size, although there is a minimum limit. Below 10 the performance start to suffer, surprisingly it does not seem to correlate with sampling rate as one could argue that a higher sample rate is more sensitive to slow rise/fall times. Nevertheless, the results are similar as seen in figure 5.13, there is a limit on how slow the rise/fall times can be.

In b) there is more spread, especially at 4 GHz , although this is the expected behavior as with a change of the switches transistor size the intrinsic capacitance also changes which in turn changes the ratio of $C_{R\sqrt{2}}/C_{R1}$. The overall conclusion is that the DT version is yet again sensitive to variations of switch size.

7.2.3 Process Variations

Harmonic Rejection

To see the spread of the two versions a Monte Carlo simulation was yet again performed, no mismatch was added. The g_m version had perfect voltage sources as its input while DT used ideal current sources together with perfect clock sources of 16 ps rise/fall, running at a sample rate of 1 GHz . The question to ask here is, how much spread is expected from the circuit itself.

Table 7.1: Harmonic rejection of the upper and lower sideband with a Monte Carlo simulation, 1724 runs with the g_m version while the DT ran with 1510 runs.

	$g_{m,LSB}$	$g_{m,USB}$	DT_{LSB}	DT_{USB}
σ (dB)	3.81	3.96	4.12	4.25
μ (dB)	42.66	43.35	36.30	38.21

The overall results from table 7.1 point against the DT version due to its higher spread, although the difference is ~ 1 dB with $3\text{-}\sigma$. by looking at the mean value of upper and lower sideband at -3σ the winner is g_m at 31.35 dB attenuation while the DT version only achieved 24.70 dB , mainly due to its already low mean value.

Discussion and a Receiver on Paper

Analog discrete-time filter comes with a lot of new functions and a new way of working, or at least from the perspective from an analog designer, but they also bring, as with all things, new issues that cannot be ignored.

Let's start by looking independently at each sub-aspect within a discrete-time filter and ending with a theoretical NB-IoT receiver on paper.

8.1 Discrete-Time Filters

8.1.1 Switches

A transconductors common-mode output voltage is typically set to half of its supply to maximize its output range, $600mV$ in our case, and with this we are in a region where NFET and PFET switches work quite bad (figure 5.8), pointing towards a transmission gate switch, DC blockage capacitor in the signal path for isolation or DC-shift its clocks (figure 5.4).

Two of these ideas are bad. Transmission gates will consume more than twice the power and the DC blockage will introduce signal losses (capacitive voltage division) and require huge amounts of area. Although the area aspect might be fine as these filters already require extensive amount. The best idea is to DC-shift all clocks to $V_{dd} + V_{CM}$ when ON and V_{CM} when OFF. This will of course draw more power and require more area, but it is still the best idea one have, their on-resistance is given in figure 5.9 and offers a flat response independent on V_{CM} . Although, by combining the same clock phase to a single DC-shifter one can at least save area.

The on-resistance of a switch, R_{on} , must be low enough to not impact the filters impedance, results from figure 5.10 points towards a R_{on} of less than a tenth of the filters single-ended impedance, or as seen in eq. 8.1. By decreasing the on-resistance even further would in theory make a more ideal filter, but as this effectively means increasing the size of a switch, one does also increase the parasitic

capacitance. And as C_R is usually small, in the order of ~ 100 fF, it don't require a lot to move the center frequency.

$$R_{on} = R_{eq}/10 \quad (8.1)$$

8.1.2 Transconductance

The active part that drives any discrete-time filter is also its biggest flaw, formally the transconductor. Parameters as voltage gain, noise, depth of sinc notches, linearity, mismatches, and common-mode voltage are all set by the g_m -cell one uses. Furthermore, the DT-BPF is semi-dependent of the input HPF within the transconductor, as one do not want to set this cut-off frequency as low as possible but rather close to the filters cut-off frequency (low side). If one sets it too low, one will amplify frequencies of no interest, possible interferers, while if it's too high the center frequency will increase its spread over process variations.

The way C_H is connected is not directly linked to the filter itself, but to its driver, the transconductor. In either way it is an important aspect. By connecting the C_H capacitor differentially, one saves twice the area in comparison to a single-ended connection, which on paper is the way to go. However, with a differential load the driving transconductor *sees* a light common-mode load while differentially a heavy. The results are seen in figure 6.6 and points towards two directions. To proceed with a differential load one must construct a transconductor that suppresses common-mode, which is a more complicated design and presumably reduced the g_m efficiency. With a single-ended load the requirements on CMRR is reduced, although some reduction is still needed, perhaps a stronger CM error amplifier is all one need.

The long story short here is, I would not use any of the four transconductors from section 6.1. They all suffer from some type of unwanted by-product, all but the CS stage lacks CMRR while has the lowest IIP2 and g_m efficiency, PD loves to amplify CM signals, FD is a worse version of the PD in all aspects, FB is hard to control (bias) and its AC-response is dependent on its input impedance.

What we are looking for is something similar to the PD but with CMRR, an idea that might work is to expand with another stage to its input, such that the first stage is a fully-differential error amplifier with bias and common-mode control, its output is then connected to the push-pull configuration as the PD already have. This would solve the common-mode issues but also keep the high g_m/I_d efficiency that a push-pull stage gives. What one pay with is an overall higher current consumption as the first stage needs its own bias current, and reduced linearity due to the decreased headroom. A higher supply voltage for the transconductors would in turn solve the reduced linearity but once again consume more current. The switches can still run on the same 1.2 V supply, or perhaps even lower. Another thing that one should added in every transconductor is a simple first-order aliasing filter, it does not have to be close to the given IF, perhaps five

times higher up, just as a precaution and to reduce the DT filter to another DT filter frequency mixing.

8.1.3 Relation Between IF and Sample Rate

An IF that is as low as possible is preferably used, mainly due to the reduction of required bandwidth within all active circuits, thereby minimizes the current consumption. With DT filters there is another aspect which points towards a low IF.

In figure 2.17 one can observe that the systems poles are close to the unit-circle at 0 and $f_s/4$ or $f_s/8$, depending on which M/M or $M/2M$ filter is used. And with a shorter distance the effective Q-factor is increased. The same conclusion but from another point of view is given in section 5.5.

A good rule of thumb is to run with a sample rate greater or equal than 500 or 50 of its IF for a M/M and $M/2M$ filter, see eq. 8.2, 8.3 for the exact definition. This will ensure a good filter response. The numbers 50 and 500 is not derived from any equation but rather by extracting the attenuation at an offset of one decade and comparing it with the theoretical value from multiple of MATLAB simulations.

$$f_{s,4/(4 \text{ or } 8)} \geq 500IF \quad (8.2)$$

$$f_{s,8/(8 \text{ or } 16)} \geq 50IF \quad (8.3)$$

The conclusion above goes against the common fact of increased power consumption at higher sample rates ($P \propto f_s$), which points towards a complete opposite direction. Furthermore, the impedance of a DT filter is inversely proportional to the sample rate (eq. 2.8), meaning that the transconductor that drives the filter will see a heavier load with higher sample rates, thus decreasing the voltage gain. And with lower filter impedance the switches on-resistance must also be decreased by a proportional amount (eq. 8.1), which will demand higher driving strength on its clock buffers and that will in turn increase the power consumption even further. There is much to gain by running a DT filter at a lower sample rate.

8.1.4 Layout

One aspect that I think will have a potential negative impact on the overall performance, more than common analog passive/active filter, something that was not considered in this thesis or any published paper, and it will only be seen in the latest steps of a design phase. It goes back to the share amounts of signal and clock phases that one must layout and connect, there will be a lot of routing. As an example, with a fully pipelined 8/16 filter one must match 8 g_m -cell, 256 switches, 16 C_H and 16 C_R (table 5.1), sure one can of course built these as a unit-cell and then multiple by 16 but there is still a lot of routing between these unit-cells were

each clock phase must have the same parasitic to have the same rise/fall times. At least I think it's safe to say that the layout of DT-filters require more time and an eye for details.

8.1.5 Simulation

Another aspect that was hardly brought up in previous research papers and also in this thesis, the lack of common-mode suppression in both DT filters and its g_m -cells will, to say the least, create issues with simulations. The first point is more of a designing aspect, low to none suppression of common-mode results in long settling time before Spectre can run its PSS + PXF simulation, if it at all converges.

If I've known what I know now, I would have spent more time on a more complex design of the transconductor, suppression of common-mode cannot be ignored. The second point is more of a sanity sake, you can't have your receiver oscillating with common-mode at the same frequency as your signal of interest.

A minor side note with discrete-time that one should understand from the beginning that they take longer time to simulate, I don't know how much one should prioritize this over other aspects, but again 'time is money' and being first to market with 'barely enough' performance can be better than late to the market with a superior product that beats your competition. The long story short here is, settling time and PSS + PXF is resource intensive, at least in comparison to simpler AC simulations. Although, if one plan for longer design time it should work just as good.

8.1.6 Power Consumption

To estimate the power consumption of a DT filter, several assumptions are needed. Starting from the on-resistance of a switch. Relationship to R_{eq} is given by eq. 8.1 and a process variable, $p_{40nm} = 400$ ($\Omega\mu m$), corresponding to the link between size and its on-resistance, extracted from figure 5.11. By now we can derive eq. 8.4, which gives the size of a single switch, given the choice of C_R and f_s . Furthermore, by interpolating figure 5.11 with a second-order polynomial the power consumption can then be derived, seen in eq 8.5. To obtain the power consumption of a DT filter, one simply multiple P_{sw} by the number of switches, which is given in table 5.1.

$$W_{sw} = p_{40nm}/R_{on} = 10p_{40nm}/R_{eq} = 10p_{40nm}C_Rf_s (\mu m) \quad (8.4)$$

$$P_{sw} = (4.6888 + 0.0651W_{sw} - 0.00015117W_{sw}^2)f_s/10^9 \quad (8.5)$$

The power consumption for the LPF and BPF variant was extracted from the equations above. For the LPF a filter order of 2, 4 and 6 were used, while the BPF

were with the 4/4, 4/8, 8/8 and 8/16 configuration. In both cases, the sample rate spanned between 1 and 10 GHz, and as f_s varies, C_R must also vary to keep the cut-off/center frequency constant. The capacitive span of C_R was [200, 100, 66.7, 50, 40, 33, 28.6, 25, 22.2, 20] fF, corresponding to 1 to 10 GHz, the end product is a constant R_{eq} of 5 K Ω at all f_s .

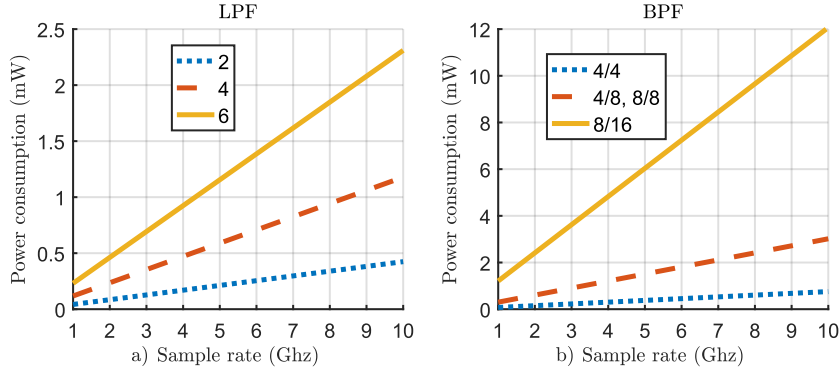


Figure 8.1: Estimated power consumption to run a DT filter. a) shows the LPF variant with a order of 2, 4 and 6 while b) shows the BPF with the 4/4, 4/8, 8/8 and 8/16 configuration. Their respective g_m -cells are excluded.

In figure 8.1 we see a linear increment of power usage with frequency for all topologies, the slope is the only thing that differs. The LPF shows a somewhat reasonable consumption, even at higher orders. The BPF variant shows a similar consumption, at least by excluding the 8/16 configuration. In any case, I think it's quite obvious that the 8/16 version is out of the question here, at least for battery powered devices. Perhaps it will work at lower sample rates, but then again, the issue of folding arises. One must really argue for the 8/16 version as in terms of filtering it is just a fraction better than the 4/8, although it will perform harmonic rejection. An interesting note is that the result from 8/16 fits very well as what was given in [8], well within ballpark numbers.

8.2 A Receiver on Paper

Now let's look back on NB-IoT and at least on paper create a receiver that is suitable. Starting with what we know.

8.2.1 LNA

Although the LNA is outside the scope of this thesis, it is important to at least mention it to see the whole picture. The RF frequency bands to cover are between

461 to 2200 MHz , grouped into four bands (table 3.1). This points towards an implementation of several different LNA paths with its own LC tank to resonate at the give frequency band, and I don't think I need to point out how much area this will require. The positive part with resonant circuits at respective RF band is the intrinsic harmonic rejection filter one get for free, hence sets looser requirements on the baseband part.

As an example, a RLC filter of 1Ω , $1.5 nH$ and $80 pF$ are doable on-chip and results in a resonant filter at $460 MHz$ with a Q-factor of 4.3, resulting in 30 and 39 dB of harmonic rejection at the 3rd and 5th harmonic, respectively. And at higher frequency bands the LC filter will be smaller and with a higher Q-factor.

The other solution is a wideband LNA as used in [8] (f_{-3dB} 0.1-4 GHz), which simplifies the overall design and saves a lot of area. However, a wideband LNA sets strict requirements on harmonics rejection. At $461 MHz$ the 3rd and 5th harmonics are at 1383 and 2305 MHz respectively, which is well within the LNA bandwidth, even the 7th and 9th harmonics could cause issues, although it will be attenuated by 16.9 and 19.1 dB respectively (Fourier expansion).

With that said, I doubt that a single wideband solution is the way to go as 70.3 dB of harmonic rejection is required (OBB - 16.9) to suppress the 7th harmonic. The 3rd and 5th harmonic are in theory doable to handle, but in practice this means calibration and extremely good matching between signal and clock phases. A more realistic way is to divide the frequency bands into two groups, 461 to 960 (ULB + LB) and 1475 to 2200 MHz (MB + HB), such that each group has their own LC tank with a variable C to set the correct center frequency, only two separated LNA paths are hence needed.

8.2.2 ADC and IF

Continuing on with the rest of the receiver and looking back at section 3.4, particularly at table 3.6 and figure 3.3.

The ADC resolution must be at least 12 bits as zero attenuation is possible with the ACS test ($f_{\Delta} = 0.2 MHz$). With 12 bits, the receiver chain must be able to achieve 70 dB of voltage gain, by assuming 20 dB of static voltage gain within the LNA the BB parts only needs to attain a variable gain between 0 to 50 dB .

Looking back in section 1.3, Arm requested an IF at 10 MHz and a maximum power consumption of 10 mW for the whole BB chain. However, with the given IF, 12 bits will not be enough, to remove interference specified in the IM test one needs a filter order higher than 10(!), and I think it's safe to say that this will definitely overrun the power budget.

There is only two directions to take, either one reduces the IF or increases the ADC resolution to 15 bits. With higher resolution the ADC complexity and power consumption increases. In [21, 22] a dual channel ADC with 15 bits and a sample rate of 20 MHz or 22.5 MHz will consume 9.4 mW or 9.72 mW , respectively.

Which is almost the same amount as the whole BB power budget. With that said, I will assume a 15 bit ADC is too much and therefore we must reduce the IF.

An IF at 2.5 *MHz* will require at least a fourth order filter and remove all IM2 products specified in the IM test. The IBB and ACS (1.2 and 2.2) tests will still cause IM2 products within our bandwidth, high IP2 requirement is still required on our transconductors. However, with 2.5 *MHz* the image frequency will be at 5 *MHz* in figure 3.2, hitting the end of the IM test. By moving somewhat up in frequency to 3 *MHz* the requirements is reduced, therefore the best-case IF is 3 *MHz*.

8.2.3 Filtering, Harmonic and Image Rejection

Let's summaries everything so far. The signal bandwidth of NB-IoT is extremely small, only 180 *KHz* is needed, pointing towards a sharp BPF without the need of a flat frequency response. The ACS test is covered by an ADC resolution of 12 bits while the rest of the tests are managed by a fourth order filter. What is left are harmonic and image rejection, let's start with the first one.

In the LNA section above we assumed a suppression of at least 30 *dB* at the third harmonic, and another 9.5 *dB* from the down-conversion within the mixer (Fourier expansion). With that said, we are still missing 47.7 *dB* (102.2-15-30-9.5) of rejection to balance signal and interference level, such that they are equal in magnitude. In figure 7.4 we see that it's possible to attain another 41.7 *dB* with somewhat high mismatch, only 6 *dB* is thereby left. With figure 2.22 in mind we know that another stage won't solve the problem. What we need is calibration to adjust any mismatch, just enough to achieve a total rejection of at least 47.7 *dB*. How this is achieved is beyond the scope of this thesis, all I can say is that it is needed and with it we will meet our requirements.

In any case, one could argue that even less attenuation is required as our ADC is specified to handle an extra 33 *dB* of headroom. The issue though, is that there is no difference between our wanted signal and an interference at $3LO + IF$, the down-converted products are exactly identical in terms of frequency and phase. Although the OBB interference is only specified as a static continuous-wave, making it quite easy to be removed in the digital world, as long as the ADC has enough DR to handle signal and interference. This argument makes sense in terms of what 3GPP has specified in their 'synthetic' tests but not in the real-world, one can never have enough filtering.

With an IF of 3 *MHz*, its image lands at -3 *MHz*, or 6 *MHz* in absolute terms, which rests directly within the IBB test. Given zero reduction of this image the required DR is then 46.2 *dB*, although the ADC already have 33 *dB* of headroom to absorb the ACS interference, to be later removed in the digital world, in theory this means that only 13.2 *dB* of IMRR is required.

And as these DT filter don't repeats itself at negative frequencies the theoretical attenuation is thereby given by the filter order and the distance between IF and

its image. One way of obtaining this is to convert the distance to octaves and then multiply by increments of -6. For each filter order one gain one additional -6 *dB* per octave in attenuation. The number of octaves is given by $\log_2(\frac{f_F+f_\Delta}{f_F})$ which simplifies to $\log_2(3) = 1.585$, as f_Δ is 2IF, which results in 9.51 *dB* of attenuation for every additional filter order. And as we have already specified a fourth order filter the requirements on image rejection is thereby attained with good margins to cover any potential mismatch.

8.2.4 Block Diagram

With everything we have learned so far it is time to build our receiver on paper. Starting from the output of a 8-phase mixer, its load should consist of a passive capacitor, working as an integrator, or in other terms, as a sinc filter to suppress aliasing. Its capacitance should be set such that the effective f_{-3dB} lands at 5 *MHz*.

Next in line should be a g_m -HR (figure 7.1) with some kind of calibration scheme to guarantee at least 42 *dB* of rejection. This circuit should also include a first-order LP filter to further suppress aliasing. The easiest solution is probably a passive single-order at its input, rough values are 30 *pF* and 1 *KΩ*. The f_{-3dB} should also be set to 5 *MHz*.

The 8 outputs are then combined such that only 4 are left, no further HR rejection is needed, thus there is nothing to gain with 8 signal phases. Another 6 *dB* of voltage gain is therefore attained due to the doubling in amplitude.

By now we have a second-order LP at 5 *MHz*, and with a sample rate of 2 *GHz* the expected attenuation at $f_s/2$ is thereby 91.7 *dB* ($12\log_2(1000/5)$) which should be well enough to solve all folding issues (section 5.6.4) but also help with interference that is semi-close to the IF.

This is then followed by two DT filters with its own g_m -cell at its output, the first DT filter is driven by the g_m -HR block while the last works as a buffer with gain, driving the ADC. A capacitive load between the last stage and the ADC is probably a good thing to have, further improving the design by another anti-aliasing filter before any information transforms into digital bits. The DT filters in question should both be configured as a fully pipelined 4/8, running at an effective sample rate of 2 *GHz* with C_R of 100 *fF*, which is equivalent to a 5 *kΩ* load. A value of 3.6 *pF* on C_H will center the frequency at 3 *MHz*, keep the capacitor as single-ended to load common-mode signals as well. One should strive for low capacitive values (section 5.6.5).

The choice of transconductor is left out as something better is needed than the four transconductors from section 6.1, see the Transconductance section 8.1 for more thoughts on a better version. In any case, variable gain between 0 to 50 *dB* is needed, which should be a rather simple task by controlling its bias current.

By now we should have a working baseband receiver that can handle all tests, as specified by 3GPP. A block diagram is given in figure 8.2. The required IIP2, IIP3

and approximated power consumption of this receiver is given in the two sections below.

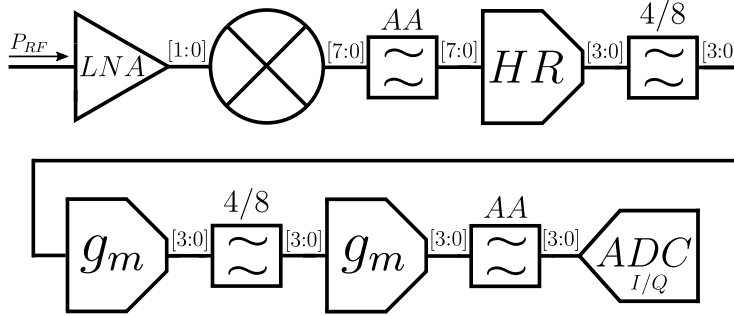


Figure 8.2: Block diagram of a NB-LoT receiver.

Nevertheless, it is worth pointing out our assumptions again. Two perfect LNA with high linearity, both having an LC tank for their respective RF band, ULB + LB and MB + HB. A perfect mixer with its 8-phase clock generator, which is in turn driven by a differential LO between 1.844 to 8.8 GHz. Furthermore, we are missing noise requirements for the whole chain, which was intentionally left out due to time constraints.

8.2.5 Requirements on IIP2 and IIP3

Looking back at the approximated requirements on IIP2 and IIP3 in table 3.7, but with our assumed LNA gain of 20 dB.

Starting with ACS, test 2.1 and 2.2 will be the hardest in terms of linearity as it's the test where the interference is closest to our wanted signal, but also due to the high-power of -25 dBm, no attenuation is assumed. The 20 dB from the LNA is enough for our signal to reach $P_{ADC,min}$, no further amplification is needed. But this also means that our interference is also amplified by 20, to -5 dBm. therefore the actual IIP value is 20 dB higher than given in the table, the true value is thereby an IIP2 of 38 and IIP3 at 16.5 dB.

All other tests will give a lower IIP than the ACS test, this is due to their greater distance to the IF and thereby attenuation is achieved from filtering, even though the power difference between signal and interference are greater. As an example with IM test 1, with a notation of signal and interference power as $[P_s, P_i]$.

Starting at [-96.2, -46], the LNA increases the levels to [-76.2, -26]. The second-order LP filter at 5 MHz reduces this to [-76.2, -26.68], which is ~ 20 dB lower from the ACS test. What differs here is that the signal is still too low, another 38.2 dB is needed to reach $P_{ADC,min}$. Assuming a voltage gain of 10 and another 6 dB by combining the 8 signals to 4 the effective gain is thereby 16 dB from g_m -HR stage, resulting in a level of [-60.2, -10.68]. The first 4/8 filter suppresses the

interference by another 9.52 dB ($12\log_2(\frac{3+2.2}{3})$) which gives $[-60.2, -20.2]$. Which is followed g_m -cell of 12 dB , 4/8 filter and another g_m -cell of 12 dB , resulting in $[-48.2, -8.2]$, $[-48.2, -17.72]$, $[-36.2, -5.72]$ respectively. The signal is now above $P_{ADC,min}$, the interference is below $P_{ADC,max}$ and all previous levels were lower than what the ACS test gave.

To follow up on our four transconductors. With IIP2 in mind, all but the CS stage will handle the power levels. On IIP3 only the FB stage is able to handle the hard ACS test, highlighting once again that further improvements are needed on a new and better transconductor. In any case, the simulation of IIP2 was done with a rather high mismatch of 5 %, pointing towards that the actual IIP2 is probably higher for all topologies

8.2.6 Power consumption

The power consumption on our theoretical baseband receiver with a voltage gain of 50 dB is calculated as followed. The g_m/I_d efficiency is taken from 6.5, which is converted to voltage gain by eq. 2.10. The first amplification stage is of type g_m -HR which translate to current scaling of $2 + \sqrt{2}$, for each signal phase as there are three g_m -cells for one signal phase, in which one is scaled by $\sqrt{2}$ time more than the other two. The last two stages consist of four common signal paths, meaning its bias current is multiplied by 4. Last, the power consumption for the 4/8 filter is taken from 8.1.

Two cases are given. In the first the g_m -HR stage is of FB type, while the other one is PD. In the second case all stages consisting of the FB topology, which in turn is the more realistic one due to the high IIP3 requirements.

With the FB and PD combination a bias current of 100 and 150 μA are used, respectively for each single-ended g_m -cell. resulting in a voltage gain of 51.2 dB . The expected consumption is thereby 4.72 mW . While with only FB stages the bias is increased to 100 and 225 μA (100 for $g_m - HR$), resulting in an increment of consumption to 5.44 mW and a voltage gain of 51.38 dB . In both cases the DT filters are constant at 1.21 mW .

Given the more realistic scenario the total power consumption is thereby 6.65 mW at a 1.2 V supply, which is well below our requirement of 10 mW .

Conclusions

9.1 Discrete-time Low-pass Filter

The LPF topology is the simplest realisation of a DT filter and looking at its most important parameter, the cut-off frequency, it is only dependent on one capacitance ratio, α_1 (eq. 2.5), and its sampling frequency (eq. 2.21). Together with table 6.6 and the assumption that the sampling frequency is a derivative from a well design PLL, or another equivalent source, it is safe to say that the core principle of a DT-LPF is by far more stable from mismatches than a regular RC filter, both passive and active.

All g_m -cell from section 6.1 uses an input capacitor to isolate its bias voltage, which means that a flat response from 0 to its cut-off frequency is impossible. As an example, a resistance of $100\text{ K}\Omega$ and a (huge) capacitor of 100 pF will result in a cut-off frequency of $\sim 16\text{ KHz}$, one can of course increase the resistance, but it might increase the noise, depending on the source impedance of the signal. As a last point, these filters can only create real-poles and given a high-order filter more than 3 dB will be lost at its cut-off frequency (11.2 dB with a 7th order in [18]), although this was improved with complex poles in [23]. There are a few more issues but we will bring it up within the BPF section below.

The end question will always be, should one use these filters instead of regular passive or active LPF? To answer this, the first question one should ask themselves is, do I have a fast and stable clock already available, and can I route this clock to the block itself in layout? If no, then a regular passive or active filter is the way to go. If yes, then there might be reasons to use these filters. By looking at table II in [18] (performance summary and comparison with the state-of-the-art) one finds a good overview of different LPF topologies, and there are parameters were DT filter are better and were they are worse, but general they are in the same order. The only parameter where they stand out to the positive is the variability of bandwidth were pure analog filter greatly suffers.

In my own opinion, there is only a few scenarios where I would go with DT-LPF, which is a case were stability of cut-off frequency over temperature is notably

important, and perhaps low noise performance. In other cases, I would go with analog filters due to its simplicity as a whole but also as there is no folding issues to worry about with pure analog filters.

9.2 Discrete-time Band-pass Filter

The DT-BPF topology is more complex than the simple DT-LPF due to the share amount of signal and clock phases one requires, this varies of course depending on which M/M or $M/2M$ one uses. As a starting point, it is similar to the LPF variant, everything that is true for the LPF is also true for the BPF. The center frequency of M/M and $M/2M$ are dependent on two capacitance ratios, α_1 and α_2 (eq. 2.5, 2.6), and its sampling frequency (eq. 2.45, 2.35), which points towards a stable filter over process variations, at least by only looking on its core concept, theory and simulations.

The filter in question is highly configurable and one of few ways to implementing harmonic rejection, image rejection, and baseband filtering at the same time, although for harmonic rejection one must use 8 or more signal and clock phases. A 8/16 filter achieves in theory 22 dB rejection on both the third and fifth harmonics [8]. Although it was possible to achieve 36.5 dB of rejection (figure 7.4) with the DT-HR version (figure 7.1), given an phase error of 1°. The same paper also shows measurements of harmonic rejection with two 8/16 filters and one g_m cancellation (figure 7.1), the combined rejection where between 58 to 75 dB, although it was only 3 samples.

In my mind, this matches what the theory says, meaning if one block give X then two blocks won't give $2X$ of rejection, as demonstrated in figure 2.21. Note that this concept is also true for image rejection as it is built upon vector cancellation. To achieve linear scaling, each rejection block must have its own calibration scheme and low mismatches on its gain and phases. Just because one uses a DT filter it doesn't automatically mean one can skip calibration.

Should one choose a BPF with discrete-time or just go with the standard analog passive/active BPF? Assuming a fast and stable reference clock is already available, and area is of no concern, then I would still say no, at the moment there is simply too much against the architecture itself. Key issues are folding and power consumption. Table 5.2 shows an overview of three 8/8 filters with their respective g_m -cell at different sample rates, or in other words, different decimation ratios. The end result shows that a sample rate lower than twice the LO frequency will increase the harmonic noise floor enough such that the weakest RF signal will be below it, and remember, this simulation was with no mismatch whatsoever, the real result is probable much worse. The high power consumption was summarised in section 8.1.6. Given the power budget of 10 mW, it is safe to say that the 8/16 draws too much power, even at lower sampling rates. Without the 8/16 only the 8/8 is left that achieves harmonic rejection, but the 8/8 only gives a first-order filter which again points to a high power consumption as four 8/8 filters, and thereby 32 g_m -cells, are needed to acheive enough filtering.

Furthermore, there is nothing with discrete filters that are in particular better for NB-IoT, mainly due to the low bandwidth NB-IoT requires and thus pointing towards a low IF. Which is the opposite where these filters are good at. Discrete filters does not solve any issues that can be solved with previous architectures, such as the homodyne receiver in [17]. A receiver without the front-end filter was also never achieved, mainly due to the share amount of RF bands to cover and thereby sets high requirements on harmonic rejection, as high as the 7th or 9th harmonic.

Given that analog BPF can also create complex poles without any folding issues, attaining image rejection and consume less power [24], there isn't any reason to use DT filter. Harmonic rejection is still possible with standard g_m cancellation as seen in figure 7.1. Although in the future when smaller process nodes ($<10\text{ nm}$) becomes more common I expect to see a rise in analog DT filters.

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