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Laminated HZO on InAs:

A study of as-deposited ferroelectricity

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Abstract

As the limits of transistor feature size scaling is reaching its saturation, new innovations are needed to prevent performance loss. High performance transistors on the III/V semiconductor platform implemented with ferroelectric oxides might in the future satisfy this demand. But the integration of ferroelectrics on materials such as InAs degrades the substrate and other vital components from the high processing temperatures required to achieve orthorhombic crystallinity. In this master thesis, new engineering strategies have been explored to improve the thermal budget of ferroelectric hafnium zirconium oxide (HZO) implemented on InAs. This was realized through integration of atomic layer deposition (ALD) grown oxides in primarily metal-oxide-semiconductor capacitor (MOSCAP) devices using conventional nano-processing techniques. The MOSCAPs were later characterized by standard current-voltage (IV) measurements and the positive-up negative-down (PUND) technique in order to determine the oxide quality, and especially any ferroelectric behaviour. Ferroelectricity was found in both MOSCAP and metal-insulator-metal capacitor (MIMCAP) structures with the highest as-deposited remanent polarization on InAs at 6.6 $\mu C/cm^2$ and 12.2 $\mu C/cm^2$ in the MIM stack. The highest remanent polarization among the MOSCAPs was found in a scaled sample at 6.4 nm, which outperformed samples with similar, but thicker oxides. IV-sweeps also revealed suspected ferroelectric tunnel junction (FTJ)-like behaviour in MOS devices. An annealing study was conducted to investigate if enhanced remanent polarization could be achieved by performing RTP on as-deposited samples. This yielded a remanent polarization of 14.5 $\mu C/cm^2$ after post-process anneal at 450 °C for 300 s. As-deposited ferroelectric HZO offers new paths for integration of the emerging material in temperature sensitive processes, but requires further research to maximize its potential.

Populärvetenskaplig sammanfattning

En kall eftermiddag den 23 december 1947 hände något fantastiskt på ett laboratorium i New Jersey, USA. Forskare vid Bell laboratoriet demonstrerade för första gången en funktionell transistor! Transistorn är en elektrisk komponent som har tre terminaler där man kan ansluta andra komponenter. Om man leder en ström eller spänning genom ett par av terminalerna kan man kontrollera strömmen genom ett annat par av terminaler. Detta låter som vilken annan elektrisk komponent som helst och inte ens forskarna vid Bell laboratoriet kunde ha förutspått att de hade kommit med århundradets uppfinning.

Transistorn är komponenten som utför beräkningarna i nästan all modern teknik. I allt från mobiltelefonen till bilen, från torktumlaren till kaffemaskinen sitter transistorn och tuggar ettor och nollor medans du njuter av morgonens espresso. Sedan dess uppfinning har transistor tagit många vägar i sin utveckling. Arkitekturen har förändrats drastiskt och de har mer än något annat blivit mindre. I den moderna processorn som driver din dator finns hundratals miljoner transistorer, men processorn i sig är bara några få kvadratcentimeter stor!

Detta är möjlig för att i takt med att samhället har strävat efter snabbare, effektivare och mindre teknik har en enorm halvledarindustri växt fram. Halvledaren är den typ av material som möjliggör transistorn. Dessa är elektriska isolatorer (de leder inte ström) som kan göras ledande (som en metall). Både halvledarindustrin och forskare har försökt möta den stora efterfrågan på bättre transistorer genom att utveckla avancerad teknik som låter oss manipulera och bygga med material på nanoskalan, alltså mindre än en tusendel av ett hårstrå. Detta har lett till otroligt små transistorer. Men idag har vi börjat stöta på ett fundamentalt problem: vi närmar oss samma skala som enskilda atomer! Detta gör att man måste ta hänsyn till bland annat så kallade kvantfysikaliska fenomen. För att fortsätta förbättra tekniken behövs det nya strategier, som att till exempel undersöka exotiska material.

Ett sådant material undersöks i detta examensarbete: ferroelektriska kristaller. Dessa kan liknas vid ferromagneter, fast istället för att avge ett magnetisk fält som gör att de kan fästas på kylskåpet avger ferroelektriska material istället ett elektriskt fält. Detta tillstånd kan bestå utan att man lägger på en elektrisk spänning vilket gör att de kan användas extremt energisnålt, samtidigt som de har andra användbara egenskaper. De kan bland annat implementeras som supereffektiva minnen eller som synapser i artificiella hjärnor!

Ett stort problem med den mest användbara klassen av de ferroelektriska materialen är att de kräver väldigt höga temperaturer vid tillverkningen, som i sin tur förstör andra saker i processen. I detta projektet har jag undersökt strategier för att producera dessa kristaller vid mildare temperaturer. Detta har skett genom att ändra hur materialet byggs på den atomära skalan. Genom att implementera materialet i en pytteliten kondensator har jag kunnat karaktärisera hur väl detta fungerat. I framtiden kommer kanske dessa material hitta sin väg till din ficka i form av effektivare transistorer.

Acknowledgements

First, I want to thank my supervisor Lars-Erik Wernersson who not only gave me the opportunity to do research in an area of personal interest, but also provided guidance through interesting discussions and great advice. I also want to thank Anton Persson who throughout this project not only was an excellent lab-coach, but also provided me lots of motivation for my work. A big thanks also goes to Hannes, Robin, Theodor and others in the nanoelectronics group, for both your help and our interesting discussions. I also want to acknowledgement the lab staff at Lund Nano Lab, for providing me a lot of support in the lab whenever needed. Finally, I want to thank my friends and family for highlighting my free time.

List of Acronyms and Abbreviations

ALD Atomic Layer Deposition
APM Ammonia-Peroxide Mixture
As Arsenic
BEOL Back-End Of the Line
CMOS Complementary Metal-Oxide-Semiconductor
CV Capacitance-Voltage
CVD Chemical Vapour Deposition
EIT Department of Electrical and Information Technology
FTJ Ferroelectric Tunnel Junction
FeFET Ferroelectric Field-Effect Transistor
FRAM Ferroelectric Random-Access Memory
GIXRD Grazing Incidence X-ray Diffraction
GPC Growth Per Cycle
In Indium
IE Current-Electric Field
IV Current-Voltage
HCl Hydrochloric Acid
Hf Hafnium
HZO Hafnium Zirconium Oxide
IPA Isopropyl Alcohol
La Lanthanum
LNL Lund NanoLab
MFT Mean-Field Theory
MIMCAP Metal-Insulator-Metal Capacitor
MIS Metal-Insulator-Semiconductor
MOSCAP Metal-Oxide-Semiconductor Capacitor
MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor
MOVPE Metal-Organic Vapour Phase Epitaxy
MPB Morphotropic Phase Boundary
MSE Mean-Square Error
MW Memory Window
NMOS n-channel Metal-Oxide-Semiconductor
PEALD Plasma-Enhanced Atomic Layer Deposition
PE Polarization-Electric Field
PMA Post-Metallization Anneal
PUND Positive-Up Negative-Down
PVD Physical Vapor Deposition
PVDF Polyvinylidene Fluoride
PZT Lead Zirconate Titanate
RTP Rapid Thermal Processing
SS Subthreshold Swing
Ti Titanium
TEMA-Zr Tetrakis(ethylmethylamino)zirconium
TER Tunneling Electroresistance
TDMA-Hf Tetrakis(dimethylamino)hafnium
TMA Trimethylaluminium
UVL Ultraviolet Photolithography
Zr Zirconium

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1 Introduction

We live in a time that could be labeled the age of silicon. The abundant semiconductor has laid the foundation for the powerful electronic devices that drive both the economy and our daily lives in the form of computers, mobile phones, and transportation, just to name a few. For the past 30 years, the scaling of Si based transistors has followed Moore's law which states that "the number of transistors and resistors on a chip doubles every 24 months" [1], which implies an exponential trend. As the devices approached the nanoscale more than 20 years ago, this trend was close to being broken, but new innovations related to, for example, UV-lithography and material science always rejuvenated the trend [1]. Today, as the feature sizes of planar devices approach the atomic scale, we are running out of actual things to make smaller. The future requires new ways to "scale", for example, by exploring the third dimension to a greater extent or by implementing exotic materials [2]. One such class of materials is the hafnium-based ferroelectrics, which can be implemented as the insulator in a modern transistor. Ferroelectrics can enable power savings in transistors or be the foundation of dense memory arrays for faster computation [2]. Another direction is leaving the comfort of the Si-platform and exploring III/V semiconductors, such as InAs. These materials offer transport properties superior to Si [3] which makes them interesting for high-performance electronics.

This master thesis explores the implementation of zirconium-doped hafnium oxides (HZO), mainly on planar InAs substrates. This is realized using modern nanoprocessing tools and techniques, such as atomic layer deposition (ALD) and UV photolithography (UVL) at the Lund Nano Lab (LNL) clean room facility. ALD is used to grow oxides with atomic control on InAs followed by top-down processing to define the metal contacts to finalize a Metal-Oxide-Semiconductor Capacitor (MOSCAP). These MOSCAPs are then characterized at the research lab at the Department of Electrical and Information Technology (EIT). Here, the electrical properties of the oxides are evaluated and the search for ferroelectric crystallization is achieved using the Pulse-Up-Negative-Down (PUND) technique. The goal of this thesis can be summarized with the following points

- Investigate the behaviour of HZO on InAs substrates at elevated ALD growth temperatures.
- Search for as-deposited ferroelectricity in the laminated HZO.
- Optimize a potential scalable ferroelectric laminate (with ferroelectric and electrical properties in mind).
- Investigate the possibility of boosting the ferroelectric properties by performing RTP slightly above the deposition temperature.
- Characterize the oxide for device properties (relative permittivity and FTJ switching).

InAs was chosen as the substrate partly because it has excellent characteristics for high performance transistors (e.g., high electron mobility), but it was also chosen because it degrades at high temperatures [4], [5], thus making it a great test platform.

This report is split into several parts with an initial block covering the basic theory of the ferroelectrics and the processing techniques relevant for their fabrication, found in sections 2-3. This is followed by sections 4-5 which covers the experimental work and characterization methods. The results are presented in section 6, which starts with a presentation of the different process series produced in this thesis. Finally the the results are discussed (section 7) followed by some concluding remarks (section 8). At the very end of the report you will find an appendix (section 10) with some complementary data.

2 Ferroelectric materials and their applications

As the name suggests, the ferroelectric effect shows striking similarities to ferromagnetic materials. However, rather than the material exhibiting a permanent magnetic moment, ferroelectric materials instead show remanent electric polarization without an external electric field [6]. This allows materials which can exhibit charge states that are programmable by applying an external field, and that remains as the field is removed. In this section, the basics of ferroelectric materials and their applications are reviewed.

2.1 A short history

The ferroelectric effect is not a 21st century discovery, as the term was first established by *Erwin Schrödinger* in 1912 [7]. The concept of a permanent dielectric polarization had previously been theorized by *Peter Debye*, but *Schrödinger* was interested in extending this theory to predict real ferroelectric materials. But it took until 1920 for the first experimental evidence of ferroelectricity to be discovered by American physicist *Joseph Valasek* [8]. In his paper, Valasek examined the interesting material Rochelle salt, since it had previously exhibited piezoelectric effects (where a charge is released proportional to an applied force on the crystal). Deviations from the expected behaviour of an, at the time, conventional piezoelectric could be explained by Valasek to be related to the hysteresis-like polarization of the material [8]. During the rest of the twentieth century, several more ferroelectric materials were discovered, and this was especially accelerated during the Second World War, where the high dielectric constant of the ferroelectric materials were required for sonar technology [7]. This led to the creation of the first artificial ferroelectric perovskite, barium titanate, which exhibited a dielectric constant above 1000 (this was an order of magnitude greater than any other known dielectric at the time) [7]. Until 2011 the most studied class of ferroelectric materials were ceramics with perovskite structure, but their complicated crystal structure makes them unsuitable for most semiconductor integration [6]. However, in 2011 ferroelectricity was discovered in HfO_2 thin films [9], a material that was already well established in the modern semiconductor industry as a high-k dielectric[1] in transistor gate stacks [2]. This development meant a new generation of ferroelectric device applications could be realized.

2.2 Basic theory

To understand the practicality of ferroelectric materials for applications such as memory modules and transistor scaling, it is essential to explore fundamental physics and material science. As you might have inferred from the previous section, the ferroelectric effect is found in crystalline materials. These should contain a crystal structure that exhibit non-centrosymmetric symmetry [6]. This means that ions in the crystal can settle into energetically stable positions that results in a polarization state removed from neutrality. Similar to ferromagnets, a common way to describe ferroelectric materials is with the formation of *domains* in the crystal that contain ions which have electric dipoles that are all oriented in the same direction [10]. When subjected to external bias the charge state present in each crystal domain will switch to conform with the applied field. A field that exceeds a certain threshold, called the coercive field, E_c, will switch all domains in the entire crystal domain. This will leave the material in a state of constant remanent polarization, P_r. This behaviour can be seen in a ferroelectric hysteresis curve as depicted in Fig. 1. For large positive fields above E_c the material will polarize in the positive direction, and vice versa for negative fields. The coercive field and remanent polarization, P_r are noted in the figure. The method that is used to generate P-E graphs like this is expanded upon in section 5.3. The remanent polarization, and the coercive fields, are the most commonly reported figures of merit for ferroelectrics, as they concisely summarise the switching properties. For certain applications such as the integration of ferroelectrics in memory modules, the actual quantities of these become relevant as the device properties are directly linked to, for example, high P_r. An example of this is the performance of ferroelectric FETs, detailed in section 2.4.1, which is directly related to the remanent polarization [11].

[1] An industry term for high dielectric constant.

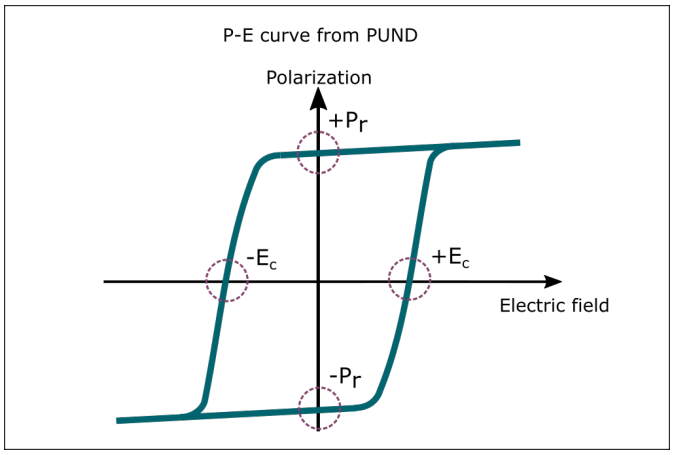


Fig. 1: This figure depicts the typical hysteresis behaviour of the polarization in a ferroelectric material. The polarization which remains at zero external field, the remanent polarization (P_r), is indicated. Also noted is the electric field required to switch the ferroelectric domains, the so-called coercive field (E_c). While the coercive field appears to be symmetrical for positive and negative bias here, this is not necessarily the case as e.g. interface charge traps might respond differently to different signs of the external bias.

In order for a material to crystallize into a structure that allows for ferroelectric domains to form, it has to go through a phase transition that removes some crystal symmetry through the movement of ions in the structure into non-centrosymmetric sites. The most prominent way to model this behaviour is Landau theory that treats the interactions of the system microscopically, and is unconcerned with atomic level interactions [12]. Landau theory can be applied to any system that exhibits phase changes regarding symmetry, such as ferroelectric materials. The energetics of the system in, and around the phase change with respect to an order parameter and other intensive properties are given from the *Landau free energy*, F (usually given per unit of volume). For ferroelectric materials we are concerned with the order parameter polarization (P) [12]. In order to construct a simple model of the system in the Landau picture, one usually adopts a mean-field theory (MFT), to disregard long range interactions. This is made possible by only taking into account the influence that the nearest or next-nearest state has on each state [13]. MFT is a powerful approximation for many-body systems and it can allow you to greatly simplify calculations by removing spatial fluctuations in the Landau model (assuming the polarization is a constant function of space). This is usually also referred to as the *Landau-Devonshire* model, wherein the free energy can be expressed as a power function of the order parameter, in this case the polarization, according to [12], is given by

$$F = F_0 - EP + \sum_{k=1}^{n} \frac{a_k}{k} P^k, \tag{1}$$

where a_k are expansion coefficients that are dependent on intensive parameters (meaning they are independent of system scale, e.g. temperature and pressure), while F_0 indicates the Landau free energy density in the high temperature regime, where it is independent of the polarization state. The term $-EP$ contains the contribution to the free energy from an external field E. Because the ferroelectric phase is equivalent to a non-centrosymmetric crystal structure, and if the polarization state exists around the centre of inversion, the Hamiltonian has to be invariant to the change of polarization state ($P \rightarrow -P$) [12]. Since the states have to be energetically equivalent, all odd powers of the summation in equation 1 has to fall out, giving

$$F = F_0 - EP + \frac{a_2}{2} P^2 + \frac{a_4}{4} P^4 .... \tag{2}$$

A further simplification that is often considered is that the coefficients are assumed to only be temperature dependent ($a_k = a_k(T)$), disregarding the influence of external pressure, magnetic fields etc. Now critical temperatures for first- and second-order phase transition of crystals can be found [12]. You can also illustrate the energy landscape of a ferroelectric by plotting equation 2 for certain values of a_k. A full derivation reveals that the double-well structure found in Fig. 2 is meta-stable for temperatures below the critical temperature (or Curie temperature), T_c [12]. In Fig. 2 the effect an external field has on the energy landscape is also depicted.

For certain materials such as HZO, which will be discussed in section 2.3, another response to external electric fields might occur that distinguishes itself from the standard ferroelectric behaviour. This is the antiferroelectric phase of a crystal, where the crystal structure contains dipoles that are oriented antiparallel to each other, which causes the total polarization on the macroscopic level to cancel for zero external field [14]. These dipoles can all be switched in the same direction by applying an external field similar to ferroelectrics, but will return to the antiferroelectric state once the field is removed[2].

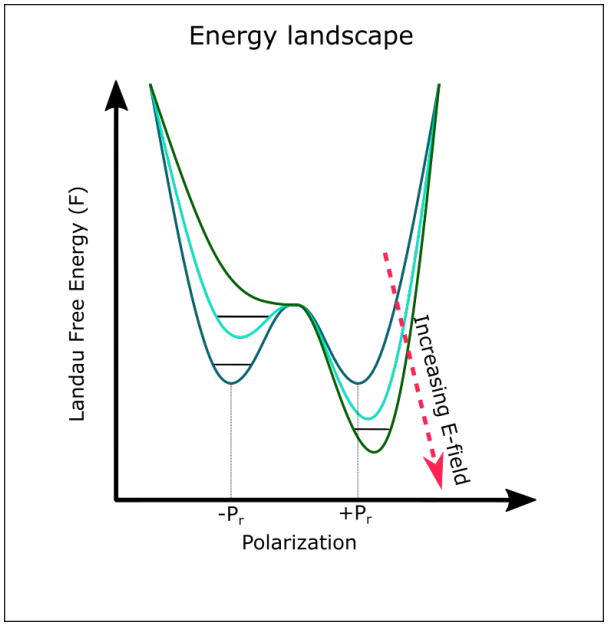


Fig. 2: This figure depicts the energy landscape generated from equation 2 and how it changes as an electric field is applied across the ferroelectric. Once the electric field passes the coercive field, the state (black horizontal line) can pass the energy barrier and settle into the "positive" polarization state. This figure is partially inspired by [15]

2.3 Ferroelectric materials

There are several different classes of ferroelectric materials, and what they all have in common is that they are crystalline materials that can undergo a phase transition into a non-centrosymmetric structure. Instead of covering this extensive topic in detail, let us instead consider some outstanding examples. This topic is considered in great detail in [10].

2.3.1 Perovskites and Organics

Among the inorganic ferroelectric material classes, the most extensively studied group is likely the perovskites (materials who share the crystal structure of perovskite). One of these materials is *lead zirconate titanate*, often abbreviated PZT. This compound has the chemical formula $PbZr_xTi_{1-x}O_3$, where x indicates atomic fraction [10].

[2]These materials have found use as high energy density capacitors for advanced weapon systems or energy tools [14].

Above its Curie point this material behaves as a piezoelectric, meaning it generates a voltage as a response to an external force. In this state it has the crystal structure illustrated to the left in Fig. 3, but if the crystal is cooled quickly below T_c, it can transition into its ferroelectric phase through a second-order phase transition resulting in the asymmetrical crystal depicted in Figs. 3 and 4 [10]. This is the ferroelectric tetragonal phase of PZT [3] [10]. The polarization switching mechanism is indicated by the green arrow in Fig. 4a. This material is very flexible as both its electric and ferroelectric properties can be tuned to a high degree by doping the crystal with various ions [10]. It has found applications in everything from ultrasound transducers to ferroelectric memories (in FRAMs, which are detailed in section 2.4.1).

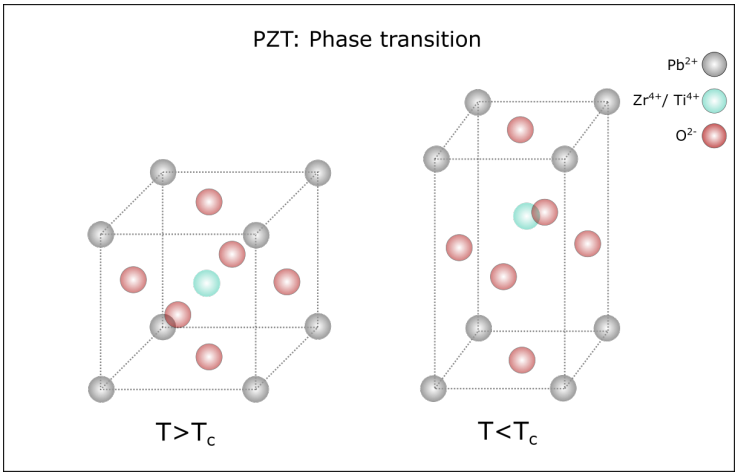


Fig. 3: The transition of PZT from its standard piezoelectric phase to the tetragonal ferroelectric phase when cooled below the curie point. This figure is inspired by a similar figure in [10].

Organic materials, and especially polymers, have also been found to exhibit ferroelectric properties. The first polymer that was found to be ferroelectric was *polyvinylidene fluoride* (PVDF), which can be seen illustrated in Fig. 4b with one of its switching mechanics. This class of materials have dipoles spread along the organic chain, that can align to an external field through several different mechanisms (e.g., shrinking, stretching, and conformation changes) [10]. The last of these mechanisms is displayed in Fig. 4b where the polymer flips between two conformations to align with the field. Several of these chains will align in parallel to form the crystalline polymer structure of PVDF. There is a plethora of possible applications for these materials, as the material properties can be tuned to a high degree (e.g., the dielectric constants can be tuned by adding nickel to the polymer blend when fabricating PVDF [10]). They are also attractive for flexible electronics [6], which can be used for wearable electronics.

[3] But the material can also settle in a ferroelectric rhombohedral structure under certain thermodynamic conditions, which also exhibits ferroelectric behaviour [10].

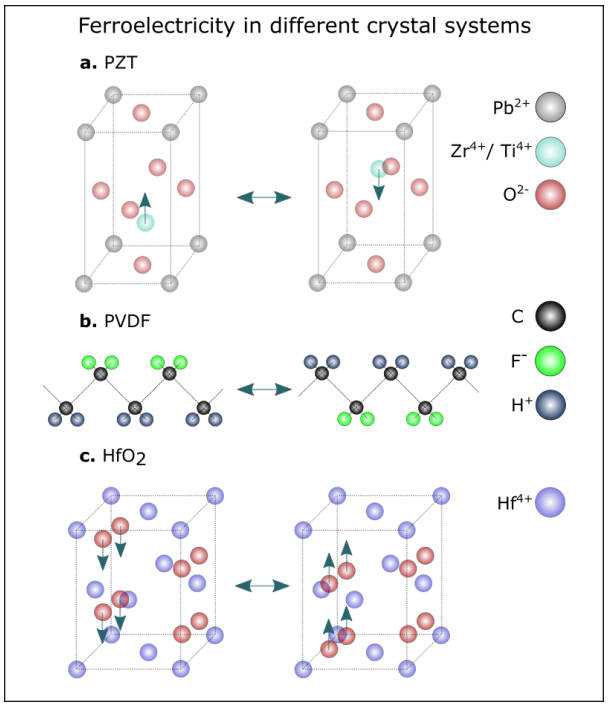


Fig. 4: This figure illustrates different switching mechanisms of ferroelectric crystal systems. This figure is inspired by [6].

2.3.2 Thin film ferroelectrics

Even though perovskites such as PZT have found their way into some electronics, they face severe problems regarding scaling. This is because of the small band gap causing large leakage currents, and the difficulty of integrating them in suitable *Chemical Vapour Deposition (CVD)* processes such as *Atomic Layer Deposition* (ALD), which will be expanded on in section 3.1 [16]. When ferroelectricity and anti-ferroelectricity was first reported in hafnium dioxide in 2011 [9], these problems could be surmounted since the material had already been established as one of the standard high-k dielectrics in the industry since several years back[4]. The high-k (high relative permittivity) properties of HfO_2 are beneficial since it allows a thicker gate oxide in a transistor with equivalent capacitance compared to lower-k dielectrics, enabling further scaling [17].

The ferroelectricity in HfO_2 is widely thought to be the result of an orthorhombic phase with the space group (symmetry group) $Pca2_1$ [16]. This phase is not found in the conventional phase diagram[16], but is believed to originate from a mechanical strain induced in the material, which forces crystallization into a tetragonal-esque crystal rather than the monoclinic fluorite structure, when subjected to rapid thermal treatment [9]. This strain can for example be induced by a capping layer, such as a top metal [9]. In Fig. 4c the orthorhombic crystal structure of HfO_2 is depicted together with the oxygen switching mechanism of the $Pca2_1$ space group that allows different polarization states in the material.

After the discovery of ferroelectricity in HfO_2, an intense decade of research on the material followed, as many of the device concepts (that will be discussed in the next section), could now be implemented on the silicon platform. It was soon realized that doping the hafnia (HfO_2) films could elevate the remanent polarization, while keeping the ease of integration [16]. Many dopants are promising, for example, lanthanides such as gadolinium and lanthanum [18]. Especially La doped films have achieved a remanent polarization of up to 55 $\mu C/cm^2$, and are only outperformed by the dopant considered in this project, zirconium [18]. Zr doped Hf thin films are most commonly abbreviated as

[4]This makes it curious that it had not been discovered earlier since it was probably one of the most well studied compounds ever at the time due to its prominence in the intel CMOS process.

HZO, and this can allude to any film that has the composition $Hf_xZr_{1-x}O_2$. The similar properties shared between Hf and Zr means the films can become ferroelectric for Zr concentration exceeding 50% [16]. Ferroelectricity is most common in HZO for Zr concentrations between x=0.3 and x=0.5, while for concentrations ranging from x=0.7 to x=1, the zirconia (ZrO_2) settles into a tetragonal crystal structure that exhibits antiferroelectricity [16]. For a detailed study of the effects Zr doping has on the ferroelectric properties of HZO, see [19]. The high Zr concentration allowed in HZO is also beneficial due to the low crystallization temperature of zirconia, which can force the crystallization of hafnia into the orthorhombic phase at much lower temperatures than normal, allowing for thermal treatments as low as, and below 400 °C for some deposition techniques after top-metal capping [4], [16], [20]. The benefits of this, and methods to push the temperature even lower, are further discussed in section 3.3 and it is one of the core problems this project hopes to address. Another feature of Zr doping is the formation of a morphotropic phase boundary (MPB) between the orthorhombic HfO_2 and tetragonal ZrO_2 [21]. The MPB arises at the boundaries of crystals that are chemically different [21]. The MBP of HZO can support both the tetragonal and orthorhombic crystal phases since these differ just slightly in free energy, and when present it boosts the relative permittivity of the film [21].

2.3.3 HZO laminates

The ALD processing technique, which was mentioned earlier, allows for atomic control of thin film growth and therefor the opportunity to design insulators with unconventional structures. One such structure is the laminated HZO dielectric. In the standard 1:1 (Hf:Zr) HZO films, you alternate between hafnia and zirconia for each crystal layer. In laminated HZO, the films are instead grown with varying thickness for each oxide species. The difference between the standard HZO layer and the laminated layers is presented in Fig. 5. The laminate structure is theorized to modify the crystallization energetics during film growth in ALD. Researchers have found that the crystallization of HfO_2 into the orthorhombic phase can be realized at lower temperatures using this method [22]. Another potential benefit is the suspected emergence of a *"mixed ferroic phase"*, where the oxide show both ferroelectric and antiferroelectric properties simultaneously [22]. This has also been shown to potentially facilitate the *negative capacitance effect* in these films, which will be discussed further in section 2.4.3. While the exact reason laminated HZO improves the crystallinity of the orthorhombic phase is not known, there are several theories. A prominent explanation is that the lattice parameters of zirconia are marginally larger than those of hafnia in the orthorhombic, tetragonal, and monoclinic phase, which imparts biaxial strain in the upper layers of the thin films [21]. Theoretical models of laminated structures have also revealed interface-related kinetics. For example, growth on a tetragonal matrix (e.g., a zirconia bottom layer) is theorized to facilitate a higher maximum fraction of monoclinic crystallinity in the stack [21].

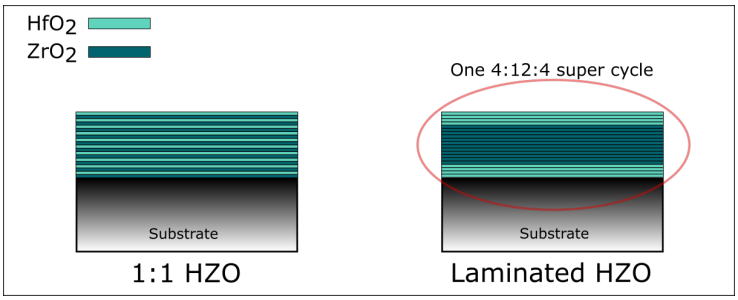


Fig. 5: The left oxide stack depicts a conventional deposition of 1:1 HZO, also known as solid-solution HZO. The right stack depicts laminated HZO where hafnia and zirconia are grown for several layers each. The encircled laminate is for example the 4:12:4 (Hf:Zr:Hf) structure which consists of a total 20 oxide layers. One "layer" of these laminates are in this project referred to as a supercycle.

2.4 Applications

There are several technological drives that motivate the research of ferroelectric HZO. In this section, some current and future applications of ferroelectric thin films are presented and motivated. This entire section is not necessary for a general understanding of the results, and if the reader is not interested, I suggest only reading the subsection labeled "Memory Technology".

2.4.1 Memory Technology

Humans are quickly increasing the amount of data we collect, both about ourselves and nature. While processing speeds have increased exponentially over the last couple of decades, as scaling has reached the atomic scale, our ability to move and store data has not kept up at the same rate. This is especially troublesome for von Neumann architectures, where the data and processing power are kept at separate locations (this is true for essentially all modern computer hardware) [23]. This gives rise to the von-Neumann bottleneck, as handling the data becomes limited by the transfer of data from memory to the processor [23]. Implementing in-memory computation where the actual memory module performs the calculation can mitigate this problem drastically and boost the performance up to 100 times [23]. In this section, the implementation of ferroelectrics as memory modules suitable for in-memory computation is discussed.

The retention of charge states at zero bias that ferroelectric thin films can offer has allowed them to become a leading contender for the future of solid state memory. This is because the polarization states can be used for bit representation. Several different device concepts are currently being researched for both more conventional memory modules, as well as for more exotic implementations such as in-memory computation as mentioned earlier. The most developed of these technologies is probably the Ferroelectric Random Access Memory, *FRAM*, which consists of a regular Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) that controls the current to and from a ferroelectric capacitor. An example of how a state-of-the-art FRAM device is constructed can be found in [6]. If the ferroelectric capacitor is set to an initial polarization state, a readout with an applied bias will either switch that state, resulting in a change in current as the charge is moved, or nothing will happen. This is a destructive read which means the state has to be rewritten if the polarization is switched. Another problem with these devices is that scaled devices require a high coercive field that degrades the endurance [6]. There have been several commercial devices which implement this technology and a notable example is the implementation as a 32-kBit memory in PlayStation 2 (perovskite based) [24].

Another device is the Ferroelectric FET, the *FeFET*, which can be constructed in the regular MOSFET structure, but with the dielectric replaced by a ferroelectric thin film such as HZO (see Fig. 6). This operates on the basis that the state of the remanent polarization in the ferroelectric insulator will modify the threshold voltage due to the difference in capacitance between the states [25]. A large bias applied to the gate will set the ferroelectric to a desired polarization state and corresponds to a write operation. This set state will generate an electric field that affects the channel depending on the direction of the polarization. For example, in a n-channel MOS (NMOS) a negative polarization will cause electrons to attract towards the channel since this is the direction of the added field, thus lowering the threshold voltage. The opposite will occur if the polarization state is reversed, increasing the threshold [25]. By applying a voltage (below the coercive field) to the gate that does not affect the ferroelectric state, it is possible to read the state non-destructively since the current read-out will depend on the threshold voltage. A large problem with these devices is that they are integrated in Metal-Insulator-Semiconductor (MIS) structures, which in turn means that they will suffer from a depolarization field. This is an effect that arises from the fact that the gate metal can supply enough charge to compensate for the polarization charge at its interface, while the semiconductor cannot compensate for it on the other side. This will lead to a field that opposes the field caused by the polarization of the ferroelectric, thus lowering the difference between high/low threshold states, which in turn lowers retention of the memory state (meaning it cannot store information for as long). This means the memory window (MW) in Fig 6 decreases.

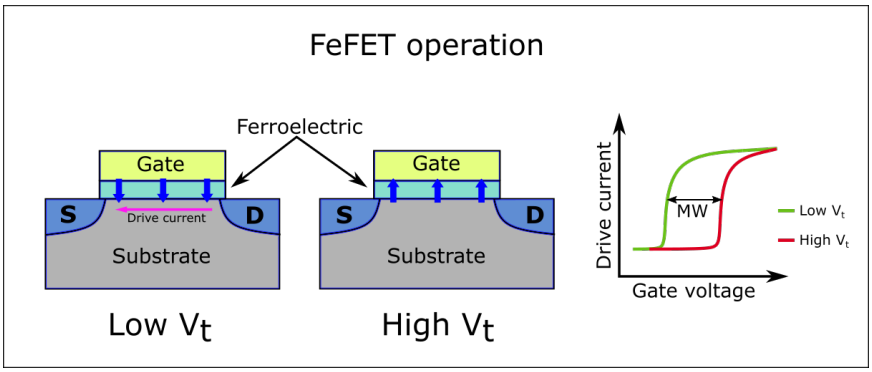


Fig. 6: A FeFET in the traditional planar n-MOS design. The polarization state is indicated by blue arrows in the ferroelectric oxide, and the corresponding IV characteristics is plotted in the graph to the right. This illustration was inspired by a figure from [26].

An emerging memory device that does not require a transistor is the Ferroelectric Tunnel Junctions, *FTJs* as depicted in Fig. 7. These are quite simple devices, consisting only of either a Metal-Insulator-Metal (MIM)- or Metal-Insulator-Semiconductor (MIS)-junction with a ferroelectric insulator. The principle of the MIM FTJ is that one uses two different metals that have different work functions. Due to an effect called *tunneling electroresistance* (TER), the resistance through the junction depends on how the band structure is modified as you switch between the two polarization states [25]. In simple terms one state will result in a higher energy barrier (for example Φ_2 in Fig. 7) for the electrons, decreasing the probability of electrons passing over or through it. TER is usually given as the R_{off}/R_{on} ratio of the device. MIS FTJs also exist, which is an attractive alternative to MIM based devices since they can offer higher on/off ratios, but similar to FeFETs these can also suffer from depolarization fields [6].

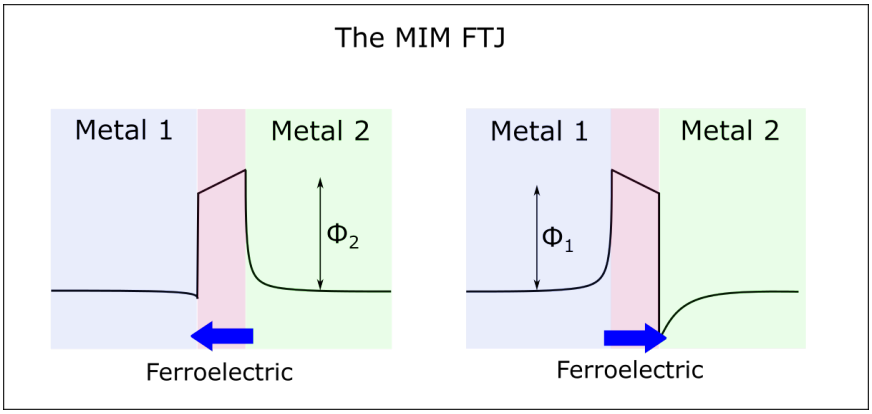


Fig. 7: The basic construction and band diagram of a MIM FTJ. The two metals should exhibit different work functions in order to facilitate a barrier height difference indicated by Φ_1 and Φ_2. The arrow points in the field direction of the set polarization state. This illustration was inspired by a figure from [6].

2.4.2 Neuromorphic Networks

The idea behind neuromorphic computing is to create a network that can learn to perform tasks similarly to how biological brains operate [27]. In brief, the brain learns by modifying the strength of the connections (synapses) between neurons (a type of brain cell). By designing neurons and synapses using ultrafast devices that are scaled to feature sizes in nanometers, researchers hope to create machines that can learn faster and more efficiently than humans. Neuromorphic circuits have already been created that outperform conventional computers (with "in-software" learning) in both speed and energy efficiency for specific tasks [27]. Since ferroelectric materials integrated in various devices such as FeFETs and FTJs have all been shown to exhibit multilevel switching, these are prime candidates for synapse implementation in neuromorphic networks [28]. Multilevel switching means some of the domains of the ferroelectric are switched below the coercive field. Similar to how the biological neuron-synapse-neuron connection operates in the brain, you want to use voltage pulses to gradually change how strong the synapse connections between specific "hardware neurons" are. The discrete domains of the ferroelectric material are thus set to several different polarization states because of these pulses. The ferroelectric then acts as a *memristor*, where the resistance, and thus the strength of the synapse, is changed gradually. Since these devices are also nonvolatile, meaning the polarization state remains for beneficial timescales (months to years), the learning is retained without having to refresh the state, which would cost more energy [28]. Neuron implementation of ferroelectric devices has also been fabricated and relies on the partial polarization effect [28]. The ferroelectric neuron can operate as an integrator if the voltage pulses can cause polarization to accumulate in the film, while it is not switched entirely.

2.4.3 Beyond-Boltzmann Transistors

Modern transistors have entered a new era of scaling where not only the feature sizes of devices are scaled to their limits, but also alternative geometries and materials are being considered [2]. One such improvement is to lower the so-called Boltzmann barrier, which is the lowest subthreshold swing a transistor can achieve at room temperature. The subthreshold swing, often abbreviated SS, is the gate bias that changes the current density of the channel by one order of magnitude (units of mV/dec) and can for conventional transistors get as low as 60 mV/dec. This limit arises from the Boltzmann distribution of charge carriers at the source and drain contact [2]. Going below this limit has the direct implication of reduced voltage in transistors, and thus less power dissipation which is both a power saving and performance boost. The subthreshold swing can be expressed as [29]

$$SS = \underbrace{\frac{\partial V_g}{\partial \Psi_s}}_{\text{bodyfactor}} \frac{\partial \Psi_s}{\partial \log_{10} I}, \tag{3}$$

where the bodyfactor relates the change in surface potential (Ψ_s) at the insulator-semiconductor interface to the gate voltage (V_g) and can thus be written as if the voltage is divided between the capacitance supplied by the two materials (C_s from the semiconductor and C_i from the insulator)

$$\frac{\partial V_g}{\partial \Psi_s} = 1 + \frac{C_s}{C_i}. \tag{4}$$

The second term in equation 3 can be shown to be 60 mV/dec at room temperature, which means the optimal SS is achieved when the bodyfactor$\rightarrow$1, which is almost true for high-k insulators where C_i is typically large [29]. To push SS below the limit of 60 mv/dec, the bodyfactor must be reduced below one which is possible if either C_i or C_s can be negative. Since capacitance indicates how charges move as a response to a certain bias, it is not entirely intuitive to ponder the concept of negative capacitance as it would indicate a decrease in charge carriers for bias with the opposite sign [30]. However, for a regular parallel plate capacitor one can write [30]

$$C = \underbrace{\frac{dD}{dE}}_{\varepsilon_0 \varepsilon_r} \frac{A}{t}, \tag{5}$$

where the change in charge displacement D as a function of the electric field E equals the permittivity of the insulator. A and t indicate the area and thickness of the capacitor respectively. This means that for a material that expresses negative permittivity, one can construct a negative capacitance. In dielectrics that exhibits non-linear behaviour, such as a ferroelectric material, one finds that the polarization P is not linear with the electric field and since D is proportional to P you will have negative capacitance when

$$\varepsilon_r \propto \frac{dP}{dE} < 0. \tag{6}$$

This is equivalent to the state resting at the local maximum in the Landau-model described earlier in section 2.2, and illustrated in the free energy landscape of Fig. 2. Due to the polarization's relation to free energy, a negative slope in the P-E curve is thus unstable. This transition would occur between the top-left and bottom-right corners in Fig. 1. The negative capacitance transition can however be shown to be stable if the ferroelectric is integrated with a sufficiently thick (regular) dielectric in series. A detailed explanation of this can be found in [30]. This is a concept that has grown in popularity during the last decade and experimental evidence of this effect has been demonstrated in perovskites already in 2011 [31]. In order to realize true transistors beyond the Boltzmann barrier this technology still has several hurdles to cross such as CMOS integration and thermal stability in the Si process [30]. Several of these problems can potentially be addressed with laminated HZO explored in this thesis, as it has displayed very promising results in scaled systems. In a preprint from a research group at *Berkeley University* ultra-thin films of laminated zirconium doped hafnia was shown to exhibit negative capacitance effects when integrated with Si [22]. They measured a capacitance that would indicate a thinner oxide than what was observed using transmission electron microscopy.

3 Processing techniques

The study of ferroelectric thin films is made possible through nanoprocessing. Advanced tools which facilitate the fabrication of oxides and contact metals with nanometer-size precision are needed. In this section, the processing tools and techniques used to fabricate MOSCAPs for the study of ferroelectric HZO are described. If you are already familiarized with these methods, you can skip ahead to section 4.

3.1 Atomic Layer Deposition

The requirement for the implementation of ferroelectric films made from HZO is that they are both thin and possess the desired composition. To achieve monoatomic control over the fabrication of such films, it is often most beneficial to process the oxides using Atomic Layer Deposition (ALD). ALD belongs to a family of nano-processes known as Chemical Vapour Deposition (CVD) techniques [32]. Regular CVD processes are based on the principle of injecting all chemicals that will constitute the thin film into a reaction chamber and allowing them to undergo chemical reactions on the surface of the sample to form the desired thin film. ALD on the other hand, acts in a more self-limiting fashion. While the chemical reactions still occur at the surface, only one precursor (reactant) is injected into the chamber and these are designed in a manner that only allows for one monoatomic layer to form at once, saturating the surface (for certain process parameters) [32]. The process can be designed in several ways to deposit a plethora of different thin films at varying temperatures, pressures, and other process parameters. To get a better understanding of the basic process, let us consider how Al_2O_3 (alumina) would be deposited on a pre-oxidized substrate [32]. This is illustrated rather than HZO deposition because its ALD mechanism is more complicated and not fully understood [33]. The following steps are also illustrated in Fig. 8, inspired by a figure from [32];

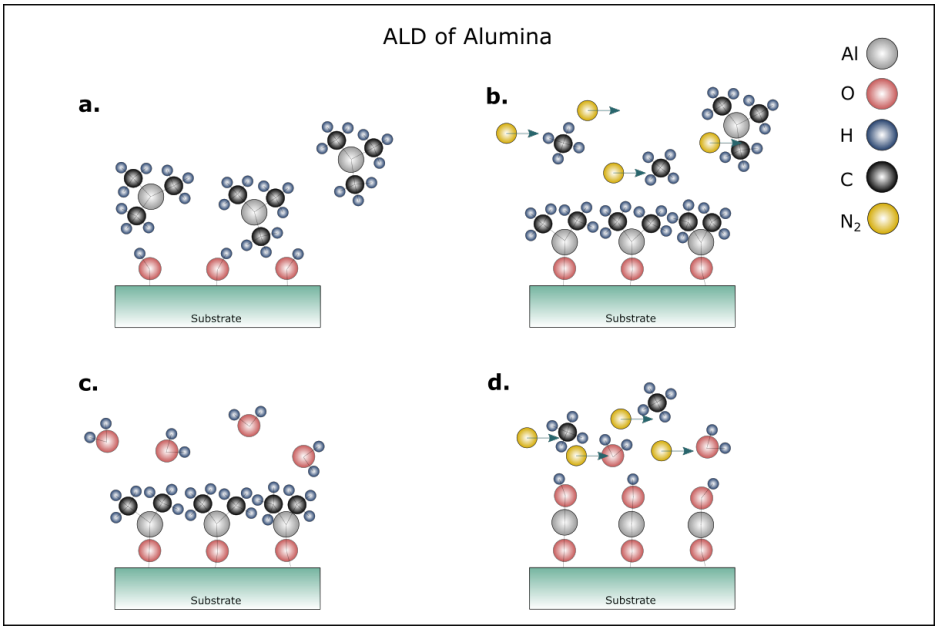


Fig. 8: The ALD growth of alumina on a pre-oxidized substrate. These steps are repeated in order to grow further layers. This figure is inspired by a similar figure from [32].

a. A heated Si substrate surface is exposed to an organometalic compound abbreviated TMA (trimethylaluminium) that reacts with a native hydroxide layer.

b. The ALD chamber is purged by flushing it with a carrier gas (usually nitrogen gas), that carries away byproduct methane and any remaining TMA precursor.

c. Now the surface needs to be oxidized in order to facilitate growth of the next layer. This is done by using water as a precursor, that will replace the methyl groups left at the surface.

d. Following this, the reaction space is once again purged with a carrier gas. In order to grow another layer, the steps a-d are repeated.

All of this is performed in a special reactor designed for the ALD process (see Fig. 9). The reactor comes with a vacuum system, a sample holder, as well as several heaters and valves that are fitted with thermometers and pressure gauges. To optimize the quality of the film, the ALD processing machine allows you to modify several different process parameters. Some of the most important ones are the chamber temperature, pressure, and flow rates of precursors as well as the pulse and purge times of the precursors and their byproducts. In this thesis, the pulse sequence and chamber temperature will be the main parameters that are modified. The temperature is an especially important parameter and a *temperature window* is usually defined, which is the range of temperatures where the ALD reaction is entirely self-limiting, as illustrated in Fig. 8 [32]. This means the entire surface is covered in a monolayer of the desired film after each growth cycle. When the temperature is too low, there might not be enough thermal energy to facilitate the surface reactions, or if too high, it might lead to decomposition of precursors and undesired/terminated growth. This might be the case for the Zr precursor used in this thesis, Tetrakis(ethylmethylamino)zirconium (TEMA-Zr), for temperatures exceeding 250 °C [34]. No evidence of this degradation was found in literature for the Hf precursor used, which was Tetrakis(dimethylamino)hafnium (TDMA-Hf).

The chamber illustrated in Fig. 9 is a thermal ALD of the Picosun Sunale R100 series which was used in this project. In thermal ALD, as the name suggests, the energy that facilitates the surface reaction is provided through a heating element. Another feature is that the oxidizing agent most common in thermal ALD is either H_2O or ozone gas [35]. A contender to thermal ALD for the fabrication of ferroelectric thin films (often found in literature) is the plasma-enhanced ALD (PEALD), which is argued to provide a higher oxidation rate by adopting a O_2 plasma as the oxidizing agent [35]. The argument for using PEALD rather than thermal ALD for ferroelectrics is that it would facilitate better crystallinity in the HZO due to higher surface reaction energies, which in turn would allow for a lower temperature during the post-metallization anneal [20], [35]. While there are some research that demonstrates the advantages of PEALD over thermal-ALD [20], the difference is not massive, and comparable performance has been achieved using thermal-ALD systems similar to this thesis [4].

Also worth considering is the high interface-trap density that is native to the oxide at InAs surface [33]. In order to reduce the effect of the sub-optimal surface, a HCl wet-etch can be performed on each sample before ALD of HZO, which removes the oxide. If the samples have minimal exposure to air following this, it is believed to result in a more well defined interface for ALD growth [33]. The importance of the interface is not only related to the growth of the oxide, but it is also believed that if integrated on a transistor platform, the quality will dictate the electronic properties of the entire gate stack [36].

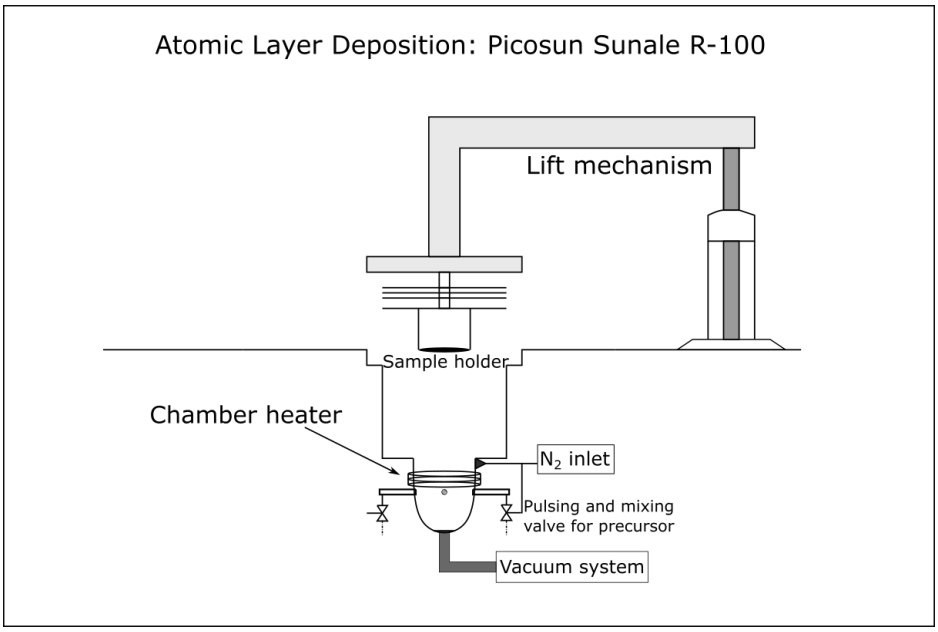


Fig. 9: This figure depicts a sketch of the Picosun sunale R-100 ALD reactor used in this project. It is a thermal ALD and is located in a glove box cluster in LNL, which contains a nitrogen atmosphere to minimize moisture from entering the reaction space.

3.2 Sputtering

A critical step in the fabrication of thin film ferroelectrics based on HZO is the deposition of a suitable top metal to facilitate the strain-induced formation of the desired o-phase in the oxide during the post-metallization anneal [37]. This is performed using a physical vapor deposition (PVD) technique. PVD is characterized by the transformation of condensed matter to a vapor phase, which deposits on the surface to form a thin film. The method used to accomplish this defines two main classifications of PVD: sputtering and evaporation processes. Evaporation will be elaborated on later while this section focuses on sputtering. Sputtering involves the deposition of thin films by ion bombardment of a target [38]. The ions are accelerated onto the target material and knock out the atoms that then impart onto the sample, usually positioned facing the target, to form a thin film. The general chamber layout is illustrated in Fig. 10.

There are a myriad of different chamber, target and plasma source designs that are used in modern sputtering systems. The sputtering system used in this thesis work adopts magnetrons to generate an Ar plasma. The AJA sputtering system in Lund Nano Lab (LNL) offers both RF and DC based magnetron guns depending on the metal you want to deposit, but TiN is deposited using a RF source. In Fig. 10, the bottom part contains the RF magnetron (at the bottom of the target container) that generates the plasma used for the sputtering. A field is applied between the cathode (located at the sample holder) and the anode (located underneath the target material) that accelerates electrons in the lateral direction. Magnets that are located below the cathode cause a Lorentz force that bends the electrons into a trajectory towards the target that rests on the cathode. These electrons are not sufficient to knock away any target atoms, which is why argon gas is pumped into the vacuum chamber. When Ar atoms come into contact with high energy electrons, they are ionized and an ion-rich plasma forms close to the target surface. Argon ions carry enough energy to sputter the target material that is thereupon ejected towards the sample and deposited as a thin film. The entire sample stage rotates continuously during deposition to ensure even film distribution. A separate quartz crystal acts as a thickness monitor. This operates on the principle that the resonance frequency of the crystal changes as material is deposited on it, from which the thickness can be extrapolated. This also means the thickness monitor has to be programmed regarding material density, acoustic impedance, and tooling factor, which accounts for the tilt and relative position of the target.

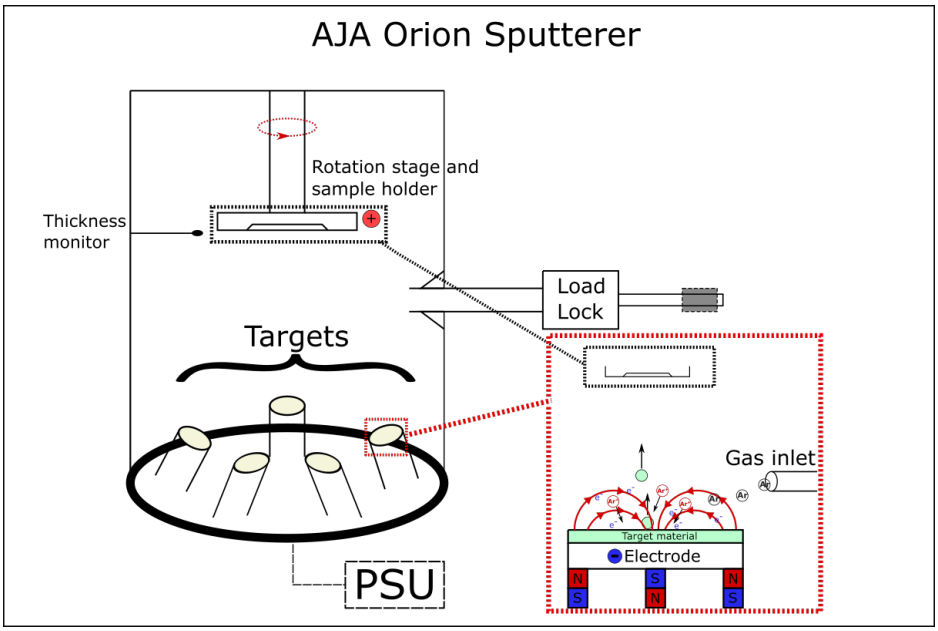


Fig. 10: A depiction of the AJA Orion 5 magnetron based sputterer in the LNL nano-process lab. Figure partially inspired by [39].

The reason TiN is deposited on top of the oxide is related to the crystallization of the HfO_2 from the tetragonal (t-)/amorphous phase into the orthorhombic (o-) phase with the correct space group as described before in section 2.3.2 [9]. Results from CV-measurements seem to indicate that the stress induced from the top-metal capping is critical for any ferroelectric phases to appear following post-metallization thermal treatment, using rapid thermal processing, which is discussed in the next section. The reason TiN is sputtered rather than evaporated, which in theory yields a higher quality film, is that the process parameters can be optimized to ensure the metal crystallizes into TiN(111) [37]. This is desired because the TiN(111) structure puts a tensile stress on the underlying oxide up to 1.4 GPa that assists the crystallization [37].

3.3 Thermal Processing

Rapid thermal processing (RTP) is a processing technique commonly used in the semiconductor industry as a means to facilitate the diffusion of dopants or oxidation of surfaces [40]. The idea is to first heat the sample rapidly to high temperatures, and then allow it cool for an extended amount of time to avoid breaking the wafer due to thermal shock. RTP performed at LNL uses high powered IR lamps which can heat the sample to 1000 °C in a few seconds. When studying ferroelectric thin films based on HfO_2, the thermal process that enables the o-phase crystallinity is the post-metallization anneal (PMA). This is, as previously discussed, performed after the metal capping of the film to induce tensile strain in the oxide.

However, a major problem of using HfO_2 is its rather high crystallization temperature in the region of 600-800 °C [41] from the amorphous phase. This can prevent the integration of these ferroelectrics in the back-end of the line (BEOL) on semiconductor platforms that cannot withstand such high temperatures. BEOL in the semiconductor hardware industry refers to everything that occurs on top of, and after the initial fabrication of devices directly on the wafer, such as wiring. A promising temperature-sensitive material is InAs, which exhibits great electronic properties, but is degraded by high temperature RTP [4], [5]. However, the addition of Zr dopants into the oxide has been shown to reduce the crystallization temperature of the orthorhombic phase due to ZrO_2 exhibiting a lower crystallization temperature itself [42]. The addition of Zr dopants during growth of the film has resulted in ferroelectricity being found in oxides annealed at temperatures in the 300-400 °C range [4], [20], [35].

3.4 Evaporation

Similar to sputtering as detailed before, the evaporation technique is a form of PVD process where the material is evaporated or sublimed into vapour and deposited as a thin film. This method differs from sputtering since in the evaporation process the target[5] itself is heated, as opposed to sputtering where the target is bombarded with high energy ions [43]. Evaporation in general has several advantages over sputtering such as offering higher deposition rates and being able to maintain a better vacuum during the process (which in turn leads to cleaner films). Evaporation targets can either be in the liquid or solid phase and this usually depends on the vapour pressure of the material in question. For example, the evaporation of Ti can be done from the solid phase well below its melting temperature. [43][6].

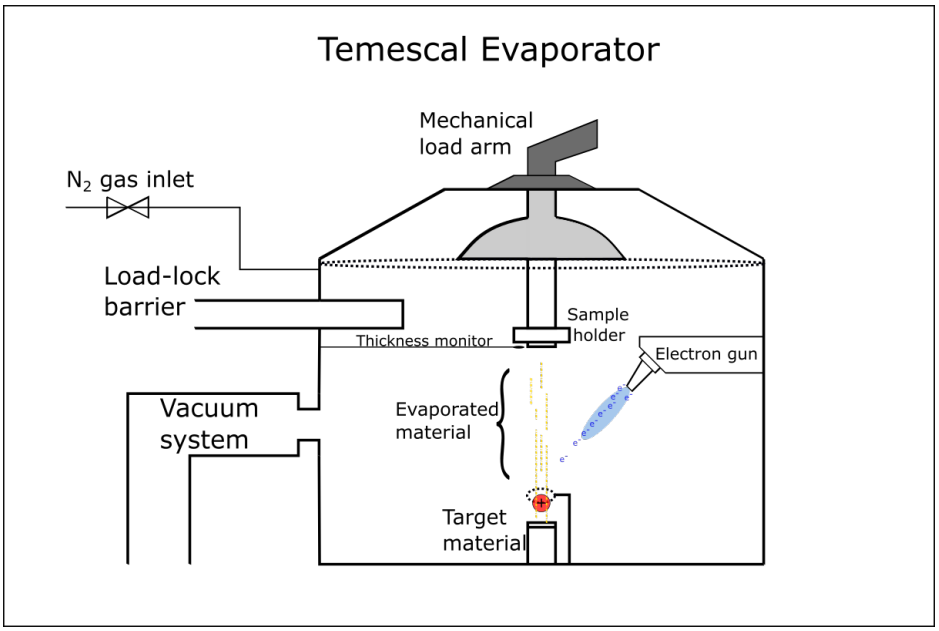


Fig. 11: An illustration of the Temescal E-beam evaporator in the LNL nano-process lab.

A depiction of an evaporation setup can be seen in Fig. 11 which is based on the tool used at LNL. The source material that should be evaporated is placed in a holder at the bottom that is usually of the metal "boat" type (metal sheet with a pocket for material) or a wire in a helical or cone shape [43]. The source can be heated in several different ways; one of which is resistance heating where a current is run through the target holders (which are typically made of tungsten that is stable at high temperatures) [43]. The evaporator used in this thesis is the Temescal E-beam evaporator which as the name implies uses an electron beam to heat the target. This heating system provides several advantages over a traditional resistance-based heater such as cleaner deposits and faster deposition rates for sources with high melting points [43]. The electrons are accelerated to the target and the transferred energy subsequently evaporates the atoms in the target that travel upwards and deposits on the surface of the sample. In e-beam evaporation systems, the electron source is partially isolated from the sample to further reduce contamination, and the electron beam is often guided with a magnet in a 270° arc to the surface of the target [43]. This is also the case in the Temescal e-beam evaporator used in this project, but for simplicity Fig. 11 illustrates an electron gun set-up instead. Samples are loaded using a mechanical arm into a load-lock compartment that can be isolated from the rest of the vacuum in the machine to reduce pump-down time. The sample can be mounted in several different holders, which allows different sample sizes as well as masks to be incorporated in the

[5] This can also be referred to as the "source".

[6] A rule of thumb is that melts of material are not needed if the vapor pressure is greater than 10^{-3} Torr ≈ 0.133 Pa at the melting temperature of the material [43].

process. The thickness of the film is kept track of using a monitor next to the sample in a similar manner to what was described previously for the sputtering system.

3.5 UV lithography

The modern semiconductor industry relies on fabrication processes that have both high resolution and high throughput, and the most prominent of these is UV lithography (UVL). UVL is a "top-down" method that uses short-wavelength light to transfer patterns from a "mask" onto a sample located underneath [44]. In the most basic of cases, the process is performed accordingly:

1. The sample is coated in a liquid polymer called a resist that is in some manner sensitive to UV radiation.
2. The sample, now coated in resist, is baked in order to dry the resist on the surface.
3. The actual lithography is performed in a tool called "mask-aligner", where, as the name implies a mask containing the pattern you want on the sample (or the negative of it) is present. Once aligned you illuminate the surface through the mask with a UV lamp.
4. Following exposure, the resist on the sample is developed, where either the pattern projected trough the mask onto the surface or the negative of it is etched away.

Spin coating is the most common method of applying the resist to the sample surface. After the sample is cleaned, it is placed on a small rotating platform and held in place by a vacuum coming from underneath. By adding a small amount of liquid resist on top of the sample and turning on the spinner the resist is evenly distributed across the surface[7]. Following this, the sample is soft-baked, and the resist is thus both liberated from any remnant moisture and the polymer also sticks better to the surface [44]. There are a myriad of different types of resists with differing properties. Most UV-resists can be split into two different camps: positive and negative resists. As an example, the resist used in this project was ma-N 440 which is a negative resist (it belongs to the 400 series and leaves behind four μm resist after spin coating) [46]. When a negative resist is exposed to UV radiation, the solubility of the exposed polymer is decreased drastically [44]. This is because negative resists are designed by mixing a polymer with a chemical sensitive to UV light. The chemical will act as a catalyst that is initiated after being exposed to the light and will in turn cause polymers to cross-link. The larger the polymers get, the less soluble they become while the areas not exposed to UV radiation will still retain its initial solubility [44]. A positive resist would work in the opposite manner and uses a slightly different mechanism that would cause it to become more soluble after exposure [44].

[7] A great demonstration of this can be found at [45].

4 MOSCAP Processing

In this section, the fabrication of the metal-oxide-semiconductor capacitors (MOSCAPs) used to characterize the HZO oxide will be detailed. This process has been developed and optimized over several years by researchers and previous master thesis students in the nanoelectronics group at the Department of Electrical and Information Technology, LTH. In Fig. 12, all the major steps of the process flow that will be discussed in this section are illustrated.

Throughout this project, the substrate that the MOSCAPs are fabricated upon consisted of a Si base substrate which had 300 nm of InAs epilayer grown on top, using Metal-Organic Vapour Phase Epitaxy (MOVPE) in the (111) crystal orientation. Since these samples were believed to have a rather low-quality surface, they were first subjected to a cleaning regime that started with a standard acetone and IPA rinse to remove organic residues from the surface. Following this, any microscopic organic remains were eliminated during a plasma treatment in a PlasmaPreen asher for 60 seconds. The oxide was wet etched in HCl (37%) diluted with deionized water (diluted by adding 1 part acid and 10 parts water to a beaker) for 15 seconds at room temperature (RT)[8]. Afterwards, the samples were placed in a UVOH 150 ozone cleaner to re-oxidize the surface for 10 minutes at 50 °C. This process was repeated twice more. Now the samples were ready for ALD of the oxide. This was preceded by one last HCl wet etch before the samples were quickly put in the PicoSun ALD vacuum chamber to minimize the native reoxidation of the surface. Since both the sample temperature and precursor pulsing sequence are varied between and within the different MOSCAP series produced in this thesis, they are reported in section 6.1 in greater detail. In table 1 the ALD parameters kept constant throughout all processing can be found. The metalorganic precursors used in this thesis for the deposition of HfO_2 and ZrO_2 are, as mentioned previously, TDMA-Hf and TEMA-Zr respectively. Since the oxide was deposited at significantly higher temperatures (275-325 °C) than normal (200°C), the samples had to spend considerably more time in the chamber than a normal deposition. This was required for the chamber temperature to reach the set value and stabilize. This problem is related to an underperforming control system in the ALD. After the oxide had been grown for the set cycles, the thickness was evaluated using ellipsometry with a Woollam RC2 ellipsometer. The thickness was evaluated at three different coordinates on the sample to get more data for statistic evaluation.

Before deposition of the top metal, the sample was quickly blown with a nitrogen gun to remove any potential macroscopic dirt (such as paper fiber from clean room wipes) from the surface. The TiN top metal was sputtered in the AJA Orion 5 sputterer, and the deposition took approximately ten minutes. Meanwhile, the thickness was monitored continuously such that the deposition could be canceled when it reached 10 nm. Following this, the samples are customarily subjected to PMA using RTP, however, since this thesis focuses on as-deposited ferroelectricity, this was not performed at that point. Instead, the samples were prepared for UV lithography by first performing a standard cleaning with acetone and IPA to remove any organic residue, followed by sample dehydration on a hot plate at 150 °C for ten minutes to ensure there is no moisture left on the surface. Afterwards, the samples were immediately spin-coated with ma-N 440 resist for 45s at 6000 revolutions per minute. Once removed from the spinner, the samples are put on a hot plate to bake the resist at 95 °C for three minutes. Now the samples could be exposed to UV light through a mask that defines the negative projection of the contact of the capacitors. This was performed using a MJB4 Karl Süss mask aligner. The sample was put into hard contact with the mask and exposed for 50 seconds after a 5 second stabilization time. This step defined the shape of the contacts on the MOSCAPs. A top view of these can be found in the bottom right of Fig. 12. All devices characterized consisted of the inner circle with radius r. The mask was patterned with hundreds of devices with varying radii which could be fabricated simultaneously.

Once the resist had been exposed to UV light through the mask, all exposed parts of the resist were soluble in the associated developer ma-D 532/S. The samples were stirred in the developer for 105 seconds each at a frequency of one Hz, followed by a deionized water rinse for 60 seconds. To remove any remaining resist, the samples were descumed[9] for 30 seconds while being covered with a Faraday cage to increase the isotropicity of the plasma etch. The contacts were formed by evaporating five nm of Ti followed by 200 nm of Au in a Temescal electron-beam assisted

[8] Any further mentions of HCl wet etch in this report has been performed this way

[9] This refers to removing residual contaminants such as a resist.

Table 1: The recipe optimized for growth of HZO in the Picosun Sunale R-100 thermal ALD. The higher the chamber temperature, the longer stabilization time is required.

Parameter	Standard Recipe	In this project
General		
Chamber temperature [°C]	200	250-325
Stabilization time [min]	4	30-60
Intermediate space flow [sccm]	350	350
Number of reactor flushes	3	3
Precursor settings		
Zr source temperature [°C]	110	110
Zr pulse time [s]	1.6	1.6
Zr purge time [s]	5.0	5.0
Hf source temperature [°C]	100	100
Hf pulse time [s]	1.6	1.6
Hf purge time [s]	5.0	5.0
H_2O source temperature [°C]	-	-
H_2O pulse time [s]	0.1	0.1
H_2O purge time [s]	10.0	10.0

evaporator. Now the metal deposited on the resist could be removed in a lift-off process. This involved putting the samples in acetone and dissolving the polymer, but could require some mechanical assistance by blowing on the surface with a pipette. The last process step involved removing the TiN that covered the area between the contacts. This was done through an acid-wet etch using an ammonia-peroxide mixture (APM) which was heated to 60 °C. The samples were submerged for 30 seconds each and could afterwards be measured and characterized.

Most samples fabricated in this project followed the details above, but three samples deviated from this process slightly. One sample (Fig. 13**a**) in the first series (M1) was fabricated on a n-doped InAd substrate rather than the usual InAs epilayer on Si. This surface was also cut along the (100) crystal plane rather than the (111)-plane of the epitaxially grown samples. In series M3 two samples were slightly different compared to the process described in this section. One sample (Fig. 13**b**) was constructed as a metal-insulator-metal (MIM) directly on a Si substrate, meaning a TiN layer had been sputtered on the bottom substrate. The other one (Fig. 13**c**) was identical to the standard process, except for a 6 ALD cycle interface layer of Al_2O_3 towards the oxide.

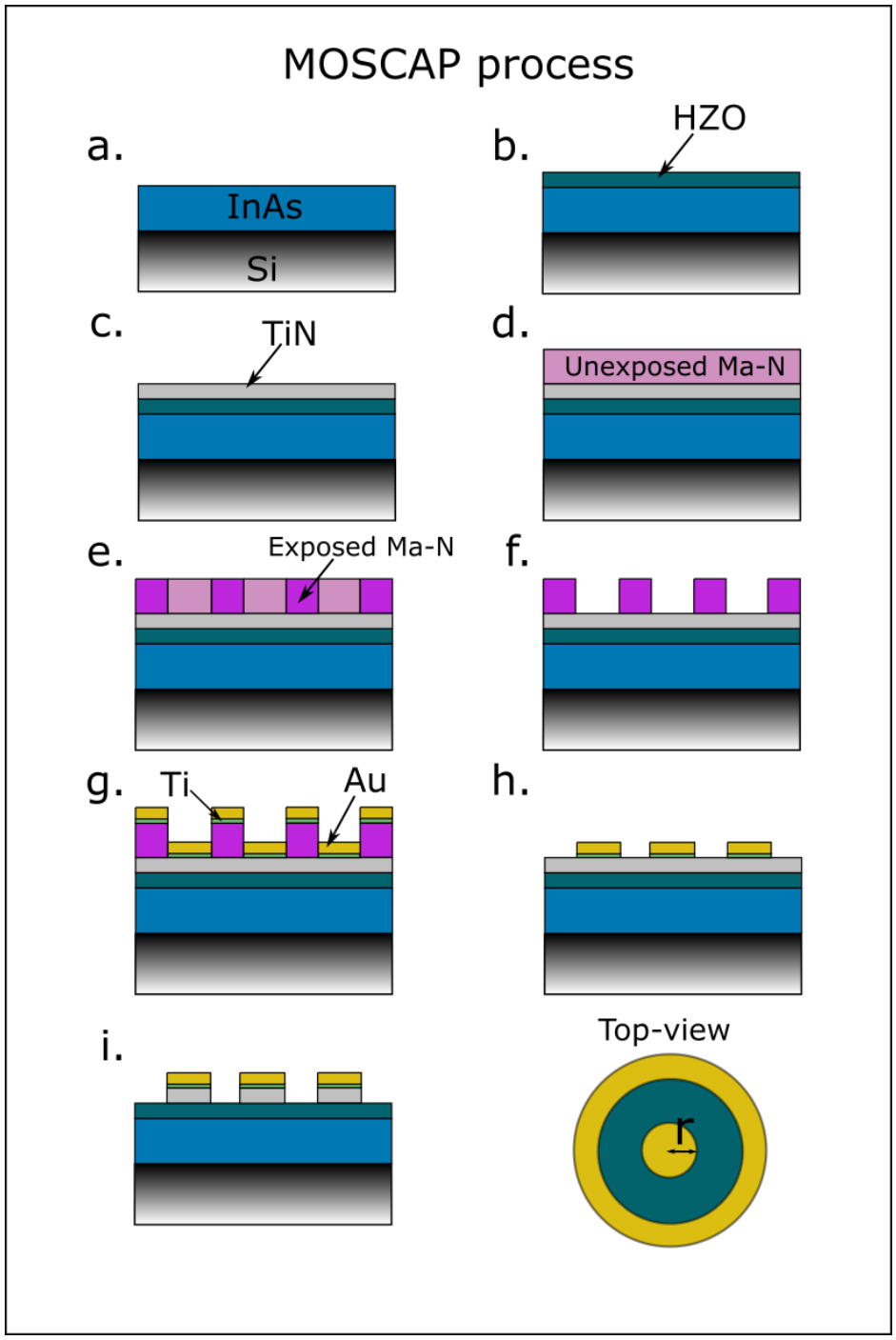


Fig. 12: This figure depicts the major steps in the fabrication of a single MOSCAP in this project. **a.** Most of the samples fabricated will start as Si with InAs deposited on top. **b.** HZO is grown using ALD and **c.** TiN is sputtered on top. Following this the sample is **d.** spin-coated with Ma-N 440 resist and **e.** exposed to UV-light through a photomask. **f.** The resist is developed using Ma-D and **g.** the Ti/Au contacts are evaporated onto the sample. **h.** Acetone lift-off reveals TiN which is subsequently **i.** etched using APM. A top-view of a device can also be observed in the figure.

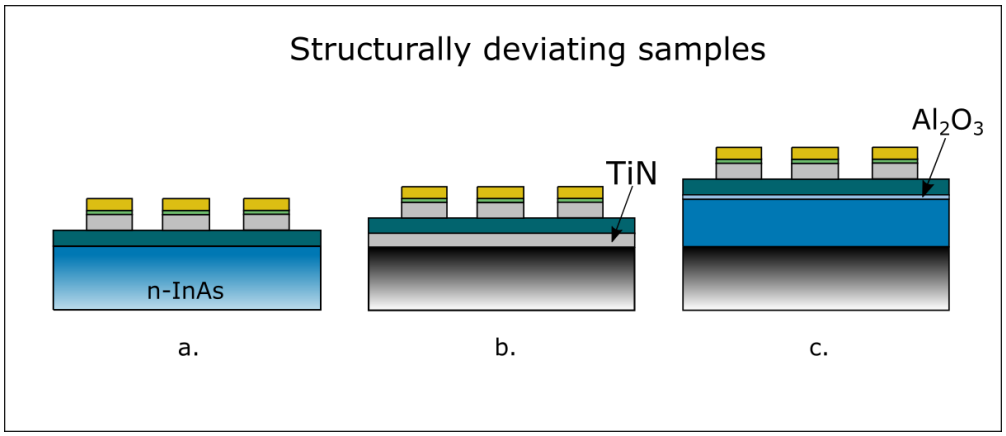


Fig. 13: This figure illustrates the samples deviating from the otherwise general structure depicted in Fig. 12. **a.** A sample fabricated on n-doped InAs substrate in series M1 (id: 275_nInAs). **b.** A sample constructed with metal-insulator-metal devices on Si in series M3 (id: 7L4i(MIM)). **c.** This sample was prepared according to the fabrication scheme in Fig. 12, but with 6 cycles of Al_2O_3 grown using ALD before the HZO at 300°C (without removing the sample). It is contained in series M3 (id: 7L6Ali).

5 Measurement Techniques

Once fabricated, the thin films of ferroelectric HZO require characterization to determine leakage, thickness, remanent polarization, and other properties that are relevant for further research. This can be done using the methods detailed in this section.

5.1 Ellipsometry

Ellipsometry is an indirect characterization method where elliptically polarized light that has been reflected after hitting a sample is analyzed, and a model that contains information about the sample is fitted to the acquired data [47]. A basic illustration of an ellipsometer can be found in Fig. 14. This builds on the principle that the polarization state of the light will change after the light is reflected or transmitted through some material. The light exiting the polarizer in Fig. 14 will be polarized in two different orientations in relation to the sample. There is p-polarized light, which has an electric field component oscillating perpendicular to the surface of the sample, and s-polarized light oscillating parallel to the surface of the sample. These two polarization states have different field amplitudes, which is why the resulting crossection of the field is shaped as an ellipse (see the ellipse in Fig. 14). Rather than simply measuring the intensity of the reflected light, the ellipsometer also uses two other parameters: Ψ which is related to the amplitude of the ratio of reflectivity between two different polarization states and Δ which is the phase difference between the polarisation states [47]. This can be illustrated in the following equation, where r_p and r_s are Fresnel reflection coefficients of the states [47].

$$\frac{r_p}{r_s} = \tan(\Psi)e^{i\Delta}. \tag{7}$$

The measured data is then compared to the data generated from a model (created in a special software) of the investigated sample [48]. This model contains information about the optical constants of the material in the sample such as refractive index and attenuation coefficient [48]. In contrast to more traditional methods that squarely rely on measuring the reflected intensity, ellipsometry offers several advantages. These are, for example, improved precision (you do not measure absolute intensity) and more data since it extracts information from two parameters (Δ and Ψ) [47]. The detector is used in conjunction with the analyzer to find the electric field amplitudes of the reflected light by measuring the relative intensity [49]. While sample models are often generated from tabulated values, they can also be obtained from a parameterized Cauchy dispersion equation, which can be used to calculate the optical constants, for example, the refractive index $n(\lambda)$ [50]

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4}, \tag{8}$$

where A, B, and C are fit parameters that modify the wavelength dependence of the refractive index. This can provide an excellent fit in the visual spectrum for transparent materials.

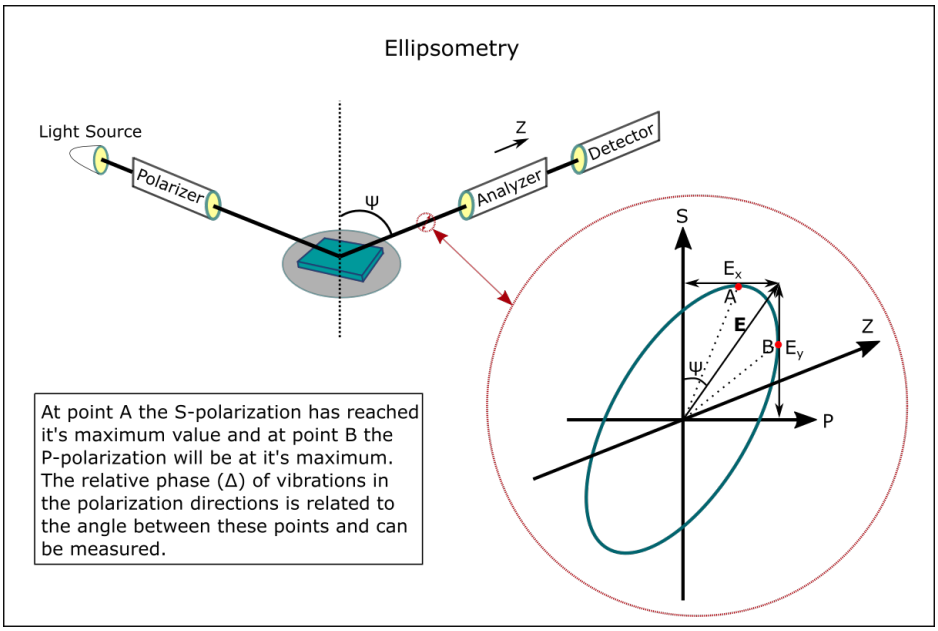


Fig. 14: This figure depicts a simple ellipsometer setup as well as a depiction of the propagating S- and P-fields. This figure was inspired by several figures from [49]. The polarizer is the optics which sets an initial ellipsometric polarization and the analyzer is used to determine the change in the polarization and can be constructed in various configurations [49].

5.2 IV-Characteristics

To characterize an oxide, simply sweeping the voltage (V) and measuring the resulting current (I) can tell a lot about the device. If the insulator is leaking through different mechanisms, this can be extrapolated from the IV-characteristics. These leakage mechanisms can for example be Fowler-Nordheim tunneling (tunneling through a triangular energy barrier) and Schottky emission (the charge carriers travel over the energy barrier of the oxide), and there are well established models that can be fitted to measured IV-curves [51]. From these fits the energy barrier and other figure of merits can be extracted [51]. These measurements can also tell you about the maximum durability of the film, known as the *breakdown voltage*, where the resistance essentially falls to ”zero” and the current goes to the set compliance. On the samples manufactured in this project the IV-characteristics is mainly used to study the quality of the oxide. The breakdown effect that causes the oxides to break is related to several different mechanisms. One such mechanism is electrostatic overstress (EOS). EOS is caused by currents in the material resulting in localized heating, which damages the thin film [52]. This is the most probable cause of breakdown in the devices produced in this project.

Using regular IV-measurements the devices can also be trialed for basic FTJ characteristics (see section 2.4.1). This is done by performing simple IV-sweeps above the coercive fields of ferroelectric samples and sweeping back to zero for both the positive and the negative direction, looking for hysteresis in the measurement. From the hysteresis the TER can be calculated.

5.3 PUND

PUND is a standard method of measuring the ferroelectric polarization of a material. Note that almost the entire description of PUND in this section is based on [53]. PUND is an acronym for Positive-Up Negative-Down and is a pulsed voltage method that uses a pulse train shaped as in Fig. 15. In the figure, the current can be observed together with the associated pulse train. Before the PUND technique it was possible to generate ferroelectric hysteresis curves, but not as sharp looking as can be seen in Fig. 1 [54]. This is because the PUND method can

remove leakage from the oxide that is unrelated to the polarization state such as that from the parasitic capacitance (trap charges) [54]. This is essentially done by pulsing twice in both bias directions.

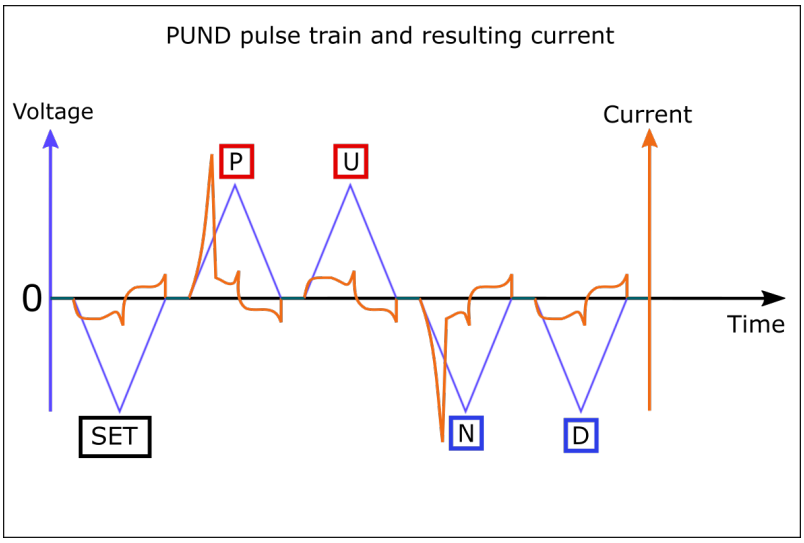


Fig. 15: This figure depicts the triangular pulse train (blue colored, left axis) that is applied across the oxide in order to determine the polarization-electric field characteristics as well as the resulting current (orange colored, right axis). This is an idealized illustration and in reality the device can, for example, have different leakage currents depending on field direction. The voltage pulses (the entire pulse train) are in this thesis project applied with a frequency of 10^3 Hz.

The first pulse labeled "SET" in Fig. 15 functions, as the name implies, by presetting a known polarization state. This is followed by a "P"-pulse that switches the state into the opposite polarization. As this pulse is applied, one can observe a high current peak in Fig. 15, which results from the charge that is moved during the switching. Following this, another pulse with the same polarity as the "P" pulse is applied, now labeled "U", but the large current peak is not observed. This is because this pulse will not switch the ferroelectric state, since it has the same polarity. Instead, it will trigger stray capacitances such as charge traps to depolarize. This current is also generated during the P-pulse, but is partly obscured by the ferroelectric switching. The difference between the currents generated by these pulses should contain only charge that were moved because of the state flip. The corresponding sequence is repeated for negative fields to characterize the second polarization state, which motivates the "N"- and "D"-pulses[10]. With the difference between these currents, the polarization can be calculated since the total charge $\mathbf{Q}$ is just the cumulative integral of the current I,

$$\mathbf{Q} = \int_0^t I(t')\, dt', \tag{9}$$

where t is the total time span of the "P"- or "N"-pulses during PUND. The charge that has been shifted corresponds to a displacement vector, $\mathbf{D}$, which for a linear dielectric in a relatively weak field, $\mathbf{E}$ can be expressed as [55]

$$\mathbf{D} \equiv \varepsilon_0 \mathbf{E} + \mathbf{P} = (1 + \chi)\varepsilon_0 \mathbf{E}. \tag{10}$$

[10]Usually the current differences (P-U and N-D) can be plotted versus the electric field resulting in I-E plots that can be found together with the P-E curves in the result. This is included since it technically is the derivative of the P-E curve, and can thus contain details that disappear when integrated.

Here the polarization **P** is linear in the external field, and modified by the electric susceptibility χ. For high-k dielectrics such as HZO the approximation **D**≈**P** can be made since the susceptibility will be quite large. Since the charge and displacement are related through the area factor (A) of the capacitor, the polarization vector can now be connected

$$\mathbf{P} = \frac{\mathbf{Q}}{A}. \tag{11}$$

The electric field across the capacitor is defined as $\mathbf{E} = \mathbf{V}/\mathrm{t}_{ox}$, where t_{ox} is the thickness of the oxide. Now the polarization-electric field curve (the *P-E curve*) can be generated by plotting how the polarization changes as the electric field is varied during the voltage pulse. This yields hysteresis curves similar to the one seen in Fig. 1. Sometimes when a PUND pulse is applied to a ferroelectric device, the results might indicate much weaker polarization then expected, or not at all, despite knowing the oxide is ferroelectric. In HZO, this is related to "pinning" of the ferroelectric domains by charge traps or other defects and the so-called wake-up effect must occur to free them [56]. This means the film is pulsed with wake-up cycles, which usually consists of fast positive and negative voltage pulses numbering in the thousands. This frees the pinned domains but can cause the fatigue effect [56], where the remanent polarization is reduced after a certain amount of wake-up. Furthermore, from the PUND measurement, a rough estimate of the relative permittivity of the oxides can be estimated. From equation 5 you can write

$$\varepsilon_r = C\frac{t}{\varepsilon_0 A}, \tag{12}$$

and a capacitive current I_c is given by the change in voltage over time, scaled by the capacitance [57],

$$I_c = C\frac{dV}{dt}. \tag{13}$$

This can now be used to estimate the permittivity since the capacitive current can be extracted from the U- and D- pulses in PUND as long as the leakage is low enough. The P- and N- pulses generally should not be used since they might contain polarization currents. It should be noted that C-V measurements are superior for accurate estimation of the relative permittivity. As a final note both the IV-characterization and pulsed measurements using the PUND technique were performed using an MPI TS2000-SE semi-automatic probe station equipped with a Keysight B1500A Parameter Analyser. The B1500A can perform pulsed measurements due to the addition of a B1530 waveform generator.

5.4 CV-measurements and GIXRD

This section quickly covers two alternative methods commonly used in the literature to characterize ferroelectric materials, that were not performed in this thesis. One such method is capacitance-voltage (CV) measurement. CV-measurements are often performed to characterize oxides for defect response at various AC frequencies or material properties such as the thickness or relative permittivity [58]. The method involves measuring the capacitance of an oxide by applying a small signal AC voltage (with constant amplitude) which overlays a DC voltage [58]. The current generated from the small signal voltage will give rise to a current, which can be integrated to find the charge that is moved during the voltage sweep. This can be used to calculate the capacitance as the DC voltage is varied. By calculating the capacitance of a MOSCAP during accumulation (when charge carriers accumulate at the semiconductor-oxide interface), you can accurately calculate the relative permittivity of the oxide if the thickness is known [58].

Another prevalent method is Grazing Incidence X-ray Diffraction (GIXRD), where x-rays impact the sample at incidence angles slightly above the angle of total reflection to avoid noise from the substrate [59]. The incidence angle is varied and the intensities of reflected x-rays are measured. This intensity will have peaks corresponding to various crystal phases in the material [59]. This can be used to measure the relative prevalence of, for example, orthorhombic, monoclinic and tetragonal crystal phases in HZO thin films [22].

6 Results

In this section the different process series (labeled M1, M2 and M3) and associated results are presented. Most errors/error bars are calculated from the standard error of the mean, except for the ellipsometric data from Si wafers in series M2, which is instead given in mean-square error (MSE) of the fit parameters used in the ellipsometer software (which are unit-less). According to [50], a MSE below 15 is considered adequate.

6.1 Process Series

To make it easier to study the result section (and the appendix for the interested), all sample series are presented in this subsection with both their motivation and a visual representation in the form of a process matrix. In each process matrix, an "id" can be used to later identify the sample. Unless anything else is mentioned, all samples are processed on InAs(111), which has been epitaxially grown on a Si wafer. The InAs epilayer was non-intentionally doped (nid) with approximate doping concentration $5{\cdot}10^{17}$ cm^{-3}.

6.1.1 Series M1: 1:1 HZO at elevated temperatures

The process matrix of the first series is summarized in Fig. 16. In the initial MOSCAP series, it was decided that the ALD growth at higher temperatures needed to be addressed, since the as-deposited crystallization of the ferroelectric phase was believed to be promoted by the crystallization of ZrO_2 (which starts occurring in the ALD process already around 200 °C [42]). The oxides are grown as solid solution HZO (1:1 HfO_2:ZrO_2), with the other deposition parameters featured in table 1. The targeted thickness was ∼15 nm by running the ALD process for 150 cycles (this was based on the fact that at 200°C deposition temperature the growth rate is in the Picosun ALD, approximately known to be 1 Å/cycle using this recipe). The naming scheme presented in Fig. 16 should be read as "Deposition Temperature_x", where "x" indicates what is special about each sample. Three additional samples were added to the growth at 275 °C to investigate some miscellaneous things:

1. id: 275_wRTP, which was subjected to low temperature annealing at 200°C for 30 min after top-metal capping in the RTP oven. This was added to see if the leakage characteristics could be improved similar to [60].
2. id: 275_nInAs, which was grown on a different substrate, a InAs(100) wafer, n-doped to $5{\cdot}10^{17}$ cm^{-3}. The effect of the InAs substrate has previously been known to influence the behaviour of the oxide, see e.g. [61].
3. id: 275_surface, which was identical to the other samples, except it had two fewer steps of precleaning before being put in the ALD chamber. This meant it was only subjected to one ozone cleaning/re-oxidization step and one wet etch after a regular acetone/IPA rinse, before being placed in the ALD chamber. This sample was added to investigate the influence of the quite thorough treatment.

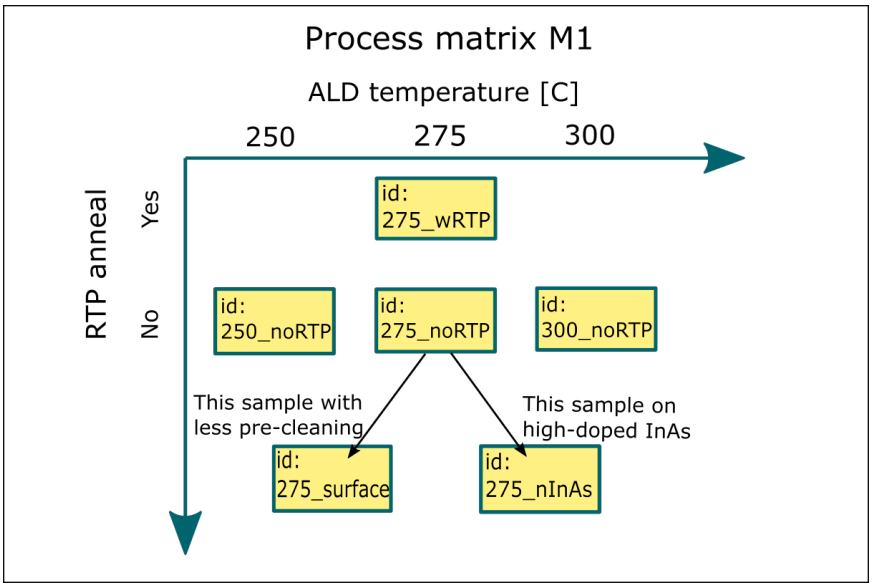


Fig. 16: The process matrix of the initial MOSCAP series to investigate high temperature deposition of the oxide.

6.1.2 Series M2: 60%Zr laminates at elevated temperatures

In this series, the HZO oxides were constructed from different laminate structures presented in Fig. 17 at ALD chamber temperatures of 300 °C and 325 °C. The motivation behind this was that while some of the samples from series 1 appeared ferroelectric, it was weakly so, and the hypothesis was that either the temperature or Zr concentration was too low to facilitate the desired crystallization. All laminates presented here contains 60 at% Zr and are given in the configuration Hf:Zr:Hf (see section 2.3.3 to get an idea of the construction of laminates). The naming scheme of the samples presented in Fig. 17 is "Laminate Structure_Deposition Temperature", e.g., sample 4124_300 was grown with laminate structure 4:12:4 (Hf:Zr:Hf) at 300 °C.

To reduce the potential effect of changing the interface layer, it was also decided to have four cycles of HfO_2 towards the InAs interface for every sample in this series. While the target thickness still remained at 15 nm, it was not possible to grow the same number of cycles for each laminate. In total, the 4:12:4 laminate was grown for 144 cycles and the 5:15:5 and 6:18:6 laminates were grown for 154 cycles. Due to limitations in the programmable loop of the Picosun ALD, the top layer of the oxide was always twice the HfO_2 (e.g. for the 4:12:4 laminates, the top layer was 8 cycles of HfO_2). Together with the two 4:12:4 laminate samples, a 2" Si wafer was also placed in the ALD chamber to investigate how well the oxides would grow at several different coordinates in the chamber at 300 and 325 °C. The 4:12:4 samples were placed on the wafers and centered as much as possible on the ALD carrier wafer (where you place your sample).

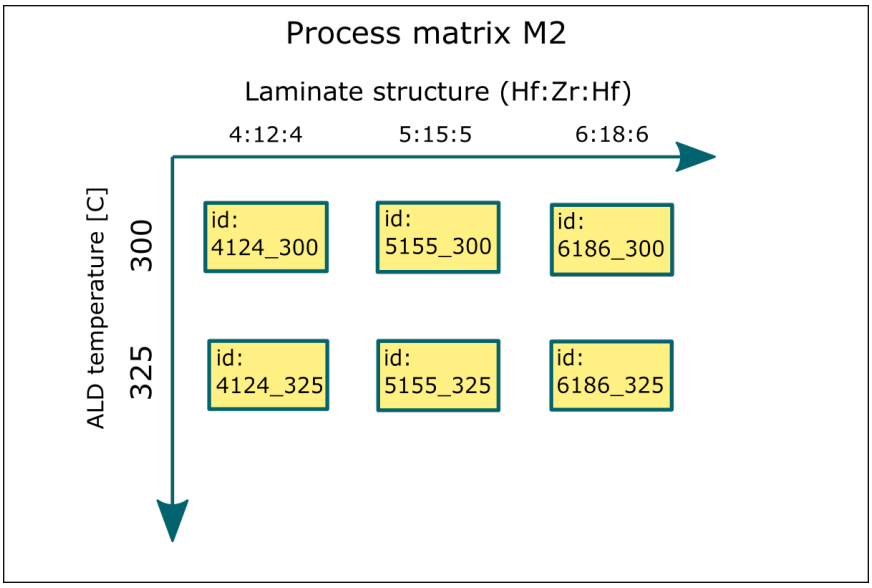


Fig. 17: The process matrix of the second series where different laminates and deposition temperatures were examined.

6.1.3 Series M3: Scaling and interface study of a laminate

Since almost all samples produced in series M2 showed ferroelectric crystallization, this series instead aimed to investigate the most promising laminate and temperature combination from that series. The sample labeled 4124_300 (grown at 300°C ALD chamber temperature with the laminate structure 4:12:4 (Hf:Zr:Hf)) showed the highest remanent polarization, and adequate oxide quality. It was also the most scalable of the samples and was thus chosen to investigate just that. The interface layer down to the substrate was also varied to produce the process matrix in Fig. 18. The id of each sample should be read as "Number of supercycles_Interface Layer Cycles" , e.g., sample 7L4i was grown for 7 supercycles with 4 layers of HfO_2 towards the substrate. Two samples in this series are significantly different from the others:

1. id: 7L6Ali had 6 ALD cycles of alumina towards the InAs substrate. This was added to test if this would improve leakage characteristics of the oxide since this is a common use case for alumina in transistor processes [62].
2. id: 7L4i(MIM) had its oxide grown on a TiN bottom electrode that had been sputtered on a Si(100) wafer. This was added as a reference sample in order to compare with MIM structures in literature.

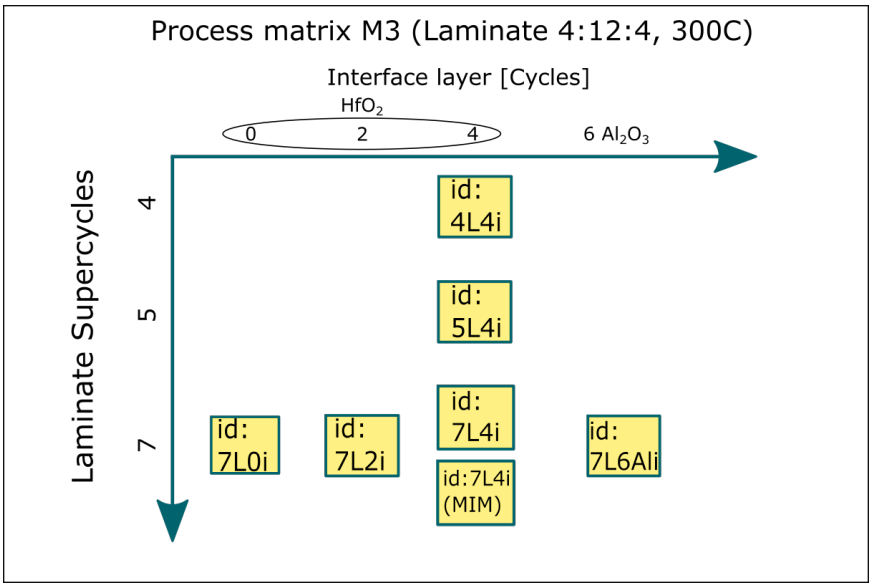


Fig. 18: The process matrix of the third series where the scaling and interface were examined for the most prominent sample from series 2.

6.1.4 Annealing study: Scribing and RTP of series M1 and M2

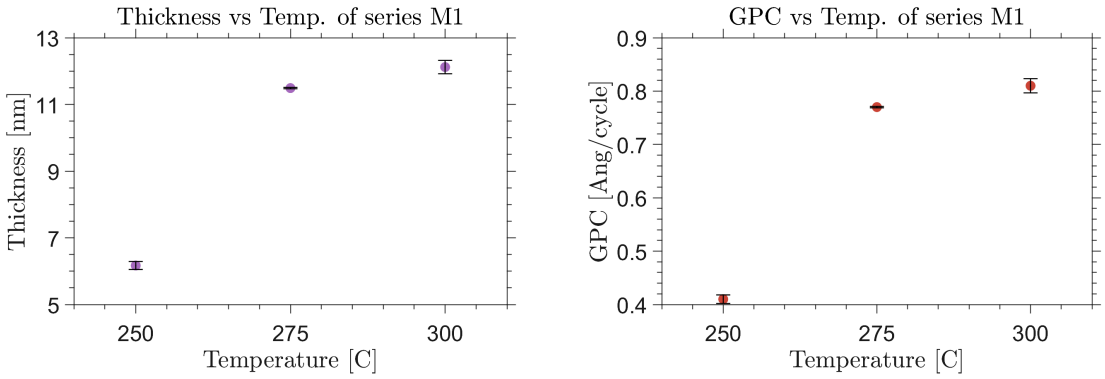
To study if the remanent polarization of the samples from the aforementioned series could be improved upon, they were scribed and subjected to post-process RTP. This means a diamond cutter was used to split the samples into four similar pieces, and three of these pieces from each original sample was put in the RTP at temperatures of 350, 400 and 450 °C for 30 s in an N_2 atmosphere. This is in alignment with [63]. All of these samples were measured with the PUND technique to determine the remanent polarization. The sample 275_nInAs from series M1 was not part of this series as it was already too small to handle comfortably.

6.2 Ellipsometry results

In this section, relevant growth data extracted using ellipsometry is presented. This is primarily the oxide thickness and growth rate per cycle (GPC), which refers to the thickness (in angstroms) grown for every ALD cycle.

6.2.1 Series M1

Fig. 19a contains the oxide thickness of samples produced in series M1 for different ALD temperatures. Meanwhile, Fig. 19b displays the GPC of the samples from series M1 for the same temperatures.

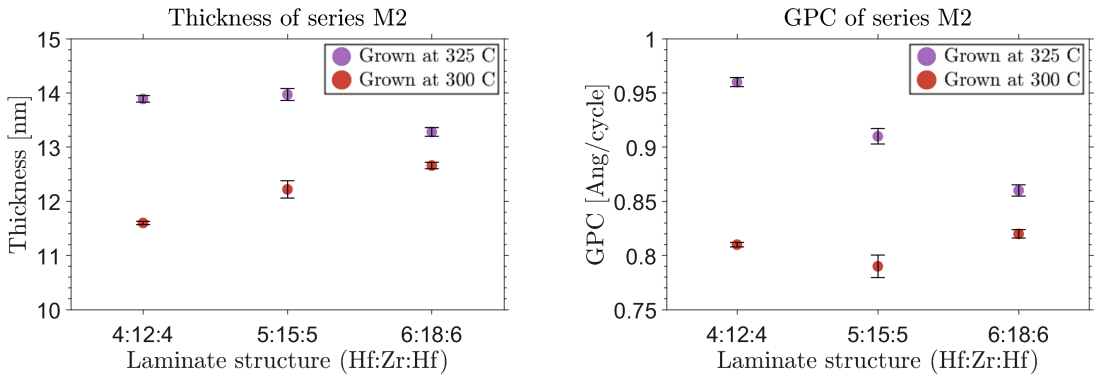


(a) (b)

Fig. 19: (a) The thickness of samples from series M1 vs ALD growth temperature. (b) The GPC of samples from series M1 vs ALD growth temperature.

6.2.2 Series M2

Fig. 20a indicates the thickness of samples produced in series M2 for different laminate structures (Hf:Zr:Hf) of HZO, grown at two different temperatures. When studying this graph, remember that the 4:12:4 laminates were grown for 144 ALD cycles, while the others were grown for 154 cycles. Fig. 20b contains the GPC of the samples with different laminate structures and temperatures.



(a) (b)

Fig. 20: (a) The thickness grown for each laminate structure at the two different deposition temperatures. (b) The corresponding GPC for each laminate and ALD temperature

Fig. 21a contains the thicknesses at various coordinates on an Si wafer added in the ALD chamber with some of the

samples from series M2. The wafer was placed in the ALD reaction chamber and had 4:12:4 laminated HZO grown on top at 300 °C. Fig. 21b contains the corresponding MSE for each coordinate. Meanwhile, Figs. 21c and 21d displays similar data, but for an oxide growth at 325°C instead. The wafers have been measured with the primary flat of Si(100) oriented towards the operator in the ellipsometer. This flat was oriented towards the right when facing the ALD. These wafers were placed in the ALD chamber with a smaller sample (for MOSCAP processing) located on top at the center point.

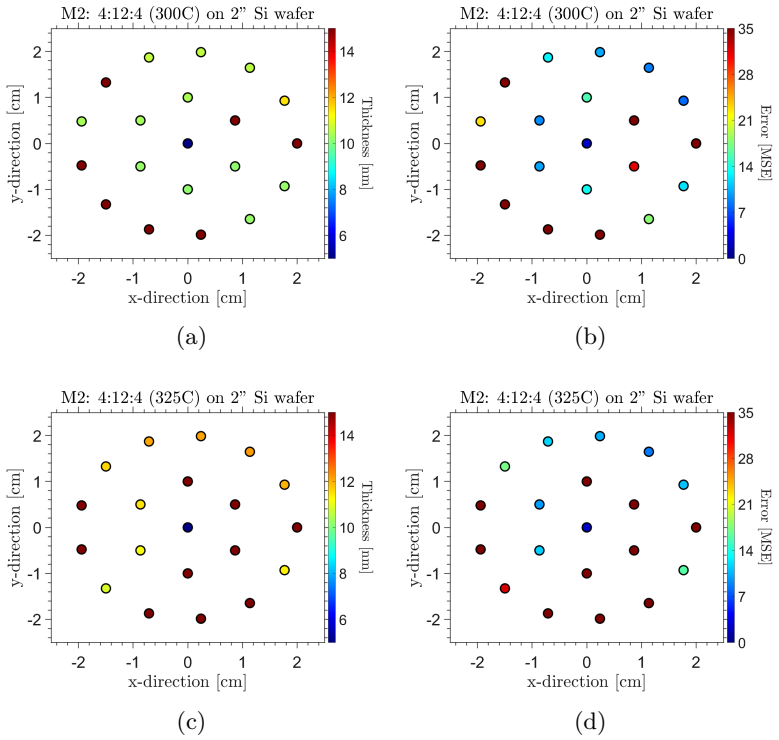
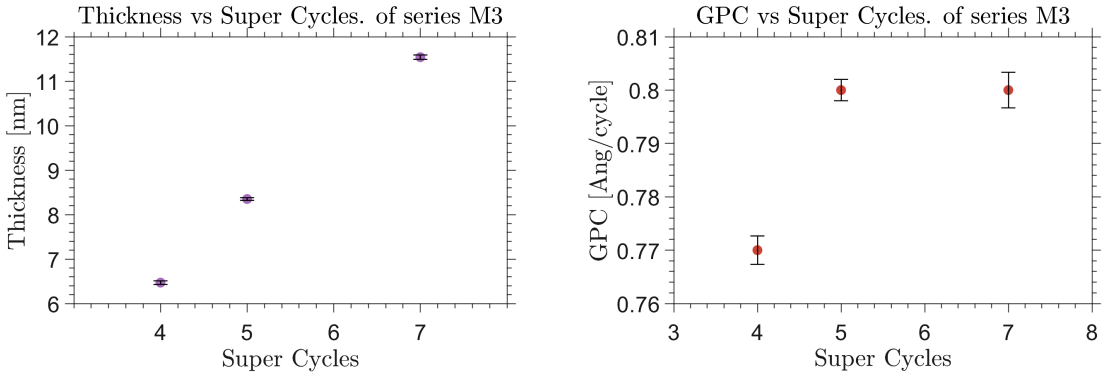


Fig. 21: (a) and (c) highlight the deposition of 4:12:4 laminated HZO at 300 and 325 °C respectively at different locations on polished Si(100) wafers. The MSE of each location is displayed in figure (b) and (d) respectively.

6.2.3 Series M3

Fig. 22a holds the thickness data of MOSCAP samples produced in series M3, for different supercycles of 4:12:4 laminated HZO. Note that one 4:12:4 supercycle would correspond to 4+12+4=20 regular ALD cycles. Fig. 20b contains the GPC of the samples from series M3 for the different number of supercycles. Additionally worth noting is that the MIM sample produced in this series (not included in Fig. 22a) had a thickness of 13.1 nm, which deviated from the MOS samples with 7 supercycles.



(a) (b)

Fig. 22: (a) The thickness of the oxide (in MOSCAPs) for different supercycles. (b) The GPC for the different number of supercycles.

6.3 IV results

In this section, the leakage data from process series M1, M2, and M3 are presented, together with IV-sweeps performed on certain samples in search for FTJ behaviour. Note that the breakdown voltage data for all samples exist in the appendix at the end of this report. No obvious trend was found for that data, which is why it is not included here.

6.3.1 Series M1

In Fig. 23, the IV-characteristics of the entirety of series M1 can be found, with each sample indicated by the associated id. The breakdown of the oxides occurs when the data spike vertically.

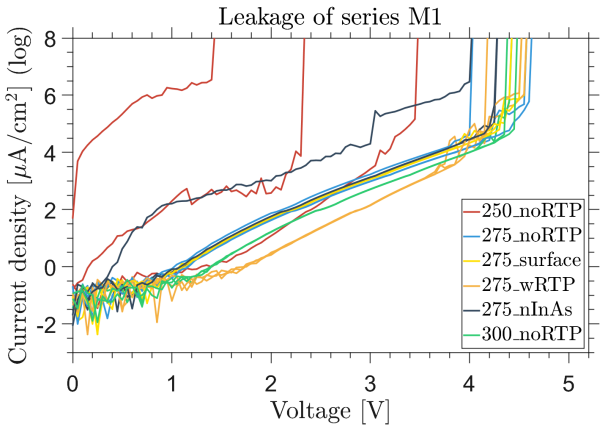
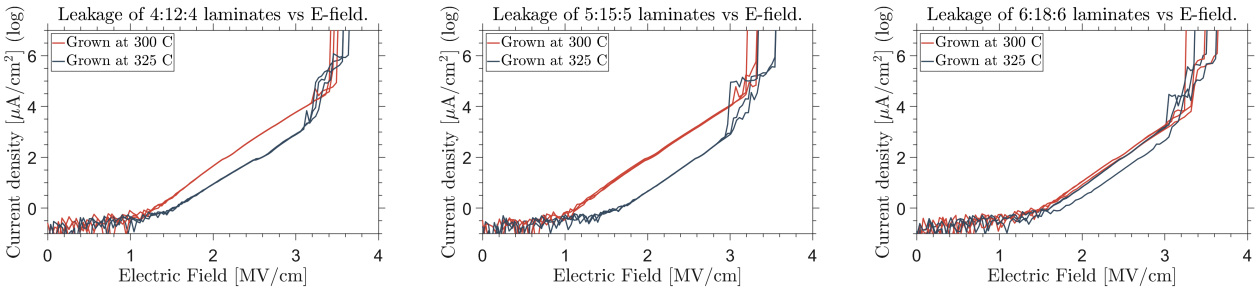


Fig. 23: IV-plots for all samples of series M1. This data is extracted from MOSCAPs with radius 15 μm.

6.3.2 Series M2

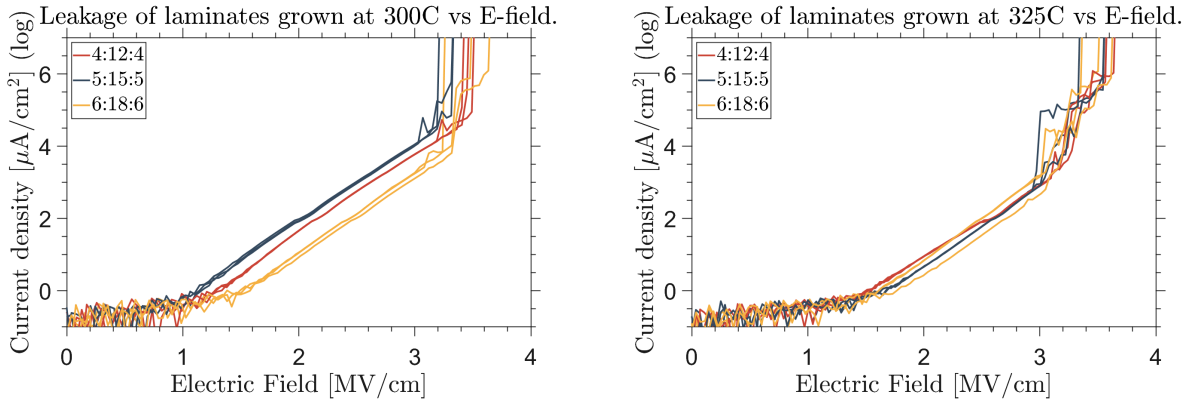
The leakage characteristics of the laminate structures 4:12:4, 5:15:5, and 6:18:6 at ALD temperature 300 and 325 °C is illustrated in Figs 24a, 24b and 24c respectively.



(a) (b) (c)

Fig. 24: (a) IE-plot of 4:12:4 laminate grown at 300 and 325 °C. (b) IE-plot of 5:15:5 laminate grown at 300 and 325 °C. (c) IE-plot of 6:18:6 laminate grown at 300 and 325 °C.

Figs. 25a and 25b contains IE-plots that compare the leakage of series M2 for each laminate structure at ALD growth temperatures 300 and 325 °C, respectively.

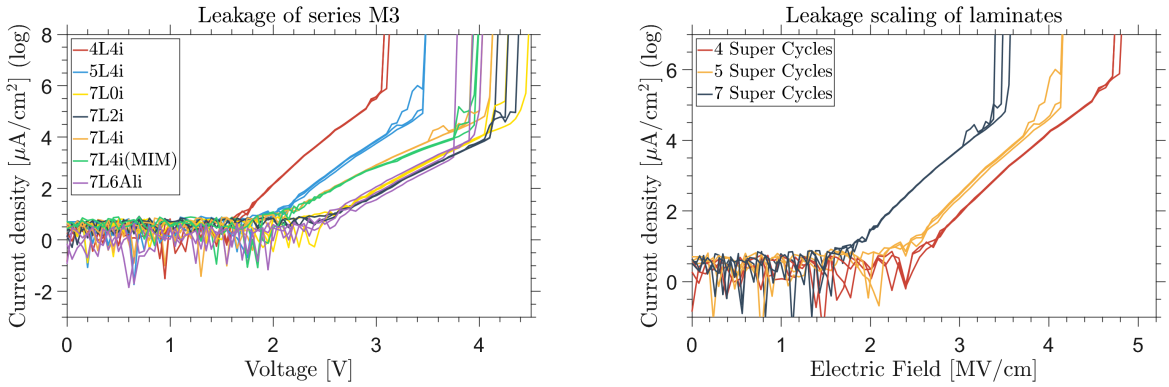


(a) (b)

Fig. 25: (a) IE-plots for different laminates grown at 300 °C and (b) IE-plots for different laminates grown at 325 °C.

6.3.3 Series M3

Fig. 26a contain the IV-plots for all samples of series M3 extracted from MOSCAPs with radius 15 μm and Fig. 26b compares the leakage against the electric field over the oxide for different number of super cycles.

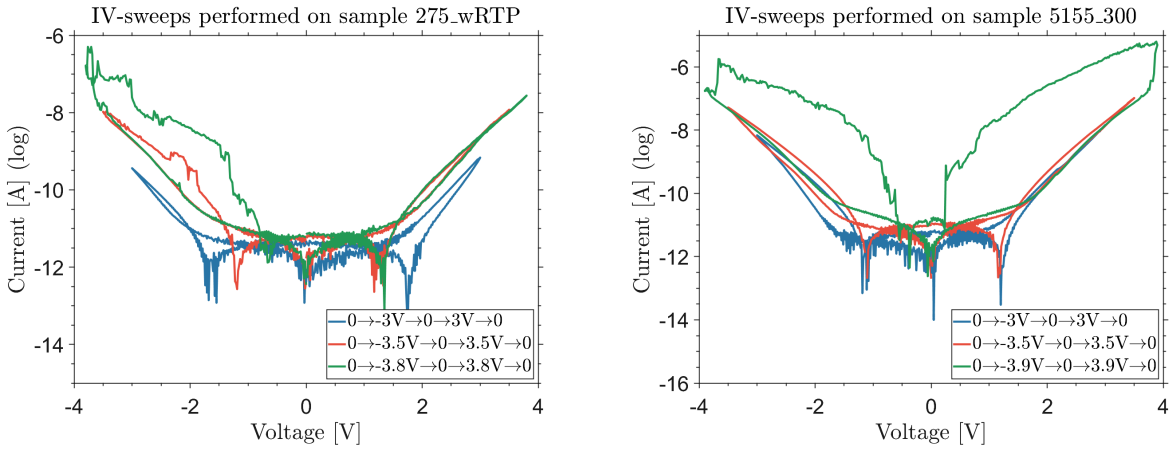


(a) (b)

Fig. 26: (a) IV-plots for all samples of series M3 extracted from MOSCAPs with radius 15 μm. (b) Comparison of the leakage against the electric field over the oxide for different number of super cycles.

6.3.4 IV-sweeps

Figs. 27a and 27b contains IV-sweeps performed at different voltages for ferroelectric samples from series M1 and M2, respectively. The sample from series M1 had solid-solution HZO grown at 275 °C while the sample from series 2 had laminated 5:15:5 HZO grown at 300 °C. In Fig. 27a the TER at -2 V in the negative 3.8V sweep can be extracted as TER=$10^{1.88}$, and in Fig. 27b the TER at -2 V in the negative 3.9 V sweep is TER=$10^{2.58}$. At +2 V in this figure, the TER in the positive 3.9 V sweep can be extracted to be TER=$10^{3.00}$.



(a) (b)

Fig. 27: (a) Some IV-sweeps performed on a ferroelectric sample from series M1 where the oxide had been grown at 275°C ALD, at varying voltages. (b) IV-sweeps on a 5:15:5 laminate from series M2 that had been grown at 300 °C, at varying voltages.

6.4 PUND results

This section shows some hand-picked results from applying the PUND technique to the samples produced in this master thesis to screen for ferroelectric figures of merit. Additionally, the approximate relative permittivities are extracted for all samples and presented in a table. As an example for the interested reader, a PUND-pulse with the measured current (similar to figure 15) is included in the complementary PUND-data in the appendix.

6.4.1 Series M1

Fig. 28 contains two P-E curves of ferroelectric oxides produced in series M1, together with the corresponding I-E graph that shows the current that is integrated to generate the P-E graph. Figs. 28a and 28b, contains a set of P-E and I-E curve for solid solution HZO grown at 275 °C. This was generated from PUND pulses at 4V, without any wake-up cycles, and had a remanent polarization $P_r = 2.1\ \mu C/cm^2$. Meanwhile, Figs. 28c and 28d, contains the set of P-E and I-E curve for solid solution HZO grown at 300 °C. Here PUND was performed at 4V, also without wake-up cycles. The remanent polarization was $P_r = 1.5\ \mu C/cm^2$. The red arrow indicates how this was extracted, while the purple ellipse indicates the distortion due to leakage.

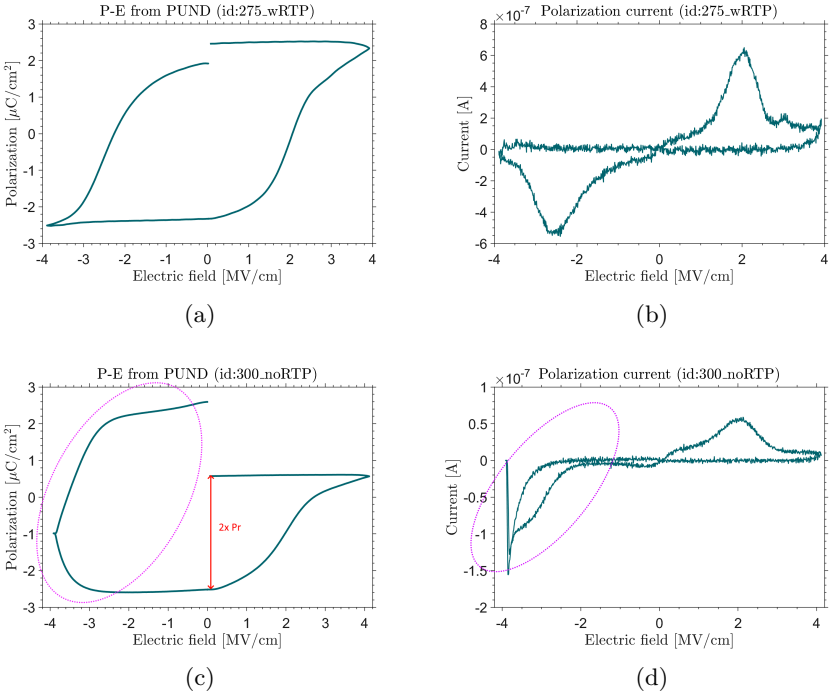


Fig. 28: (a) The P-E curve (4V PUND, no wake-up), with the highest remanent polarization measured in series M1 for an oxide grown at 275 °C (b) the corresponding switching current in an I-E plot. (c) The P-E curve (4V PUND, no wake-up) measured in series M1 for an oxide grown at 300 °C (d) the corresponding switching current in an I-E plot.

6.4.2 Series M2

Fig. 29 contains the best remanent polarization for the two different ALD temperatures, and for each laminate structure produced in series M2. The remanent polarization for the 300 and 325 °C data points was generated from PUND at 4 V and 4.5 V respectively[11].

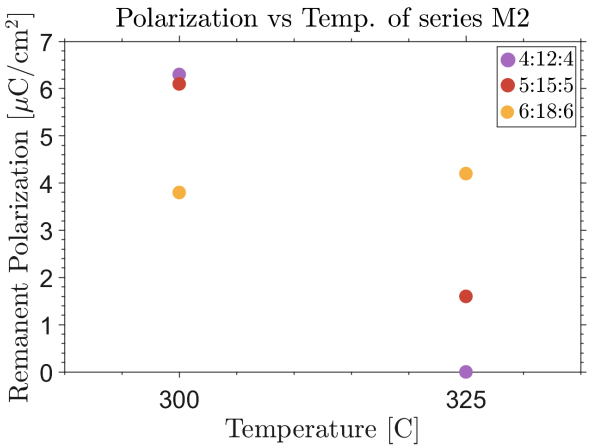
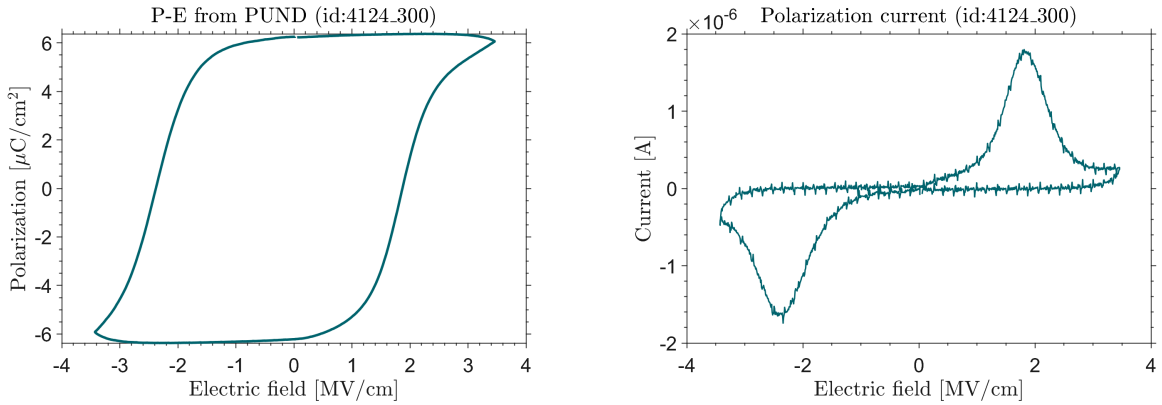


Fig. 29: This figure depicts the best remanent polarization for the two different ALD temperatures, and for each laminate structure produced in series M2. The P_r for the 300 °C data points was generated from PUND at 4 V, while for the 325 °C data, PUND was applied at 4.5 V.

Fig. 30 contains the P-E curve for the 4:12:4 laminated HZO oxide deposited at 300 °C, and the corresponding I-E data. Here, the PUND pulse was applied at 4V without any wake-up cycling. The remanent polarization was P_r = 6.3 μC/cm^2.



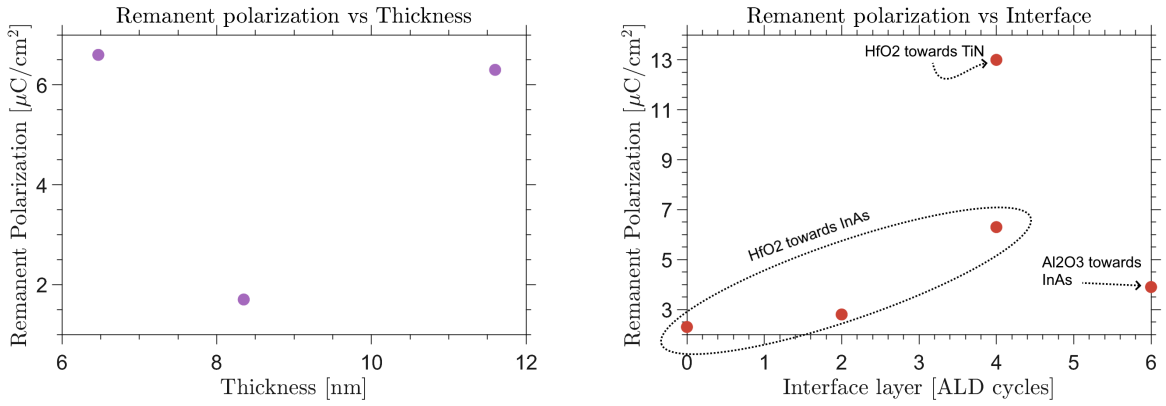
(a) (b)

Fig. 30: (a) The P-E curve (4 V PUND, no wake-up) with the highest remanent polarization measured in series M2 for the 4124_300 sample and (b) the corresponding switching current in an I-E plot.

[11] Note that the higher voltage is required for thicker samples in order to reach equivalent electric fields.

6.4.3 Series M3

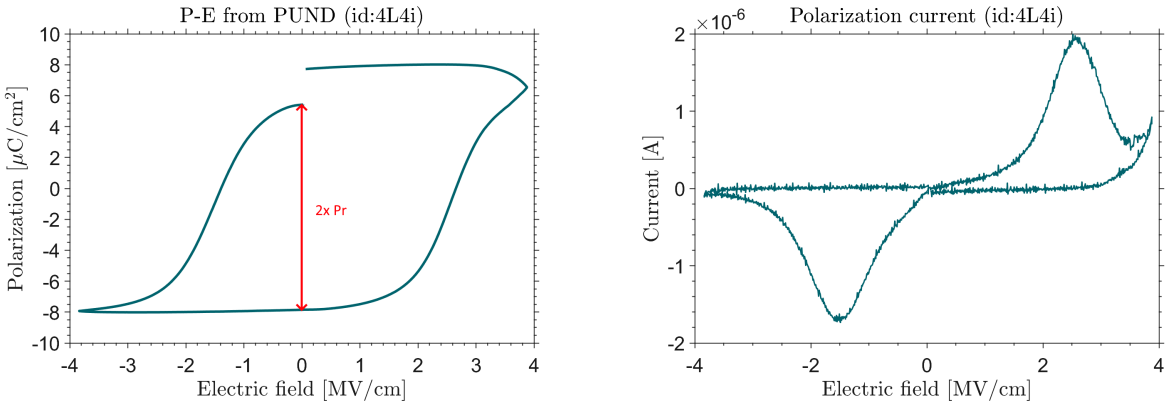
Fig. 31a displays the highest remanent polarization when scaling the supercycles for the 4:12:4 laminate structure deposited at 300 °C. In Fig. 31b, the interface layers of the 4:12:4 laminate grown for seven supercycles have been modified and the maximum remanent polarization is indicated. The interfaces are indicated in the figure.



(a) (b)

Fig. 31: (a) The highest remanent polarization measured versus the thickness after reducing the number of supercycles. (b) The highest remanent polarization for samples with different interface layers.

In Fig. 32 the P-E plot of the highest achieved polarization for the most scaled sample in the series is plotted. The graph beside it contains the corresponding I-E curve. Due to significant leakage, the remanent polarization was extracted according to the red arrow. This yields $P_r = 6.6\ \mu C/cm^2$.

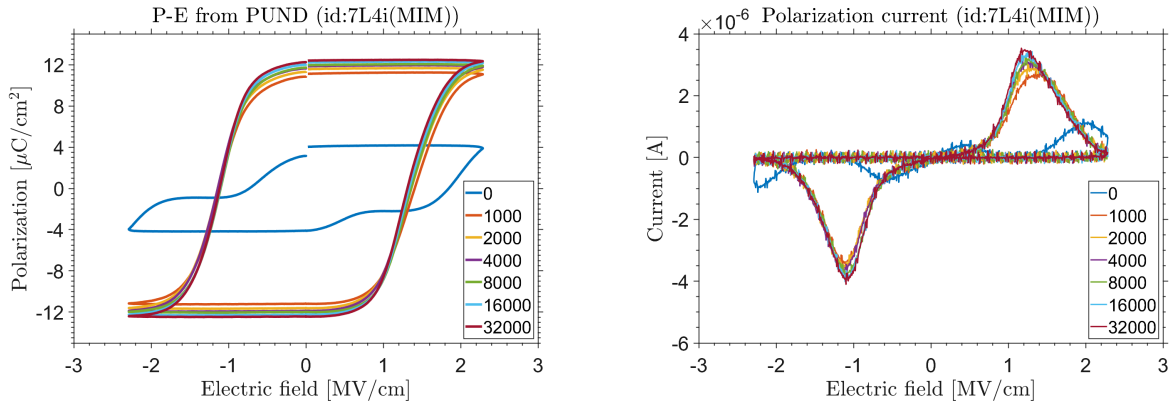


(a) (b)

Fig. 32: (a) The P-E curve (2.5V PUND, 5000 wake-up cycles at 2.5V) with the highest remanent polarization measured for the most scaled sample of series M3. The sample consisted of 4 supercycles (id:4L4i), and (b) the corresponding switching current in an I-E plot.

The highest as-deposited remanent polarization achieved in this master thesis is displayed in Fig. 33. This was a MIMCAP with and oxide consisting of a seven supercycle 4:12:4 laminate, deposited at 300 °C on TiN. Here, the PUND pulse has been applied at 3V after a number of wake-up cycles indicated in the figure. Already after the first

1000 cycles, the remanent polarization rapidly approaches its saturation at $P_r = 12.3\ \mu C/cm^2$. The corresponding I-E plots are plotted in the right figure.



(a) (b)

Fig. 33: (a) P-E curves after different number of wake-up cycles for the MIMCAP sample of series M3 (id:7L4i(MIM)). PUND was performed at 3V. This was the highest as-deposited remanent polarization achieved in this project. (b) The corresponding switching currents in an I-E plot.

6.4.4 Relative Permittivity

Table 2: This table contains the relative permittivity of the samples produced in this project. The permittivity is calculated from the average value of the current during the U-pulse of PUND for devices with as little leakage as possible.

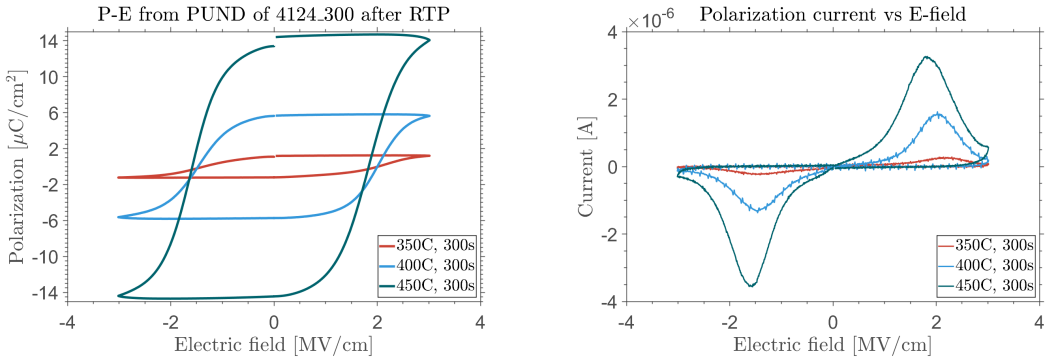
Series M1	ε_r	Series M2	ε_r	Series M3	ε_r
250_noRTP	-	4124_300	25	4L4i	18
275_noRTP	13	5155_300	27	5L4i	24
275_surface	-	6186_300	21	7L0i	19
275_wRTP	26	4124_325	39	7L2i	24
275_nInAs	21	5155_325	33	7L4i	20
300_noRTP	24	6186_325	30	7L4i(MIM)	39
-	-	-	-	7L6Ali	21

In table 2 the permittivity of the different samples produced in this master thesis is summarized. It has been calculated from primarily the U-pulse of PUND to avoid the inclusion of polarization current in the calculations. These are extracted from data from devices with little to no apparent leakage. The samples for which the permittivity has not been noted had too much leakage to extract any useful data.

6.5 Annealing study

The initial results of the annealing study, where all of series M1 and M2 were scribed and subjected to RTP at different temperatures, have been underwhelming. The remanent polarization of all samples has not, or just marginally improved. Some samples have even displayed worse remanent polarization after being subjected to the same PUND and wake-up cycling as the as-deposited samples. Clear improvements could be found for two samples in series M1 grown at 275 °C (id:275_noRTP and 275_surface), which became ferroelectric after 400 and 450 °C RTP for 30s. However, the highest achieved remanent polarization among these even at 450 °C RTP was P_r=6

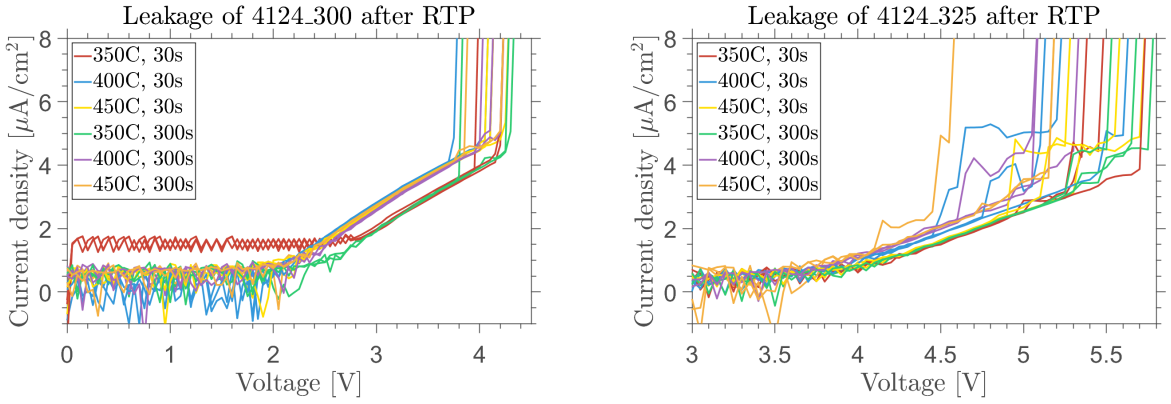
μC/cm^2. As a last trial, the scribed samples from the 4:12:4 laminate samples were once again annealed, but for an additional 300 s each, at the same RTP temperatures as previously (350, 400, 450 °C). The result of this is indicated in Fig. 34. The remanent polarization achieved was 1.2, 5.7, and 14.5 μC/cm^2 for RTP at 350, 400, and 450 °C respectively on the 4:12:4 laminate sample originally grown at 300 °C. No ferroelectricity was found in the corresponding sample originally grown 325°C even after the longer duration RTP.



(a) (b)

Fig. 34: (a) The P-E curves after PUND performed on the 4124_300 sample after additional RTP since the first attempt failed. All P-E curves are generated after PUND performed at 3.5V after 3000 wake-up cycles. (b) The corresponding switching currents of the different samples in an I-E plot.

Figs. 35a and 35b depict the leakage of 4:12:4 laminate samples originally grown at 300 and 325 °C, respectively. Both the results after the initial RTP study where the samples were heated for 30 s, and after the second RTP attempt for an additional 300 s are reported. All data comes from r=15 μm devices.



(a) (b)

Fig. 35: (a) The IV-characteristics of the 4124_300 sample from series M2 at various different RTP temperatures after 30 and an additional 300 s anneal time (b) The IV-characteristics of the 4124_325 sample from series M2 at various different RTP temperatures after 30 and an additional 300 s anneal time

7 Discussion

In this section, the results presented in section 6 will be discussed and compared with relevant research.

7.1 Ellipsometry

The recipe used to grow the HZO oxides listed in table 1 has been optimized for the specific ALD chamber used in this thesis, when the chamber temperature is kept at 200 °C. The growth rate is then expected to be approximately one Å/cycle, which for 150 cycles in series M1 would correspond to 15 nm. As can be seen in Fig. 19a, this was clearly not the case here as the oxides are thinner than expected for all growth temperatures. Especially deviating is the growth at 250 °C, which only resulted in 40% of its targeted thickness. This dip is difficult to explain since there is a myriad of different variables that can cause suboptimal growth. An example of this is the other ALD process parameters, or even the type of substrate (this was the case for the MIM sample grown in series M3, which grew thicker than MOS samples, with equivalent growth conditions). In another work [64], a slight dip in the deposition rate of HfO_2 can be observed in the temperature window 200-375 °C, but with deposition performed on Si substrates rather than InAs. This dip does not account for the discrepancy since it also suggests the oxide should grow even worse at 275 °C and 300 °C, which is not the case in Fig 19a. Growth rates that are more in line with what was observed here, except for at 250 °C, can be found in [65], where growth rates in the range 0.75-0.8 Å/cycle was observed for 250-300 °C depositions. However, this was for pure HfO_2 rather than HZO.

Other sources also indicate that ZrO_2 has reduced growth rate in this temperature window. In [42] the deposition rate is reduced within the relevant temperature window, but remains quite a lot higher than the results observed for HZO in this project at 1.2-1.4 Å/cycle. Research indicates the occurrence of termination of growth during the ALD process for various oxides. In [66] this occurs at temperatures of 250 °C and 275 °C after 80 and 20 cycles of ZrO_2 growth, respectively. However, the oxide is deposited on carbon nanotube substrates, which differs greatly from InAs. There is some evidence that the precursor used for ZrO_2 deposition in this project (TEMA-Zr) starts decomposing above 250 °C chamber temperature, which can lead to either termination of growth [66], or an increased growth rate if other components of the precursor (e.g. coal) are incorporated on the surface [34].

Some oxides deposited during series M2 were more in line with the targeted thickness of 15 nm. While the laminates deposited at 300 °C grew in line with the 300 °C sample from series M1, the samples deposited at 325 °C all grew approximately 2 nm thicker than their 300 °C counterparts (see Fig. 20a). This might be related to the previously mentioned decomposition of Zr precursor at elevated temperatures where precursor atoms other than Zr could become incorporated in the oxide. Note that the apparent linear trend observed for 300 °C growth in Fig. 20a results from the 4:12:4 laminate being grown for fewer total cycles. A real trend can be observed for the GPC of laminates in figure 20b, where the growth seems to decline for thicker laminates, where thicker ZrO_2 layers are sandwiched between the HfO_2. The reason behind this is not clear and it is most likely not related to the stability of TEMA-Zr, since the atomic percent Zr should be the same for all laminates.

Observing the HZO grown on Si wafers in Figs. 21a and 21c, they indicate that the 4:12:4 laminates grow relatively well on Si. The middle point of each wafer has, as expected, zero growth. This is because this is the location where regular samples were placed during deposition. Comparing Figs. 21a to 21c, we can see that the 325 °C deposition grew thicker, which corresponds to the results for the MOSCAP samples in Fig 20a. The red points on both wafers are much thicker than the others, and are in the μm range with large MSE (which indicates a bad fit). This can be caused by dust or other dirt particles being present at these points during growth, or other defects. These points might also indicate that the ALD deposition is highly coordinate dependent. Surprisingly, the area around the middle of Fig. 21c seems to contain many such errors. This is despite the middle of the wafer usually being the cleanest part.

In Fig 22a, a linear trend in the thickness-scaling can be observed, and the GPC displayed in Fig. 22b does not deviate significantly as the number of supercycles are reduced. The growth rates per cycle of all samples are in line with what was expected from ALD at 300 °C from the previous two series, except for the MIM sample, which grew slightly thicker than the rest. While it is difficult to predict the exact reason the oxide grew better in the MIM, research performed on different ALD processes indicates that the substrate, and especially the surface construction,

plays a central role in determining the growth [67]. These differences can be caused by, for example, different surface crystallinity or nucleation barriers (the energy required to form small islands on the surface). The difference between these samples can also partly be an artifact of the way the ellipsometer functions. The MIM capacitor has to be modelled slightly differently compared to the MOSCAP (it was modeled using a Cauchy model, see section 5.1) due to the structural differences, which means they are not trivial to compare. You should always be careful when comparing samples that structurally deviate from each other by much.

7.2 IV-characteristics

In Fig. 23, the IV-characteristics of every sample in the first process series can be seen. While trends in general were difficult to distinguish here, two of the samples appear to be significantly worse in terms of leakage than the others: the sample grown on n-doped InAs substrate rather than epilayer InAs (id:275_nInAs), and the oxide grown at 250 °C, which was the thinnest sample (id:250_noRTP). Another outlier is the low-temperature annealed sample (id:275_wRTP), which appears to have an order of magnitude lower leakage current in Fig. 23, compared to any other sample. Research on other substrates and oxides has previously indicated that a post-metallization anneal can greatly improve leakage currents. For example, in [60] an Al/SiON/Si MOS structure was annealed at 400 °C for 60 min, which reduced the leakage of the oxides approximately three orders of magnitude. In [60] the breakdown voltages also appear to improve drastically post-anneal, but this improvement is not clear for the oxides in this work. To explain the suboptimal leakage observed in the n-doped InAs sample, one might consider what sets this sample apart. The InAs in this sample does not just originate from a non-epitaxial wafer, but it is also n-doped (rather than nid as the other samples), and the surface is oriented in the (100) crystal direction as opposed to the (111) direction of the other samples. The crystal orientation might have some influence as high-k dielectric deposited on InAs(111)B (As-terminated) has been found to have lower interface defect density than InAs(100) [61], which would lead to better IV-characteristics. Note that the exact surface construction is not known for the substrates in this project. This is because the samples are subjected to a wet etch before being placed in the ALD chamber, which means it is not known if it is In- or As-terminated.

Since the thickness of the oxides of series M2 differed significantly, the IE-characteristics were compared rather than the IV-data. The leakage of the different laminate structures for the two different deposition temperatures is plotted in Figs. 24a, 24b, and 24c. The two samples with the highest degree of suspected o-phase (highest P_r), the 4:12:4 and 5:15:5 laminates deposited at 300 °C, are also the ones which show the largest leakage. The entire series also have breakdown voltages that seem to improve for samples with lower remanent polarization. This could be related to the fact that as ferroelectric crystals are formed, grain boundaries can also form along the crystal planes. This is illustrated well in Fig 4. in [68]. This could mean that the samples that have lower leakage also contain much more amorphous material, which in turn would explain the lower remanent polarization. In Fig. 24c one can see that the oxide with 6:18:6 laminate grown at 300 °C behaves more like its 325 °C counterpart than the other samples deposited at 300 °C to theirs. At the same time, it has displayed lower remnant polarization, meaning the thicker ZrO_2 in each supercycle might be associated with a more amorphous film. In summary, oxides with more ZrO_2 layers within each supercycle and that are deposited at higher temperatures, grow thicker, and apparently contain more amorphous material. This provides further evidence that the Zr precursor might be decomposing during growth from the elevated temperatures. Another interesting aspect is the fact that all IV-curves for this series (and series M3) only seem to have one leakage mechanism for most of the voltage sweeps, since the exponential leakage in the graphs (linear in the log-plots) does not change slope. Therefore, it might be interesting to try to fit different leakage mechanisms to these plots as detailed in [51]. I did not have time to do this at this point.

The leakage of series M3 almost followed expectations. The scaled samples (id:4L4i and 5L4i) showed more leakage (see Fig. 26a), and among them the 4 supercycle sample had an order of magnitude worse leakage. This is consistent with it being almost 2 nm thinner. Among the samples consisting of seven supercycles, the two samples with 7 supercycles and 4 cycles of HfO_2 interface layer (id:7L4i and 7L4i(MIM)), were grown together and had very similar IV-characteristics. The MIM sample was expected to have the lowest leakage, since this had been the general trend for these samples when the oxide is deposited at 200 °C in the Picosun ALD, but this was not the case here. It is also difficult to say which of the samples where the interface layer was modified (id:7L0i, 7L2i, and 7L6Ali) had the best IV-characteristics. The two samples which had 0 and 2 cycles of HfO_2 towards the oxide had comparable leakage to

the sample with an alumina interface layer, but Fig. 26a indicate that they have higher breakdown voltages. One would expect an alumina interface layer to noticeably improve the leakage as this is a common application for that oxide [62]. While alumina has been grown at 300 °C in another ALD reactor at LNL, it has not been optimized for this temperature in the Picosun ALD which in turn might have deteriorated the growth. Comparing the samples where the interface layer HfO_2 is reduced from 4 to 0 cycles of HfO_2 (id: 7L4i, 7L2i, and 7L0i), the leakages seem to decrease as the hafnia layer towards the substrate decreases (or in other words: ZrO_2 towards InAs has better IV-characteristics). This might indicate that a more amorphous film is formed already at the interface, which is in part supported by measuring the remanent polarization which decreases as the hafnia interface is removed. It could also be related to the incitement of the monoclinic phase on a tetragonal surface [21]. In Fig. 26b, the leakage of the oxides grown with 4, 5, and 7 supercycles is instead plotted against the field applied to the MOSCAP. This shows a very promising trend as the relative leakage gets significantly better when the oxide is scaled down. This might hint that the initial supercycles are of higher quality than the last 2-3 layers.

Finally, in Fig. 27 the IV-sweeps for samples with a 275 °C solid-solution oxide and a 300 °C 5:15:5 laminated oxide can be seen. This showed promising results (maybe too promising), as the TER values for both samples were above expectations. The TER of the laminated sample undoubtedly outperformed the other samples in both sweep directions, which most likely is related to the fact that it has more ferroic crystallization. This is supported by PUND measurements on the samples (for example, see Fig. 40 in the appendix). The reason the 275 °C sample does not seem to show hysteresis in the positive sweep direction is likely related to the pinning of the domains (meaning wake-up is needed), since the field over the oxide is well above the coercive field of the sample (ε_c=1.9 MV/cm) as it reached 3.3 MV/cm. Sweeping the voltage further than this caused oxide breakdown. No other example of FTJ behaviour on InAs substrates could be found in literature. To fully understand these two oxides applicability as FTJs, the retention and endurance have to be investigated. Before this is done, it cannot be definitely stated that the hysteresis arises from the polarization switching, but could rather be caused by ”filament formation”, which is an effect that has been observed in at least solid-solution HZO [69].

7.3 PUND

Two samples from series M1 showed ferroelectric behaviour: the sample grown at 275 °C that had been subjected to low-temperature RTP, and the 300 °C sample. The fact that ferroelectricity was measured at all was surprising since no steps or strategies had been taken to achieve this other than simply increasing the ALD chamber temperature. This was a great outlook for future processing since increasing the temperature had the desired effect. Both polarization states were measured using the PUND technique at 4 V, but without wake-up cycling. This was due to the rather large leakage currents causing the oxides to suffer breakdown when subjected to essentially any high voltage wake-up (> 3.5 V). The influence that excessive leakage current can have on a PUND-measurement is well indicated in Fig. 28c, where the left side of the P-E curve is distorted due to leakage. Looking into Fig. 28d, one can see this leakage in the I-E plot as the left part of the graph is entirely distorted. At lower voltages the fields are too weak to cause switching. While the remanent polarization of both samples were rather low, it could potentially be improved upon if the oxides was of higher quality, which would allow wake-up cycling.

In series M2, where the laminate-structured HZO was adopted, almost all samples turned ferroelectric directly from the ALD chamber. The highest achieved remanent polarization for both ALD temperature and laminate structure can be observed in figure 29. The samples deposited at 300 °C appear to have had more crystallization of HfO_2 in the orthorhombic phase, since the remanent polarization is generally higher. One reason behind this might be the presence of more amorphous material in the samples deposited at 325 °C, which would also explain the electrical robustness of the samples. Here it would have been useful to perform GIXRD on the samples, in order to find the relative amount of orthorhombic phase. The samples deposited at higher temperature might also need substantially more optimization of the measurements, such as much more extensive wake-up cycling as a consequence of this. In Fig. 30, the highest polarization switching of the series is plotted, which was for the sample with the 4:12:4 laminated oxide grown at 300 °C. The associated I-E curve indicates almost no leakage, even at 4V PUND.

PUND performed on series M3 revealed some of the most promising results found in this thesis. The remanent polarization was found to be almost independent of scaling (see Fig. 31a), and even improved when going from

11.6 nm thickness of a 7 supercycle sample to 6.39 nm of a 4 supercycle sample (id:4L4i). However, the five supercycle sample (id:5L4i) did not display as high remanent polarization, which is most likely caused by differences in processing. This can, for example, be inconsistencies in the initial cleaning or the wet etch before placing the sample in the ALD chamber. Another reason might be the uncertainty of the ALD growth as the stability of the chamber temperature in the Picosun is not terribly predictable at 300 °C (which I have noticed during this project). However, the fact that the ferroelectricity scales well is very promising if you want to implement the oxide in a transistor gate stack where you want it even thinner. The scaling also suggests that maybe only a narrow part of the entire oxide stack crystallizes into the orthorhombic phase. Again, this could in the future be confirmed with GIXRD which was not within the scope of this project. The best remanent polarization appeared in the MIMCAP sample (id:7L4i(MIM)), reaching values above P_r=12 $\mu C/cm^2$ already after 1000 wake-up cycles. The fact that the MIM sample performs better than the InAs samples in terms of remanent polarization could be related to the TiN bottom interface imposing some strain that assists crystallization directly during growth, similar to its function during the standard PMA. When MOS- and MIM-CAPs are produced with high temperature PMA, InAs based MOS structures outperform the MIMs with equivalent oxides [4]. This is the opposite trend to what were observed during the study of as-deposited HZO. Interestingly, the remanent polarization observed in the MIMCAP sample almost coincides with the result from PEALD in another project [35], where solid-solution HZO had been grown to 10 nm and integrated in almost the same MIM structure as in this project, but it was also subjected to 300 °C RTP [35]. The researchers found a $2{\cdot}P_r$ value of 34 $\mu C/cm^2$, which is higher than what is observed here. However, as-deposited films in that project showed less polarization than what was observed in this project, which could be further evidence that the laminate structure assists the crystallization. The permittivity of their film was estimated with ε_r=39 using a CV-method.

The relative permittivity of all samples is summarized in table 2, with their corresponding id. This section is very speculative since the capacitive current method used to extract the permittivity is slightly inaccurate (which is why the values of table 2 is given with 0 to 1 digit precision). While the values are extracted from IV-curves from PUND that appear to show as low leakage as possible, it can be difficult to distinguish. A much better practice would be to extract the relative permittivity from CV-measurement, which I did not have time to do. For reference, if you disregard the influence of the ferroelectric polarization, the relative permittivity of pure HfO_2 is typically $\sim$ 25 [70], while for ferroelectric HZO it is usually found to be $\sim$ 30 [16]. However, if the tetragonal phase is induced in HZO, the relative permittivity can reach values of $\sim$ 43 [68]. This is associated with increased crystallization of tetragonal zirconia in the oxide, and thus the antiferroelectric phase of HZO. The boost in permittivity is believed to be related to the suppression of the monoclinic phase in the material [68]. While some of the data reported in table 2 is consistent with the expected values, some samples stand out. The values associated with series M1 are modest, but the two highest relative permittivities are consistent with the ferroelectric samples, which is expected since the other samples might contain much more monoclinic phase. In series M2 and M3, a 4:12:4 laminate MOSCAP (id:4124_325) and the MIMCAP (id:7L4i(MIM)), have significantly higher relative permittivity than the other samples and the results for the MIM coincide with other works [35]. These samples have the same laminate structure with the same number of supercycles, but are grown at different temperatures. The MOSCAP, however, did not show any ferroelectricity from PUND, meaning this result should not be trusted. The MIMCAP oxide consists of a laminate of 60 at% Zr, which puts it in the range where ZrO_2 can crystallize into its tetragonal crystal structure [16]. In essence, this might mean that more tetragonal phases might have appeared in this sample during deposition than the other laminates, but no antiferroelectric behaviour was found. Moreover, the mixed ferroic state that can be observed in 4:12:4 laminates [22] might explain why the MIMCAP can contain large amounts of tetragonal phase, while remaining ferroelectric. If these values can be confirmed, it might be possible to implement ferroelectric oxides in transistors with excellent high-k properties.

7.4 Annealing study

The initial results of the annealing study after scribing the samples from series M1 and M2 was disappointing as there was almost no improvement in remanent polarization for any samples. One reason could be insufficient optimization of PUND voltages and wake-up cycles, since less time was spent per sample (due to the sheer number of samples, 33 of them). However, another theory is that the RTP process time was simply too low for the re-crystallization to have time to occur. The six samples scribed from the 4:12:4 laminates of series M2 were therefore subjected to further RTP. While the sample originally grown at 325 °C did not turn ferroelectric at any of the RTP temperatures, even after 300 s, the sample grown at 300 °C did. In Fig. 34, PUND performed on this sample at various RTP temperatures is displayed. It can be seen that greater remanent polarization is achieved for the highest RTP temperature, but it does not outperform other reduced-RTP studies on solid-solution HZO [4]. The associated I-E plot indicate low leakage at PUND performed at 3.5V, which is promising for further wake-up optimization. The leakage for both the samples mentioned above is indicated in Figs. 35a and 35b. The data for the sample originally grown at 325 °C show weak indication that the RTP temperature is a determining factor for the leakage, as the lower RTP samples appear to perform slightly better. A similar and much clearer trend can be seen in Fig. 35a. One sample annealed at 350 °C (red line in graph) appear to have two orders of magnitude higher leakage for low voltages, but this trend disappear after an additional 300s anneal at 350 °C. This discrepancy could not be explained as the data is acquired the exact same way.

8 Conclusion and Outlook

In this master thesis, the exciting prospect of as-deposited ferroelectricity has been explored. By growing HZO oxides at elevated temperatures in a thermal ALD, the immediate crystallization of the orthorhombic phase was realized. Remanent polarization values of 2.1 and 1.5 $\mu C/cm^2$ were initially found in oxides deposited at 275 and 300 °C, respectively. The oxides grew to approximately 80% of the targeted thickness, reaching approximately 11-12 nm, but the films generally became well behaved regarding leakage (with some exceptions). To potentially increase the remanent polarization, a new engineering strategy for the pulse sequence that defines the HZO oxide was adopted. This meant the HZO thin film was structured as a laminate with supercycles that contained thicker stacks of hafnia and zirconia. This, in conjunction with further elevated temperatures led to further improvement in the as-deposited remanent polarization, reaching 6.3 $\mu C/cm^2$ for a 4:12:4 laminate sample deposited at 300 °C. Growth at 325 °C seemed to degrade the ferroelectricity, but offered improved IV-characteristics. Further investigation of the 4:12:4 laminate structure deposited at 300 °C revealed that it might offer ferroelectricity that scales well. An oxide scaled to 6.4 nm displayed a remanent polarization of 6.6 $\mu C/cm^2$. This laminate structure was also implemented in a MIMCAP, which offered the highest as-deposited remanent polarization found in this project at 12.2 $\mu C/cm^2$. Some of the samples that turned ferroelectric were also screened for basic FTJ behaviour. This was discovered in two samples, where one exhibited a suspected maximum TER of 10^3. The endurance of this film has to be investigated to confirm this is not related to filament switching. Furthermore, an additional annealing study was performed to see if the ferroelectricity could be boosted by RTP at various temperatures. The initial result was disappointing, but after a last-minute trial with extended RTP time, a remanent polarization of 14.5 $\mu C/cm^2$ was achieved after 450 °C annealing for 300s for a scribed, laminated HZO sample.

Future studies should focus on the reduction of leakage currents, and investigating the possibility of implementing these oxides in a transistor process flow. The increased thermal budget means these films offers a great pairing with InAs, and other high performance III/V semiconductors that degrade at the elevated temperatures present in the standard HZO process. For a high-performance transistor, the oxide will require further scaling, and the relative permittivity should be more accurately determined, e.g. by using a CV-method. This is essential to guarantee that the films can function as both as a variable capacitor, and a high-k dielectric. Scaling the oxide further also stresses the importance of reducing leakage currents. Performing GIXRD on the oxides could also give insight into the actual crystal phases present in all samples, which could ease further optimization. The suspected FTJ-like behaviour can also be further evaluated, and for the oxide to be implemented as a memory module or memristor, the endurance and retention needs to be characterized fully. Further anneal studies could also be performed in order to find its relation to initial ALD chamber temperatures. Finally, since laminated HZO have previously manifested apparent negative capacitance in other works, their application for steep-slope transistors should be evaluated.

9 References

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10 Appendix

10.1 Ellipsometry: Complementary Data

Some complementary data from ellipsometry for all process series in section 6.1 is presented here for the interested reader.

10.1.1 Series M1

Table 3: This table contains the thicknesses of the samples fabricated in series M1, together with the standard error of each measurement and the growth rate.

Sample id	Thickness [nm]	Standard error [nm]	Growth rate [Å/cycle]
250_noRTP	6.17	0.12	0.41
275_noRTP	11.49	0.02	0.77
275_surface	11.49	0.04	0.77
275_wRTP	11.51	0.03	0.77
275_nInAs	11.67	0.04	0.78
300_noRTP	12.12	0.20	0.81

In table 3 the thickness of series M1 resulting from ellipsometry is presented together with the standard error of each measurement and the growth rate. All these samples were grown for 150 cycles in ALD at different temperatures using the standard recipe from table 1.

10.1.2 Series M2

Table 4: This table contains the thicknesses of the samples fabricated in series M2, together with the standard error of each measurement and the growth rate.

Sample id	Thickness [nm]	Standard error [nm]	Growth rate [Å/cycle]
4124_300	11.60	0.03	0.81
5155_300	12.22	0.16	0.79
6186_300	12.66	0.06	0.82
4124_325	13.89	0.06	0.96
5155_325	13.97	0.11	0.91
6186_325	13.28	0.08	0.86

The ellipsometric result of the second series can be seen in table 4. Here the thickness, standard error and growth rates are also displayed.

10.1.3 Series M3

Table 5: This table contains the thicknesses of the samples fabricated in series M3, together with the standard error of each measurement and the growth rate.

Sample id	Thickness [nm]	Standard error [nm]	Growth rate [Å/cycle]
7l0i	11.30	0.05	0.81
7l2i	11.41	0.09	0.80
4L4i	6.47	0.04	0.77
5L4i	8.35	0.03	0.80
7L4i	11.54	0.05	0.80
7L4i (MIM)	13.09	0.18	0.91
7L6Ali	11.44	0.04	0.78

The thickness, standard error for each measurement and growth per cycle for series M3 is summarized in table 5.

10.2 IV-characteristics: Complementary Data

Some complementary IV-data for all process series in section 6.1 is presented here for the interested reader.

10.2.1 Series M1

Fig. 36a displays the (logarithmic) leakage current at 3V of all samples in series M1 for several different MOSCAP radii, while Fig. 36b displays the breakage voltages of different device sizes.

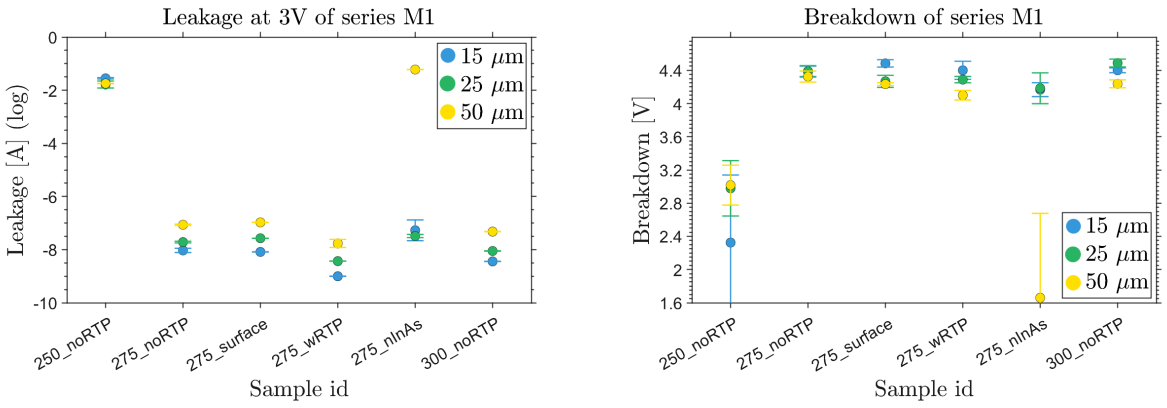
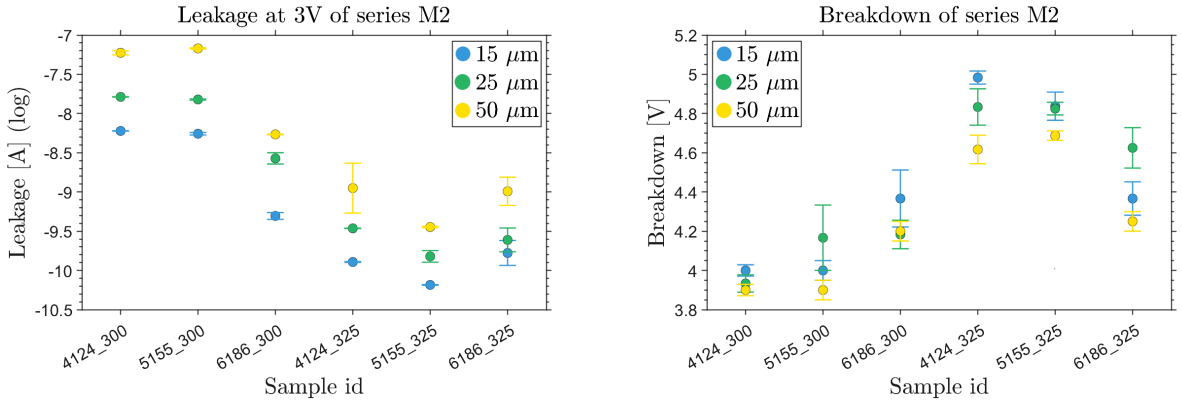


Fig. 36: (a) The leakage current (logarithmic) of each sample in series M1 for different device radii and (b) the breakdown voltage of each sample for different device radii.

10.2.2 Series M2

Fig. 37a displays the (logarithmic) leakage current at 3V of all samples in series M2 for several different MOSCAP radii, while Fig. 37b represent the corresponding breakdown voltages. This data is extracted from MOSCAPs with a contact radius of 15 μm.

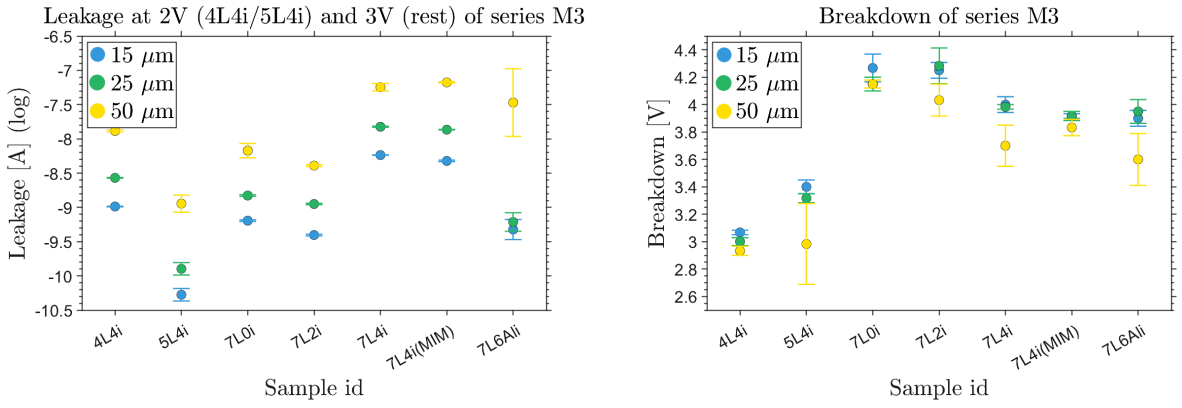


(a) (b)

Fig. 37: (a) The leakage current (logarithmic) of each sample in series M2 for different device radii and (b) the breakdown voltage of each sample for different device radii.

10.2.3 Series M3

In Fig. 38a the leakage current of all devices in series M3 is presented. The leakage is extracted for two different voltages since the thinner samples do not last for as high electric fields as the thicker ones. This means the samples with four and five supercycle have had their leakage extracted at 2 V while the rest had it extracted at 3 V. Fig. 38b indicates the breakdown voltage of all samples.



(a) (b)

Fig. 38: (a) The leakage current (logarithmic) of each sample in series M3 for different device radii and (b) the breakdown voltage of each sample for different device radii.

10.3 PUND: Complementary Data

Some complementary data from PUND for all process series in section 6.1 is presented here for the interested reader.

10.3.1 Series M1

After performing the PUND-technique on all samples of series M1, Fig. 39 summarizes the highest (measured) remanent polarization of each sample as well as the coercive fields required to achieve the switching.

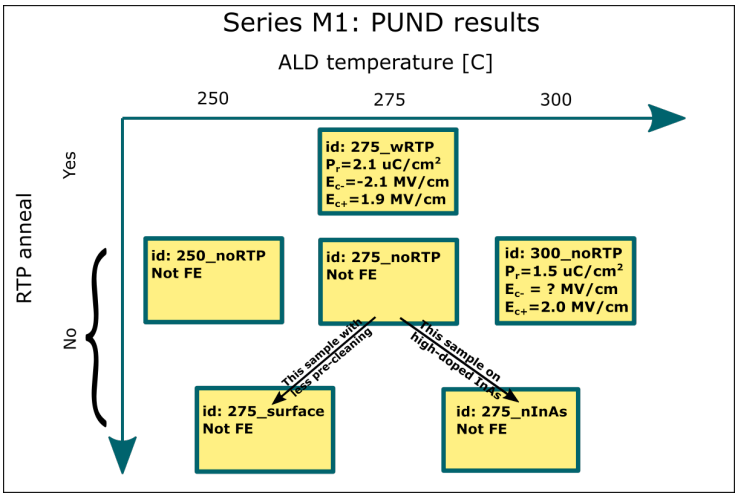


Fig. 39: This figure summarizes the highest achieved remanent polarization for series M1 together with the average coercive field for which the state switched.

10.3.2 Series M2

After performing the PUND-technique on all samples of series M2, Fig. 40 summarizes the highest (measured) remanent polarization of each sample as well as the coercive fields required to achieve the switching.

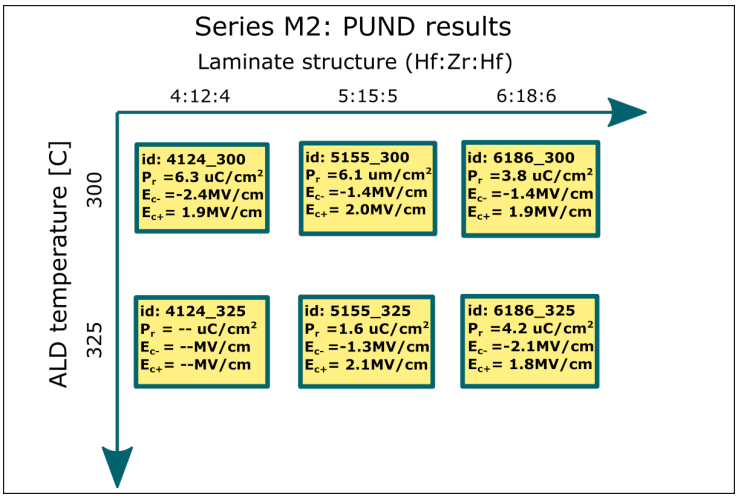


Fig. 40: This figure summarizes the highest achieved remanent polarization for series M2 together with the average coercive field for which the state switched.

In Fig. 41 the P-E graphs of the three interesting samples not included in the results are displayed. The samples have id: 5155_300, 6186_300, and 6186_325, respectively, with the corresponding I-E curve to the right can be found. The PUND pulses used to generate these graphs were:

1. Sample id: 5155_300: 3.5V PUND with 2000 wake-up cycles at 3.5V.
2. Sample id: 6186_300: 3.5V PUND with 15000 wake-up cycles at 3.5V.
3. Sample id: 6186_325: 4.5V with no wake-up cycles.

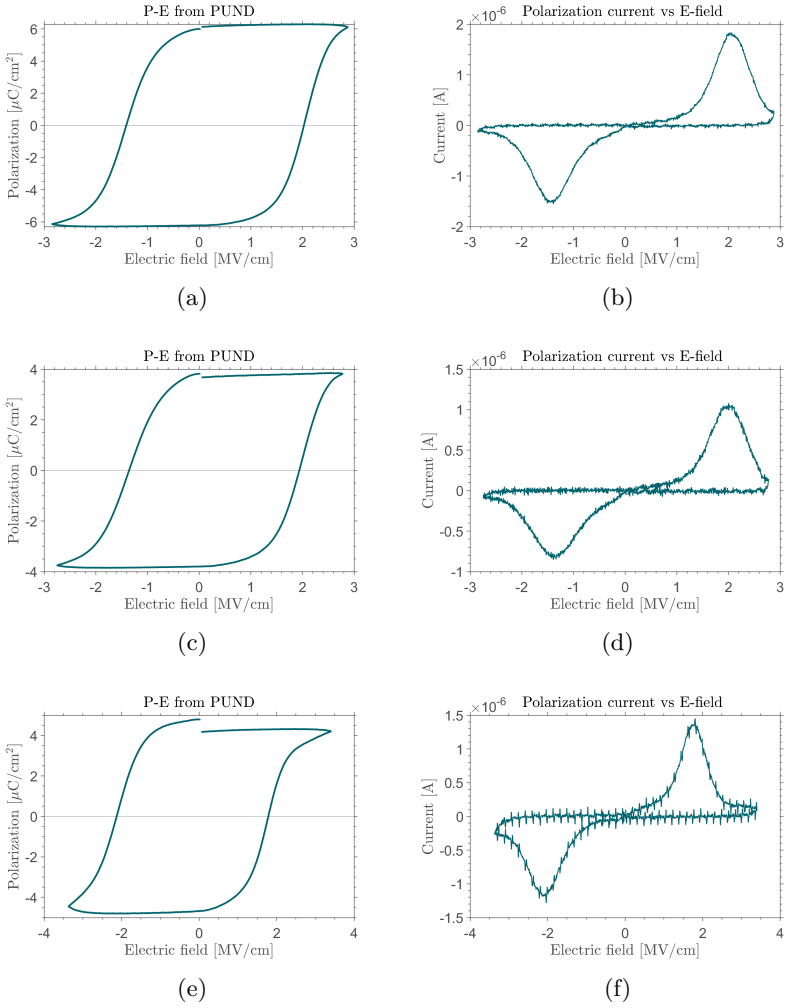


Fig. 41: (a) The P-E curve (3.5V PUND, 2000 wake-up cycles at 3.5V) with the highest remanent polarization measured in series M2 for the sample 5155_300 and (b) the corresponding switching current in an I-E plot.(c) The P-E curve (3.5V PUND, 15000 wake-up cycles at 3.5V) with the highest remanent polarization for the sample 6186_300 and (d) the corresponding switching current in an I-E plot (e) The P-E curve (4.5V PUND, no wake-up) with the highest remanent polarization for the sample 6186_325 and (f) the corresponding switching current in an I-E plot.

10.3.3 Series M3

The PUND result with the highest remanent polarization for each sample of series M3 is accounted for in Fig. 42. All samples grown with 7 supercycles have been measured using PUND at 3V, while the scaled samples have been measured with PUND at 2.5V

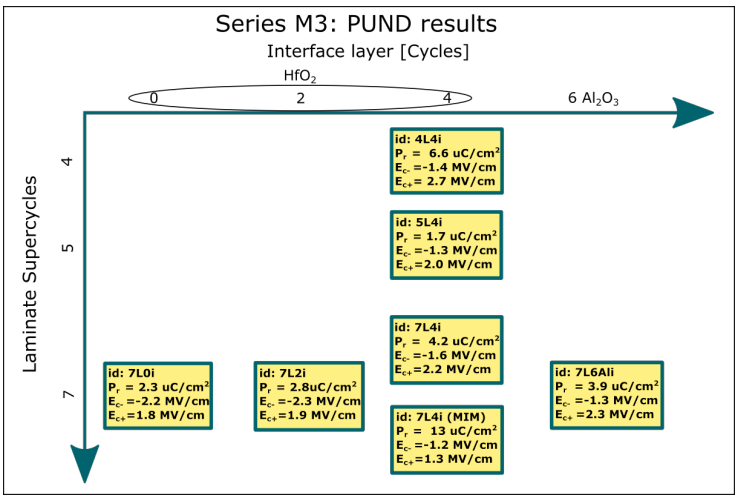


Fig. 42: This figure summarizes the highest achieved remanent polarization for series M3 together with the average coercive field for which the state switched.

Fig. 43 depicts an example of a PUND pulse train being applied to a ferroelectric oxide and the measured current that is used to calculate the polarization of the crystal domains.

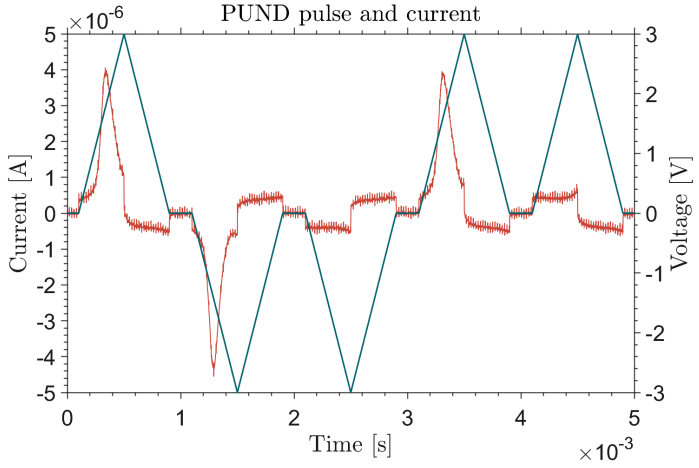


Fig. 43: This figure illustrates an example of the PUND pulse train that is applied to the oxide in order to generate P-E graphs.