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Industrial Electrical Engineering and Automation

Integrated DC fast charger in an electric vehicle

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Master Thesis

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Abstract

More and more electric vehicles are emerging with a nominal battery voltage higher than what most older DC fast chargers are capable of charging. This requires the vehicle manufacturers to include a high power DC to DC converter in order to be able to charge at these stations, adding cost and complexity. Instead, with only minor modifications of the traction system, the motor and inverter can be used as three parallel DC to DC converters, removing the need for an extra converter.

The aim is to develop, assemble and test a low voltage system that can run at about the same current level as existing charging stations. Its performance is assessed and the measured efficiency is compared to a theoretically derived one. The results are then extrapolated to a higher voltage in order to investigate its feasibility.

The system is proven to work satisfactorily at the low voltage, although with quite poor efficiency of about 80 % at around 5 kW charging. When increasing the voltage the efficiency seems promising although some concerns are raised about the increased current ripple.

Sammanfattning

Fler och fler elbilar dyker upp med en nominell batterispänning högre än vad de flesta äldre DC-snabbladdare klarar av att ladda. Detta kräver att biltillverkarna inkluderar en högeffekts DC till DC omvandlare för att kunna ladda vid dessa stationer vilket ökar kostnad och komplexitet. Istället, med små modifikationer på drivlinan, så kan elmotorn och växelriktaren användas som tre parallella DC till DC omvandlare vilket eliminerar behovet av en extra omvandlare.

Målet är att utveckla, montera och testa ett lågspänningssystem som kan köras vid ungefär samma strömnivåer som existerande laddstationer. Dess prestanda utvärderas och den uppmätta verkningsgraden jämförs med en teoretiskt framtagen sådan. Resultaten extrapoleras sedan till en högre spänning för att undersöka dess möjligheter.

Systemet bevisas fungera tillfredsställande vid den låga spänningen, dock med ganska dålig verkningsgrad på cirka 80 % vid runt 5 kW laddning. När spänningen ökar så verkar verkningsgraden lovande men vissa bekymmer tas upp med det ökade strömripplet.

Acknowledgements

We would like to thank BorgWarner for giving us the opportunity and the resources to pursue a very interesting project which is very relevant in time. A special thanks to Gabriel Dominguez and Hans Aulin for developing the concept and inviting us to work on and realize the concept. We would also like to thank the numerous amount of people that have helped us with various problems – Lucas Lindén for helping us come in contact with the right people, setting us up in the lab and supplying us with various equipment and tips, Ted Brink for making sure that we were on the right track and received the help we needed, Pierre Pettersson for lending us his knowledge and equipment, Jon Axelsson and Niklas Henriksson among others for good advice and help with physical design and manufacturing. Without all of your support, this thesis would not have been possible.

We would also like to thank our faculty supervisor at LTH, Mats Alaküla, for answering our many questions, coming with insightful thoughts and providing guidance when needed. Also, a special thanks to Getachew Darge for lending us the motor and inverter, and providing us with tips and help with the equipment on demand.

Contents

Nomenclature

ADC	Analog to Digital Converter
DIO	Digital Input/Output
EMC	Electromagnetic Compatibility
FPGA	Field-Programmable Gate Array
HDL	Hardware Description Language
IEA	Division for Industrial Electrical Engineering and Automation
IGBT	Insulated-Gate Bipolar Transistor
IO	Input/Output
MAB	MicroAutoBox
NO	Normally Open
NVH	Noise, Vibration and Harshness
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PLC	Programmable Logic Controller
PMSM	Permanent Magnet Synchronous Machine
PWM	Pulse-Width Modulation
RMS	Root Mean Square
RTD	Resistance Temperature Detector
SFC	Sequential Function Chart
TTL	Transistor–Transistor Logic

Chapter 1

Introduction

1.1 Background

Constant development in battery and powertrain technology results in more energy efficient vehicles. A natural step in reducing losses is to increase the battery voltage thus reducing the current and consequently resistive losses assuming constant power. Additionally, the lower current enables thinner conductors, although thicker isolation, with the net result of cheaper and possibly lighter cables. However, the higher voltage derivative means that EMC will be of greater importance and the machine winding insulation also degrades faster.

Charging these higher voltage batteries using the existing DC fast charger network is not trivial since the majority of the charging stations are not able to supply the higher voltage. This requires some form of transitional solution until enough fast chargers can supply the higher voltage. One solution is to include an on-board high power DC to DC converter only used to charge at the existing stations. Although, this increases cost and mass as well as complicating the packaging of the vehicle. Instead, it is possible to use the existing motor and inverter, normally used for propulsion, together with a few additional components as a DC to DC converter assuming the neutral point of the machine is accessible.

The Porsche Taycan from 2019 was one of the first electric vehicle to utilise an 800 V system [1]. It uses a separate converter to boost the voltage when charging at 400 V, which is normally the limit of the older stations. Additionally, the newly released Audi e-tron GT uses the same J1 platform as the Porsche Taycan thus also use an 800 V battery [2]. In 2021 Hyundai Motor Group started to manufacture cars based on their E-GMP platform; the Hyundai Ioniq 5, Kia EV6 and Genesis GV60 [3]. The platform uses an 800 V battery and a system very similar to the one presented in this thesis which can use the motor and inverter to boost the voltage from 400 V to 800 V [4]. There are also some low volume manufacturers such as Lucid and Rimac who also produce 800 V cars and handful of Chinese manufacturers that are planning to use 800 V [5, 6, 7]. Almost all 800 V vehicles promises over 300 kW charging power at 800 V chargers, whereas the older fast chargers are usually limited to around 150 kW. One of the limiting factors is the heat generation in the plug.

BorgWarner strives to offer cost-effective and complete solutions for hybrid and electric vehicles. As more OEMs adopt 800 V systems, BorgWarner want to investigate a system without the dedicated converter.

1.2 Project aims

The aim of the thesis is to develop, assemble and test a 24 V to 48 V DC to DC converter that makes use of an electrical machine and an inverter according to Fig. 1.1. The currents will be about the same as for a high power DC charger. The feasibility of a higher voltage system will also be investigated based on the results.

A first prototype will be developed that can be used as a reference if BorgWarner wants to develop a higher voltage variant in the future. Further insight in integrated DC chargers will be gained as well as correlation between loss modelling and measurements.

The main challenges include choosing and sizing components, designing and assembling the system as well as developing control.

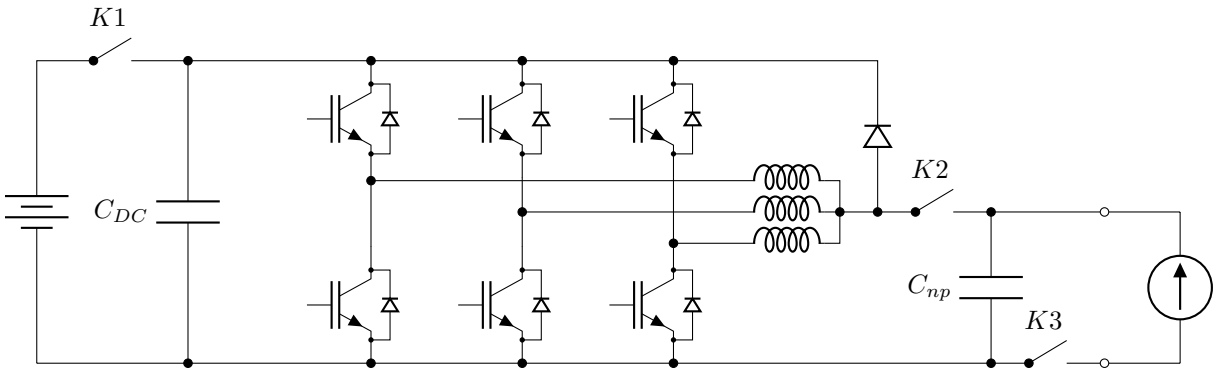


Fig. 1.1. Proposed circuit diagram from BorgWarner with the battery to the left, the six inverter switches, three phase windings in the machine, the charging station to the right as well as a bypass diode used when the station is capable of charging the battery without the boost converter.

1.3 Methodology

The main approach will be to develop a simulation model in Simulink, including control, to estimate the performance before assembling the system. The model will be based on the main differential and algebraic equations using parameters extracted from data sheets as well as measurements of the chosen components. For simplicity the switching losses in the transistors are not modelled.

Worth mentioning is that the simulations and choice of components are not done in a sequential way, but rather two tasks done in parallel. It is partly an iterative process were the component needed is largely specified, then the component is checked for availability, either if it is available in-house or available for order, then more simulations are done to evaluate the component.

The main components of the system will be a 48 V Semikron inverter which includes gate drivers and sensors, a dSpace MicroAutoBox used for control and interfacing with the gate drivers, an electrical machine where the neutral point is easily available and two Regatron bidirectional, high current, power supplies to act as charging station and battery. The three phases of the machine will act as the inductors in three parallel converters, one in each phase leg of the inverter. The control algorithm will be developed in Simulink together with third-party blocks from dSpace in order to be able to interact with inputs and outputs as well as directly compile and download the program to the MicroAutoBox.

The efficiency will be estimated using a set of relatively simple equations in order to be able to compare the result to the measured one as well as extrapolate an efficiency for a higher voltage system.

During the physical tests the efficiency will be measured, using a power analyzer, on each side of the circuit and the difference between the two will be used as a measurement of the losses in the system. The effect of changing the switching frequency and interleaving the carrier waves will be studied. No absolute measurement will be used for the vibrations, but a description of the apparent noise and vibration will be included. Additionally, techniques to reduce the input and output current ripple are evaluated. The conclusions from the tests combined with the estimates will then be used to extrapolate the performance and feasibility of a future high voltage system. The low voltage system will be run at roughly the same current as the high voltage system would during realistic charging in order for the results to be more representative.

Chapter 2

Modeling

2.1 Power electronic converter

The conventional three-phase, two-level voltage source converter consists of three pairs of transistors, also called phase legs, each with an anti-parallel diode. The upper or lower transistor in each leg is switched on in order to produce a desired average phase potential [8, ch. 8]. If the neutral point of the three-phase inductive load is connected to the negative pole of the DC link through a source it is possible to run bidirectional current in each phase separately and thus operate them as parallel two-quadrant converters.

2.1.1 Modulation

To produce the control signals for the transistors a modulator is used. It compares a high frequency sawtooth or triangular wave, called the carrier wave, to a reference which generates a pulse-width modulated (PWM) signal as seen in Fig. 2.1. As to not short circuit the phase leg, the generated PWM signal is applied to the upper transistor and its logical inverse to the lower transistor. An extra delay called dead time or blanking time is applied to the rising edges of the PWM signals to accommodate for the time it takes to turn off and on the transistors.

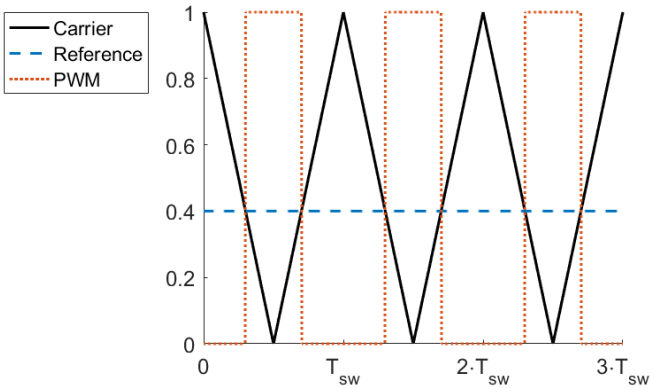


Fig. 2.1. PWM generation where T_{sw} is the switching period.

2.1.2 Interleaving

When controlling parallel converters connected to the same DC link and load, a common technique is to phase shift the carrier waves for each controller, also know as interleaving, in order to reduce the total input and output current ripple [9, 10, 11].

While operating the three parallel boost converters it is convenient to run equal amount of current in each phase to distribute the heat generation, as well as minimizing the torque produced on the motor shaft. If the carrier waves are synchronized, each phase will contribute roughly the same

amount of current during the same time interval. This means that the inverter outputs between between zero and three times the phase current to the DC link as seen in Fig. 2.2a. The worst-case RMS current through the capacitor is at 50 % duty cycle assuming it compensates for the entire ripple. Thus, the worst-case RMS value of the capacitor current is approximately 1.5 times the phase current. If, however, the carrier waves are interleaved, that is they are phase shifted 120 degrees, the current contribution from each phase to the DC link is seen in Fig. 2.2b. This means that the capacitor only needs to compensate for approximately 0.5 times the phase current in worst-case. This also assumes that the inductors are decoupled which is not entirely true in a machine. Additionally, the fundamental frequency of the total input and output current is three times higher as it is a sum of three evenly phase shifted signals. In reality the DC link will not compensate for the entire ripple current. But, since using interleaving increases the fundamental frequency the impedance to the capacitors are decreased thus take more ripple current. Additionally, the ESR generally decreases when the frequency is increased, thus the capacitor can take slightly more ripple current while not overheating. A downside with interleaving is that the ripple currents in the phases are not synchronized and will thus produce a small rotating magnetic field in the machine and potentially causing more mechanical vibrations.

2.1.3 Capacitor stress

When running a machine with high power factor, for example a permanent-magnet AC machine, the worst-case current stress on the DC link capacitor can, according to [12], be approximated by

$$I_{C,rms} = \frac{1}{\sqrt{2}} I_{N,rms} \tag{2.1}$$

where $I_{C,rms}$ is the capacitor current and $I_{N,rms}$ is the phase current. The capacitor is also assumed to supply the entire ripple current.

As mentioned in section 2.1.2 the current stress on the capacitor is approximately three times larger if interleaving is not used. Using this together with (2.1) gives an approximation of the phase current needed to give the same worst-case capacitor stress. Thus, running a phase current without interleaving of $\sqrt{2}/3 \approx 0.47$ times the rated phase current in motor drive gives roughly the same current stress on the capacitor. If, however, interleaving is used the same current stress on the capacitor is experienced when running $\sqrt{2} \approx 1.41$ times the rated motoring phase current. Therefore, if the DC link capacitor is dimensioned according to [12] and interleaving is not used, one has to reduce the phase current from the rated one in order to not overheat it.

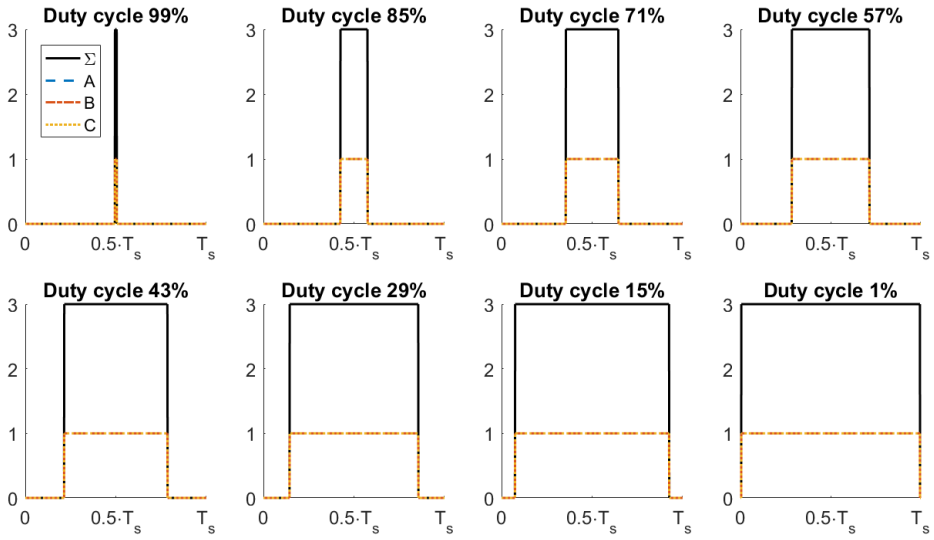
2.2 Control design

The designed control system consists mainly of a state machine that determines which contactors should be closed and what current reference to use, three current controllers, one for each phase, a modulator as well as a lot of analog to digital converters (ADC) and digital input/output (IO). The variables used in the equations in section 2.2 and 2.3 can be seen in Fig. 2.3.

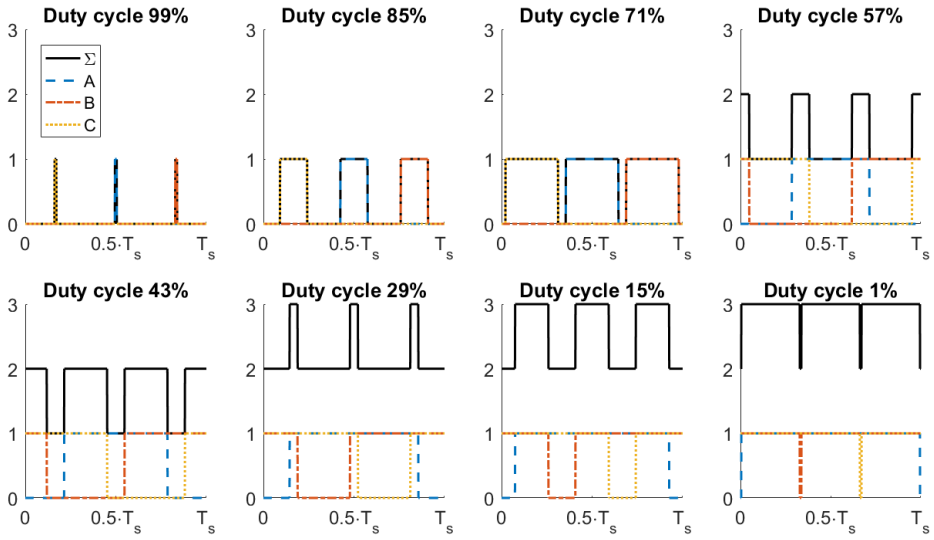
2.2.1 State machine

The designed state machine contains the states *Wait*, which is the initial state and initializes all contactors to open, *DC link Precharge*, which enables contactor $K1$ after the DC link capacitor, C_{DC}, has been precharged through a resistor, *Neutral point Precharge*, which enables $K2$ connecting the machine's neutral point and the filter capacitor, C_{np}, and precharges it through the inverter from the battery, *Boost mode*, which enables $K3$ connecting C_{np} to the charging station and allows for battery charging, and finally *Discharge neutral point*, which disables $K3$ and discharges the input capacitor through the inverter at the end of a charging session. The majority of the time is spent in the *Boost mode* state.

A version of the state machine implemented in sequential function chart (SFC) can be seen in Fig. 2.4. Using SFC is a common way to implement more complex state machines on programmable logic controllers (PLCs) although it is not available in Simulink thus only used for illustration purposes. The state machine in the Simulink model is implemented using set-reset latches and conditionally enabled subsystems.



(a)



(b)

Fig. 2.2. Idealized inverter DC link current normalized by the phase current together with each phase contribution during a switching period. The currents are given for different duty cycles of the lower transistor (a) without and (b) with interleaving. Note the large inductor time constant for illustration purposes.

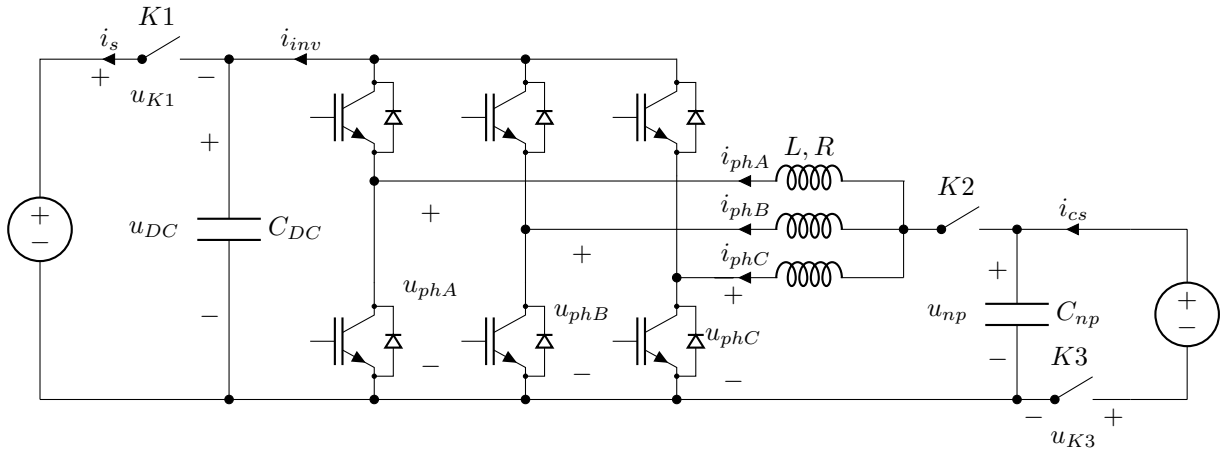


Fig. 2.3. Circuit diagram of the main circuit and the quantities used for control and in simulation.

2.2.2 Current controller

The phase current controllers are PI controllers with feedforward based on [13, ch. 3] given by

$$u^*_{ph,i}(k) = \left(\frac{L}{T_s} + \frac{R}{2}\right) \cdot \left(\left(i^*_{ph,i}(k) - i_{ph,i}(k)\right) + \frac{T_s}{\left(\frac{L}{R} + \frac{T_s}{2}\right)} \cdot \sum_{n=0}^{k-1} \left(i^*_{ph,i}(n) - i_{ph,i}(n)\right) \right) + u_{np}(k) \quad (2.2)$$

where $u^*_{ph,i}$ and $i^*_{ph,i}$ is the average phase voltage reference and phase current reference, $i_{ph,i}$ is the measured phase current, L is the phase inductance, T_s is the sampling time, R is the phase resistance and u_{np} is the voltage at the neutral point. The sampling frequency is usually either equal to or twice the carrier wave frequency and synchronized in such a way as to sample the quantity in the middle of the ripple. This is ideally when the carrier wave turns.

The given controller is a dead beat controller which means that it ideally eliminates the error in one sampling period. But, this gives a very aggressive controller and with parameter uncertainties, measurement noise as well as delays from execution and propagation time it necessitates the gains to be turned down. The performance requirements are quite low as the time scales are relatively long when charging so gains can be turned down to improved robustness. Although, reducing them too much will mostly affect the performance of the precharge and discharge of the neutral point capacitor as the current is relatively small.

The average phase voltage can not be higher than the available DC link voltage or lower than zero. This saturation can be modelled and integral anti-windup is employed by means of back-calculation [14, ch. 3.5]. This means that an additional term is added to the controller in (2.2) given by

$$\frac{T_s}{T_t} \cdot \sum_{n=0}^{k-1} \left(\text{sat}\left(u^*_{ph,i}(k)\right) - u^*_{ph,i}(k)\right) \quad (2.3)$$

where T_t is a time constant and sat() is a function that limits the argument between the DC link voltage and zero. A common value for T_t in a PI controller is the integral time constant in (2.2), thus $T_t = \frac{L}{R} + \frac{T_s}{2}$.

2.2.3 Boosting

While charging each phase current reference is derived from a desired battery current according to (2.4) where u_{dc} is the measured DC link voltage, i^*_s is the battery current reference and u_{np} is the measured neutral point voltage. But, due to the open-loop control of the battery current together with losses in the system the measured battery current will always be smaller than the desired. In order to minimize the discrepancy the losses can be estimated, as done in section 2.4, and compensated for by increasing each phase current reference by means of P_{loss}. Alternatively, a cascaded PI controller can be used to make sure the battery current is equal to the reference.

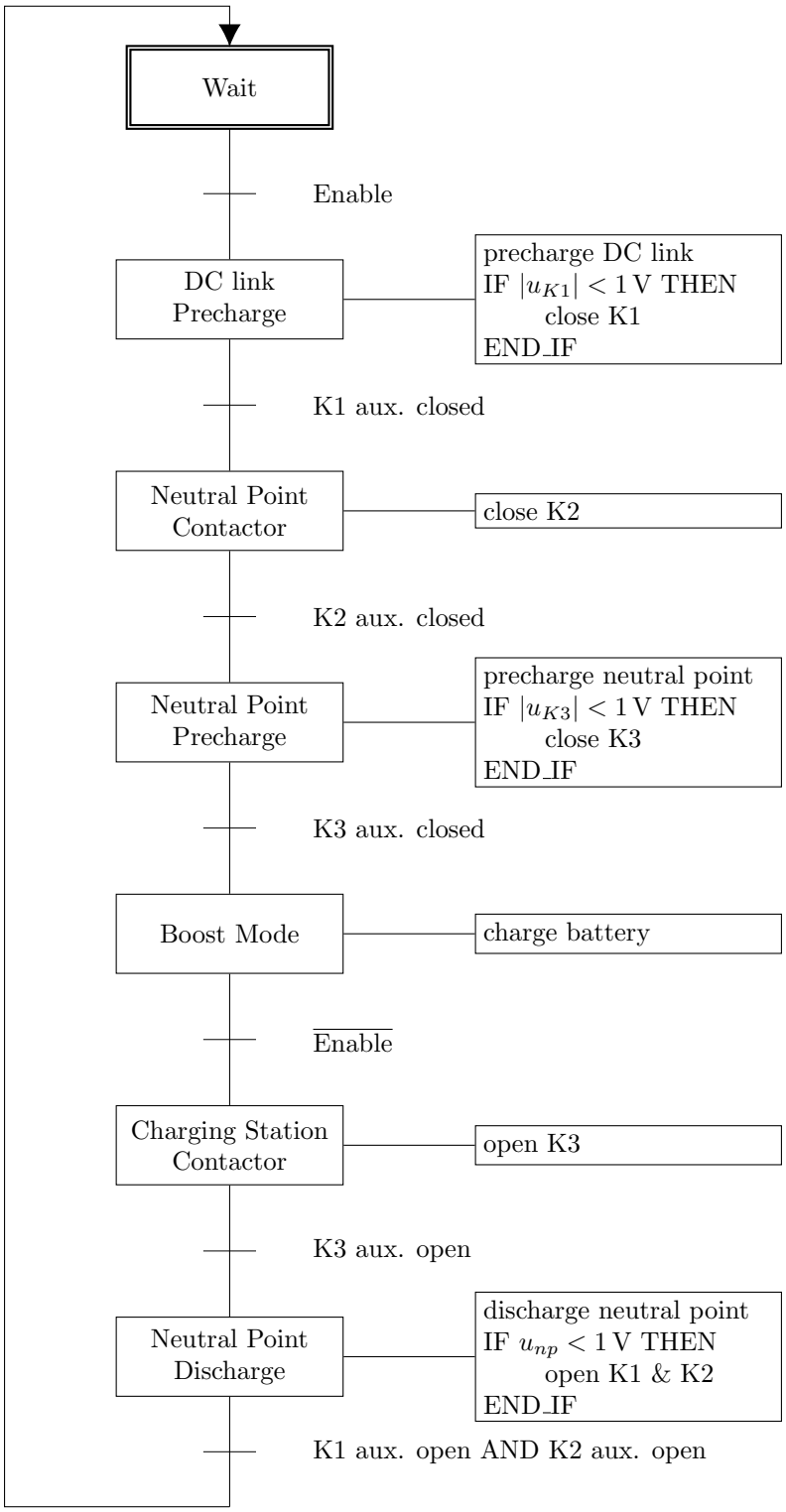


Fig. 2.4. The state machine implemented in SFC including some pseudocode. Note the two extra *Contactor* steps to make sure the contactor is closed or opened.

Only the resistive losses in the windings are compensated for in this project as the discrepancy was not seen as a problem.

$$i^*_{ph,i}(k) = \frac{1}{3 \cdot u_{np}(k)} \cdot \left(u_{dc}(k) \cdot i^*_s(k) + P_{loss}(k)\right) \tag{2.4}$$

2.2.4 Precharge and discharge

The precharge of the DC link is done without external control and is further explained in section 3.1.1.1. It is also not actively discharged except for a bleeder resistor and when the emergency stop is pressed, as explained in section 3.1.1.4.

Precharging and discharging the capacitor connected to the machine's neutral point is done by running a small current in each phase through the inverter. The current reference for each phase is derived from a P-controller given by

$$i^*_{ph,i}(k) = K_p \cdot \left(u^*_{np}(k) - u_{np}(k)\right) \tag{2.5}$$

where u^*_{np} is the neutral point voltage reference, u_{np} is the measured voltage at the neutral point and K_p is the proportional gain which is empirically tuned. The main reason for using a controller instead of a fixed current is to not overshoot the target voltage or undershoot zero voltage while precharging or discharging. Additionally, the voltage reference is a ramp function from either the currently measured voltage to the voltage of the charging station or from the measured voltage to zero with a rise and fall time of about one second. Starting from the currently measured voltage as well as using a ramp function is to avoid steps in reference signal which could introduce unnecessary oscillations.

2.3 Converter simulation

To be able to sanity check the phase current controllers and the precharge/discharge control for the neutral point capacitor a simple simulation model is made in Simulink. The model is based on the differential equations for the phase inductances, although uncoupled, as well as a the DC link and neutral point capacitors, seen in (2.6) through (2.8). The variable $u_{ph,i}$ is the phase voltage which is derived from the equivalent circuits in Fig. 2.5 through 2.8 depending on the switch states and current direction, r and V_0 is explained in section 2.4.2. The inverter current, i_{inv}, is the sum of the phase currents conducted through the upper diode or transistor in each phase leg. Additionally, i_s is the current to the battery and i_{cs} is the current from the charging station. They are given by the difference between their respective source voltage and capacitor voltage divided by the impedance. The special case when the phase current is zero and neither of the switches is on is handled separately and sets the phase voltage to the neutral point voltage. Note that the model neglects switching losses and capacitor losses and is thus not suitable for efficiency estimations.

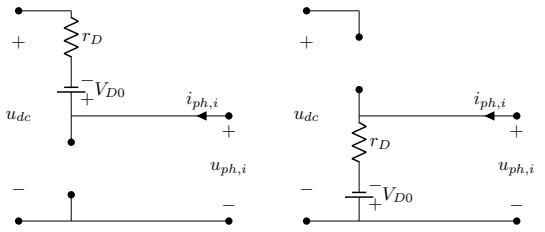
The model assumes that the impedance between the battery and DC link capacitor is only the internal battery resistance. Additionally, the impedance between the neutral point and charging station is only modelled as a small cable resistance, thus the capacitor at the neutral point has little effect when the contactor to the charging station in closed. The amount of ripple current the capacitors supply is thus underestimated as the inductance to each supply not simulated. This means that the voltage ripple in reality will be a bit higher but as the controller is not on the edge of stability it is assumed to perform satisfactory if the current controller gains are reduced slightly.

Further, the model contains a state machine presented in section 2.2.1, three phase current controllers presented in section 2.2.2 and three modulators presented in section 2.1.1 to convert the average phase voltage reference to PWM switch signals.

$$L\frac{di_{ph,i}}{dt} = u_{np} - u_{ph,i} - R \cdot i_{ph,i} \tag{2.6}$$

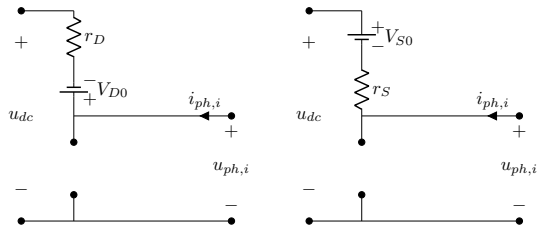
$$C_{DC}\frac{du_{dc}}{dt} = i_{inv} - i_s \tag{2.7}$$

$$C_{np}\frac{du_{np}}{dt} = i_{cs} - \sum_i i_{ph,i} \tag{2.8}$$



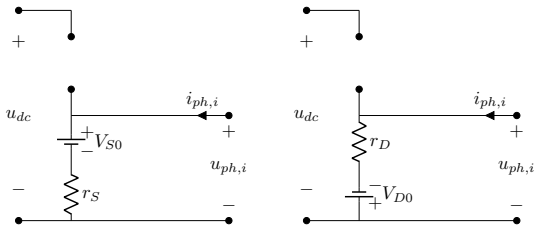
(a) $i_{ph,i} > 0$ (b) $i_{ph,i} < 0$

Fig. 2.5. Equivalent circuits when both IGBTs are off for both current directions.



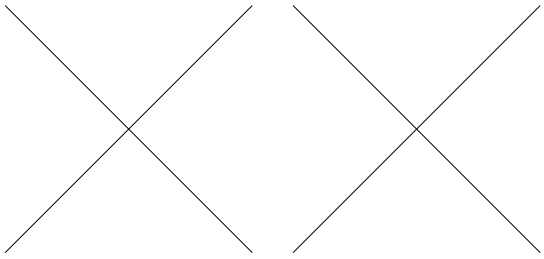
(a) $i_{ph,i} > 0$ (b) $i_{ph,i} \leq 0$

Fig. 2.6. Equivalent circuits when the upper IGBT is on for both current directions.



(a) $i_{ph,i} \geq 0$ (b) $i_{ph,i} < 0$

Fig. 2.7. Equivalent circuits when the lower IGBT is on for both current directions.



(a) $i_{ph,i} > 0$ (b) $i_{ph,i} < 0$

Fig. 2.8. The case with both IGBTs on is not allowed as it would result in a short circuit.

2.4 Losses

To be able to extrapolate the efficiency of the system the losses in each component are modelled according to simple equations. The theoretical efficiency is compared to the measured one to validate it in order to then be able to estimate a theoretical efficiency when the voltage is increased. The losses are derived from voltages, currents and the duty cycle pairings measured during the tests as the simulation model is not detailed enough.

2.4.1 Machine losses

The majority of the losses in an electrical machine can be divided into copper, core and mechanical losses. The copper losses are a result of the resistance of the windings and are modelled by

$$P_{cu} = 3 \cdot R \cdot I^2 \tag{2.9}$$

where R is the resistance of one phase winding and I is the RMS value of the phase current. The core losses are a result of the rapidly changing magnetic field in the iron. But, since the current and thus the generated magnetic field is only changing with the current ripple they are neglected. The mechanical losses are mostly due to friction and air resistance and are thus also neglected since the machine is assumed to not be rotating.

2.4.2 Inverter losses

The inverter losses are modelled by conduction and switching losses in the transistors and diodes. Both components possess nonlinear output characteristics and are thus linearized on the general form $V = V_0 + rI$ where V_0 and r are usually given in the transistor and diode datasheet. The average conduction losses are then given by

$$P_{cond} = V \cdot I \cdot D \tag{2.10}$$

where V is the voltage across the diode or switch from the linearization, I is the average phase current and D is its duty cycle. The switching losses are given by

$$P_{sw} = \frac{E_n}{V_n \cdot I_n} V \cdot I \cdot f \tag{2.11}$$

where E_n is the switching energy when operated at the voltage V_n and current I_n, V and I is the operating point at which the losses are to be estimated and f is the switching frequency. For the transistor the switching energy includes turn-on and turn-off energies, usually given as E_{on} and E_{off} in the datasheet, and for the diode it includes the reverse recovery energy, often given as E_{rr}. The total inverter losses are then given by

$$P_{inv} = 3 \cdot P_{S,cond} + 3 \cdot P_{S,sw} + 3 \cdot P_{D,cond} + 3 \cdot P_{D,sw} \tag{2.12}$$

where subscript S is the transistor losses and subscript D is the diode losses.

2.4.3 Capacitor losses

The capacitor losses are modelled by

$$P_{cap} = R \cdot I^2 \tag{2.13}$$

where R is the equivalent series resistance (ESR) and I is the RMS current. The capacitors are assumed to supply the entire ripple current for simplicity.

Chapter 3

Prototype design

3.1 System overview

A plethora of circuit designs and other design decisions have been made, most of which can be seen in appendix A. A selection of these are also seen and explained in this section. The complete setup used for higher current testing is seen in Fig. 3.1.

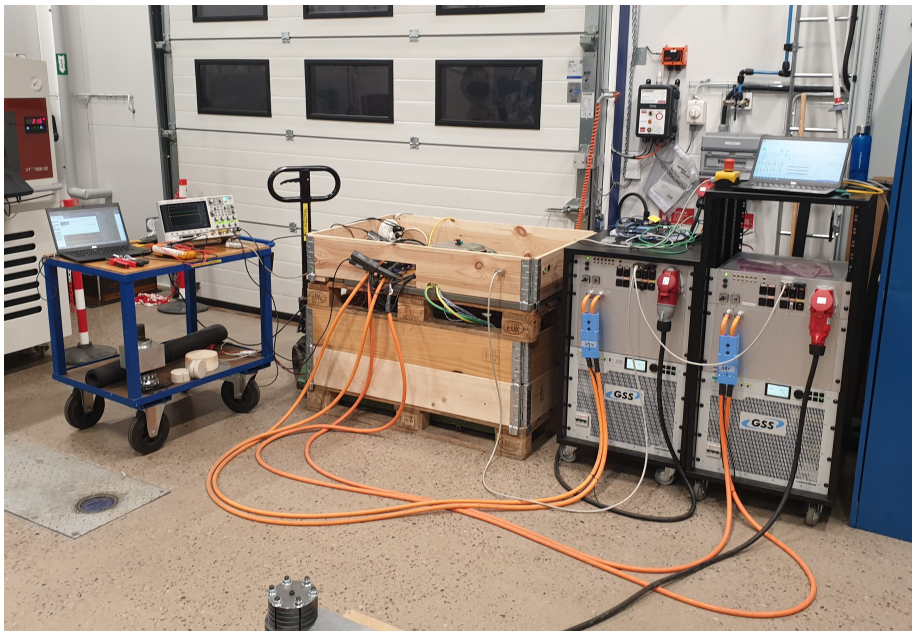


Fig. 3.1. The experimental setup with two Regatron power supplies to the right and the pallet containing the system in the middle.

3.1.1 Components and peripheral circuits

3.1.1.1 Contactors

In the testing setup, three disconnecting contactors, K1 through K3, were used. These were implemented to be able to disconnect the power sources, using K1 and K3, as well as the motor, using K2, when it is used as a traction device.

The specifications for the contactors in this thesis were not strict and the main characteristics considered were the current and voltage capability as well as price. The two types that were used can be seen in Table I.

The Schaltbau contactor was sourced from a previous project which had an additional peripheral circuit, see Fig. A.1, adding a precharge circuit which precharges the secondary side through a power

TABLE I
CONTACTOR SPECIFICATIONS

Name	Current Rating	Voltage Rating	Type	Contactors
Schaltbau C310S 500 24l V1	500A	60V	1 Pole, NO, aux	K1
Kilovac LEV200 H4ANA	500A	900V	1 Pole, NO, aux	K2 and K3

resistor and only closing the contactor when the voltage drop across it is less than 1 V. The Schaltbau also implements a built in economizer circuit, minimizing the current drawn after the contact is closed. The whole system was built into a metal box, see Fig. 3.2, which could be interfaced by using D-sub hybrid connectors. The contactor box was slightly modified to allow a digital 12 V signal from the contactor's auxiliary switch to be read. It also included two emergency stop inputs that both required 12 V in order for the contactor to be able to close.

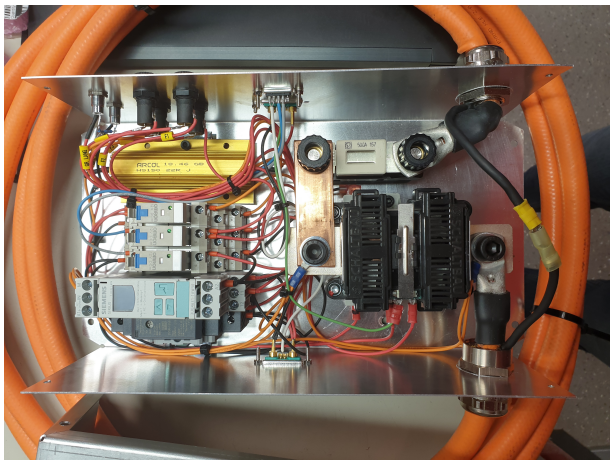


Fig. 3.2. Contactor box without lid designed for a previous project at BorgWarner including a power resistor, voltage measuring relay, relays for emergency opening of contactor and fuses.

The Kilovac contactors were bought new and with far higher voltage ratings than needed. The main reason being the scarce supply of high current and low voltage contactors. Although the high voltage rating is unnecessary it is not an issue in this project. The rated coil voltages of the Kilovac contactors are 12 V and they do not implement an internal economizer.

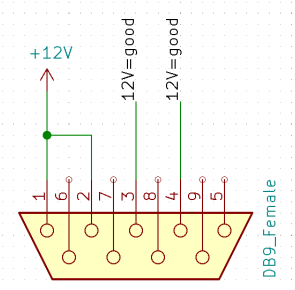
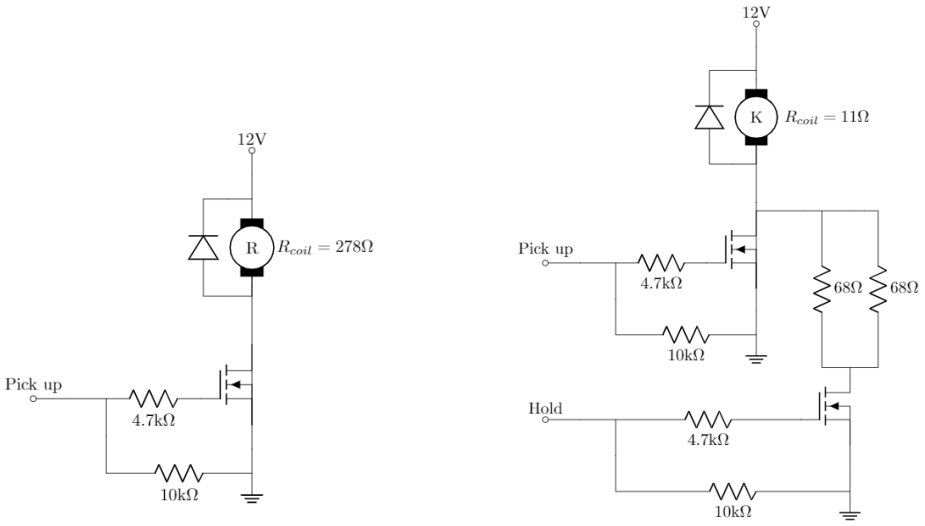


Fig. 3.3. Emergency stop connector of contactor box.

3.1.1.2 Amplifiers

As the micro controller used in this thesis was operating at 5 V TTL level as well as having a limited current sourcing/sinking capability, three peripheral circuits were needed to control the contactors. One for controlling the Schaltbau within the contactor box, and two for the Kilovacs with economizing capability.

To control the contactor box, one of the emergency stop inputs was used, see Fig. 3.3. When 12 V is supplied to both pin 3 and 4 the precharge circuit is activated and the Schaltbau contactor is turned on appropriately. When either of the pins loses 12 V both the precharging and the contactor is turned off. By controlling a relay connecting one of the pins to the 12 V pins, the contactor box activation could be steered externally. As mentioned previously the voltage and current available from the micro controller was limited and since the relay utilized was requiring a coil voltage of 12 V, an amplifier circuit was made. See circuit schematic in Fig. 3.4a.



(a) Amplifier circuit controlling a relay which in turn controls K1.

(b) Amplifier circuit controlling contactors K2 and K3 with economizer functionality.

Fig. 3.4. Amplification circuits for controlling contactors with the micro controller.

To control the Kilovac contactors K2 and K3, a similar circuit was designed and soldered, see Fig. 3.4b. This circuit got the addition of an economizer consisting of resistances in series with the contactor coils. An economizer circuit using PWM signals from the micro controller was considered but not pursued as this circuit is sufficient for restricting current and the losses were not of great concern in the peripheral circuits.

3.1.1.3 Capacitors

Initially, two sets of capacitor banks were expected to be used, one on the DC link included in the inverter and one as a filter capacitor placed at the neutral point in order to stabilize the voltage and reduce the amount of harmonics pulled from the charging station. To dimension the neutral point capacitor an initial current ripple estimation through each motor phase was made. The phase inductance was assumed to be 1 mH based on the data from the PhD thesis in which the motor was designed [15]. This resulted in a theoretical current ripple of 1.5 A per phase. The ripple current is triangular thus the RMS current in the capacitor is roughly $3 \cdot 1.5/2/\sqrt{3} \approx 1.3$ A. The capacitor type that is widely available at BorgWarner has a current ripple rating of 10 A and a capacitance of 10 mF meaning there was a large safety margin. But, due to uncertainties in the inductance while running common mode currents, as well as uncertainties in the impedance to the power supply, three of these capacitors are used in parallel resulting in a total capacitance of 30 mF at the neutral point. The specifications of all capacitors can be seen in Table II.

As seen in section 3.4, the apparent inductance when running common mode currents was actually closer to 0.19 mH resulting in a ripple current of 8 A peak to peak per phase. This means that the RMS capacitor current is at most $3 \cdot 8/2/\sqrt{3} \approx 6.9$ A thus a single capacitor should have been enough.

The currents through the DC link capacitors are much harsher than that of the neutral point capacitors as the DC link capacitors must supply or sink current in the magnitude of the DC current reference (without interleaved switching) depending on the switch states of the inverter switches. Due to the insufficient current ripple rating of the RIFA capacitors in the inverter an additional capacitor bank in the form of a Semikron inverter was connected to the DC link with as short cables

as possible to minimize the inductance between the capacitor and the DC link. The extra inverter can be seen in Fig. 3.8 under section 3.1.1.6.

TABLE II
CAPACITOR SPECIFICATIONS

Name	Capacitance	Max Ripple	ESR	Voltage	Type
Kemet ALS30	10 mF	10 A	28 mΩ	100 V	Aluminum Electrolytic
RIFA PEH200	3.3 mF	36 A	26 mΩ	400 V	Aluminum Electrolytic
Semikron SKAI2LV internal	25 mF	N/A	N/A	100 V	Electrolytic

3.1.1.4 Emergency discharge resistances

As part of a safety measure described in section 3.2, two emergency discharge resistances were installed as to empty the capacitors from charge when the system was not in use as well as when the emergency button was pressed. In order for the voltage to drop to less than 1 V for both the 48 V side as well as the 24 V side, it would take 3.9 and 3.2 time constants respectively according to (3.1) through (3.3).

$$V_0 e^{-t/\tau} = V \tag{3.1}$$

$$48e^{-t/\tau} = 1 \quad \Rightarrow \quad t \approx 3.9\tau \tag{3.2}$$

$$24e^{-t/\tau} = 1 \quad \Rightarrow \quad t \approx 3.2\tau \tag{3.3}$$

Two Arcol power resistors with a resistance of 10 Ω and 12 Ω, with a continuous power dissipation capability of 100 W and 50 W respectively, were selected since the discharge time, given by (3.4) through (3.6), from full charge was deemed adequate. The power ratings were overdimensioned as the energy stored in the capacitors is relatively small at these voltages.

$$\tau = RC \tag{3.4}$$

$$\tau = 10 \cdot 31.6 \cdot 10^{-3} = 0.316 \quad \Rightarrow \quad t = 3.9\tau = 1.23\,\text{s} \tag{3.5}$$

$$\tau = 12 \cdot 30 \cdot 10^{-3} = 0.36 \quad \Rightarrow \quad t = 3.2\tau = 1.15\,\text{s} \tag{3.6}$$

3.1.1.5 Current sensors

Two extra current sensors were used, seen in Fig. 3.5, in addition to the two integrated in the inverter built within the Division for Industrial Electrical Engineering and Automation (IEA). These were initially obtained with the purpose of logging the currents from the power supplies. However, due to the fact that the IEA inverter only contained two phase current sensors, instead of the three that were present in the inverter initially intended to use, one of the extra current sensors was repurposed and used as an external phase current sensor instead.

Since the initial use case was only logging and not control, the specifications was not ideal for measuring lower currents with high accuracy. Before early testing was performed, some concern was raised of the noise and sensitivity of the current sensor. Although the sensor was not ideal, early testing confirmed it was sufficient for the purpose of this thesis.

To measure the input and output current when using a power analyzer, two high precision current sensors was used. All current sensors used can be seen in Table III.

TABLE III
CURRENT SENSOR SPECIFICATIONS

Name	Primary Current	Accuracy	Output	Type	Placing
LEM HAS 400-S	400A	±0.4%	Voltage	Hall effect	External
LEM LA 200-P	200A	±1%	Current	Hall effect	Inverter internal
LEM ITN 600-S	600A	±0.00173%	Current	Hall effect	Power Analyzer

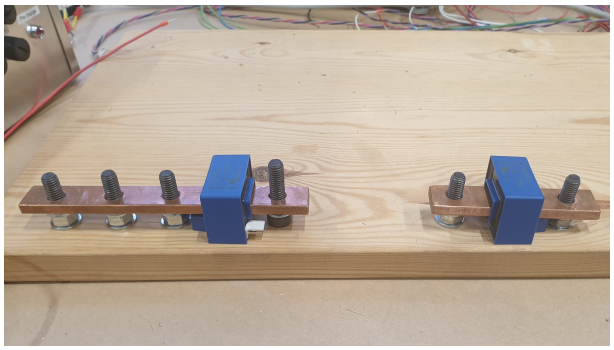


Fig. 3.5. External current sensors on busbars. The bolt heads are countersunk and isolated using hot-melt adhesive (hot glue) on the underside.

3.1.1.6 Mounting

All small loose components and peripheral circuits were mounted on a wooden plank. The relays and other equipment supporting the standard was mounted on DIN rails as to keep everything more organized. Throughout most of the project, nothing was permanently decided and component placing and choice were subject to change. This resulted in a final setup where many cables were crossing each other. To contain everything and make the setup compact and easy to move, everything has placed on a pallet stack, as seen in Fig. 3.6. The motor and inverter were placed on the lower pallet, while the micro controller, contactor box and the rest of the components was placed on the pallet on top. A bird's-eye view of the setup of the wooden plank in the top pallet can be seen in Fig. 3.7, while the motor and inverter inside the lower pallet can be seen in Fig. 3.8.

Underneath the top components were two electrically connected grounding plates. These acted as a simulated vehicle chassis at reference ground potential to which all components were connected, as if mounted to the vehicle chassis. The grounding plates were tied to protective earth through a large resistance as to not accumulate a high static charge.

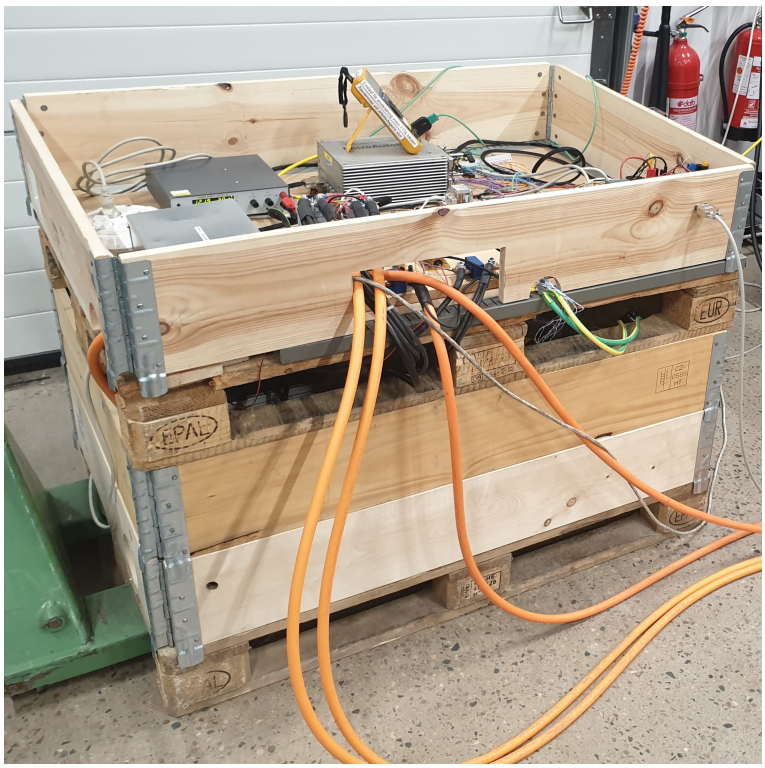


Fig. 3.6. The pallet stack.

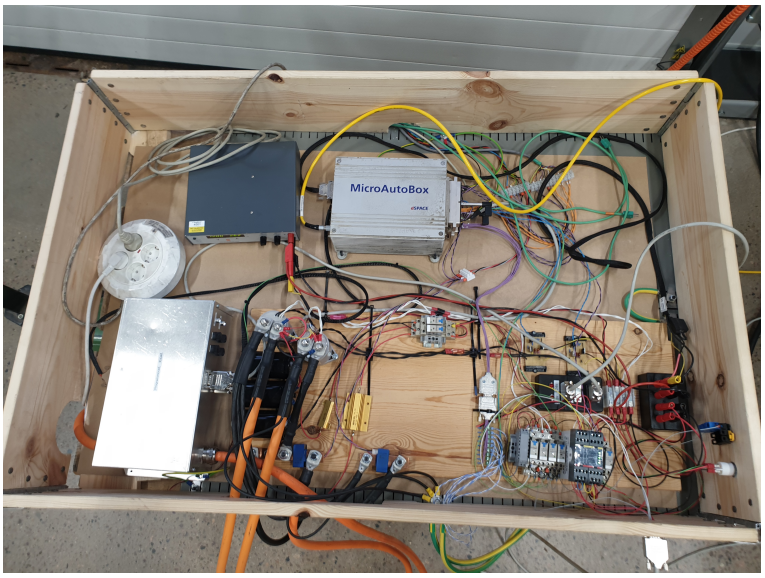


Fig. 3.7. Bird's-eye view of everything mounted inside the top pallet. The contactors can be seen to the left and the safety system to the right as well as two current sensors on the bottom.

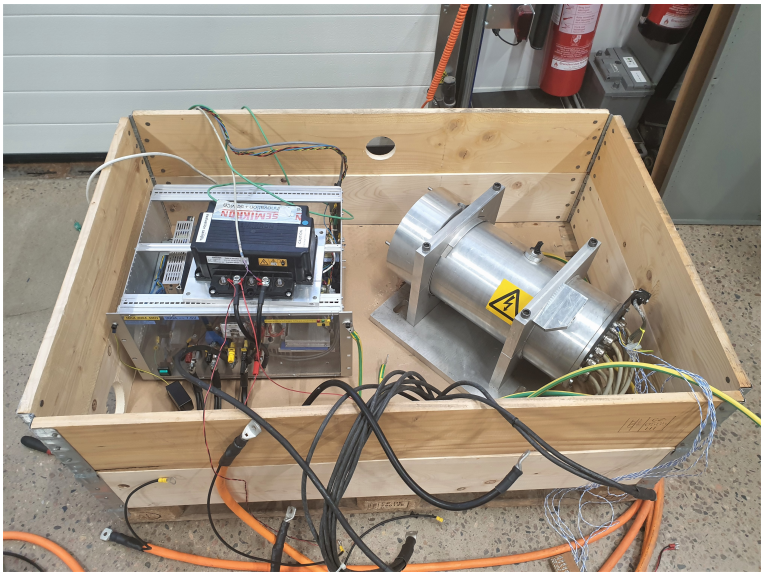


Fig. 3.8. A view of the motor and inverter inside the lower pallet with the top pallet removed. To the left, the additional capacitor bank inside the Semikron inverter can be seen on top of the inverter used which was connected by two short cables to the DC link during testing (not fully connected in the figure).

3.1.1.7 EMC mitigation

When designing a circuit, electromagnetic compatibility (EMC) needs to be considered. In the setup, the large amount of cables in close proximity to each other as well as the relatively close proximity of the power cables raised some concerns over emission and disturbances picked up. In order to minimize emitted disturbances power cables were placed with as small gap as possible between positive and negative to minimize the loop area. When possible shielded cables which were grounded in the grounding plates were used as well.

To minimize received disturbances on signal cables, twisted pairs of positive and negative wire were used extensively. In some cases, mainly for long signal cables, shielded cables were used. Finally, although not possible to a great extent, the cables were tried to be kept separated and to be minimized in length.

3.1.2 Control hardware

The whole system was controlled using a MicroAutoBox (MAB) II 1401/1513/1514 with the 1553 AC Motor Control Unit by dSpace with over 80 configurable input/output (IO) ports. It is a Real Time system designed for fast prototyping that runs on an IBM Power PC processor but also includes an FPGA. It consists of two IO modules, the one used by the Power PC and the one used by the FPGA, see Fig. 3.9. The communication between an external computer and the MAB for data visualization and programming was performed via Ethernet.

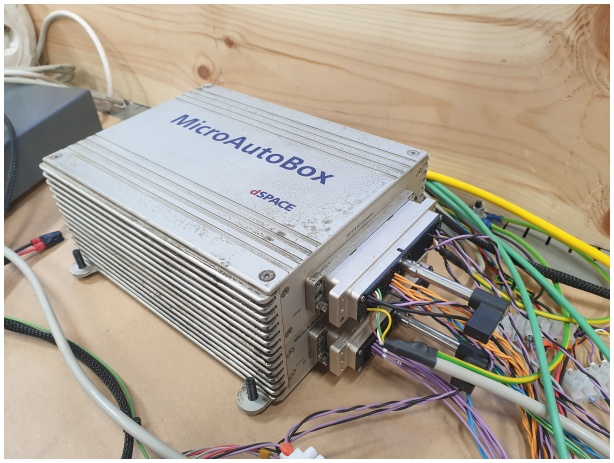


Fig. 3.9. The MicroAutoBox II used.

3.1.3 Control software

The control software consists of two parts, one which runs at twice the switching frequency and one which runs at around 1 kHz. The part that runs quickly is run on the FPGA and contains the modulator, current controllers as well as the measurements needed for them. The slower one contains everything else such as the state machine, precharge/discharge control, contactor control and temperature measurements. The control is programmed using Simulink together with third-party blocks from dSpace to be able to interact with the IO and FPGA. The Simulink model is then compiled into C and a hardware description language (HDL) and downloaded to the MAB.

Since both the current controller on the FPGA and the one used while simulating are programmed in Simulink they are identical. The state machines are also identical, although the state transitions are triggered manually on the real process because it simplifies testing of parts of the system.

To visualize the data in real time, log the data, and manually control parameters, a second program is used called Control Desk by dSpace. A custom interface is designed using built-in time plots, buttons and displays where the variables in the Simulink model are read and written to in real time. The interface used for early testing of the current controllers is seen in Fig. 3.10.

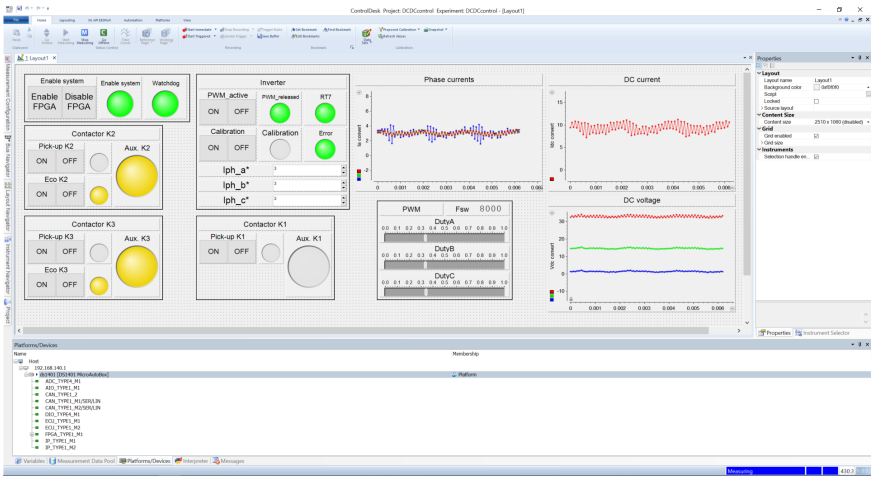


Fig. 3.10. The dSpace Control Desk layout used for testing each current controller separately in boost mode with a resistive load. Note that the DC current measures the sum of the phases instead of the load current. This is resolved in all further testing.

3.1.4 Power electronic converter

The 48 V Semikron SKAI2 LV inverter that was intended to be used did not cooperate. Therefore, the power electronic converter used was a three-phase, two level inverter built within IEA at LTH by Getachew Darge, seen in Fig. 3.11. It had the option of running either water cooled or air cooled depending on the current capability desired. Initially it had a DC link capacitance of 1.65 mF where two capacitors were connected in series in order to increase the maximum voltage. Due to a mishap described section 3.4.8 the capacitor mounting had to be rebuilt. It was decided that it would be more beneficial to have the capacitors in parallel for the use case in this project, meaning that the capacitance on the DC link of the inverter ended up being 6.6 mF with a maximum voltage of 400 V, as opposed to the previous 800 V.

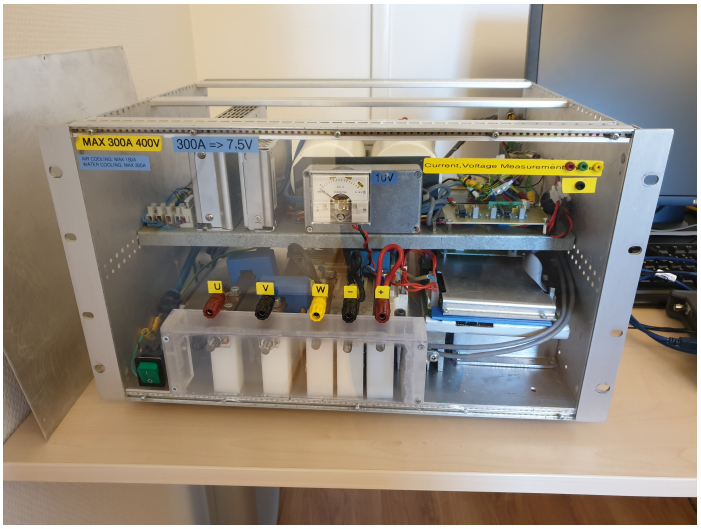


Fig. 3.11. Inverter supplied by IEA.

The switches used in the inverter is three half bridge IGBT modules made by Semikron. These are driven by a Semikron gate driver circuit each. The component names can be found in Table IV. The gate drivers have a dead time set to 5 µs which was configured when the inverter was built by means of connecting a resistor between two pins. This meant that while longer dead time is possible to implement in software, the lower limit is bounded unless the resistor is changed. The characteristics of the IGBT modules, both the IGBTs and the reverse diodes, used for calculating the losses of the inverter is found in Table V.

TABLE IV
IEA Inverter switch components

Component type	Brand	Name	Description
Gate Driver	Semikron	SKHI 23/12	Built-in dead time, Interlock prevention
IGBT Module	Semikron	SKM 300GB123D	1200 V, 300 A

TABLE V
IGBT module Characteristics

	Symbol	Value (typ.)	Condition
IGBT	E_{on}	(28 mJ)	$V_n = 600\,\text{V},\ I_n = 200\,\text{A},$
	E_{off}	(26 mJ)	$R_{Gon} = R_{Goff} = 4.7\,\Omega,$
	V_0	1.4 V (1.6 V)	$T_j = 25\,^\circ\text{C}\ (125\,^\circ\text{C})$
	r	5.5 mΩ (7.5 mΩ)	
Inverse diode	E_{rr}	8.5 mJ	$V_n = 600\,\text{V},\ I_n = 200\,\text{A},$
	V_0	1.1 V	$T_j = 25\,^\circ\text{C}\ (125\,^\circ\text{C})$
	r	4.5 mΩ	

To connect power cables to the inverter, cable lugs with 8 mm holes were used as to connect the cables directly to the busbars inside the inverter with as low resistance as possible. The signal interface of the inverter consisted of screw terminals routed through the backside, see Fig. 3.12. Each IGBT was controlled by pulling one of the six transistor control terminals high with a 5 V TTL level signal. Additionally, the pins of the internal current sensors were accessible such that the shunt resistances could be user-defined. Finally, ±15V as well as ground was available which was used for powering the external current sensors.

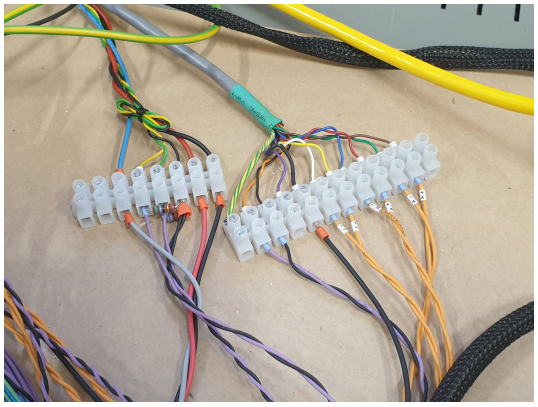


Fig. 3.12. Interface to inverter.

3.1.5 Electrical machine

The electrical machine used was designed and built during Rasmus Andersson's PhD thesis [15]. It is a three-phase, 6-pole, 80/180 kW (cont./peak) permanent magnet synchronous machine (PMSM), with distributed windings and V-shaped magnets, which is oil cooled. It also utilizes stator skewing in order to reduce the torque ripple. The machine has later been rewound as a six-phase machine but pairs of phases are connected outside the machine to produce a three-phase machine. Additionally, the neutral point is not connected inside the machine but instead connected outside by means of additional cables. It also houses seven PT100 resistance temperature detectors (RTD) used to measure the temperature at different positions inside the machine. The phase resistance was measured to 20 mΩ per phase using a four wire measurement at room temperature. The machine is seen in Fig. 3.13.

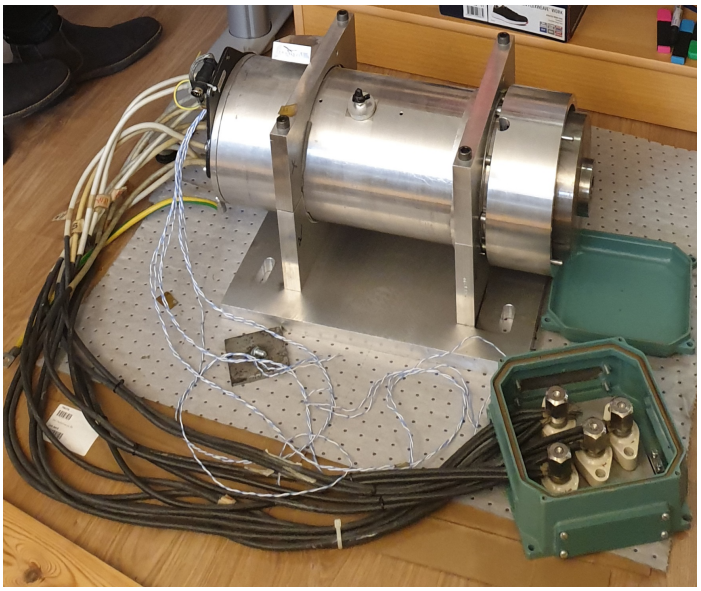


Fig. 3.13. The electrical machine used in the project with black, unshielded phase and neutral point cables as well as white and blue twisted pair cables used for the PT100 RTDs.

3.1.6 Limitations

The main limit of the current was set by the 24 V power supply, as it had a built-in limit of 385 A. Most tests were however performed at much lower current levels. This was initially due to uncertainty of the heat generation in different components, and later due to the areas of interest were more on control stability and losses which could be performed at lower currents. The concern regarding heat generation originated in part by the fact that the inverter and motor are designed with liquid cooling in mind, which were not used during testing, as well as the high current stress on the DC link capacitors.

After the current controllers had been proven to work at around 120 A per phase most tests were performed at current levels maximally 90 A per phase. This was due to the diminishing return of results obtained by running the system at higher currents compared to the risk of something overheating. Although, when a longer test was performed to measure the steady state temperature, the risk of overheating did not seem likely.

Interleaved PWM signals were not used when testing. To use interleaved PWM signals a requirement would be to shift the modulation wave for each phase leg. Since this is a rather unconventional modulation technique for an inverter there was no official support from the dSpace software. A workaround was attempted by trying to implement a software based modulation, implementing phase shifted counters acting as modulation waves. The code was however not efficient enough and Task Overrun errors was thrown when the program was downloaded to the MAB, meaning that the program was too processor intensive to run in real time at a reasonable switching frequency. Ways of getting around this problem might have been to use an external micro controller for generating the modulation waves and the PWM signals, or to program the FPGA using the Vivado tool chain by Xilinx. Although, to limit the scope of the project interleaving was not used.

3.2 Safety

As this project involved rather high currents a variety of safety measures were put in place. These included both personal safety as well as safety for the devices and components which were used.

3.2.1 Emergency stop

The emergency stop circuit was one of the key safety features regarding personal safety. In case of any mishap where the process had to be aborted quickly, the emergency stop circuit cut power from the power supplies immediately by cutting power to K1 and K3, as well as activating two emergency discharge resistances over the capacitors as to remove any charge from the circuit. The contactor K2 was actively not cut as to not break an inductive load and the discharge resistances are explained more in section 3.1.1.4. The emergency switch signal was also routed to the Regatron power supplies with a one second delay as to not unnecessarily wear their contactors by forcing them to open at full power. This was achieved with the help of an ABB RT7 safety relay, which included two normally open (NO) outputs and two delayed NO outputs. In addition to the emergency stop feature of the RT7 it included a feature of needing to be manually reset which was designed as to not be possible to do unless all contactors and the power supplies were in their safe and turned off state. A complete circuit diagram, including the safety relay circuit, can be seen in Appendix A.

3.2.2 Test rig

The testing was performed inside a car workshop. This provided good access to multiple high power three-phase outlets, fire extinguishers, as well as being close to a garage door.

The whole test rig was built on stacked pallets as explained in section 3.1.1.6. When testing, the stack was always loaded onto a pallet truck making it easily movable. By being close to the garage door and using Anderson connectors for the connection of the power cables to the power supplies, it was made possible to quickly disconnect everything and move the pallet stack outside in case of a fire or other incidents.

3.2.3 Temperature measurements

In a way of mitigating the risk of components becoming too hot, temperature sensors were used. Inside the motor, seven PT100 temperature sensors are mounted in various places. These are routed out and accessible for use. More in depth explanation of the temperature measuring circuit can be seen in section 3.3.3. Additionally, two type K thermocouples were adhered to the DC link capacitors using aluminium tape. These were monitored using a digital multimeter as a way to know if either of the capacitors reached a high temperature. This was implemented due to uncertainty of the distribution of current ripple between the two DC link capacitor banks and whether one or the other would heat up more.

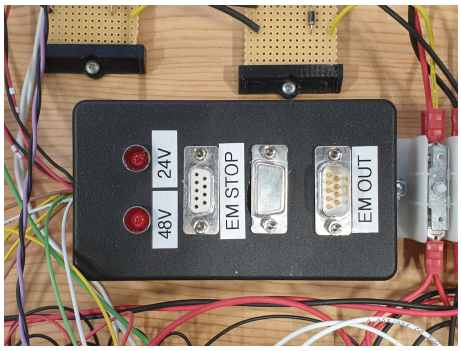
3.2.4 Other safety measures

By continuously testing the system in parallel with the construction each component's functionality was verified. To verify correct behaviour of the current controller the power supplies were configured to limit the current and voltage. Early tests used small benchtop power supplies while the Regatron power supplies were not available. Succeeding tests got incrementally higher voltage and current limits until the values reached that of the final testing. In the low current testing phase, shunt resistors were used in lieu of a power supply with current sinking (Q4) capability.

At all times of testing, but especially when tests reached a significant amount of current ($>10\,\mathrm{A}$), components were observed during and between tests to see that nothing had built up too much heat. The tests were always supervised and never left unattended.

To know if the system was armed an indicator light was installed in the pallet collar and two extra LEDs were connected in series with resistances to indicate whether the capacitors were charged, see Fig. 3.14.

(a) Light to indicate the status of the RT7 safety relay, where red means stopped and green means active, with the reset button to the right.



(b) LEDs indicating if either the 48 V or 24 V side of the system is charged.

Fig. 3.14. Indicator lights

3.3 Sensing and filtering

The following sections treat the measuring of analog signals. The location of the voltage and current measurements can be seen in Fig. 3.15. The phase currents, i_{phA}, i_{phB}, i_{phC}, and the voltages, u_{DC}, u_{np}, u_k, are used for control. Additionally, the currents, i_s, i_{cs}, and voltages, u_{dc}, u_{np}, are used to calculate the efficiency of the converter.

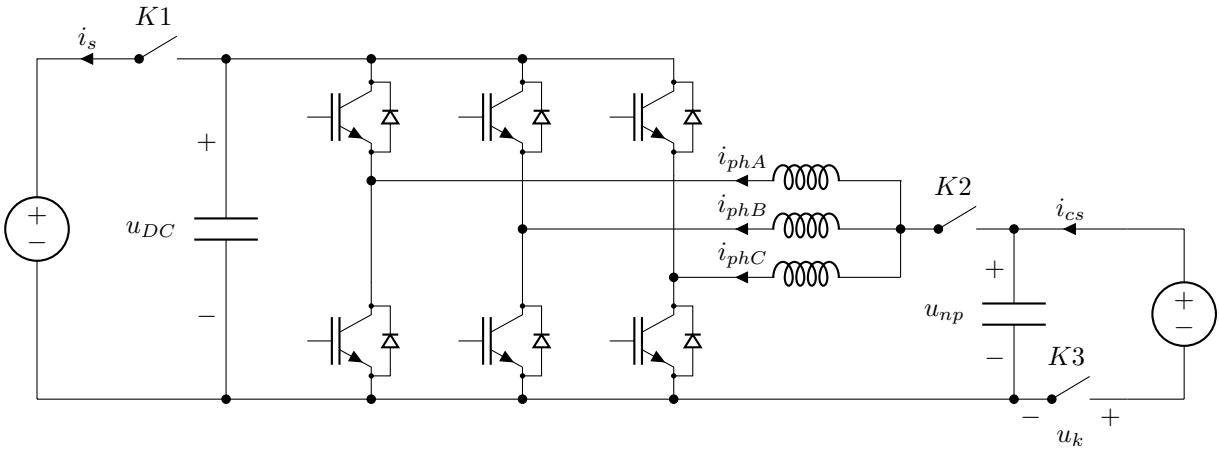


Fig. 3.15. Circuit diagram of the main circuit and the measured quantities used for control and efficiency calculation.

Worth noting is that even though theoretically, the resolution of the signals is high, the performed measurements will not have that accuracy since signal disturbances will be picked up, making the measured signal more noisy and not as accurate as the resolution might suggest.

A summary of the measurements can be seen in Table VI where the range is either limited by the sensor itself or the maximum ADC voltage.

3.3.1 Voltage sensing

To sense the voltage of the circuit, a voltage division was needed to scale down the voltage to the range which the MAB could handle. The circuit diagram can be seen in Fig. 3.16. It was designed to scale down the voltage about six times. Thus, the MAB could theoretically measure voltages up to about ±90 V without being damaged since the ADC could handle ±15 V.

The voltage measurements were connected to the programmable FPGA with an 14 bit, 10 MHz ADC with a capability of ±15 V, giving a 10 mV resolution of the measured voltage, see (3.7). The measurement was differential and latched to the FPGA each time the carrier wave turned. Due to

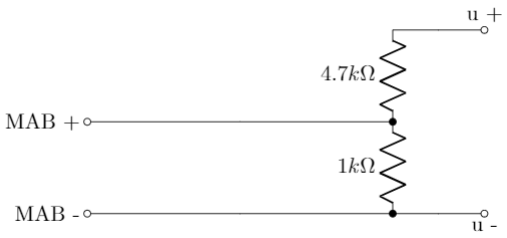


Fig. 3.16. Voltage sensing circuit.

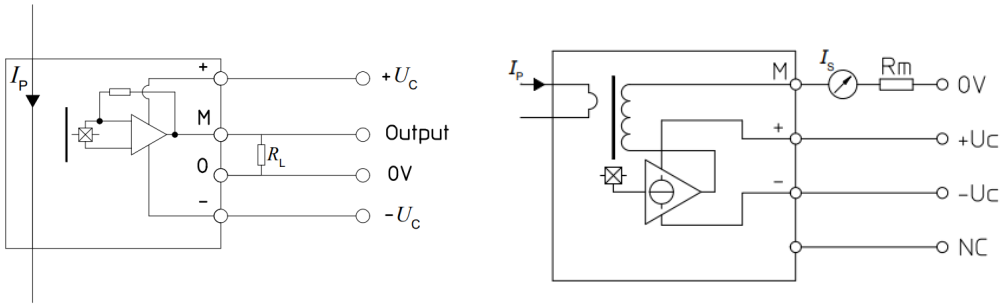
the relatively slow change of the voltage a built-in average filter of eight 100 ns samples centered around each latch was used.

$$\frac{30}{2^{14}} \cdot \frac{5.7}{1} = 0.01\,\mathrm{V/step} \tag{3.7}$$

Both higher and lower resistor values were considered, but it settled on 1 kΩ and 4.7 kΩ, both with 1 % tolerance, as it was a good trade-off between lower impedance, to reduce disturbances picked up, and bleeding too much current through and thereby charging the capacitors. The resistance tolerance does not affect the significant figure.

3.3.2 Current sensing

The same ADC type was used for the current sensors but with a range of ±5 V and no digital filter. The equivalent circuit diagrams for the sensors can be seen in Fig. 3.17. The supply voltage was ±15 V which was supplied from the inverter.



(a) LEM HAS 400-S with $R_L = 1\,\mathrm{k\Omega}$.

(b) LEM LA200-P with $R_m = 56\,\Omega$.

Fig. 3.17. Equivalent circuit for the (a) external and (b) inverter internal current sensors [16, 17].

The external sensor of type LEM HAS 400-S outputs 4 V at 400 A and with the 14 bit ADC using 10 V range the resolution of the measurements on the primary current becomes 0.06 A as seen in (3.8). The internal LEM LA 200-P drives the secondary current with a factor of 1:2000 to the primary. With a shunt resistor of 56 Ω (±5 %) and an identical ADC the resolution becomes 0.02 A as seen in (3.9).

$$\frac{\frac{10}{2^{14}}}{\frac{4}{400}} = 0.06\,\mathrm{A/step} \tag{3.8}$$

$$\frac{\frac{10}{2^{14}}}{56} \cdot 2000 = 0.02\,\mathrm{A/step} \tag{3.9}$$

These can be put into context of the worst case accuracy of the sensors which for the LEM HAS 400-S is ±4 A and for the LEM LA 200-P is ±0.8 A. Thus, the accuracy of the sensors is more of a limitation than the resolution achievable with the ADC in the MAB.

3.3.3 Temperature sensing

To read the temperature within the motor a voltage division was made with the PT100 temperature sensors and 1 kΩ (±1 %) resistors to convert the signal to be readable by the micro controller. The circuit of the voltage division can be seen in Fig. 3.18. In one of the voltage dividers a known resistance of 137 Ω was used as a way to calibrate the sensors and remove any static errors due to small neglected resistances. The reason why not all sensor spots is filled is due to the switch to an other inverter resulting in less available temperature sensors.

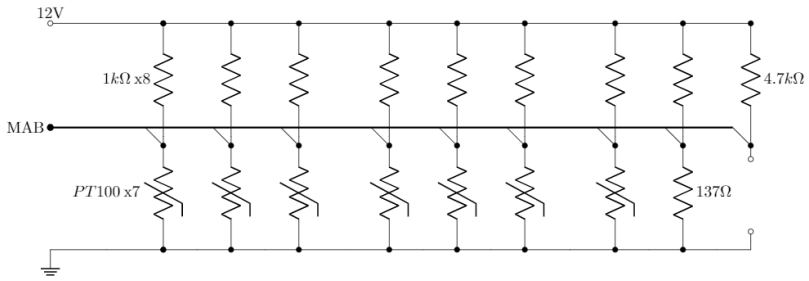


Fig. 3.18. Temperature sensor voltage divider circuit.

The resistor values chosen for the voltage division were based on the voltage limit of the micro controller and the resolution of the ADC within the MAB. The ADCs used have a 16 bit resolution with a range of ±10 V giving the temperature measurements around 0.08 °C resolution as seen in (3.10). Note that the resistance tolerance does not affect the significant figure. The denominator in the right fraction represent the voltage increase over the PT100 when the temperature rises from 0 °C to 100 °C. The numerator represents the temperature change in degrees Celsius. Additionally, the temperature is filtered by a first-order low-pass filter using a cutoff frequency of 0.1 Hz. The physical circuit can be seen in Fig. 3.19.

$$\frac{20}{2^{16}} \cdot \frac{100}{12\left(\frac{138.5}{1000+138.5} - \frac{100}{1000+100}\right)} = 0.08\,^{\circ}\mathrm{C/step} \tag{3.10}$$

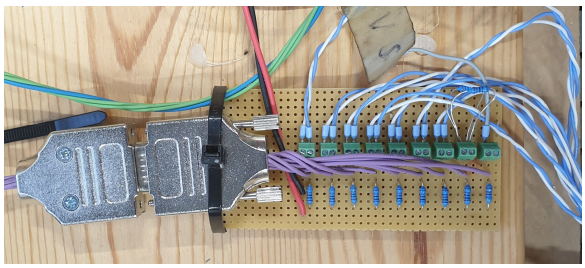


Fig. 3.19. Temperature sensor voltage divider physical circuit.

TABLE VI
MEASUREMENT SUMMARY

Quantity	Sensor	Range	Accuracy	Filter
Voltage	Voltage divider	−90 V to 90 V	±5 mV	Moving average
Current	LEM HAS 400-S	−400 A to 400 A	±4 A	No filter
Current	LEM LA 200-P	−180 A to 180 A	±0.8 A	No filter
Temperature	PT100	−50 °C to 170 °C	±0.04 °C	Low-pass

3.4 Experiments

3.4.1 NVH observations and torque

Noise, vibrations and harshness (NVH) of the setup was studied by means of manual observations. As soon as the switching of the inverter IGBTs began an audible tone with the same frequency as the modulation wave, usually 8 kHz, could be heard. It grew stronger with higher currents, but it was not uncomfortable. An audio spectrum analyzer smart phone application was tried out to see the audio spectrum, however, due to the noisy environment in which the tests were carried out at the switching sound was not noticeable on the resulting graph. There were no other audible frequencies or harmonics when testing and the motor was perfectly still and not vibrating when felt by hand.

At very low currents the rotor could be moved manually but when the phase currents got up to around 10 A per phase it was no longer possible to turn the motor shaft as it had settled in a lowest energy position where the torque produced by each phase canceled out. Note that the machine uses stator skewing and therefore have very low cogging torque, thus producing little to no torque initially when lining up.

3.4.2 Temperature

When the circuit was driven for about ten minutes at 90 A on the 48 V side, around 220 A on the 24 V side, it was deemed that the system would not reach a much higher temperature and was in steady state. This assumption was not derived from any theoretical values but rather the perception from the authors that the thermal time constant of the inverter components were low enough that the steady state would be reached in the time tested. At this point the motor reached a temperature of about 40 °C. The busbars connecting the internal capacitors to the DC link reached an estimated temperature of around 70 °C given they were at 53 °C three minutes after the test concluded.

3.4.3 Electrical noise

When driving low to no currents, the signal noise amplitude from the external current sensor was about three times larger than that of the internal sensors'. However, when the current was increased, the signal noise increased as well and the noise amplitude got to the same level for all current sensors when above 100 A on the DC link side. Additionally, the touchpad on the laptop monitoring the system stopped working at around this time.

3.4.4 Oscilloscope readings

Some measurements were performed with an oscilloscope but due to limitations of the current probes the current had to be limited. The oscilloscope readings can be seen in Fig. 3.20 through 3.23 and are all taken when a DC link current reference of 30 A was used.

Due to tight space within the inverter no current probes were suitable for measuring the current ripple in the internal inverter capacitors and therefore no result of this is presented. Although, in Fig. 3.21 it can be seen the current derivative is limited in the external DC link capacitors. This is likely due to the small inductance of the cables connecting it to the inverter, thus, the DC link capacitors inside the inverter likely takes the majority of the high frequency components.

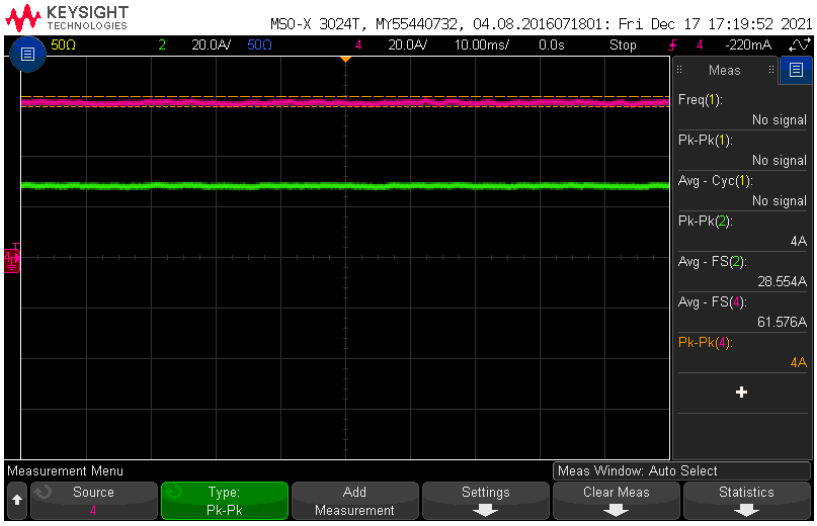


Fig. 3.20. Current on the 24 V side (cerise) and the 48 V side (green) from and to the power supplies of 61.6 A and 28.6 A respectively, each having roughly 4 A peak to peak ripple. The oscilloscope is set to 20 A/div and 10 ms/div.

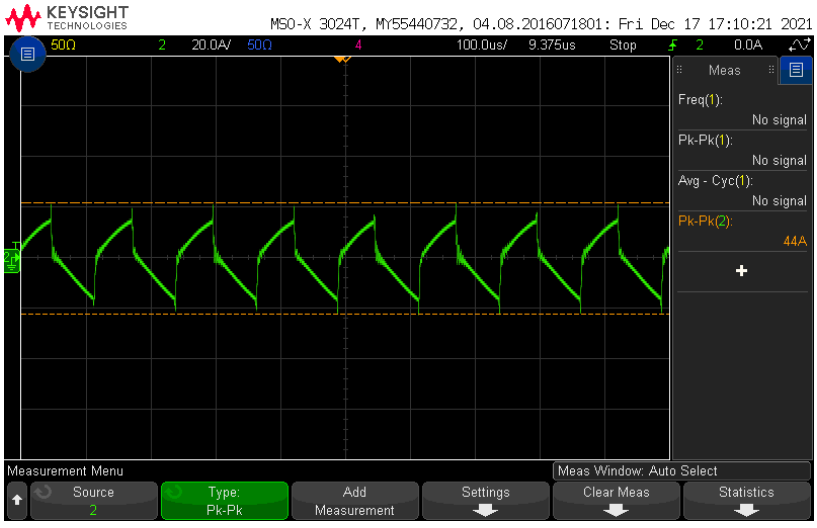


Fig. 3.21. Current in the additional 25 mF DC link capacitors of roughly 44 A peak to peak using 20 A/div and 100 µs/div.

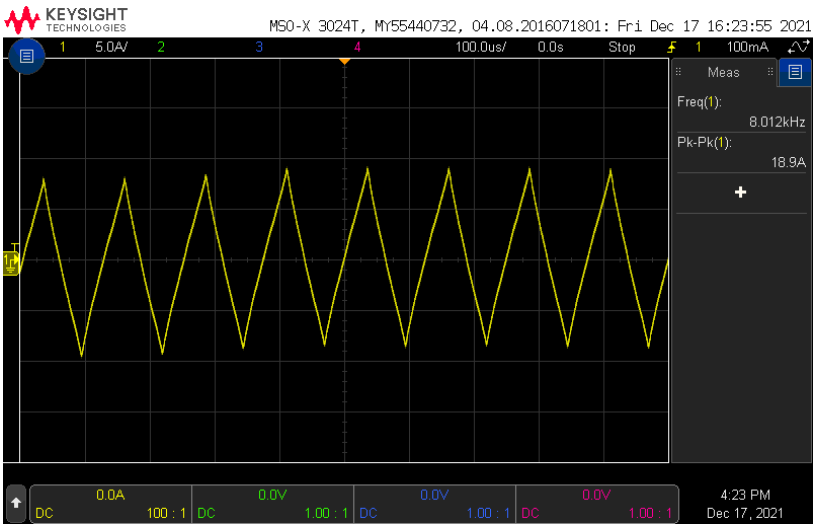


Fig. 3.22. Current in the 30 mF neutral point capacitors of approximately 18.9 A peak to peak using 5 A/div and 100 µs/div.

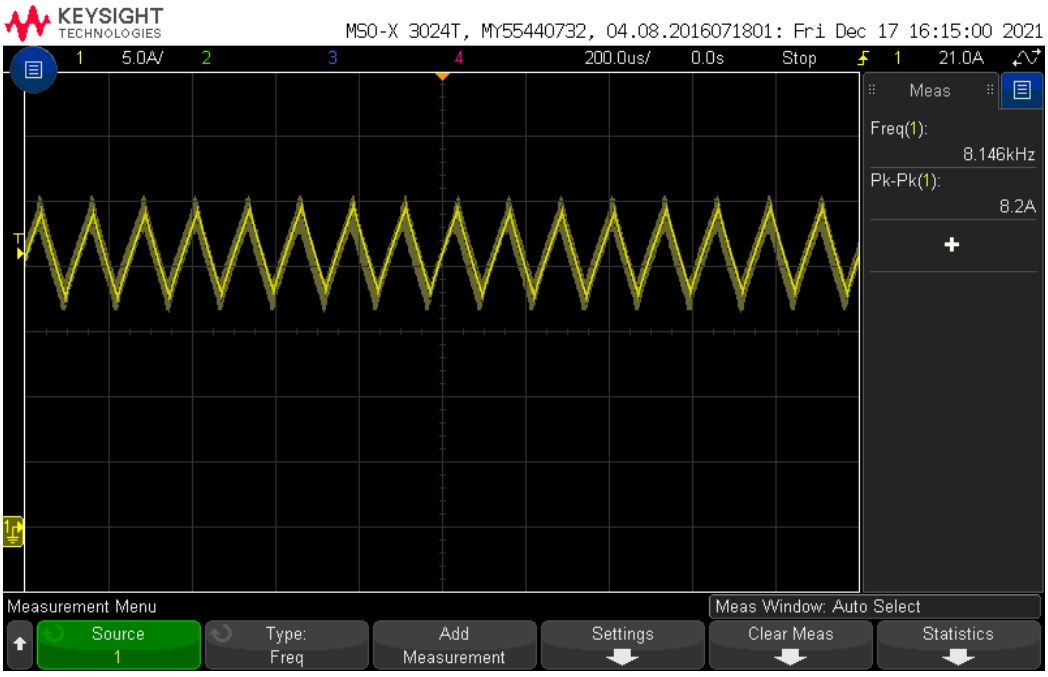


Fig. 3.23. Current in phase C with an average of about 20.5 A and a ripple of 8.2 A peak to peak. The oscilloscope is set to 5 A/div and 200 µs/div.

3.4.5 Precharge and discharge

The precharge and discharge of the neutral point capacitor can be seen in Fig. 3.24. The voltage has a slight stationary error and some small oscillatory behaviour but avoids over- and undershoots. The initial voltage during precharge is due to current leaking through the voltage measurement across the contactor connected to the simulated charging station.

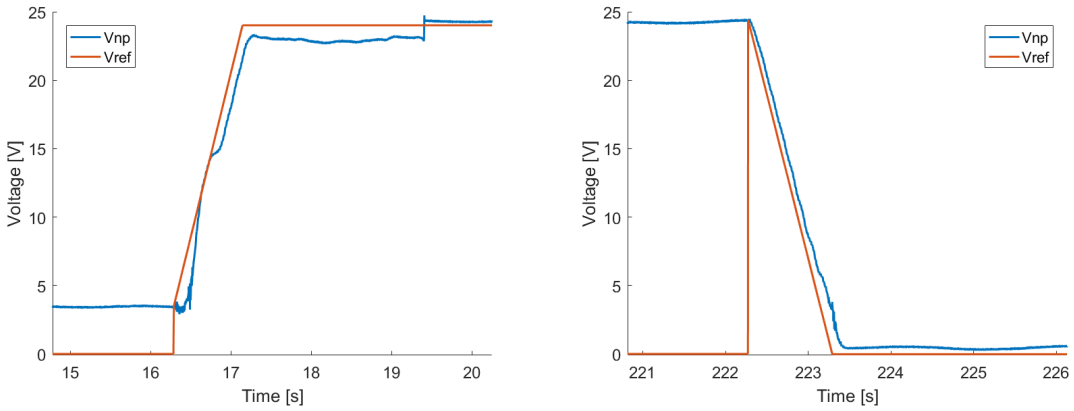


Fig. 3.24. The voltage across the neutral point capacitor during (a) precharging and (b) discharging through the inverter and the corresponding reference for the P controller. In (a) the contactor is closed at around 19.5 s thus the sudden jump in voltage.

3.4.6 Efficiency

Some experiments were carried out to compare the efficiency when boosting against the theoretical one. The theoretical efficiency is derived using

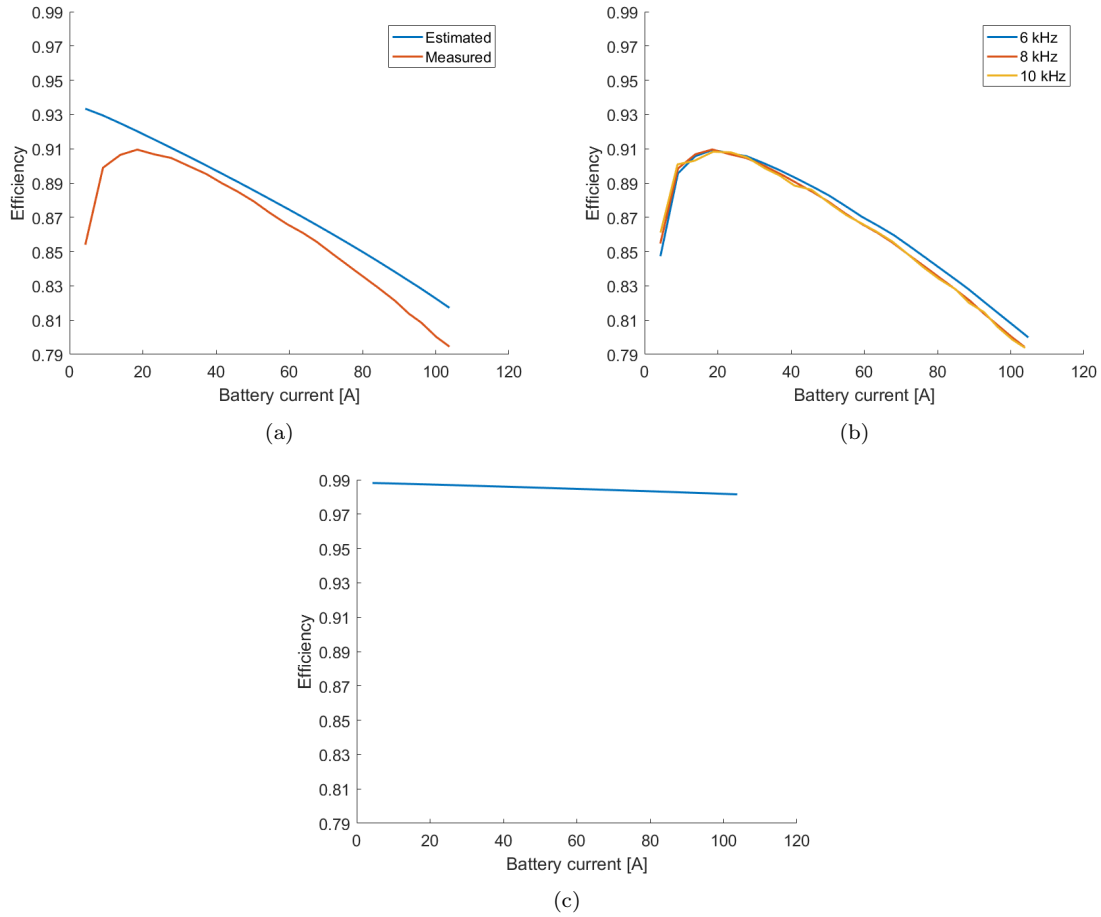
$$\eta = \frac{u_{np} \cdot i_{cs} - P_{cu} - P_{inv} - P_{cap}}{u_{np} \cdot i_{cs}} \tag{3.11}$$

where u_{np} and i_{cs} are defined according to Fig. 3.15 and the losses according to section 2.4. The capacitors inside the inverter are assumed to take the entire ripple current as the ESR of the external one is unknown. The DC link capacitor current is assumed to be rectangular in shape, although this gives an underestimation of its RMS value.

The tests were performed by increasing the battery current reference in steps of 5 A up to 120 A while logging the input and output currents and voltages using a power analyzer. Additionally the duty cycle was logged in order to be able to estimate the efficiency according to section 2.4. The resulting efficiency together with the estimated one is seen in Fig. 3.25a. Note that the maximum battery current is just above 100 A, an output of about 5 kW, which is below the maximum reference due the open-loop control and insufficient compensation.

Additional experiments were carried out to measure the impact of the switching frequency. The efficiency and currents were measured using the same procedure as previously but at two additional switching frequencies. Each time the controller gains were recalculated before running the test, although, the controller was still stable even without gain adjustments. The resulting efficiency versus measured battery current at different switching frequencies can be seen in Fig. 3.25b.

To get an estimate of the efficiency at a higher voltage the theoretical efficiency is recalculated although with a 400 V input and 800 V output. This would roughly correspond to a 80 kW charger. The corresponding efficiency is presented in Fig. 3.25c. Note that due the increase in voltage the current ripple is very high as seen in (3.17). Thus, it is assumed that the current ripple is reduced somehow to about the same order of magnitude as the low voltage system.



(a) (b)

(c)

Fig. 3.25. The (a) measured and estimated efficiency at 8 kHz, (b) measured efficiency at different switching frequencies and (c) extrapolated theoretical efficiency for a 400 V to 800 V converter.

3.4.7 Calculations

3.4.7.1 Motor common mode inductance

By measuring the rise time of the current ripple from the oscilloscope, as seen in Fig. 3.23, the inductance experienced by each phase could be calculated with (3.12) through (3.15), where f is modulation wave frequency, Δi is the current change, D is the duty cycle, u is the voltage and Δt is the on time.

$$u(t) = L\frac{di}{dt} \approx L\frac{\Delta i}{\Delta t} \tag{3.12}$$

$$f = 8.146\,\text{kHz} \quad \Delta i = 8.2\,\text{A} \quad D = 0.525 \quad u = 24\,\text{V} \tag{3.13}$$

$$\Delta t = \frac{D}{f} = 64.4\,\mu\text{s} \tag{3.14}$$

$$L = \frac{24 \cdot 64.4 \cdot 10^{-6}}{8.2} = 0.189\,\text{mH} \tag{3.15}$$

3.4.7.2 Phase ripple at higher voltage

To calculate the ripple when driving the same circuit at 400 V to 800 V, (3.12) is used and Δi is solved for using the same duty cycle, modulation wave frequency and inductance as before but with the higher voltage, as seen in (3.16). The estimated phase ripple magnitude at the higher voltage is seen in (3.17).

$$f = 8.146\,\text{kHz} \quad L = 0.189\,\text{mH} \quad D = 0.525 \quad u = 400\,\text{V} \tag{3.16}$$

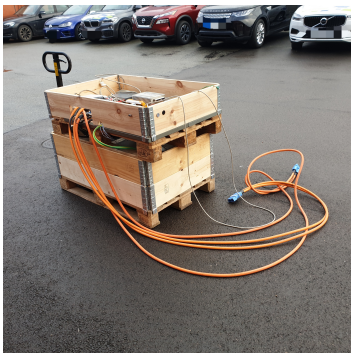
$$\Delta i = \frac{400 \cdot 64.4 \cdot 10^{-6}}{0.189 \cdot 10^{-3}} = 136.3\,\text{A} \tag{3.17}$$

3.4.8 Mishaps

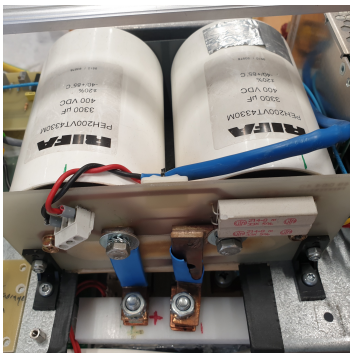
There were two incidents worth mentioning that happened during the testing phase. The first one being when the large Regatron power supplies were first tested. Both were connected to the circuit, but only the 24 V was turned on while bypassing the safety relay, meaning that the discharge resistors were still activated. No current should have been flowing, but the power supply display read 2 A. This was indeed what happened as one of the discharge resistors got hot. The cause was determined to be the way the power supplies' signal cables were connected normally, as the cable would connect their signal ground together. The signal ground was also connected to each negative terminal. This closed the circuit and meant that current could flow through the signal cable. Had this not been noticed, the precharging of the neutral point capacitor would not have had any effect as the capacitor would have already had charge and the K3 contactor would have been rendered useless as the current could take a different path. A workaround was constructed by making a new cable which did not connect the signal grounds of the power supplies together. The new and old wiring diagram can be seen in Fig. A.4 and A.5 in appendix A.

The second incident happened when the circuit was driven at the maximum power it was designed to perform at. Thus, 353 A were driven to the motor from the 24 V power supply. After just a short while smoke started to emerge from the lower pallet. Everything was shut down as quickly as possible and the pallet was pulled outside to cool off and not destroy anything in case of a fire. When everything had cooled down the inverter was deemed the source of the smoke and it was slightly taken apart to see what the source of the smoke was. It was discovered that the printed circuit board (PCB) connecting the capacitors in series could not handle the current ripple as it had melted and it was determined to be the cause of the smoke. After inspecting that the capacitors were fine and making sure nothing else had taken damage the capacitors were connected in parallel with busbars and reinserted into the inverter. This gave the DC link higher capacitance and a higher margin for the current ripple. The event sequence can be seen in Fig. 3.26.

(a) Highest current driven through the system.

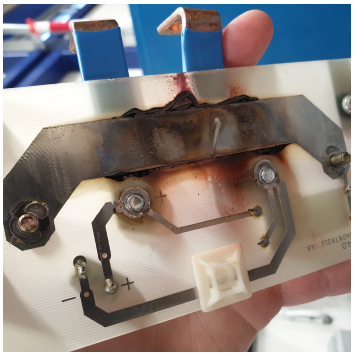


(b) Test pallet outside due to smoke emerging from the lower pallet.

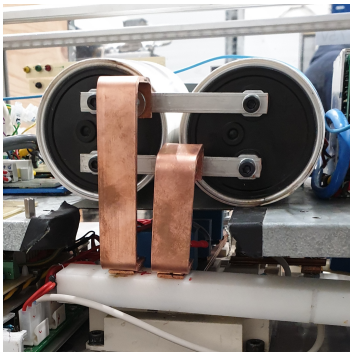


(c) Capacitors inside inverter before removal.

(d) Capacitors removed from the inverter.



(e) The burnt PCB which was the source of the smoke.



(f) Capacitors mounted in parallel with new busbars.

Fig. 3.26. The smoke incident.

Chapter 4

Discussion

4.1 Conclusions

As seen in Fig. 3.20 the currents had a quite low ripple at the power supplies, less than 4 A peak to peak. This implies that the capacitors took care of most of the ripple on both the DC link and the neutral point. The peak to peak measurements were also over multiple switching periods, meaning the single period current ripple is even smaller.

The fact that the busbars to the internal capacitors got warm as well as the external capacitors used only alleviated a relatively small ripple current implies that the internal capacitors account for most of the current ripple mitigation. This is to be expected as the impedance to the external one is likely quite large due to the few hundred nanohenries of the cables connecting it to the DC link.

The rather large efficiency discrepancy at low currents in Fig. 3.25a could be because the linear scaling of switching losses assumed in (2.11) does not hold when scaling with such a large factor as from 600 V to 48 V. Thus, using an inverter rated closer to operating point used should hopefully result in closer estimations.

When comparing the efficiency measured and theorized in Fig. 3.25a to the theorized efficiency at 400 V to 800 V in Fig. 3.25c, it can be noted that the efficiency increases quite a lot at the higher voltages. This is expected as the resistive losses will stay constant when the current magnitude is constant, while the increase in voltage causes the power throughput to become larger, that is, higher power is transferred with the same resistive losses. Although, as the voltage is increased, the switching losses will increase as well. Worth noting is that while the theorized efficiencies may give an indication of the efficiency, it does not completely match that of the measurements, thus, further testing and evaluation has to be performed for more accurate efficiency estimates.

As seen in Fig. 3.25b the efficiency is not notably changed when the switching frequency is changed. One explanation could be that the switching losses of the IGBTs are quite small due to the voltage rating being a lot higher than the voltage used, thus, the losses reduced by decreasing the switching frequency is compensated for by the increased capacitor losses due to increased ripple.

The heat generation in both the motor and the IGBTs in the inverter was not problematic, and should probably become even less problematic in high voltage systems as the newer inverters incorporate more efficient switches and properly dimensioned cooling systems. Additionally, the limiting factor will likely be the charging plug as the current is split in three between the phases in the machine.

More concerning is the current ripple, especially in the phases when higher voltages are used, as the current derivative will be much higher when operating at 16 times higher voltages, as indicated by the results of (3.17). Additionally, the apparent phase inductance seems to be a lot lower when running common mode currents as opposed to the currents run when driving. To reduce the ripple, increasing the switching frequency is one solution but will likely not be enough alone, thus, an additional external inductor is most likely required, possibly in tandem with interleaved PWM signals.

The charging station has been modeled and run as a constant voltage source for the purpose of simplifying the current control, although, most charging station outputs a requested current, thus, additional control will be required. A solution could be to keep the current control used in this project and add an additional fast voltage control loop that requests a current from the charging

station in order to keep the voltage at neutral point constant. The control loop would likely need to use feedforward of the phase currents to be fast enough in order not cause too much voltage ripple. Another, more brute-force solution, could be to request a current from the charging station that is larger than the sum of the currents controlled through the phases. This would likely cause the charging station to increase its output voltage to try an increase the current. As the current requested is never reached the station will eventually reach its maximum voltage and act as a constant voltage source. This assumes that station does not report an error if the requested current is not reached within a finite amount of time as well as reaching its maximum voltage. Although, the former solution is likely the better option.

4.2 Summary

The concept of using the traction system of an electric vehicle and driving it as a boost converter is proven to be possible. And with the extrapolated results of the efficiency at 400 V to 800 V, quite efficiently as well.

The need for including an extra DC to DC converter in a car with an 800 V battery might not be necessary any more if some small adjustments are performed to the traction system. Although, the increased current ripple at the higher voltage levels is something that will have to be mitigated in one way or another.

4.3 Future work

To further enhance the system some improvements that might be worth looking into is suggested. The large current ripple at higher voltages will most likely be of concern. To reduce the stress on the capacitors and extend their operating life, evaluating the use of interleaved switching is proposed. Although, the possibility for additional vibrations need to be investigated and weighed against the reduced ripple.

Other suggestions for decreasing the ripple is using an extra inductance to lower the current derivative. Increasing the switching frequency will also further decrease the ripple, which also moves the audible frequency out of the hearing range for a larger part of the population.

Further, finite element analysis of the machine should be performed in order to evaluate the flux paths and investigate the iron losses, the coupling between phases as well as the forces generated at different rotor positions.

Additionally, a more detailed simulation model should be used which includes switching losses, capacitor losses and the mutual inductance between the phases in order to be able to predict the efficiency.

The stationary error in the battery current should also be addressed either by compensating for more losses or by designing a PI controller. Additionally, a control loop to request a current from the charging station instead of a voltage needs to be developed or solved some other way.

An enhancement to the state machine should also be done by adding more support for edge cases such as turning the charger off at different stages of precharging.

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Appendix A

Circuit diagrams

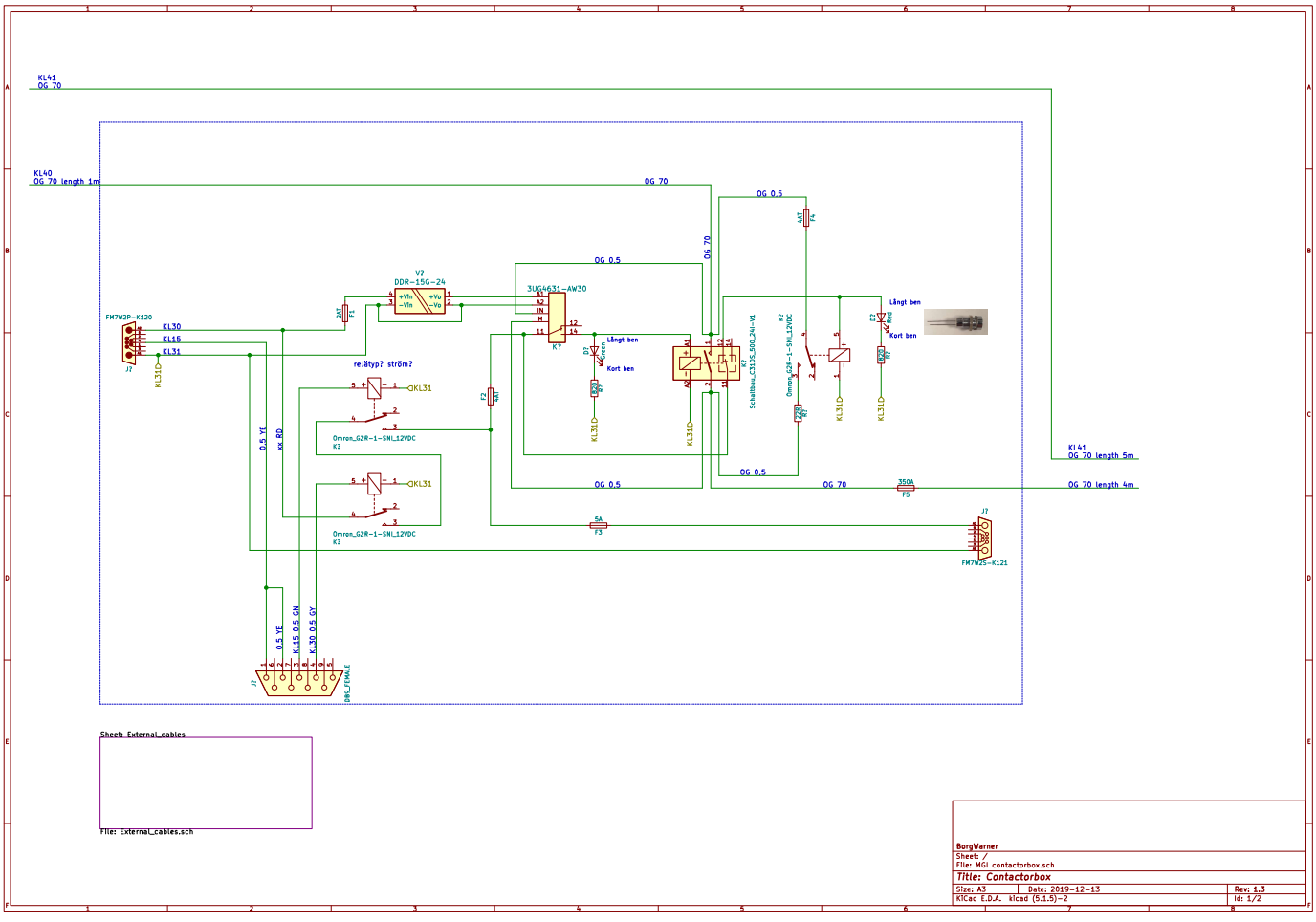

Fig. A.1. Contactor box (K1).

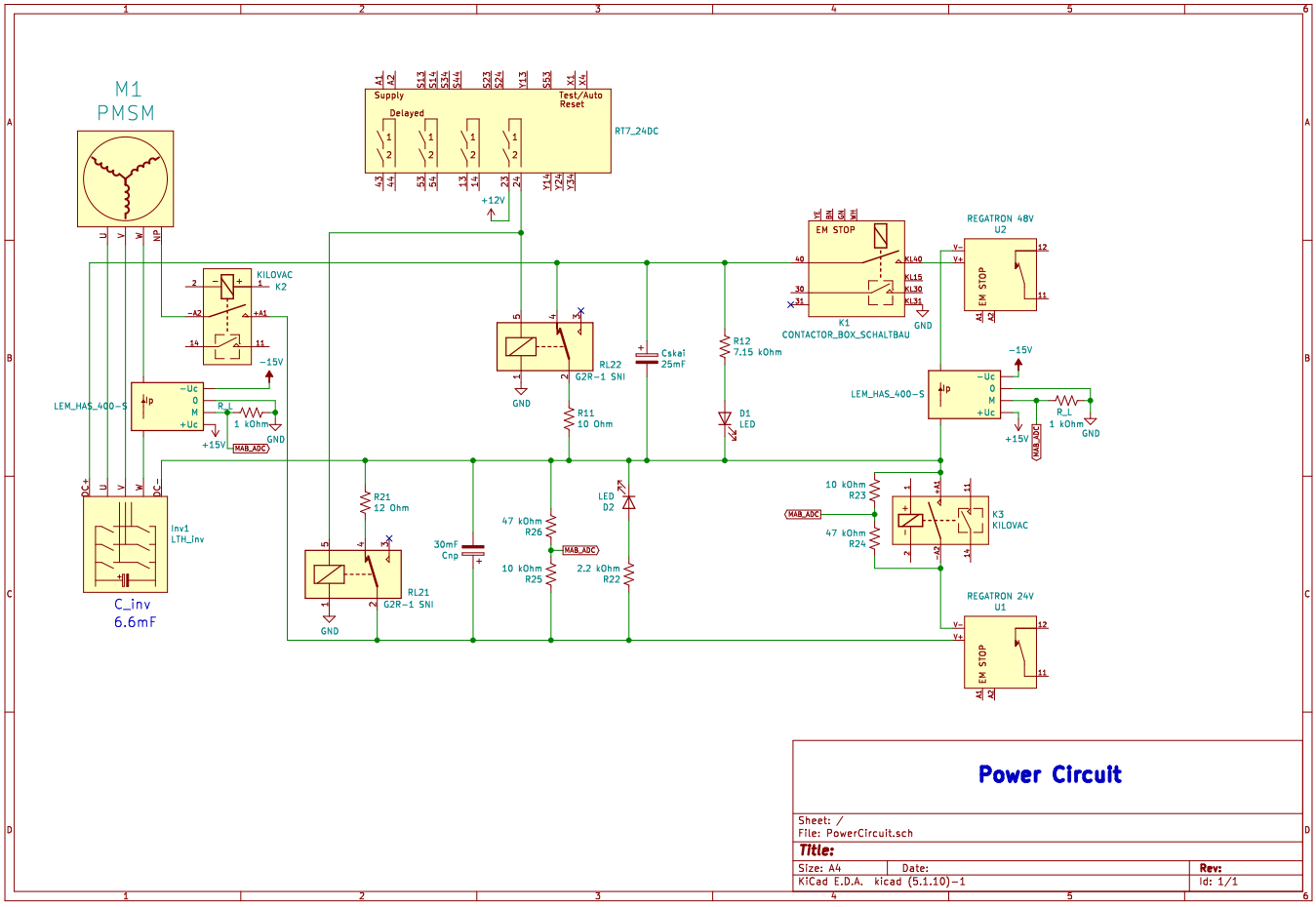

Fig. A.2. Power circuit.

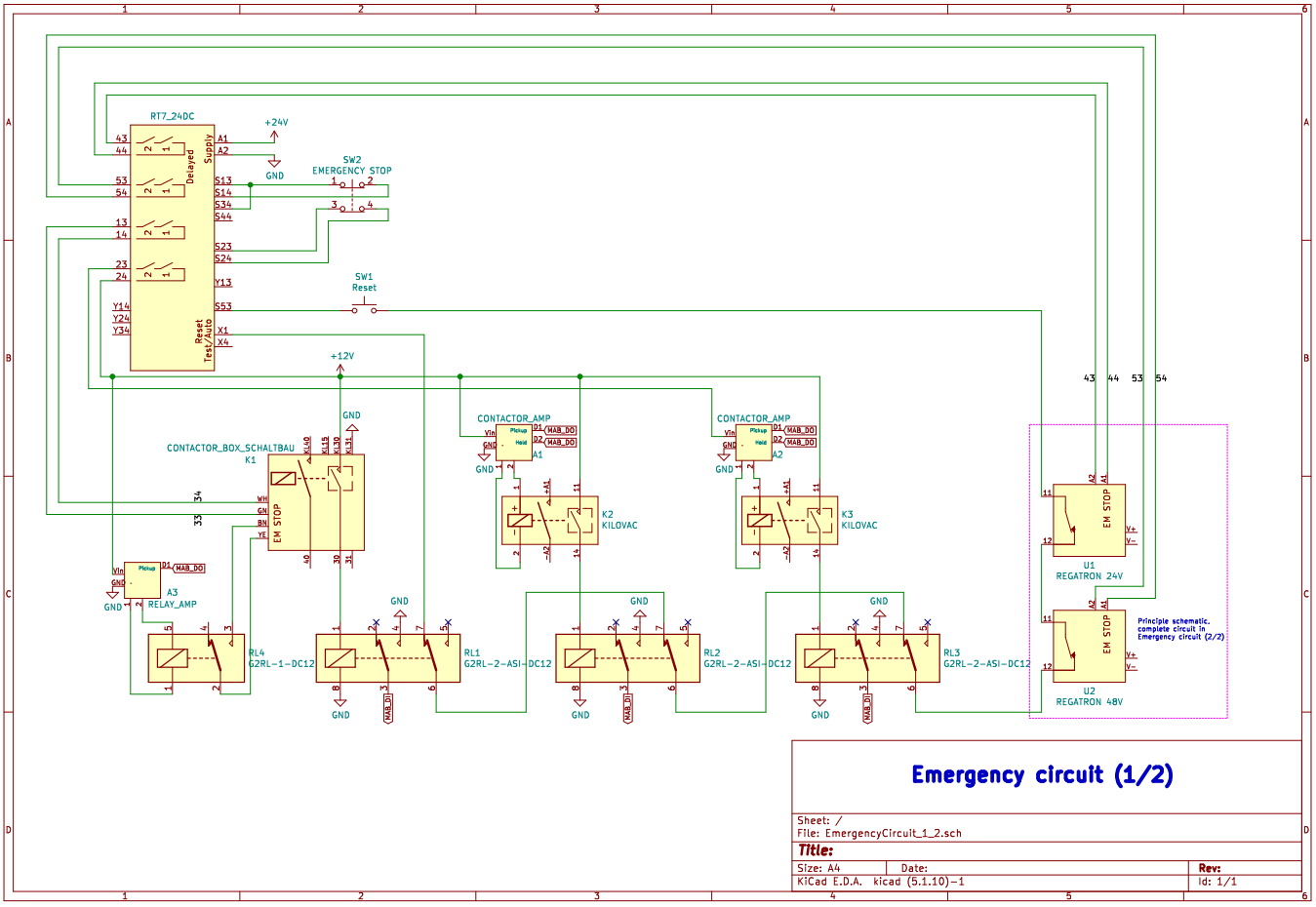

Fig. A.3. Emergency stop circuit 1/2.

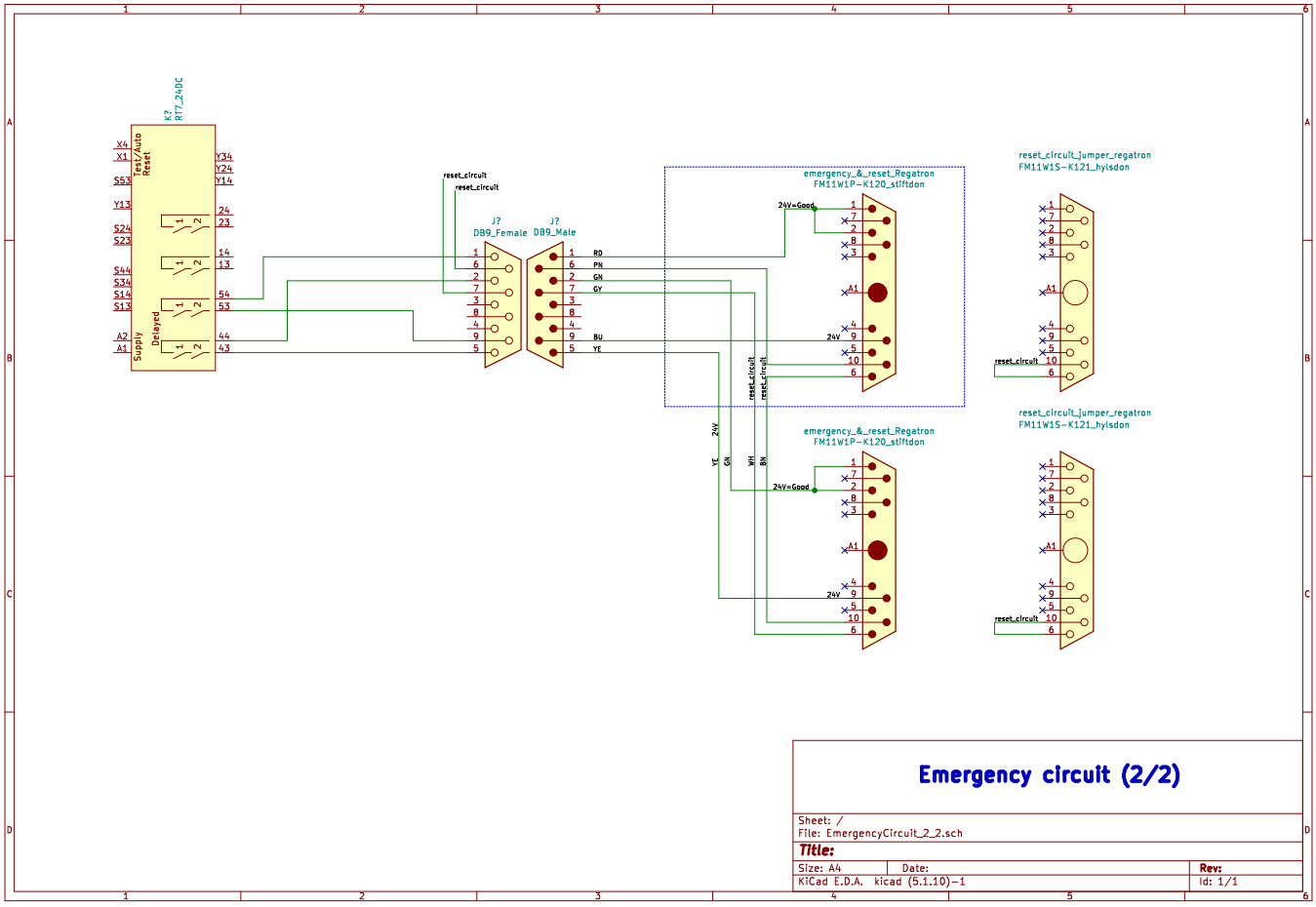

Fig. A.4. Emergency stop circuit 2/2.

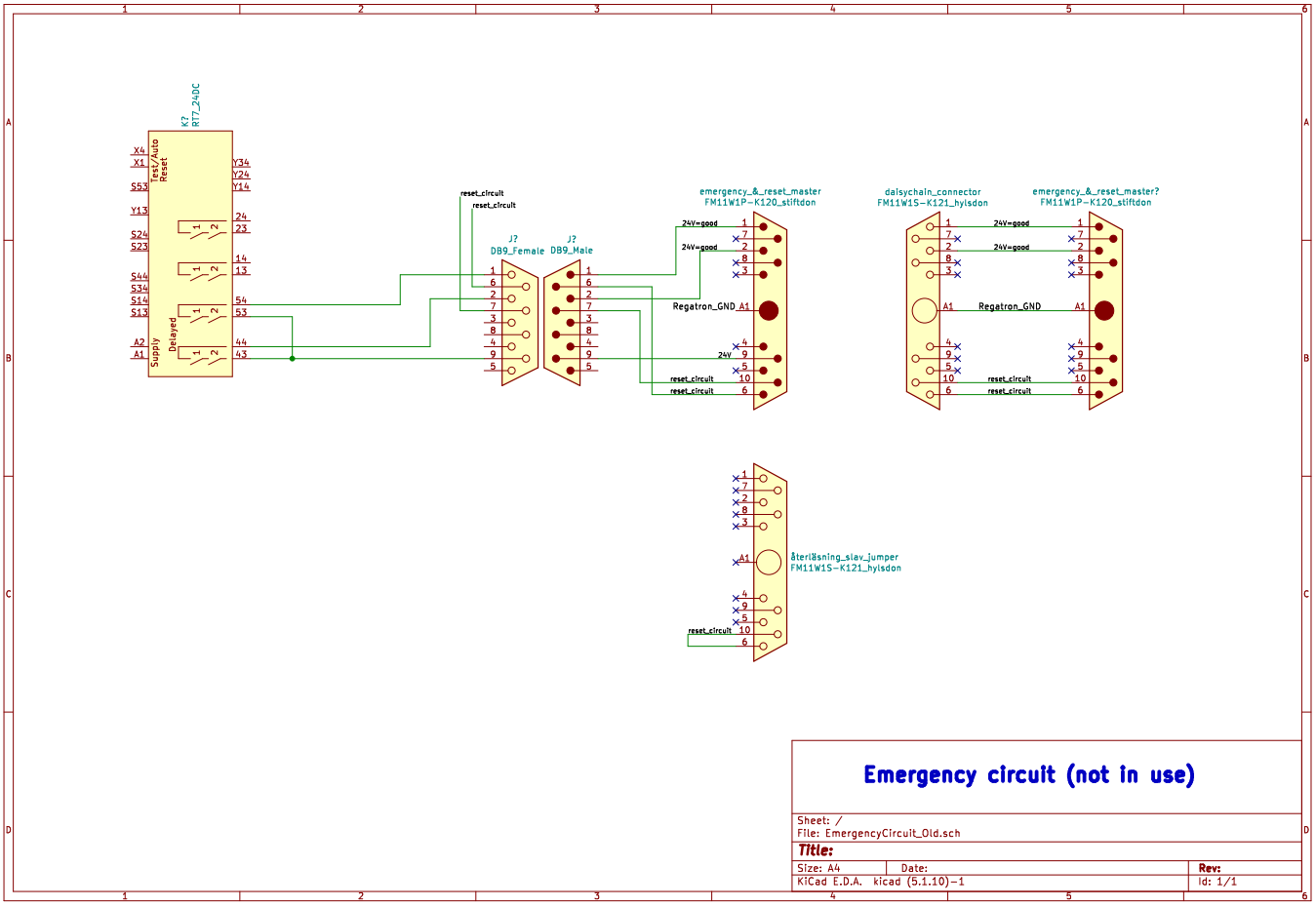

Fig. A.5. Old Emergency stop circuit 2/2.