LUND UNIVERSITY

MASTER THESIS PROJECT

Thermoelectric measurements on InAs nanowires with a ratchet-barrier

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Abstract

Efficient extraction of thermal energy from electrons at the micro- and nanoscale is a long-standing scientific goal that could enable novel types of heat engines, heat management, and solar cell applications. Semiconductor nanowires are a promising system for investigating such devices for several reasons, such as their thermoelectric properties, and the potential to be grown in heterostructures with high flexibility. This provides great potential to tune the nanowire properties to suit specific applications, for example to generate band structures that act as filters to extract charge carriers with specific energies. Such energy filters have previously been investigated in nanowires, including rectangular thermionic barriers and quantum dots, but have been limited in either conversion efficiencies or power output. It is therefore of interest to investigate other systems to function as energy filters. For example, the influence of the shape of a thermionic barrier on thermionic current extraction has not been explored in-depth. In order to expand the understanding of how to most effectively extract energy from energetic electrons, this master thesis aims to investigate whether an asymmetrically shaped thermionic barrier leads to an asymmetric thermoelectric response. For this purpose, thermoelectric measurements have been performed on indium arsenide (InAs) nanowires with a compositionally graded indium arsenide phosphide ($InAs_{1-x}P_x$) segment, forming an asymmetrically shaped potential barrier, using a top-heater architecture for applying temperature gradients along the nanowire. Thermoelectric currents were successfully generated as a result of a temperature gradient along the nanowire at ambient temperatures of 77 K and 300 K. At an ambient temperature of 77 K, asymmetric thermoelectric behaviour was demonstrated, with a generation of higher open circuit voltage when heating on one side of the barrier compared to heating on the other. This was proposed to be a result of the asymmetry of the barrier, and an indication that the shape of the barrier matters thermionic current extraction. The experimentally obtained results were compared to a theoretical model based on the WKB approximation, which captured some of the key features of the experimental results. At an ambient temperature below 1 K, indications quantum dot formation could be seen, further complicating the thermoelectric characterization and therefore such measurements were not further pursued.

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Contents

Acronyms

InAs indium arsenide

InAs$_{1-x}$P$_x$ (compositionally graded) indium arsenide phosphie

IV current voltage

I$_{SC}$ short circuit current

V$_{OC}$ open circuit voltage

1D one-dimensional

ALD atomic layer deposition

SEM scanning electron microscope

EBL electron beam lithography

Au gold

Ni nickel

IPA isopropanol

V$_{BG}$ back gate bias

V$_{SD}$ source-drain bias

V$_H$ heating bias

E$_F$ Fermi level

E$_C$ conduction band edge energy

E$_V$ valence band edge energy

Si silicon

SiO$_2$ silicondioxide

HfO$_2$ hafniumdioxide

1. Introduction

Classical heat engines can convert heat to usable work, but are not suitable for miniaturization as they rely on moving parts [1]. Thermoelectric energy conversion, on the other hand, provides a mean to convert heat to usable energy, for systems as small as the nanometer scale [2]. Nanostructures are also of interest for power production and for heat management, due to engineering potential of their thermoelectric properties [3] and the potential of obtaining high thermal-to-electric energy conversion efficiency [4], without moving parts [1].

One system of interest for nanoscale thermoelectrics are semiconducting nanowires [1, 4], elongated shapes with high length/diameter aspect ratio with diameters of ∼100 nm and below [5]. Nanowires can be grown in heterostructures with very high control and flexibility in material choices, including growth of lattice mismatched materials [5]. This flexibility in material choices offers great possibilities for band gap-engineering, i.e. combining different semiconductor materials with different band gaps [6]. Through band gap-engineering the band structure can be adapted to fit specific applications, for example, to create potentials that can act as filters to extract charge carrier of certain energies [7].

For example, well defined quantum dots in nanowires can be defined as energy filters [1, 8, 9], and it has been demonstrated that such a system can function as a heat engine with high conversion efficiency [4]. It has been theoretically assessed that the efficiency while operating at maximum power condition is higher for a one-dimensional system with a thermionic barrier, a barrier that transmits carriers of high energy, than a quantum dot [4]. Thermionic extraction has been observed in nanowires with a rectangular thermionic barrier, where a temperature difference is created by optical excitation, but with a low (quantum) efficiency [10]. It is therefore of interest to investigate alternative systems suitable for energy filtering. Investigating potential asymmetric thermoelectric behaviour for asymmetrically shaped barriers in nanowire devices could provide knowledge of the effects of barrier shape and hence how to engineer a barrier for optimal device performance. It has theoretically been assessed that a rectangular barrier with a so-called pre-barrier, an additional barrier segment (of positive potential) adjacent to the barrier but with lower height, has higher transmission than a rectangular barrier with no pre-barrier [11]. A triangular potential barrier could therefore have beneficial transmission properties as a triangular barrier can be seen as a barrier with many pre-barriers of increasing height. A stepwise, compositionally graded, triangular thermionic barrier embedded in nanowires has electrically been characterized

by Nylund et. al. [12], but no measurements to record thermionic response was conducted.

In this master thesis project, it has been investigated whether an asymmetrically shaped potential barrier result in asymmetrical thermoelectric response. For this purpose, indium arsenide (InAs) nanowires with a compositionally graded indium arsenide phosphite ($InAs_{1-x}P_x$) segment, forming an asymmetric, ratchet-like barrier were used. See figure 1 (bottom) for the band structure of the nanowire. A top-heating architecture was used for thermal biasing, where the heating contacts are positioned on top of the electrical contacts with an electrically insulating oxide layer between the electrical contacts and the heater contacts. See figure 1 (top) for a schematic illustration of the device.
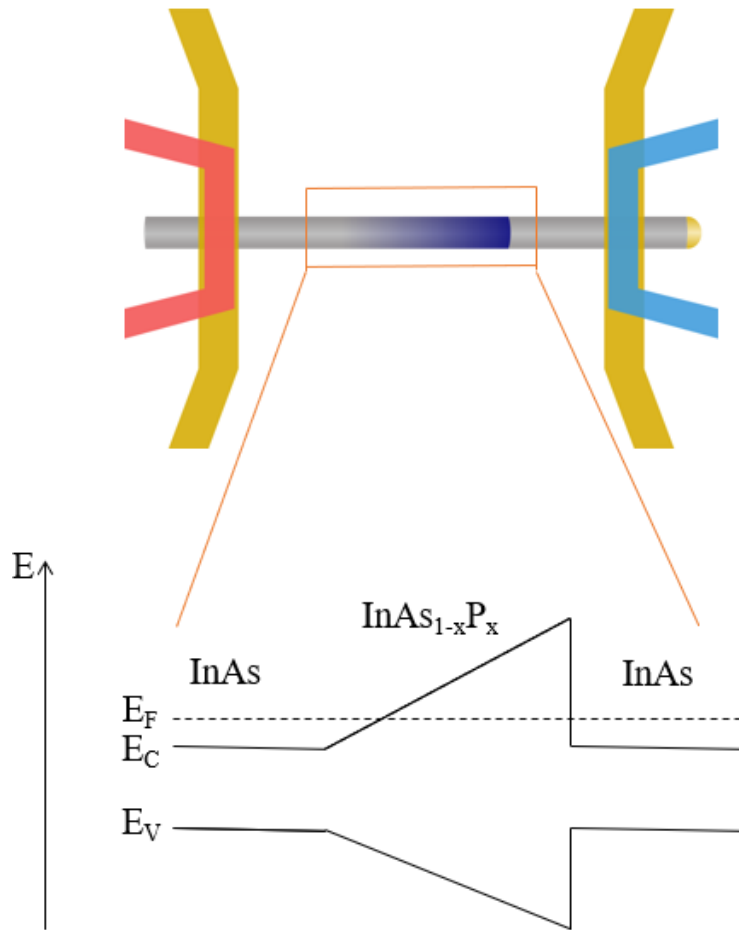
Figure 1: A schematic illustration of the device, with the band structure orientation indicated in relation to the gold seed and contacts. The nanowire is illustrated in grey with the barrier in blue. The golden seed is illustrated at the right end of the nanowire. The electrical contacts placed over the nanowire are indicated in yellow, and the heater contacts are indicated in red and blue.

The principle of performing thermoelectric measurements on a nanowire with

a ratchet-like barrier is to keep one side of the nanowire cold and the other side hot. In this project this is achieved by applying a heating bias ΔV_H on one of the heater contacts. This will create a temperature gradient along the nanowire and a temperature difference between the different sides of the barrier. The elevated temperature on one side of the barrier causes electrons on the heated side to have a higher probability of occupying states of high energy than the electrons on the cold side, in accordance with Fermi-Dirac statistics [13]. Therefore, electrons having a higher probability of crossing the barrier from the hot to the cold side, allowing for a thermionic current to flow over the barrier in one direction only. Figure 2 illustrates how heating on either side of the barrier effects the Fermi-Dirac distributions, which favours transport from the heated side across the barrier to the cold side, resulting in a current I. Heating on the ramp side of the barrier will be referred to as HR (heated ramp) and heating on the abrupt side of the barrier will be referred to as HA (heated abrupt). The current at no bias voltage across the barrier, at short circuit conditions, will be referred to as the short circuit current, I_{SC}. When an electron crosses the barrier from the hot side to the cold, the heat on the hot side will be reduced. Some heat will be transformed into electric work [1] and some as heat contribution to the cold side. A quantity which can be considered at the voltage where the current in the system is zero, which will be referred to as the open circuit voltage V_{OC}.
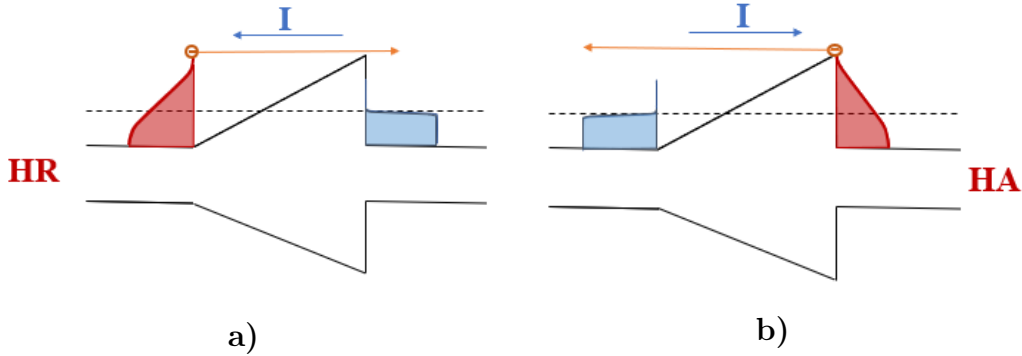
Figure 2: Illustrations of the short circuit current for heating on a) the ramp side (HR), and b) the abrupt side of the barrier (HA).

If an electrical bias is applied across the nanowire, referred to as source-drain voltage, V_{SD}, in this project, the bands will bend and the barrier shape will be altered, see figure 3. Such bending of the bands will affect carrier transport and possibly favour different transport mechanisms, dependent on the barrier shape. In the case seen to the right in figure 3, the barrier height will effectively be reduced seen from the left and will favour transmission over the barrier from the left to right. In the case to the left in figure 3, electrons can travel over

the barrier from right to left by thermionic emission, but with a reduction in effective barrier width this could also allow for tunnelling through the barrier. [12]
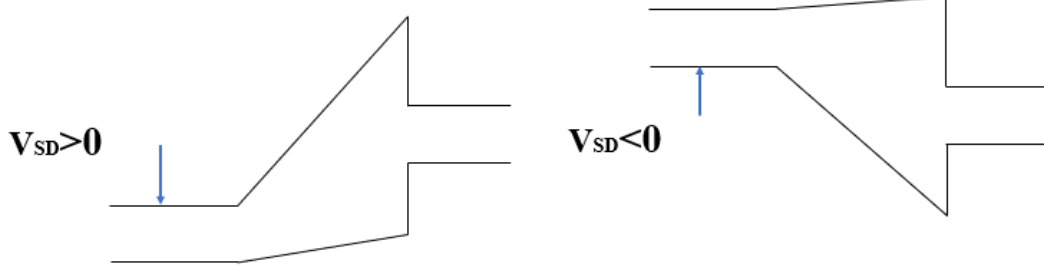
Figure 3: Schematic illustration of applying positive (left) and negative (right) V_{SD} on the ramp side of the barrier.

To investigate if an asymmetrical barrier result in asymmetrical thermoelectrical response, that is non-linear behaviour when applying a temperature gradient on the two sides of the barrier. To investigate this, thermoelectric measurements were performed, including current-voltage, IV, measurements and simultaneously applying a temperature gradient by heating of the device. From such measurements features such as short circuit current, I_{SC}, and open circuit voltage, V_{OC}, were extracted. Measurements were conducted in three ambient temperatures; 300 K, 77 K, and sub-1 K.

To gain further insight to the system, the experimental results were compared to a theoretical model based on the WKB-approximation (named after Wentzel–Kramers–Brillouin) where the current response was modelled when altering the applied bias, with and without a temperature difference across the barrier.

2. Theory

This section will introduce the relevant theory to understand the project. To start with, the energy distribution of electrons in a semiconductor will be presented. This will be followed by an introduction of nanowires, low dimensional effects, and transport in low dimensions. Finally, a presentation of ongoing research on thermal biasing, energy filters for carrier extraction, and ratchet-like barriers in nanowires will be given.

2.1. The Fermi-Dirac distribution

The energy distribution of electrons is important for the properties of the semiconductor, and it is dependent on the temperature. It will become evident throughout the report that the energy distribution of electrons is essential to understand thermoelectrical effects in for example semiconductor nanowire systems.

Just as for energy levels of a single atom the Pauli exclusion principle governs occupancy of a state to be either one or zero also in a semiconductor, and the probability that a state of a certain energy E is occupied by an electron is given by the Fermi-Dirac distribution function, often referred to the Fermi distribution, seen in equation 1. [13]

$$F(E) = \frac{1}{1 + e^{(E-E_F)/kT}} \tag{1}$$

where k is the Boltzmann constant, T is the temperature and E_F is the Fermi level. The Fermi level is the energy where the probability of a state being occupied is 50%. A main feature of the Fermi-Dirac distribution function is that it is symmetrical around the Fermi level. [13, 6] In figure 4 the Fermi distribution function is plotted for different temperatures. For T=0 K, the Fermi distribution function is a step function, but as T increases $F(E)$ becomes more spread out. This means that the probability of finding an occupied state at a higher energy increases with increasing temperature. [13]
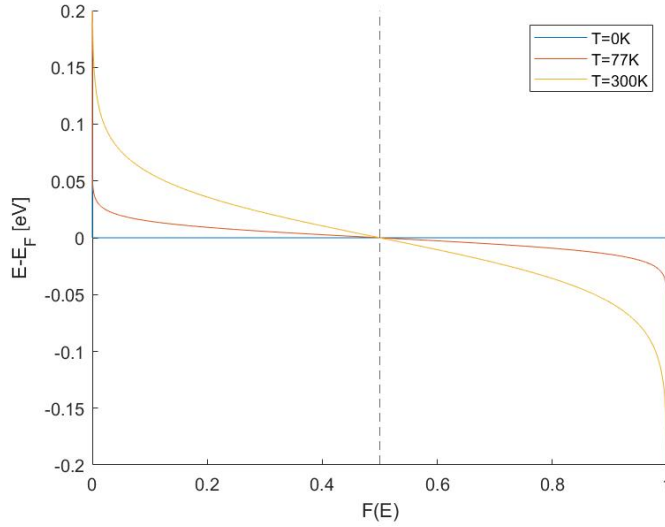
Figure 4: The Fermi-Dirac distribution function $F(E)$ vs $E - E_F$ for T=0 K, 77 K, and 300 K, the dashed line indicates $F(E)$=0.5. Inspired by [13].

2.2. Nanowires and low dimensional effects

Nanowires are structures that have diameters of one to hundreds of nanometres in diameters. Electrons are restricted in two dimensions and free to travel in one dimension. This is due to the limited depth and width but longer length of the structure, and nanowires are often referred to quasi-one-dimensional systems [5]. This section will introduce nanowire heterostructures and effects that become important in nanowires and with the low dimensional nature of nanowires such as Fermi level pinning, nanowire defects and formation of quantum dots.

2.2.1. Nanowire heterostructure

Nanowire heterostructures are nanowires that are grown with two or more materials [5]. Due to the small diameters of nanowires, they can sustain strain when combining materials of different crystal structures or lattice constants (simplified the distance between atoms in the crystal) without breaking and without dislocations at the interface [14]. This offers much more flexibility in obtaining heterostructures than in bulk structures [15]. Combining materials of different properties such as band gap creating heterostructures, often referred to as band engineering, offers the possibility to affect the behaviour of the charge carriers in a semiconductor and tune properties to specific applications. [6]

For example, InAs/InP has a lattice mismatch of 3.2 %, and InAs/InP is impossible to grow in bulk structures due to the large lattice mismatch. InAs/InP structures are, however, possible to grow as nanowires without the formation

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of defects such as dislocations. [16]

The energy required to completely remove an electron from a crystal is referred to as the vacuum level. When aligning the energy bands of different materials in heterostructures, the vacuum levels are always aligned. This is referred to as Anderson's rule. This gives that the bottom of the conduction bands of two different materials are separated by the difference between the value of the vacuum levels. A band diagram of a heterojunction can be drawn based on Anderson's rule, but it does, however, not give a full image of the discontinuities of the bands. [6]

There are three different types of alignment of bands. If the band gap of a material with the narrower band gap is enclosed in the band gap of the material with greater band gap, it is called type I alignment. If both the conduction band and the valence band edge are located at a higher energy compared to another material, but there is an overlap of band gap of the two materials, it is called type II alignment. If there is no overlap in bandgap, it is called type III alignment. [6]

2.2.2. Surface states and Fermi level pinning

At the surface of a semiconductor the translational symmetry of the crystal lattice is broken, resulting in electronic surface states that differ from the bulk states. These electronic surface states can have either donor or acceptor character, and depending on whether these states are occupied or not, they can be charged or uncharged. Charging of the surface states will cause a formation of a space charge layer in the near-surface region, and the valence and conduction band will bend either upwards or downwards in respect to the Fermi level to ensure that the condition of surface charge neutrality is satisfied. [17, 18] As a result, the energy required to extract an electron from the bulk will practically not depend on the Fermi level of the bulk, a phenomenon referred to as Fermi level pinning [19]. These phenomena are important for nanowires due to the large surface-to-volume ratio, and surface effects can dominate [20].

2.2.3. Nanowire defects and electronic properties

Defects in nanostructure can have sever effects on electronic properties [21, 22, 23, 24]. Defects, such as surface defects, stacking faults and charge defects, can lead to trapping of charge carriers. Trapping and detrapping of charge carriers can cause the electrostatic potential to vary along the nanostructure and can change in time [21]. This, in turn, affects the conductance and the carrier mobility of the nanowire [22, 25]. These effects can also cause quantum dots, regions where carriers are limited in all three dimensions [6], to form in

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low temperature environments [22]. The electrical characteristics of quantum dot will be given below.

2.2.4. Quantum dots

A quantum dot is a system where a carrier is restricted in all three spatial dimensions. A quantum dot has a discrete spectrum of energy levels, which has led to quantum dots often being referred to as artificial atoms [7, 26]. Due to Coulomb interaction between electrons the electronic states of the quantum dot will be sensitive to the number of electrons present [26]. If the quantum dot, often referred to as an island, is connected to a charge reservoir and there is only a weak tunnel coupling between reservoir and island, single electron tunnelling can be observed in the system. Transport through quantum dot systems is often discussed in terms of the capacitance of the system. For an island that has the self-capacitance C_Σ, the cost of adding an electron, the charging energy of the system is e^2/C_Σ, where e is the elemental charge [26, 27]. If the charging energy is larger than the thermal energy of the system, no current can pass through the island, this phenomenon is called Coulomb blockade [27]. Within the quantum dot the energies will be quantified, referred to as resonant energy levels. [6]

If considered in one dimension, if a bias V_{SD} is applied over the quantum dot with a sea of electrons on either side the chemical potentials, the quasi-Fermi levels of the reservoirs, will not be aligned. If a resonant energy level is positioned between the chemical potential on either side of the quantum dot electrons can flow through the quantum dot via the resonant energy level which can contribute to current. An applied gate voltage V_{BG} will shift the energy of the resonant levels within the quantum dot, and if the bias over the quantum dot is small, current will flow for only some values of the back gate creating peaks, so called coulomb peaks, in the current response. [6] The current can also be plotted as a function of both V_{SD} and V_{BG}, in such diagram rhomb shapes will appear, called coulomb diamonds, for the combinations of V_{SD} and V_{BG} the current is blocked. Some features appear clearer if the differential conductance $G = dI/dV_{SD}$ is plotted in place of the current. [7]

2.3. Transport in low dimensions

Heterostructures will affect the carrier behaviour in the nanowires [7, 6], due to variations in the potential landscape. As transport does not behave classically in low dimensions [6], some additional features must be considered. Below is a description of what happens at potential step, the concept of tunnelling, the WBK theory which is an approximative method to find the transmission

function will be introduced, and current across a barrier in one dimension will be described.

2.3.1. Transmission at a potential step

Consider a potential landscape in the x-direction with potential $V(x < 0){=}0$ and a potential step at $x = 0$ of height V_0 such that $V(x > 0){=}V_0$. An electron with an energy $E > V_0$ moving across the potential step from $x < 0$ to $x > 0$ would classically always pass. But if the problem is viewed quantum mechanically, the wavelike nature of the electron will give rise to two outgoing waves at the potential step, one transmitted wave and one reflected wave. This would also be true for an electron of energy $E > V_0$ passing the potential step from $x > 0$ to $x < 0$. [6]
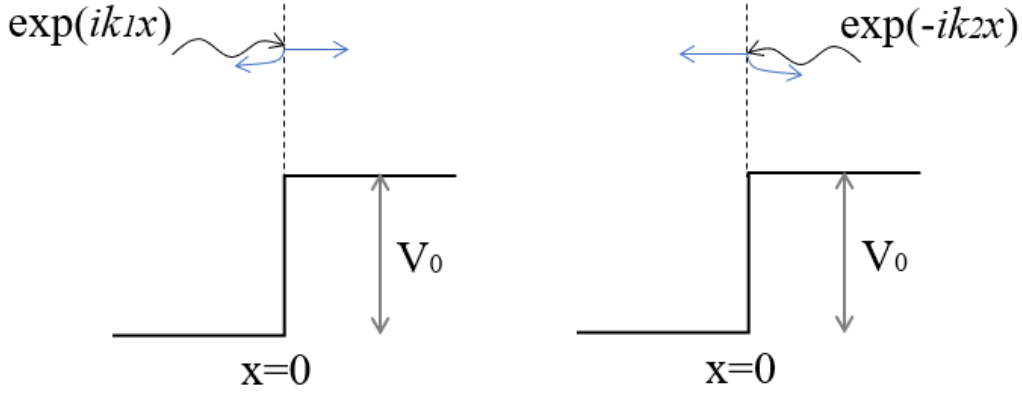

Figure 5: An incoming wave at a potential barrier form the left (left in image) and from the right (right in image), in black, and transmission and reflection of the wave illustrated in blue.

The wavefunction of a particle, ϕ, can be found by solving the Schrödinger equation, presented here as the one-dimensional time-independent Schrödinger equation

$$\left[-\frac{\hbar^2}{2m}\frac{d^2}{dx^2} + V(x)\right]\phi(x) = E\phi(x), \tag{2}$$

Where $\hbar$ is the reduced Planck's constant, m is the mass, $V(x)$ is a varying potential, and E is the energy. The form of the wavefunction of the free electron, where $V(x){=}0$, is $F\exp(ikx)$, where F is the amplitude, and k is the wave number. There will also be a temporal factor $\exp(-iEt/\hbar)$, where t is the time, but this term will be ignored in this section as it is the same for all waves. If the problem is considered generally and one wave on either side of the potential step is travelling in the $+x$ direction and one wave on either

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side of the potential step is travelling in the $-x$ direction, the solutions to the Schrödinger equation ϕ will be given by

$$\phi(x) = \begin{cases} Aexp(ik_1x + Bexp(-ik_1x), & \text{x} < 0, \\ Cexp(ik_2x + Dexp(-ik_2x), & \text{x} > 0, \end{cases} \tag{3}$$

where A, B, C, and D are the amplitudes of the waves, k_1 is the wave number for $x < 0$ and is given by $k_1 = \sqrt{2m_1E/\hbar^2}$, where m_1 is the effective mass for the medium of $x < 0$, and k_2 is the wave number for $x > 0$ and is given by $k_2 = \sqrt{2m_2(E - V_0)/\hbar^2}$, where m_2 is the effective mass for the medium of $x > 0$. The wavefunctions as well as the derivative of the wavefunctions must be continuous at the potential step, which for $x = 0$ gives

$$\begin{cases} A + B = C + D, \\ k_1(A - B) = k_2(C - D). \end{cases} \tag{4}$$

For the system of equation in equation 4 to be solvable, there can only be two unknowns of the system. [6] Instead of the amplitude of the waves, the current or flux is usually of interest. The current density of the wave $Fexp(ikx)$ is given by $(\hbar k/m) \mid F \mid$. To find the ratio between the reflected current and the incoming current, called the reflection coefficient R, the current density of the reflected wave is divided with the incoming wave. Similarly, to find the corresponding transmission coefficient T, the current density of the transmitted wave is divided by the incoming wave. Note that $T + R = 1$. [6]

2.3.2. Tunnelling

If the electron in the problem above instead has an energy of $E < V_0$ approaching the potential step from $x < 0$, it would classically always be reflected at the barrier. But if viewed quantum mechanically, the wavefunction will penetrate the barrier. The wave number within the barrier will be $\kappa = \sqrt{2m_2(V_0 - E)/\hbar^2}$, and the outgoing wave in the barrier will be given by the exponentially decaying function $Cexp(\kappa x)$, and similarly, the wave in the $-x$ direction for $+x$ will be a growing exponential function $Dexp(\kappa x)$. If the transmission and reflection coefficient are calculated as mentioned above, one would find that $T=0$ and $R=1$, indicating perfect reflection. Unlike the classical point of view, the quantum mechanical point of view gives an exponential tail in the barrier, but it does not contribute to a current. [6]

If the barrier is of finite thickness, however, the fact that the wave function extends into the barrier also imply that there is some probability of carriers to reach the other side of the barriers. This phenomenon of a carrier to travel through a potential barrier is called tunnelling. [7]

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2.3.3. WKB: an approximative method to find the transmission function

Finding the transmission of a barrier is often not trivial. For many barrier problems it is very difficult or even impossible to find analytical solutions for the transmission [6]. Instead, approximate methods or numerical methods can be used. One approximate method applicable for a triangular barrier, and hence possibly for the barrier of the nanowires in this project, is the WKB theory, named after Wentzel, Kramers and Brillouin. [6] below is an introduction to the main ideas of the WKB theory, but the theory and its limitations will not be discussed in full, and the interested reader can find further discussion on the subject in e.g. [6] chapter 7.4.

The WKB theory can be used to solve the Schrödinger equation where the potential can be approximated to change slowly in space. As discussed in section 2.3.3, a particle travelling in a landscape of a constant potential can be described with the wavefunction $\exp(ikx)$, where $k = \sqrt{2m(E-V)/\hbar^2}$. If the potential V is varying in space, k can be expanded to $k(x) = \sqrt{2m(E-V(x))/\hbar^2}$, $V(x)$ is the potential varying in space. The phase will in the case of a constant potential landscape change linearly, kx, but in a varying potential landscape this will no longer be true. [6]

The phase can be set to $\chi(x)$, giving the wavefunction $\Phi(x)=\exp(i\chi(x))$. and $k(x)$ is the local wave number introduced to account for a varying $V(x)$. By substituting this into the time-independent one-dimensional Schrödinger equation, equation 2, this gives

$$[\chi']^2 - i\chi''(x) = \frac{2m}{\hbar^2}\big[E - V(x)\big] \equiv k^2(x). \tag{5}$$

If the potential is varying slowly, the second derivative, $\chi''(x)$, is small, and $\chi(x)$ can be approximated as

$$\chi(x) = \pm \int^x k(x')dx' \tag{6}$$

To further develop the solution of the WKB approximation, the approximation in equation 6 can be used in the equation for $\chi(x)$ as

$$\left[\chi'\right]^2 = k^2(x) + i\chi''(x) \approx k^2(x) \pm ik'(x) \tag{7}$$

By taking the binomial expansion of the square root of the expression in equation 7, $\chi'(x)$ can be approximated as

$$\chi'(x) \approx \pm k(x)\sqrt{1 + \frac{ik'(x)}{k^2(x)}} \approx \pm k(x) + \frac{ik'(x)}{2k(x)} \tag{8}$$

This expression can be integrated to find $\chi(x)$

$$\chi(x) = \pm \int k(x)dx + \frac{i}{2}lnk(x) \tag{9}$$

resulting in a wavefunction

$$\Phi(x) \approx \frac{1}{\sqrt{k(x)}}exp\left(\pm i \int^x k(x')dx' \right) \tag{10}$$

To consider tunnelling $k(x)$ can be substituted with $\kappa(x) = \sqrt{(V(x) - E)/\hbar^2}$ and removing the i in the exponent in equation 10. The transmission function for tunnelling through a barrier can then with the WKB approximation be written as

$$T \approx exp\left[-2 \int_{x_L}^{x_R} \kappa(x)dx \right], \tag{11}$$

where x_R and x_L are the edge points of the barrier. [6]

2.3.4. Current across a barrier in one dimension

The current across the barrier can be described using the Fermi distributions on either side of the barrier and the transmission function across the barrier. If considering a barrier with a surrounding sea of electrons, electrons impinge the barrier from both sides. The current can be found if the current contributions from either side of the barrier are summed. The current contribution from the left side, I_L of the barrier can be described by

$$I_L = \frac{2e}{h} \int_{E_{C,L}}^{\infty} f(E, \mu_L)T(E)dE, \tag{12}$$

where e is the elemental charge, h is Planck's constant, $E_{C,L}$ is the conduction band edge on the left side, $f(E, \mu_L)$ Fermi distribution function dependent on the energy E and chemical potential μ_L on the left side and the energy dependent transmission function $T(E)$. Similarly, the current contribution from the right side, I_R of the barrier can be described by

$$I_R = -\frac{2e}{h} \int_{E_{C,R}}^{\infty} f(E, \mu_R)T(E)dE, \tag{13}$$

where $E_{C,R}$ is the conduction band edge and the chemical potential μ_R on the right side. Note that I_R is defined as negative, this is due to the electron flow will be opposite to that from the left side. Summing the two current contributions give

$$I = I_L + I_R = \frac{2e}{h} \int_{E_{C,L}}^{\infty} f(E, \mu_L)T(E)dE - \frac{2e}{h} \int_{E_{C,R}}^{\infty} f(E, \mu_R)T(E)dE =$$

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$$= \frac{2e}{h} \int_{E_{C,max}}^{\infty} (f(E, \mu_L) - f(E, \mu_R)) T(E) dE \qquad (14)$$

where $E_{C,max}$, is the larger of $E_{C,L}$ and $E_{C,R}$, as no transport can be conducted for energies between $E_{C,L}$ and $E_{C,R}$. The final equality can be written as the transmission coefficient is the same from either side of the barrier, due to time reversal invariance of the system (that time does not have a preferred direction) and that current must be conserved. [6]

As can be seen in equation 14, the current is dependent on the temperature on each side. A temperature difference between the two sides of a barrier, e.g. from an applied temperature gradient, can result in current generation, called thermocurrent [28]. At a barrier or energy filter heating of one side of the barrier can lead to electrons gaining sufficient energy to pass over the barrier. Such electron flow can result in a current. [7] Additionally a transmitted electron from the hot side to the cold side of the barrier, can result in voltage generation, called thermovoltage [28]. Such transmitted electron will contribute to some heat transfer from the hot side to the cold side as well as electric work [7].

2.4. Ongoing research and progress on methods for thermal biasing, energy filters and ratchet-like barriers

Thermoelectric characterization of nanostructures has gained interest in the resent years, much due to possible advantageous properties for direct thermal-to-electric energy conversion in nanostructures [29]. Nanostructures are being considered for thermal transport applications such as hot-carrier optoelectronic devices [1, 30], heat engines and on-chip coolers [1]. This section gives a short introduction to ongoing research in field, focused on nanowires and progress using different energy filtering profiles for carrier extraction. First some progress in thermal biasing methods will be given followed by a discussion and progress of different types of energy filters in nanostructures. As it has been predicted that a graded potential barrier could offer beneficial transmission properties [30], the ratchet-like barrier is of interest in the context, and previous studies of electrical characterization of nanowires with a ratchet-like barrier will be presented.

2.4.1. Methods for thermal biasing

Finding suitable techniques for thermal biasing of nanostructures at low temperatures come with several challenges. Including unwanted global device heating, unwanted gating effects, and continuous tuning of the thermal bias [29]. Thermal biasing of nanostructures can be achieved by heating one of the leads,

whilst keeping the other side cold [7, 29]. The heating mechanism is conventional Joule heating, achieved by running a current through a resistive element. The Joule heat should then be transferred from the resistive element to the nanostructure [7]. There are several options for placement of the resistive element, including side heating, contact heating and top heating.

With side-heating, thermal biasing of the device is not a concern [7], however, as the method relies of heating of the substrate a high heating power P_H is required which can lead to a rise in the ambient temperature, making measurements in low temperatures impossible. A large ambient temperature of the whole nanostructure can be much larger than the temperature difference between the hot and cold contact ΔT [7, 29].

Another method for thermal biasing of nanostructures is to directly lead a heating current through the contact leads, resulting in local heating and the method is convenient in a nanostructure processing point of view. The main disadvantage of the method is that by leading a heating current through the leads electrical biasing is introduced, and it is difficult to use it and simultaneously as doing measurements of thermovoltage V_H or current I_H. [7]

Gluschke et al. [29] has introduced an alternative method for thermal biasing of nanostructures referred to as top-heating. In this approach a heater lead is placed on top of the electrical lead, with an insulating layer between the leads. This has been proved to achieve a high local heating using a small heating power also allowing for usage of back-gate and to tune the temperature difference freely [29]. The disadvantage of the method is that it requires more advanced fabrication in several steps, as the electrical leads and the heater leads must be done in two different lithographic steps and separated by an insulating material [7].

The top-heating approach has been previously evaluated as a method of performing thermoelectric measurements on single InAs devices In that case, a four-probe geometry allowed for thermometry by determination of the temperature dependence of the resistances of the electrical leads. The heating power, the power required to run a heating current through the top heater, was stated as $P_H = V_H^2 R_H / (R_H + R_S)^2$, where R_H was the total heater resistance and R_S was a serial resistance connected to the on-chip heater. It was found that the temperature of the heated contact, as well as the temperature difference ΔT between the electrical contacts, increased linearly with the heating power, while global heating effect on ambient temperature was negligible. [29]
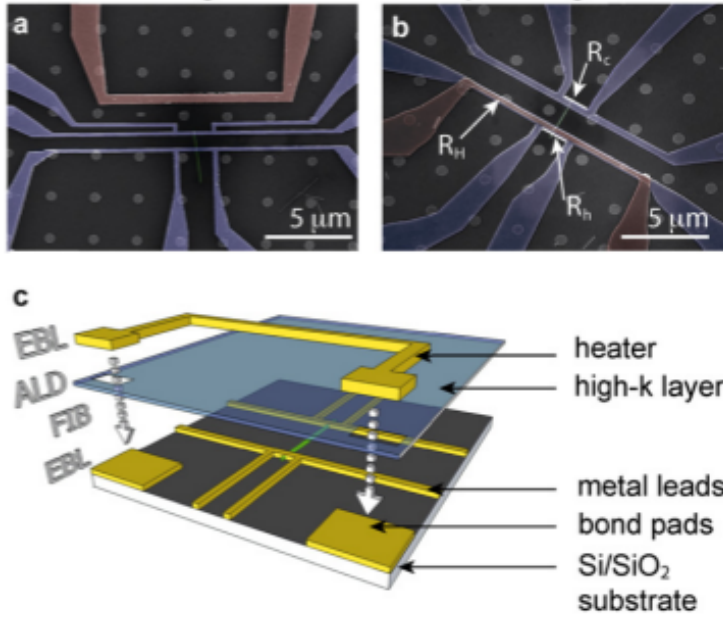
Figure 6: SEM images with electrical contacts indicated in blue and the heating contact indicated in red of a) a side heater device and b) a top-heating device, with the resistances of the heated metal lead and cold metal lead R_h and R_c, and the resistance of the heater R_H. c) is a schematic illustration of the layer structure of a top-heating device, with indicated required processing steps to the left and the device components to the right. Reprinted from [29]

2.4.2. Energy filters for carrier extraction

Traditional cyclical heat engines require moving elements, causing miniaturization to be difficult and limits low-power applications. The thermal efficiency of traditional engines is also bound by the Carnot limit, with the best Stirling engines reach a thermal efficiency of about half the Carnot limit. An alternative to the traditional engines is particle exchange (PE) heat engines, where an energy filter controls a thermally driven particle flow. In difference to traditional engines, PE heat engines require no moving elements and can be achieved in solid state materials and are therefore good candidates for low-power applications and for downsizing of components. [1]

Previously, a PE heat engine has been realized through epitaxially defined quantum dots within single nanowires [1, 8, 9], see figure 7 a) for a semiconductor nanowire defined quantum dot. The two sides of the quantum dot form electron reservoirs, tunnel-coupled by the quantum dot with tunnelling rate of Γ. The resonance energy ε_0 can be tuned in relation to the chemical potentials of the cold and hot side, μ_C and μ_H, by applying a back gate bias, using top-heaters for thermal biasing of the quantum dot. If the resonance energy is positioned such that the electronic state occupancy at the energy ε_0

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at the heated side is higher than of the cold side, the temperature difference can result in a current I, see figure 7 b). [1]
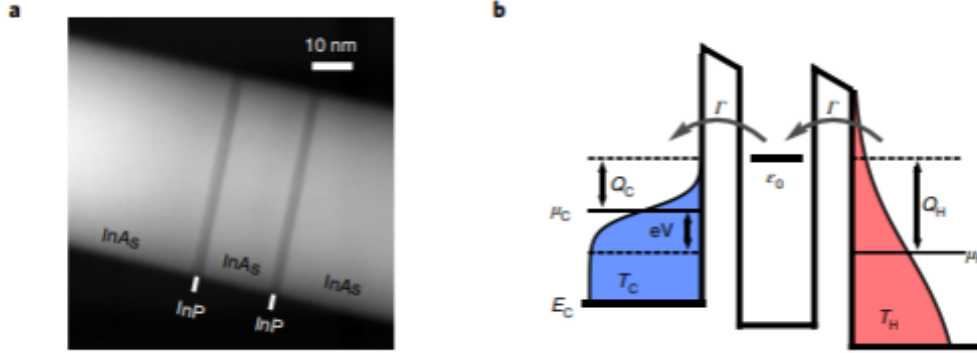

Figure 7: a) SEM image of the InAs nanowire with the two InP segments, and b) an illustration of the quantum dot heat engine, with indicated resonant energy level ε_0, the conduction band energy E_C, the tunnelling rates Γ, the temperatures $T_C < T_H$, chemical potentials μ_C and μ_H, and Fermi-Dirac distributions in blue and red of the cold and hot side respectively. An electron travelling through the quantum dot from the hot reservoir via the resonant level will reduce the heat of that side of Q_H, part of which will be transformed into the work eV and the rest will be a heat contribution of Q_C to the cold reservoir. Image reprinted from [1].

Josefsson et. al. [1] demonstrated high efficiencies for heat engines based on quantum dots defined in semiconductor nanowires, and that nanostructures are of interesting for thermal-to-electric energy conversion and has potentials as heat engines. However, the power that could be extracted from the quantum dot heat engine was low [1]. The low power output for a quantum dot energy-selective filter is due to a delta-like transmission function through a quantum dot, and to achieve higher power a broadening of the transmission function is required [4]. The achievable efficiency while systems deliver maximum power has been theoretically analysed and found to be higher in a one-dimensional thermionic barrier than a quantum dot [4]. Using a rectangular thermionic barrier thermionic extraction has been observed where a temperature difference is created by optical excitation [10]. An illustration of a rectangular barrier with a temperature difference across the barrier can be seen in figure 8. The (quantum) efficiency was, however, low [10]. It is therefore of interest to investigate alternative systems for thermionic extraction.

Figure 8: An illustration of a rectangular barrier with a temperature difference across the barrier, with the Fermi distribution functions indicated on either side of the barrier.

Nylund et. al. [12] has realised an asymmetric, ratchet-like barrier in a semiconductor nanowire and demonstrated asymmetric current response under (electrical) bias conditions, discussed in more depth in section 2.4.3 below. It is therefore of interest to investigate an asymmetric ratchet-like barrier in a semi-conductor nanowire to identify possible asymmetrical thermoelectric response, as this could mean that the thermionic emission is facilitated in one direction. Additionally, transmission properties have theoretically been analysed at a barrier with so-called pre-barriers, an additional barrier segment adjacent to the barrier, with aim to suppress electron reflection at the barrier. A pre-barrier of a positive potential, lower than the barrier height, exhibited higher transmission than the case of no pre-barrier. [11] A stepwise, or triangular, barrier, which can be seen as a barrier with many pre-barriers of gradually increasing height, could therefore have favourable transmission properties compared to a rectangular barrier with no pre-barrier.

2.4.3. Electrical properties of the ratchet-like barrier

Electronic transport through an InAs nanowires with a ratchet like barrier has been explored as a function of ambient temperature by Nylund et. al [12]. A ratchet shaped barrier is created by stepwise changing the composition $InAs_{1-x}P_x$ from x = 0 to x= 1, see figure 9 f). The structure results in asymmetry of the current-voltage, IV, characteristics see figure 9 f). This asymmetry originates from the asymmetry of the barrier, resulting in different potential landscapes depending on the direction and sign a potential is applied. As depicted in figure 9 b), when applying a small (the applied voltage is smaller than the barrier height) positive bias at the nanowire end closest to the sharp end of the barrier, some electrons will be able to pass the barrier by thermionic emission, see figure 9 c). If the voltage is increased to greater than the barrier height a large current was observed, as the barrier effectively was eliminated, see figure 9 d). Applying a negative bias to the same side resulted in a much smaller current, in line with that electron injection only being possible through thermionic emission or thermionically assisted tunnelling (made possible as the applied voltage change the effective barrier width), see figure 9 e). [12]
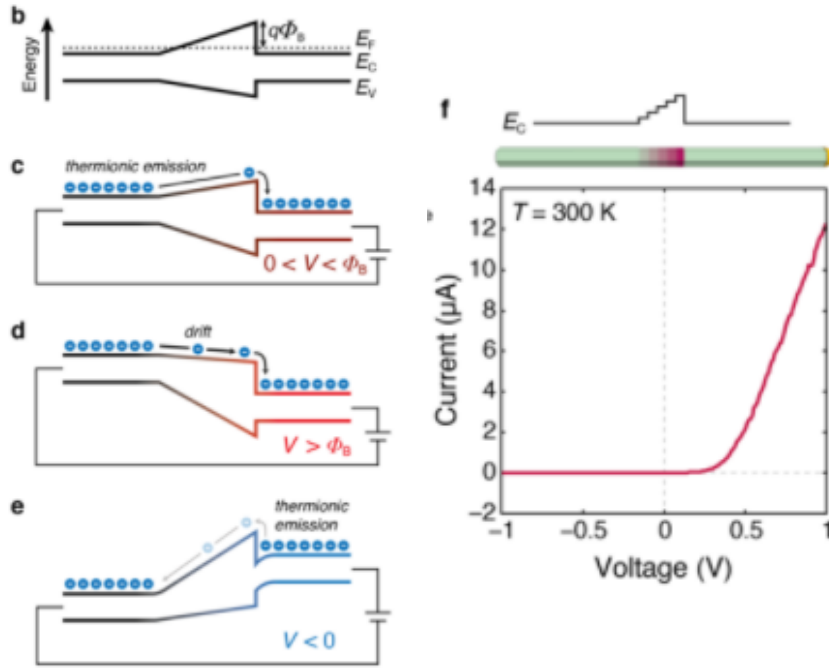
Figure 9: b) simplified band structure nanowires (note that the band diagrams has been drawn smoothly instead of sawtooth-shaped for simplicity), c)-e) schematically drawn band diagrams under bias f) conduction band of the stepwise, compositionally graded InAs/InAs$_{1-x}$P$_x$ nanowires, illustration of the nanowire and IV characteristics. Image reprinted from [12].

3. Experimental details

In this section the experimental details and methodology of the project will be described. First the growth details and resulting band structure of the nanowires used in this project will be presented, followed by a description of the single-nanowire device structure and the fabrication steps necessary to realize it, including electrically interfacing it. Finally, a short description of how measurements were conducted at various ambient temperatures will be given.

3.1. The nanowire and band structure

The nanowires used in the project are InAs nanowires with a compositionally graded barrier of InAs$_{1-x}$P$_x$, with a diameter of 75 nm, the barrier length is 100-200 nm and is located at about 1100 nm from the gold seed particle grown by Mukesh Kumar, see figure 10 for a transmission electron microscope image (TEM) of the nanowire. A description of the nanowire growth is given in appendix A.
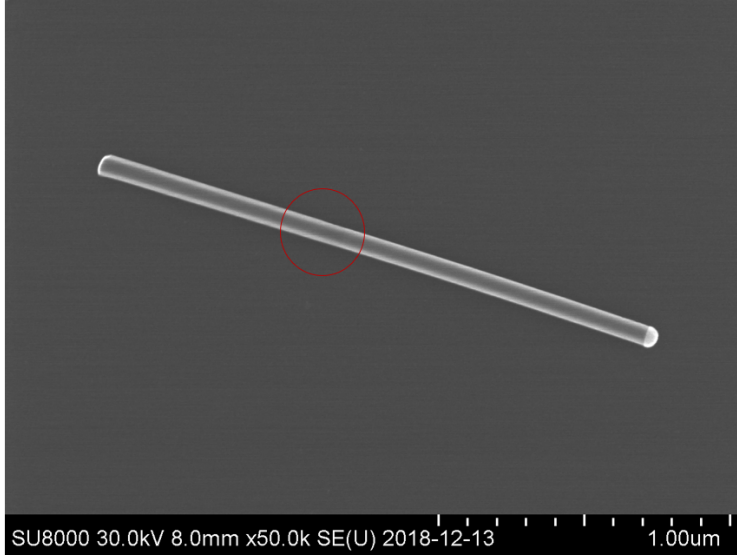
Figure 10: A TEM image of the nanowire, with the barrier marked with a red circle.
Image provided by Mukesh Kumar.

The band structure for an InAs nanowire with a compositionally graded barrier of $InAs_{1-x}P_x$, where x indicates the percentage of P and extends from 0 to 1, can be evaluated in terms of Anderson's rule.

The increase of percentage of P can be seen as continuous and adjacent heterojunctions from pure InAs to pure InP. According to Anderson's rule the vacuum levels will be aligned throughout the barrier. By using the electron affinities χ, the energy from the bottom of the conduction band to the vacuum level, and the bandgaps of the materials used the full band structure can be illustrated. The electron affinities and bandgaps at T=0K and at T=300K of InAs and InP can be seen in table 1. [6]

Table 1: The electron affinities χ and bandgaps at T=0K and at T=300K of InAs and InP. Values taken from [6].

	InAs	InP
χ (eV)	4.92	4.38
$E_g(T$=0K) (eV)	0.42	1.42
$E_g(T$=300K) (eV)	0.35	1.34

Electrons in InAs accumulate at the surface due to high densities of donor-type surface states and the Fermi level at the surface is thus pinned above the conduction band edge [6, 16, 20]. There is also potential presence of unintentional doping of carbon atoms acting as donors introduced at growth, causing n-type behaviour in InAs nanowires. In an unbiased system, the Fermi level have been found to pin above the conduction band edge for InAs nanowires.

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[16] Due to dominating surface properties of nanowires, the Fermi level will be considered to be located over the conduction band edge in all discussions.

An illustration of the band structure at $T=0K$ of the heterostructure used in this project can be seen in figure 11. Note that the band structure at $T=300K$ would be very similar, only with a reduction of bandgap of 0.07 eV and 0.06 eV for InAs and InP respectively, calculated from values from [6].
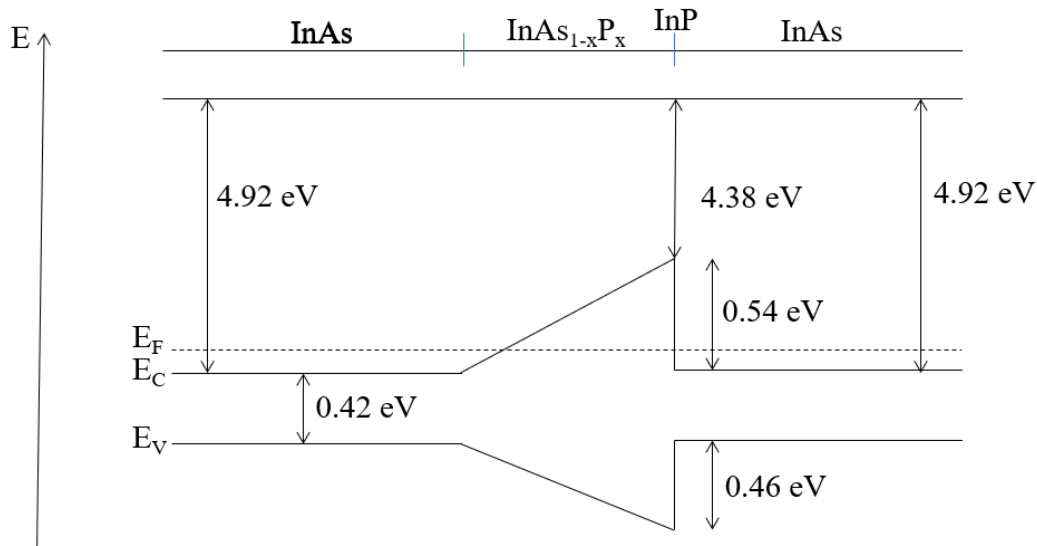

Figure 11: A schematic illustration of the band structure with indicated E_F, E_C and E_V, and including the values for the electron affinities and relevant band properties for InAs and InP at $T=0K$. Image not drawn to scale, values calculated from [6]

The band alignment can be seen to be of Type I, see section 1.2.1, so that both electrons and holes will be restricted by the InP barrier.

3.2. The device layout

In this work, single nanowires are deposited on top of a 5x3 mm Silicon substrate, referred to as the measurement chip, before further fabrication of metal contacts. The measurement chip is approximately 1 mm thick, and heavily n-doped to be conducting even at low temperatures. To electrically insulate the nanowire from the conducting Silicon, the top is covered by a layer of approximately 100 nm of SiO_2, see figure 12. In this way, if an electrical voltage is applied to the n-type Si, it will change the electrical potential uniformly for any device deposited on top of the SiO_2. Such a functionality is referred to as a back gate. On top of the chip, a gold pattern has been deposited that defines 10 fields with 12 contacts to each field, see figure 12 a) and b). Each field has a background of dots vertically and horizontally spaced of 2.5 μm forming a coordinate system, see figure 12. Origo of the system is found at the centre of each field and each, and every 10 μm has a larger marking.
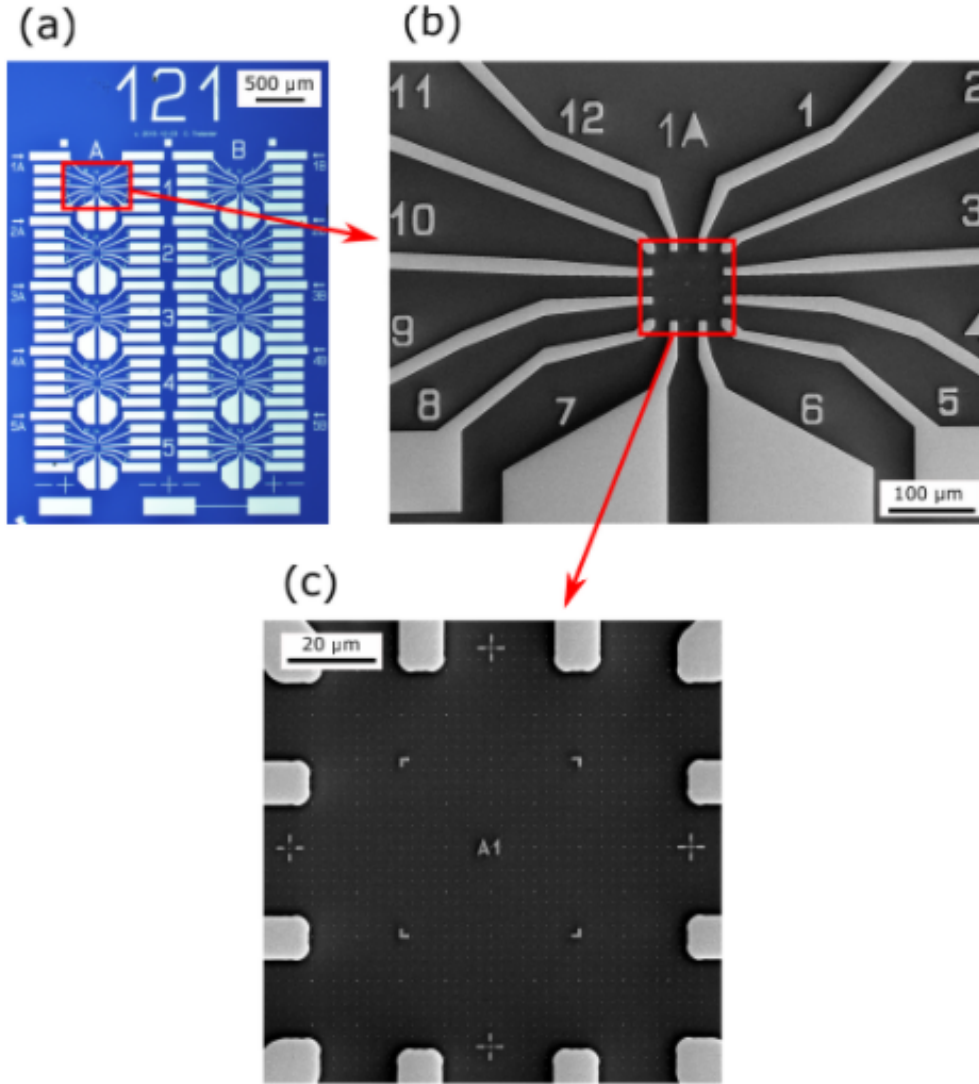
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Figure 12: SEM image of a) a 10 field chip, b) closeup of one field with pads, and c) more zoomed in image showing the grid. Image reprinted from [7].

The nanowire devices will then be fabricated on the fields of the substrate (fabrication process described below). The devices are designed such that one electrical contact in either end of the nanowires will be in direct contact with the nanowire. A top-heater architecture as suggested by Gluschke et. al. [29] will be used to apply a temperature along the nanowire. Requiring deposition of an oxide layer on top of the electrical contacts, and then placement of the metallic leads for heating directly above the nanowire and electrical contacts. An illustration of the device can be seen in figure 13, with a voltage source V_{SD} and a current preamplifier A indicated. A voltage source, electrically separated by the oxide layer from the nanowire, of $\Delta V_H = V_{H,R} - V_{H,R}$ is used for local heating. In the case presented in figure 13, the heater on the ramp side of the barrier is used, measurements will also be performed using

the heater on the abrupt side. Measurements will be performed in this source-drain configuration, and with the opposite configuration, that is, with V_{SD} and A switched places in figure 13.
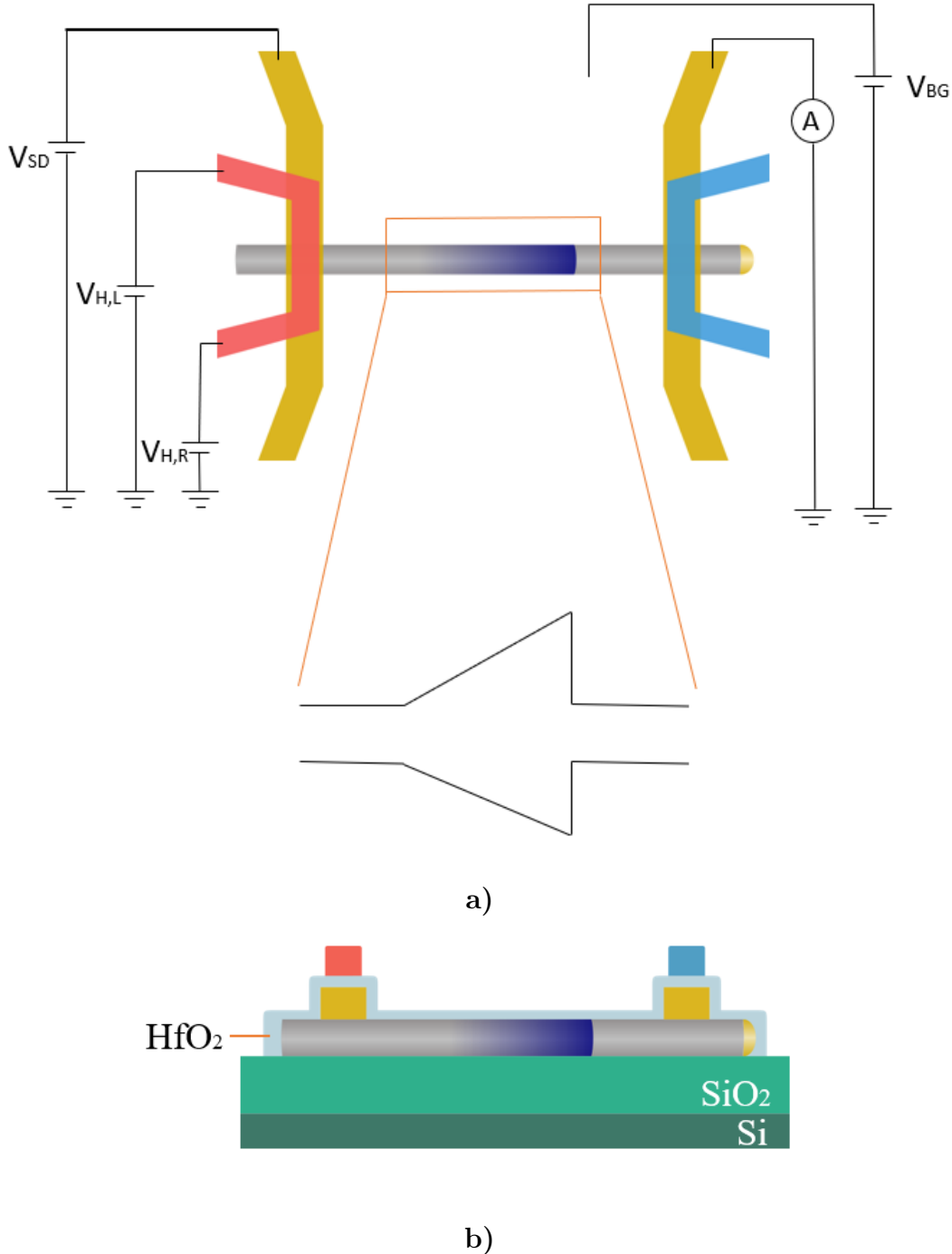

a)

b)

Figure 13: a) A schematic illustration of the device, with the band structure orientation indicated in relation to the gold seed and contacts. The nanowire can be seen illustrated in grey with the barrier in blue with the golden seed at the right end. The electrical contacts placed over the nanowire are indicated in yellow, and the heater contacts are indicated in red and blue. b) A side view of the nanowire device on top of the Si/SiO$_2$ substrate, with the insulating oxide layer (HfO$_2$) indicated.

There are two possible source-drain contact configurations. Either as illustrated in figure 13, with source on the ramp side of the barrier and drain on the abrupt side of the barrier, or with source on the abrupt side of the barrier and the drain on the ramp side of the barrier. The two cases are illustrated in figure 14. The bias on the drain side is 0 V, and alternated at the source side.
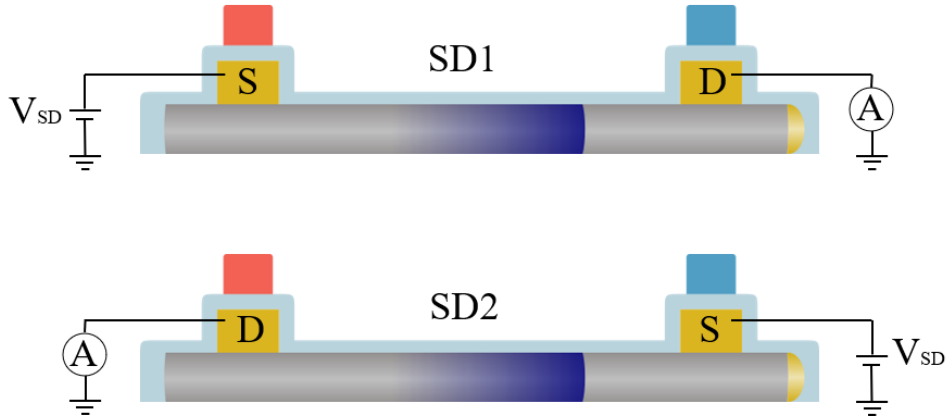

Figure 14: The side view of the device, illustrating the two source-drain contact configurations with the voltage source (V_{SD}) and current preamplifier (A) indicated. Top: source-drain contact configuration 1 (SD1) with the source contact closest to the ramp side of the barrier and the drain contact closest to the abrupt side of the barrier. Bottom: source-drain contact configuration 2 (SD2) with the drain contact closest to the ramp side of the barrier and the source contact closest to the abrupt side of the barrier.

3.3. Device fabrication

In this section a step-by-step account of the device fabrication is given. A schematic overview of the processing steps can be seen illustrated in figure 15. A description of the instruments involved will be given in Appendix B.
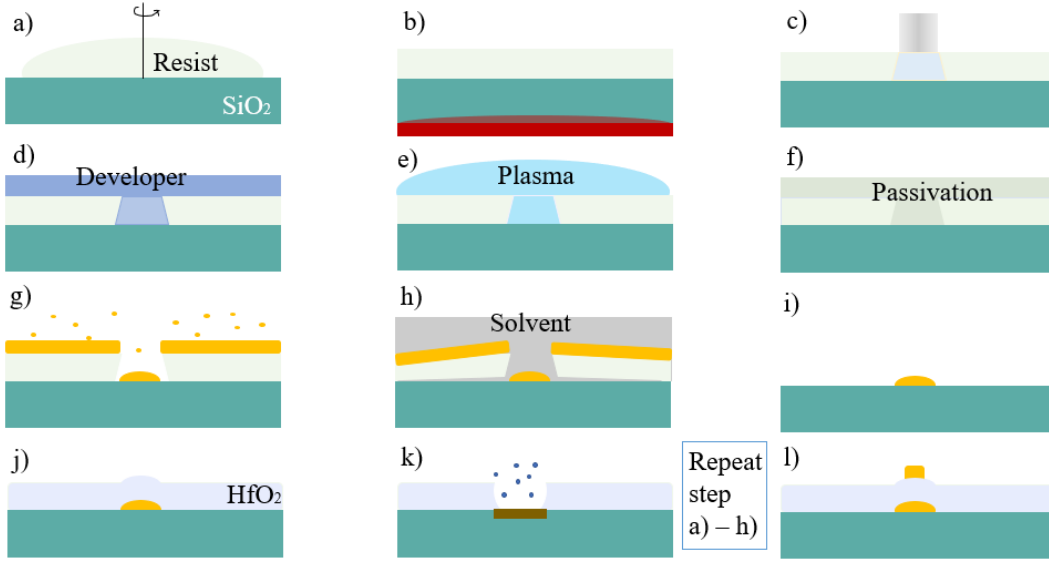
Figure 15: Schematic overview of the processing steps used for device fabrication a) spin coating of a resist onto the sample, b) to harden the resist and to evaporate solvents the sample was baked on a hotplate, followed by c) EBL exposure and d) development of the pattern exposed to the electron beam, and e) to remove residual resist the sample was plasma etched. f) to promote electrical contacting of the nanowire, the sample was passivated, followed by g) metal evaporation, and a subsequent h) lift-off, resulting in a i) first metal pattern on the sample. For the device design of this project heater contacts, electrically insulated from the other contacts were desired. To achieve this, j) an oxide (HfO$_2$) was deposited, followed by k) opening the oxide at the pads designed for heater contact using a FIB. For the deposition of the heater contacts step a)-h) was repeated, resulting in l) a complete transfer of device design.

STEP I, DEPOSITION The initialising step of the device fabrication was to deposit the NW on the fields on the measurement chip. Before-hand, the chip was cleaned by submerging it in Acetone and subsequently placed in an ultrasonic bath for five minutes, rinsed in IPA and blow-dried using N$_2$ gun. The nanowires could then be transferred from the growth substrate to the measurement chip by carefully touching the growth substrate with a pointy piece of clean room tissue followed by touching the measurement chip with the tissue. Some nanowires will break and stick on to the tissue when touching the growth substrate and then be deposited on the measurement chip and stick due to van der Waals forces when touching the chip. To control if nanowires were successfully deposited on every field, an optical microscope was used for visual inspection. The process of depositing nanowires was repeated until nanowires could be seen in every field.

STEP II, IMAGING AND DESIGN To identify suitable nanowires, that is nanowires of adequate length and with no contact with other nanowires, and find their exact location on the fields, all fields were imaged with a scanning electron mi-

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croscope (SEM) FEI Nova NanoLab 600 with an acceleration voltage V_{acc}=10 kV. For each field, the most suitable NW was chosen.

The micrographs obtained with the SEM was used to determine the nanowire location and orientation within the coordinate grid of its corresponding field and based on this the desired EBL-pattern was designed in RAITH150. The pattern of both the top heaters and the electrical contacts were created in the same file, but in different layers as the heaters and the electrical contacts will not be exposed at the same time.

STEP III, DEPOSITION OF RESIST The measurement chip was then spin coated with PMMA A5 resist, a positive resist, by fixing it to a spinner by vacuum and depositing resist onto the surface of the chip. A spinning speed 5000 rpm for 60 s was used, resulting in a resist thickness of roughly 300 nm. To harden the resist and evaporate solvents the chip was placed on a hot plate of 180 °C for five minutes directly after spinning. The back of the chip was scraped to remove possible residues.

STEP IV, EBL EXPOSURE An EBL Raith 150 system was used for the EBL exposure, with an acceleration voltage V_{Acc} of 20 kV and an aperture size of 10 μm. The sample was exposed to the first layer of the design file created in the EBL software, that is the electrical contacts.

STEP V, DEVELOPMENT OF THE RESIST To remove the exposed resist, the EBL exposure was followed by development of the sample, performed by submerging the chip in MIBK:IPA 1:3 for 40 s. Then followed by rinsing in IPA for 20 s and finally blow drying it with a nitrogen (N2) gun.

STEP VI, REMOVAL OF RESIDUAL RESIST Plasma etching were performed to remove residual resist not washed away during development and create an undercut in the exposed pattern.

STEP VII, PASSIVATION As oxide layers, which may inhibit electrical contact, quickly form on the surface of IIIV nanowires, the sample surface was chemically passivated just before metal deposition. The etching was performed in an 20 % ammonium sulphite (NH_4S_X) water bath of 40 °C for 2 min, followed by rinsing the sample in H_2O, and blow dried with a N2 gun.

STEP VIII, METAL EVAPORATION Next, the sample was moved to a low-pressure evaporator (AVAC) for material deposition of Ni/Au (0.250/0.750

kÅ). Au and Ni were placed in the assigned material boats and the system was then pumped. After the pumping of the system the deposition was initialised by turning on a current through the material boat of Ni, and gradually increasing it until the adequate evaporation rate of 1.8 Å/s was achieved. The shutter was then opened and was left open until the desired deposition thickness was achieved. The current was turned down and the aperture was turned to the Au material boat and the process was repeated for the Au, and Au was deposited with an evaporation rate of 7 Å/s.

STEP IX, LIFT-OFF After venting the system the sample was removed for lift-off, that is removing all resist still on the sample and accompanying metal, so that only exposed pattern is left. Lift-off is done by submerging the sample in acetone heated to 50°C for 15 minutes. The beaker with the sample was removed from the hotplate and a pipette was used to 'blow' acetone on the sample carefully not to blow any air on the sample, to remove both resist and metal. When most of the metal had been removed, the sample was moved to a beaker of room temperature acetone to be further rinsed. The sample were then put in a beaker of IPA to remove acetone. Finally, the sample was dried with a N_2 gun. This step completes the first layer.

STEP X, OXIDE DEPOSITION Before deposition of metal for the top heaters an 80 layer of hafnium dioxide (HfO_2) was deposited on the sample to ensure electrical isolation between the different contacts. This was done by atomic layer deposition (ALD) in an ALD Savannah-100 for 80 cycles at 100°C.

STEP XI, OPENING THE OXIDE The ALD were followed by opening the HfO_2 layer on the pads designated for the heater contacts using a focused ion beam (FIB). In this project a focused ion beam FEI Nova NanoLab 600 was used for removing the oxide layer. A square pattern was designed and aligned with the pads and these regions were then exposed to the FIB.

REPEAT STEP II-IX After this, the process from the resist deposition was repeated, see section III-IV for details. The spin coating was performed as in step III. The EBL was once again performed in an EBL Raith 150 system but now for the level including the heaters using a V_{acc} of 30 kV to increase the resolution, followed by the same development procedure. The material evaporation was performed in a AVAC evaporator with deposition of Ni/Au (0.250/0.750 kÅ) with evaporation rates of 2.2-6 Å/s and 3 Å/s for Ni and Au respectively. The evaporation was followed by lift-off performed as in STEP IX.

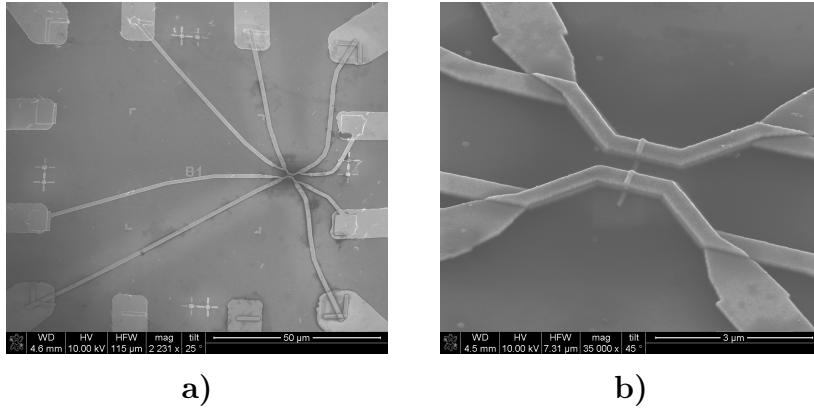In figure 16 a SEM image of the completed device can be seen.

Figure 16: SEM images of a) a field with one device, and b) zoomed in tilted view of the nanowire with the electrical and heater contacts.

3.4. Electrically connecting the measurement chip

For electrical measurements to be possible the measurement chip was mounted onto a ceramic carrier and glued onto it with a conductive silver paste. The carrier had 14 small gold coated pads that are connected to 14 pins, and one larger pad to mount the sample on. The devices could then be connected to the carrier by bonding of gold or aluminium wires from the gold pads on the carrier to the gold pads on the measurement chip with a FS Bonder. Two of the smaller gold pads on the carrier were bonded to the back of the measurement chip (the n-type Si), to be used as overall gating. The 12 remaining pads could be used to connect to the devices, and as each device requires six contacts (two for each heater, one for source and one for drain) two devices could be connected at the same time.

3.5. Characterisation

Measurements were performed in three different temperature environments: room temperature (ca 300 K), liquid nitrogen (77 K) and in a Triton dilution fridge (sub 1K). A description of the measurements in the different environments as well as a short description of how the relevant biasing was applied is given below as well as a theoretical model used to describe the system.

3.5.1. Applying bias

Three different types of biases were applied to the devices: source-drain bias, heating bias, and back gate, described below.

SOURCE - DRAIN BIAS: The bias over the nanowire was applied to one of the ends of one of the electrical contacts, and the amplifier, connected to the

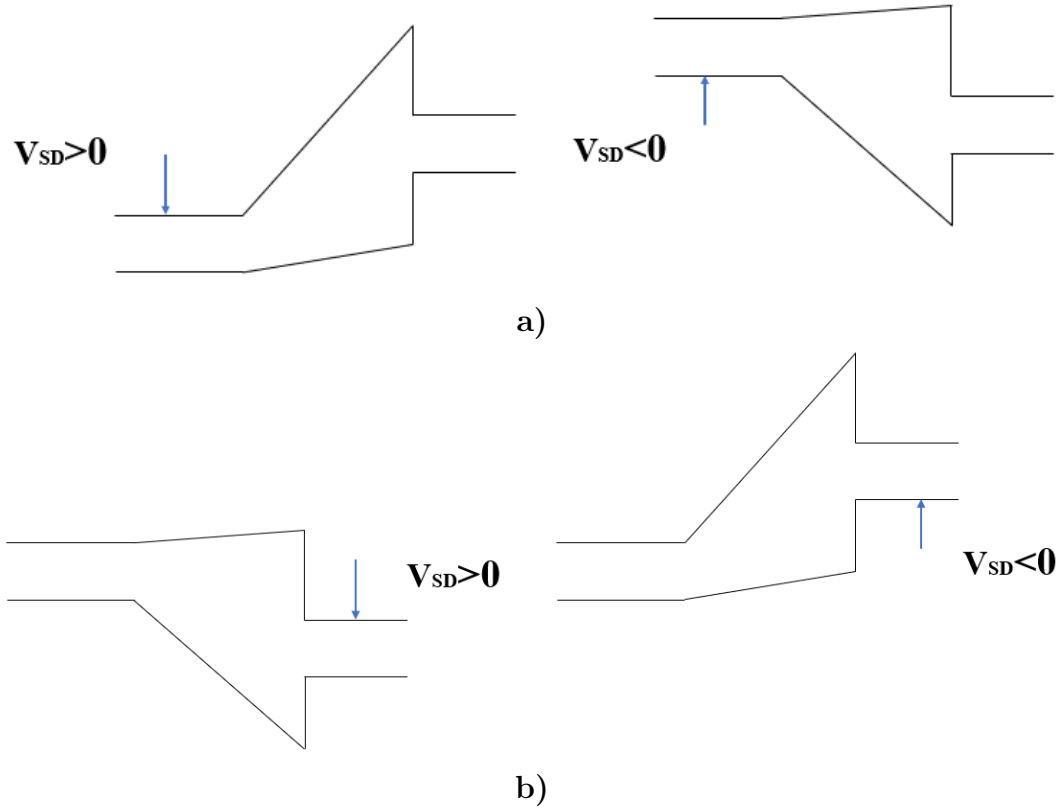read out, was connected to one of the ends of the other electrical contact. Noted as V_{SD}.

Figure 17: Schematic illustration of applying positive (left) and negative (right) V_{SD} on a) the ramp side of the barrier and b) the abrupt side of the barrier.

HEATING BIAS: Heating bias was applied symmetrically over the heater to avoid gating effects, this mean applying $-\frac{1}{2}V_H$ to one end of a heater and $\frac{1}{2}V_H$ to the other end of the same heater. The total heating bias is then referred to as ΔV_H. As there are two heaters, one on either side of the barrier, they will be referred to as V_{HR}, for applying a heating bias on the ramp side, and V_{HA} for applying a heating bias on the abrupt side of the barrier.
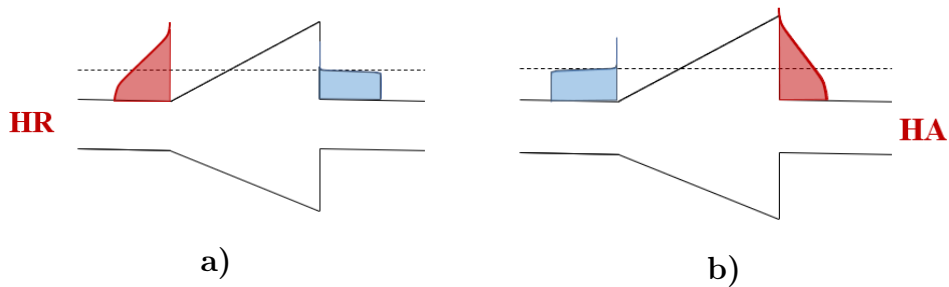

Figure 18: Schematic illustration of applying V_H resulting in a temperature difference on a) the ramp side of the barrier (HR) and b) the abrupt side of the barrier (HA).

BACK GATE: Applying a back-gate voltage, applying a voltage to the silicon substrate, can adjust the Fermi level position and hence also the carrier concentration [16]. Applying a positive back gate bias will cause the Fermi level to rise. Noted as V_{BG}.
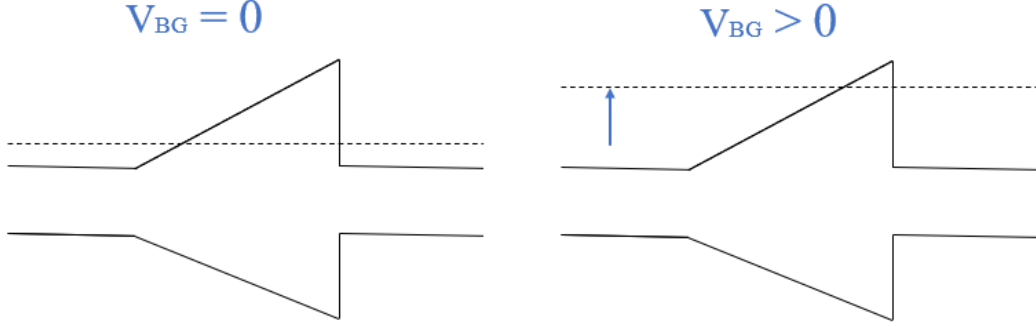

Figure 19: Schematic illustration of the band structure with no applied biases (left) and an applied V_{BG}>0 V causing a rise of the Fermi level (right).

3.5.2. Characterisation techniques

Three main types of measurements were performed to identify behaviour of the nanowire devices.

IV-CURVES To electrically characterize the nanowire devices current-voltage, IV, measurements were performed to establish asymmetric current response due to the asymmetry of the barrier.

IV-CURVES UNDER HEATING The primary approach to try to identify asymmetries between heating on the two sides of this project was to perform current-voltage, IV, measurements with heating on either side of the barrier and compare features of the IV-curves. The key features that will be considered will be the current resulting from thermal biasing, the thermocurrent, and the thermovoltage resulting from thermal biasing. The thermocurrent will primarily be evaluated at short-circuit conditions, where the voltage across the nanowire is zero, and this quantity will be referred to the short circuit current I_{SC}. The thermovoltage will be evaluated at open-circuit conditions, where the current is zero, and will be referred to as the open circuit voltage V_{OC}.

STABILITY DIAGRAMS Measurements where both the bias over the nanowire V_{SD} and the gating bias V_{BG} under different heating biases were also performed, to be plotted as stability diagrams, with the intention to detect quantum dot behaviour as well as thermal effects.

3.5.3. Measurement setup in room temperature

For the measurements in room temperature, the sample was mounted on a holder in a vacuum chamber.

To apply voltage to the back gate and heaters a Stanford Research System SR830 Locked-in Amplifier and a Keithley 2636B System SourceMeter was used, and to apply source-drain bias voltage over the nanowire a Yokogawa GS200 Voltage Current Source. To detect the current through the nanowire a Hewlett Packard 3401A Multimeter was used together with a Stanford Research System SR570 Low-Noise Current Preamplifier.

3.5.4. Measurement setup in liquid nitrogen

For the measurements in liquid nitrogen the sample was mounted on a dipstick, which subsequently was attached to a liquid nitrogen dewar.

Most of the measurements were preformed using a Yokogawa GS200 Voltage Current Source for the source and drain bias and the back gate, for the heaters Yokogawa GS200 Voltage Current Sources or a Stanford Research System SR830 Locked-in Amplifier was used. The current signal through the nanowire was amplified using a Femto200 amplifier and then read on a Hewlett Packard 3401A Multimeter.

For some measurements a Keithley 2636B System SourceMeter was used as a voltage source for back gate or source-drain bias, and a Stanford Research System SR570 Low-Noise Current Preamplifier was used for signal amplification.

During the project, I did also participate in building a new dipstick and setting up a measurement station. Due to the thin rod of the dipstick, it was suspected that it easily caught vibrations that lead to noise, leading to the decision to use a well-tried dipstick.

3.5.5. Measurement setup in Triton Dilution Fridge

A Triton Dilution Fridge was used for performing measurements at sub 1K temperatures. To apply back gate, source-drain biasing and heating voltage Yokogawa GS200 Voltage Current Source voltage sources were used, and the current signal through the nanowire was amplified using a Femto200 amplifier and then read on a Hewlett Packard 3401A Multimeter. The principles of a dilution fridge are given in appendix C.

3.6. Modelling the system

A one-dimentional transport model across a triangular barrier was provided by Peter Samuelsson. The model considers an effectively one-dimensional scattering potential connected to source and drain contacts, illustrated in figure 20, and only the conduction band with electrons as charge carriers was considered. The model simulates the case when applying an electrical bias to the ramp side of the barrier and includes tunnelling through the barrier and thermionic emission over the barrier. The model also allows for an optional temperature increase on either side of the barrier, simulating heating on one side.
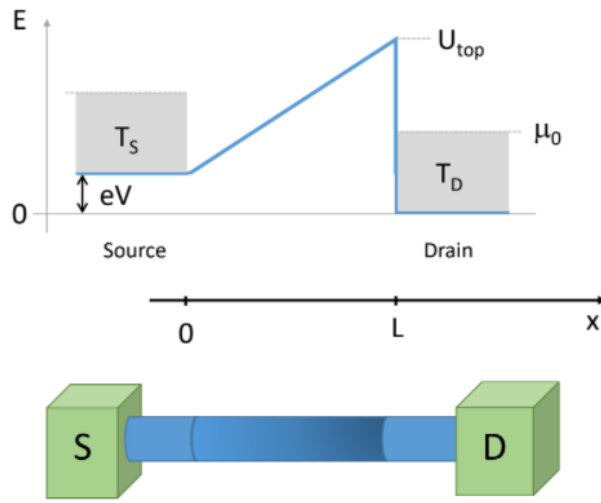
Figure 20: Top: Sketch of the triangular barrier system, with the source (S) and drain (D) indicated. An x-axis is introduced, with the temperatures on each side of the barrier indicated and with the barrier extending from x = 0 to x = L. Bottom: Schematic of the nanowire with contacts. Illustrated by Peter Samuelsson.

The current through the barrier is given by

$$I = \int (f_A(E, T_A) - f_R(E, T_R)) T(E, V) dE \qquad (15)$$

where the Fermi distribution functions of the ramp side and the abrupt side of the barrier are given by

$$f_R(E, T_R) = \frac{1}{1 + e^{(E - \mu_R)/kT_R}}, f_A(E, T_A) = \frac{1}{1 + e^{(E - \mu_A)/kT_A}} \qquad (16)$$

with the corresponding temperatures and chemical potentials

$$T_R = T_0 + \Delta_R, T_A = T_0 + \Delta_A, \mu_R = \mu_0 + eV, \mu_A = \mu_0. \qquad (17)$$

That is, T_0 is the ambient temperature and ΔT_R and ΔT_A are non-zero if the respective contact is heated and zero otherwise. The source is on the ramp

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side of the barrier and kept at an electrical potential $-V$ and the chemical potential is μ_0.

The transmission function of the triangular barrier is approximated by the WKB theory,

$$T(E,V) = C exp\left(-\int_{x_0}^{L} \sqrt{\frac{2m}{\hbar^2}(U(x,V)-E)}dx \right) \qquad (18)$$

where C is a real, positive constant of dimension conductance over charge. Here $U(x,V)$ is the electrical potential of the triangular barrier

$$U(x,V) = (U_{top} - eV)\frac{x}{L} + eV, 0 < x < L, eV < U_{top} \qquad (19)$$

such that $U(0,V) = eV$ and $U(L,V) = U_{top}$. That is, the applied source potential changes the slope of the triangular barrier, with the top potential U_{top} staying constant. From $U(x,V)$ we get the classical turning point x_0 is found from

$$U(x_0,V) = E \longrightarrow x_0 = L\frac{E - eV}{U_{top} - eV} \qquad (20)$$

This gives the transmission function

$$T(E,V) = C exp\left(-\frac{2L}{3}\sqrt{\frac{2m}{\hbar^2}}\frac{(U_{top}-E)^{3/2})}{U_{top} - eV} \right), E < U_{top} \qquad (21)$$

Additionally, for thermionic emission, that is energies larger than the barrier height $E > U_{top}$, the transmission probability is unity, giving the transmission function $T(E > U_{top}, V) = C$.

4. Measurement, Results and Analysis

Here the result of the measurements is presented along with analysis of the observations. The measurements and the results will be given in sections, with indicated ambient temperature. After the measurement and result, an analysis will be given. Measurements of four devices will be presented, indicated as device A, B, C, and D. The devices were fabricated on the same chip at the same time, with nanowires from the same growth substrate and device design as seen in figure 13.

4.1. 77 K and 300 K Measurements
4.1.1. 77 K and 300 K: The IV-curve
The current, I, measured when applying a source-drain bias V_{SD} over the nanowire, referred to as IV-curves, can be seen in figure 21 a) and b) for

device A, in ambient temperatures of 300 K and 77 K, with a range V_{SD}=-0.3 - 0.6 V. The source-drain contact configuration SD1, top in figure 14, that is source at the ramp side of the barrier and drain at the abrupt side of the barrier.
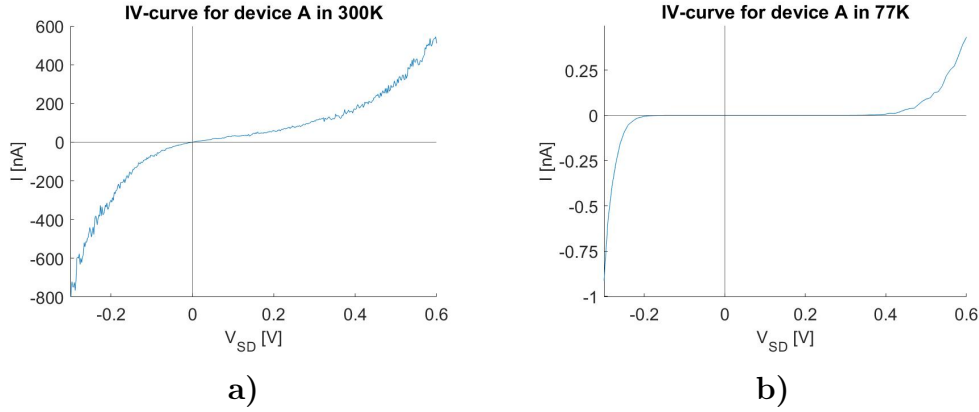

Figure 21: *IV*-curves for device A in ambient temperatures of a) 300 K and b) 77 K.

IV-curves of device B can be seen in figure 22 a) and b), performed in ambient temperatures of 300 K and 77 K respectively, with a range of V_{SD}=-0.4 - 0.4 V and V_{SD}=-0.65 - 0.9 V.
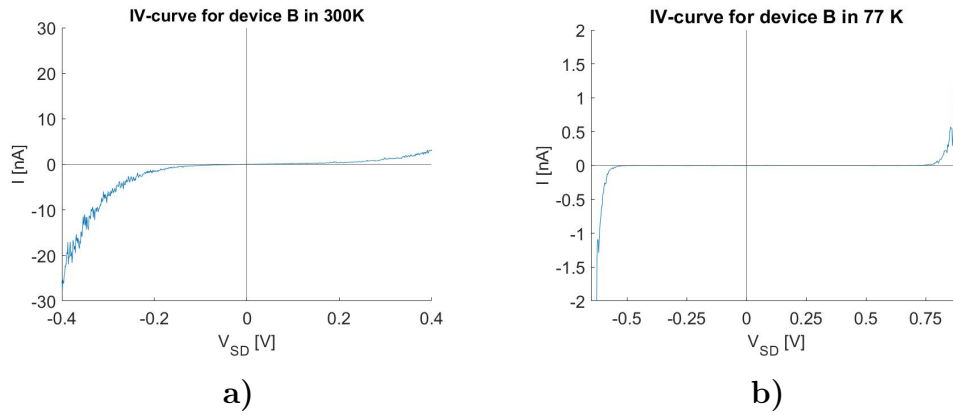

Figure 22: *IV*-curves for device B in ambient temperatures of a) 300 K and b) 77 K. Note the different ranges in V_{SD}.

Analysis

An asymmetry in onset when applying negative and positive bias V_{SD} over the nanowire for both devices, see figure 21 and 22. The different onset for positive and negative V_{SD} indicate that the transport of electrons depends on the direction of the flow and hence what side of the barrier the electrons must pass by. In this case, it can be deduced that in the negative current direction the electrons pass the ramp side of the barrier and in the positive current the electrons must pass by the sharp side of the barrier. Applying a sufficient

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negative bias to the ramp side of the barrier will result in effectively no barrier for the electrons, and they can easily pass from left to right, resulting in a large injection, see figure 23 a). Applying positive bias to the ramp side will make the barrier effectively narrower but it will remain. Electrons can pass over the barrier by thermionic emission or possibly by tunnelling through the barrier as the applied bias will alter the effective barrier width making it narrower (in this work it is not possible to determine the fraction of the current that is generated through tunnelling and thermionic emission respectively), see figure 23 b) for an illustration of the possible transport mechanisms. This result is in line with the results and reasoning of the study on electrical properties of InAs nanowires with a step-like graded, triangular, barrier conducted by Nylund et. al. [12].
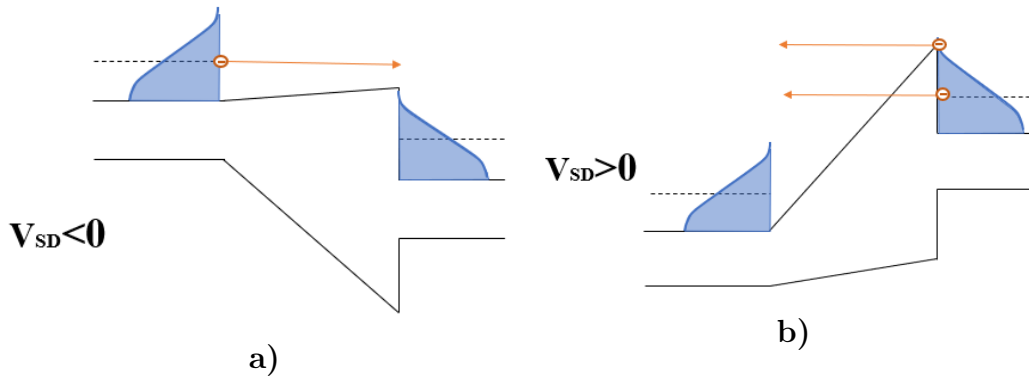

Figure 23: a) Applying a sufficient negative bias to the ramp side of the barrier will result in effectively no barrier for the electrons, and they can easily pass from left to right, and b) applying positive bias to the ramp side will make the barrier effectively narrower, but will remain. Electrons can pass over the barrier by thermionic emission and possibly by tunnelling through the barrier when the effective width of the barrier is reduced due to the applied bias.

If comparing the IV-curves at an ambient temperature of 300 K, see figure 21 a), and in 77 K, see figure 21 b), the current onset can be seen to be much sharper in liquid nitrogen than in room temperature. This can be explained by the shape of the Fermi distribution function at different temperatures. At high temperatures, here about 300 K, the Fermi distribution function is spread out, and electrons have a probability to occupy states at a relatively large range of energies. For lower temperatures, here about 77 K, the Fermi distribution function will be much more compressed and the range of probable energies for electrons to occupy is narrower, and the electrons will have more similar energies. For the higher temperature electrons at states of higher energies will have the possibility to pass over the barrier at lower biases than at low temperatures, even if the Fermi levels would be the same, see figure 4 for the shape of the Fermi Dirac distributions at 77 K and 300 K.

It is seen that the current is several orders of magnitude larger at an ambient temperature of 300 K than at an ambient temperature of 77 K at the same bias. This can also be explained by the spreading of the Fermi function. At an ambient temperature of 300 K, an electron is more likely to occupy a state close to the barrier edge, which can contribute to current with only a small V_{SD} applied. In addition, more donors could be ionized at an ambient temperature of 300 K than at an ambient temperature of 77 K, resulting in more charge carriers available for current contribution.

Performing measurements at an ambient temperature of 77 K results in a higher temperature gradient and less thermal noise than in higher temperatures, but it also results in smaller currents due to that electrons are less likely to occupy high energy state and hence to cross the barrier and contribute to current. This motivates measurements in different ambient temperatures and the usage of global gating in lower temperatures.

4.1.2. 77 K: IV-curves under heating

IV measurements were performed at an ambient temperature of 77 K on device B with different heating biases applied on the different sides of the barrier, with a source-drain voltage range of V_{SD}=-20 mV - 20 mV and a heating voltage range of ΔV_H=0 - 0.8 V, with the source-drain contact configuration SD1. Thermal biasing alone was not sufficient to generate a current at low, therefor a V_{BG} was applied to raise the chemical potential and increase the conductivity. Selected IV-curves at a V_{BG}=10.35 V are plotted in figure 24, with applying a heating bias on the abrupt side of the barrier (V_{HA}) indicated in a green scale and applying a heating bias on the ramp side of the barrier (V_{HR}) indicated in an orange scale. Each line is an average of six sweeps to suppress noise and fluctuations.
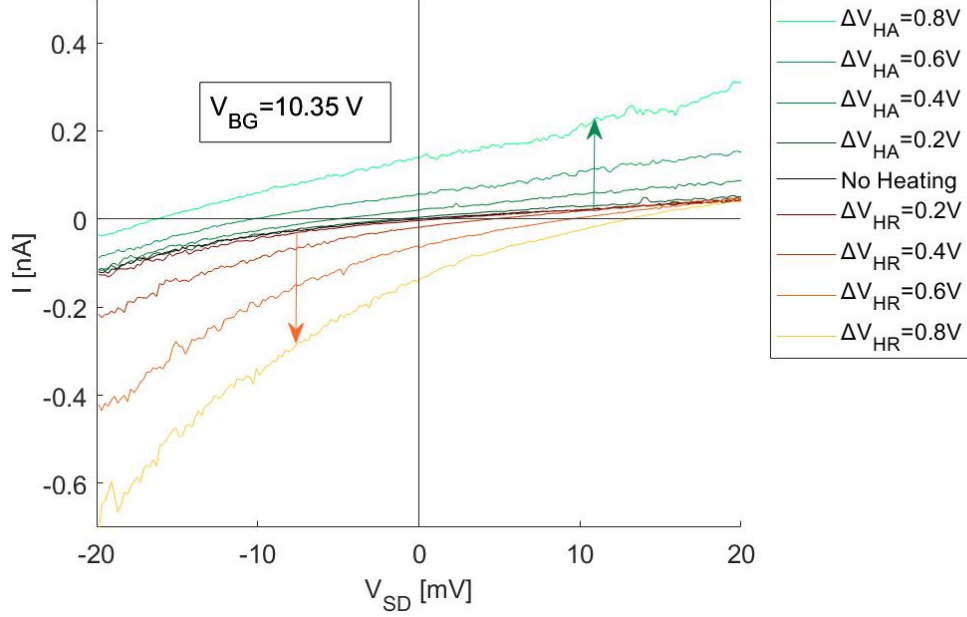
Figure 24: *IV*-curves at V_{BG}=10.35V, with heating on either side of the barrier. Heating on the abrupt side of the barrier is indicated in a green colour scale, with the green arrow indicating higher V_{HA}, and heating on the ramp side of the barrier is indicated in an orange colour scale, with the orange arrow indicating higher V_{HR}.

Analysis

At the given conditions, it can be seen that heating on either side of the barrier have an influence on the appearance of the *IV*-curves at an ambient temperature of 77 K, see figure 24. Applying a heating bias on the ramp side of the barrier will contribute to a negative current and applying a heating bias to the abrupt side of the barrier will contribute to a positive current. When heating on the ramp side of the barrier some electrons could gain enough energy to diffuse over the barrier, in line with the change in shape of the Fermi distribution, but electrons on the cold side will not exhibit the gain in energy to the same extent. A net flow of electrons can therefore be seen from the ramp side to the abrupt side of the barrier. With source on the ramp side of the barrier and drain on the abrupt side of the barrier, this will result in a negative current. Figure 25 a) illustrate transport over the barrier enabled by heating on the ramp side of the barrier at short circuit conditions (V_{SD}=0 V). Similar reasoning can be conducted for heating on the abrupt side, where the heating result in transport over the barrier from right to left in figure 25 b), resulting in a positive current.
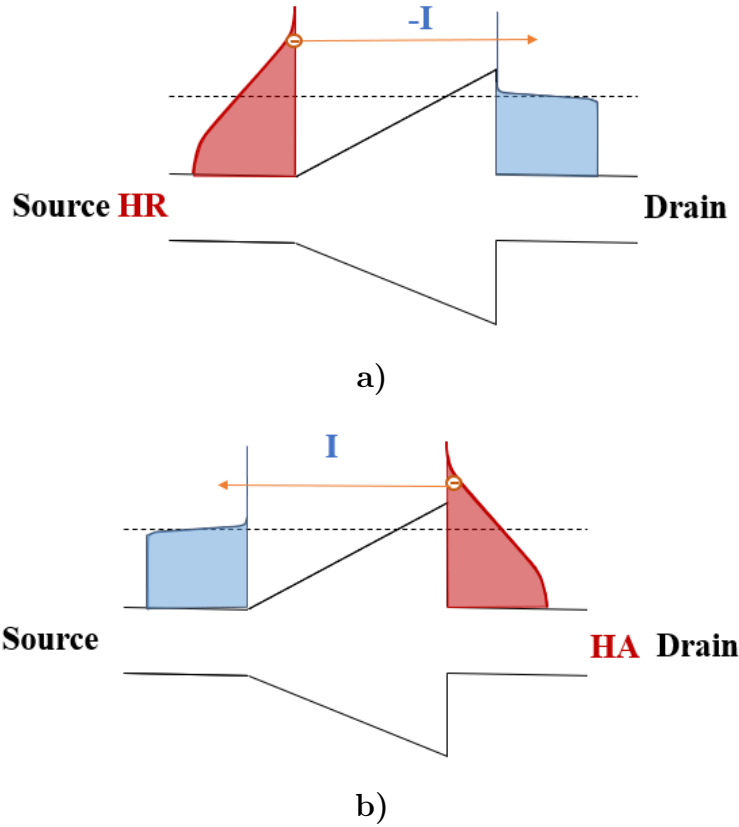
Figure 25: Illustrations of the short circuit current for heating on a) the ramps side (HR), and b) the abrupt side (HA) of the barrier.

To be able to evaluate the effect of the barrier on thermionic extraction from heating on either side, and to identify asymmetries from heating, it is necessary to know whether the heaters apply the same temperature gradient across the barrier. The heating power, the required power to provide a temperature gradient, is dependent on the resistance of the heater [29]. This could cause geometrical differences between the heaters to result in differences between their resistances and hence heating properties. As the heating create a temperature gradient along the nanowire, the temperature at the barrier can differ also dependent on the distance between the heaters and the barrier. To evaluate the heating properties, the short circuit current can be considered. At short circuit conditions the barrier does not exhibit any deformations (that arises from for example applying electrical biasing), and electrons approaching from either side of the barrier should have the same probability of being transmitted. Applying a thermal bias on either side should hence result in the same (absolute) thermocurrent if the heaters heat symmetrically.

As the shape changes with different biasing cases, as seen in figure 18, the transmission functions are no longer necessarily the same for different applied

biases V_{SD}. Evaluating features of the IV-curves at other points than at short-circuit conditions could therefore provide indications of an asymmetric behaviour under electrical bias. The IV-curves can for example be evaluated at the voltage where the current is zero, at the open circuit voltage V_{OC}, when heating on either side of the barrier. Non-linear behaviour of V_{OC}, that is, different V_{OC} when heating on either side of the barrier, could indicate asymmetric thermoelectric behaviour.

4.1.3. 77 K: The short circuit current and open circuit voltage

The short circuit current, I_{SC}, where V_{SD} across the nanowire is zero, can be extracted from the IV measurements for different heating voltages for each side, presented as absolute values in figure 26. The error bars represent the standard deviation of the six sweeps.
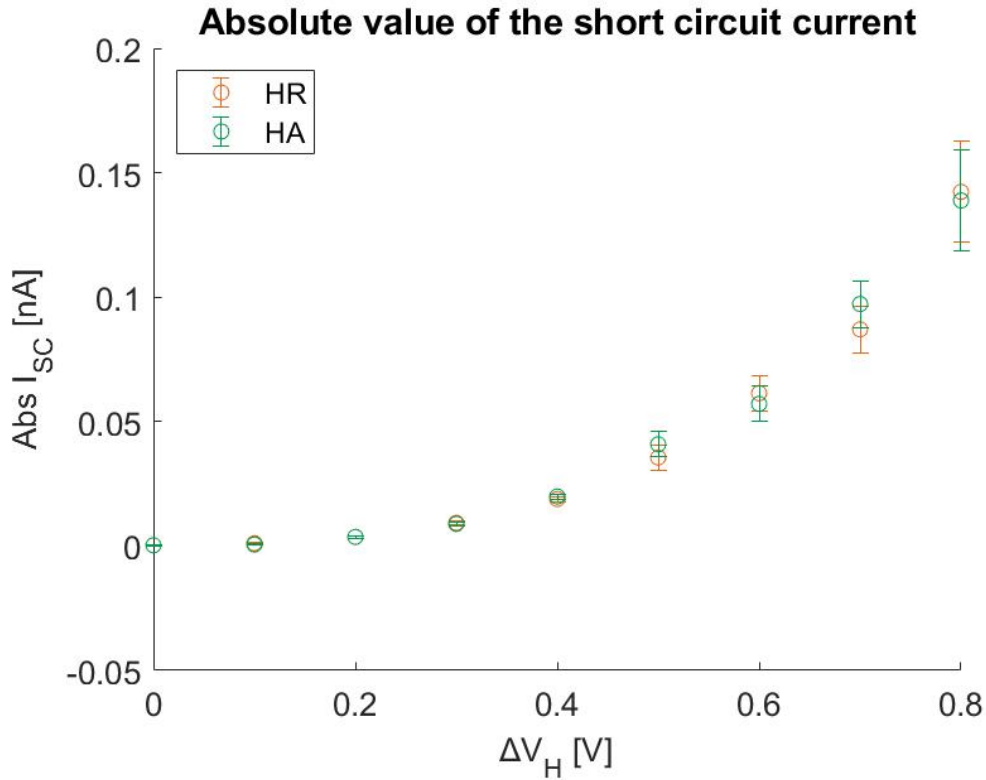

Figure 26: The short circuit current, I_{SC}, plotted against heating bias ΔV_H with error bars represent the standard deviation of the six sweeps.

Similarly, the open circuit voltage, V_{OC}, can be extracted from the same data form where the current is zero, and can be seen presented as absolute values in figure 27.
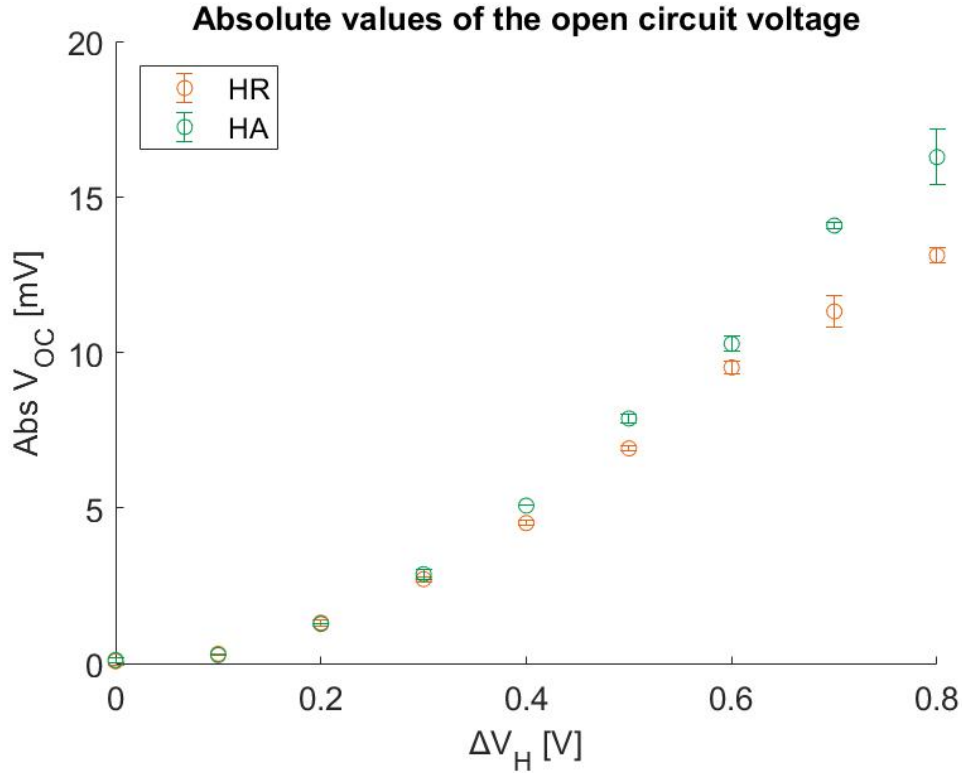
Figure 27: The open circuit voltage, V_{OC}, plotted against heating bias with error bars represent the standard deviation of the six sweeps.

Analysis

The absolute value of I_{SC} obtained from heating on either side of the barrier, seen in figure 26, overlaps greatly for most of the heating biases. With the reasoning in the analysis section of 4.1.2, this imply that the heaters appear to apply the same temperature gradient no matter which side is heated.

In figure 27 non-linear V_{OC} response can be seen, with higher V_{OC} when heating on the abrupt side of the barrier for higher heating biases. The transport mechanisms at work at the V_{OC} for heating on the different sides can be analysed to gain insight to the underlying reasons to the difference in V_{OC}.

The V_{OC} is the required applied voltage to achieve net zero current through the device, in other words to counter the flow of electrons from the heated side to cold side. In the case of heating on the ramp side of the barrier, the counter flow of electrons from the cold side will travel across the barrier from the abrupt side, and the possible transport mechanisms could be thermionic emission over the barrier or tunnelling through the barrier. Heating on the ramp side of the barrier can be seen to result in a positive V_{OC}, see figure 24. When applying a positive V_{SD} on the ramp side of the barrier, the bar-

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rier width will effectively be reduced. This reduction could enable tunnelling through the barrier. See figure 28 for a schematic illustration of the band structure and possible electron transport across the barrier.
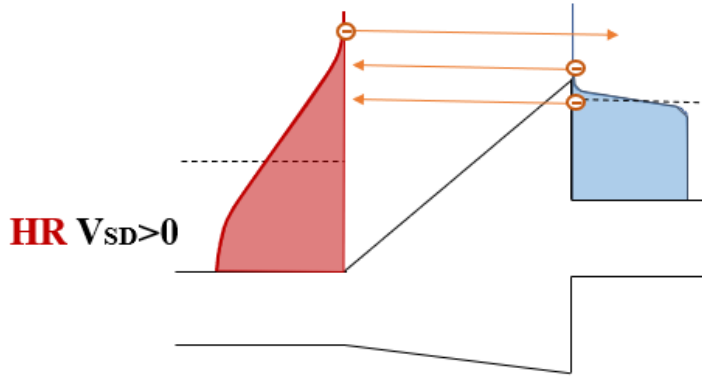

Figure 28: Possible transport mechanisms across the barrier at conditions of $I=0$ A when heating on the ramp side of the barrier.

For heating on the abrupt side, the counter flow of electrons will instead be crossing the barrier from the ramp side. Stimulating a flow from the ramp side of the barrier require a negative bias applied to this side, and the open circuit voltage can indeed be seen to be negative in figure 24. The barrier will for become effectively wider, possibly suppressing tunnelling. The transport mechanism for back flow will instead be passing over the barrier. In figure 29 the band structure with the back flow of electrons can be seen illustrated to pass over the barrier when applying a temperature gradient on the abrupt side of the barrier.
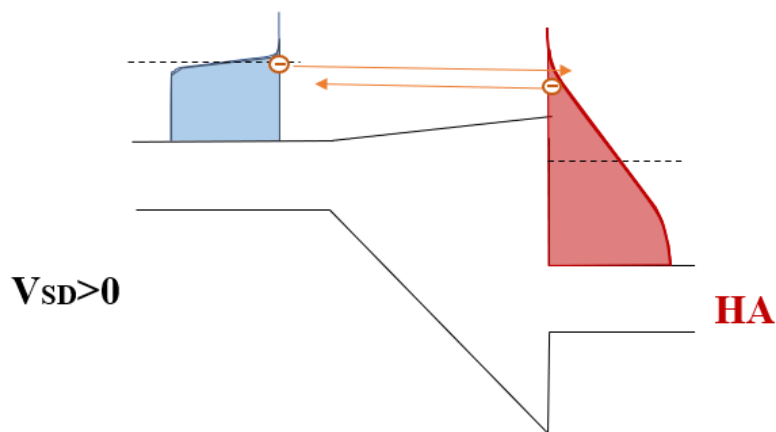

Figure 29: Illustrations of possible transport mechanisms at conditions $I=0$ A of transport over the barrier when heating on the abrupt side of the barrier.

In this measurement, V_{OC} for heating on the abrupt side is higher than the

V_{OC} for heating on the ramp side of the barrier. On a conceptual level, this observation matches that the flow of electrons from the abrupt side of the barrier will counter the flow of electrons emerging when heating on the ramp side at lower (absolute) V_{SD} than the flow of electrons from the ramp side will counter the flow of electrons emerging from heating at the abrupt side of the barrier.

Tunnelling probability through the barrier will depend on the barrier thickness. For lower values of V_{BG} the barrier segment at the Fermi level will be thicker, see figure 19, and could require higher V_{SD} to make the effective barrier width sufficiently thin for the tunnelling to match the electron flow from the ramp side of the barrier. With this reasoning, V_{OC}, and possibly also the relation between the V_{OC} from heating on the two sides of the barrier, could have a dependency on V_{BG}.

The same measurements were conducted for the other source-drain contact configuration SD2, and the results seem to qualitatively agree. This could indicate that the general behaviour seen in these measurements is not considerably dependent on the contact configuration. The data and a corresponding analysis are given in appendix D.

4.1.4. 300 K: IV-curves under heating

IV-curve measurements under heating were also performed at an ambient temperature of 300 K. The conductivity of the device is much higher at an ambient temperature of 300 K, as seen in section 3.1.1, and an applied V_{BG} was not required to see current contribution from heating at low V_{SD}. The IV-curve measurements under heating at V_{BG}=0V, with an applied heating bias of ΔV_H=0 - 1.4V at a V_{SD} range of V_{SD}=-0.6 - 0.6V, can be seen in figure 30
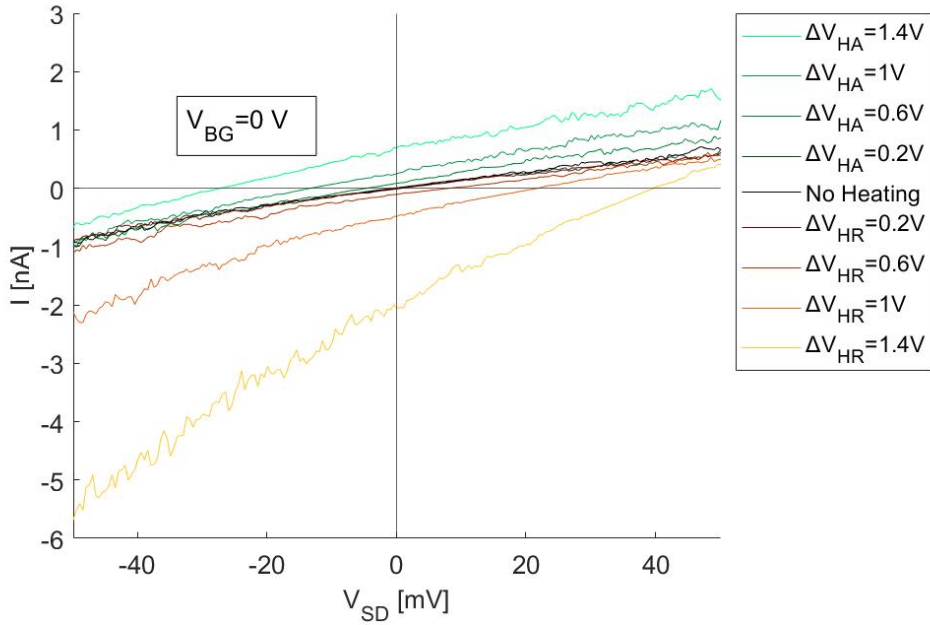
Figure 30: IV-curves at V_{BG}=0V at an ambient temperature of 300 K, with heating on either side of the barrier. Heating on the abrupt side of the barrier is indicated in a green scale and heating on the ramp side of the barrier is indicated in an orange scale. Each line is an average of six sweeps.

The extracted short circuit current and open circuit voltage for the different heating voltages on each side of the barrier can be seen in figure 31 a) and b) respectively.
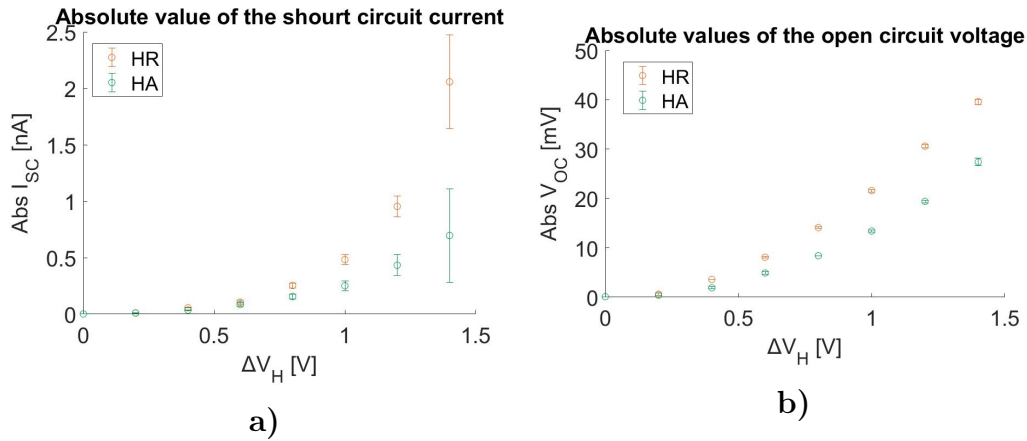

Figure 31: Extracted absolute values of the a) short circuit current and b) the open circuit voltage at an ambient temperature of 300 K with V_{BG}=0V, form heating on either side of the barrier with error bars represent the standard deviation of the six sweeps.

Analysis

The IV-curves under heating in room temperature have the same general appearance as the same measurements in liquid nitrogen. That is, a negative I_{SC}

and a positive V_{OC} when heating on the ramp side of the barrier, and a positive I_{SC} and a negative V_{OC} when heating on the abrupt side of the barrier, see figure 30.

However, the I_{SC} from heating on the two different sides are not overlapping to the same extent as in liquid nitrogen see figure 31 a). This could be due to a change of resistive properties of the heaters in different temperatures. The resistance of a metal increase with temperature [31], differences in resistance between the heaters that were not visible in liquid nitrogen could be enhanced in room temperature. As the joule heating is dependent on the resistive medium, the heat transferred to the nanowire could be affected. In this case, heating on the ramp side of the barrier seem to result in higher currents compared to heating on the abrupt side of the barrier, which could, with this reasoning, be due to higher heat dissipation from the heater on that side. This means that applying the same heating bias to the two heaters won't result in the same temperature along the nanowire, and the effects of applying the same heating bias on the two sides are no longer comparable, at least not in a straight-forward way.

The V_{OC} of the measurement at V_{BG}=0V can be seen to be higher for heating on the ramp side than on the abrupt side, see figure 31 b), opposite to what was found for IV measurements with applied heating bias in liquid nitrogen with back gate V_{BG}=10.35V. As the heating power for the two heaters seem to differ at room temperature, it is not possible to say with confidence whether this is due to the shape of the barrier, and not a difference in applied temperature gradient. If this is due to the barriers ability to extract electrons, this does not contradict the reasoning of dominating mechanisms of reverse transport, as discussed above. This could then be explained by being in the regime where the dominating back flow is over the barrier from the ramp side, compared to tunnelling through the barrier or passing over the barrier from the abrupt side.

4.1.5. 300 K: V_{BG} dependence of V_{OC}

To examine the V_{BG} dependence of V_{OC}, i.e. how V_{OC} depend on the position of the chemical potential, the V_{OC} was extracted from IV-curves at a heating bias of ΔV_H=0.8V for the range of V_{BG} values, see figure 32 a). These measurements exhibited fluctuations in conductance, and possibly an offset changing with V_{BG}. The offset was approximated to change linearly with back gate, based on the values of the offset at V_{BG}=0V and V_{BG}=10.35V. The difference between the V_{OC} obtained from heating on each side of the barrier ΔV_{OC}= $|V_{OC}(HR)| - |V_{OC}(HA)|$ as a function of V_{BG} can be seen in figure 32 b).
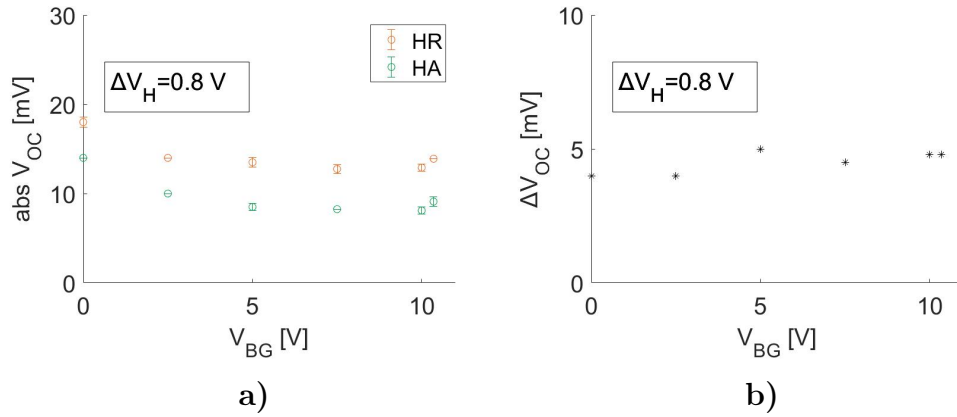
Figure 32: a) The absolute values of the open circuit voltage for different back gate values for a heating bias of ΔV_H=0.8V on either side of the barrier with error bars represent the standard deviation of the six sweeps, and b) the difference in open circuit voltage between heating on the two sides ΔV_{OC}.

Analysis

With the change in conductivity as well as the uncertainty in heating symmetry, the values of the V_{OC} for several different back gate values at ΔV_H=0.8 V seen in figure 32 a), can not with certainty be assigned a result of the barrier shape. But if the difference between the open circuit voltage at each back gate is considered, no tendency for a change in heating on which side generating the highest V_{OC}. This could indicate that the relation between V_{OC} from heating on either side of the barrier has a temperature dependence.

4.1.6. Modelling the current

The theoretical model of the current presented in section 3.6 is used to predict the *IV* characteristics for similar conditions as the experimentally obtained results in section 4.1.3. That is, *IV*-curves with heating bias at an ambient temperature of 77 K with a V_{BG}=10.35 V. In the model, the barrier length is set to 150 nm, the ambient temperature set to 77 K, the barrier peak at 540 meV above the conduction band edge and the chemical potential to 535 meV above the conduction band edge, unless nothing else is specified. The actual position of the chemical potential in this case is not known, but as a current can be seen even for very small applied V_{SD}, the chemical potential will be assumed to be close to the barrier peak. The modelled and experimentally obtained *IV*-curves with no heating bias can be seen plotted in figure 33. The model does not provide quantitative values, so the theoretical curve has been normalised with a constant $w = \hat{y}y^T(yy^T)^{-1}$, given by the least square method, minimizing the difference between the measured currents $\hat{y}$ and the (scaled) theoretical currents y, at the corresponding voltages:

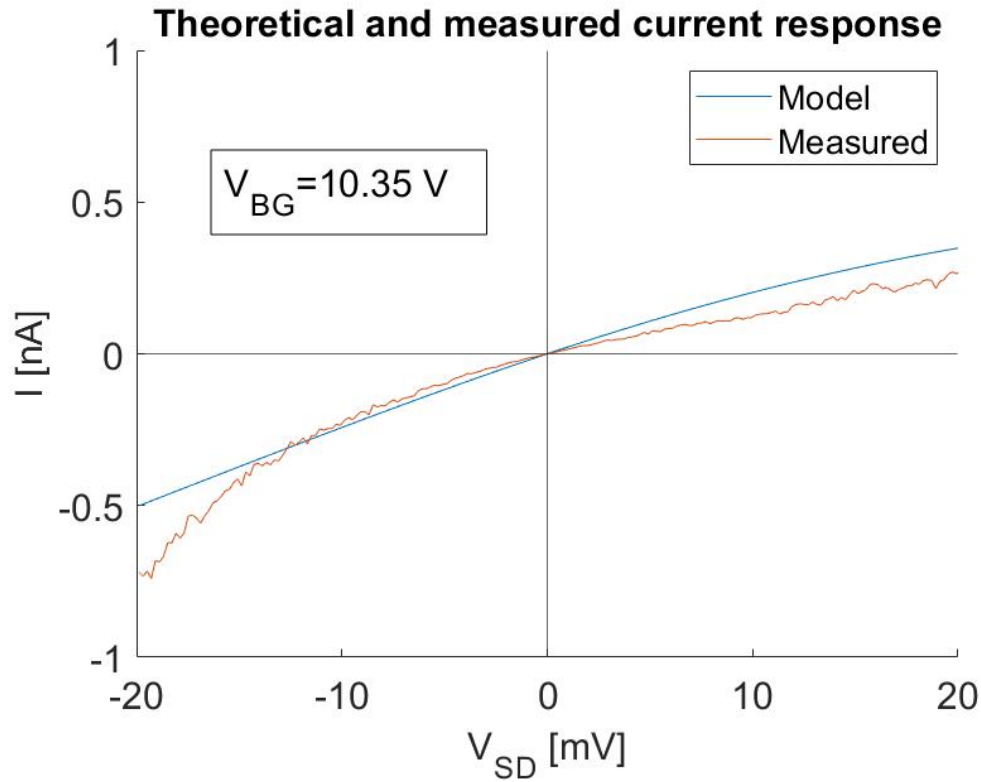$$w = \operatorname{argmin}_w \frac{1}{2}||\hat{y} - wy||_2^2. \tag{22}$$

Figure 33: Theoretical and measured current response at no heating bias at an ambient temperature of 77 K.

To model the case where there is a temperature gradient applied, IV-curves were obtained with a temperature difference between the two sides. IV-curves for a set of different temperature configurations $(\Delta T_R, \Delta T_A) = (0, 0)$ in black, (10,0), (20,0), (30,0) in red and (0,10), (0,20), (0,30) in blue, where ΔT_R and ΔT_A are the differences in temperature between the ambient temperature (77 K) and the temperature on respective side of the barrier, can be seen in figure 34. The chemical potential is kept at 535 meV over the conduction band edge on either side of the barrier. As the real value of the chemical potential, and the temperature difference across the barrier are not known, the current is plotted in arbitrary units.
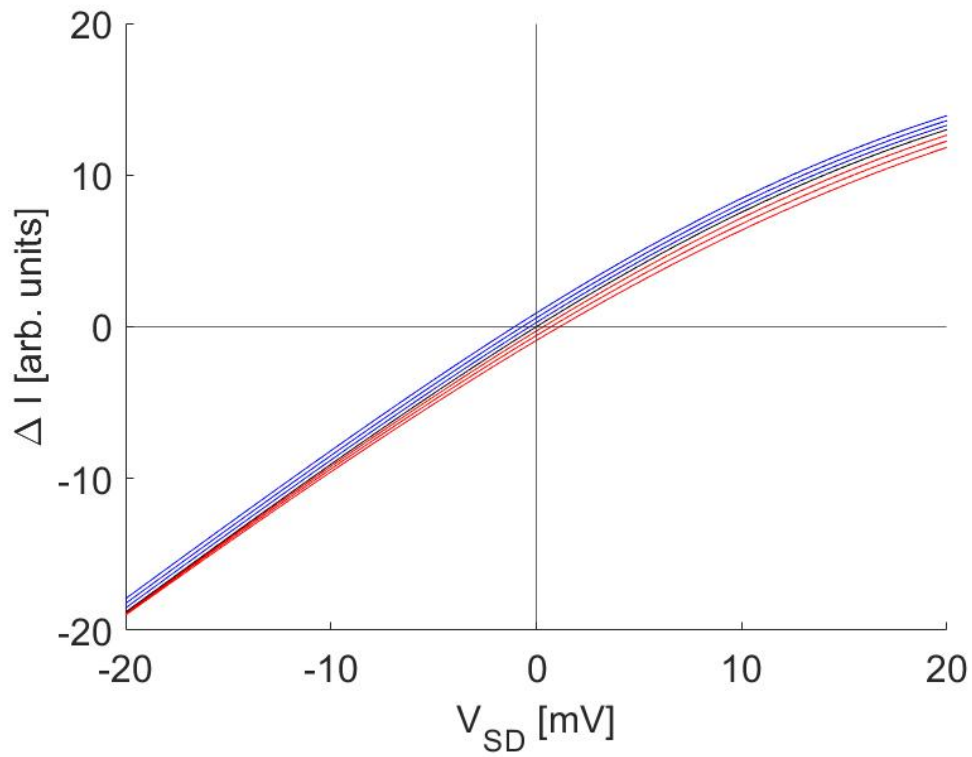
Figure 34: Modelled IV-curves for a set of different temperature configurations (ΔT_R, ΔT_A) = (0, 0) in black, (10,0), (20,0), (30,0) in red and (0,10), (0,20), (0,30) in blue.

The extracted I_{SC} can be seen in figure 35 a) and the V_{OC} can be seen in figure 35 b).
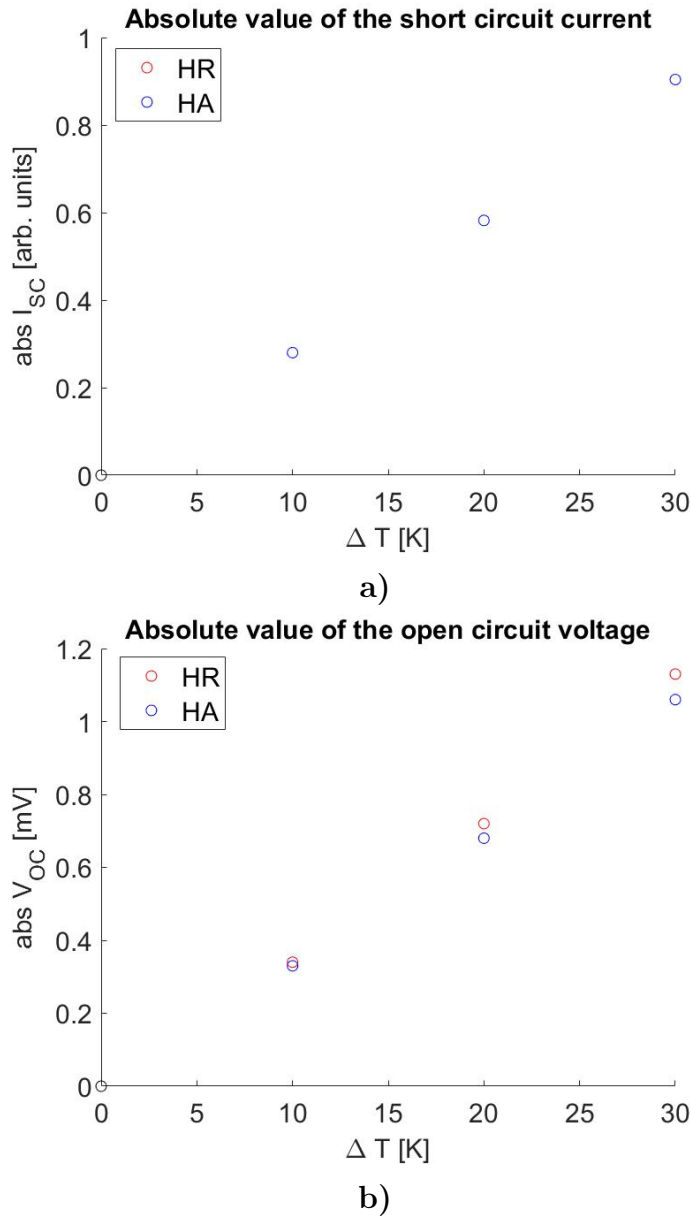
Figure 35: The extracted a) short circuit current, and b) open circuit voltage of.

To investigate a V_{BG} dependence of the V_{OC}, the V_{OC} was extracted from IV-curves at different chemical potentials with a temperature configuration of $(\Delta T_R, \Delta T_A) = (30, 0)$ (red) and $(\Delta T_R, \Delta T_A) = (0, 30)$ (blue), plotted in figure 36 a). The difference between the obtained V_{OC} with a temperature applied on either side of the barrier can be seen plotted in figure 36 b).
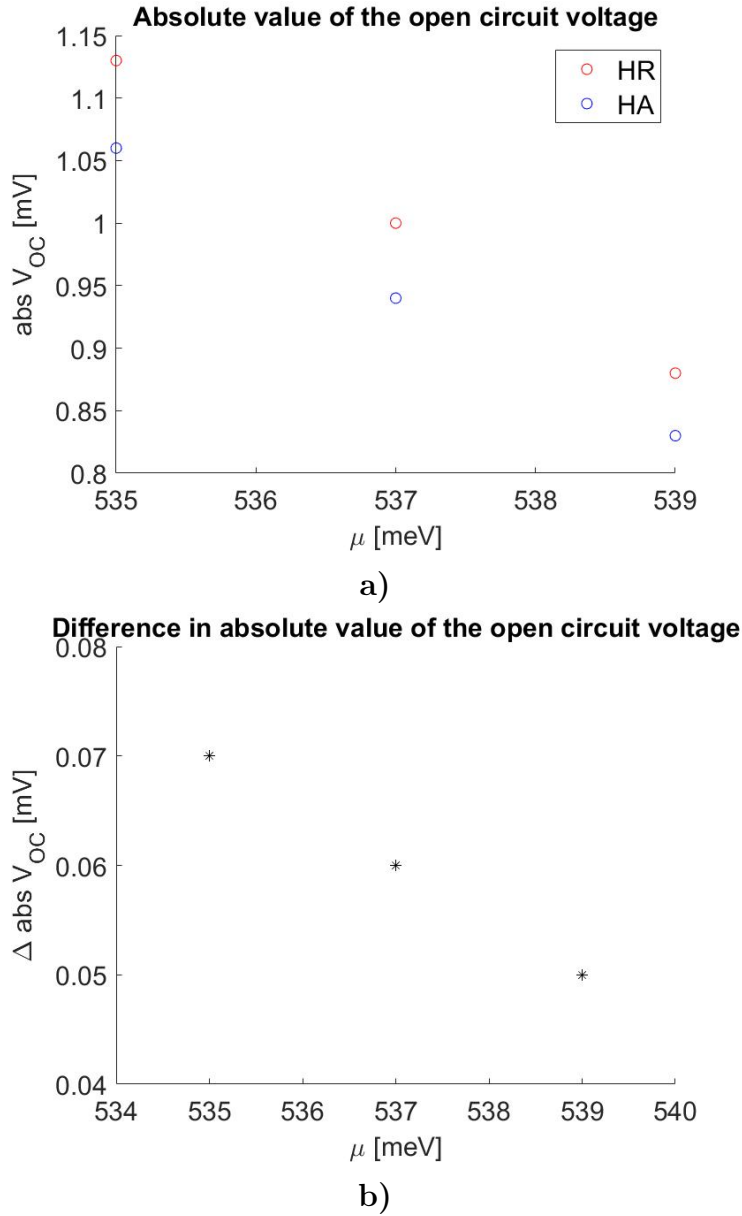
Figure 36: a) Generated open circuit voltages for $(\Delta T_R, \Delta T_A) = (30, 0)$ in red and $(\Delta T_R, \Delta T_A) = (0, 30)$ blue for a set of chemical potentials, and b) the difference between the open circuit voltages from adding a temperature difference on either side of the barrier.

The modelled IV-curve can be seen to not perfectly overlap with the measured IV-curve. But the theoretical and measured curves have some common features, for instance, neither exhibit a plateau for low V_{SD}, and they both seem to decrease more rapidly for negative V_{SD}, than for positive V_{SD}. However, the theoretical curve has a more linear appearance than the measured curve and the current response is even more negative for negative V_{SD} and less positive for positive V_{SD} for the measured curve than the theoretical.

The I_{SC} can be seen to overlap from applying a temperature difference on

either side of the barrier see figure 35 a), this is in line with the experimental results, see figure 26, and the reasoning conducted in section 4.1.3. The V_{OC} can be seen to be higher for heating on the ramp side of the barrier, see figure 35 b), which is opposite to what was seen in figure 27. In accordance with the reasoning in section 4.1.3, tunnelling through the narrow peak can for some back gate values be the reverse back flow of electrons that generate the highest V_{OC}, if the chemical potential is misplaced for the simulation, it could be so that the simulated system is not within this region.

The I_{SC} obtained from the simulations exhibit a seemingly linear appearance, see figure 35 a). With so few data points it is difficult to evaluate the shape of I_{SC}. Due to the limited scope of this project this was not pursued further, but to conduct a further comparison to the experimentally obtained data additional data points would be desired. Further exploration of I_{SC} could provide clues on both dominate features of transport, and detect differences between model and physical system.

There are several reasons to why the model does not perfectly predict the experimental results. Some of quantities and features of the physical system is not known. The position of the chemical potential is not exactly known and estimated in these simulations. The IV-characteristics depend on the position of the chemical potential (V_{BG} in the measurements), so a misplacement of the chemical potential the physical and modelled system are not the same. The shape of the barrier of that nanowire device will likely not be perfectly triangular but have some degree of roughness and possibly also slightly different shape. Another unknown is the length of the barrier. The barriers are known to be between 100-200 nm and is in the model approximated to 150 nm, but this can hence be off with ± 50 nm. The temperature difference at the barrier, and across the barrier, in the physical system is likely lower than the numbers that have been used in the model. Gluschke et. al. measured a temperature difference of 38-46 K at the contacts for room temperature and 4.2 K respectively, and as the heating creates a temperature gradient across the nanowire, this value is probably smaller at the barrier. This modelling has also assumed that the cold side of the barrier remain at the ambient temperature, this is probably also a false assumption. Josefsson et. al. [1] found a temperature difference across a quantum dot to be about 1 K at an ambient temperature of sub 1K. It is difficult to translate this value to liquid nitrogen and the measurements of this project as the heating power is not known. The model is also based on approximations and therefor to some extent based on simplifications of the physical system. Such simplifications include that

the transmission function does not change with V_{SD}, and hence with barrier shape, for energies above the barrier height in the model. The model does also describe a one-dimensional system, but the nanowires used in this project are probably not perfectly one-dimensional systems.

4.1.7. 77 K: Stability diagrams

Measurements of sweeping V_{SD}, stepping V_{BG} with different fix ΔV_H were performed on device B, with source-drain contact configuration SD1, see figure 14 (top), with bias ranges V_{BG}=8.5 - 11 V for the measurement with no ΔV_H applied, and V_{BG}=8.5 - 10.5 V for the measurements with applied ΔV_H, and V_{SD}=-5 - 5 mV for all measurements. The reason for the different ranges of V_{BG}, is that the measurements with no ΔV_H applied has an exploratory component to identify regions of interests. The differential conductance's can indicate quantum dot formations, and are plotted in figure 37.
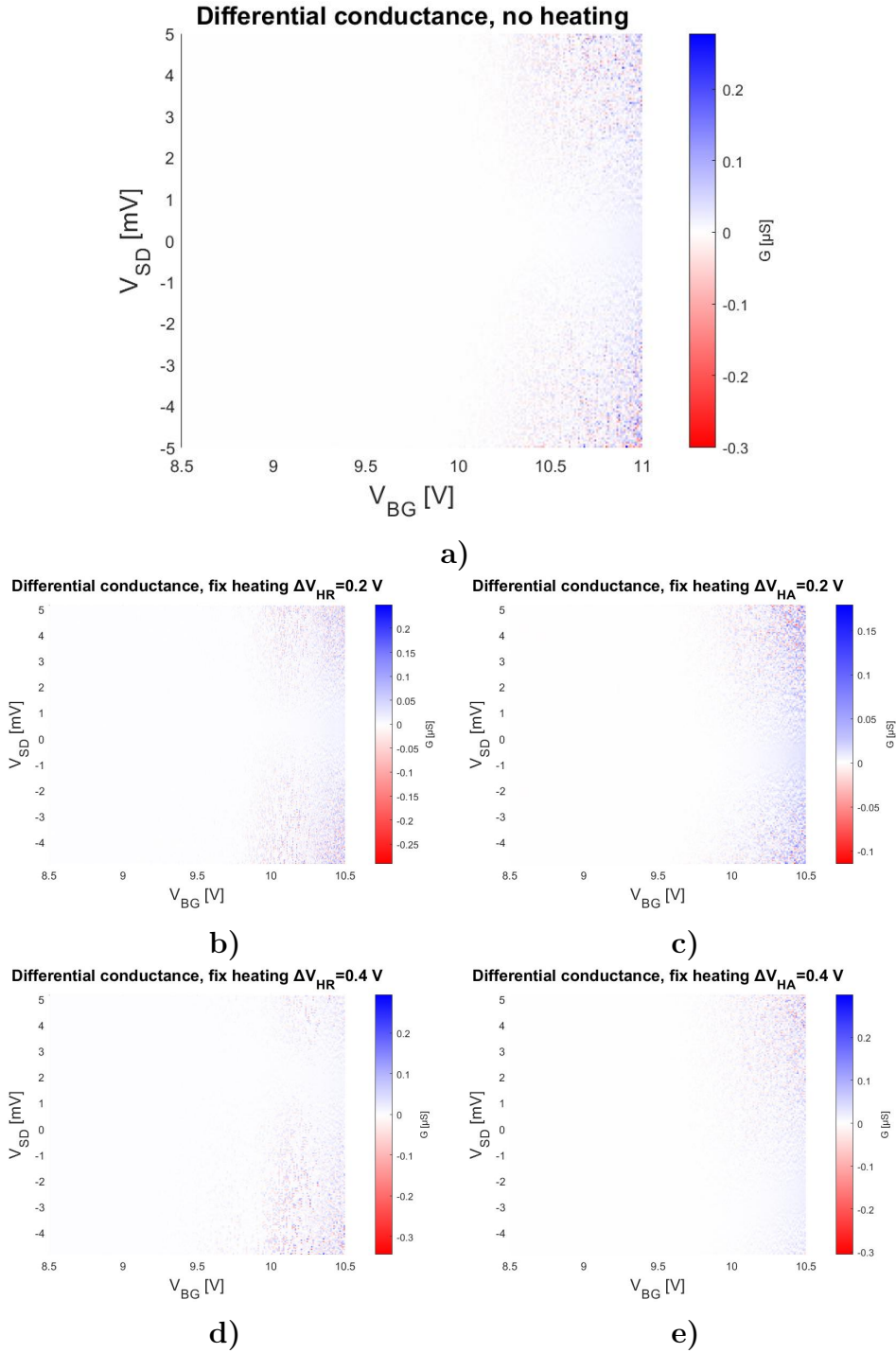
Figure 37: The differential conductance of device B with a) no heating bias, and with heating bias b) V_{HR}=0.2 V, c) V_{HA}=0.2V, d) V_{HR}=0.4 V, and e) V_{HA}=0.4 V.

Analysis

The stability diagrams in figure 37 show no indication of quantum dot formations in liquid nitrogen for device B. Due to instability of the device (which seem to change with time), the same measurements were not performed on the other source-drain configuration.

4.1.8. Differences between devices

In figure 38 the IV-curves of different devices at an ambient temperature of 77 K can be seen, all plotted for a range V_{SD}=-0.6 - 0.8 V, with source-drain contact configuration SD1.
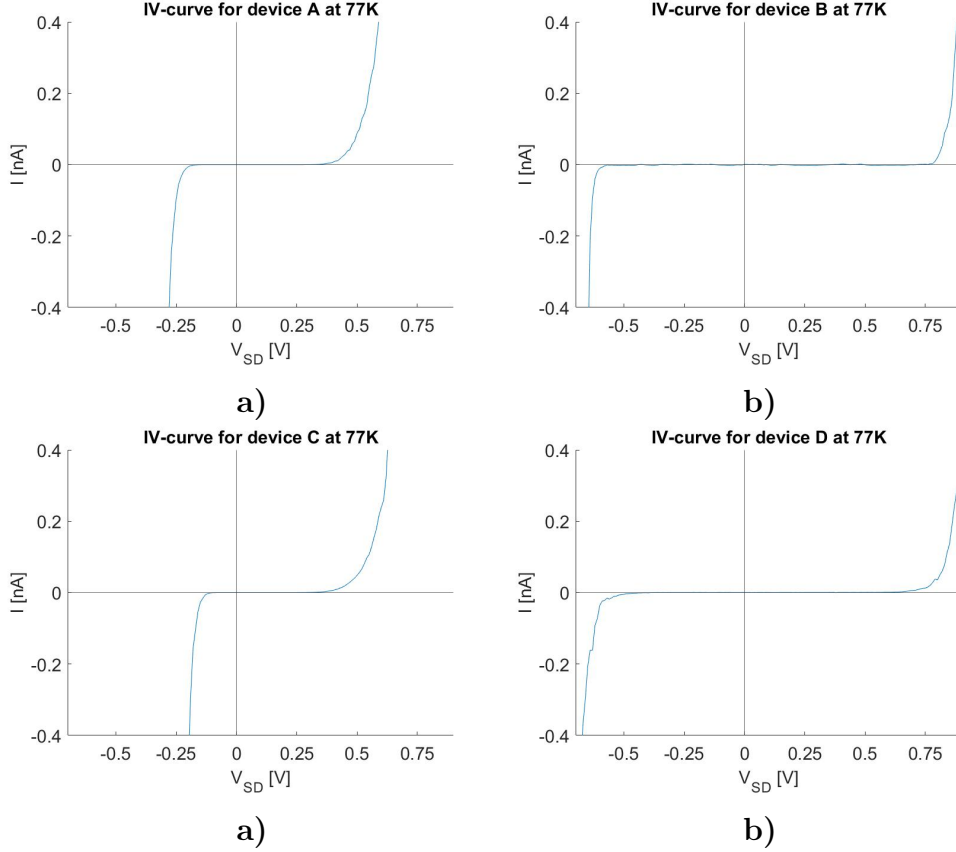

Figure 38: IV-curve of device a) A, b) B, c) C, and d) D.

Analysis

All the devices exhibit an asymmetry in the IV-characteristics, consistent with the reasoning in section 4.1.1. However, the IV-curves can also be seen to clearly differ in current onset.

The differences between the IV-curves seen in figure 38 could be due to difference in diameters of the nanowires. The length and steepness of the barrier can also differ between the nanowires, which could cause differences in IV-curves between devices. During growth, the barriers can also form slightly different, this could also contribute to the differences in IV-characteristics.

4.1.9. Source-drain contact asymmetry

IV measurements were performed on both source-drain contact configurations to investigate asymmetries of the devices and circuit. In figure 39 the IV-

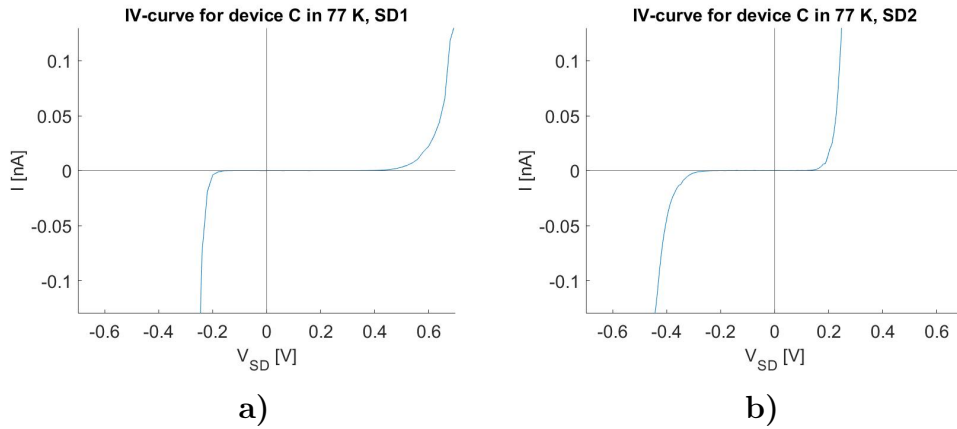curves in ambient temperature 77 K of device C can be seen, plotted in a range V_{SD}=-0.65 - 0.65 V.

Figure 39: *IV*-curve of device C with source-drain contact configuration a) SD1, and b) SD2.

The *IV*-curves in ambient temperature of 77 K of device B can be seen in figure 40, plotted in a range V_{SD}=-0.8 - 0.8 V.
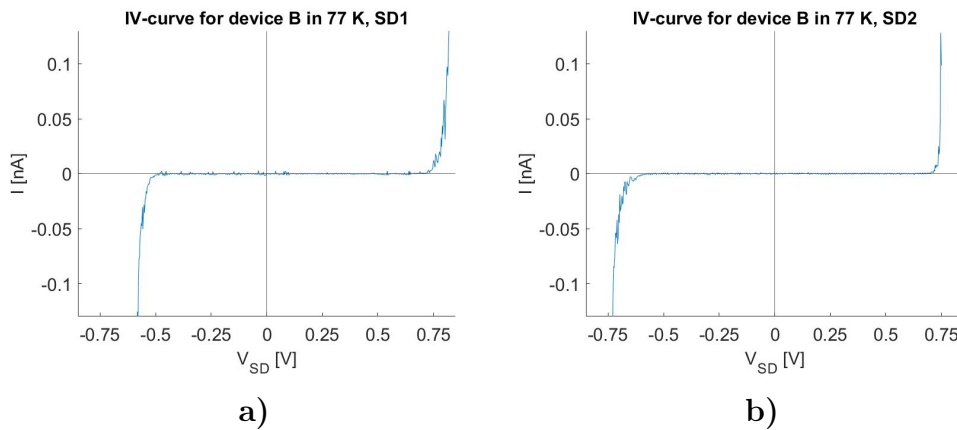

Figure 40: *IV*-curve of device B with source-drain contact configuration a) SD1, and b) SD2.

Analysis

The *IV*-curve could be expected to be mirrored when changing source-drain contact configurations. That is, the absolute value of V_{SD} of the current onset for negative bias with one source-drain contact configuration would translate to the absolute value of V_{SD} of the current onset for positive bias with the other, and respectively for the onset for positive bias. But considering *IV*-curves of device C and B, see figure 39 and 40, this is not the case.

The *IV*-curves at the two different source-drain contact configurations of device C, seen in figure 39, showcase an expected earlier current onset for negative

V_{SD} than for positive V_{SD} for SD1 and vice versa for SD2. But the current onsets are for slightly different (absolute) values of V_{SD}. There could be differences in resistance in the lithographic contacts and the bonding contacts, however, how the voltage drop across the circuit would probably be expected to be the same in the two source-drain contact configurations. The differences in current onset seen in figure 39 for the two source-drain contact configurations can not be fully accounted for or explained in this work. It could be due to some unknown asymmetries of how the voltage drops across the circuit that differs in the two different source-drain contact configurations, which could slightly enhance or decrease the onset asymmetry.

If considering the IV-curves at the two different source-drain contact configurations of device B, seen in figure 40, one of the configurations exhibit the expected asymmetry but the other seem symmetric about zero. Just as explained above, this phenomenon can not be explained by means of this work. But a potential asymmetry of the voltage drops over the circuit could cancel the asymmetry from the barrier, resulting in the curve seen in figure 40 b).

To investigate such asymmetry, V_{SD} could be applied symmetrically.

4.2. Sub 1K measurements

4.2.1. Sub 1K: The IV-curve

An IV-curve of device A performed in sub-kelvin (about 40 mK) ambient temperature can be seen in figure 41, with an applied $V_{BG}=2$ V and $V_{SD}=$-0.45 - 0.8 V, with source-drain contact configuration SD1.
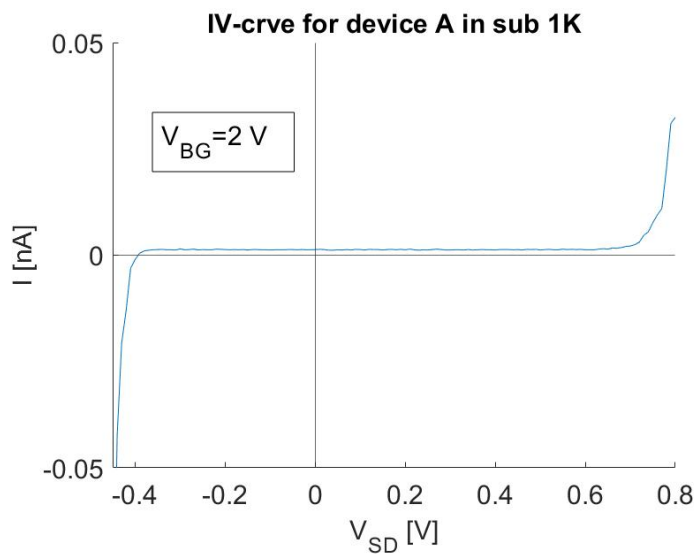

Figure 41: An IV-curve of device A in sub-1K ambient temperature with an applied V_{BG}=2V.

Analysis

If comparing the *IV*-curve performed in Triton, see figure 41, with the same measurement performed in ambient temperatures of 77 K and 300 K, see figure 21, the device requires more applied bias to be conductive (both V_{SD} and V_{BG} to achieved the plot seen in figure 41). This can be motivated in a similar sense as the difference between the measurements in ambient temperatures of 77 K and 300 K discussed in section 4.1.1. The Fermi distribution will in a temperature of 40 mK almost be a step function, similar to the T=0 K in figure 1, and a relatively high bias is required to allow electrons to pass the barrier.

4.2.2. Sub 1K: Stability diagrams

Measurements of sweeping V_{SD}, stepping V_{BG} with different fix ΔV_H were performed on device A, with source-drain contact configuration SD1. The differential conductance's are plotted in figure 42, with ranges V_{SD}=-50:50 mV and V_{BG}=4.7 - 6.5 V for the no heating bias measurements, V_{SD}=-13 - 13 mV and V_{BG}=5.5 - 6.5 V for heating bias ΔV_H=0.2 V, and V_{SD}=-6 - 6 mV and V_{BG}=6.2 - 6.6 V for heating biases of ΔV_H=1 V, 4 V. The reason for the different ranges of V_{SD} and V_{BG}, is that the no heating bias measurements and ΔV_H=0.2 V have an exploratory component to identify regions of interests. Stability diagrams of obtained with the other source-drain contact configuration, SD2, can be seen in figure 43, with the same corresponding V_{BG} and V_{SD} ranges.

Figure 42: The differential conductance of device A with a) no heating bias, and with heating bias b) ΔV_{HR}=0.2 V, c) ΔV_{HA}=0.2 V, d) ΔV_{HR}=1 V, e) ΔV_{HA}=1, f) ΔV_{HR}=4 V, and g)ΔV_{HA}=4 V. Note that the V_{BG} range is larger for the no heating bias and ΔV_H=0.2 V measurements.
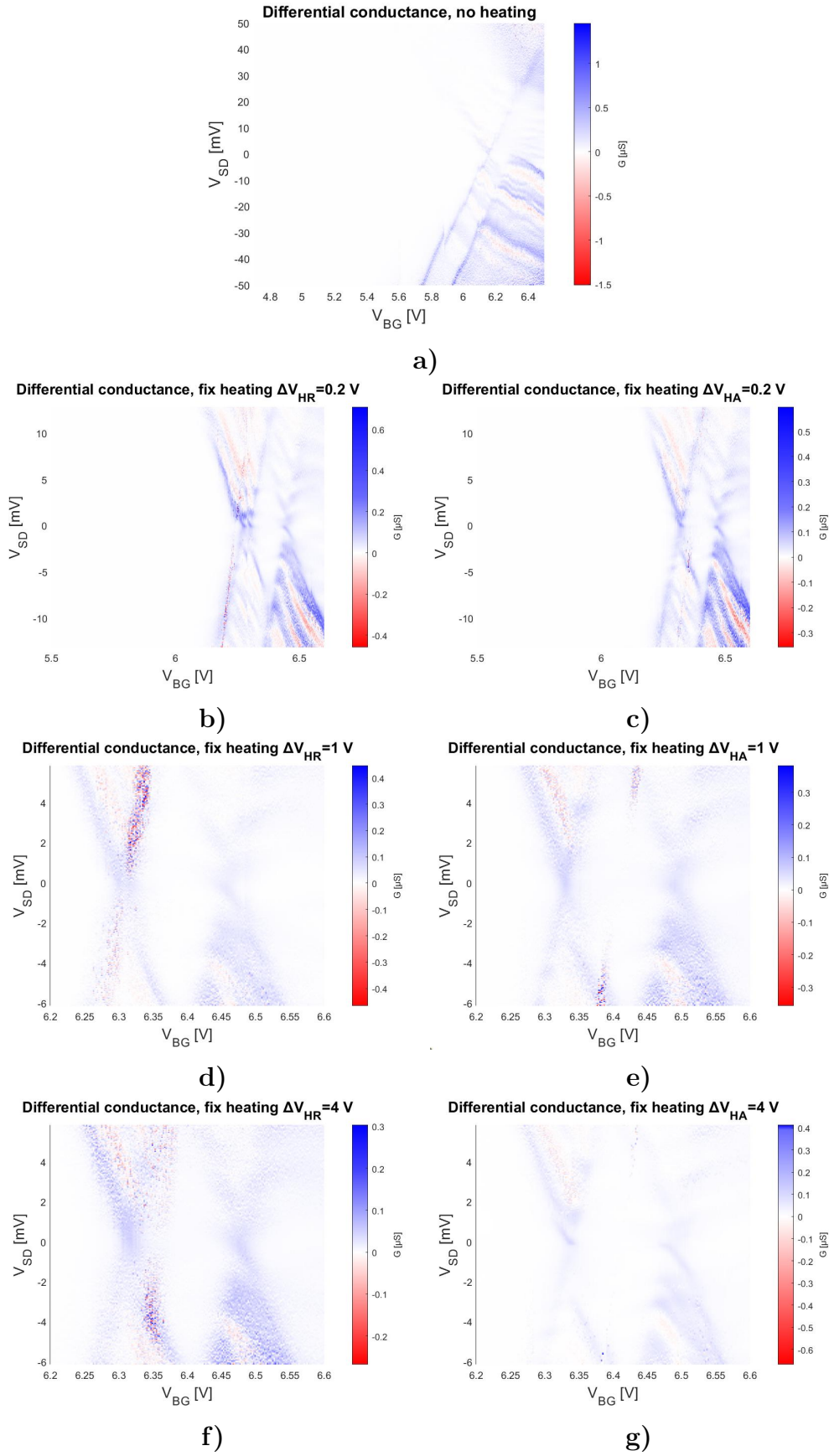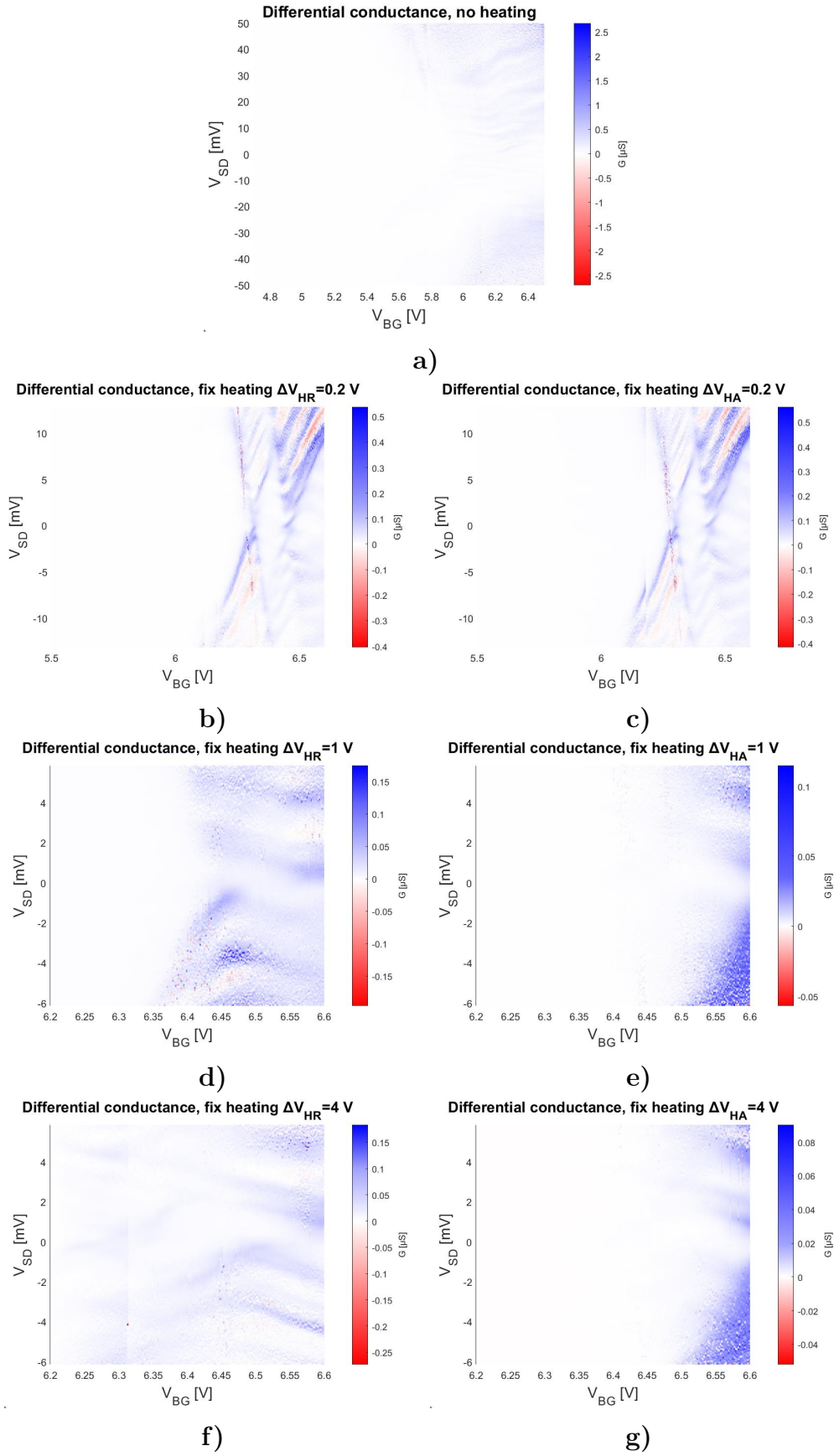
Figure 43: The differential conductance of device A with a) no heating bias, and with heating bias b) ΔV_{HR}=0.2 V, c) ΔV_{HA}=0.2 V, d) ΔV_{HR}=1 V, e) ΔV_{HA}=1, f) ΔV_{HR}=4 V, and g)ΔV_{HA}=4 V. Note that the V_{BG} range is larger for the no heating bias and ΔV_H=0.2 V measurements.

Analysis

The plotted differential conductance's in figure 42 show diamond shaped patterns, indicating formation of a quantum dot in the device. The potential barrier is not perfectly smooth, but has some degree of ruggedness created in growth, see figure 44 for a smooth barrier (left) and a more realistic barrier (right). At low temperatures such roughness in the barrier or nanowire structure can create puddles acting as a quantum dot, which would be in line with the appearance of the stability diagrams.

Figure 44: An illustration of the band structure with an ideal, smooth, ratchet-like barrier (left) and a more realistic, rugged, barrier (right).

A clear difference can be seen in the stability diagrams performed with different source-drain contact configurations, see figure 43. With most of the measurements on first source-drain contact configuration exhibiting quantum dot behaviour, while for the second only two exhibits quantum dot behaviour. The differences could be due to trapped charges and different electrostatic configuration at the different measurements. When switching the source and drain contacts, V_{BG} was run down to zero, to then be driven up to the V_{BG} where the stability diagrams were obtained again. This changing of V_{BG}, and hence the Fermi level, could have caused electrons to distribute differently, and causing different electrostatic configurations at the two settings. The asymmetric behaviour discussed in section 4.1.9, that can not be accounted for, could also be at play in these measurements, causing differences between the two contact configurations.

For heating biases of ΔV_H=1 V and ΔV_H=4 V for the second contact configuration, see figure 43, when the quantum dot behaviour is not prominent, heating on the different sides seem to cause different behaviour. However, due to the dominating quantum dot behaviour and effects of trapping of states, the focus of this project was turned to measurements in ambient temperatures of 77 K and 300 K where quantum dot behaviour was not detected.

5. Conclusions and outlook

This thesis has investigated whether an asymmetrically shaped thermionic barrier leads to asymmetric thermoelectric behaviour. This has been done by thermoelectric measurements on InAs nanowires with a compositionally graded

barrier of $InAs_{1-x}P_x$, forming a ratchet-like barrier. Measurements have been conducted at ambient temperatures of 300 K, 77 K, and sub 1 K, using a top heater design for thermal biasing via Joule heating.

Stability diagrams of measurement performed at an ambient temperature of sub 1 K exhibited features such as Coulomb diamonds, indicating quantum dot formation in the low temperature. Due to this, the focus of the project was turned to measurements in higher ambient temperatures, 77 K and 300 K, where no indications of quantum dot behaviour were detected.

Under no external source-drain bias and at an ambient temperature of 77K, symmetric thermocurrent response with respect to which side of the barrier that heating bias was applied to was demonstrated. As the transmission is expected to be the same from both sides of the barrier at short circuit conditions, this was interpreted as that the heaters on either side of the barrier did heat symmetrically. Evaluation of the open circuit voltage indicated a difference between heating on the different sides of the barrier, i.e. a non-linear response could be seen, signified by the asymmetric behaviour. Specifically, a higher open circuit voltage was observed when heating on the abrupt side of the barrier. The difference in open circuit voltage is proposed to be a result of the asymmetric barrier. The transport mechanism behind this can be explained by an asymmetry in tunnelling current through the narrow top of the barrier.

Thermocurrent was also detected at 300 K. The open circuit voltage was extracted for the same heating bias at different back gate values. This did not indicate that the difference between the obtained open circuit voltage from heating on either side of the barrier changed with global back gate, which could indicate that there also is a temperature dependence in which side generate the highest open circuit current when heated.

Some key features of the experimentally obtained current response, such as the overall shape of the IV-curve and to some extent how applying a temperature gradient influences the current response, could be captured using the WBK approximation to model the system. Modelling of the open circuit voltage did also indicate that there could be a back gate dependency (formulated in terms of chemical potential in the model) of the open circuit voltage. This provided theoretical support for some of the behaviours of the experimentally obtained results.

This thesis provides a first step towards an understanding of the thermoelectric

properties of an asymmetric, triangular, barrier and its potential as a system for thermionic extraction. An asymmetric thermoelectric response was demonstrated, which is the first indication of that shape of the barrier matters for thermionic extraction.

There are several suggestions for continued electrical characterisation. For example, measurements could be conducted to investigate if the relation between V_{OC} from heating on either side of the barrier has a temperature dependency. This could possibly be done by using a dip stick with a thermometer placed in a liquid nitrogen dewar and performing measurements in different temperatures by gradually changing the position of the sample in relation to the liquid nitrogen surface. Second, the mechanism dominating transmission may differ not only with ambient temperature but also with temperature gradient across the barrier. It would therefore provide additional insight to further push the devices by applying higher heating biases. For reproducibility, testing of additional devices could provide helpful input. Especially as the devices investigated here have shown fluctuations in conductance, likely due to surface trap states. Additional devices would provide higher reliability and confidence in the results.

It would be valuable if the relation between heating voltage applied to the heater and the resulting temperature at the corresponding end of the nanowire could be determined. This would require further development of theory, possibly by adapting the curves to the diode equation used in [12] to fit the current response with and without heating bias applied, or to further develop the theoretical model used in this project.

To fully understand the mechanisms behind the observed thermocurrents and thermovoltage, the theoretical model requires further work or development until it can accurately reproduce the experimental observations. For example, a V_{SD} dependence of the transmission function for energies above the barrier height could be included. The uncertainty of the correspondence between theoretical model and physical system could also be reduced if the experimental shift in chemical potential as a function of V_{BG} could be established. Another approach to find the position of the chemical potential would be to fit the modelled IV-curve to the experimentally obtained IV-curve with the position of the chemical potential as a variable. The temperature difference across the barrier is unknown in the physical system, a better understanding of this would provide better conditions for accurate modelling. On the other hand, such model could be used as a tool to find the temperature difference.

It would also be of interest to further evaluate the performance in terms of conversion efficiency and power, and to compare the ability of thermionic extraction of an asymmetric barrier with other systems, such as rectangular thermionic barrier or a quantum dot. Identifying methods to establish the conversion efficiency and power and subsequently performing required measurements would be of highest interest.

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6. Appendix

6.1. Appendix A - Nanowire growth

In the 1960s Wagner successfully grew silicon microwires using the vapour-liquid-solid (VLS) method, about thirty years later nanowires in the 10 nm scale were grown using the VLS method [14] and the ideas of the VLS has remained the base for many nanowire growth approaches [16]. The basic principle of VLS is that metal nanoparticles are used as catalysts to initialise growth of desired semiconductor materials in gas phase. The metal particle is heated to create a liquid metal-semiconductor eutetic alloy. Growth spices in gas phase that come in contact with the metal particle will be incorporated and a crystal will form at the liquid-solid interface. [14, 16]

The nanowire growth approach relevant for this project is an evolved VLS method performed in a chemical beam epitaxy (CBE) environment. In the CBE approach, the growth is performed in ultra-high vacuum, and instead of presenting the precursors as a vapor they are introduced as a beam. [16] To form the heterostructure, the precursors of the beam is varied. [7]

In this project, the nanowires were grown using CBE from 40 nm diameter Au aerosol seed particles deposited on InAs (111)B substrates.

6.2. Appendix B - Nanoscale semiconductor procession

6.2.1. Scanning electron microscope

The principle of an electron microscope is similar to that of an optical microscope. Instead of a beam of light originating from a light source as in an optical microscope, an electron microscope has an electron source providing a beam of electrons and electromagnets are used to focus the electron beam like optical lenses in an optical microscope. The electron microscope has much higher resolution than an optical microscope, enabled by the much shorter electron wavelengths than optical wavelength normally used. A scanning electron microscope (SEM) is a type of electron microscope, where highly energetic electrons are emitted from an electron gun that scan surface of the specimen, to create an image, the backscatterd electrons are collected. SEM provide very high resolution and has a high magnification power. [32]

6.2.2. Electron beam lithography

Electron beam lithography (EBL) is an important technique in nanoprocessing, allows for writing of high resolution patterns [33]. EBL was evolved from SEM when an electron sensitive polymer material was discovered, polymethyl-methacrylate (PMMA), that could be used as resist. An EBL system works

similarly to a SEM, with a focused electron beam directed to the sample of interest.[34] There are two classes of EBL resists; positive and negative. A positive resist becomes more soluble when exposed to the electron beam, and the negative become less soluble when exposed to the ion beam. PMMA was used in this project and is a positive resist, and positive resists will be the subject for the rest of the discussion. [33] When the electron beam enters the sample, it collides with atoms in the resit and substrate. This causes electrons to deflect, which broads the beam. [33] The energy of the electrons, controlled by the acceleration voltage, are important for the exposure process. High energy electrons generate higher resolution with less broadening of the beam within the resist, than electrons of low energy. However, low electron energies create a better undercut, which can be desirable as it facilitates lift-off. [34]

6.2.3. Evaporation
Evaporation in this project were performed by a physical vapor deposition (PVD) technique. In PVD a source material in solid state is changed into vapor phase. The source material is then evaporated in gas phase and transported to the target where it is deposited as a thin film. [32]

6.2.4. Focused ion beam
A focus ion beam system (FIB) is based on the same principles as electron beam systems, but a FIB has a beam of ions instead of electrons. Just like a SEM, the FIB has a emission source, but of ions instead of electrons, and a focusing mechanism, some tools has dual beam system which can operate at both ion beam (acting as a FIB) and electron beam (acting as a SEM). The difference is that a FIB have different mass and (possibly) different charge. The FIB can be used to sputter away material. When an ion beam bombard the surface of the specimen, the ions transfer energy to the atoms of the specimen. Some of these atoms can then escape from the solid. [34]

6.2.5. Atomic layer deposition
Atomic layer deposition (ALD) is a technique to deposit thin films. It is performed by sequentially introduce two or more precursors to the surface of a substrate, the precursors react and form sub-monolayers. The precursors are pulsed sequentially, with purging of the excess precursor between the precursor pulses. The precursors react at the surface of the substrate and one new layer is created at the time, and the process is repeated until desired thickness of the film is achieved. [35]

6.3. Appendix C - Dilution Refrigerators
Dilution refrigerators (DR) are one type of sub-kelvin cooling systems, that is, it is used for cooling below 1 K. A DR rely on properties of a mixture of helium

isotopes for cooling, specifically ^{3}He-^{4}He mixtures. The ^{4}He atoms are Bose particles, and at temperatures below 2.7 K ^{4}He is essentially a superfluid with zero viscosity ans zero entropy. [36] The ^{3}He atoms are Fermi particles, and the Pauli exclusion principle will prevent ^{3}He from transitioning to a super-fluid until significantly lower temperatures. ^{3}He-^{4}He mixtures does transition into superfluid, but the temperature for this transition is dependent on the concentration of ^{3}He, see figure 45 a). [37] At temperature below 0.87 K phase separation occurs for a ^{3}He-^{4}He mixture. If the concentration of ^{3}He is above 6.6 % the ^{3}He-^{4}He mixture separate into a ^{3}He rich phase and a concentrated phase. The concentrated phase will float on top of the dilute phase due to higher density, see figure 45. The finite solubility of ^{3}He in low temperatures is to core of DR systems.
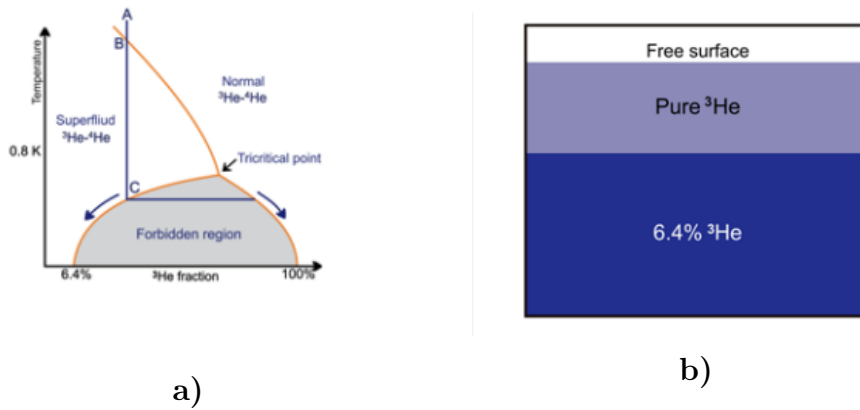

a)

b)

Figure 45: a) A phase diagram of ^{3}He-^{4}He mixtures, and b) illustration of the phase separation of ^{3}He-^{4}He mixtures at low temperatures. Reprinted from [37].

The process of DRs is to cool ^{3}He by being pressurised in different tempera-tures, and by flowing through heat exchangers where it is cooled of the return flow. ^{3}He then enters the mixing chamber with a concentrated phase and a di-lute phase, and the ^{3}He that pass through the concentrated phase-dilute phase interface will contribute to cooling. ^{3}He leaves the mixing chamber in dilute phase and will flow through the heat exchanger and cool incoming ^{3}He before entering a heated still. Due to the higher vapor pressure of ^{3}He compared to ^{4}He this will lead to evaporation of mainly ^{3}He. The ^{3}He that evaporated in the still will continue to a new cycle. [36]

6.4. Appendix D - 77 K: IV-curves under heating SD2

IV measurement at an ambient temperature of 77 K with thermal bias, at V_{BG} =10.5 V. The measurement was performed on the same device and same cool down on with the source-drain contact configuration, SD2, with source at the abrupt side of the barrier and drain at the ramp side of the barrier,

see bottom figure 14. The contacts were switched without driving down back gate, see figure 46. However, to obtain stable measurements, the back-gate value differs, and no quantitative comparison can be conducted.
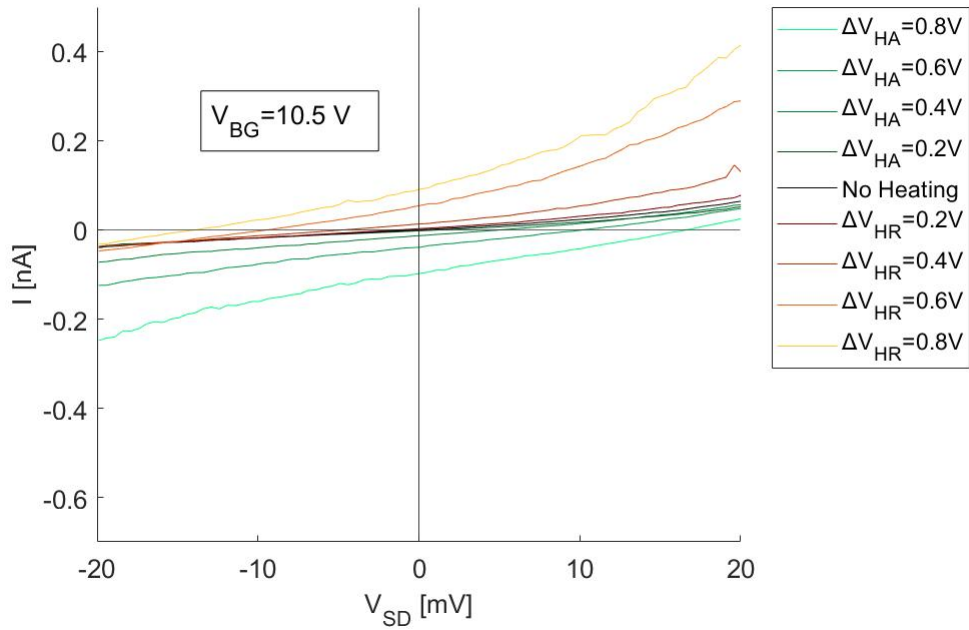

Figure 46: *IV*-curves at V_{BG}=10.5V, with heating on either side of the barrier. Heating on the abrupt side of the barrier is indicated in a green scale and heating on the ramp side of the barrier is indicated in an orange scale. Each line is an average of six sweeps.

From the *IV* measurements, the short circuit current and the open circuit voltage can be extracted for different heating voltages for each side, presented in figure 47 a) and b) respectively.
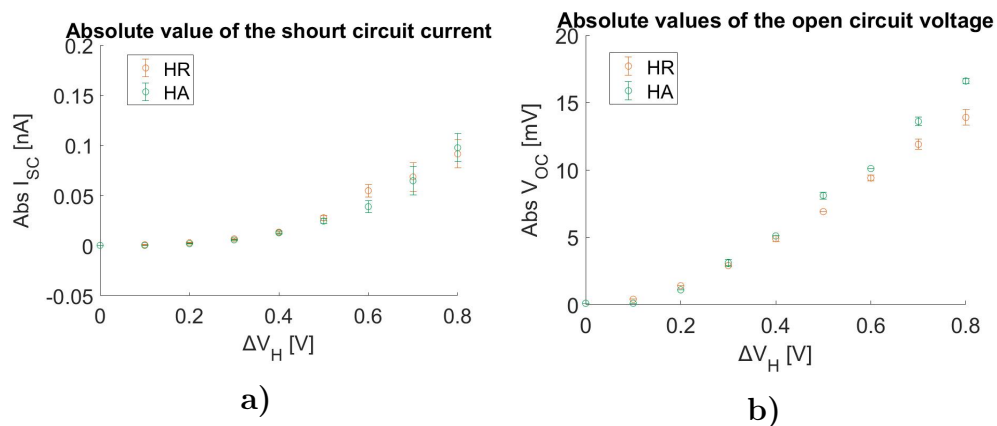

Figure 47: Extracted values of the a) short circuit current and b) the open circuit voltage, form heating on either side of the barrier with error bars represent the standard deviation of the sweeps.

Analysis

Performing the same measurements with the source on the abrupt side and the drain on the ramp side of the barrier show a positive I_{Sc} and negative V_{OC} for heating on the ramp side of the barrier and a negative I_{SC} and positive V_{OC} for heating on the ramp side of the barrier see figure 46. This is expected as it the same mechanisms in work only the source and drain switched in relation to the barrier, causing the current to switch sign. Illustrations of transport at short circuit conditions can be seen in figure 48 a) and b), and at condition I=0 A in figure 48 c) and d) for drain on the ramp side of the barrier and source on the abrupt side off the barrier. In reverse configuration, the same trends for I_{SC} and V_{OC} are seen, indicating that the observations is not due to the asymmetries in the circuit.
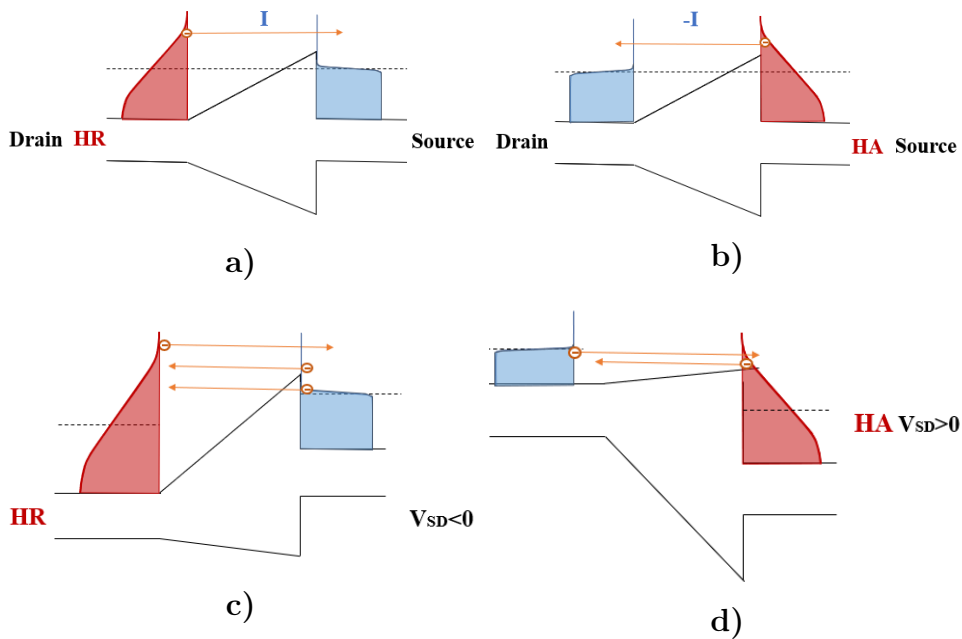

Figure 48: Illustrations of the short circuit current when heating on a) the ramp side of the barrier and b) the abrupt side of the barrier, and transport at open circuit conditions when heating on c) the ramp side of the barrier and d) the abrupt side of the barrier.

6.5. Appendix E - Handling unstable devices

The majority of the measurements conducted in 77K and 300K were performed on device B, but an obstacle to obtain clean data was unstable behaviour of the device. In figure 49 an *IV* measurement of device B can be seen. The jumps in current could be due to trapping and detrapping of electrons changing the conductivity of the device.
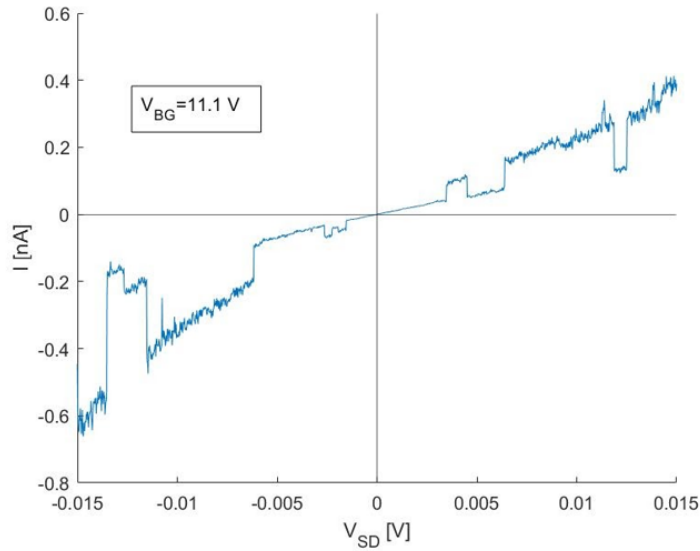
Figure 49: *IV*-curve of device B in 77 K, with a sweep time of 6.5 min, exhibiting unstable behaviour.

Here is a short summery of how the instability was handled in this project

• The device seemed to be more stable for some values of V_{BG}, this was used by exploring the current response for different values of V_{BG} and measurements were conducted for more stable V_{BG}. As discussed, this was one of the major limitations to what measurements could be performed, and how different measurements could be compared.

• When a more stable value of V_{BG} was found, V_{BG} were not adjusted, as adjustments seemed to disturb the stability.

• The measurements, and measurements series were limited in time.

• For some measurement types, multiple measurements at the same setting were performed and then averaged, both to suppress noise and current fluctuations.

• To ensure stability throughout a measurement series, reference sweeps were obtained before, between measurements and after the measurement series in the form of *IV*-curves at that value V_{BG}.

• The device did also seem effected by thermal recycling, which could be due to that the device freezes differently at cool down.

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