D-band Power Amplifiers in Vertical InGaAs Nanowire MOSFET Technology for 100 Gbps Wireless Communication

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Abstract

Two different topologies of power amplifiers (PAs) are designed in the frequency range 130-174.8 GHz for use in backhaul transmitters. These are the pseudo-differential common source (PDCS) and the single-ended stacked amplifier topologies. The PAs are designed in Cadence AWR design environment with virtual source models, implemented in Verilog-A, of InGaAs nanowire transistors using a 20 nm gate length. The results are compared amongst each other as well as with other state-of-the-art PAs. The PDCS PA achieves a simulated gain of 24.1 dB, a saturated output power (P_{sat}) of 12.1 dBm, a maximum power-added efficiency (PAE_{max}) of 9.8 % and an output power at the 1 dB compression point (P_{1dB}) of 8 dBm using a supply voltage of 0.81 V. The stacked PA achieves a gain of 18.9 dBm, P_{sat} of 13.6 dBm, PAE_{max} of 14.6 % and P_{1dB} of 10.4 dBm using a supply voltage of 2.25 V. Additionally simulations using AWR Microwave Office is performed to evaluate the system performance of the PAs when transmitting at a data rate of 100 Gbps. The PDCS PA and stacked PA achieved a maximum output power of 3.6 dbM and 6.5 dBm respectively at the error vector magnitude (EVM) limit of 3.5 % for 256 QAM signals. For 64 QAM signals they achieved a maximum output power of 6.5 and 8 dBm respectively at the EVM limit of 5.5 %.

Popular Science Summary

As cellphones and computers are able to achieve a fast internet the need for faster communications might seem unnecessary to the average user. But as technology advances the amount of devices which use it increases, everything from household appliances to cars are becoming connected to the internet. While some applications are simple quality-of-life, improvements others may improve modern society, one example being autonomous driving cars. In an ideal world where all cars are autonomous and shared, the amount of cars could decrease significantly which in turn would open up space in urban environments. In this scenario the need for traffic lights would be eliminated, and while it may seem like a small change it could reduce the time it takes to travel by car. As well as reduce the environmental impact of having multiple cars in idle.

While the relatively newly launched fifth generation cellular network (5G) have made improvements to the data rate, it is necessary to increase it further. Beyond 5G cellular networks are looking to expand the data rate by operating at higher frequencies than its predecessors. These frequencies are often referred to as mmWave frequencies. In wireless communication the data is sent with electromagnetic waves. The data rate is correlated with the bandwidth of the signal, the bandwidth being the span of frequencies that the signal covers. Higher frequency ranges has a greater amount of available bandwidth, which can be used to increase the data rate.

Higher frequencies do however pose a difficult task for the transistors. The scaling of transistors has shrunk them to a point where new transistor technologies are necessary. The vertical nanowire transistor is one technology which has a great performance and area-efficiency.

The power amplifier is the final stage before the antenna in a transmitter. It amplifies the signal, with a larger output power of the signal it may travel further without being undetectable. However, careful design has to be performed to not destroy the shape of the signal in the process. In this thesis two different circuit architectures are designed using nanowire transistors, and then compared with other technologies to verify that the technology is competitive and suitable for high data rate communication at high frequencies.

Acknowledgements

We extend our utmost gratitude to our supervisors, Tobias Tired and Lars Ohlsson Fhager, who with their extensive knowledge has enabled us to complete this thesis through meaningful discussions and feedback sessions. A thank you to Lars-Erik Wernersson for taking his time to guide us through the choice of master's thesis. Additionally this master's thesis would not have been possible without NordAmps, and we would like to thank them for giving us the opportunity and for making us feel welcomed. A special thank you to Simon Olson for providing us with insights in day to day discussions.

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Chapter 1

Introduction

1.1 Background

The need for an increased data transfer rate is a continuously growing problem of the digital world. Not only does consumers of cellular data want faster communication, but with the advancement in technology more and more application areas are developing which require incredibly large amounts of data to be transferred continuously. For example autonomous driving requires a significant amount of data to be transferred and evaluated constantly. One possible solution to increase the data transfer rate is to increase the bandwidth of operation. As there is a lot of available bandwidth at higher frequencies, operating there is suitable to achieving a high data rate. The D-band (130-174.8 GHz) shows promise for long distance transmissions as the loss due to atmospheric absorption, as shown in Figure 1.1, is relatively low[1].

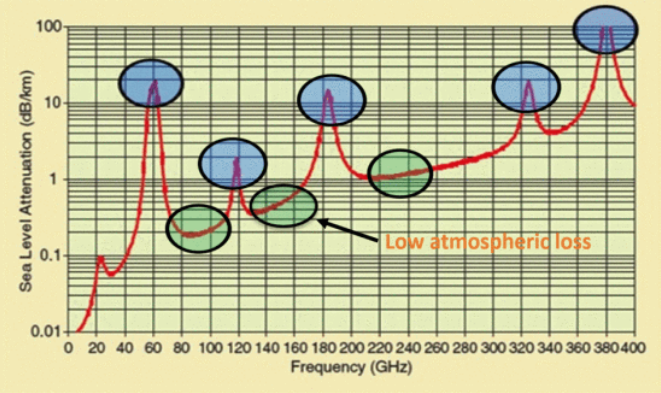


Figure 1.1: Atmospheric absorption over frequencies. The green circle indicated by Low atmospheric loss indicates that the D-band is a suitable candidate for long-distance transmission. [1]

To operate at these frequencies has proved difficult for Si-based transistors as it is too close to the maximum current- and power-gain cut-off frequencies (f_T and f_{max} respectively). For example, Global Foundries 22 nm fully-depleted silicon on

insulator (FDSOI) has an f_{max} of 290 GHz[3], or the Infineon B11HFC SiGe 130 nm technology having an f_{max} of 370 GHz[4]. With this in mind, III-V compound based transistors, possible of reaching f_T and f_{max} of 600 GHz and 1 THz respectively, are of great interest[5].

The aim of this master thesis is to develop a power amplifier (PA) design, using the AWR design environment, for backhaul applications within the D-band, based on the III-V nanowire transistor technology from NordAmps. In order to establish that the amplifier is of use to industry it will be compared to existing technologies in terms of saturated output power (P_{sat}), gain, supply voltage and power-added efficiency (PAE). The PA is then tested in Microwave Office to evaluate the performance using a high order modulated signal with the goal of achieving 100 Gbps wireless transmission.

Chapter 2
Theory

2.1 Transistor

The transistor technology from NordAmps originates from research at Lund university. It consists of vertical nanowire transistors made of the compound InGaAs grown on a Si wafer[6],[7]. Each transistor consists of a number of nanowires divided into a set of gate fingers. The gate length is in this work set to 20 nm and it stretches around the nanowire with a 25 nm diameter in a gate-all-around (GAA) structure. The source is at the bottom and the drain on the top as shown in Figure 2.1a.

In order to improve the frequency range of the transistor, to allow high frequency PA design, adjustments are made to the device layout. For example rather than contacting the drain as a full pad on top of the wires, the drain contact is split into fingers as shown in Figure 2.1b, with the amount of fingers being equal for the drain and the gate. Another important adjustment is performed due to the breakdown voltage (V_{bd}) of the transistor, which in itself is fairly low, at approximately 0.5 V_{rms}. By extending the gate upwards with a spacer layer of SiO_2 as well as the high-k gate oxide, a so called field plate capacitor is formed. This adjusts the band bending on the drain side of the channel and can increase increase the V_{bd} significantly[8].

Dividing the drain into fingers increases the transistor f_{max} by roughly 20 GHz as it reduces the parasitic capacitance between drain and source, but the use of a field plate capacitor increases the drain to gate capacitance, ultimately reducing the f_{max}. For high power applications such as the PA, the benefit of having a higher possible voltage swing does however outweigh the drawback of a slightly reduced f_{max}. For example, a transistor with 620 wires and 10 fingers has its f_{max} reduced from 419 GHz to 388 GHz with a 31 nm long field plate capacitor, given the same bias conditions. This results in a loss in Maximum Stable Gain (MSG) roughly 0.67 dB throughout the frequency band of operation but increases the V_{bd} to 0.9 V_{rms}. The model of the transistors used in the simulations are provided to us by NordAmps. They are Virtual Source [9] models adjusted to fit the technology of NordAmps transistors.[10],[11]. The characteristics of two transistors with the dimensions of 10 fingers, and 620 or 810 wires respectively have been studied.

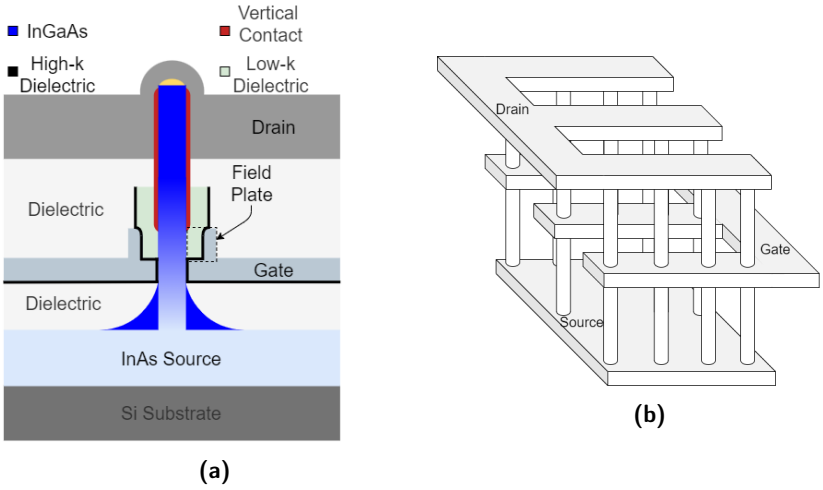
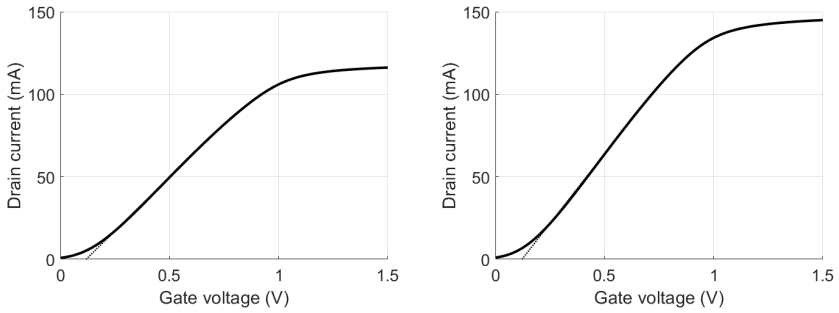


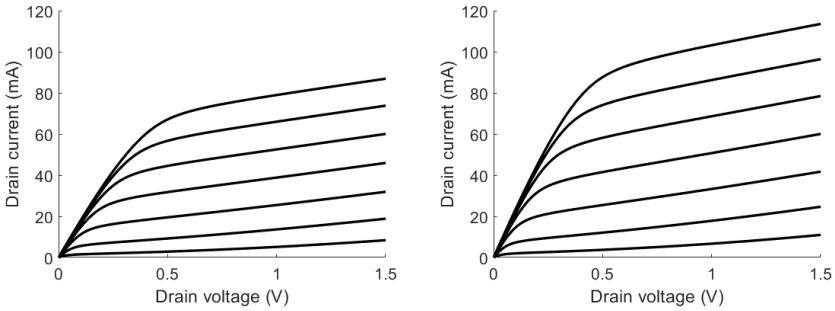
Figure 2.1: Structure of the nanowire transistors of NordAmps. (a) shows the structure of each nanowire, (b) highlights how the gate and drain fingers connect each nanowire.

The V_{ds} of the transistors are 0.81 V and 0.75 V, respectively. Transistors with these values are presented because they represent the output stage transistors of the different designs, as will be further elaborated in Chapter 3. The transfer characteristics are shown in Figure 2.2 where a linear approximation has been performed to show that the transistors have a V_t of roughly 0.12 V. The output characteristics are shown in Figure 2.3 where V_{gs} increases linearly in steps of 0.1 V from 0.1 to 0.7 V.



(a) 620 wires, 10 fingers, $V_{ds} = 0.81$ V. **(b)** 810 wires, 10 fingers, $V_{ds} = 0.75$ V.

Figure 2.2: Transfer characteristics of two nanowire transistors.



(a) 620 wires, 10 fingers. **(b)** 810 wires, 10 fingers.

Figure 2.3: Output characteristics of two nanowire transistors, V_{gs} increases linearly in steps of 0.1 V from 0.1 to 0.7 V.

By biasing the transistors at a certain gate voltage the f_{max} and f_T is extracted by applying an input signal of increasing frequency and measuring the S-parameters of the device. This allows calculation of the Mason's unilateral gain, U, and current gain, H21, parameters. The f_{max} is given when the unilateral masons gain is unity, while f_T is given by where the extrapolated -20 dB/decade slope of the H21 parameter reaches unity. Figure 2.4 shows the extraction of the f_{max} and f_T for a 620 wires transistor with a current of 23.2 mA.

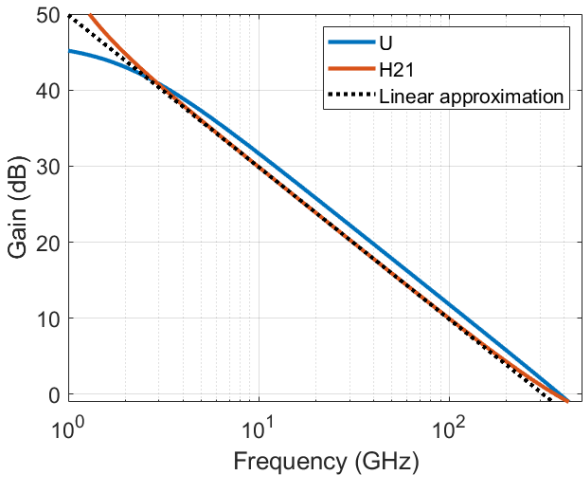


Figure 2.4: Extraction of f_t and f_{max} for a transistor with 620 wires, 10 fingers, V_{ds} of 0.81 and I_{ds} of 23.2 mA.

By sweeping the current and extracting the f_{max} and f_T, as shown in Figure 2.5a, it is possible to determine a biasing point for which the gain of the device is at an optimum. The transconductance g_m shows a similar maximum current value, as seen in Figure 2.5b. One contributing factor to the f_{max} being larger for the smaller transistor is that its V_{ds} is larger. Another factor is the gate resistance.

With a larger amount of wires to each finger the length is on average longer to each of them. With the length being larger comes a greater gate resistance, and with that the f_{max} decreases. This reasoning also applies to the fingers, by increasing the amount of fingers the gate resistance is lowered. This reasoning applies until a certain amount of fingers where the distance to each finger from the contact is becoming large enough to negatively impact the gate resistance. With this in mind, a guideline of 50-100 nanowires per finger and not much more than 10 fingers per transistor is established.

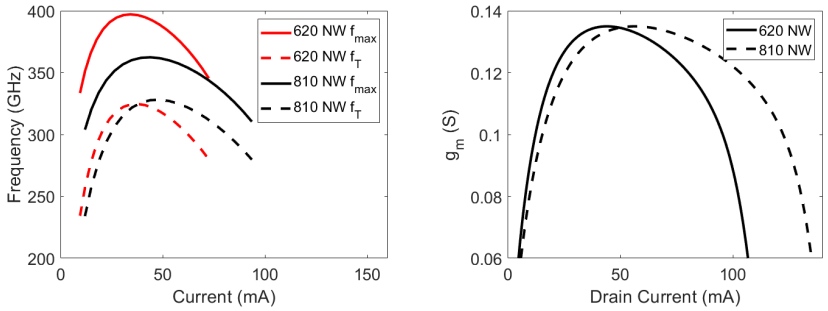


Figure 2.5: f_{max}, f_T and g_m for two transistors with 10 fingers, and 620 wires with $V_{ds} = 0.81$ V and 810 wires with $V_{ds} = 0.75$ V respectively.

2.1.1 Breakdown voltage

In order to properly determine the V_{bd} for the transistor it is necessary to account for both the biasing and the time-varying signal. As the time-varying signal is of a high frequency order, the peak voltage value is not instantly breaking the device, this makes the RMS value a better indication of the breaking point. Assuming that the bias voltage is a constant function $v_1(t) = K$, where K is a constant, and that the time-varying signal is a sinusoidal function $v_2(t) = Asin(\omega t)$, where $\omega = 2\pi/T$, the total V_{rms} can be expressed as

$$V_{rms}^2 = \frac{1}{T}\int_0^T (v_1 + v_2)^2 dt = \frac{1}{T}\int_0^T (2v_1v_2 + v_1^2 + v_2^2)dt. \tag{2.1}$$

Since the integral over a period of the term $2v_1v_2$ is equal to zero the functions are orthogonal to each other and the V_{rms} can be described as[12]

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T (v_1^2 + v_2^2)dt} = \sqrt{V_{1,rms}^2 + V_{2,rms}^2}. \tag{2.2}$$

2.2 Power amplifiers

The PA is to be used as the final stage before the antenna in a mmWave transmitter and it should have a large output power, high efficiency and a high gain to not

put hard requirements on the mixer and the PA drivers. By having a large output power the distance to which the signal may be transmitted before it is undetectable increases. In order to drive the large output power, several factors have to be taken into consideration and some significant figures of merit will in the following sections be introduced and explained further.

2.2.1 Output power and linearity

To achieve a large output power it is necessary to drive a large current, as well as to have a large voltage, this will allow for larger swings and with it a higher power compression point. However, the V_{bd} sets the maximum voltage across the drain and source which the device can handle before it breaks. Naturally this establishes a limit to the voltage swing and with that also the current swing.

Another important aspect for the modulation of the signal is the linearity of the device. If the input signal is large enough to cause either the voltage or current swing to reach its maximum or minimum value the amplifier compresses. The 1 dB compression point (P_{1dB}) is defined as the point when the output power has deviated 1 dB from its linear behaviour as shown in Figure 2.6, and it is an important figure of merit when comparing different PAs.

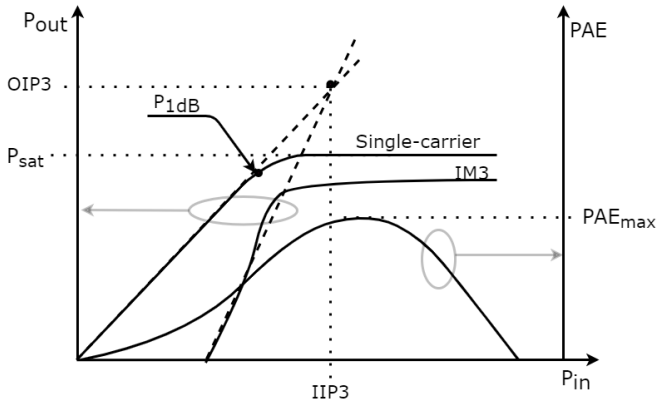


Figure 2.6: Power transfer characteristics of a PA. P_{1dB} indicates when the single-carrier signal has been compressed by 1dB. OIP3 is the point where the extrapolated power of the single-carrier and third order intermodulation products are equal.

Harmonic distortion

When a continuous wave input signal $v_i = Acos(\omega t)$ is supplied into a non-linear device, several harmonic signals will be produced. This effect may be understood by examining the input to output voltage relationship through a Volterra series [13]

$$v_o = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 ... a_n v_i^n \tag{2.3}$$

where a_n are constants and n goes towards infinity, the accuracy of the approximation increases for higher orders of n. By inserting the signal $v_i = A_1 cos(\omega_1 t)$ and solving for the output it is seen that there will be signals at the frequencies $k * \omega$, where k is an integer. Since gain diminishes with higher frequencies, the harmonic distortion becomes increasingly small for PAs operating in the D-band, especially if the f_{max} is in the range of 300-400 GHz. Even though these higher order harmonics are of a small magnitude it is a good idea to increase the linearity by removing them with a resonant circuit at the output.

Intermodulation distortion

By inserting a two-tone signal $v_i = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)$, with frequencies in close proximity to each other, which is the case with modulated signals, in (2.3). Solving the equation, shows that there are intermodulation (IM) products which appear at other frequencies than the harmonics of the fundamentals. For the PA the even order IM products are not of relevance as they will be outside of the frequency range. The uneven order IM products does however have an effect, as seen in Figure 2.7, some are close in frequency. The third-order products $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are the most relevant ones as higher order distortions have a decreasing magnitude [13]. These third order products have a 3:1 input-output slope compared to the fundamentals, and thus appear much smaller for low input powers, but as the input power increases they do reach a significant distortion level, see Figure 2.6. The OIP_3 is the intersection between the linear slopes of the fundamental single carrier signal and the IM_3, as was shown in Figure 2.6. The OIP_3 can be a good value to compare the performance of PAs, where a higher value indicates a better linearity.

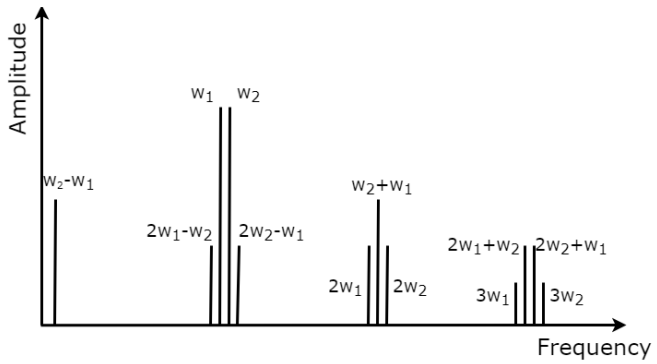


Figure 2.7: Schematic of first, second and third order harmonics and intermodulation products over frequency.

2.2.2 Power added efficiency

Since the PA is designed to deliver a large output power it is known to be a large consumer of power, and with that one of the most restricted amplifiers in terms of efficiency. The power added efficiency relates the gain of the PA with its efficiency

through the equation

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}\left(1 - \frac{1}{G}\right), \tag{2.4}$$

where P_{out} is the power delivered to the load, P_{in} is the power delivered by the source, P_{DC} is the dissipated DC power and G is the gain. PAE is a common benchmarking parameter of PAs. Through analysis of the equation with a graph as shown in Figure 2.8 it is clear that increasing the gain from for example, 15 to 20 dB, does not imply a significant increase in PAE. Rather the importance lies in having a high output power compared to the dissipated DC power.

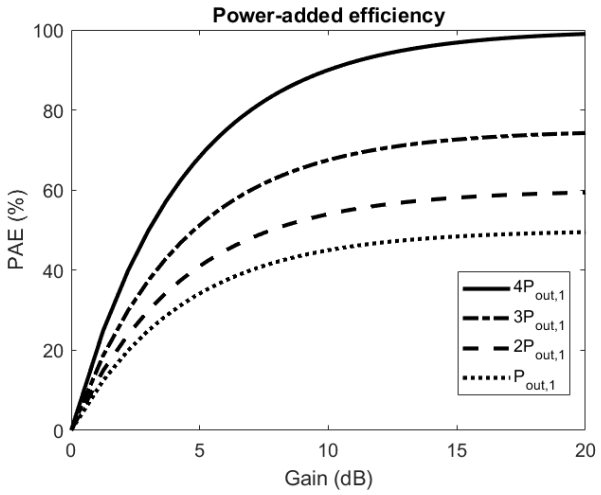


Figure 2.8: PAE as a function of gain with a varying output power and constant dissipated DC power.

2.2.3 Design specifications

At the moment there is not much information regarding 6G standardisation and it is likely to be finished around 2030[14]. Therefore, the 5G specifications are considered for this thesis. The application of the PA sets the requirement in its output power. Estimations from [15], regarding small cell base stations and back-haul applications, approximates the effective isotropic radiatiated power(EIRP) to be 55 and 60 dBm respectively. In [16] transceivers capable of communication at 100 Gbps at a distance over 160 m using 1024 antenna elements are studied. They show that by the use of 256 antennas a short distance transmission with a 100 Gbps data rate is possible. By assuming an equivalent antenna design as [16], phased array antennas with a gain of 5.1 dBi, the required power delivered from each PA for a small cell base station may be calculated as [15]

$$P = EIRP - 20log_{10}(N_{ant}) - G_{ant} + L, \tag{2.5}$$

where N is the amount of antennas and L is the PA to antenna loss. Using the estimated 55 dBm EIRP, 256 antennas, and approximating a loss of 3 dB due to

the high frequency of operation [15], the power delivered per PA should be at least $P = 4.7$ dBm.

Modulation and error in communication

Quadrature amplitude modulation (QAM) is a type of modulation which uses two signals, the in-phase (I) signal and the quadrature (Q) signal. By combining these two signals, a modulation in phase and amplitude is possible in order to represent a set of bits in each radio symbol of the transmitted signal. For example the 16 QAM scheme allows one signal to represent 4 bits of data while 256 QAM can transmit up to 8 bits of data per radio symbol. By using a higher modulation, the data rate can be increased without affecting the bandwidth of the signal, giving a more dense data package. Bandwidth, modulation and data rate can be expressed using Nyquist formula [17]

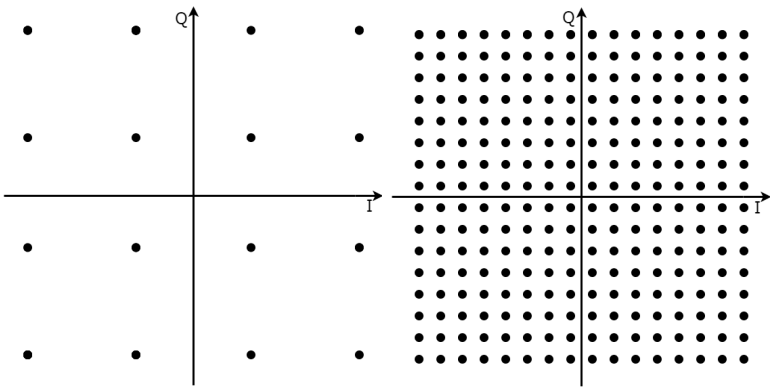
$$C = 2 * BW * Log_2(M) \tag{2.6}$$

where C is the data rate, BW is the bandwidth and M is the modulation order. Nyquists formula shows that there are several ways to achieve a 100 Gbps data rate. By either using a 256 QAM scheme with a bandwidth of 6.25 GHz, or with 64 QAM scheme and a bandwidth of 8.33 GHz. Recommendations from the European communications committee (ECC) indicate that only parts of the D-band will be available for fixed service systems[18]. These sections are between 130-134 GHz, 141-148.5 GHz, 151.5-164 GHz and 167-174.8 GHz. This implies that to achieve a 100 Gbps data rate there are three available sections for 256 QAM and one for 64 QAM.

To understand the QAM in a simple manner one can study the IQ diagrams shown in Figure 2.9, where Figure 2.9a represents 16 QAM and 2.9b represents 256 QAM. Each symbol (dot) represents a certain digital value for the bits. The exact values are not shown in the figures as different encryptions may have different values to each symbol. The importance lies rather in the fact that each symbol has an unique representation.
The higher the modulation order, the higher the demands due to the inevitable error caused by non-linearities in the PA. By establishing the error vector –the distance between the ideal reference symbol and the measured signal point, see Figure 2.10– the average error vector magnitude (EVM) in the transmission can be calculated as [19]

$$EVM_{RMS} = \frac{\frac{1}{N}\sum_{n=1}^{N}|S_n - S_{0,n}|^2}{\frac{1}{N}\sum_{n=1}^{N}|S_{0,n}|^2} = \sqrt{\frac{\frac{1}{N}\sum_{n=1}^{N}E_n E_n^*}{\frac{1}{N}\sum_{n=1}^{N}S_{0,n}S_{0,n}^*}}, \tag{2.7}$$

where S_n is the n:th measured symbol, $S_{0,n}$ is the reference ideal n:th symbol, E_n is the error of the n:th and N is the amount of unique symbols. Each modulation is normalized such that the mean square amplitude of all possible symbols is one and for simplicity the final EVM value is multiplied by 100 to give a percentage. Naturally, as the amount of symbols within the constellation increases with higher modulation, the EVM margin decreases. Table 2.1 shows the EVM requirements



(a) 16 QAM **(b)** 256 QAM

Figure 2.9: Constellation diagrams of 16 QAM and 256 QAM illustrating the difference in the amount of ideal reference symbols.

for different QAM schemes [20], [21], [22]. The 64 QAM modulation is shown for two different code rates while 16 and 256 QAM is shown for one. Code rate is the relation between useful and redundant bits in the signal. A higher code rate means that more of the signal carries useful information but puts higher demands on the EVM [23].

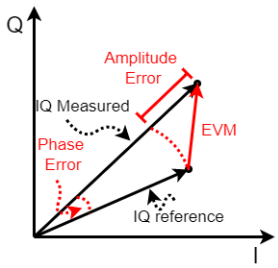


Figure 2.10: Illustration of the EVM.

Modulation	EVM (%)	Code rate
16 QAM	12.5	3/4
64 QAM	8	2/3
64 QAM	5.5	3/4
256 QAM	3.5	3/4

Table 2.1: Maximum EVM for different orders of QAM.

The PA gives rise to EVM contributions through non-linearities. These non-linearities affects both the phase and amplitude. When the amplifier approaches

compression the transmission is gradual meaning that even though the amplifier is not yet fully compressed, the amplitudes of the signals get somewhat squished. This will impact the EVM and thus the amplifier needs to be operated a certain distance below its compression. This is called backoff and the amount that is needed is dependant of the linearity of the amplifier.

Having phase noise (PN) in a system causes a spread in the signal which extends outside of the intended channel. Should this PN be large, it may disrupt the communication in channels adjacent to it. While the PA is the main contributor to the error there are also contributions from the circuit blocks prior to the PA. In order to evaluate the system performance of the PA under more realistic circumstances a suitable PN is chosen. After evaluating different technologies the specifics of [2] were selected, it details a transceiver circuit with an integrated offset synthesizer which is suitable for IQ modulated signals. It has a PN of -89 dBc/hz at 1 MHz offset from the carrier at the frequency 156 GHz and its bandwidth is 16 GHz. The phase noise profile has been approximated as shown in Figure 2.11 and was applied to the system simulations. This profile corresponds to a RMS phase jitter of 1.75°, meaning that the dots in the IQ-diagram are rotated by an average of 1.75° due to the phase noise [24].

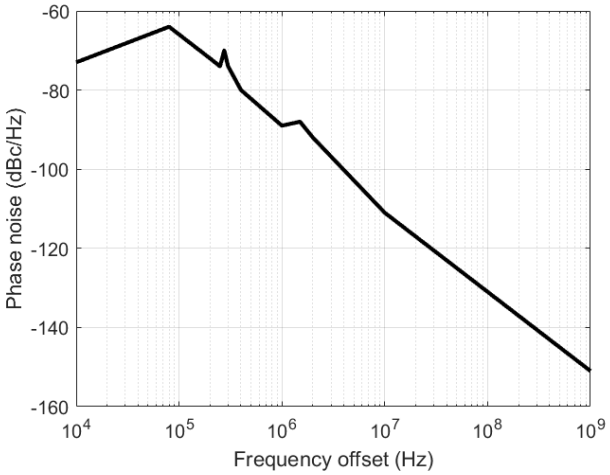


Figure 2.11: Approximated phase noise which was used in the system simulations, adopted from [2].

2.2.4 Power amplifier classes

PAs are typically divided into different classes. Traditionally they are classified depending on the drain current conduction angle α [25],[26]. If the input signal is a wave, α corresponds to the angle of the wave in which the drain current $I_d \neq 0$.

$$\frac{\alpha}{2\pi} = \frac{t}{T} \tag{2.8}$$

where T is the period of the incoming waveform and t is the time interval in which $I_d \neq 0$. Newer advancements in the field have expanded the definition but for the sake of the D-band frequencies the classes A, B and AB are optimal due to their low distortion and thus they were considered in this thesis.

Class A

Class A transistors have similarities to the small-signal amplifier with the main difference being that the proper choice of matching and DC operating point is to maximize output power rather than gain. They are defined as having $t = T \implies \alpha = 2\pi$. The conduction angle plays a key part in the biasing of the transistor. By studying the load line of the transistor under these conditions, as seen in Figure 2.12, it shows that V_{ds} should be in between the maximum and minimum voltage in order to allow a full swing, and that the input signal can not force a higher current then $\mathrm{I_{max}}$ without compression.

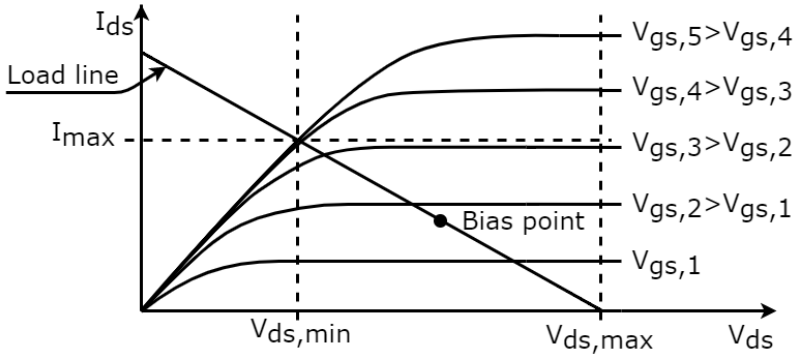


Figure 2.12: Output characteristics of a CS NMOS amplifier. The bias point indicates where the amplifier should be biased for class A operation along the load line.

Class B & AB

Class B is defined as having $t = T/2 \implies \alpha = \pi$ and class AB is an intermediate class between A & B with $\pi < \alpha < 2\pi$ which makes them both highly non-linear devices. They do have a benefit over class A amplifiers in that their maximum efficiency is higher. By having a conduction angle of less than 2π the DC power is reduced which leads to this higher efficiency. In a class A amplifier the maximum efficiency is 50 % while class B can reach around 78 %, where the efficiency is expressed as $\eta = P_{RF}/P_{DC}$. Not only does a class B amplifier have a higher maximum efficiency than class A, it has a lower efficiency decrease as backoff is performed. The downside however, is the gain which is higher for class A.

2.2.5 Load Pull

When working with power amplifiers in contrast to for example low-noise amplifiers, the small-signal parameters are not enough to determine the behavior of the

circuit. When increasing the amount of power through a transistor it will eventually reach compression. This means that the swing in either current or voltage will be larger than the transistor can handle. This is called the large-signal performance and it behaves differently than the small-signal scenario. This means that when designing matching networks for example, it is not enough to use a conjugate match or equivalent, since these are small-signal techniques. This is where the load pull technique comes in. It works by varying the load applied to the device and evaluating the influence on the performance. By doing this the optimal load impedance in terms of PAE, output power and gain can be found along with contours indicating the drop of each parameter as the match drifts from the optimal point[25],[26].

2.3 Topologies

The choice of topology has a great impact on the performance of the PA and should be chosen according to the characteristics of the transistor. As mentioned in section 2.1 the breakdown voltage is 0.9 V_{rms} for the transistors in this project. In contrast to other technologies such as the InP bipolar transistor presented in [27], where $V_{CEO,bd}$ is 4.5 V, and in the Si CMOS technology of [28], where the supply voltage is 1 V, this forces the use of topologies which are competitive with a reduced voltage swing over each transistor. With this requirement in mind the single-ended signal method of the stacked PA, elaborated in section 2.3.3, and the differential signal method of the Pseudo-Differential Common Source (PDCS), shown in section 2.3.2, holds great promise.

2.3.1 Common source

Assuming an ideal class A Common Source (CS) amplifier – as shown in Figure 2.13 – with an input signal below compression levels the output signal will mirror the input wave frequency with an increased amplitude. Given that the amplifier is at its optimum biasing point, the output waves will swing between $V_{ds,min}$ and $V_{ds,max}$ in voltage and between 0 and I_{max} in current as shown in Figure 2.12. In order to allow a maximum transfer of power between the amplifier and the load the optimum impedance of the load is

$$Z_{opt} = \frac{V_{DD}}{(I_{max}/2)}, \tag{2.9}$$

as an imbalance causes either the voltage swing to be high and the current swing to be low, or vice versa depending on if the impedance is large or small. One should note that this assumes a highly linear amplifier and as such the waveform has not been distorted by for example intermodulation or harmonic contents. With these effects in mind, the swings may very well go below or above the ideal values. Nonetheless it is important to keep in mind the effects of the load impedance if one chooses to design with the help of a power combiner/divider as is further elaborated in section 2.4.

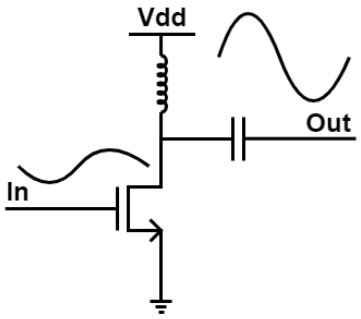


Figure 2.13: Class A biased CS NMOS amplifier with incoming and outgoing signal.

2.3.2 Pseudo-differential CS NMOS

The idea of a differential input mode is that by dividing the input signal into two signals with opposite phases, each wing of the amplifier acts on half of the input. Therefore the voltage swing in each transistor will be smaller, hindering it from reaching the breakdown point. At the output, the signals are then added together to achieve a larger voltage swing than for the single ended amplifier. If the voltage swing in each wing behaves as the swing for the CS amplifier the total output swing would instead go from $V_{ds,min}$ to $2\mathrm{V}_{\mathrm{ds,max}}$ which leads to a larger possible voltage swing, and as such a larger possible power swing.

What separates the PDCS amplifier as seen in Figure 2.14 from the fully differential amplifier is that it does not use a tail current source. This further increases the voltage swing as the tail source – which often consists of a transistor – requires a minimum drain source voltage in order to supply a constant current to the circuit.

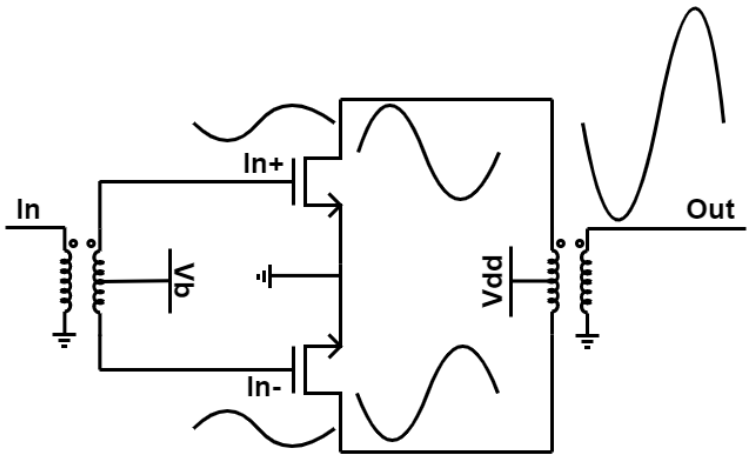


Figure 2.14: PDCS NMOS amplifier with transformer output input illustrating how the signal is amplified.

The downside to not having the tail current source is the common-mode (CM) rejection ratio (CMRR), which suffers significantly[29]. This effect is shown by studying a simplified small-signal model of a PDCS amplifier with a load as shown in Figure 2.15.

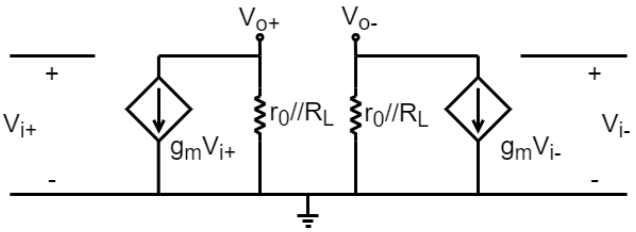


Figure 2.15: Simplified small-signal schematic of a PDCS amplifier.

The input signal can be divided and expressed as

$$V_{i+} = \frac{V_{id} + V_{ic}}{2} \quad , \quad V_{i-} = -\frac{V_{id} + V_{ic}}{2} \tag{2.10}$$

and solving the differential-mode (DM) system gives that

$$V_{od} = \frac{V_{id}(-g_m(r_0//R_L)}{2} - \frac{-V_{id}(-g_m(r_0//R_L)}{2} \implies \tag{2.11}$$

$$A_d = \frac{V_{od}}{V_{id}} = -g_m(r_0//R_L). \tag{2.12}$$

Where V_{od} is the differential output voltage and A_d is the differential voltage gain. As both sides are equal in CM it is only necessary to study one side of the amplifier. Each side is a standard CS stage resulting in a CM gain of $A_c = -g_m r_0//R_L$ and as such the CMRR is

$$CMRR = \frac{A_d}{A_c} = 1. \tag{2.13}$$

A high CMRR is desired for an amplifier in order to filter out any undesired signals which are applied equally to both sides [29]. However, the use of a transformer on the output nodes causes the CM signal to cancel itself and hence they are not transmitted through it.

In order to increase the gain and the reverse isolation a cross-coupled neutralization capacitor C_n is used. C_n is placed between the drain of the transistor on one side of the amplifier and the gate of the other, as shown in Figure 2.16a. Because of the opposing phase of the DM signal C_n counteracts the negative feedback-loop effect of the parasitic capacitance between the drain and the gate C_{gd}. Its effect is best seen by studying the small-signal Y-parameters of the amplifier in DM, seen

in Figure 2.16b, as[30]

$$Y_{11} = \frac{1}{R_G} + j\omega C_{gs} + j\omega(C_{gd} + C_n), \tag{2.14}$$

$$Y_{12} = -j\omega(C_{gd} - C_n), \tag{2.15}$$

$$Y_{21} = g_m - j\omega(C_{gd} - C_n), \tag{2.16}$$

$$Y_{22} = \frac{1}{r_0} + j\omega C_{db} + j\omega(C_{gd} + C_n). \tag{2.17}$$

To increase the gain and reverse isolation the relationship between C_{gd} and C_n should be balanced such that the term in (2.15) and (2.16) become increasingly small, while keeping the terms in (2.14) and (2.17) under control to ensure stability. However, while C_n counteracts C_{gd} and increases the stability for DM it will add to the effect of C_n in the CM, potentially causing an instability[31]. Should the PA be unstable in CM it should be handled without affecting the DM operation. This can be achieved by adding a resistor between Vb and the transformer in figure 2.16a. The resistor shifts the unstable pole from the right-hand to the left-hand plane[32].

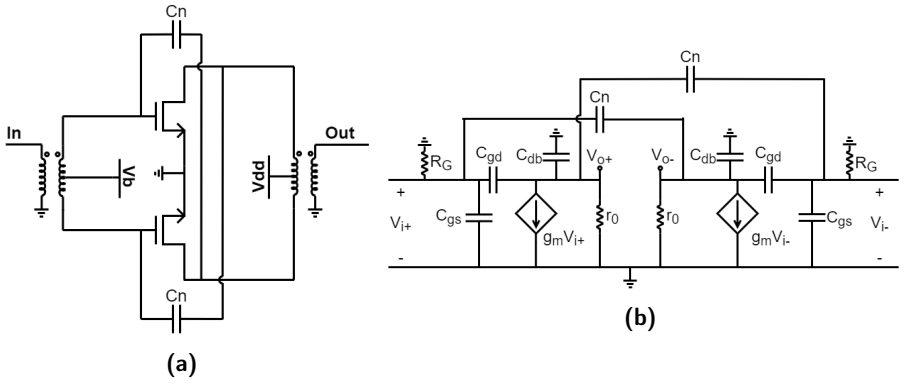


Figure 2.16: Schematic of a PDCS PA with two cross-coupled neutralization capacitors and its small-signal model in DM.

2.3.3 Stacked

The stacked PA topology is a modification to the classic cascode topology, a common source transistor followed by a common gate. The difference being that the common gate transistor has a capacitor on its gate which is small enough to not be a signal ground[33]. The added capacitor together with the parasitic gate-source capacitance make up a voltage divider that controls the gate voltage. This will enable the gate voltage of the common gate transistor to swing, thus reducing the gate-drain and drain-source voltage swings of each transistor in the stack, which is very valuable given the low breakdown voltage of the transistors. The goal is then to make the stacked transistors drain voltages swing in phase. At lower frequencies where $f_0 << f_T$ this is done by choosing an appropriate value on the

gate capacitance, but at higher frequencies an interstage matching also needs to be implemented. This will make the output node swing with the sum of these waves and thus increasing the overall voltage swing of the amplifier, see Figure 2.17. By utilizing this the overall voltage swing from the amplifier can be held high while keeping the relative swing on each transistor below the breakdown voltage.

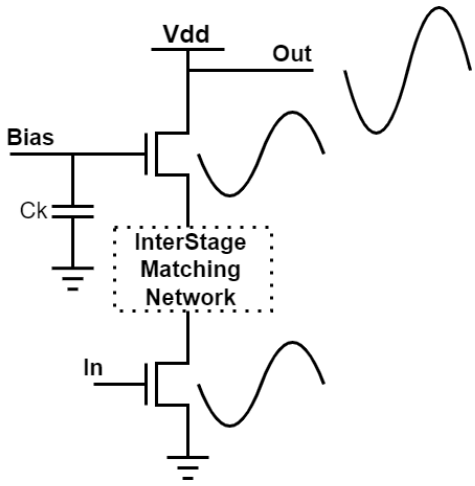


Figure 2.17: Stacked PA, highlighting the amplification due to the phase matched voltage swings.

Another advantage with the stacked topology is that the optimum load impedance for each transistor in the stack increases linearly, meaning that the k:th transistor wants to see $\mathrm{k} * R_{\mathrm{opt}}$. This is good since a large transistor, which is needed to get a large output power, has a very low R_{opt} which would complicate the matching to the 50Ω antenna. By using a simplified small-signal model only consisting of the parasitic capacitances and the impedance seen at the contacts, see Figure 2.18, the load seen by transistor $Z_{\mathrm{k}-1}$ is expressed as[34]

$$Z_{d,k-1} = \frac{C_{\mathrm{gs},k} + C_k + C_{\mathrm{gd},k}(1 + g_{m,k} Z_{d,k})}{(g_{m,k} + sC_{\mathrm{gs},k})(C_{\mathrm{gd},k} + C_k)} \tag{2.18}$$

By setting the real part of equation (2.18) to $\mathrm{k} - 1 * R_{\mathrm{opt}}$ and solving for C_{k} one finds

$$C_k = \frac{C_{\mathrm{gs},k} + C_{\mathrm{gd},k}(1 + g_{m,k} R_{\mathrm{opt}})}{(k-1) g_{m,k} R_{\mathrm{opt}} - 1}, \qquad k = 2, 3, \ldots, K. \tag{2.19}$$

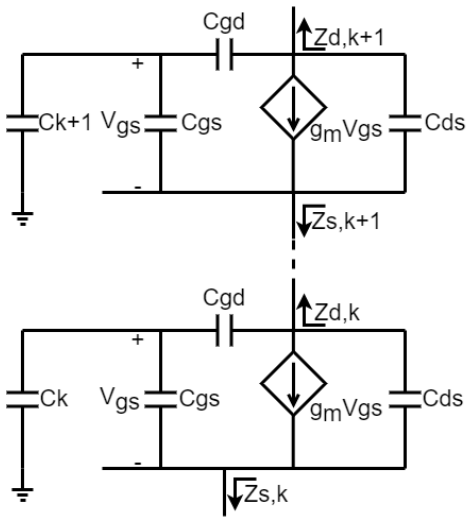


Figure 2.18: Small-signal model used in analysis of the stacked PA.

When implementing this capacitor, the imaginary part of (2.18) is disregarded but in reality this gives rise to an unwanted reactance which will interfere with the phase alignment of the drain voltages. This is where the interstage matching network comes in to play. There are generally three different ways to combat this problem, a shunt inductance, a shunt capacitor or a series inductance, see Figure 2.19. These methods are discussed in detail in [35]. The shunt capacitor increases the effective C_{ds} which puts higher demands on the output matching networks. The series inductance will scale $\mathrm{R_{opt}}$ and thus C_k further complicating the structure. They also introduce a problem thanks to the low-Q factor inductors available in the process used. This will affect the biasing and create further issues along the way. The shunt inductance is best equipped for the process and will be used in this design. [36]

The sizing of the inductance adjusts the imaginary part of (2.18) to match the optimal value. As shown in [35] sizing the inductance according to

$$\begin{aligned}\frac{1}{L_k} = \omega^2 \frac{(C_{\mathrm{ds},k} - C_{\mathrm{ds},k+1})}{k} + \frac{\omega^2 C_{\mathrm{gs},k+1}}{k g_{m,k+1} R_{\mathrm{opt}}} \\ +\omega^2 \frac{C_{\mathrm{gd},k}}{k}, \qquad k = 1, 2, \ldots, K-1.\end{aligned} \tag{2.20}$$

will ensure a proper phase alignment. Its based on the same small-signal model, shown in Figure 2.18, as (2.19).

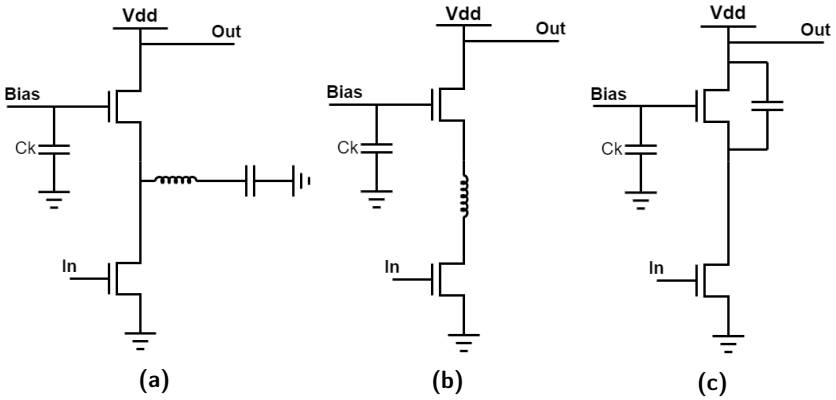


Figure 2.19: Illustration of the different interstage matching techniques available. (a) shunt inductance, (b) series inductance, (c) shunt capacitance.

2.4 Power divider & combiner

Another commonly used method of increasing the output power is a so called power divider & combiner network where several sets of stages are connected either in parallel or series. Two examples, one series and one parallel combiner using transformers, are shown in Figure 2.20. There are several methods of dividing / combining, three of which will be covered here, the parallel and series transformers as well as the Wilkinson method, which due to not being used in this thesis is explained in Appendix A. It is important to notice that while it is possible to have parallel divider and series combiner it introduces a mismatch between the signals which must be accounted for.

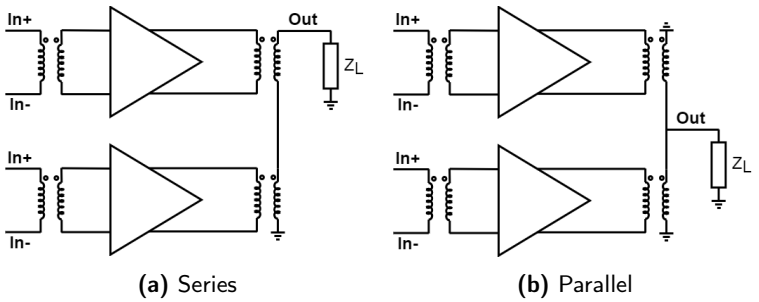


Figure 2.20: Series and parallel combination of two branches using transformers at the output stage of two power amplifiers.

2.4.1 Series transformer

To better understand the benefit of using a series transformer network it is helpful to study how the output of the previous amplifier stage is impacted by it [37].

Figure 2.21 shows a combiner network with k amount of branches. If all branches prior to the combiner are identical and the transformers are assumed to be ideal the currents $I_1 = I_2 = ... = I_k$, the voltages $V_1 = V_2 = ... = V_k$ and the parasitic resistances $R_1 - R_k$ are equal. The current relation can then be given as

$$\frac{I_o}{I_k} = \frac{N_k}{N_o} \implies I_k = \frac{I_o}{N_k/N_o} \tag{2.21}$$

where I_o is the same in all transformer output windings due to the series connection. A similar expression can be made for the voltage

$$\frac{V_k}{V_{o,k}} = \frac{N_k}{N_o} \implies V_k = \frac{N_k V_{o,k}}{N_o} \tag{2.22}$$

and as V_{ok} is the voltage division over the transformer k the expression can be expanded to

$$V_k = \frac{N_k}{N_o} \frac{I_o(R_{p,o} + Z_L)}{k} \tag{2.23}$$

It is shown that the necessary voltage across each branch in order to produce a certain current in the output node is decreasing with an increase in k and as such it could be of use when operating with a low supply voltage. This can also be expressed in terms of input power for each branch

$$P_{in} = \frac{V_{in}^2}{Z_{in}} = \frac{V_{in}^2}{R_{p,k} + \frac{1}{k}\left(\frac{N_k}{N_o}\right)^2 (R_{o,k} + Z_L)} \tag{2.24}$$

where Z_{in} is the input impedance consisting of both the parasitic resistance and the transformed load impedance. The input power of each branch increases as the number of branches increases. This is a great result as it shows that by using a series combiner it is possible to achieve the same amount of current with a smaller voltage. Therefore, it is a suitable candidate for devices with a low breakdown voltage. To see how the branches combine their power it is convenient to define the power-combining ratio (PCR) as [37]:

$$PCR_{Series} = \frac{P_L}{P_{in}} = \frac{V_L I_o}{V_{in} I_k} = \frac{I_o^2 Z_L}{I_k^2 Z_{in}} = \frac{I_o^2 Z_L \left(\frac{N_k}{N_o}\right)^2}{I_o^2 Z_{in}} \implies$$

$$PCR_{Series} = \frac{Z_L \left(\frac{N_k}{N_o}\right)^2}{R_{p,k} + \frac{1}{k}\left(\frac{N_k}{N_o}\right)^2 (R_{o,k} + Z_L)}. \tag{2.25}$$

While it may be desirable from the perspective of input power to increase N_o, the turns of each branch on the output side, the PCR shows that by doing so the efficiency of the combiner decreases. Instead it is desirable to keep the turns ratio close to unity while increasing the amount of branches.

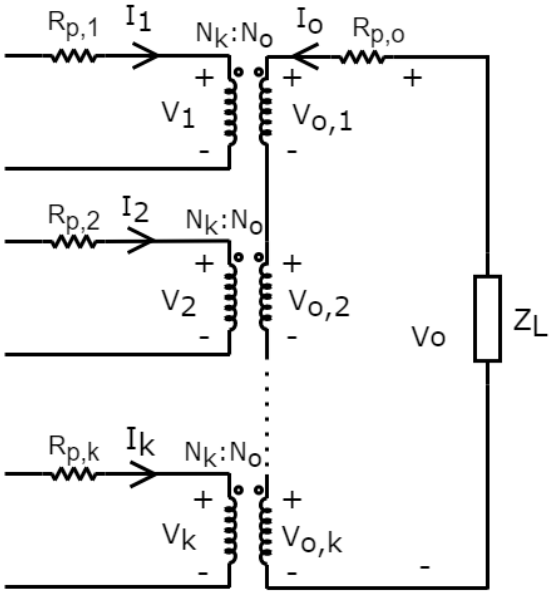


Figure 2.21: Series transformer combiner network with a load impedance.

2.4.2 Parallel transformer

The parallel transformer combiner is shown in Figure 2.22[37]. With the same reasoning as was made for the series transformer combiner that each incoming branch and parasitic line resistances are identical the current from each branch contributes equally to the total output current such that $I_o = \sum_{i=1}^{k} I_{o,i} = kI_{o,k}$.

By rearranging the current relation for one transformer and expanding it to see the effect of one branch on the total current the relation is described as

$$I_{o,k} = I_k \frac{N_k}{N_o} \implies I_o = \sum_{i=1}^{k} I_i \frac{N_k}{N_o} = kI_k \frac{N_k}{N_o} \tag{2.26}$$

and the relationship between the voltage can be described as

$$\frac{V_k}{V_o} = \frac{N_o}{N_k} \implies V_k = I_o(R_{p,o} + Z_L)\frac{N_o}{N_k}. \tag{2.27}$$

Again by transforming the impedance of the output side the input impedance can be used to examine the input power of each branch

$$P_{in} = \frac{V_{in}^2}{Z_{in}} = \frac{V_{in}^2}{R_{p,k} + k\left(\frac{N_o}{N_k}\right)^2 (R_{p,o} + Z_L)}. \tag{2.28}$$

Comparing this to the case of the series combiner in equation (2.24) the parallel combiner with its increasing impedance instead reduces the input power to each

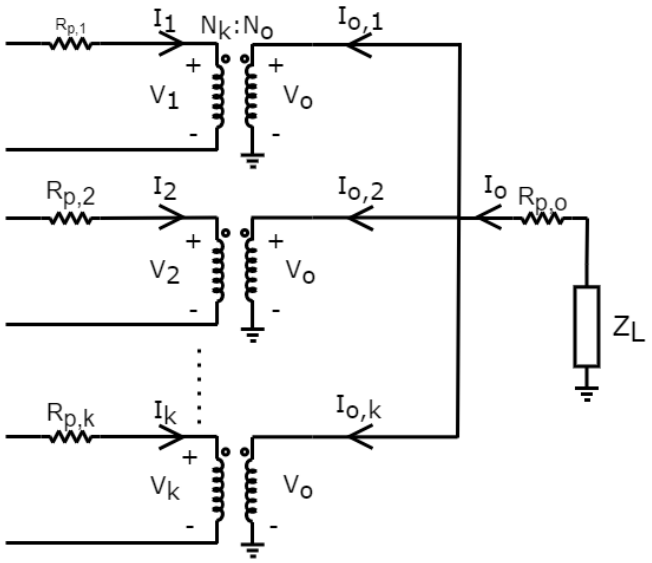


Figure 2.22: Parallel transformer combiner network with a load impedance.

branch. The positive effect can be seen by studying the PCR

$$PCR_{Parallel} = \frac{P_L}{P_{In}} = \frac{I_o V_L}{I_k V_{in}} = \frac{k^2 I_o^2 Z_L \left(\frac{N_k}{N_o}\right)^2}{I_o^2 Z_{in}} \implies$$

$$PCR_{Parallel} = \frac{k^2 Z_L \left(\frac{N_k}{N_o}\right)^2}{R_{p,k} + k\left(\frac{N_o}{N_k}\right)^2 (R_{p,o} + Z_L)} \tag{2.29}$$

By increasing the amount of branches the impact from the parasitic resistance decreases and therefore a device with high parasitics may benefit more in using this combiner. For the series combiner a larger amount of branches increases the distance enough to create a significant phase shift between the first and last branch of the PA. This effect can through clever layout design be minimized with a parallel combiner.

Chapter 3

Project Designs

3.1 Pseudo-differential CS

The final PDCS design in this project is seen in Figure 3.1. It consists of one output stage (OS) and three driver stages (DS). While the OS requires large transistors to achieve a large output power, the DS are smaller to not consume a lot of DC-power and aim to provide a substantial gain. C_n were balanced in each stage to match the value of the parasitic C_{gd} to increase the gain and reverse isolation in DM as was seen in equation (2.16) and (2.15). The resistors R_b were then set to a value which ensures CM stability, as well as being within reasonable dimensions for the process.

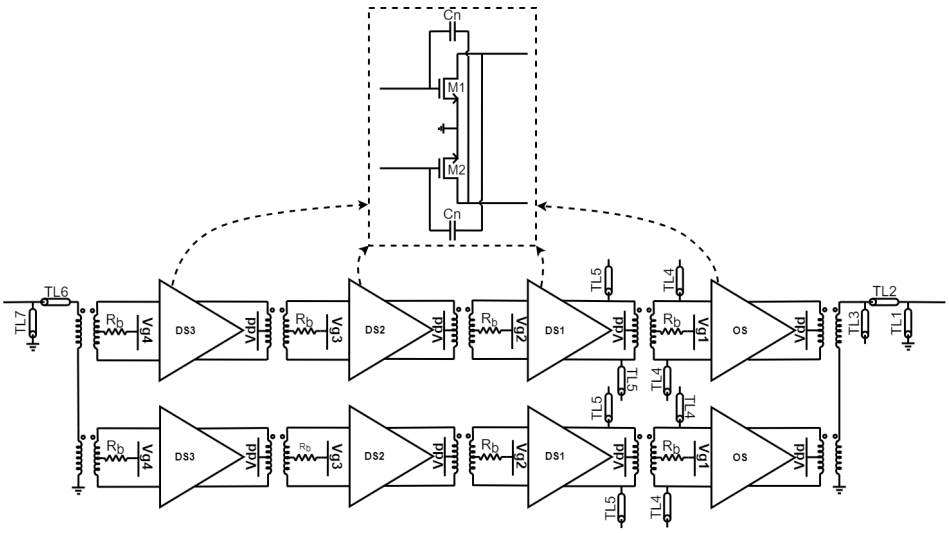


Figure 3.1: Schematic of the final design of the PDCS PA

When designing the stages an important factor is the resonance between the transistors and the nearby transformers. As the dimensions of the transistor increase so does the internal parasitic capacitances, and to accommodate for this the inductance of the transformers needs to maintain the resonance at the desired frequency

as

$$2\pi f_0 = \omega_0 = \frac{1}{\sqrt{LC}}.$$

However, the process has a minimum recommended inductance size of the transformers at an inductance of 40pH. Hence increasing the dimension of the transistors beyond this limit will cause a resonance at a lower frequency than is desired. This effect is compensated for by having the driver stages resonate at higher frequencies, effectively creating a wide-band amplifier. The transformers are an effective tool to transfer power for several reasons. Firstly, at the input of the PA the use of a balancing unit (balun), achieved by grounding one side of the transformer, transforms the single-ended signal to a differential signal. At the output the balun transforms the differential signal back to a single-ended signal. Secondly, they provide a DC isolation between first and secondary winding. Thirdly, the CM signals cancel each other at the transformers and are not transmitted to the next stage. The transformer model is provided to us by NordAmps and detailed in appendix B.

The combiner/divider network is chosen as a series transformer combiner/divider as it provides a lower input impedance than the parallel combiner, resulting in an increase in the output power. The amount of branches is determined by studying the loss of back to back transformers. By adjusting the capacitor shown in Figure 3.2a between the back to back transformers the resonance is set to 150 GHz. The total loss then varies as seen in Figure 3.2b when the amount of branches increase. Note that the loss caused by one row of transformers is then half of the total loss shown in the figure.

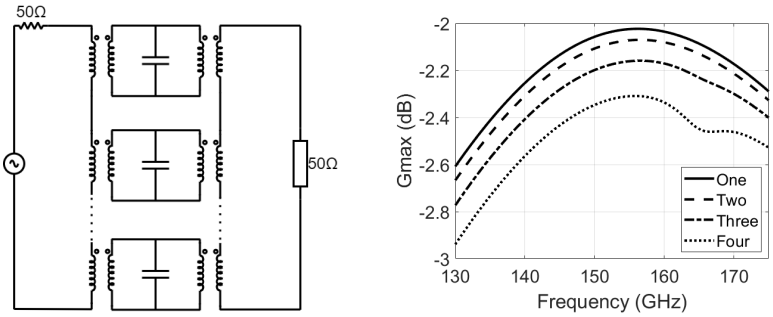


Figure 3.2: Back to back transformers and the total loss as the amount of branches increases.

As can be seen the loss for increasing the branches are worse as the amount of branches increase. A doubling of the amount of branches would correspond to increasing the dissipated DC power by a factor 2, but because of losses the output power will not increase as much. This causes a declining effect in the PAE when the amount of branches increase. With this in mind, the amount of branches chosen were two.

3.1.1 Matching networks

With the careful design of each stage and the transformers between them an additional interstage matching network is not necessary, it can however provide a better matching at certain stages allowing the PA to achieve better performance. Such is the case for the output of DS1 to the input of the OS, as seen in Figure 3.1. The number of wires on each transistor in the OS is large and by implementing shunt transmission lines (TLs) the power transfer was improved. The output matching network was implemented to provide a linear performance through the D-band and chosen as one series and two shunt TLs. Load-pull simulations were performed at the output to allow for an output matching network, which provides a good output power with similar magnitude across the band. Figure 3.3 shows the optimum load impedances for maximum output power around the compression point of the transistors for the entire frequency range. Pink markers show the optimum impedances, while blue markers are impedances for the implemented design. For lower input powers than the compression point, the pink markers extends outwards, effectively separating the values which is optimal for each frequency. Through several iterations this matching network was deemed the most suitable for achieving a broadband design.

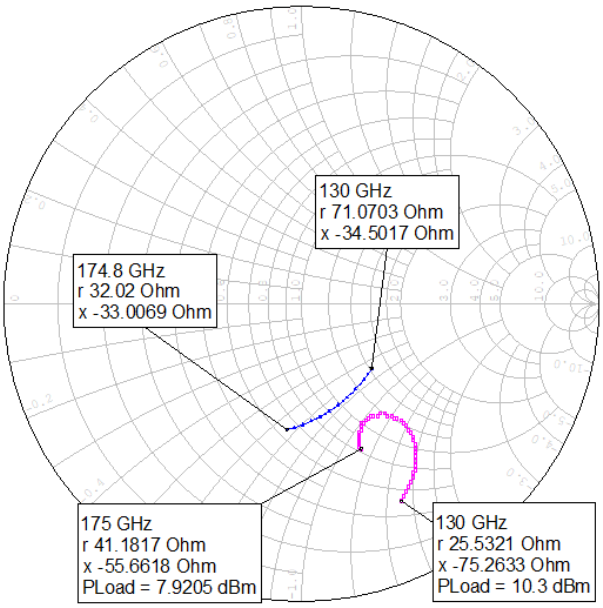


Figure 3.3: Load-pull simulations of the PDCS PA for an input power close to compression. Pink markers show the optimum load impedance for maximum output power and blue markers show the load impedance of the final design.

3.1.2 Large- & Small-signal performance

The small-signal S-parameters are shown in Figure 3.4. The PDCS PA has a maximum gain of 24.1 dB at 137.3 GHz and a 3 dB-bandwidth of 58 GHz in the range of 122 to 180 GHz. As S12 is below -55 dB across the frequency band it is omitted from the figure.

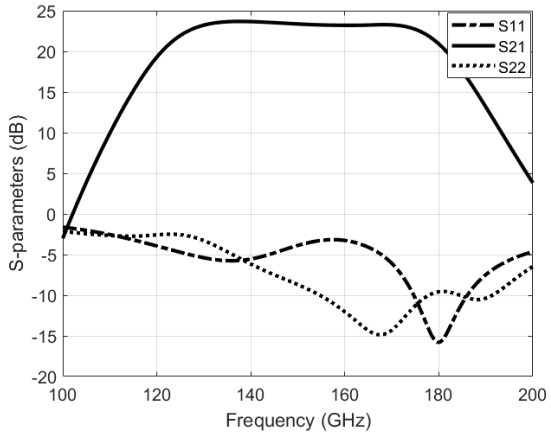


Figure 3.4: Small-signal S-parameters of the PDCS PA. S21 is less than -55 dB across the frequency range and therefore omitted.

Figure 3.5 shows how the output power at 150 GHz as well as the third order intermodulation $2w_2 - w_1$with the second tone at 151 GHz. The linear behaviour of both curves is extrapolated and the OIP_3 is shown to be at 18.4 dBm.

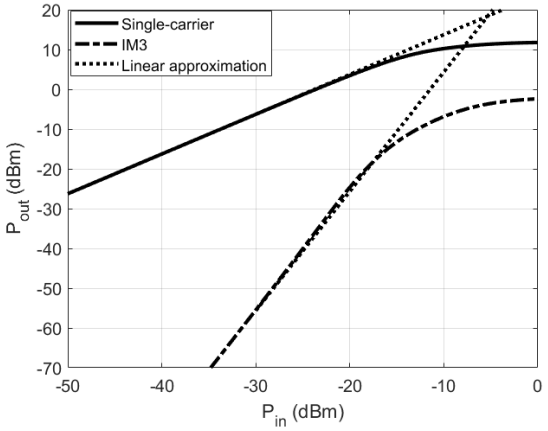


Figure 3.5: Output power of a 150 GHz single-carrier signal as well as the third-order intermodulation of a 2-tone signal of 150 and 151 GHz.

Figure 3.6 shows the PAE, P_{out} and gain of the PDCS PA at $\mathrm{P_{1dB}}$ across the frequency band. The $\mathrm{P_{sat}}$ and the $\mathrm{PAE_{max}}$ across the frequency band is seen in Figure 3.7. The PDCS PA reaches its maximum $\mathrm{P_{1dB}}$ of 8 dB and $\mathrm{PAE_{max}}$ of 9.8 % at the frequency 130 GHz. The maximum $\mathrm{P_{sat}}$ is 12.1 dBm at the frequency 136 GHz. While we see a degradation of the $\mathrm{P_{sat}}$ and $\mathrm{PAE_{max}}$ for higher frequencies the PDCS PA performance at $\mathrm{P_{1dB}}$ remains fairly constant.

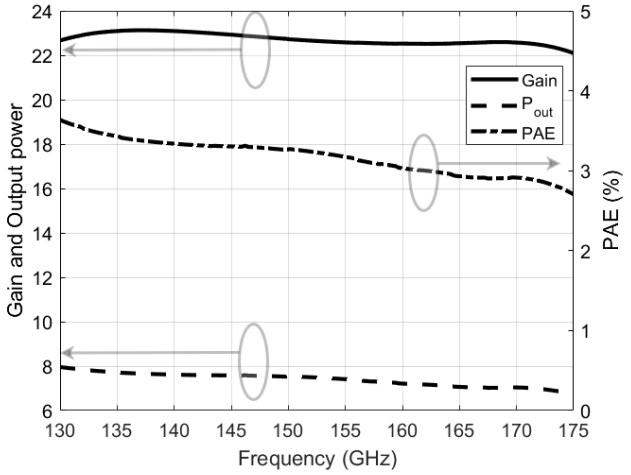


Figure 3.6: P_{out}, Gain and PAE are shown at the $\mathrm{P_{1dB}}$ for the PDCS PA.

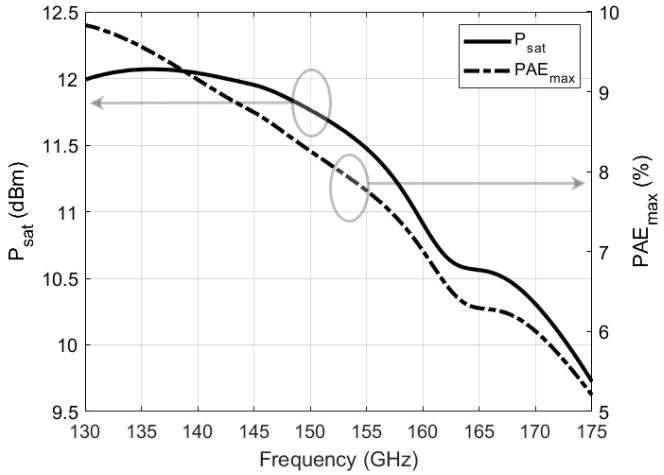
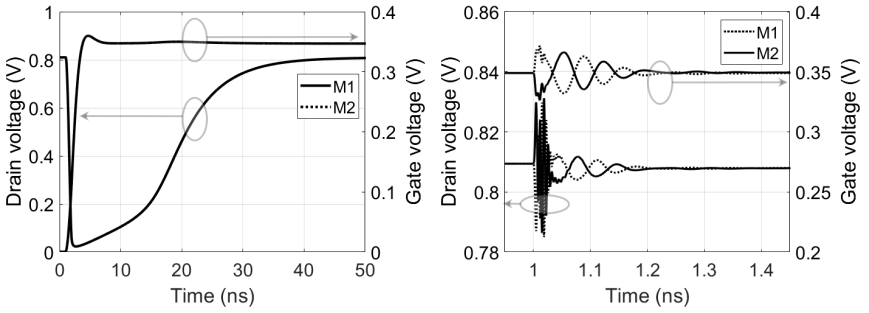


Figure 3.7: Maximum PAE and $\mathrm{P_{sat}}$ of the PDCS PA over frequency.

3.1.3 Stability

Both the common and the differential stability has been studied. The initial check was and should always be the Rollett stability factor[38], which for the PDCS PA is above 20 in the frequency range 100-200 GHz. To be certain of stability, especially for the CM case, step-signal responses has also been studied. Figure 3.8 shows the voltage response on the transistors in the OS when they are subjected to a CM and DM step signal.

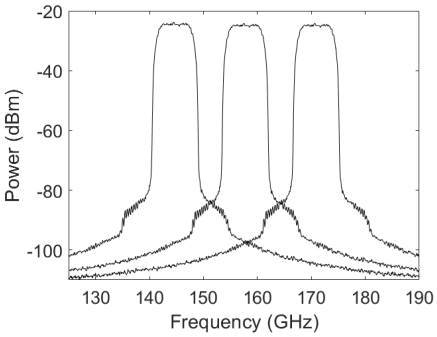


(a) CM **(b)** DM

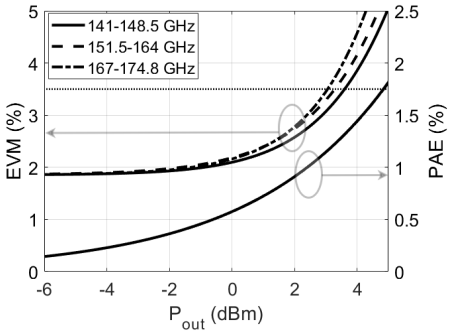
Figure 3.8: Response at the drains and gates of the transistors in the OS when a step function is applied in CM and DM.

3.1.4 System performance

There are three sections of the D-band suitable for fixed service systems with a 256 QAM signal, section 1 at 141-148.5 GHz, section 2 at 151.5-164 GHz and section 3 at 167-174.8 GHz. By adding the described noise profile, adjusting the modulation to 256 QAM and the bandwidth to achieve 100 Gbps, a spectrum simulation of the three sections were performed and seen in Figure 3.9a. The spectrum simulation is shown for a -30 dBm input signal power and it has a 3-dB bandwidth of approximately 6.25 GHz. When the input power is increasing the amplitude, the leakage to nearby channels becomes larger relative to the output power due to non-linearities. The EVM and PAE as functions of the output power of the PA are shown in Figure 3.9b. The dotted line marks the 3.5 % EVM limit of the 256 QAM, and its shown that the output power for the three sections are 3.6, 3.3 and 3.1 dBm at the input powers -19.8, -19.8 and -20 dBm respectively. The PAE curves of the sections is similar enough to not be distinguishable in the graph, their values at the EVM limits are 1.3, 1.2 and 1.2 % respectively. The PDCS PA at its maximum EVM limit does not reach the goal of 4.7 dBm output power for 256 QAM scheme.



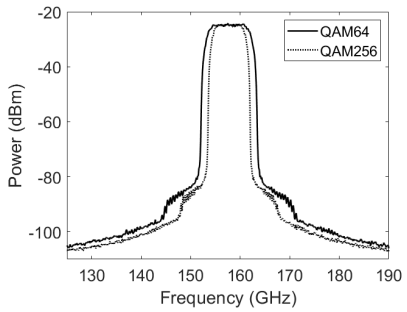
(a) Spectrum of the three signals.



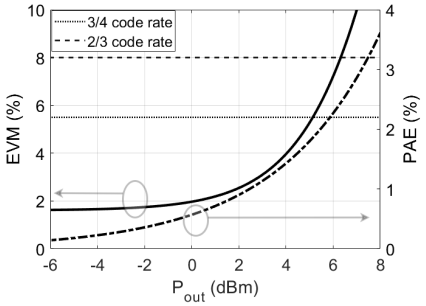
(b) EVM and PAE over output power for the signals. Dotted line marks the 3.5 % EVM limit.

Figure 3.9: Results from the simulations of the 256 QAM modulated signals for the PDCS PA with noise added.

After adjusting the signal to a 64 QAM scheme and increasing the bandwidth the spectrum is simulated in section 2 and shown in Figure 3.10b. Again the spectrum is plotted at an input power of -30 dBm but now with a 8.33 GHz 3-dB bandwidth. This operation mode allows the PA to deliver an output power of 5.1 dBm at the EVM limit of 5.5 %, as seen in Figure 3.10a. This is achieved with an input power of -17.53 dBm and the PAE is at that point 1.84 %. For the 64 QAM scheme the PDCS PA output power reaches the goal prior to the EVM limit.



(a)

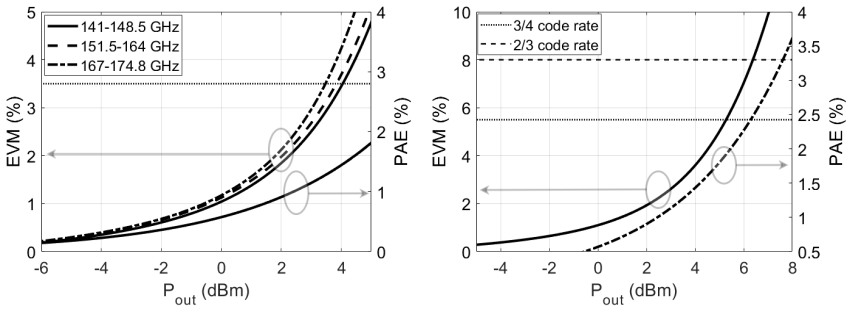


(b) Dotted line marks the 5.5 % EVM limit.

Figure 3.10: Spectrum of the 64 QAM modulated signal at the output of the PDCS PA with a -30 dBm input power and the EVM and PAE as functions of the output power.

To better understand the performance of PA and to show the impact of the added noise, EVM and PAE simulations were performed without the noise. The results are shown for 256 QAM in Figure 3.11a and 64 QAM in Figure 3.11b. As expected the PA without the added noise profile achieves a smaller minima in EVM and

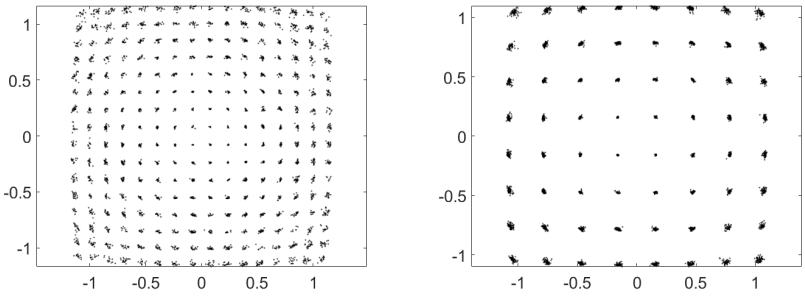
slightly improved performances at the EVM limits. The output power at the EVM limit for 256 QAM are 4, 3.8 and 3.5 dBm for section 1, 2 and 3 respectively. The respective PAEs are 1.5, 1.4 and 1.3 %. For 64 QAM the output power at EVM limit is 5.3 dBm with a PAE of 1.9 %.



(a) 256 QAM **(b)** 64 QAM

Figure 3.11: Results from the simulations of EVM and PAE with 256 QAM and 64 QAM for the PDCS PA without added noise.

The IQ-diagrams of the signals in section 2 for the 256 QAM and 64 QAM is shown with the added noise at their respective EVM limits in Figure 3.12.



(a) 256 QAM, EVM 3.5 % **(b)** 64 QAM, EVM 5.5 %

Figure 3.12: IQ diagrams for 256 QAM and 64 QAM at their respective EVM limits in the second section for the PDCS PA.

3.2 Stacked Amplifier

Design of the stacked PA follows a similar design flow as for the PDCS. First the output stage was designed so that a high output power can be achieved. As said before, in order to have a high output power there needs to be a high current which means large transistors. The problem with making the transistors larger is that both R_{opt} and the optimal input impedance becomes very small. This complicates both the input and output matching networks and tend to make them

narrowband. Therefore a compromise was made with a decent output power and manageable optimal input and output impedance. When the output stage was completed, a driver stage was designed, as explained earlier. Here the driver stage was chosen to be a scaled down version of the output stage. This is to increase the gain of the amplifier as the output stage is mostly designed for maximum output power. The final design of the stacked PA is seen in Figure 3.13.

Work was performed on using a Wilkinson combiner/divider, as presented in appendix A. This increased the output power and P_{1dB} while slightly decreasing PAE and Gain. However, it had a negative impact on the system performance reducing the amount of power delivered at maximum EVM and will therefore not be presented.

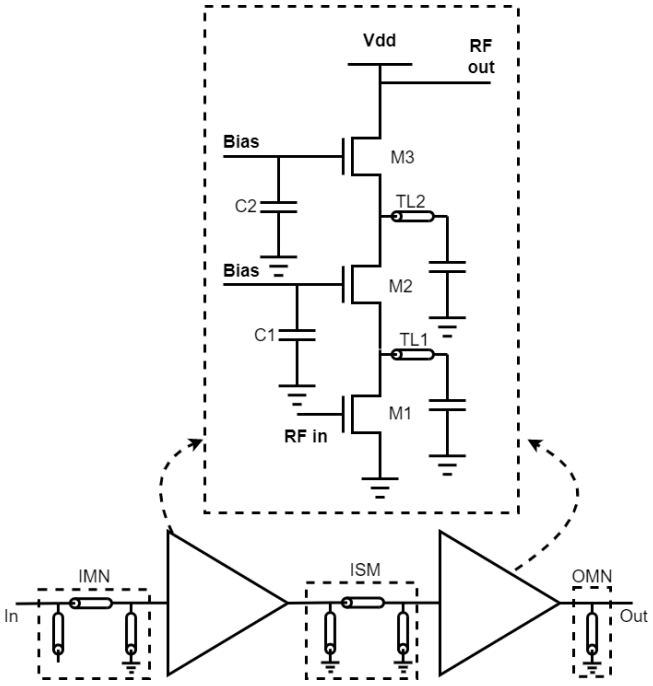


Figure 3.13: Schematic of the final design of the stacked PA.

3.2.1 Load Pull

In order to find the optimum load impedance, Z_{opt}, a load pull simulation was performed. For the output stage of the amplifier, a more rigorous load pull was done that took into account the large-signal performance of the transistors. In Figure 3.14 the resulting contours along with markers showing Z_{opt} for maximum PAE and output power is presented for the three levels of the stacked topology. The real value of Z_{opt} from the stand alone transistor, Figure 3.14a, is then used as R_{opt} when sizing the capacitors and inductors using (2.19) and (2.20).

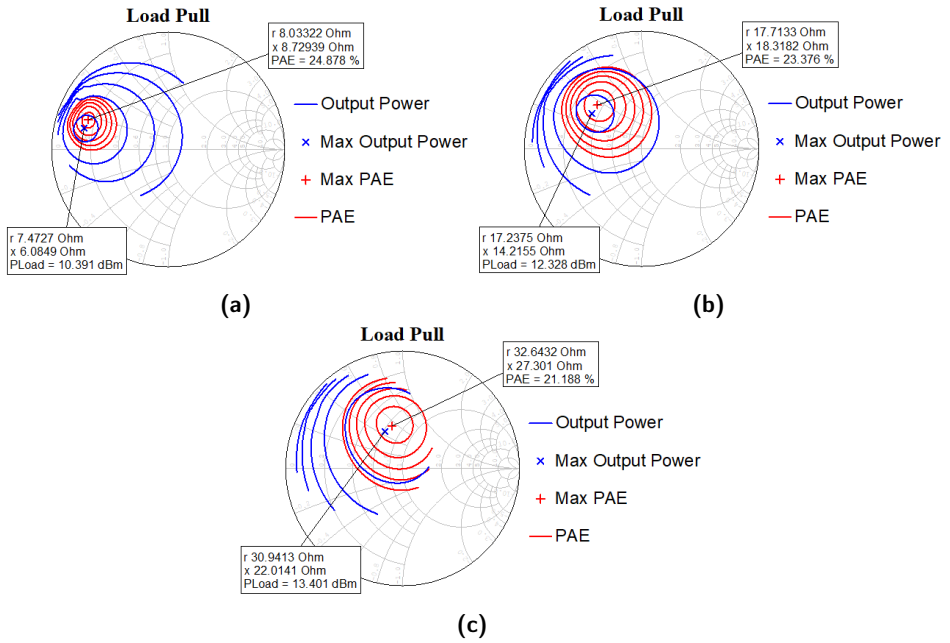


Figure 3.14: Load Pull results for (a), the single transistor, (b), 2-stacked, (c), 3-stacked showing Z_{opt} for max PAE and output power for 4 different input powers along with a marker for the best result, 7 dBm input power. The contours show a decrease of 2 dBm/% respectively for an input power of 7 dbm.

3.2.2 Internal matching and phase shift optimization

After sizing the capacitance and inductance according to theory, using R_{opt} from the load pull simulations, the phase of the drain voltages were examined, see Figure 3.15a. The match was decent but not optimal. This is due to the fact that equation (2.19) and (2.20) are estimates based on a simple small-signal model that does not fully represent the transistors used. To better match to the optimum found by the load pull simulations the phases aligned more properly, see Figure 3.15c. This was performed by tuning the capacitances and inductances between each stage in order to adjust the impedance seen by each drain. Here the impact of the internal matching inductance is also examined, see Figure 3.15b. The importance of the inductance is quite clear and without it the stacked topology would not work at these frequencies. It is also shown that the amplitude of the signals on each transistor is more even in Figure 3.15c than in the calculated case. This again points to the fact that the equations used originate from a simplification that is not a good approximation for this technology.

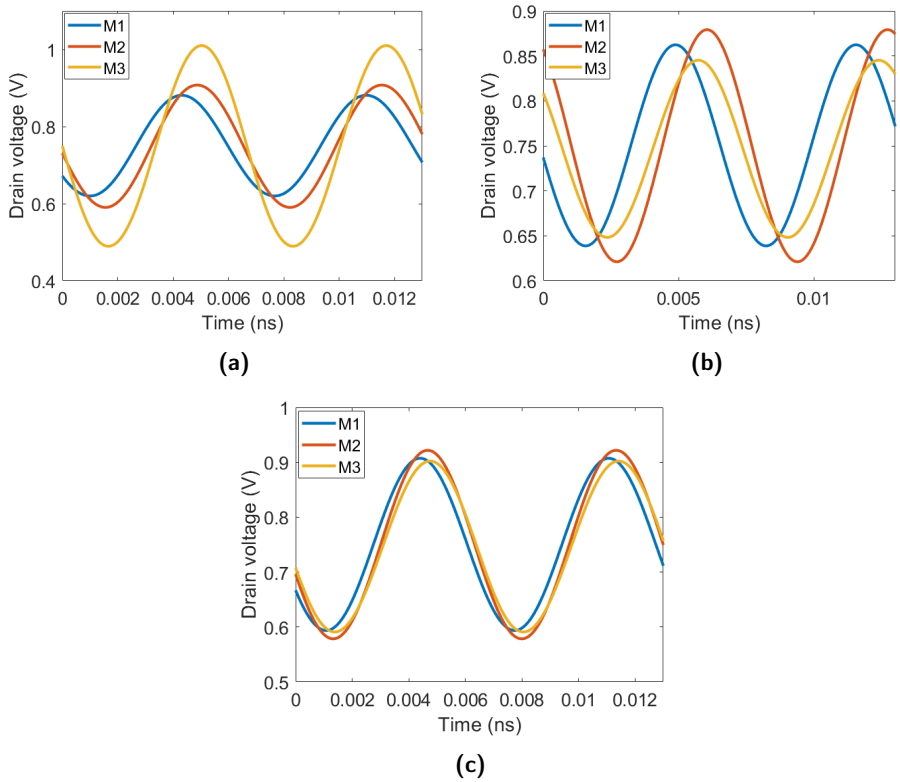


Figure 3.15: Phases for each of the transistors in the output stage of the stacked topology. (a) the originally calculated capacitance and inductance, (b) the optimised capacitance without a inductance applied, (c) the fully optimised circuit used for all other simulations.

3.2.3 Large- & Small-signal performance

The small-signal S-parameters of the stacked PA is shown in Figure 3.16, where the maximum small-signal gain is found to be 18.9 dB at 134.7 GHz with a 3 dB-bandwidth of 49.2 GHz between 127.8 and 177 GHz. In order to keep the broadband behavior of the design, the focus when designing input and output matching networks were to keep S11 and S22 low for higher frequencies. Otherwise the large-signal performance of the PA would suffer at high frequencies.

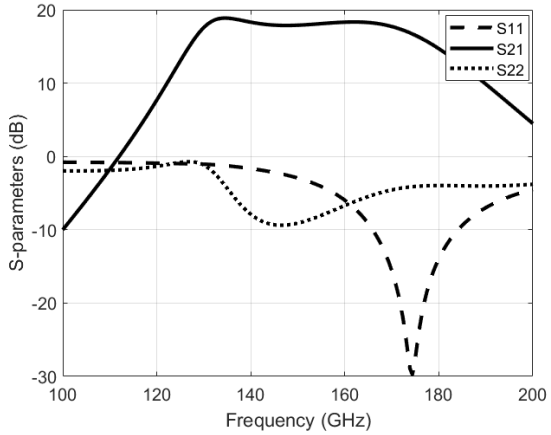


Figure 3.16: small-signal S-parameters over frequency for the stacked topology. S12 is omitted due to being lower than -55 dB for all frequencies.

In Figure 3.17 the output power and third order intermodulation product vs input power is presented at 150 GHz. OIP_3 is extrapolated and found to be 21.6 dBm. In Figure 3.18a the output power, gain and PAE at 1dB compression over frequency are presented. P_{1dB} is over 8.5 dBm for all frequencies and is peaking at 147 GHz with a value of 10.4 dBm. Figure 3.18b shows saturation power along with max PAE over frequency. The maximum PAE is 14.55% at 147.5 GHz and max P_{sat} is 13.6 dBm at 153.6 GHz.

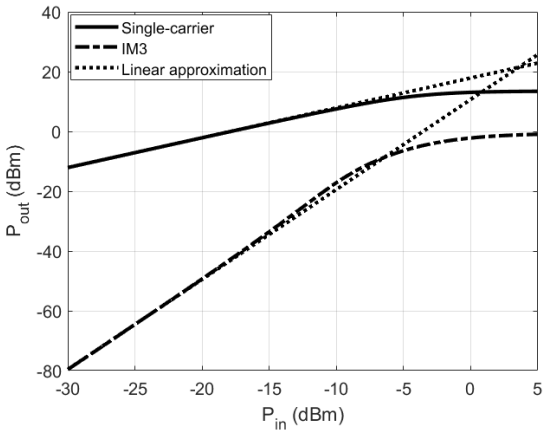
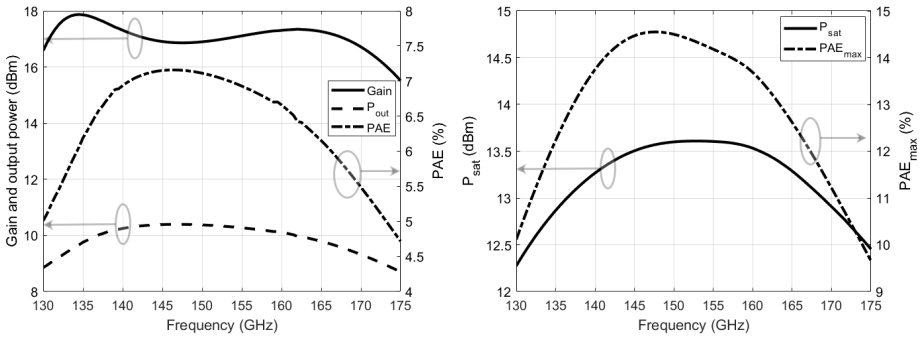


Figure 3.17: Output power of the stacked topology with a single tone source at 150 GHz, and the third-order intermodulation of a two-tone source at 150 GHz and 151 GHz. OIP3 was extrapolated to 18.4 dBm.

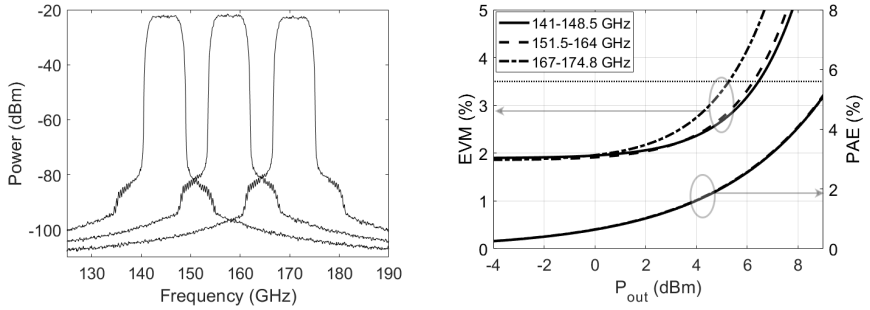


(a) **(b)**

Figure 3.18: (a) Output power, Gain and PAE at 1-dB compression over frequency, (b) Saturation power and maximum PAE over frequency for the stacked topology.

3.2.4 System performance

After evaluating the typology's large- and small-signal performance its system performance was tested. The approach was the same as for the PDCS topology. The topology was tested in the three different frequency sections which spectrum's are presented in Figure 3.19a for an input power of -22 dBm. They have a bandwidth of 6.25 GHz in order to comply with the goal of 100 Gbit/s presented earlier. The EVM and PAE as functions of the output power is presented in Figure 3.19b. The horizontal dotted line shows the 3.5 % EVM limit of the 256 QAM. Going from the lowest frequency section the output power at 3.5 % EVM were 6.5, 6.2 and 5.2 dBm respectively. The PAE at these powers were 2.9, 2.7 and 2.1 % respectively. All three sections had an output power higher than the requirement of 4.7 dBm presented earlier.



(a) **(b)**

Figure 3.19: (a) Spectrum's used for the three 256 QAM simulations. (b) EVM and PAE over output power for the three 256 QAM sections. The horizontal line shows the maximum EVM allowed for 256 QAM.

For the middle section, 64 QAM is an alternative to 256 QAM since the required bandwidth of 8.33 GHz still fits in the allocated frequency section. The results from the 64 QAM simulations are shown in Figure 3.20. Figure 3.20a shows the spectrum of the 64 QAM on top of the 256 QAM to illustrate the increased bandwidth. As mentioned earlier, the 64 QAM tolerate a higher EVM, 5.5 %, and thus the output power at maximum EVM has increased to 8 dBm with a PAE of 4.1 %. The constellation diagrams for both 256 and 64 QAM at maximum EVM for the middle section are shown in Figure 3.21.

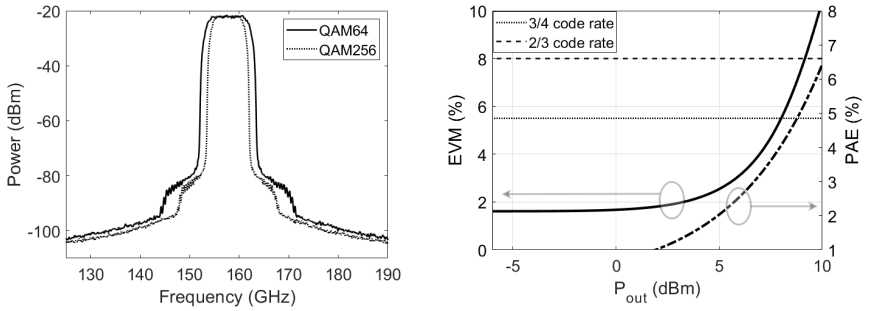


Figure 3.20: (a) Spectrum used for the 64 QAM simulation on top of the spectrum for the 256 QAM simulation in the same frequency section. (b) EVM and PAE over output power for the 64 QAM simulation. The horizontal line shows the maximum EVM allowed for 64 QAM.

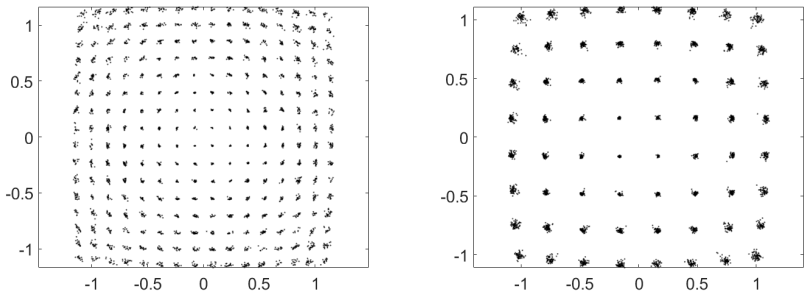


Figure 3.21: Constellation diagrams of the (a) 256 QAM case and (b) 64 QAM case at their respective maximum EVM.

As for the PDCS, the performance of the stacked topology was simulated without the added phase noise. The result from this can be seen in Figure 3.22. Here the output power at maximum EVM for each frequency section is 6.9, 6.7 and 5.7 dBm respectively, with a PAE of 3.2, 3 and 2.4 % respectively. This is an

increase of around 0.5 dBm for each section and shows that, as long as the phase noise is kept at a reasonable level the stacked PA reaches the requirements. For the 64 QAM case the increase was only 0.1 dBm to 8.1 dBm. The main difference to be seen from this simulation is that the noise floor at ∼1.9 % EVM disappears and the EVM approaches 0 for low input powers.

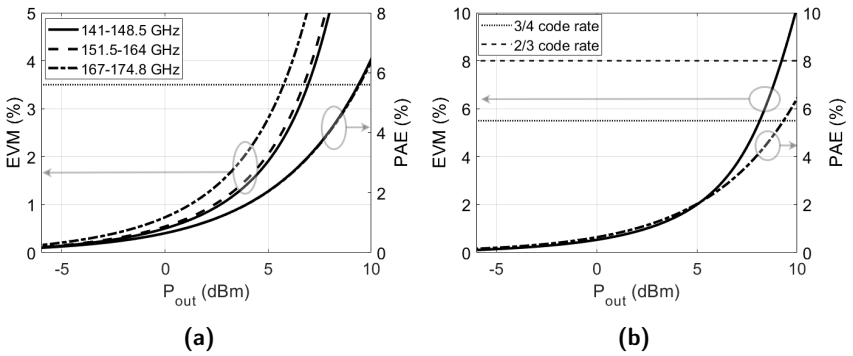
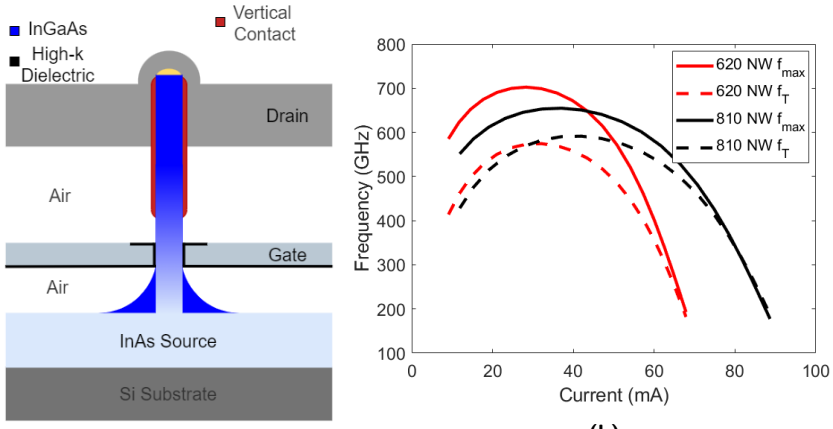


Figure 3.22: EVM and PAE over output power without added phase noise for (a) 256 QAM and (b) 64 QAM.

3.3 Next generation model

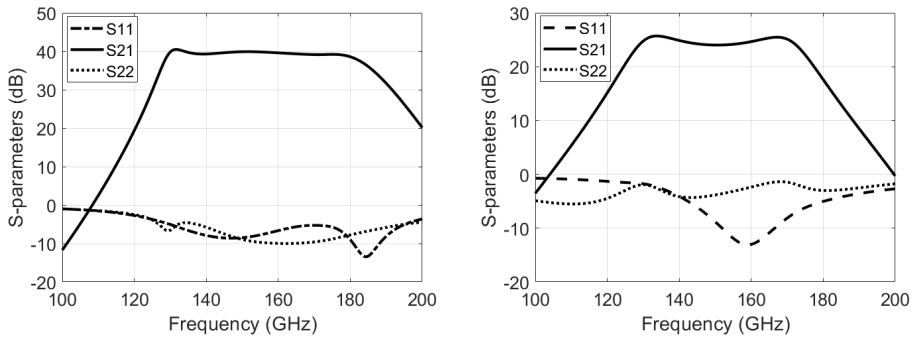
Towards the end of the thesis period NordAmps presented a next generation (NG) model. By replacing the dielectric spacers with air, as seen in Figure 3.23a, the f_{max} and f_T may be improved significantly[11]. The research surrounding this model is still in progress and thus the field-plate capacitor has not been implemented. This means that the V_{bd} of the transistor is 0.5 V_{rms}. Again the drain is contacted by fingers to allow for high frequency PA design. The f_{max} and f_T for transistors of the same dimensions as the previous model is shown in Figure 3.23b. To compare the NG models performance with the current one the same designs are used as for the PDCS and stacked PAs. Meaning that the amount of stages as well as transistor dimensions remains equal. The matching networks and biasing points are however altered to match the new characteristics of the transistors. While this does not give the optimum performance of this model it allows for a meaningful comparison.



(a) **(b)**

Figure 3.23: NG model and the f_{max} and f_T for two transistors using 10 fingers and different numbers of fingers.

The small-signal parameters for the PDCS and stacked PAs with the NG model is seen in Figure 3.24. The designs achieved a S21 gain of 40.5 and 25.7 dB, while their bandwidths stretched between 128.4-182.6 and 127.2-174.3 GHz respectively. It is evident that the increase in f_{max} allows the designs to reach a much higher gain.



(a) PDCS **(b)** Stacked

Figure 3.24: S-parameters for the PDCS and Stacked PAs using the NG model.

Comparing large-signal characteristics was performed by observing the P_{1dB} characteristics, and the P_{sat} and PAE_{max}, shown in Figure 3.25 and 3.26, respectively. Again the gain of the NG model is shown to be significantly larger then the previous one. However, the output power is lower as expected due to its lower V_{bd}. The PDCS and stacked PA achieves a P_{1dB} of -1.6 and 3.1 dBm respectively. The stacked PA did however achieve a larger PAE_{max} than the current model, its PAE_{max} of 16.3 % shows great potential for high-efficiency designs.

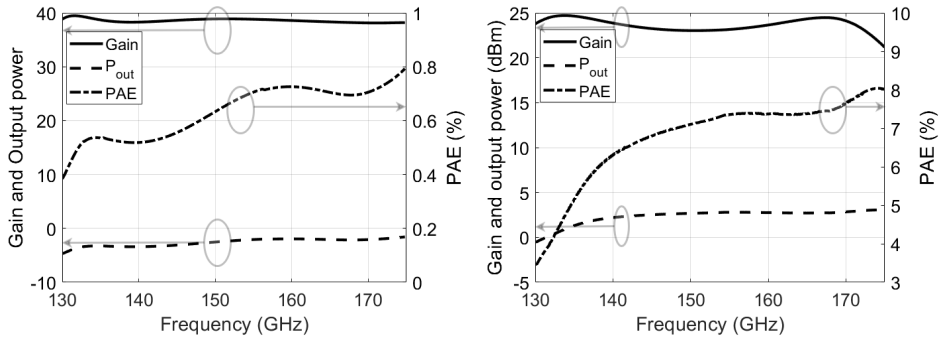


Figure 3.25: Gain, P_{out} and PAE for the PDCS and stacked PAs at the 1dB compression points using the NG model.

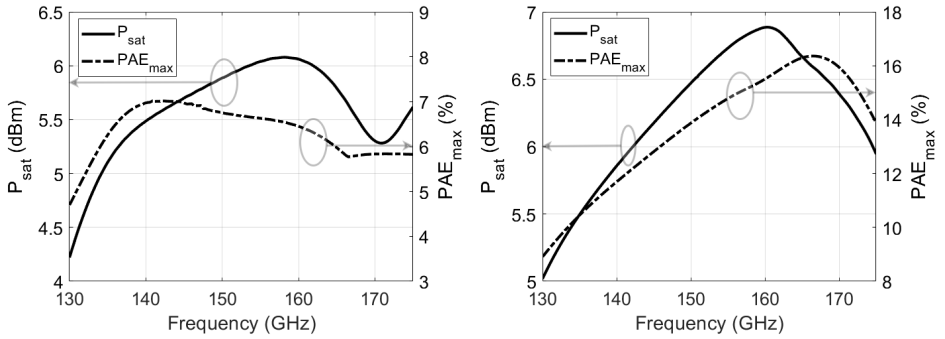


Figure 3.26: $\mathrm{P_{sat}}$ and $\mathrm{PAE_{max}}$ for the PDCS and stacked PAs using the NG model.

3.4 Comparison

3.4.1 This work

The stacked PA shows a superior performance to the PDCS PA in most regards. Its maximum $\mathrm{P_{sat}}$ and $\mathrm{P_{1dB}}$ exceeds the PDCS PA by 1.5 dBm and 2.4 dBm respectively. Two reasons as to why this is the case are: as the voltage on each transistor in the stacked topology swings in phase, the output node experiences a larger possible voltage swing, while still not violating the breakdown voltage. Additionally the PDCS topology is limited by the resonance relationship between the transformer inductance and the internal parasitic capacitances of the transistors. This causes a size limit of the transistors as the transformers have a minimum required inductance. Hence reducing the possible current swing.

With the use of several stages tuned for slightly different frequencies and the combiner network, the PDCS PA is able to achieve a wider bandwidth and higher gain than the stacked PA. The bandwidth of the PDCS PA covers the range between 122-180 GHz with a maximum S21 of 24.1 dB compared to the stacked PA bandwidth of 127.8-177 GHz with maximum S21 of 18.9 dB.

It is shown through simulations with Microwave Office that the stacked PA achieves an output power of 5.2, 6.2 and 6.5 dBm at the EVM limit 3.5 % using 256 QAM scheme. This shows that the stacked PA achieves an output power past the goal of 4.7 dBm with a 100 Gbps data rate for 256 QAM. The PDCS PA using the same configuration with the output powers 3.6, 3.3 and 3.1 dBm does not. However, for the 64 QAM scheme both PAs achieve more than the output power goal at the EVM limit 5.5 % with a 100 Gbps data rate. The output powers at that limit is 5.1 and 8 dBm for the PDCS and the stacked PA respectively.

3.4.2 Other works

In order to compare the designs a table has been composed involving several state-of-the-art PAs from different technologies, see table 3.1.

Ref.	Process	BW (GHz)	S_{21} (dB)	P_{sat} (dBm)	PAE_{max} (%)	P_{1dB} (dBm)	V_{cc} (V)	Year
This work	**2-way, 4-stage PDCS**	**122-180**	**24.1**	**12.1**	**9.8**	**8**	**0.81**	**2022**
This work	**2-stage, 3-stacked**	**127.8-177**	**18.9**	**13.6**	**14.6**	**10.4**	**2.25**	**2022**
[39]	28nm CMOS 4-stage PDCS	121-143	22.5	8.0	6.6	5.2	0.9	2020
[40]	28nm CMOS 2-way, 3-stage PDCS	120-150	21.9	11.8	10.7	10 *	1	2021
[41]	16nm FinFET CMOS 2-way, 3-stage PDCS	114-136*	25.6	13.1	11	7.1	0.8	2020
[41]	16nm FinFET CMOS 2-way, 3-stage PDCS	114-136*	25.6	15	12.8	9.2	1	2020
[42]	100nm GaN HEMT 4-stage cascode	128-146	34	26.4	11.5	-	12†	2019
[27]	250nm InP HBT 8-way, 3-stage CB	125.8-145.8	20.3	23	17.8	20.2	2.65	2021
[43]	130nm InP HBT 3-stage, 2-stacked	140-210	30	13.4	17.4	4.9	2.3	2021
[44]	55nm SiGe BiCMOS 4-stage CB	125-159	34	17.6	17.5	16.8	2.2	2021
[44]	55nm SiGe BiCMOS 4-stage CB diff.	125-150	25	19.3	13	18.5	2.2	2021
[45]	90nm SiGe BiCMOS 4-way, 2-stage cascode	110-145	18.2	21.9	12.5	18.6	4	2021
[46]	130nm SiGe BiCMOS 2-stage cascode	124-146*	16.7	15	7.8	15	4.2	2022
[47]	130nm SiGe BiCMOS 3-stage cascode	110-170	21.6	12.1	5.1	10.26	3.3	2021
[48]	130nm SiGe BiCMOS 4-stage cascode diff.	100-180	24.8	11	∼5	9.5	2.7	2016

*Estimated, † V_{ds}, -Not specified.

Table 3.1: Comparison with state-of-the-art PAs

The major advantage of this work is the broadband design. While there are examples of other broadband amplifiers they suffer in other metrics. For example [43] which has about 3 and 5.5 dBm lower P_{1dB}, or [47] and [48] which maximum

PAE is almost 5 and 10 % lower than the presented designs. CMOS, the other technology with a low V_{bd} and f_{max} performs equally or worse to our design at a significantly smaller bandwidth. The FINFET design of [41], does not see a similar performance for the lower supply voltage 0.8 V. With a higher supply voltage of 1 V it is comparable; however, the bandwidth is barely reaching the 130 GHz mark. Our designs do not reach the performance of the narrowband HEMT, HBT and BiCMOS PAs. However, these technologies are, additionally to being narrowbanded, capable of a larger supply voltage. While our stacked design uses a somewhat high supply voltage it is important to remember that this is an effect of the topology rather than the technology.

Chapter 4
Conclusion & Future work

In this thesis, two different PA topologies were designed for D-band (130-174.8 GHz) backhaul applications. The goal was to verify if the technology is suitable for PA design at high frequencies. By performing a comparison between the topologies as well as with other state-of-the-art PAs the performance of the topologies were studied. They were also simulated with high order QAM modulations to see whether or not they were capable of wireless transmission at a 100 Gbps data rate.

The first design was a four stage pseudo-differential common source amplifier with a two-way series-transformer power divider/combiner network. The second design was a single ended two stage three stacked amplifier. Both designs were shown to be competitive when compared to other works.

Both designs are shown to be capable of 100 Gbps data rate transmission. However, the first design does not achieve the set out goal for output power using 256 QAM and is limited to using 64 QAM. With recommendations given by the ECC regarding available bandwidth this implies that the design, given this power boundary, would only be suitable for operation between 151.5-164 GHz. The stacked amplifier design achieves the power goal with both modulation schemes and would as such be suitable for 100 Gbps data rate transmission in the three sections available. That is, given the power boundary, the stacked design is suitable for operation between 141-148.5, 151-164 and 167-174.8 GHz.

In conclusion, this thesis shows that PA design using vertical InGaAs nanowire transistors for high frequency operation is not only possible, but a highly competitive technology.

4.1 Future work

In order to further improve the work of this thesis there are a few steps which could be performed.

- The next verification step is to perform a layout design and produce the circuits for measurement. Due to time limitations this was unfortunately not an option given the time span of the thesis. Additionally Monte-carlo simulations should be done to investigate the impact of process variations.

- Through investigations the pseudo-differential CS and stacked topologies were found to be preferable. However, further research and design of other topologies could be of interest.
- The phase locked loop reference used in this thesis for system simulations is tested for 156 GHz and has a bandwidth of 16 GHz. As such using its performance across the entire D-band is an approximation. To fully determine the impact on full system performance a complete transmitter should be designed.
- The toughest constrain for the PA designs presented here is the V_{bd}. The field-plate capacitor was introduced to mitigate the problem but has a degrading effect on f_{max}. Further optimization in manufacturing of the field-plate and the doping profiles of the nanowire transistor could enable a higher V_{bd} with a better f_{max}.
- The field-plate capacitor length in this thesis was chosen to provide a larger V_{bd} without affecting the f_{max} significantly. In reality there should be an optimum value of the length which provides the best results in the final PA design. However, to the best of our knowledge this is a rigorous investigation which would require the design of many PAs to determine.
- Further research into the NG model presented in section 3.3 is necessary. It shows great potential which with a tailor-made design and a higher V_{bd} could lead to an exceptional PA.

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Appendix A

Wilkinson

The Wilkinson power divider, first proposed by E.Wilkinson in 1960[49], splits power from one input port into two output ports. By utilizing quarter wave transmission line transformers and a resistor, as shown in Figure A.1a, equal and in phase power division is ensured. This can be seen by studying the ideal S-parameter matrix from the three port system[26]

$$S = -\frac{1}{\sqrt{2}} j \begin{pmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{pmatrix}. \tag{A.1}$$

In a ideal case port 2 and 3 are fully isolated from each other meaning any power delivered from only one side will not end up in the other. The system is also symmetric meaning that if the same power is delivered from port 2 and 3 the sum of them will end up in port 1. By utilizing this a full divider/combiner structure can be done using Wilkinson to split the input into two PAs and the combine the amplified waves to the output. When working with real Wilkinson dividers/combiners there will be loss present. This originates from non ideal transmission lines but as seen in Figure A.1b this loss is very low. The main drawback of the design is that it is an inherently narrow structure thanks to relying on quarter wave transmission lines. This can be somewhat combated by increasing the amount of transmission lines making the structure more complex but that is something that wont be covered in this thesis.

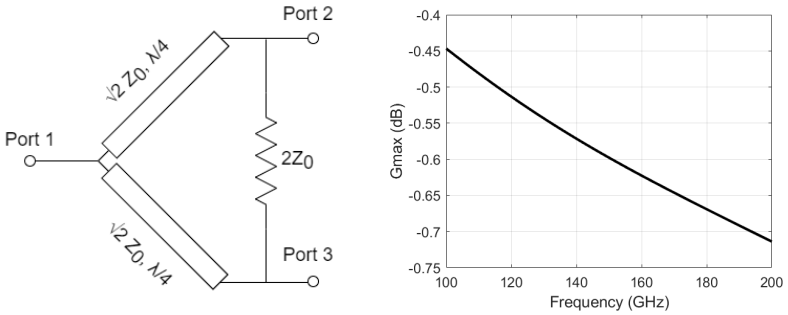


Figure A.1: Illustration of a wilkinson power divider and the simulated loss over frequency for a divider/combiner.

Appendix B

Transformer model

The transformer is modeled from the work of [50] and the stack is shown in Figure B.1. The transformers are made in the top two layers to minimize the capacitance to the substrate. Additionally the conductors and the vias are made from gold to minimize the resistance. The transformer circuit model is shown in Figure B.2a, where C_{inter} represents the capacitive parasitic between the windings and C_{sub} represents the capacitive parasitic from the windings to the substrate. Their respective resistances models the Q-factor. There are two DC-taps located in the center of each winding. These are made possible due to the skin effect, an effect which causes the transformer to have an impedance which is dependant on frequency[51]. L_{bias} and L_t represents the inductors with their respective resistances to model the Q-factor. C_t decouples the RF from the DC in the model. The turns ratio of the transformers used are 1. By adjusting the coupling coefficient and overlap between secondary and primary winding we have set the transformer loss according to Figure B.2b.

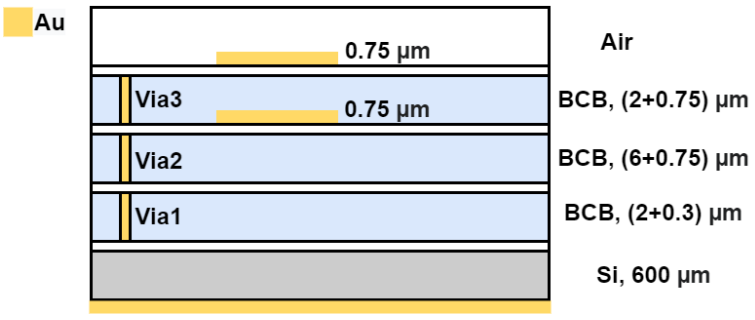
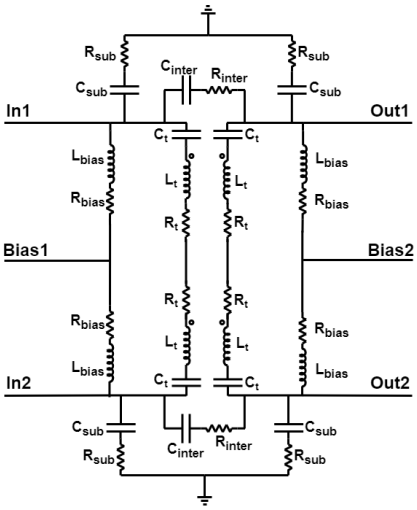
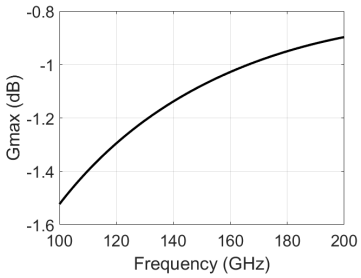


Figure B.1: Illustration of the stack with transformers which are modeled for the circuit simulations.



(a) Model.



(b) Loss over frequency.

Figure B.2: Model of the transformer provided by NordAmps and its maximum gain loss in the frequency range 100-200 GHz.