Analysis of condition for ALD deposition of ferroelectric HZO

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Abstract

Deposition of ferroelectric hafnium zirconium oxide (HZO) on semiconductor samples with Atomic Layer Deposition (ALD) has proven to be a viable method of production. But while the physical processes of ALD deposition is relatively well know, there exists some gaps in knowledge about different parameters for the ALD and the resulting depositions. This work is about analysing mainly how the purge time and chamber temperature of a thermal ALD affects the deposited HZO films thickness, defect density and general ferroelectric switching capabilities. This involved depositing ferroelectric HZO using the different recipes, measuring the thickness of the samples with an ellipsometer and testing the electric characteristics with high frequency IV measurements. The results seemed to align fairly well with known theory. Higher temperatures generally result in faster reactions but also increases the evaporation of the deposited. To counteract this, shorter purge times should be used at higher temperatures, giving a ”sweet spot” of temperature and purge time. Even though the results seemed to agree with the theory to an extent, extrapolating clear linear trends were nearly impossible with the measurements. But more importantly, all the samples showed ferroelectric properties which was earlier hard to achieve with certain ALD depositions within Lunds University. This speaks to the stability of the current method of deposition. Another important result was that samples deposited with the same parameters showed very similar thickness and electric properties, once again showing how stable and reliable the ALD process seems to be.

Since there isn't enough results to draw clear conclusions, further testing and analysis is encouraged. This would mean testing other temperatures and purge times, and perhaps also measuring other electric properties, like endurance.

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Chapter 1

Popular Science Summary

It is fair to say that the microelectronics have become integral for the modern society. Today you can't walk down the street without seeing computer screens, LED-lights and the vast amount of cellular almost everyone carry around in their pockets. The devices are of course still improving as the market is always asking for cheaper and faster products.

The improvement of the processing power for the devices the first couple of decades since it's invention has almost solely been possible by the down scaling of the smallest component of a logistical circuit, the transistor. But in recent years, this has proven harder due to the original transistor design not working well when the devices are small enough to heavily experience quantum mechanical disturbances. This in turn has introduced a heavier emphasis on innovation with the physical design of the transistors and also what materials to use.

A metric that has gained a lot of traction because of the need for portable devices is the ability to reduce power usage. This is due to the limited power available in the batteries of the portable devices. The main way to reduce the power consumption for computing is to minimize the leakage current for the transistors. This is hard to achieve with the current popular design of the transistor as it carries an intrinsic lower limit on how much current will be generated from a given voltage. To avoid this, new fundamental designs of the transistor is being explored.

An electric property that might be of use for the transistors of tomorrow is the ferroelectric property. In short a ferroelectric material is a material that can retain a electric field after being exposed to an external electric field. This material can also shift its electric field back and forward, making it possible to perhaps be used as a method of storing information.

The ferroelectric phenomenon has been known for a long while but the material that exhibited ferroelectric switching did not retain these properties when scaled to the size of modern microelectronics. Thankfully the material hafnium, which is currently being implemented as a material for modern transistors, has been shown to be able to achieve ferroelectric properties during certain conditions.

How to deposit hafnium in large stable processes is being debated, and one very promising deposition method seems to be the atomic layer deposition (ALD). The different metrics of how to deposit the hafnium using ALD is what is being analysed in this work.

Chapter 2

Introduction

The world of modern electronics we know today would not be possible without the introduction of semiconductors. The semiconductor industry is very large with an approximated revenue of $464 billion in the year 2020[8]. There is a large variety of semiconductor devices that have different purposes, such as transistors, memory cells, LED's etc. Within these devices, there can also be different structures of the units, creating unique approaches on how to handle the tasks at hand. A good example is the memory devices, where there are volatile and non-volatile memories, faster or slower, more or less energy efficient and so on[9].

During the last couple of decades, the size of the transistors used in modern computers and electronics have been scaled down drastically. The trend of reduction in transistor sizes was observed in 1965 by Intel's co-founder George Moore. Moore postulated that the number of transistors on a given unit of area would double every two years[10]. This is often referred to as "Moore's Law" and has in modern days been a driving force for the continued scaling of transistors in the modern day.

To make these different devices, a lot of resources are spent on analysing the semiconductors and their behaviour in various conditions. This has led to the discovery in several properties for some semiconductors. One of these recent discoveries is the appearance of ferroelectricity in doped HfO_2[11].

Ferroelectricity is a phenomenon where a material is capable of retaining a certain polarization after an electric field has been applied to it[12]. Materials that inhabit this phenomenon are called ferroelectric materials or ferroelectrics. The material can also change direction of this polarization by applying electric fields in different directions[12]. The phenomenon might have some applications in modern electronics as both a way of storing information or as a potential alternative to create a negative capacitance field emission transistor (NCFET). Other

relevant devices are ferroelectric field emission transistor (FeFET)[13] and ferroelctric tunnel junction (FTJ) devices[14].

Since HfO_2 is already used in modern transistors as the gate oxide, this became very interesting for the electronics market. One discovery which came from the doping of Hf is the ferroelectric properties of Hafnium Zirconium Oxide (HZO). The oxide ranges from not ferroelectric to ferroelectric and anti-ferroelectric depending on the concentrations of Hafnium and Zirconium[15].

Lunds university is working with III-V-material and has succeeded in intergrating ferroelectric HfO2 on InAs[16]. It has been noticed that the films have a significant amount of defects[17] and has set out as goal to optimize the ALD process to keep the good ferroelectric properties while at the same time reducing the defects. This has been analysed by retaining the good performance in PUND-measurements and at the same time reducing the leakage current which is a sign of the density of defects in the film.

To produce these ferroelectric HZO films, Atomic Layer Deposition (ALD) has shown great potential[18]. When using the ALD, different temperatures and exposure times are used for the different steps of the deposition. This work will revolve around analysing the effects of different temperatures in the ALD chamber and the duration of the purge time for water. Measurements will be made of the breakdown voltages, leakage current, the ferroelectric properties and also the physical growth of the samples.

Chapter 3

Theory

3.1 Ferroelectricity

A ferroelectric material is a material which can be polarized by the exposure of an external electric field and then retain part of this polarization after the electric field has vanished[19].

Electric polarization is defined as the separation of the center of positive charge and the center of negative charge in a material[20]. This can be more easily understood when looking at the standard model of a magnet. The magnet has a positive pole and a negative pole. Electric polarization works the same way, except the fields are electric instead of magnetic[20].

Ferroelectricity was first discovered in 1921 by Joseph Valasek. The discovery occurred when investigating the material ”Rochelle Salt”[12].

This property comes from a slight asymmetry in the crystal structure, which gives certain atoms two or several meta-stable configurations[21]. Depending on which of these states the atoms sit in, the material will have different polarization. This is because there will be a net shift in what position the positive atom cores are located in the lattice. As the positively charged ions move when an electric field is applied, a net change in polarization is made. This change in polarization can be seen as movement of charges over a specific time, which is the same as an electric current. An illustration of how the polarization relates to the energy can be seen in Fig. 3.1.

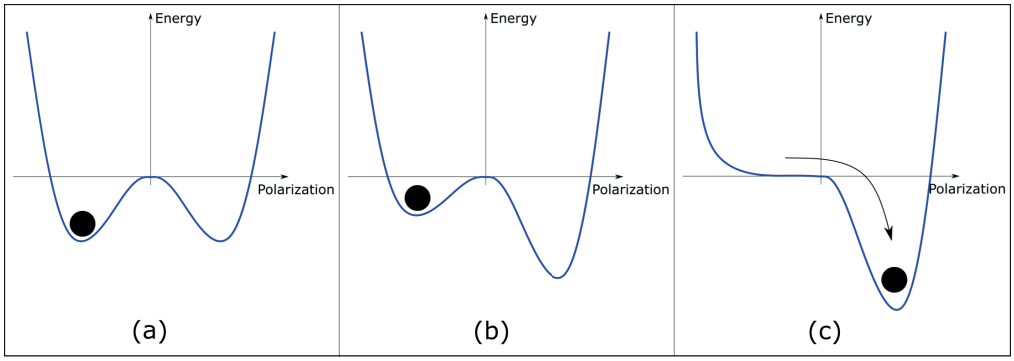


Figure 3.1: The figures reporesent the polarization and potential energy for the different states where (a) is the system without an applied electric field. As an electric field is applied in (b), the left energy state is lifted slightly and finally in (c) the electric field is large enough for the atom core to shift from one state to the other. Illustration made from [1]

Typically, the atoms are polarized in larger regions where all the crystal cells share the same polarization. These regions are called ”domains”[21][22]. These domains don’t all have to be oriented the same direction. If for example every other is polarized one way and the rest the other way, the material will appear to not be polarized from a macroscopic perspective. When this is the case, the domains can be visualized as in Fig. 3.2(a). But by applying an external electric field, the orientation of all the domain can be made the same, as can be seen in Fig. 3.2(b). When the electric field is later removed, the material keeps its remanent polarization, which is the unique property of the ferroelectric materials[12], as can be seen in Fig. 3.2(c). This means most of the domains point in the same direction even though an external electric field is not applied, but not all the domains.

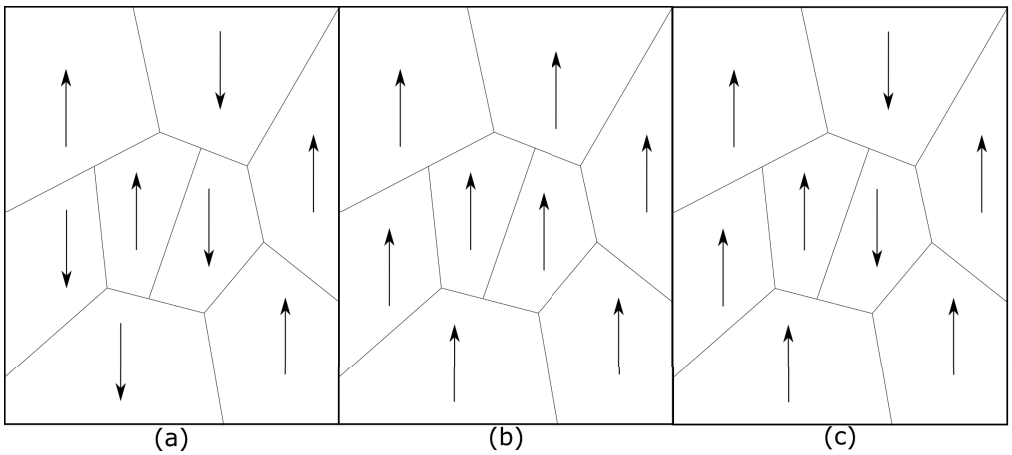


Figure 3.2: Illustration of crystal domains where (a) shows the net polarization is zero as since the arrows cancel each other out (b) an electric field is applied, causing the domain to align alongside the electric field and finally (c) some domains retaining the polarization after the removal of the external electric field, resultning in a net remenant polarization. Illustration made from [2]

When discussing the ferroelectric materials, the perovskite oxides are often considered the archetypal system[23]. But these materials have shown a poor ability to retain their ferroelectric properties when being scaled down to nm sizes. This makes them incompatible with the current size of semiconductor processing electronics.

Luckily, in 2011 there was a revolutionary discovery of ferroelectric behaviour in doped hafnium oxide thin films[11][24]. This drastically changed the viability of ferroelectric devices in modern electric devices. Hafnium oxide was already being integrated as a high-k alternative to silicon oxide in modern devices. What is also very important about the discovery is that the crystal lattice retains its ferroelectricity even when scaled to at least 10 nm sizes[11].

3.2 Hafnium Oxide

Moore's law has pushed modern transistors to its limits in terms of size. One big problem was the quantum mechanical effects that arrived between the gate and channel in the transistors by extensive scaling[25]. To handle this problem, the previously used gate oxide SiO_2 was replaced by the high-k dielectric HfO_2[26]. Having a high-k material essentially means that the material has a high ability to

be polarized. This means a thicker high-k oxide can create the same electric field below as a thin oxide with lower k value when applied with the same bias[27]. By having a thicker oxide, the tunneling problems from the scaling could be avoided for a couple of transistor generations.

When creating electrical components with several different materials, it is important that they can be implemented together. For example, if the crystal structure for the different materials are too different the interface between the materials can be strained or contain defects. This can lead to different electrical and mechanical properties which might be detrimental to the final devices metrics.

An important property of the hafnium oxide is that it is very compatible with the silicon substrate. Because of the combination of being a high-k dielectric and also having good compatibility with silicon, it is current being implemented in many modern transistors[26].

3.3 P-E and PUND-measurement

There are several different ways of analysing the ferroelectrical phenomenon. The most common way to do this is to analyse the polarization of the material as a function of an applied electric field. One efficient way of doing this is to create a capacitor using the ferroelectric material instead of a dielectric material between the two contacts. The contacts then have a voltage applied to them, creating an electric field over the ferroelectric material. The voltage typically have certain shapes for different types of measurements, usually in the form of pulsed voltages. The current created between the contact pads is measured.

When the current has been measured, the data can be handled to plot a P-E curve. To calculate the total charge stored in the material, the current has to be integrated over the time the voltage was applied;

$$Q(t) = \int_{t_1}^{t_2} I(t)\, dt \tag{3.1}$$

where the equation assumes that the dielectric is perfect, meaning no current is being conducted through the material[28]. In reality this is not the case, as there is almost always a certain amount of leakage current due partially to defects in the material. The stored charge in the material is then normalized by the area of the capacitor, giving the dielectric displacement, D;

$$D(t) = \frac{Q(t)}{A} \tag{3.2}$$

where A is the capacitor contact area, in this case a circle and the area is given by;

$$A = \pi r^2 \tag{3.3}$$

The polarization can be calculated as the dielectric displacement plus a small correction to accommodate for low permittivity dielectrics[28]

$$P(t) = D(t) - \varepsilon_0 E(t) \tag{3.4}$$

The calculation of the electric field is a bit simpler. The electric field is simply calculated as;

$$E = \frac{V}{d} \tag{3.5}$$

where V is the applied voltage on the pads and d is the distance between the surfaces.

To quantify the ferroelectric properties of a material, certain measurements have to be made. The current caused by the switching of the material should ideally be separated from the unwanted leakage current. An effective way of doing this is by doing a positive up negative down (PUND) measurement. In Fig. 3.3, a standard PUND measurement can be seen

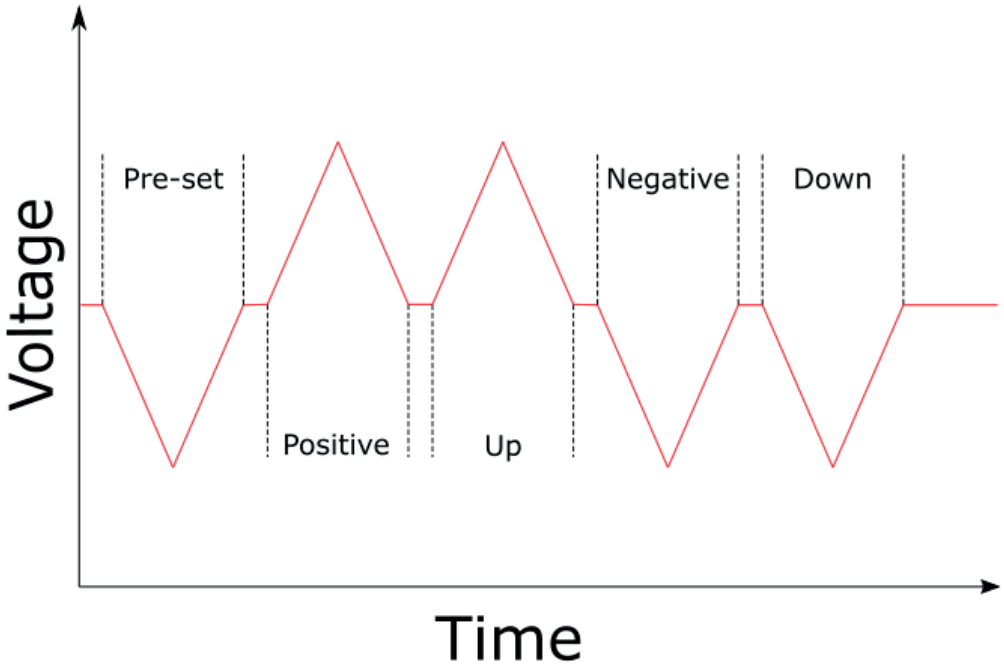


Figure 3.3: Illustration of the voltage applied to the device during the PUND measurement and the names of the different peaks

The measurement is designed to separate the ferroelectric induced current from the leakage and capacitive current. The input is the voltage and then the induced current is measured. The measurement consists of five voltage spikes. The first spike is there to make sure the material is oriented the right way before the measurement, typically called preset. The data from this spike is not actually used. The next two spikes are oriented the same way, typically positive in voltage. The first one of these is called ”positive” and the current from this spike will include both the switching and the leakage/capacitive current. Since the crystal is oriented by the positive electric field, there won't be a switch in the material during the second positive spike. This spike is referred as the ”up” spike. Since there is no switch in the material, there will not be a switch current. This means that the measured current will only be leakage and capacitive current. The last two spikes are ”negative” and ”down”. These do the same thing as positive and up, except the voltage applied is negative[29].

To get the switching current without the leakage/capacitive current from the up is subtracted from the positive current. This removes the two other current sources, leaving only the switch current. The same thing is also done with negative

and down.

3.4 Hysteresis Loop

To analyse the ferroelectric properties of a material, the polarization of the material as a function of an applied electric field has to be analysed first. When this P-E plot is made, the ferroelectric material will make a so called hysteresis loop[30]. One can be seen in Fig. 3.4.

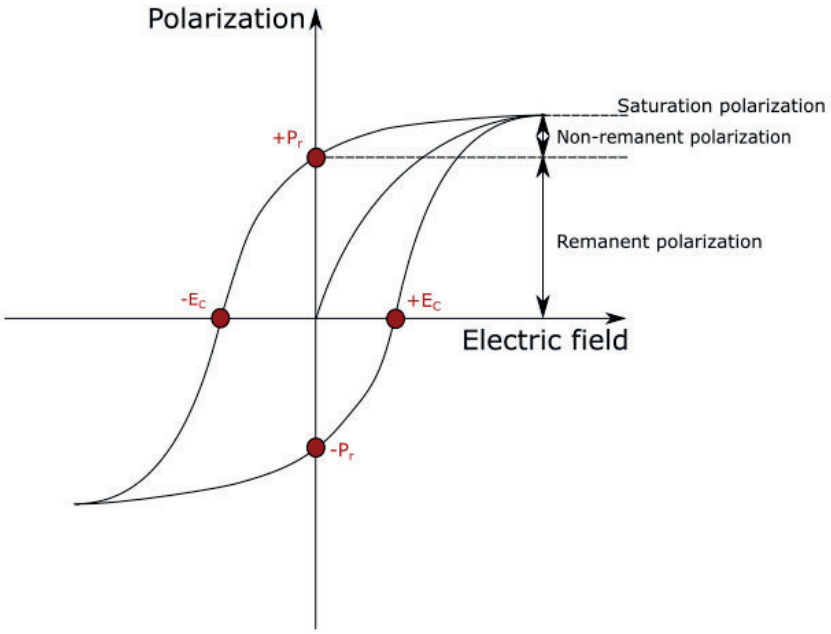


Figure 3.4: Picture of a ferroelectric hysteresis loop [3]

What can be seen in Fig.3.4 is that the material starts of in the center of the plot where no electric field is applied and there is no polarization. As an electric field is applied, the polarization is increased, though not linearly. At high enough E-field, the polarization flattens out. This polarization is called the saturation polarization. This is when all the domains are pointing in the same direction. When the electric field then is removed, the plot follows the upmost curve in Fig. 3.4. As the electric field reaches zero, the polarization is no longer zero, this is because the material is ferroelectric. The polarization at this point is called the remanent polarization.

A negative E-field is then applied and the effect is mirrored, except this time the polarization is negative.

3.5 Electron Transport Mechanisms

Different conduction mechanisms through oxides can generally be decided into two groups, ”Electrode-limited conduction mechanisms” and ”Bulk-limited conduction mechanisms”[31]. These mechanics are important for understanding why there is current through the oxide even though oxides are supposed to act like insulators and not conduct any current.

3.5.1 Electrode-limited conduction mechanism

The electron limited conduction mechanisms are very dependent on the electrode-dielectric contacts that form when creating the samples. At this interface, there is a barrier that limits how electrons can move between these materials. In the cases below, a metal-insulator interface is the barrier that is described. The electrode limited mechanisms are (1) Schottky or thermionic emission, (2) Fowler-Nordheim tunneling and (3) direct tunneling. A visual illustration of the different transport mechanisms can be seen in Fig. 3.5, but will be explained individually in the sections below.

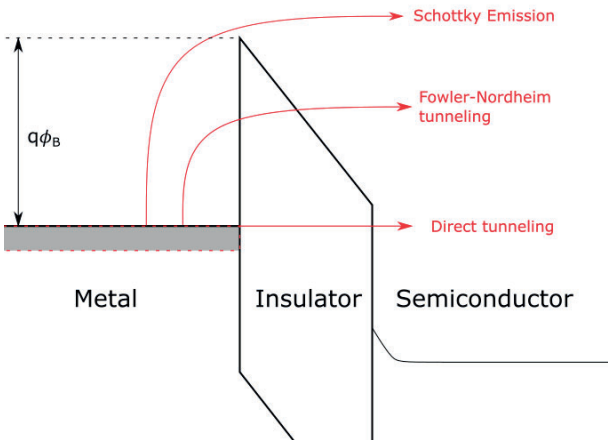


Figure 3.5: The different transport mechanisms over a MIS interface.

Schottky Emission

Schottky emission is that is dependent on thermal energy to pass the metal-oxide barrier. Electrons that receive thermal energy according to the Fermi distribution [32]. This means that for a certain energy above zero kelvin, a certain number of charge carriers will have enough energy to pass the barrier[31]. The equation for the current density is;

$$J = A^* T^2 exp\left[\frac{-q\Phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}}{kT}\right] \tag{3.6}$$

$$A^* = \frac{4\pi q k^2 m^*}{h^3} = \frac{120 m^*}{m_0} \tag{3.7}$$

where J is the current density, A^* is the Richardson constant, m_0 is the free electron mass, m^* is the effective elecron mass in the dielectric, T is the aboslute temperature, q is the electronic charge, $q\Phi_B$ is the Schottky barrier height, E is the electric field across the ferroelectric material, k is the Boltzmann's constant, h is the Planck's constant, ε_0 is the permittivity in vacuum, and ε_r is the relative permittivity of the insulator[31].

Fowler-Nordheim Tunneling

Electrons have a quantum mechanism that is called "tunneling". In classical physics, the electrons will be reflected when the energy of the electron is smaller than the potential barrier. However, if the barrier is thin enough, the electron wave function can penetrate the barrier, which is the mechanism called tunneling. Tunneling is heavily dependant on the thickness of the barrier.

When a voltage is applied over an oxide, the height of the barrier will be shifted linearly, creating a triangular top of the barrier. This makes it easier for electrons to penetrate the barrier as it is thinner at the top. This tunneling is called Fowler-Nordheim tunneling.

Direct Tunneling

Instead of utilizing the bending of the barrier when tunneling though the insulator, the tunneling can occur through the entire thickness of the barrier. This is called direct tunneling.

3.5.2 Bulk-limited conduction mechanisms

The bulk-limited conduction mechanisms are dependent on the properties of the insulator itself. The bulk-limited conduction mechanisms can be divided into Poole-Frenkel emission, hopping conduction, ohmic conduction and ionic conduction

Poole-Frenkel emission

Poole-Frenkel emission is in sorts similar to Schottky emission. The thermal energy may excite electrons from trap states in the oxide to the conduction band, these electrons then act as charge carriers. The applied electric field increases the Poole-Frenkel emission.

Hopping conduction

Hoping conduction can be summarized as tunneling of trapped electrons ”hopping” from one trap site to the next in the oxide.

Ohmic conduction

Ohmic conduction is the conduction which is typically referred to when metals or semiconductors conduct electricity. This current comes from mobile electrons in the conduction band or holes in the valence band. The current density from the ohmic conduction increases linearly with an increase of electric field.

Ionic conduction

As it sounds, ionic conduction originates from the movement of ions. The movement of these ions come from lattice defects in the films. The external electric field causes the ions to jump over certain potential barriers from one defect site to the next.

3.6 Atomic Layer Deposition

3.6.1 Structure of an ALD

ALD (Atomic Layer Deposition) is a method of growing materials on substrates with high precision. This is done by putting the sample into a vacuum chamber and periodically introducing gas and then pumping it out. The idea is that each of these gases contains precursors that can chemically react to the surface of the sample, but not further react to itself. This is called a self-limiting reaction. Ideally, this means that once the gas has reacted with all of the surface, it will not react anymore and the sample will have grown exactly one monolayer of the desired element. The gas is then purged from the chamber, and the next gas is introduced after the chamber is devoid of gas again. This process loops, so essentially one layer of atoms every is grown every time a gas is pumped into the chamber. It is very common to rinse with water between every pulse of gas because the precursors cannot always react with each other directly but need a reaction with water in between[33].

The ALD process can be divided into four different stages. First, the introduction of the precursors into the chamber. The precursors react to the surface of the sample. A vital property is that the precursor gas does not react with itself in the gas phase or with other precursor units already on the sample. This leaves a single monolayer of the precursor on the sample. The second stage is the purge of the precursor gas. This is done after a specific amount of time when the gas has had enough time to form a monolayer on the substrate. The remaining gas is then vented out of the chamber, leaving the chamber once again in vacuum. The third stage is the introduction of the co-reactant. This is a element that will react to the the active seats of the precursor on the sample. When this reaction is complete, only the desired element will be left on the sample. The fourth step is the purge of the co-reactant. Just like the second step, the chamber is vented and left in vacuum once again. This cycle then repeated to create a very controlled layer of desired elements.

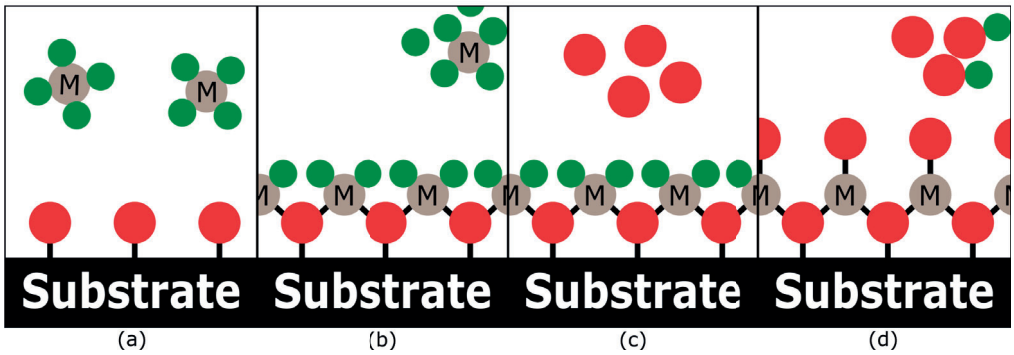


Figure 3.6: Illustration of one cycle from an ALD. The precursor has is introduced to the chamber and reacts with the substrate surface (a) and a complete reaction occurs so the surface can no longer react with the precursor (b). The excess gas is removed from the chamber. The co-reactant is then introduced into the chamber (c), reacting with the active groups of the precursor molecules on the surface. The gas remaining of the co-reactant and the bi-products are removed from the chamber (d) and a single monolayer of the metal has been formed.

The ALD machines of today can generally be separated into two different kinds. These two are called thermal ALD and plasma ALD. The key difference between these two is the temperatures at which they can operate. Since the ALD is used in a lot of semiconductor areas, the temperature can be of most importance, as semiconductors can be sensitive to high temperatures. This can be done with a plasma ALD instead of a thermal one[34]. The difference between how they work is in how they react with the precursors deposited on the sample. Thermal ALD typically uses H_2O as a co-reactant, which requires a high temperature for the reaction to take place. While in the plasma ALD, the co-reactor is plasma that is introduced into the chamber, commonly O_2 plasma. This plasma does not have to be as high temperature as the H_2O, and can also react faster. [35]

3.6.2 Temperature and purge time

As with most chemical reactions, there is a reaction that goes in the ”other way” compared to the desired reaction. In this case, the counter reaction would be if the deposited element were removed from the sample surface. This happens to some degree, and as with most reactions it is sped up by higher temperatures. Therefore it is a bit of trial and error to find good temperatures for growing homogeneous films with ALD. The key reaction has to occur at a high rate but you don’t want the deposited elements to evaporate from the surface too quickly.

Typically when discussing temperature for an ALD process, there is a common term called ”processing window”. This is the range of temperature where the growth is independent of the deposition temperature[4], and is shown in Fig. 3.7. As can be seen in the figure, if the temperature is too low, there will probably be some incomplete reaction, leading to a lower growth rate. Another problem that can occur is condensation of the deposited gas. This will leave flakes of the precursor on top of the sample, leading to sporadic places where the film is much thicker. On the other hand if the temperature is too high, the deposited precursor has a higher chance of re-evaporating, meaning the surface might not be fully reacted by the end[4].

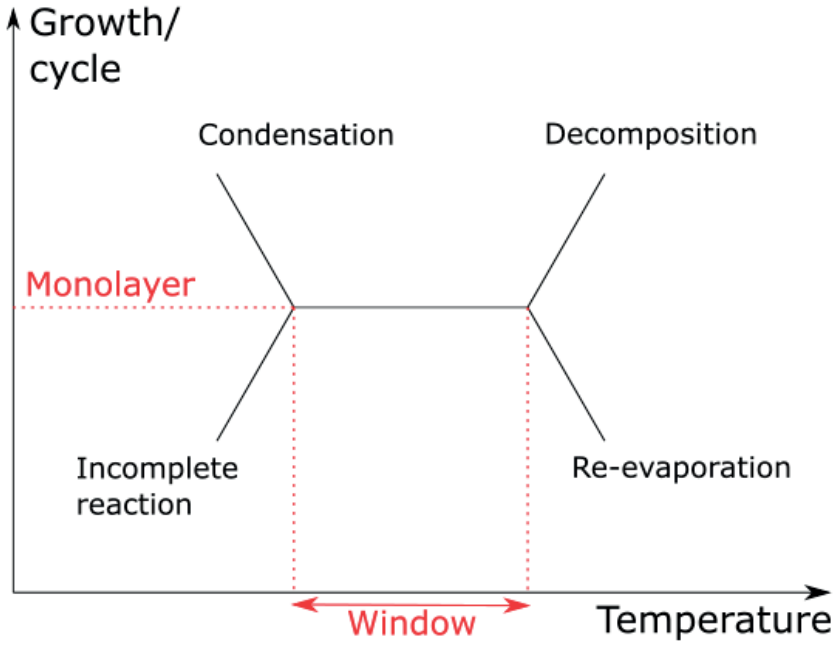


Figure 3.7: A temperature and growth rate graph showing the processing window for a general ALD process, illustrated from [4]

3.7 Annealing

When the HZO has been deposited, the material is in an amorphous phase. Here the ferroelectric property hasn’t been made yet because the ferroelectricity comes from the slight isometrically in the crystal matrix. To crystallize the HZO, the sample needs to be heated to higher temperatures. Around 400 degrees °C should be enough [36] to crystallize the HZO. To make sure the crystal lattice

exhibits the ferroelectric properties, a certain noncentrosymmetric orthorhombic phase seems is believed to be the root. This phase is called $Pca2_1$ and a strain has to be introduced during the annealing to achieve. This can be done by applying titanium nitrite (TiN) contacts on the top and bottom electrodes on the sample before the annealing. It is also important that the TiN has a $< 111 >$ orientation to induce this strain. [37]

3.8 Sputtering

Sputtering is a common method of depositing thin layers of material on samples. It is in a class of deposition techniques called physical vapor deposition[38]. The material and the sample are both inside of a chamber, which is in high vacuum [39]. Sputtering is done by bombarding the material which is to be deposited with ions to produce vapor. This vapor then travels through a vacuum and deposits on top of the sample[39]. An illustration of how sputtering works can be seen in figure 3.8

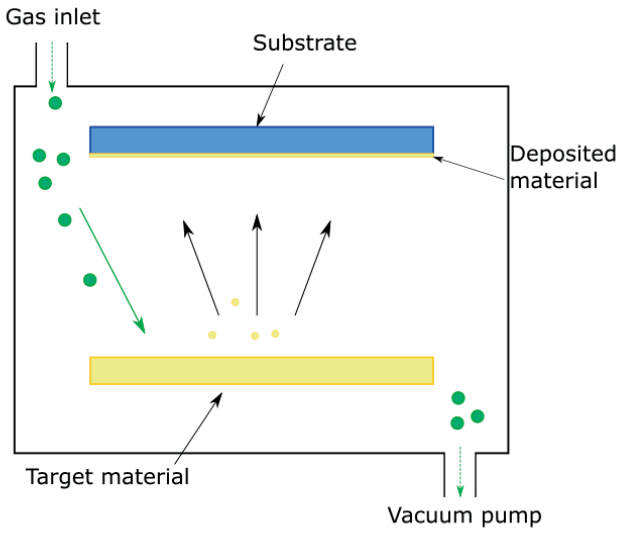


Figure 3.8: An illustration of a sputtering chamber. The ions are introduced in the gas inlet and are accelerated towards the target material by an applied bias. The material vaporizes and is deposited on the substrate above. Illustration is based of [5][6]

3.9 Ellipsometer

An ellipsometer is a tool that utilizes phase-shifts from light being reflected from materials. This measurement is done by polarizing incident light, which then reflects of the surface. The light is then re-polarized and the intensity is measured. An illustration of how an ellipsometer typically is designed is showed in Fig. 3.9

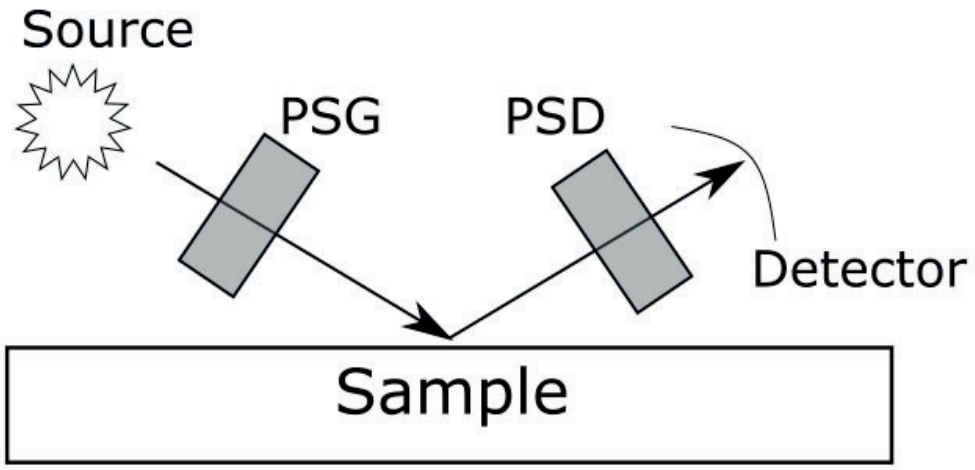


Figure 3.9: Illustration of a typical ellipsometer. PSG stands for polarization state generator and the PSD is the polarization state detector. Illustrated from [7]

The phase shift can give information about how thick a sample is. To do this, the machine must be fed a model of how the sample is composed (what kind of elements exist in each layer). From previous measurements, the machine is taught how different elements shift the light at different wavelengths [40]. The machine then compares the phase shift at different frequencies to the already known model and calculates the thickness of a wanted material. By measuring several points on the sample, an idea can be formed about how homogeneous the samples have grown.

An ellipsometer is capable of measuring more than just the thickness of a sample, but in this work it was the machines primary purpose.

Chapter 4

Processing

4.1 Preparation of samples

The material used for the substrate in this project was Si-wafers. The wafer is n-doped with a crystal orientation of $< 100 >$. The resistivity of the wafer is 1-10 Ω cm. Usually III-IV semiconductors are very popular to work with in Lund due to their high electron mobility but since this work focuses more on the oxide it seemed unnecessary. The Si-wafers were then coated with 10 nm TiN. This was done with the machine ”AJA Orion 5”. The TiN is applied to make sure the HZO can be strained, which is a necessity for the ferroelectric properties. It also enables the HZO to crystallize . This TiN Si-wafer were then broken down into smaller pieces to make it easier to manage. These pieces were approximately square with sides of 1 cm. To break the wafer down into smaller squares, a diamond pen was used. This is common practice when preparing simpler samples in Lund Nano Lab.

4.2 ALD

After the Si-substrate had been prepared the fabrication of the ferroelectric films could be started. The ALD that was used was a Picosun Sunale R-100 ALD machine. This ALD is a thermal one, which means that the oxidation occurs by the addition of water and not by using ionized ozone. The Picosun ALD uses two precursors to deposit the hafnium and zirconium. The two precursors are called TDMAHf (Tetrakis(dimethylamido)hafnium) and
TEMAZr (Tetrakis(ethylmethylamido)zirconium). These gases can have different adjustable temperatures for when they are introduced into the ALD reactor. The machine also comes equipped with a water source to oxidize the precursors when they have reacted with the sample surface.

The point of the work done in this project was to analyse how different temperatures and purge times would affect the deposited films and its electrical abilities. Therefore, a standard recipe was made where only two variables were changed. The settings for the ALD can be seen in the tables 4.1 and 4.2 below. The settings for 4.1 were already set, the reason for adding them is if these test are to be reporduced.

Settings	
Chamber Temperature	Variable
Intermediate Space	350 sccm
Flush Reaction Space	3 times

Table 4.1: First page of settings for the ALD process

Setting	TEMAZr	TDMAHf	H_2O
Precursor Temperature	110 °C	100 °C	28 °C
Carrier Gas	150 sccm	80 sccm	150 sccm
Pulse Time	1.6 s	1.6 s	0.1 s
Purge Time	5.0 s	5.0 s	Variable

Table 4.2: Second page of settings for the ALD process

The TiN samples were placed on top of a 2-inch silicon wafer. By doing it this way the HZO can be deposited on top of the TiN substrate for measurement while at the same time being able to measure the growth rate on the 2-inch wafer. Doing it like this might cause some amount of turbulence in the gas flow of the chamber due to the surface being uneven. This turbulence was deemed small enough to be negligible. Another side effect of doing it this way is that the TiN samples ”shadows” the ALD growth on the 2-inch wafer, meaning thickness measurements on the center of the wafer won't be accurate.

4.3 First and second batch

The samples were done in two different batches. Before the first batch, there was only theories about how the temperatures and purge times could affect the properties of the samples. The first batch consisted of five different samples with different parameters on the ALD. A table for the first samples can be seen in 4.3.

	10s	20s	40s
200 °C	x		
150 °C	x		
125 °C	x	x	x

Table 4.3: Samples done in the first batch of processing, where x marks which were made, the x-axis marks the purge time and the y-axis marks the chamber temperature

After analysing the first batch, it was decided that a second batch was to be made to confirm new theories about the effects of the parameters. These samples were all done with a purge time of 20 seconds and four different temperatures were tried. The specifications can be seen in Fig. 4.4

	10s	20s	40s
250 °C		x	
200 °C		x	
150 °C		x	
125 °C		x	

Table 4.4: Samples done in the second batch of processing, where x marks which were made, the x-axis marks the purge time and the y-axis marks the chamber temperature

Since there was one pair of parameters that were common for both batches, a certain amount of information about the variance of the process could be derived. The entire table for the samples from both batches can be seen in table 4.5.

	10s	20s	40s
250 °C		x	
200 °C	x	x	
150 °C	x	x	
125 °C	x	x2	x

Table 4.5: All the sample done in this work, where x marks which were made and x2 means two of this kind of sample were made, the x-axis marks the purge time and the y-axis marks the chamber temperature

4.4 Depositing the contacts

In the same manner as the TiN was applied before the oxide, another layer of TiN was applied on top of the oxide, enclosing the oxide between two layers of TiN.

After the deposition of the second TiN layer, the samples were annealed to crystallize the oxide. To be certain that the crystallization would take place, a large margin was used and the samples were heated to around 600 degrees.

The final step is to deposit the metal contact on top of the TiN. The first task was patterning using UV lithography. A negative resist was placed on the sample and was spun to form a thin layer. The sample was then baked to solidify the resist. The next task was to expose the resist to UV light under a mask. After this the samples were placed in the developer and then rinsed in water, removing the unwanted resist. Finally, using sputtering, 5 nm of Ti followed by 200 nm Au was deposited on the sample. Finally, the liftoff was done. By placing the samples in acetone, the remaining resist was removed along with the unwanted gold, titanium and titanium nitride. This leaves only the metal patterns that can be seen in Fig. 4.1.

Figure 4.1: Picture of the deposited metal pattern

Chapter 5

Measurement methods

5.1 Ellipsometer

The ellipsometer was used to measure the thickness of the samples. This was to compare the growth per cycle (GPC) between the samples and to make sure that no deposition was too out of line compared to the other ones. The measurements were done on the 2-inch wafers. Because there was no oxide in the middle of the sample, the measurements were done on the edges of the samples. The reason there was no oxide in the center is because an additional sample was placed on top of the 2-inch wafer to create the pieces that were actually measured.

5.2 Probing station

For electrical measurements on the samples a probing station and a electrical analyser was used. The probing station used was a ”Semi-auto probe station - TS200-SE” and the analyser was a ”Semiconductor device parameter analyser - B1500A”. There were two main measurements that needed to be done. The first one is an IV measurement to analyse the tunneling current and the breakthrough current. The second one is a PUND measurement. Since this is a high frequency measurement, a B1530A waveform generator/fast measurement unit (WGFMU) had to be attached. The PUND measurements were done to analyse the ferroelectric polarization.

The top side of the sample can be seen in Fig. 4.1. An illustration of the cross section can be seen in Fig. 5.1. In the first image Fig. 5.1(a), no voltage is applied to the contacts yet. In image 5.1(b), a large enough bias is applied on the probes that two conductive filaments are created in the oxide. Lastly in image 5.1(c), a bias is applied between one of the first contacts and the pad with a known

area. Since the first contact has a conductive filament and the substrate is fairly conductive, it can be assumed that almost all of the voltage drop is applied over the oxide in the center.

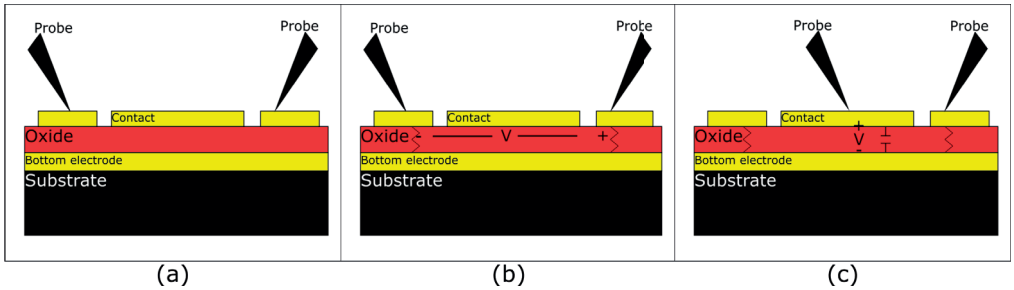


Figure 5.1: Illustration of the cross section of the sample. The sample starts of looking like in (a), and then a bias is applied over the probes (b) causing the oxide to form conductive filaments. One of the probes are moved to the main contact (c) and the measurement of the oxide can commence.

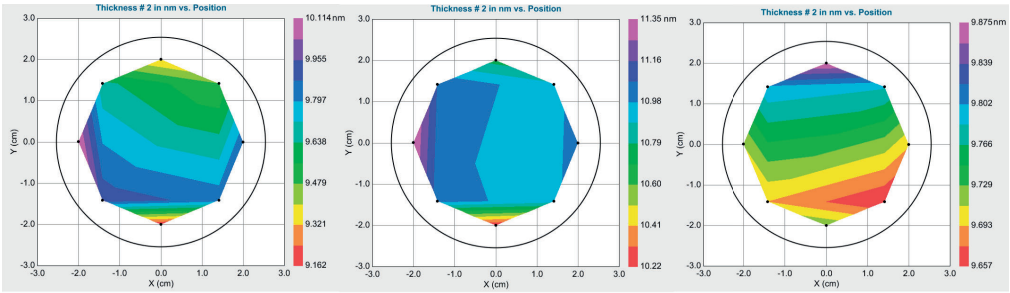
Chapter 6

Results

6.1 Ellipsometer images

All the samples made were exposed to 50 + 50 cycles for zirconium and hafnium respectively. The expected thickness should be around 9 nm when monolayer deposition is occurring. The accuracy of the ellipsometer is not as high as the values might suggest, but for simplicity they are left as is.

Below is three images from different temperatures from the first batch of the HZO films.



(a) (b) (c)

Figure 6.1: Thickness measurements of HZO film, with 125 °C and 10 s purge time (a), 150 °C and 10 s purge time (b), 200 °C and 10 s purge time (c)

In Fig. 6.1a and 6.1b, the range of thickness looks very large when looking at the scale to the side. But both of these samples have two measured points that stick out a lot, at the bottom of the sample and at the left. This might be because of not having homogeneous growth but it might also be bad luck that some kind of particle was at the measured point. The measured range for the sample grown at 200 °C seems are much better, spanning only around 0.2 nm over the entire wafer.

The average thickness does not seem to follow a clear trend from these three measurements. The thickest one is the 150 °C sample, followed by 125 °C and the thinnest one is the 200 °C sample. The expected growth rate of the HZO is slightly below 1 Å / cycle. With 100 cycles, the expected thickness is less than 10 nm, which only seems correct for the 200 °C sample.

The next three pictures are also from the same batch but all at 125 °C while the purge time is being changed between the samples.

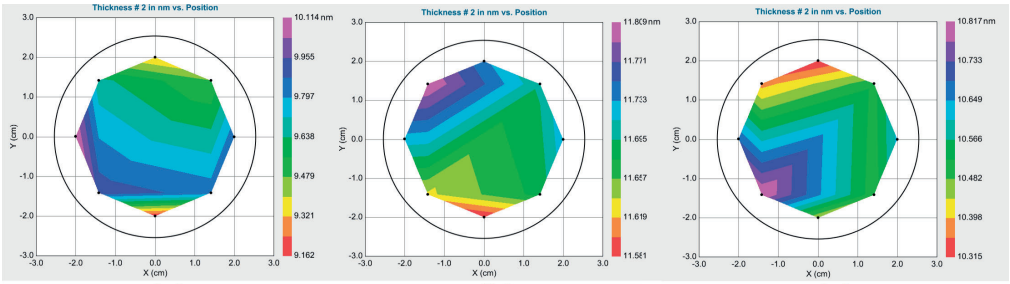


Figure 6.2: Thickness measurements of HZO film grown in 125 °C and 10 s purge time (a), 125 °C and 20 s purge time (b), 125 °C and 40 s purge time (c)

Worth noting is that Fig. 6.1(a) and 6.2(a) are the same picture, it is just easier to compare the trends in variance for different temperatures and purge times when they are placed like this.

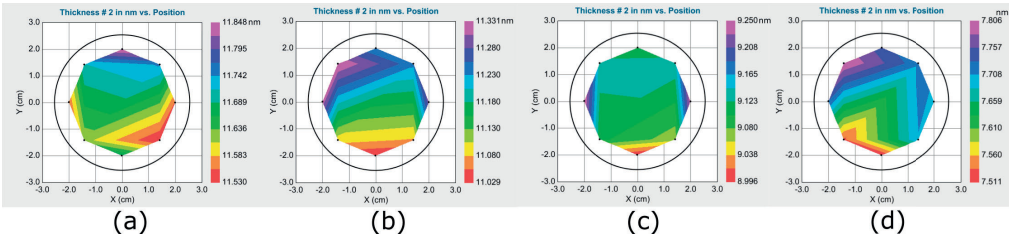


Figure 6.3: Thickness measurements of HZO film grown in 125 °C and 20 s purge time (a), 150 °C and 20 s purge time (b), 200 °C and 20 s purge time (c), 250 °C and 20 s purge time (d)

The different average thickness of the different sample can be seen in table, alongside the diference between the largest and thinnest point of the sample. 6.1.

	10s	20s	40s
250 °C		7.7 ± 0.3 nm	
200 °C	9.8 ± 0.2 nm	9.1 ± 0.3 nm	
150 °C	10.8 ± 1.1 nm	11.2 ± 0.3 nm	
125 °C	9.6 ± 1.0 nm	11.7 ± 0.2 nm	10.6 ± 0.5 nm

Table 6.1: Average thickness of the different samples, where the x-axis marks the purge time and the y-axis marks the chamber temperature

The data says that higher temperature results generally in lower growth rate. The highest growth rate occurs at 125 °C with 20 s purge time. The main speculation as to why the growth would be slower for higher temperatures is because the films might evaporate after being deposited. A trend should also be seen that higher purge times should result in the same thickness or thinner according to Fig. 3.7, because there is more time where the sample is hot when the deposited material could evaporate. This effect can perhaps be seen in 200 °C, where the 20s purge time film seems to be thinner than the 10s purge time. The same effect is not seen in 150 °C and 125 °C. A reason why this might be is because the 10s purge time is too short and there isn't enough time for the water to react to all the precursors on the surface. This would result in the next pulse of precursors not being able to react to these parts of the sample, lowering the growth rate.

However the 125 °C samples seems to have a maximum growth rate at 20s and lower growth rate at 40s. This might be a combination of the both the previous reasons mentioned. The explanation would then be that the 10s purge time doesn't allow full oxidation of the surface because it's too little time. While the 40s purge time would be too much time, as there would be an increase of evaporation because of the long time the sample spends in the hot chamber.

Finding any definitive trends in the thickness difference is difficult. Two samples stick out a lot more that the other though, and that is 150 °C and 125 °C with 10s purge times. They both have a lot more thickness difference compared to the other samples. This unstable growth is probably due to too low temperature and not having longer purge time to compensate. This can make some patches of the sample not being able to be oxidized after deposition, meaning the next pulse wont react with the surface. This in turn makes the patches not being oxidized grow slower than the surrounding surface, contributing to the variance in thickness. Since there were only eight measurement points, it is hard to tell if there are clear gradients or if there are local contamination on the samples.

6.2 IV measurements

To get a good full view of how the samples relate to each other, all five samples IV curves for 10 μm capacitors have been plotted in Fig. 6.4.

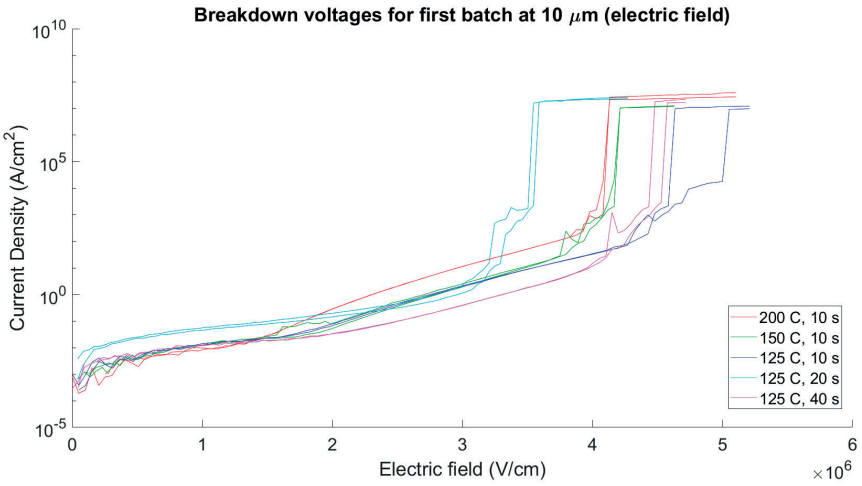


Figure 6.4: IV curve for first batch of HZO for 10 μm capacitors, each capacitor size was measured with two devices, hence two curves for every sample.

Generally what is wanted from the HZO films Iv-curve is a high breakdown voltage. This makes it possible for the film to be used at higher voltages, which is generally a good feature for electronics. Surprisingly enough, the 200 C, 10s purge time samples were the samples with the lowest breakdown voltages. This process was assumed previous to this work to be one of the better settings for this machine. The best samples in terms of breakdown voltages seems to be 125 °C with 10s and 40s purge times.

The second batch was measured before and after annealing to compare the effects in the IV measurements. The pre-anneal breakdown voltage for the second batch can be seen in Fig. 6.5.

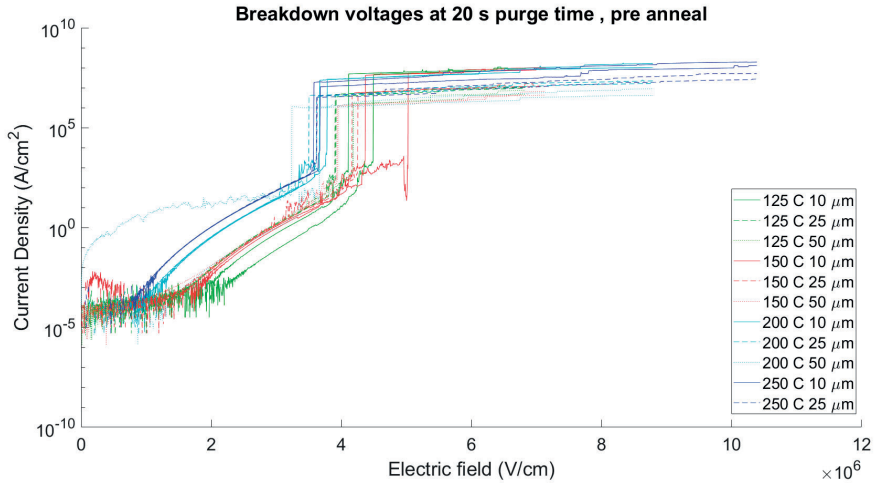


Figure 6.5: IV curve for the second batch of HZO before anneal, each capacitor size was measured with two devices, hence two curves for every sample.

The IV measurements for the second batch after the samples had been annealed can be seen in Fig. 6.6.

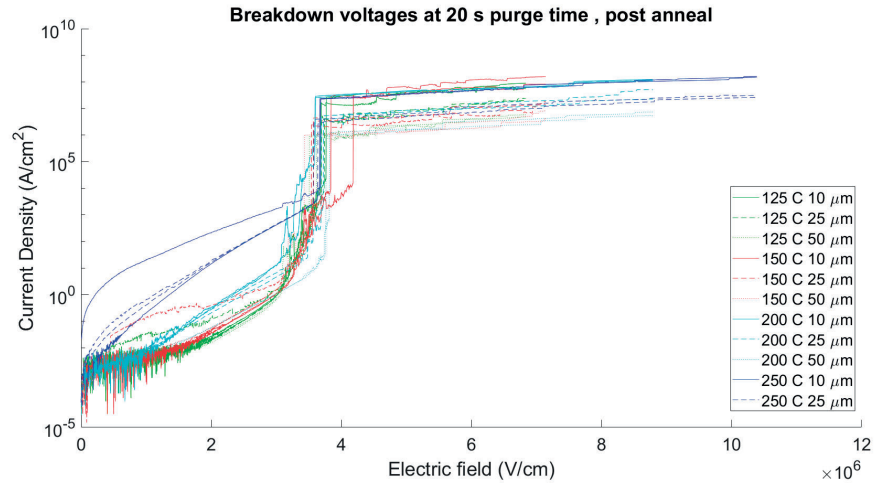


Figure 6.6: IV curve for the second batch of HZO after anneal, each capacitor size was measured with two devices, hence two curves for every sample.

The average breakdown voltages for the samples can also be seen in table 6.2

	10s	20s	40s
250 °C	2.8± 0.05 V		
200 °C	4.0± 0.05 V	3.4± 0.1 V	
150 °C	4.5± 0.2 V	4.2± 0.5 V	
125 °C	4.4± 0.3 V	4.0 ± 0.15 V	4.7± 0.2 V

Table 6.2: Average breakdown voltages for the different samples, where the x-axis marks the purge time and the y-axis marks the chamber temperature

Even though the values form table 6.2 are averages for the different samples, there is still a large amount of difference between specific devices, even within the same processing metrics. Even so, a tendency can be seen where higher chamber temperature seems to make the breakdown voltage for the devices lower. And in general the breakdown voltage seems to be higher for shorter purge times, with the extreme exception for the 40 s purge time sample, which has the highest breakdown voltage of them all.

Another way to analyse the samples is to see how much current is leaking at a specific voltage. The voltage has to be lower than the lowest breakdown voltage, otherwise it would be hard to compare them. Table 6.3 shows the leakage current at 2 V for all the samples.

	10s	20s	40s
250 °C	185 A/cm		
200 °C	0.30 A/cm	0.40 A/cm	
150 °C	0.05 A/cm	0.09 A/cm	
125 °C	0.18 A/cm	0.018 A/cm	0.03 A/cm

Table 6.3: Average leakage currents for the different samples at 2 V applied, where the x-axis marks the purge time and the y-axis marks the chamber temperature

The current in the 250 °C sample is almost three orders of magnitude larger than the second largest leakage current that was tested, which can be seen in table 6.3. This isn't all too unexpected, as 2 V is very close to the 250 °C breakdown voltage of 2.8 V. And since the current increases exponentially this leakage current will be a lot larger than the others.

6.3 PUND measurements

In Fig. 6.7, the data from a PUND measurement can be seen.

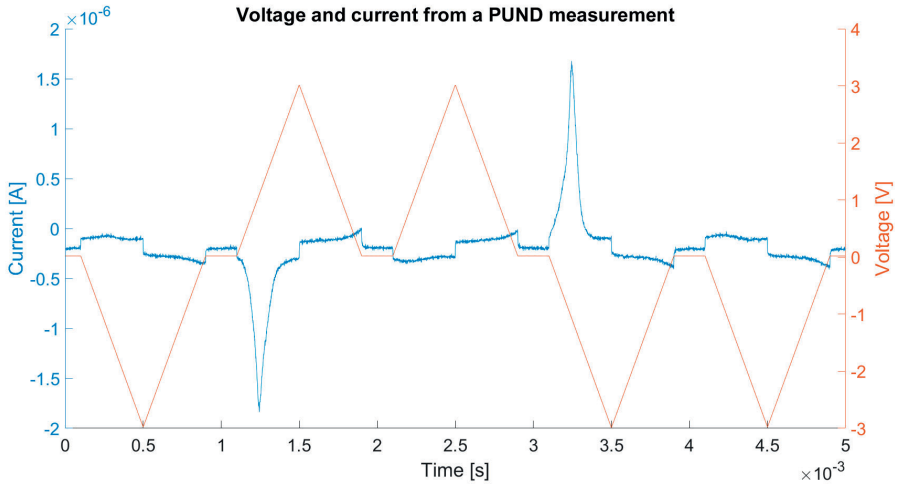


Figure 6.7: Voltage applied and current measured during a PUND measurement. The measurement was taken from a HZO sample done at 200 degree °C with 10 s purge time. The reason the current isn't zero when the applied voltage is zero is due to a problem in the probing station.

In Fig. 6.8, the switching from the PUND measurement can be seen. This is done by subtracting the current of the second positive voltage spike from the first in Fig. 6.7. The different capacitors have been normalized to their area, making them comparable to each other.

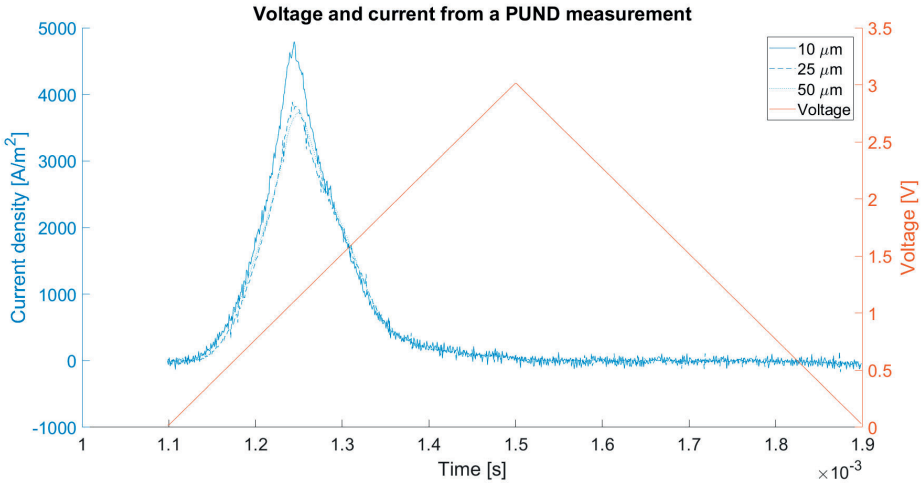


Figure 6.8: Switching current from HZO sample made at 200 degree °C with 10 s purge time

6.4 PE-curves

The data from the different PUND measurements have been compiled into two different PE-curve figures. The hysteresis loops from the first batch can be seen in Fig. 6.9 while the loops from the second batch can be seen in Fig. 6.10.

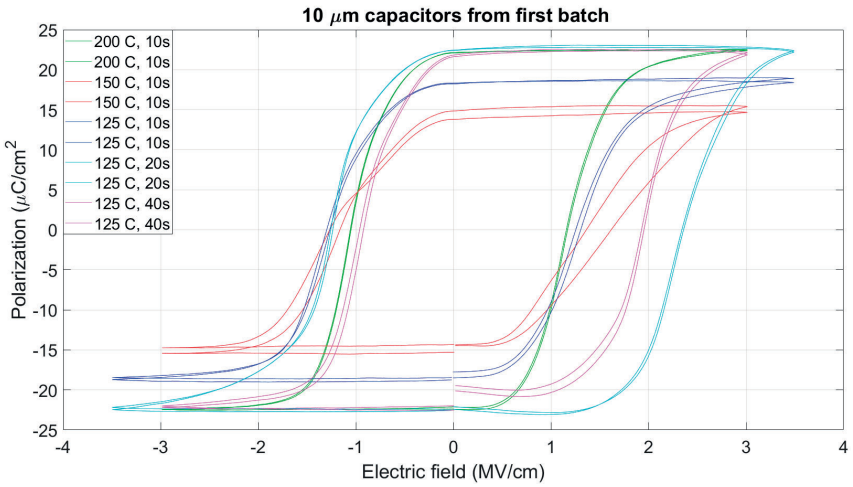


Figure 6.9: PE curve for all the samples made in the first batch. All data comes from capacitors with a radius of 10 μm.

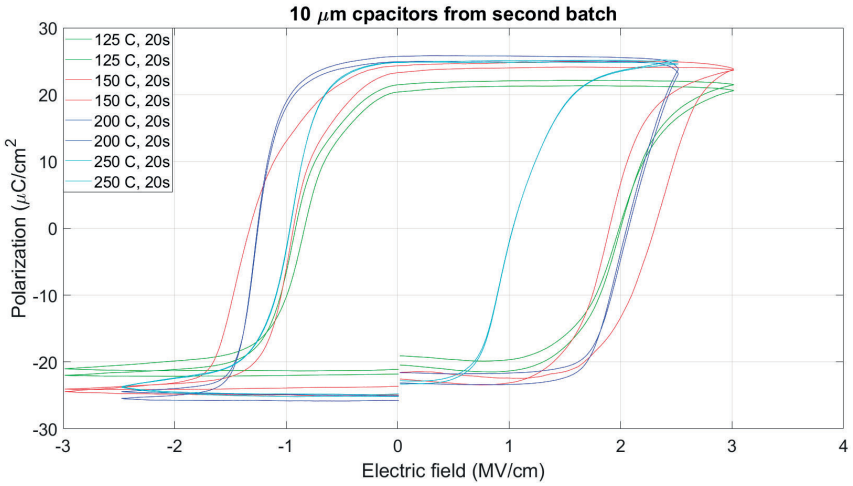


Figure 6.10: PE curve for all the samples made in the second batch. All data comes from capacitors with a radius of 10 μm.

One very noticeable thing about the PE curves is that all the samples look very good. The hysteresis loops are all visible, meaning they all inhabit ferroelectric properties. This is despite having a large shift in both processing temperature and purge time. In other words, the process of using ALD to create ferroelectric HZO films in the size of around 10 nm is very stable.

From all the PE-figures, the coercive field and the remnant polarization can be acquired for all the samples. In table 6.4, the average coercive field for all sizes of capacitors for each sample can be seen.

10 μm	10 s	20 s	40 s
250 °C		0.94 MV/cm	
200 °C	1.05 MV/cm	1.27 MV/cm	
150 °C	1.25 MV/cm	1.04 MV/cm	
125 °C	1.26 MV/cm	0.89 MV/cm	0.96 MV/cm

Table 6.4: Average coercive field for all samples, where the x-axis marks the purge time and the y-axis marks the chamber temperature

In table 6.5, the average remnant polarization can be seen.

10 μm	10 s	20 s	40 s
250 °C		16.0 $\mu C/cm^2$	
200 °C	20.9 $\mu C/cm^2$	26.6 $\mu C/cm^2$	
150 °C	15.3 $\mu C/cm^2$	21.9 $\mu C/cm^2$	
125 °C	17.8 $\mu C/cm^2$	19.3 $\mu C/cm^2$	20.1 $\mu C/cm^2$

Table 6.5: Average remnant polarization for all samples, where the x-axis marks the purge time and the y-axis marks the chamber temperature

6.5 Yield statistics

An important metric for the viability of processing is the consistency. When producing samples, as many of the devices on the sample as possible should be working. This was originally not intended to be analysed too much but during the measurements, it was discovered that some samples had far more non-working devices compared to other. Therefore, yield statistics were made for all the different samples. This was done by measuring 20 devices with 10μm radius and 20 devices with 50μm radius on each sample. Since the previous measurements have indicated that all devices that didn't leak showed ferroelectric properties, the yield measurement only consisted of a simple IV-sweep to check if the leak current was large before measurement. The yield measurements weren't done on all the samples. In tables 6.6 and 6.7 the yield in percent can be seen for the two diameters. The 250 degree sample proved to have very bad yield, hence why there is not a single 50μm capacitor that didn't leak, and over 20 10μm capacitors had to be measured to find two that actually worked.

10 μm	10 s	20 s	40 s
250 °C		5 %	
200 °C	85 %	90 %	
150 °C	90 %	80 %	
125 °C		85 %	

Table 6.6: Yield percentage for 10 μm devices, where the x-axis marks the purge time and the y-axis marks the chamber temperature

50 μm	10 s	20 s	40 s
250 °C		0 %	
200 °C	50 %	25 %	
150 °C	40 %	15 %	
125 °C		80 %	

Table 6.7: Yield percentage for 50 μm devices, where the x-axis marks the purge time and the y-axis marks the chamber temperature

What can be noticed clearly is that the yield is generally a lot higher for capacitors with a smaller area. This is probably because there is a certain concentration of defects in the films. If the capacitor area is large, there is a higher probability that there will be defects somewhere on the large area that form filaments in the oxide. This will lead to a leak-current that is unwanted.

A thing worth noting is that one contributing cause for the yield measurements was the 250 °C sample. It was not possible to find a single 50 μm device that was not leaking. This led to the hypothesis that higher temperatures could lead to an increase in defects and faulty devices. But in the tables, this does not seem to necessarily be the case. There are simply some processes which create generally less leaky devices, where the 125 degree °C case seems to create the highest yields.

6.6 Comparisons between batches

As mentioned earlier, there was one setting that was present in both batches. This was the samples with 125 °C chamber temperature and 20 s purge time for water. In table 6.8, the different measurements for the two different samples have been compared.

	First batch	Second batch
Thickness	11.70 nm	11.70 nm
Thickness variation	0.23 nm	0.32 nm
Breakdown voltage	4.29 V	4.02 V
Current at 2V	0.018 A/cm	0.060 A/cm
Coercive field	0.89 MV/cm	1.01 MV/cm
Remnant polarization	19.3 $\mu C/cm^2$	21.1 $\mu C/cm^2$

Table 6.8: Comparisons between first and second batch for 125 °C and 20 s purge time samples

The average thickness of both batches were incredibly close, meaning the physical growth of the oxide seems very stable. While the electric properties seem to differ a bit, the values for the coercive field and remnant polarization are fairly close for both batches. Overall, the batches are very similar in the properties, while there were a lot of room for human error to occur.

Chapter 7

Conclusion

In this work HZO films was processed by ALD and the significance of the different ALD parameters for the properties of the films were analysed. Drawing definitive trends from the data is a bit challenging because of a large amount of difference in the tests. One key thing to take away from this work is the stability of the ALD process that is being used. Despite varying the temperature and purge time by large quantities, the vast majority of the created devices exhibited ferroelectric properties. This is a very important property for industrial use of ALD deposition for ferroelectric materials, as stable processes ensure larger processing windows in terms of temperature. This makes the processes more compatible with other processess and materials.

Since there were no definitive trends that could be read from the materials, further testing is incentivized. Different temperatures and purge times could be explored to further prove current theories about the behaviour of ALD deposition of HZO.

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