Master Thesis

Temperature Dependent Electrical Characterisation of Vertical InAs-InGaAs Nanowire MOSFETs

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Abstract

This thesis presents the temperature dependence of InGaAs Nanowire (NW) metal-oxide-semiconductor field-effect transistors (MOSFETs) grown at two different temperatures. The two different growths represent one sample having nanowires which have a mixed crystal structure (showing stacking faults) and one sample with nanowires of pure crystal structure (without stacking faults). The sample with a pure crystal structure was grown at a higher temperature. Both Direct current (DC) and Low-frequency (LF) noise measurements were made on the best devices on the two samples. The DC measurements were made at temperatures ranging from a room temperature of 293 K to a cryogenic temperature of 14 K. The DC characteristics at room temperature show maximum transconductance of $1.4\, mS/\mu m$ and a SS of $85\, mV/dec$ for the sample with stacking faults and $0.8\, mS/\mu m$ and $90\, mV/dec$ for the sample without. At 14 K the SS went down to $12\, mV/dec$ and $16\, mV/dec$ correspondingly. The LF noise characterization was made at room temperature as well as at a cryogenic temperature of 14 K. The dominant noise source for both samples at room temperature is number fluctuations. The minimum trap density at 10 Hz for the sample with stacking faults was $N_{bt} = 6 \cdot 10^{18} cm^{-3} eV^{-1}$ and $1.2 \cdot 10^{19} cm^{-3} eV^{-1}$ for the sample without. Measurements made at the cryogenic temperature showed implications of mobility fluctuations being the dominant noise source instead of number fluctuations. The Hooge parameter for the sample with stacking faults was independent of current and was calculated to $\alpha_H \sim 1 \cdot 10^{-4}$. For the sample without stacking faults the Hooge parameter varied with the current and was calculated between $\alpha_H \sim 7.3 \cdot 10^{-6}$ and $5 \cdot 10^{-4}$. This study does not give any implication that a mix in the crystal structure in InGaAs NW gives any down-grade in performance in terms of subthreshold swing and LF noise.

Acknowledgements

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List of Symbols and Acronyms

DC	Direct Current
DIBL	Drain Induced Barrier Lowering
DOS	Density Of States
EBL	Electron Beam Lithography
FinFet	Fin Field-Effect Transistor
GAA	Gate-All-Around
IC	Integrated Circuit
InAs	Indium Arsenide
InGaAs	Indium Gallium Arsenide
LF	Low Frequency
LFN	Low Frequency Noise
GR	Generation-Recombination
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOVPE	Metal-Organic Vapor-Phase Epitaxy
NW	Nano Wire
PSD	Power Spectral Density
RF	Radio Frequency
RT	Room Temperature
RTS	Random Telegraph Signal
SNR	Signal-To-Noise Ratio
TEM	Transmission Electron Micrograph
VLS	Vapor-Liquid-Solid
WZ	Wurtzite
ZB	Zincblende

Symbol	Unit	Meaning
α		Scattering Coefficient
α_H		Hooge parameter
β		Frequency Exponent
C_g	F	Gate Capacitance
C_{ox}	F	Gate Oxide Capacitance
ε_0	F/m	Permittivity Of Free Space ≈ $8.854 \cdot 10^{-12}$
ε_r	F/m	Relative permittivity
f	Hz	Frequency
g_m	S	Transconductance
h	Js	Planck Constant ≈ $6.626 \cdot 10^{-34}$
I_D	A	Drain Current
k_B	$kgm^2\,K^{-1}s^{-2}$	Boltzmann Constant ≈ $1.381 \cdot 10^{-23}$
L_G	m	Gate Length
λ	m	Tunneling Attenuation Length
μ	$cm^2\,V^{-1}\,s^{-1}$	Carrier Mobility
μ_{eff}	$cm^2\,V^{-1}\,s^{-1}$	Effective Carrier Mobility
N_T	$cm^{-3}eV^{-1}$	Border Trap Density
Φ_B	V	Schottky barrier potential
q	C	Elemental Charge ≈ $1.602 \cdot 10^{-19}$

S_{I_D}	A^2/Hz	Drain Current Noise Power Spectral Density
$S_{V_{fb}}$		Flat Band Voltage Noise
S_{V_G}	V^2/Hz	Equivalent Gate Voltage Noise Power Spectral Density
SS	mV/decade	Subthreshold Swing
t	s	Time
T	K	Temperature
t_{ox}	m	Oxide Thickness
τ_0	s	Time Constant Effective Pre-Factor
V_D	V	Drain Voltage
V_{DS}	V	Drain-to-Source Voltage
V_{GS}	V	Gate Voltage
V_{TH}	V	Threshold Voltage
W_G	m	Gate Width

Chapter 1

1. Introduction

The aim of mankind has always been to constantly develop and push the limit of what is possible. The last decade the development has gone faster than ever before and society is becoming more and more integrated with electronics and computers. It is easy to forget that the first building block of modern electronics was first introduced less than a century ago. The MOSFETs are the key to making all computations in electrical circuits possible, hence it has been in every engineer's benefit to improve them. Since its origin there has been a lot of development of the transistor to make it faster, smaller and more energy efficient, without degrading its performance. But as the size of the transistor decreases, short channel effects start taking place which leads to a series of new issues, like increased power consumption due to increased leakage currents, or the gate having less control over the channel due to drain-induced barrier lowering (DIBL). Nowadays there is ongoing research on how to counteract these problems by changing the physical form of the transistors, trying out different materials as well as different ways of production.

This master thesis will examine and compare two samples of Vertical InAs-InGaAs Nanowire MOSFETs. The two samples are similar in design but were grown at different temperatures. One of the samples has stacking faults in the nanowires and the other sample which was grown at a higher temperature does not have any stacking faults. DC-measurements as well as LF noise measurements were done in order to fully get an understanding of the impact of the new growth. The thesis will examine the oxide quality in the high performance devices of the two samples and the effect of stacking faults on transistor characteristics. Chapter two will contain basic MOSFET theory needed for overall understanding as well as the concept of LF noise and stacking faults. Chapter three will go through the fabrication of the sample. Chapter four will contain the experimental setup and the method used for the measurements. Chapter five will show the results and analysis of the thesis and chapter six will conclude the work.

Chapter 2

2. Theory

This chapter will include the basics of the MOSFET to provide the reader with the proper knowledge to understand further concepts. The chapter will also go through theory of low frequency noise and the concept of stacking faults in the device.

2.1 MOSFET

2.1.1 History of MOSFET

The very first concept of a transistor was introduced as early as in the beginning of the 20:th century. These devices were not very reliable nor efficient so scientists experimented with other inventions to replace them with. Julius Edgar Lilienfeld was an Austro-Hungarian physicist and he was the first to come up with an idea of a replacement that would come to make a huge impact in the development of technology. He filed a patent in 1925 of a so-called field-effect transistor. However at that time there was not any proper knowledge of how to produce that kind of high quality devices and materials, especially semiconductors. For some decades, after a lot of research was done at Bell Labs on the subject of semiconductor devices, they were able to grow silicon dioxide on silicon wafers and could from that learn how the combination of them could be used to overcome the former problem of surface states which limited the performance. The surface states were found to be reduced at the semiconductor-oxide interface. The outcome of this realization was in 1959 that Mohamed Atalla and Dawon Kahng invented the metal oxide semiconductor field effect transistor known and well used as the MOSFET. The MOSFET made a great impact since it was more power efficient and had great scalability in relation to the bipolar junction transistor which was invented some years earlier. The MOSFET opened paths to a new era of technology with the possibility of high density integrated circuits.

2.1.2 MOSFET operation

A MOSFET is based on the principles of the MOS capacitor. It is constructed by a body and three terminals: source, drain and gate. The main purpose of a MOSFET is to control the current flowing through it from drain to source by a bias that is put on the gate terminal. Its function is to work as a

switch. The classical structure of the n-type bulk MOSFET can be seen in Figure 2.1. The substrate will then be of a p-type semiconductor material while the source and drain will be heavily doped n-type. This creates two pn-junctions, which can be seen in both Figure 2.1(a) and in the band energy diagrams of Figure 2.1(b). The most common substrate used throughout the years is silicon (Si), together with silicon dioxide (SiO_2) as gate dielectric. Other substrate materials can be used as well, e.g. germanium (Ge) and indium gallium arsenide (InGaAs). The major benefits of silicon is its availability as well as its strong native oxide which enables for a high quality interface with low density of traps. The trap states will be further explained in section 2.2. The gate oxide/dielectric serves as an insulator between gate electrode and semiconductor. The gate oxide is a crucial part of the MOSFET as to not have any gate leakage of electrons making its way from the channel to the gate. There is though commonly always some amount of gate leakage present, but the magnitude of the gate leakage is often far from the magnitude of the drain current which makes it irrelevant. However the thickness of the gate dielectric has been reduced in proportion to the continuous scaling of MOSFET dimensions. If the dielectric is too thin it will no longer hinder electrons from tunneling to the gate. This causes higher power consumption as well as poorer gate control. The oxide capacitance can shortly be described as

$$C_{ox} = \frac{\kappa \varepsilon_0 A}{t_{ox}} \tag{2.1}$$

where t_{ox} is the thickness of the oxide, ε_0 is the vacuum permittivity, A is the area and κ is defined as the relative permittivity of the gate oxide. It is then seen that the oxide capacitance can increase both through a decrease in the oxide thickness as well as an increase of the relative permittivity. By finding dielectrics with high permittivity it is possible to scale the gate length while having the same gate oxide thickness. Recently it has been popular to use high-κ dielectric which has several times higher relative permittivity than SiO_2. Such a material which has caught new interest is hafnium dioxide (HfO_2).

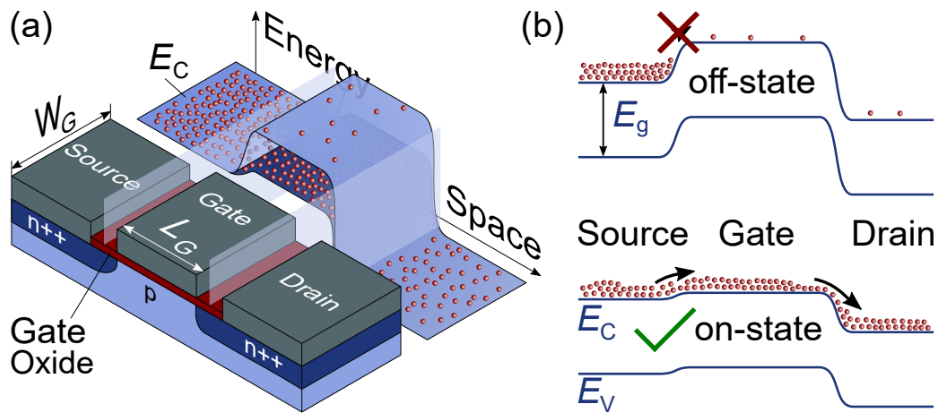

Figure 2.1 (a) The structure of a classical planar MOSFET together with (b) band energy diagrams for OFF- and ON state. Figure taken from [1].

If a positive voltage is put on the drain as the substrate and source is grounded there will be no currents flowing between the drain and source as long as the voltage over the gate is kept at zero. The MOSFET will then be turned OFF and only very small reverse leakage currents may be present. When studying the band diagrams in Figure 2.1(b) it can be seen in the off-state that a positive bias on the drain would only lower the drain side with very little or no effect on the channel current. However a very large drain bias, mainly in short channel MOSFETs, could affect the channel by so-called drain induced barrier lowering (DIBL). DIBL is a short-channel effect which causes a reduction in the threshold voltage. The physical origin of DIBL is the increase of the depletion region on the drain side which consequently decreases the channel length and gate potential barrier.

To turn the MOSFET ON, a bias is needed to be applied to the gate. This will affect the region near the surface of the gate dielectric and between the source and drain. In the n-type case, holes will be pushed away from the region near the dielectric interface and further into the p-doped substrate, making it depleted of holes. There will then only be acceptor atoms with bounded electrons left in the depletion region since the capacitance in the MOS structure only affects the free charge carriers in the semiconductor. The depth of the depletion region is related to the doping of the substrate and to the gate voltage. If the gate voltage is increased enough the depleted region becomes an inversion layer which acts as the channel of the MOSFET. This is due to the electrons in the highly n-doped source and drain being attracted to the positive potential put on the gate. The former p-type top region has then become an n-type channel which is controlled by the gate bias, hence the name inversion mode. The difference between gate- and surface potential sets the thickness of the channel. The ideal case would be to be able to switch

between the OFF and ON-state abruptly and to have OFF-currents that are zero. Unfortunately this is not the case in reality, the OFF-currents are not zero and the current is modulated over an interval of gate voltages.

To this point only the influence of the gate bias has been explained, showing the relation between carrier concentrations below and above threshold in the channel. In this case the drain bias has only been said to be positive, but depending on the drain voltage the transistor can either work in the linear- or saturation mode. The current will at the beginning increase with increased drain bias but at a certain voltage, the saturation voltage, the current will not further increase in the same manner. The pinch-off point is at a drain voltage equal to the saturation voltage. This means that the channel is pinched off at the drain side and the current will thus saturate. This is explained by the function of the channel thickness described previously. The function of the channel thickness is the difference in gate- and surface potential. By applying a bias at the drain(increasing the potential at that point) the difference in potential between gate and surface will then decrease near the drain, making the channel thinner. With high enough applied drain bias the channel near the drain will be completely pinched off. It is said that the drain-gate voltage is at threshold voltage and that the local density of the inversion charge is close to zero. The length of the pinch-off region will not increase dramatically with the drain voltage but remain fairly constant, as will the current flowing through the remaining channel. Even though the channel is pinched off the current can still be transported from the strong inversion channel to the drain by the strong electric field across it. For the linear case the drain voltage is less than the saturation voltage and the current can be described as

$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_G - V_{TH})V_D - \frac{1}{2}V_D\right] \tag{2.2}$$

Where L is the gate length (m), W is the gate width (m), V_G is the gate voltage (V), V_{TH} is the threshold voltage (V), μ is the carrier mobility in the channel ($m^2V^{-1}s^{-1}$) and C_{ox} is the gate capacitance (Fm^{-2}). In the saturation region the drain voltage is above saturation voltage and the current can then described as

$$I_{D, sat} = \mu C_{ox} \frac{W}{2L}(V_G - V_{TH})^2 \tag{2.3}$$

The expression is derived from Eq. (2.2) by inserting the saturation voltage, which is defined as $V_{D, sat} = V_G - V_{TH}$. In the case where the gate voltage is below threshold, the so-called subthreshold

region, the drain current will depend exponentially on the gate voltage. The current is proportional by the following expression

$$I_D \sim exp(\frac{q(V_G - V_{TH})}{k_B T}), \quad (2.4)$$

Where T is the temperature in Kelvin and k_B is the Boltzmann constant ($m^2kgs^{-2}K^{-1}$).

These expressions for the drain current are accurate for long channel MOSFETs. However for short channel MOSFETs the drift velocity for the carriers tends to saturate. At a given drain bias the electric field along a short channel will be greater than for a long channel. The explanation for the velocity saturation is that higher electric fields result in higher drift velocity of charge carriers. Charge carriers that hold high kinetic energy have an increased probability to scatter, mainly caused by optical phonon emissions [10]. The high scattering rate leads to a saturation in the velocity. The drift velocity can saturate in long channel MOSFETs as well if the electric field along the channel is high enough. The expression for the drain current in the saturation regime for short channel MOSFETs can be described by

$$I_{D,\,sat} = WC_{ox}v_{sat}(V_G - V_{TH}) \quad (2.5)$$

where v_{sat} is the saturation carrier drift velocity.

An important parameter that describes the relation between drain current and gate voltage is the transconductance g_m, see Figure 2.2(a). It is defined as

$$g_m = \frac{dI_D}{dV_G} \quad (2.6)$$

at a constant drain bias. The transconductance is normalized to the gate width and is ideally as high as possible. The transconductance is a measure of how sensitive the current is to a change in gate voltage. It is also the parameter that corresponds to the gain of the transistor. Two other important metrics can be found in the output characteristics of the transistor, the on-resistance R_{on} as well as the output conductance g_d , see Figure 2.2(b). The output conductance describes how well the drain voltage modulates the potential in the channel and thus the rate of change in current. The on-resistance takes its physical form as

a combination of the resistance in the channel and the contacts and series resistances of the source and drain. In the ideal case, both the output conductance and the on-resistance would be zero.

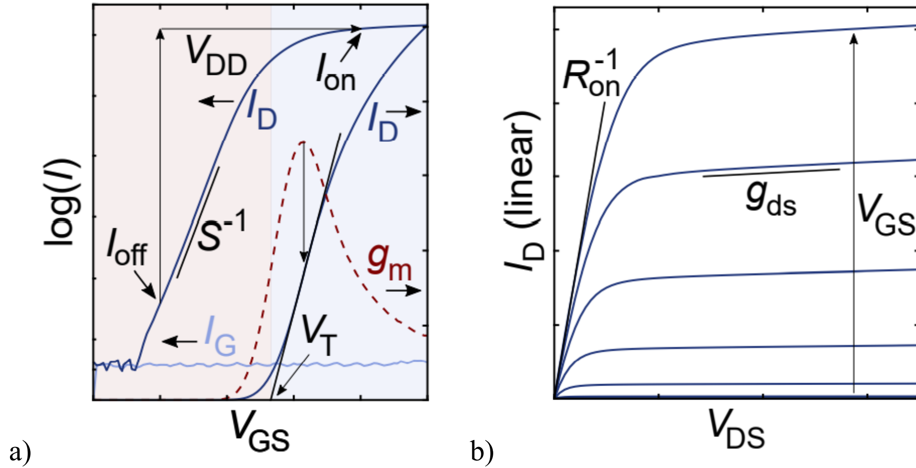

Figure 2.2 (a) Transfer characteristics. Drain current vs gate voltage. (b) Output characteristics. Drain current vs drain voltage. Figure taken from [1].

As discussed above, the optimal transistor is supposed to be abruptly switched between ON and OFF state. This is not the case in reality and the parameter which describes how fast the current changes with gate voltage below threshold is the inverse subthreshold slope

$$SS = ln(10)\frac{dV_G}{d[ln(I_D)]} \tag{2.7}$$

The inverse subthreshold slope is often referred to as the subthreshold swing (*SS*). The subthreshold swing can be seen in Figure 2.2(a) as the slope of the drain current as a function of the gate voltage before threshold in the logarithmic scale. The subthreshold swing is connected to temperature and will have a corresponding minimum value for each, due to the shape of the Fermi distribution of the source. For room temperature the minimum value is 60 mV/dec. The subthreshold swing can be written as

$$SS = ln(10)\frac{k_B T}{q} \tag{2.8}$$

This shows the linear dependence of the temperature. In theory the *SS* would then go to zero as the temperature does, but in reality the slope near a few Kelvin will flatten out and reach a minimum instead

of zero, see Figure 2.3. This is explained by the carrier density in the conduction band. The carrier density is dependent on the conduction band energy, Fermi-dirac distribution, density of states (DOS) and the characteristic decay of the exponential band tail. For low temperatures where the thermal energy is smaller than the band tail the *SS* becomes independent of the temperature and follows the decay of the band tail. For high temperatures the band tail is negligible and the *SS* follows the Boltzmann linear trend instead. This explains the saturation of the *SS* at low temperatures and that it is not possible to obtain a $SS \rightarrow 0$ in the presence of a band tail. The physical interpretation of the band tail was previously thought to explicitly originate from extrinsic mechanisms like crystalline disorders, strain and residual impurities. However it has later been found that it rather originates from intrinsic mechanisms like scattering, finite crystalline periodicities and particle interactions (electron-electron, electron-hole) [3].

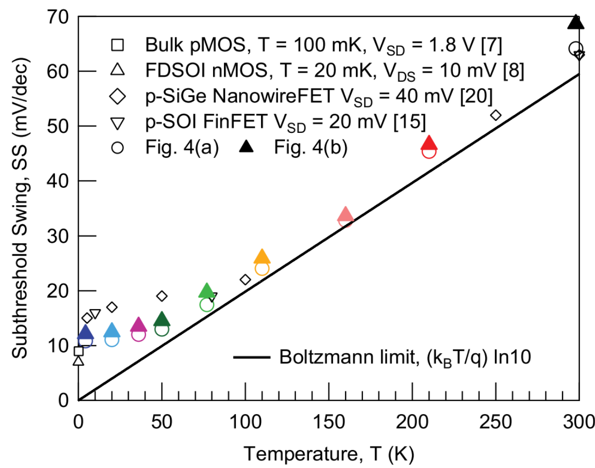

Figure 2.3. Subthreshold swing as a function of temperature. The subthreshold swing saturates at a certain temperature. The temperature for which the saturation occurs depends on technology. Figure taken from [3].

As discussed previously the threshold voltage is often defined as the voltage point where inversion is made and thus the creation of a channel between source and drain. However the threshold voltage can also be defined through the linear extrapolation of the maximum value of the transconductance in the transfer curve to the point of zero drain current.

2.1.3 Limitations of planar MOSFETs

To make the computations of the IC's faster it is in one's interest to integrate more transistors in the same device area as well as making the switching faster. The solution to this is to scale the transistors. By scaling the gate length of the transistor and other dimensions by the same amount, transistor performance will improve in switching speed, power dissipation and power delay product. Scaling results in a

reduction of power supply as well as threshold voltage. Through the years the main focus has been to keep scaling the transistors. A well known "law" stated by Gordon Moore in 1965 is that every two years the density of transistors in IC's is doubled. It is not an actual law of physics but an observation that has been surprisingly accurate and followed as a guideline or goal for developers and researchers since his statement. It has however been hard to keep up with Moore's law the last decade. The era of traditional scaling of the bulk MOSFET has come to an end. The gate length and the dimensions of the transistor has become so small that the electrostatic behavior and properties of it are no longer the same. So called short-channel effects are introduced, degrading transistor performance. The short channel effects are prominent at gate lengths of 15-20 nm. The major short channel effect is leakage, both through channel and gate(from gate oxide scaling). The leakage results in higher power consumption which counters one of the actual goals with scaling. It has therefore been required to find new possibilities to further improve device performance. Researchers and engineers are today working on integrating and combining different materials and whole new geometries of the devices. FinFETs and nanowire transistors are good candidates for new geometries. Nanowire transistors use the principle of a gate-all-around (GAA) which improves the electrostatic control of the channel and thus overcomes the short channel effects.

Silicon has since the introduction of the MOSFET been a reliable semiconductor material for the substrate. It has though been seen that the switching of the MOSFET can be made even faster by the use of high carrier mobility materials, so called III-V materials. The improved transport properties in the channel increases the efficiency of the device by allowing lower drive voltages for operation without any demand on scaling the gate length. There is a direct connection between the carrier mobility and its mean free path in the channel. If the mean free path is long enough the device could enter what is known as the ballistic regime. It is referred to as an operation mode for which no scattering of charge carriers in the channel occurs. The charge carriers will thus maintain their injection velocity through the channel, which is not the case in diffusive transport. However III-V materials have a lower density of states in relation with Si due to the larger lattice constant which is connected to a smaller bandgap. A lower density of states leads to smaller currents. To achieve high currents, there is a trade off between having high density of states and high mobility in the channel.

It should also be noted that a very small bandgap which is connected to high mobility is also connected to a number of downgrades. These effects could arise from band-to-band tunneling (BTBT) and impact ionization due to a small bandgap at a bias which provides the charge carriers with large enough energy to trigger these effects. Both effects result in large and sudden fluctuations in the current which could break

the device. The impact ionization is an increase in current due to excitation and scattering of electrons in the conduction band while BTBT is an increase due to quantum tunneling over the bandgap itself.

An example of III-V material is InGaAs which has very good transport properties. One drawback of InGaAs is that it does not make a good interface with the corresponding III-V oxides, which leads to a poor gate oxide quality. The poor quality in the oxide takes form in trap states that arise from dangling bonds and point defects [9]. III-V materials have also in relation to Si a lower density of states. This results in a Fermi level which is closer to the conduction band and thus having more traps that are available for charge capture. So even if Si would have had a higher trap density it is not certain that they would generate any noise since they are not probed at the used gate biases. Additionally Si has a different band offset between channel and gate oxide which amplifies this effect. There are many on-going studies on the topic of decreasing the effect of the traps by e.g. shifting their energy level out of operation, which resembles the natural properties that Si has. It has been seen that the density of interface traps can be reduced by the use of thin layers which are put between the semiconductor and dielectric[10].

2.1.4 Nanowire MOSFETs

Today there is a high demand for technology which is power and cost efficient and shows good performance with a small footprint. The dimension of today's MOSFETs is on the atomic level and further traditional physical scaling is no longer possible without violating these demands. It has been of interest to find new semiconductor technologies to replace the traditional bulk and often silicon based MOSFET. A promising candidate is the nanowire structure which uses the concept of a gate-all-around (GAA). The difference is that a GAA has electrostatic control over the nanowire channel all around instead of only one direction which is the case in bulk MOSFET technology.

The design and growth of the nanowire affects much of its electronic properties. The nanowires can be formed both with top-down and bottom-up techniques. The vapor-liquid-solid (VLS) process and selective area growth are common bottom-up epitaxy growth techniques for NWs. The VLS method uses catalysts in the form of metal nanoclusters to grow the wires. The catalysts are used to set the position and size of the wires. The crystal then takes form under the metal particles. For the selective area growth, the growth of the wires are made through openings in a hard mask. The hard mask is made through lithography. There exist many methods to grow NW wires with the top-down approach, e.g. hard mask patterning and reactive etching on H_2 [8]. These methods are more similar to traditional fabrication of bulk semiconductors. The NW are then etched directly from the bulk. The nanowires can also be grown

either vertically or horizontally. The vertical NW is a beneficial design in terms of packing density, since the gate length isn't connected to the footprint of the device.

When there is a lattice mismatch in heterostructures, lateral expansion causes stress in the different crystal planes, which may lead to defect formation. The design of thin nanowires with small footprint reduces this phenomenon, which gives the heterostructure design good flexibility as well as high quality [2]. It enables III-V materials to be designed on Si-substrates which is favorable in an industrial and economical perspective as well as for good transistor performance. However this puts a high demand on the controllability of the gradients and doping levels in the NWs. Poor integration of doping can cause high contact and access resistances as well as poor electrostatic control [7].

2.1.5 Stacking faults in NW MOSFETs

The origin of the stacking faults lie in the crystallography of III-V semiconductors as well as in the method for crystal growth. The most common crystal structure in III-V compound semiconductor materials (InGaAs included) is zincblende (ZB). This crystal structure is a so-called face-centered cubic structure. Another crystal structure is the wurtzite (WZ), which has a hexagonal structure. Except for the structural difference, there is a difference in band gap as well. For InGaAs NWs the crystal structure is typically a mix of both zincblende and wurtzite. By changing growth conditions, especially temperature, it is possible to switch between the two crystal structures [5][6]. As mentioned there is normally a crystal mix in III-V NWs, but they can also be grown for crystal purity [4]. With electron microscopy techniques it is possible to study the crystal structure of the nanowires. If a nanowire which is supposed to have pure crystal structure shows to have segments which are of a mixed structure it is said that it has so called stacking faults. Right now there are ongoing tests on how to grow these crystals to avoid or at least minimize stacking faults by changing the growth process. It is under debate whether a mix of ZB and WZ reduces the performance in NW-FETs. A large number of stacking faults could lead to mobility and conductivity degradation according to some publications [14].

2.2 Low-Frequency Noise

Noise is a random event in electronic systems that comes from many different sources and is often limiting the sensitivity and detectability of electrical instruments. Communication systems are examples of RF applications for which the signal-to-noise ratio (SNR) is an important measure to consider. If not considered then the capacity together with the reliability of the information exchange will falter. Due to its random nature, noise is often hard to eliminate and is in some cases even impossible to fully eliminate. The noise can be detected as fluctuations in the measured current or voltage. In electronics, the noise can

be divided into different types of noises. The fundamental noise sources are white noise (thermal and shot noise), generation-recombination (GR) noise, mobility fluctuations and random telegraph noise. Low frequency noise (LFN) or pink noise is an indirect consequence of the constant down scaling of transistor dimensions. It is connected to the transport of charge carriers so it is a combination of GR noise and mobility fluctuations. For semiconducting devices, the LFN is caused by surface charge trapping (GR noise). For thin metal films the main cause is instead carrier defect scattering (mobility fluctuations). It was for a long time thought that defects and impurities were the main or only cause of LFN, but Hooge and Vandamme found in the 1960's that the noise in thin metal films originated from lattice scattering instead [11].

The origin of the LFN in III-V MOSFETs lies in the device fabrication which causes gate oxide defects. It is the integration of high-κ dielectrics with III-V semiconductor materials that is hard to perform without getting a large amount of defects. These defects affect the transport of electrons in the channel which randomly can jump between energy states, or so called traps. This leads to both a change in surface potential as well as inversion charge density at certain points along the channel. Depending on the depth at which the traps are located they are either interface traps or border traps. The interface traps are located at the channel-oxide interface and the border traps are the ones located further into the oxide. The border traps are usually located at least a few atomic layers away from the interface. The border traps do in contrast to the interface traps not originate from the poor oxide/semiconductor interface but from oxygen vacancies instead. The electrons will through quantum-mechanical tunneling switch between the energy states. This will also cause some change in the atomic structure near the trap site due to the change of charge which causes electrostatic interactions of nearby atoms.

Since the traps cause the electrons to jump between states the current will consequently fluctuate in time. The current can be described as the average current $\bar{I}$ together with the current change caused by the traps $i_n(t)$

$$I(t) = \bar{I} + i_n(t) \tag{2.9}$$

The change in current can be seen as a change in the gate bias due to the electrons located in the traps. This will in the transfer characteristics curve be seen as a shift of the curve, i.e a change in threshold voltage. The number of traps are connected to the gate area so by scaling gate dimensions the amount of traps will decrease. The fluctuations in current are random events which can be described as the random

variable X(t). The random noise can followingly be described with a squared quantity referred to as the power spectral density S(*f*) or PSD. The relation between the two is

$$\overline{X^2(t)} = \int_0^\infty S_X(f)df \quad (2.10)$$

A noise PSD which is independent of the frequency and thus constant is categorized as white noise. LFN or 1/f noise has a PSD that is proportional to $1/f^\beta$ where β has a value around 1 for the low frequency case. The low frequency range is in this context approximately between 1 to 10^4 Hz. The value of β describes the trap density distribution. Depending on whether the majority of traps are located deep in the oxide (β>1) or close to the channel-oxide interface (β<1). The 1/f noise origins from both number- and mobility fluctuations, as described in the following sections.

2.2.1 Number fluctuations

Number fluctuations (GR noise) are as mentioned above a random change in the current due to electrons switching between traps in the oxide or at the channel-oxide interface. The trapping and detrapping event can besides changes in current cause fluctuations in mobility, electric field and space charge region width. Each trap contributes with a noise that has a Lorentzian distribution, a PSD proportional to $1/f^2$. The PSD is also dependent on the capture- and emission time constants of the trapping and detrapping events. The time constants are further explained in section 2.2.3. The probability of the electron being in the different energy states must be fairly equal to contribute to the noise. If the trap states are nearly constantly filled or empty there would not occur enough transitions to cause any significant noise. The capture- and emission time constants are of similar magnitude when the trap is within a few kT of the Fermi level. Usually there are many traps present which all contribute with a PSD of Lorentizian type, a superposition of all transition events will result in a noise which has a $1/f$ dependence instead, see Figure 2.4. It can be noted that for the case where only a few traps are involved in the GR noise it is referred as RTS noise. This will be further described in section 2.2.3.

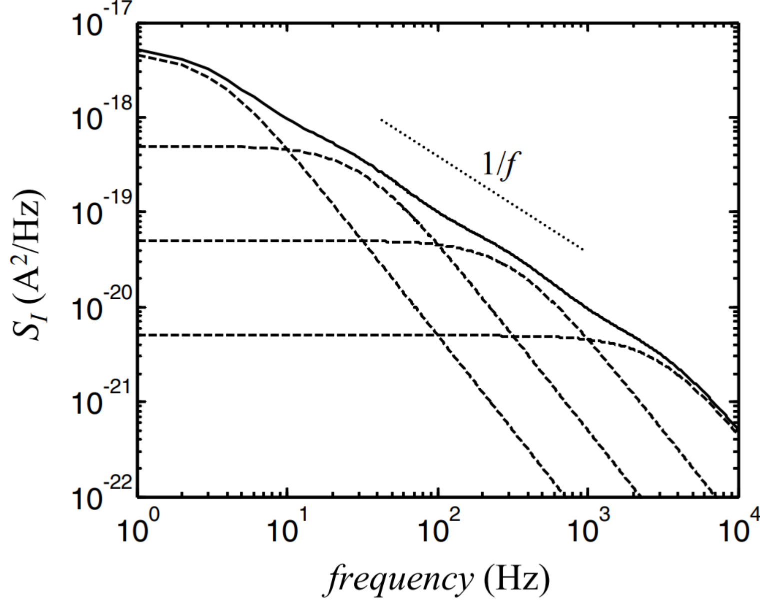

Figure 2.4. Superposition of four Lorentzians which exhibits a 1/f dependence. Figure taken from [12].

The first and simplest model of the LFN due to number fluctuations was established by A.L. WcWhorter in the late 1950's. He based his model on an even trap density distribution and elastic tunneling only. It was however found that the mobility and scattering in the channel was also affected by the charge carrier trapping in the oxide. The change in carrier mobility due to number fluctuations is called correlated mobility fluctuations. The normalized drain current noise PSD could then be described as

$$\frac{S_{I_D}}{I_D^2} = \left(1 + \frac{\alpha\mu_n C_g I_D}{g_m}\right)^2 \left(\frac{g_m}{I_D}\right)^2 S_{V_{fb}} \tag{2.11}$$

where $S_{V_{fb}}$ is the flat band voltage noise PSD, C_g is a sum of the gate oxide capacitance, the quantum capacitance, and the centroid capacitance, μ_n is the effective carrier mobility, and α is the dimensionless scattering coefficient. The α can either be positive or negative depending on how the mobility is affected. The first term of the first factor represents number fluctuations of charge carriers while the second term modulates the fluctuation in mobility due to the number fluctuation. The flat band voltage noise is connected to the elastic tunneling process and can be described by

$$S_{V_{fb}} = \frac{q^2 k_B T \lambda N_T}{W_G L_G C_{ox}^2 f^{\beta}} \tag{2.12}$$

where N_T is the trap density in the gate dielectric at the semiconductor Fermi level. Traps located further away than a few kT from the Fermi level does not make any major difference in the noise level. The tunneling attenuation length λ can further be described by:

$$\lambda = \left(\frac{4\pi}{h}\sqrt{2m^{*}\Phi_{B}}\right)^{-1} \tag{2.13}$$

with Φ_B being the energy barrier for the elastic tunneling transitions in relation to the charge carriers at the interface.

2.2.2 Mobility fluctuations

The 1/f noise is as mentioned also influenced by mobility fluctuations which is mainly due to phonon scattering. There are though several different scattering mechanisms that can occur in the channel. Scattering can arise from e.g. surface roughness and phonons(lattice). Depending on the effective electric field and the density of the inversion charge in the channel, each scattering mechanism is more or less prominent. The concept of LFN generated by mobility fluctuations was introduced by Hooge who noticed that there were no surface effects in thin continuous gold films. According to the Hooge mobility model, S_{I_D}/I_D^2 can be described as

$$\frac{S_{I_D}}{I_D^2} = \frac{q\alpha_H\mu_{eff}V_{DS}}{fL_G^2I_D} \tag{2.14}$$

where μ_{eff} is the effective carrier mobility, and α_H is the Hooge parameter which is dependent on the material(crystal quality) as well as the bias. The bias affects the different scattering mechanisms that occur which thus affects the Hooge parameter. The mobility fluctuations are then dependent on the bias condition, which is opposite from number fluctuations. Even though this model has a lack of firm theoretical foundation, it remains popular due to its utility as a first-order benchmark of noise magnitudes.

The LFN in MOSFETs is typically a combination of both number- and mobility fluctuations. It has though been seen in studies that different types of MOSFETs usually have one dominant noise source. The drain current noise PSD ($\frac{S_{I_D}}{I_D^2}$) as a function of the drain current will be different depending on which type of fluctuation that is dominant. If number fluctuations is the more dominant noise source $\frac{S_{I_D}}{I_D^2}$ will be

proportional to the normalized transconductance $(\frac{g_m}{I_D})^2$. If the noise mostly originates from mobility fluctuations instead, the $\frac{S_{I_D}}{I_D^2}$ will be proportional to the inverse drain current $\frac{1}{I_D}$. The dominant noise source can change depending on the channel length of the MOSFET. As an example, for a long channel planar device the current is more dependent on the channel mobility than for a short channel device with semi-ballistic transport properties. The long channel planar device would then be more sensitive to mobility fluctuations [1].

2.2.3 Random Telegraph Noise

As mentioned earlier, LFN is the superposition of the noise from several traps in the gate oxide. As the gate dimensions are decreased, so are the number of traps as well. When only one individual trap or very few traps are affecting the drain current in the channel, the noise is called RTS noise. The RTS noise is in difference to the LFN proportional to $1/f^2$. If the drain current is measured over time, the current is jumping between two discrete levels. The two current levels correspond to the trap being occupied or not. The time that the current is in the high level is called the capture time constant and the time that it is in the low level is called the emission time constant. The difference between the current levels is called the RTS noise amplitude. The time constants are directly connected to the gate voltage and are very sensitive to it. A trap located in the band gap will be more or less likely to be occupied depending on how the band edges are bent by the gate voltage, see Figure 2.5. A trap energy level that is higher than the semiconductor Fermi level leads to a low probability of having an electron with high enough energy to elastically tunnel to the trap state from the semiconductor. If the trap energy level is instead lower than the Fermi level then the electron will have a high probability of tunneling elastically to the trap state and remain in this state.

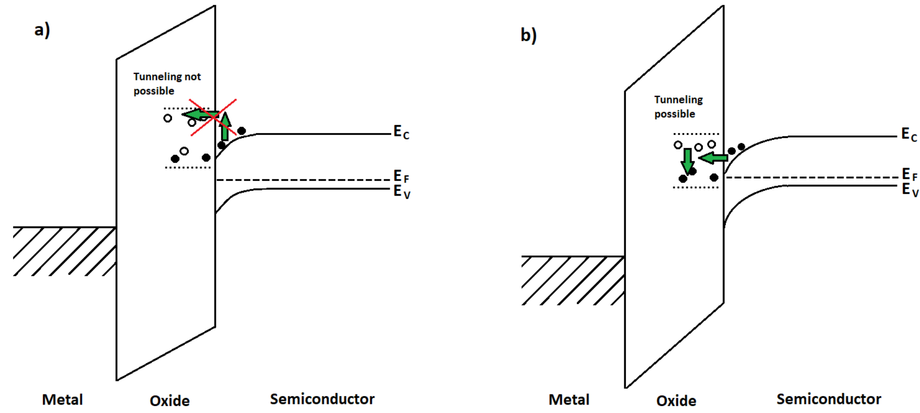

Figure 2.5. Band diagrams of biasing of trap states. (a) Lower V_{GS}, trap states not close enough to the Fermi level for tunnel transitions to occur. (b) Higher V_{GS}, trap states are closer to the Fermi level and tunneling transitions are more likely to occur.

Chapter 3

3. Device Fabrication

The Vertical InAs-InGaAs Nanowire MOSFET samples used in this work were constructed by our supervisor in advance. A short summary of the device fabrication will be given for both samples.

An n-doped InAs layer was grown on top of a p-type silicon layer by metal-organic vapor-phase epitaxy (MOVPE). The InAs layer is the source contact of the transistor. By the use of gold particles the nanowires were grown by MOVPE. The gold particles were patterned using EBL (electron beam lithography) and act as so-called nanowire nucleation sites. The first 100 nm long section of the nanowire consists of InAs. The next 50 nm section is graded InGaAs. The final 300 nm section is n-doped InGaAs. The nanowire after growth can be seen in Figure 3.1(a).

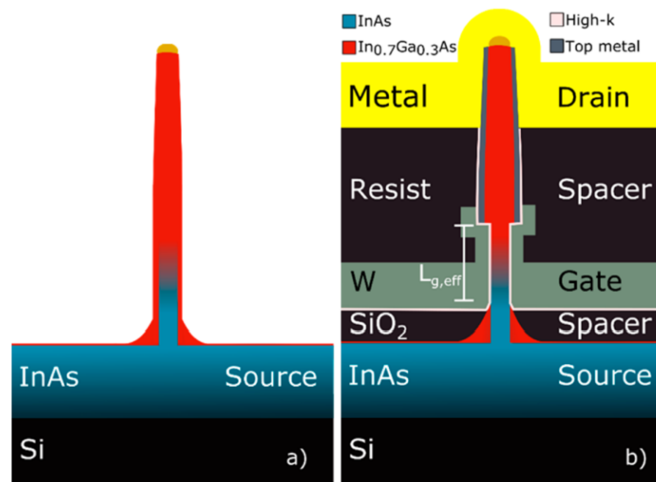

Figure 3.1. (a) Illustration of nanowire dimensions after growth (b) Completed device of Vertical InAs-InGaAs Nanowire MOSFET. Figure taken from [2].

Normally the nanowires grown in this process will have a wurtzite crystal structure. Though the whole nanowire will actually not have wurtzite crystal structure but a small segment of zincblende as well, see Figure 3.2(b). One could reason that this section appears due to the difference in gold particle size as Ga

is included in the nanowire. The stacking faults that were discussed in section 2.1.5 can be seen in Figure 3.2(c).

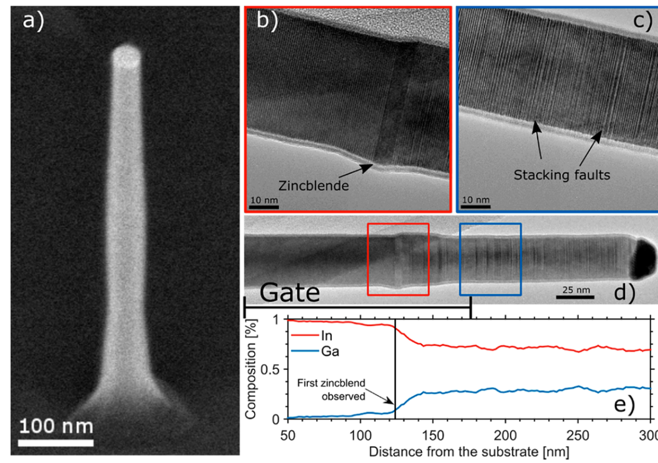

Figure 3.2 (a) SEM image of nanowire (b) TEM image of zincblende segment (c) TEM image of segment with introduced doping (d) TEM image of nanowire (e) Composition analysis of the nanowire. Figure taken from [2].

After the nanowire growth, a bottom dielectric spacer was defined that will act as an insulator between source and gate. Before the high-k dielectric and gate was deposited, the highly doped shell around the nanowire was etched. The ALD gate dielectric was 1 nm Al_2O_3 and 4 nm HfO_2. The gate metal was added by sputtering 60 nm of tungsten. The gate was followed by a second organic top spacer and a Ni/Au metal contact, see Figure 3.1(b) for the complete device.

Chapter 4

4. Experimental setup

The experimental setups for the different performed measurements will in this section be briefly explained. The Semi-auto probe station - TS2000-SE, see Figure 4.1(a), was used both for the DC- as well as the noise measurements at RT in order to contact the wanted devices on the sample. The Semiconductor device parameter analyzer - B1500A was used in the DC measurements to control and apply the biasing to the probe station and to measure the currents/voltages.

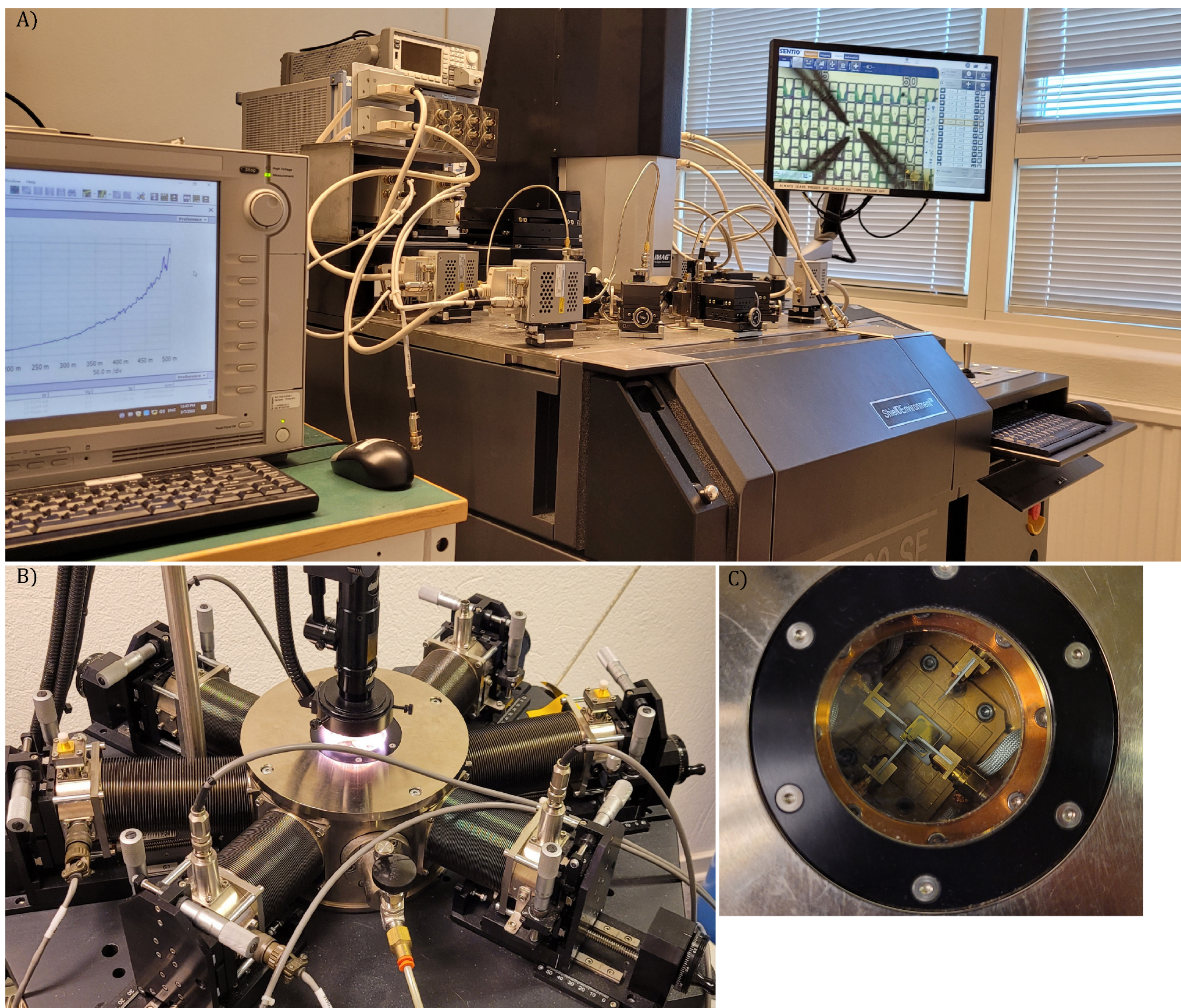

Figure 4.1 (a) The Semi-auto probe station (the black box with all the cables) and the parameter analyzer (on the left) (b) The cryo probe station (c) The inside of the cryo chamber with three probes connected to one device.

The noise measurements at RT used the same setup as the DC measurements, but with the drain contact being connected to a low-noise preamplifier instead, in order to supply a constant V_{DS} of 50 mV as well as to amplify and convert the signal from current to voltage. A lock-in amplifier from Stanford Research Systems was connected to the preamplifier, see Figure 4.2. The purpose of the lock-in amplifier was to measure the noise in the drain voltage in relation to frequency. A lock-in amplifier works by mixing the input signal, and an internal signal with a frequency of choice (the lock-in frequency), creating a signal with the sum and difference of their respective frequencies. A very narrow lowpass filter is then used to filter out every frequency component of the mixed signal that is not close to DC. This means that the only frequency component from the input signal that makes it through both stages is the frequency component that is equal or very close to the lock-in frequency. This makes it possible to measure the noise levels of a signal as a function of frequency by sweeping the lock-in frequency.

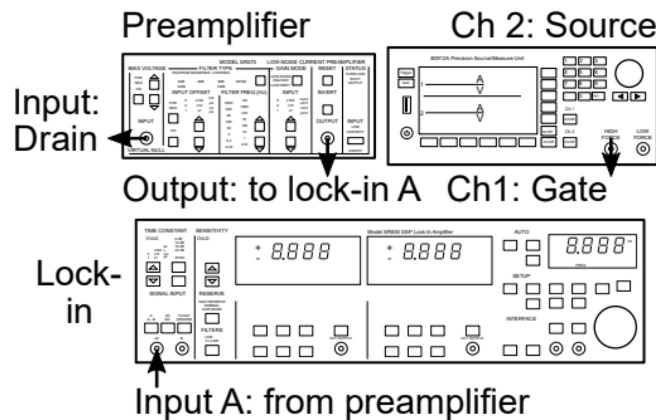

Figure 4.2. Schematic of LFN measurement setup, taken from [1].

The 1/f noise measurement was performed by sweeping the lock-in frequency between 10 and 1000 Hz at V_{DS}=50 mV and V_{GS} = (-200, -100, 0, 100, 200, 300, 400, 600) mV. A V_{DS} of 50 mV is a preferable voltage point since it is enough drain voltage to have a detectable drain current without having too highly bent channel bands.

For the DC measurements below room temperature and all the way down to 13 K, a cryo probe station, see Figure 4.1(b) and 4.1(c), was used together with the semiconductor device parameter analyzer B1500A. Transfer- and output characteristics were measured both for normal biasing and inverted biasing.

Time dependent drain current measurements were also taken. The transfer characteristics were taken with the doubled amount of points as for RT and with V_{DS} = 5 mV, 50 mV and 500 mV. For the output characteristics the same amount of points were taken and with V_{GS} = (-200,0,200,400,600)mV. The DC characteristics were taken at temperatures of T = (13, 20, 30, 40 ,50, 70, 90, 120, 150, 190, 240, 290)K for three devices on the sample without stacking faults (3738), and for one device on the sample with stacking faults (2834).

Chapter 5

5. Results and Discussion

5.1 DC-measurements at RT

The DC-measurements at room temperature showed some devices on the 3738-sample (sample without stacking faults) with good DC performance. The general gate leakage of all devices on the sample turned out to be higher than expected. For most devices the gate leakage reached a maximum of 1 μA. The highest peak transconductance of a device on the sample reached a value of g_m = 0.85 mS/μm and a minimum subthreshold swing of *SS* = 90 mV/dec. Recent measurements [2] on single nanowires with a diameter of 28 nm and effective gate length of 160 nm on the 2834-sample (sample with stacking faults) shows a maximum transconductance of g_m= 1.4 mS/μm and a subthreshold swing of *SS* = 85 mV/dec. The measurements for both samples were performed at V_{DS} = 500 mV. The DC performance for the new fabricated sample 3738(w/o SF) is slightly degraded in comparison with the 2834-sample(w SF).

5.2 Temperature dependence in DC-measurements

Since temperature dependent measurements took significantly more time due to the cryo probe station not having automatic control, unlike the Semi-auto probe station used in RT measurements, and due to downtime during temperature changes, only four devices were characterized. The devices that were chosen for the DC-measurements were those that had the lowest subthreshold swing at room temperature. The transfer characteristics for the four devices at V_{DS} = 50 mV and temperatures of 14 to 290 K can be seen in Figure 5.1. It can be seen that the maximum $I_{D,on}$ for the 2834-sample(w SF) is about the same as the devices on the sample 3738(w/o SF). However the 2834-sample(w SF) has approximately one order of magnitude better I_{on}/I_{off} ratio. The temperature dependent threshold voltage can be noted from the curves in the linear scale. It is seen that the threshold voltage increases with decreased temperature which is expected and typically seen in Si MOSFETs as well [15]. A decrease of the subthreshold swing with decreasing temperature can also be denoted from the transfer curves in the logarithmic scale, as the slope gets steeper for lower temperatures. This is also confirmed in Figure 5.2, which shows the subthreshold swing as a function of I_D for each temperature. In Figure 5.2 it can also be seen that the device on the 2834-sample(w SF) has a slightly wider current range at which the SS is low.

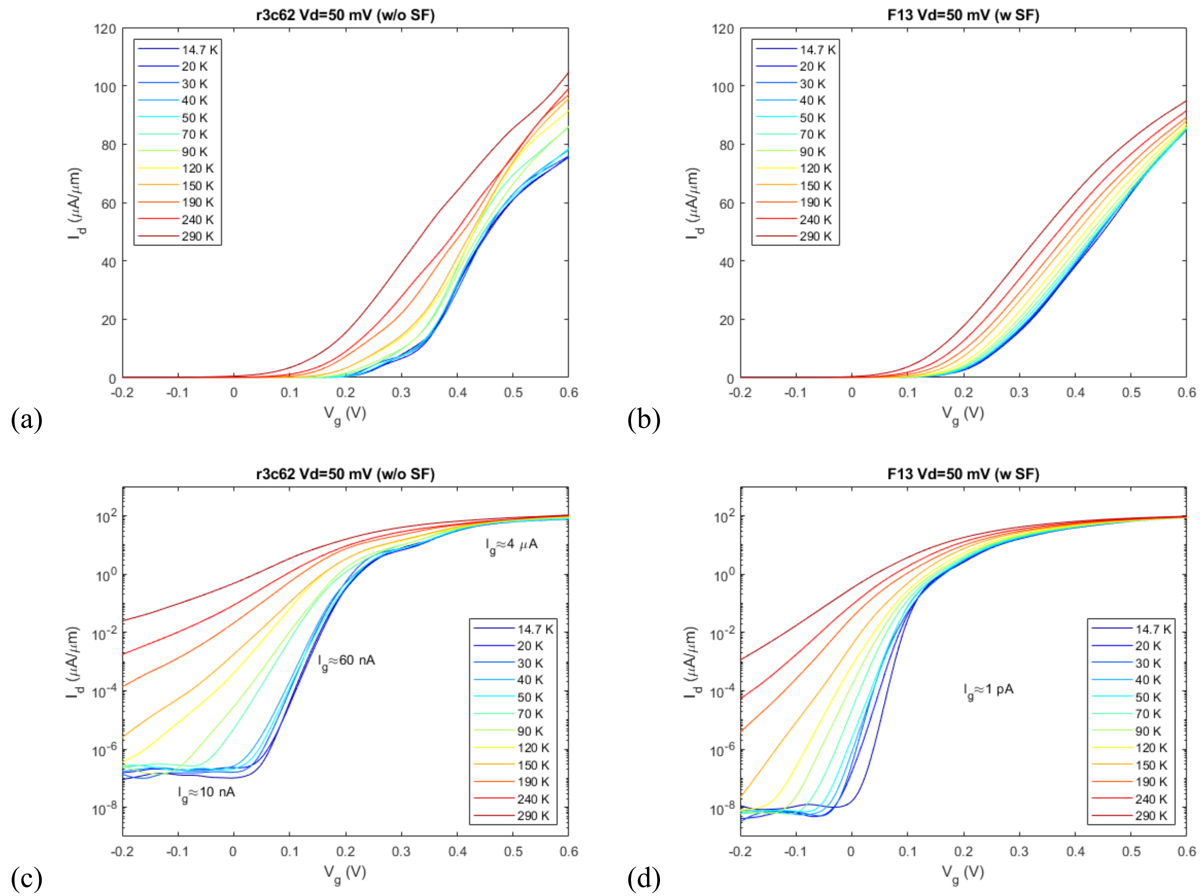

Figure 5.1 (a) (b) transfer characteristics at different temperatures for device r3c62 on sample 3738(w/o SF) and device F13 on sample 2834(w SF) respectively, at V_{DS}=50 mV and in linear scale. (c)(d) transfer curves at different temperatures for the same devices and at V_{DS}=50 mV but in logarithmic scale. It can be seen that the current decreases with decreasing temperature and that the threshold voltage increases with decreasing temperature for both devices.

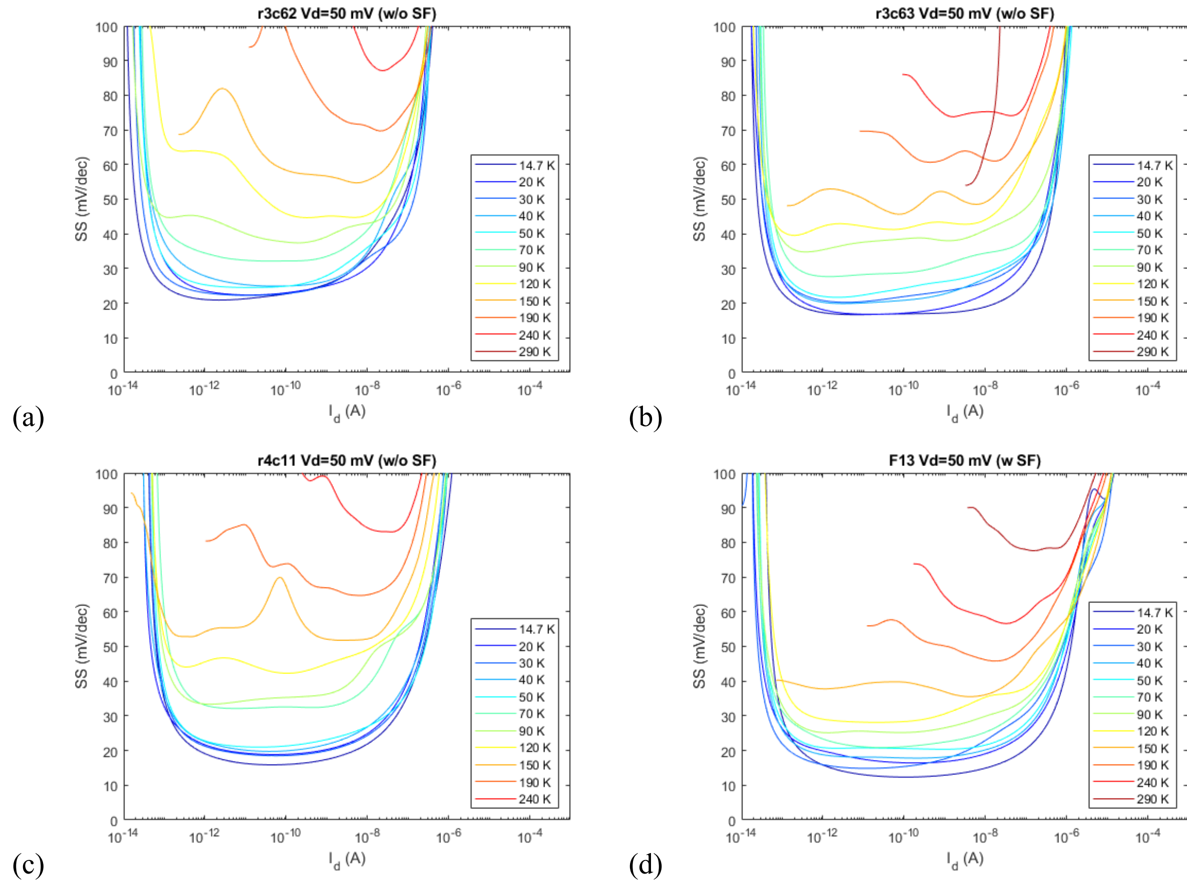

Figure 5.2 (a) (b) (c) SS (mV/dec) at different temperatures with V_{DS}=50 mV for device r3c62, r3c63 and r4c11 respectively, on the 3738-sample(w/o SF). (d) SS (mV/dec) at different temperatures with V_{DS}=50 mV for device F13 on the 2834-sample(w SF).

The minimum value of the subthreshold swing vs temperature at V_{DS} = 50 mV for the 3738-sample(w/o SF) can be seen in Figure 5.3(a), (b) and (c) while the 2834-sample(w SF) is shown in Figure 5.3(d). From these plots it can be seen that the 2834-sample(w SF) has the lowest subthreshold swing across all temperatures. All 3 of the devices on the 3738-sample(w/o SF) showed that the subthreshold swing started to flatten out below 50 K instead of following a straight line down to 0, which as explained earlier, is due to band tails. This behavior was hard to observe on the device on the 2834-sample(w SF) for the temperature range of 13-300 K. The *SS* does not follow the linear trend at low temperatures but does not flatten out either. It could be due to the fact that this device has a shorter characteristic width of the exponential band tail [3], and would flatten out at lower temperatures. The *SS* for the 2834(w SF)- and 3738(w/o SF) sample at 14 K was measured to 12 mV/dec and 16 mV/dec respectively.

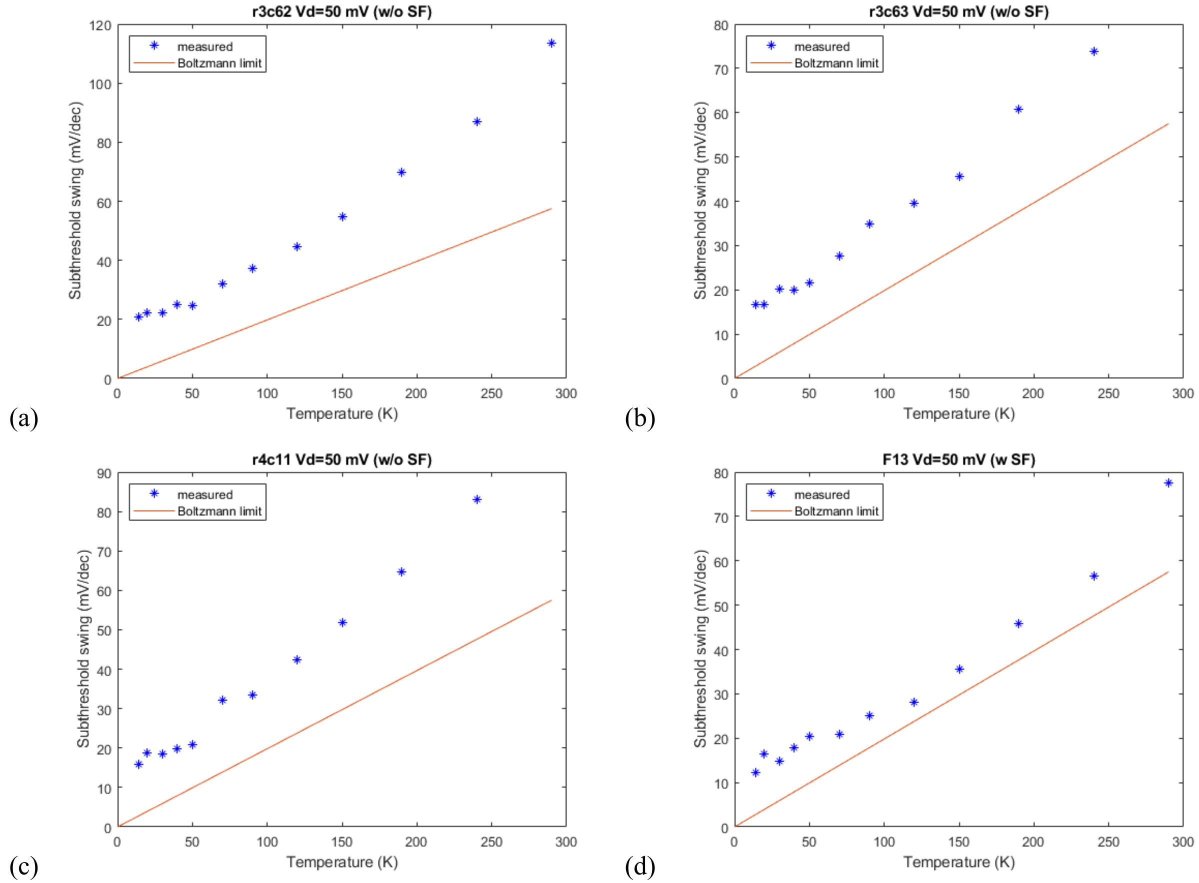

Figure 5.3 (a) (b) (c) SS (mV/dec) vs temperature at V_{DS}=50 mV for device r3c62, r3c63 and r4c11 respectively, on the 3738-sample(w/o SF). Devices r3c63 and r4c11 broke during and before the last measurement at 290 K which is why those data points are below the theoretical limit. (d) SS (mV/dec) vs temperature at V_{DS}=50 mV for device F13 on the 2834-sample(w SF).

5.3 1/f Noise at RT

The devices used for the noise measurements were selected based on the transconductance, subthreshold swing and high current but most of all by the lowest gate leakage since it was already very high. The frequency sweep measurements of the noise can be seen in Figure 5.4, where the drain current noise PSD is plotted against frequency. The 15 data points could be linearly fitted and are shown in the same loglog plots for the seven different gate voltages ranging from -200 mV to 600 mV. From the linear fits the of $1/f$ was determined for each gate voltage. For the 2834-sample(w SF) the β varied between 0.59 and 1.25.

When β is lower than 1, the trap density is higher close to the channel-oxide interface, and when β is greater than 1, the trap density is higher further away from the channel-oxide interface. Since β is both lesser and higher than one for both devices depending on the gate voltage, it indicates that the trap

location varies with gate voltage. The location of these traps is important for high frequency applications as traps closer to the channel-oxide interface will be more likely to be occupied at high frequencies, unlike traps far into the oxide which will not have time to get occupied.

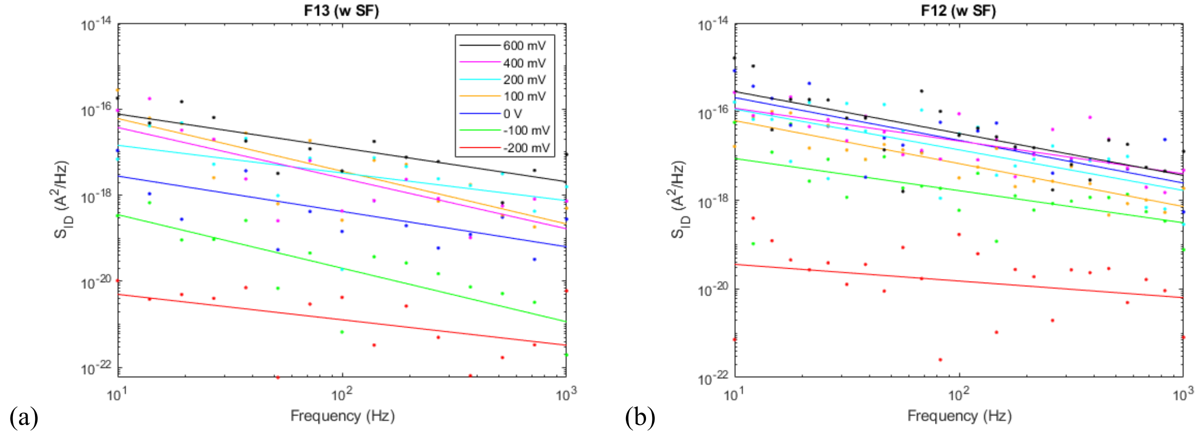

Figure 5.4 (a) (b) PSD vs frequency for two devices on the 2834-sample(w SF)

The normalized drain current noise PSD (S_{Id}/I_D^2) vs source current of the 2834-sample(w SF) can be seen in Figure 5.5(a), and the 3738-sample(w/o SF) in Figure 5.5(b). The measurements were taken at 10 Hz and V_{DS}=50 mV and these show that the dominant 1/f noise source for the 2834-sample(w SF) is number fluctuations. The measured data points follow the $(\frac{g_m}{I_D})^2$ rather than $1/I_D$ which would indicate that the contribution from number fluctuations are higher than the mobility fluctuations [1]. The measurement of the 3738-sample(w/o SF) is in comparison hard to draw any conclusions from. However most points follow the curved relationship of $(\frac{g_m}{I_D})^2$, which implies that number fluctuation is the dominant noise mechanism. The measurement point that does not follow the curve is for a very small current and is thus unreliable. With the use of E.q (2.12) the minimum trap density was calculated to $N_{bt} = 6 \cdot 10^{18} cm^{-3} eV^{-1}$ for sample 2834(w SF) and $1.2 \cdot 10^{19} cm^{-3} eV^{-1}$ for sample 3738(w/o SF). These values were calculated for both samples with a tunneling attenuation length of λ = 0.13 nm and a gate oxide capacitance per unit area of C_{ox} = 0.029 F/m^2.

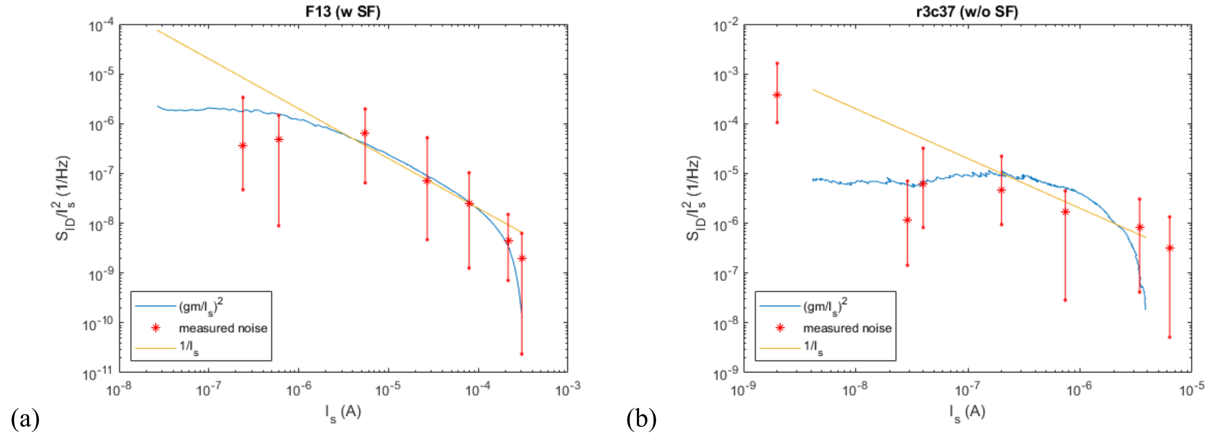

Figure 5.5 (a) normalized PSD (S_{Id}/I_D^2) vs source current for device F13 on the 2834-sample(w SF) at 10 Hz and V_{DS}=50 mV. It can be seen that the 1/f noise is dominated by number fluctuations. (b) normalized PSD (S_{Id}/I_D^2) vs source current for device r3c37 on the 3738-sample(w/o SF) at 10 Hz and V_{DS}=50 mV. The red bars show the minimum and maximum measured noise values while the red star indicates the mean value.

5.4 1/f Noise at T=13 K

The same low frequency noise measurements as in the previous section were performed at 13 K, but device r3c37 and F12 broke before the PSD vs source current measurements could be completed. Device r3c37 ended up as a short circuit between gate and drain, while device F12 stopped responding to gate bias, and only leakage currents could be observed. The reason that both devices broke was assumed to be due to the vibrations in the setup that originated from the cryogenic pump, which made the probe tips and the sample move a few micrometers in respect to each other. This movement could be seen through the microscope, and it left behind relatively big holes/scratches on the surface of all samples where the probe tips dug into the surface material.

The frequency sweep measurements of the noise PSD at 13 K can be seen in Figure 5.6. These measurements also show a clear $1/f$ dependence for all three devices, but where the noise is about one order of magnitude lower than that of the corresponding room temperature measurement independent of current. Similar studies show the same result that the noise decreases with temperature but that the magnitude of the difference increases with current as well. It should be noted that some of the linear fits of the PSD in Figure 5.6 do not have a $1/f$ dependence. One extreme case is the measurement at V_G=400 mV in Figure 5.6 (c). The PSD is seen to be nearly constant with frequency, which means that β goes towards zero. This could be due to the traps being located very near the channel. However since the measurement points are very separated it is hard to draw any direct conclusions of β. A solution would be to take more measurement points in the same frequency interval.

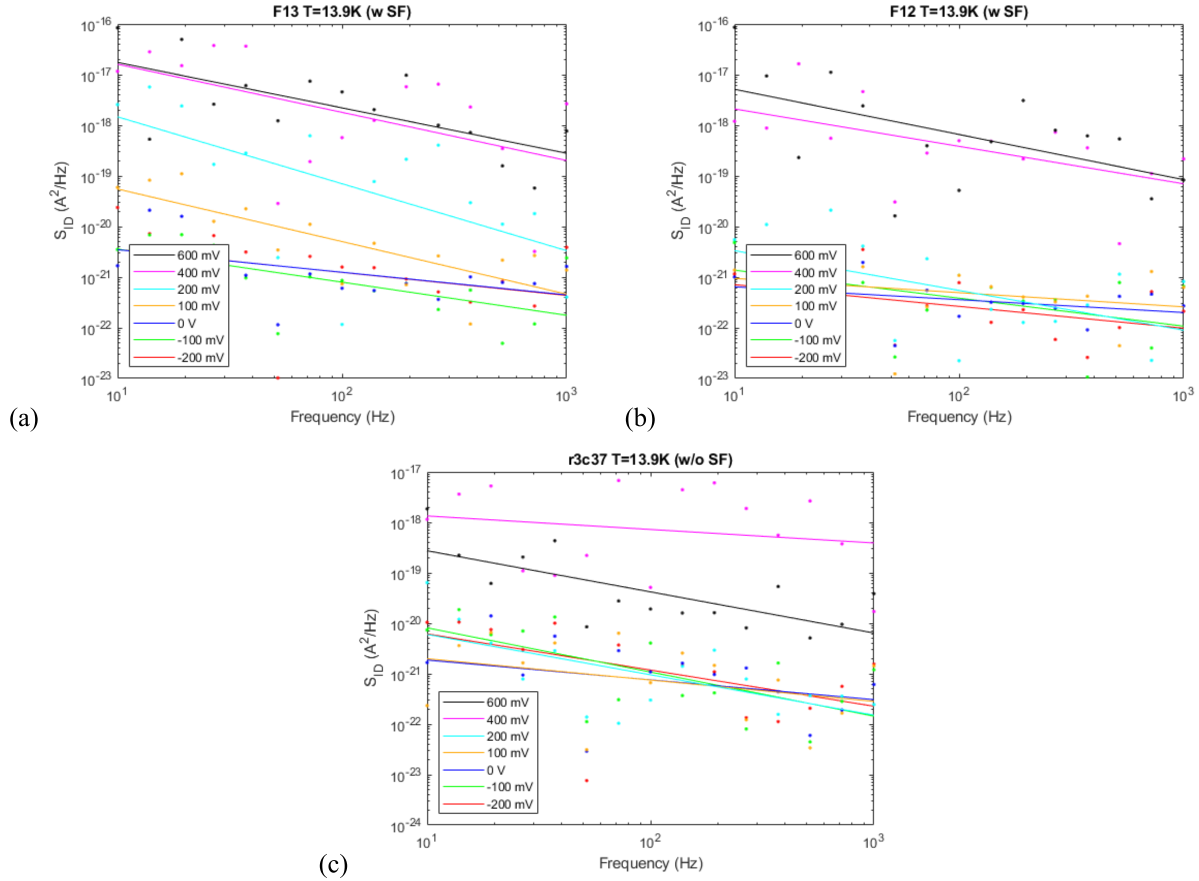

Figure 5.6. PSD vs frequency at 13.9 K for (a) device F13 on the sample 2834(w SF), (b) device F12 on sample 2834(w SF) and (c) device r3c37 on sample 3738(w/o SF).

The normalized drain current noise PSD was plotted vs source current for the 2834-sample(w SF), see Figure 5.7. The frequency was fixed to 10 Hz as it was in the previous section and seven data points were taken for gate voltages ranging from -200 mV to 600 mV, but the data points at the lower gate voltages had too small currents to be reliable. Hence they are not included in the plots of Figure 5.7. The PSD could be seen to be proportional to both $(\frac{g_m}{I_D})^2$ and $1/I_D$ for large I_S, but for small I_S the measurement points are rather proportional to $1/I_D$ for both devices. It is therefore hard to draw a conclusion as to whether the noise originates from number- or mobility fluctuations, and is most likely a mix of the two. If the drain current noise PSD is assumed to be generated by fluctuations in the carrier mobility according to Eq. (2.14) the Hooge parameter could be calculated to $\alpha_H \sim 1 \cdot 10^{-4}$ for the 2834-sample(w SF) independent of current. Enough measurements on the 3738-sample(w/o SF) were not taken to be able to determine the dominant noise source, since the measured device broke. Hence no plots of the drain current noise PSD vs current could be included for that device. However the collected measurement data

could be used to calculate the Hooge parameter for the device. The Hooge parameter was for the 3738-sample(w/o SF) dependent on current and was calculated between $\alpha_H \sim 7.3 \cdot 10^{-6}$ and $5 \cdot 10^{-4}$.

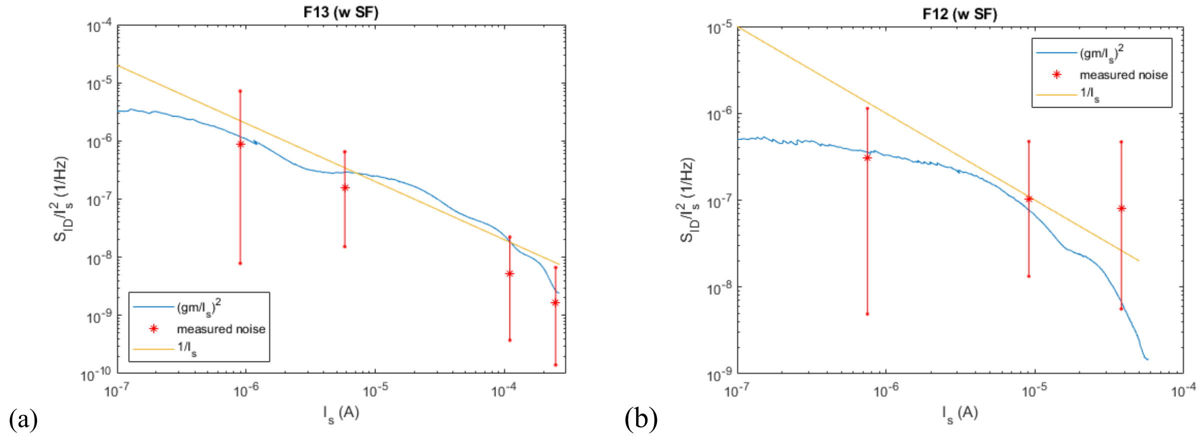

Figure 5.7 (a)(b) PSD vs source current for two devices on the 2834-sample(w SF).

5.5 RTS-noise

One device on sample 3738(w/o SF) clearly indicated the presence of a single dominant trap during the current measurements over time which can be seen in Figure 5.9(a) below. The drain current in this device had two discrete levels which indicates random telegraph signal (RTS) noise. The current histogram of this measurement for T=1-6 seconds can be seen in Figure 5.9(b). Since both current leves had about the same counts, the electrons had as easy to elastically tunnel to the trap state as to tunnel out of it and back to an empty state in the semiconductor. The position of the trap energy level relative to the semiconductor Fermi level determines how long the electron is in the different states. By changing the gate bias the trap energy level is either increased or decreased. A trap energy level that is higher than the semiconductor Fermi level leads to a low probability of having an electron with high enough energy to elastically tunnel to the trap state from the semiconductor. The capture time is then high since the electron will most of the time be in the lower energy state. If the trap energy level is instead lower than the Fermi level then the electron will have a high probability of tunneling elastically to the trap state and remain in this state. With almost equal capture and emission times seen from the measurements it could be reasoned that the trap energy level is very near the semiconductor Fermi level. The amplitude of the drain current RTS noise is roughly 0.1 μA. The amplitude of the RTS noise is connected to the trap's physical location along the nanowire circumference with respect to the channel. The amplitude is though also a function of the drain current [13].

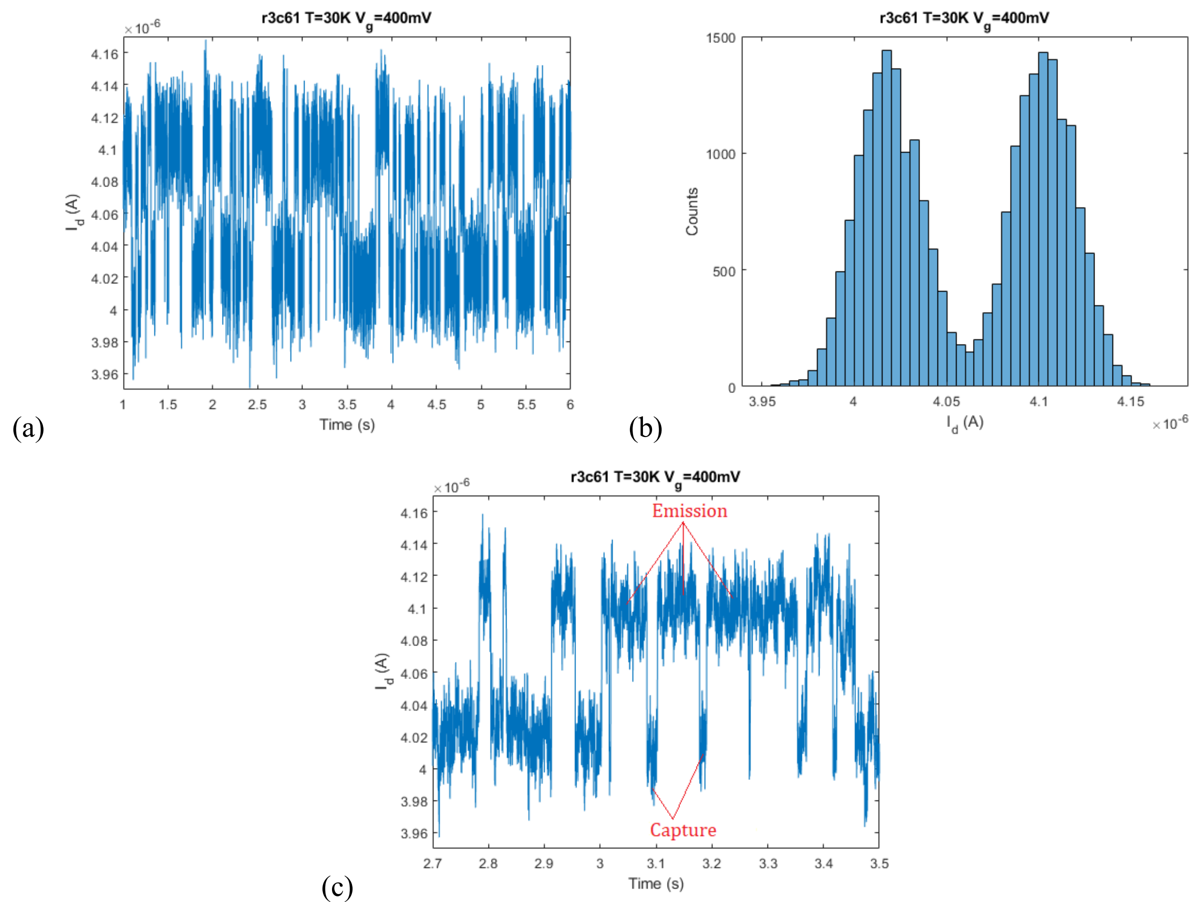

Figure 5.9. (a) RTS noise of sample 3738(w/o SF) (b) Current histogram of (a) (c) Zoom in on (a) showing the capture and emission parts.

Chapter 6

6. Conclusion and future work

Low-Frequency noise- and DC characterization was made on vertical InGaAs Gate-All-Around MOSFETs based on NWs with different growth recipes in purpose of investigating the effect of stacking faults in the nanowire structure. The DC measurements results show no improvement in any metric with the lack of stacking faults. There were neither any implications that the sample without stacking faults would have a lower subthreshold swing at cryogenic temperatures than the sample with stacking faults. For both samples the *SS* followed the Boltzmann linear trend at high temperatures and saturated due to the band tail at cryogenic temperature. The low frequency noise measurements at room temperature show for both samples that the dominant noise source is number fluctuations. The minimum trap density for the sample with stacking faults was $N_{bt} = 6 \cdot 10^{18} cm^{-3} eV^{-1}$ and $1.2 \cdot 10^{19} cm^{-3} eV^{-1}$ for the sample without. The measurement at a cryogenic temperature of 14 K does however show that the dominant noise source is hard to determine for the sample with stacking faults. Since the devices on the sample without stacking faults did not survive the measurements at cryogenic temperatures, nothing can be said of the dominant noise source. The Hooge parameter for the sample with stacking faults was independent of current and calculated to $\alpha_H \sim 1 \cdot 10^{-4}$ and the sample without stacking faults had a current dependent Hooge parameter calculated between $\alpha_H \sim 7.3 \cdot 10^{-6}$ and $5 \cdot 10^{-4}$. The LF noise measurement results show that the conductivity in the channel has a temperature dependent noise sensitivity. At higher temperatures it is more sensitive to charge trapping in the oxide while at low temperature it is more sensitive to the crystal quality of the channel, which implies that the traps are more accessible at high temperatures for the charges in the channel. In short, no direct advantage by removing SF was observed.

This work is believed to be of high importance for both keeping up with Moore's law and getting a better understanding of how to bring MOSFETs into cryogenic applications. The effect of the crystal structure in NW MOSFETs is still unclear and further investigation on the matter could give important insights. Due to both lack of time and accessibility to working devices, not enough statistics could be gathered to make

a definite conclusion. This work could be followed with further measurements on similar devices to increase the reliability of the study.

Noise in electronic circuits and MOSFETs are random fluctuations in current or voltage that can't be fully eliminated. The continuous downscaling of MOSFET dimensions has lowered the operating voltages which has made the signal-to-noise ratio an important metric. Even the smallest disturbances can have a large impact on the device performance. This has set a demand for high standards in the fabrication stage. Poor device fabrication could lead to high trap densities that degrade channel conductivity. However noise could give useful information and insight on functionality and behavior of devices. Performing noise measurements is not only important to reduce noise but to get knowledge of how to improve general performance as well.

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