E-Band SPDT RF Switch for a Class F PA in III-V Nanowire MOSFET Technology

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November 29, 2022

Printed in Sweden
Tryckeriet i E-huset, Lund

Abstract

This project designs an RF switch operating in E-band to provide a transmit path from a Class-F power amplifier (PA). The basic RF switch is based on the single-pole double-throw (SPDT) topology using shunt transistor switches and two $\lambda/4$ transmission line. The transistors used in this project are nanowire MOSFET transistors developed by the Division of Electromagnetics and Nanoelectronics, LTH, Lund University. A simple Class-F PA is designed in single stage common source topology and uses RF switch as output matching network. This project mainly investigates the behaviors of the RF switch, especially for the PA-path, and the performances of Class-F PA. In addition, this project explores the distributed RF switch as Class-F PA output matching network, in which the $\lambda/4$ transmission line can filter out even and odd harmonics.

Popular Science Summary

It has been thousands of years from traditional paper communication to wired communication, however, and only a century from wired to wireless. Decades later, wireless communication has made a great contribution to modern science and technology. From user's intuitive experience, one of the biggest variations for different wireless communication generation is the speed. Since fifth generation, or 5G, seems to be fast enough for most users, it is the beginning of the Internet of Things (IoT). IoT aims to connect all the devices, cars, household appliances, to the internet for user-friendly control. Higher frequencies and speeds mean less latency and more reliability for these devices. Besides, some applications, for instances, satellites and radar, require higher frequencies up to tens or even hundreds GHz to ensure high-quality and long-distance transmission.

Higher frequencies show more advantages while at the cost of circuit design complexity, especially for transistor modeling. Transistors are getting smaller and smaller, gradually reaching their limits, as a result, new technologies are necessary to be sorted out. Vertical nanowire transistors used in this project will be one of competitive solutions.

Antenna is one of the important component in wireless communication, transmitting and receiving the signal. In order to avoid interruption, antenna can work in Time Division Duplex (TDD) mode, allowing the signal to be transmitted or received in one time slot. An RF switch, in this situation, provides the antenna to change the operating mode, transmitting or receiving. An excellent RF switch shall provide impedance matching, lower power loss and the isolation of two paths.

Since the propagation of the electromagnetic wave in the air is divergent, dissipating power, it is necessary to amplify the power before transmission. The power amplifier (PA), as the last component before the antenna, receives signals from the previous stages and amplifies them to the antenna. The PA design goals are higher gain and robust linearity with the highest possible efficiency.

Acknowledgements

First of all, I would like to express my heartfelt gratitude and appreciation to my supervisor, Lars Ohlsson Fhager, who with vast knowledge has assisted me to solve difficulties I met in this project. Without his guidance, this project would have been almost impossible for me to achieve. Besides, a special thank to co-supervisor, Marcus Sandberg, for discussions together and suggestions which enlightened me a lot. Secondly, I am sincerely grateful to my parents in China, who has provided me with huge financial and mental supports, especially under the Covid-19 pandemic. Finally, I would like to appreciate to my girlfriend in China, who always encouraged me with love.

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Chapter 1
Introduction

With rapid development of modern electronic technology, the demand for higher speed and mass data transfer is driving the higher performance of MOSFET. Thus, it indicates the significant improvement in radio frequency (RF) application, specifically in millimeter wave and beyond.

1.1 Background

The RF switch is a fundamental component in wireless receive/transmit system. There are two main RF switches, electron-mechanical and electronical based on semiconductor technology, such as bipolar transistor (BJT) and MOSFET. This thesis mainly focuses on the latter technology with nanowire MOSFET.

Usually, there are two paths in a single-pole double-throw (SPDT) RF switch, power amplifier (PA) path and low noise amplifier (LNA) path. The basic switch topology considered here is based on shunt transistors that reflect or pass the signal. When the transistor in one of the paths is in on state, then the path is shorted to ground and off. At the same time, the transistor in the other path shall be in off state, and the signal can pass through the path between the antenna and the device.

1.2 Millimeter Wave and E-band in Satellite Communication

Traditional microwave frequency band and millimeter wave frequency band are shown in Figure 1.1 (a) [1]. A broadly explanation of millimeter wave frequency band is from 30GHz to 300GHz with 10 millimeters and 1 millimeter wave lengths respectively. A frequency band from 57GHz - 64GHz is defined as an oxygen absorption band, which means that waves in this frequency band can be attenuated by oxygen molecules by about 15 dB/km [1, 2]. Similar situation happens in the water vapor absorption band with different attenuation that depends on the density of the water vapor. Thus, these two bands are always excluded in wireless communication application. There is a more specific classification in local multipoint distribution service (LMDS) bands in Figure 1.1 (b). However it is out of the scope of this thesis.

The E-band (60GHz - 90GHz) shown in Figure 1.1 (c) contains 12.9GHz bandwidth in total, in which 71GHz - 76GHz and 81-86 GHz bandwidths are the most

targets in this thesis. Because of the large bandwidth, it is particularly suitable for satellite communication with high-speed and high-resolution [3]. In early applications of E-band transceivers, to simplify the system, common modulation such as binary phase shift keying (BPSK) are acceptable for design. In order to increase the spectrum efficiency and fulfill the increasing user amounts, it was updated to 16 quadrature amplitude modulation (QAM) and 64 QAM and beyond [4]. Some other specific standards are given by European Telecommunications Standards Institute (ETSI), presenting general requirements of power and equivalent isotropic radiated power (EIRP) for design [5].

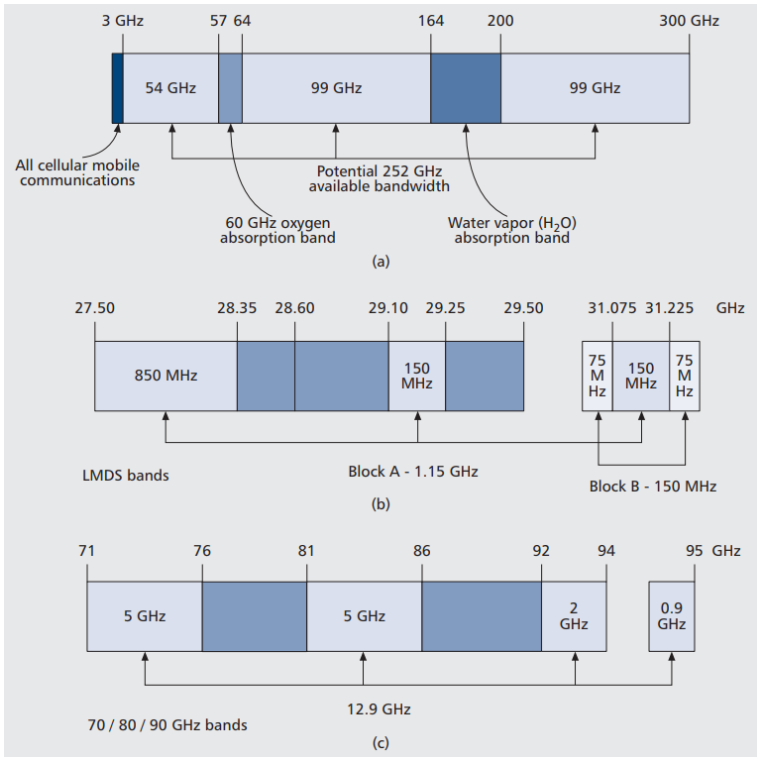


Figure 1.1: Traditional microwave band and millimeter-wave spectrum (a) and LMDS bands with A license and B license (b) and E-band (c) [1].

1.3 Aim and scope

This thesis mainly investigates nanowire MOSFET RF switch in E-band operation. One important goal is to achieve the RF switch with high isolation and low insertion loss (IL). Next is to make the performance incline to the PA path, which shall realize the class-F power amplifier matching network by the RF switch.

All the schematic design and simulations are based on Keysight ADS, including

an additional load pull simulation for the power amplifier to find the possible matching load impedance. Notice that there is conjugate match at the input port of the RF switch. The scope of this project is shown in Fig 1.2, where the PA is designed solely at the output stage and the corresponding matching network. The driver stages of PA, LNA and antenna are not considered in this project.

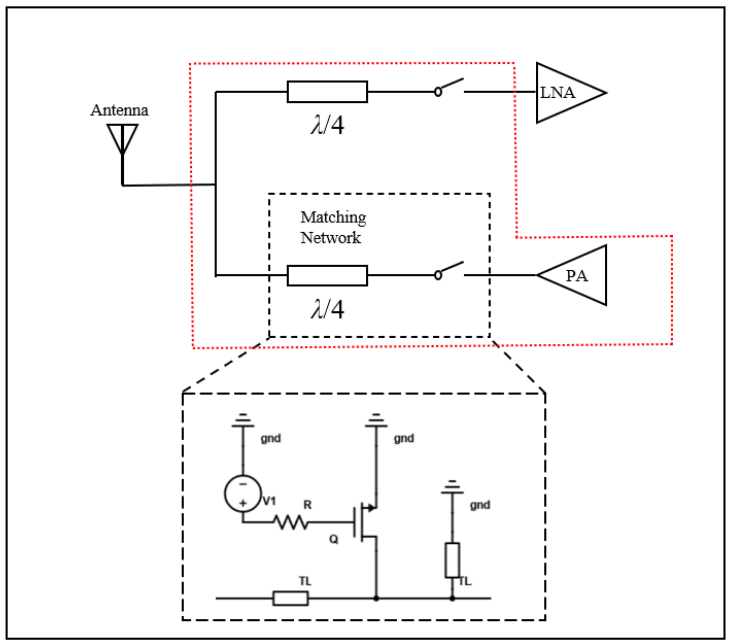


Figure 1.2: The main scope of this project is shown in the red box and the RF switch using nanowire transistors in shunt topology is shown in the black box.

Chapter 2
Theory

2.1 Metal-Oxide-Semiconductor Field-Effect Transistor

2.1.1 Metrics of the MOSFETs

The n-type MOSFET that operates as a switch is in the ON state when the gate voltage exceeds the threshold voltage and current flows between the drain and source, and on the contrary, is in the OFF state. However, this defective switch won't show a zero current during the OFF state due to the subthreshold effect. In the ON state, there are also two regions, linear region and saturation region, shown as Figure 2.1.

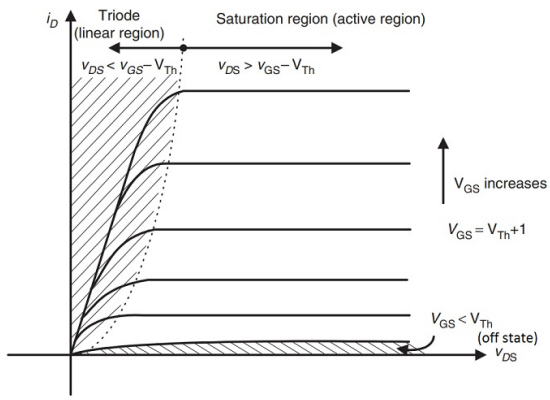


Figure 2.1: Drain current curves of an NMOS device working in linear, saturation, and cut off region (OFF state).

Since the drain current depends on the amount and the velocity of charges, a typical expression for the drain current in the linear region is

$$I_D = \mu C_{ox} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D^2] \tag{2.1}$$

where μ is the carrier mobility, C_{ox} is the gate capacitance, W and L are the gate length and the gate width, and V_G, V_{th}, V_D are the gate voltage, the

threshold voltage, and the drain voltage respectively. When the drain voltage V_D is large than $V_G - V_{th}$, the transistor runs into saturation region, and the current is defined by

$$I_{Dsat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_G - V_{th})^2 \tag{2.2}$$

The mobility μ in (2.1) and (2.2) can be given by $\mu = q\tau/m^*$, where q is the electric charge, τ is the average time interval between carriers colliding, resulting scattering, and m^* is the valid electron mass during the transportation [6]. When shorten the channel, the charge transports in a very short time, which may be lower than the average time τ. If there is no scattering in the channel, the transportation is called "ballistic". On the contrary, there are also carriers backscattering to the source. Then a factor R_c is to describe the backscattering coefficient when 0 for 'ballistic' and 1 for "backscattering", given by

$$R_c = \frac{L}{L + \lambda} \tag{2.3}$$

where λ is the mean free path and L is the gate length.

Then the drain current in (2.2) can be expressed in

$$I_D = WC_{ox}(V_G - V_{th})v_{therm}(\frac{1 - R_c}{1 + R_c}) \tag{2.4}$$

where v_{therm} is the intrinsic "Brownian" thermal velocity.

Reducing the gate length also introduces the short channel effect, leading to the loss of control by gate for the drain current. "Drain-induced barrier lowering" (DIBL) is one of the obvious results, which may cause increasing leakage current in cut off region. One possible solution to mitigate the short channel effect is to restrict the minimum length $L_{min} = 6\lambda_c$, where λ_c is the characteristic length of the transistor.

2.1.2 MOSFETs in RF Operation

Since the MOSFETs are non-linear devices, it is difficult to extract the parameters in RF operations if considering the large signal. Furthermore, in most of the RF operations, the signal swings within a limited range or is approximate to a DC value, which can be seen as linear. Thus, the small-signal model can be applied to analyze the signal, and the equivalent circuit is shown in Figure 2.2.

From the model, R_S, R_D, R_G are extrinsic resistances which contain the contacts and access resistances for each node [7]. The circuit inside the dotted rectangular is the intrinsic part of the transistor, including three capacitances C_{gs}, C_{gd}, C_{ds} and transconductance g_m and output resistance r_o.

There are two essential RF characteristics for transistors, f_T and f_{max}. The cut-off frequency f_T when the current gain becomes unity and the maximum oscillation frequency f_{max} when the power gain becomes unity are defined by

$$f_T \approx \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{2.5}$$

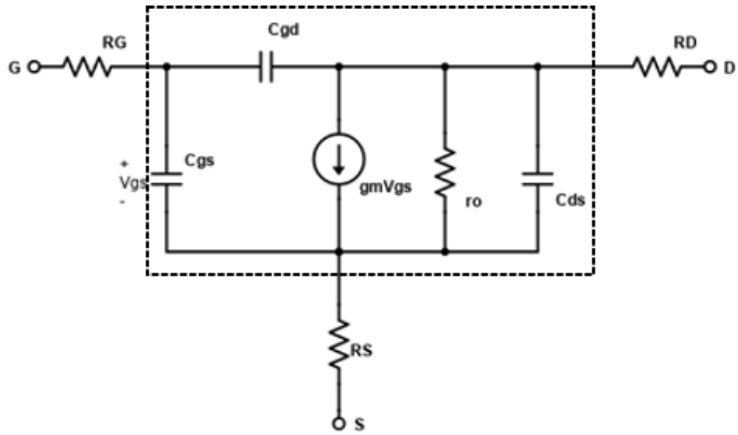


Figure 2.2: Common small signal model with intrinsic and extrinsic properties for a MOSFET.

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi R_g C_{gd}}} \tag{2.6}$$

respectively.

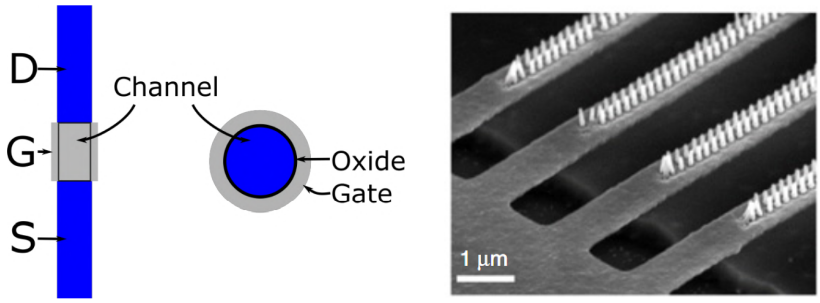
The next section will illustrate the small-signal model with S-parameter in details.

2.1.3 Vertical Nanowire MOSFETs

Common MOSFETs, such as silicon based and III–V compound MOSFETs, have shown superb performance in high frequency electronic device applications while demonstrating Moore's Law during the past decades. In the last few years, several planar MOSFETs with f_T and f_{max} reaching around 400 GHz have been proposed [8].

Dissimilar from ordinary MOSFETs, Nanowire (NW) transistors have attracted more and more attention due to excellent RF responses given by cylindrical structure. Figure 2.3 shows a common structure of a vertical NW transistor with a drain at the top, a source at the bottom, connected to the subtract, and a gate in the middle. In general, this structure, known as gate-all-around (GAA), reveals excellent control in dealing with short channel effect [6]. The characteristic length for NW transistors, λ_{nw}, is defined by (2.7), where ϵ_{si} and ϵ_{ox} are the permittivity of silicon and the gate insulator permittivity respectively, t_{ox} is the thickness of the insulating layer, and R is the radius of the NW [6]. Therefore, as mentioned in Section 2.1.1, the gate length can be scaled down due to the thin cylinder, together with the device size.

$$\lambda_{nw} = \sqrt{\frac{2\epsilon_{si}R^2 ln(1+\frac{t_{ox}}{R}) + \epsilon_{ox}R^2}{4\epsilon_{ox}}} \tag{2.7}$$



(a) (b)

Figure 2.3: A simple GAA structure for the vertical nanowire transistor (a) [10] and SEM picture after gate-finger fabrication (b) [8].

2.2 Radio Frequency Circuit Analysis

While designing RF circuit, the primary consideration is the operating frequency. Basic components in RF circuit, capacitors and inductors, provide the most of the reactance of the circuit, which is the imaginary part of the impedance. Once the frequency is determined, the capacitance and inductance can be derived as resonance at that particular point. There will be performance degradation in a frequency range around that point, in which an acceptable decline is called bandwidth.

2.2.1 Resonant Circuits

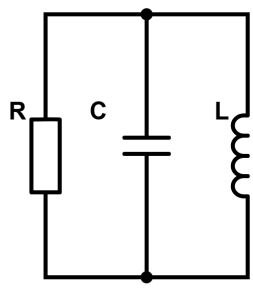


Figure 2.4: A typical RLC tank circuit resonated at frequency f_0 (or angular frequency ω_0) with the quality factor Q_P.

Typical resonant circuits consist of resistor, capacitor, and inductor with series or parallel connections. Figure 2.4 is a basic parallel RLC resonant tank, and its equivalent admittance of the circuit is given by

$$Y = Y_R + j(\omega C_P - \frac{1}{\omega L_P}) = Y_R[1 + jQ_P(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega})] \tag{2.8}$$

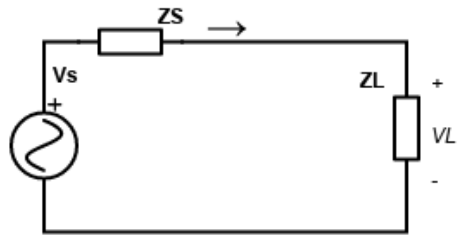


Figure 2.5: RF circuit for impedance matching, which $Z_L = Z_S$ for no reflection transfer and $Z_L = Z_S^*$ for maximum power transfer.

where ω_0 is the resonant angular frequency when the reactance is eliminated, given by

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_P C_P}} \tag{2.9}$$

and the quality factor Q_P, presenting the ratio of the storage energy and the dissipated power per cycle [11], is defined by

$$Q \equiv 2\pi * \frac{\text{maximum instantaneous energy stored in the network}}{\text{energy dissipated per cycle}} \tag{2.10}$$

In a high-Q circuit, the power loss slowly but at the price of limited bandwidth, shown in $BW = \omega_0/Q$. When designing RF circuit, there is always a trade-off between the quality factor and the bandwidth.

2.2.2 Transmission Line

When the alternating signal such as sinusoidal wave transfers through the transmission line, it may suffer a reflection signal from the load. It is usually ignored when in the low frequency or the DC signal. However, when the operating frequency is large, for example, at the GHz level, the wavelength inversely proportional to the frequency is as short as the physical transmission line length level. Thus, this reflection cannot be neglected. The wavelength is defined by

$$\lambda = \frac{v_p}{f} \tag{2.11}$$

where the v_p is the propagation velocity, which is proportional to the speed of light in vacuum. As mentioned in Section 1.2, the frequency in E-band is in the millimeter wave level. Figure 2.5 shows the power transferred from the source to the load, which Z_S and Z_L are the source impedance and the load impedance and V_S is an AC power source.

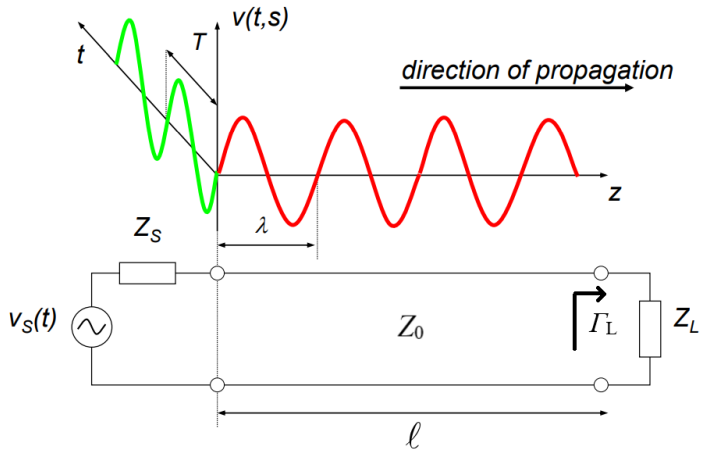


Figure 2.6: Power transfer through the transmission line with the characteristic impedance Z_0 and the propagation waveform in z domain and t domain [11].

Theoretically, the input signal can be transmitted without reflection only in the matching condition of $Z_L = Z_S$. While the maximum power transfer is conducted by the conjugate match, $Z_L = Z_S^*$.

Besides, there is a transmission line between source and load which shall be considered with a characteristic impedance Z_0, shown in Figure 2.6. The forwarding voltage propagation function in time domain t and position z is

$$v^+(t,z) = \left|V_0^+\right| \exp(-\alpha z)\cos[\omega t - \beta z + \phi_0^+] = Re(V_0^+ \exp[j\omega t - \gamma z]) \tag{2.12}$$

where the propagation constant $\gamma = \alpha + j\beta$ consists of the attenuation constant α and the phase constant $\beta = 2\pi/\lambda$, and ϕ_0^+ and V_0^+ is the phase shift and the amplitude in the forwarding direction.

The reflection voltage propagation function is the same as the forwarding direction, except the positive symbol changes to be negative. Thus, the total voltage at any time and position can be expressed in

$$v(t,z) = v^+(t,z) + v^-(t,z) \tag{2.13}$$

This work only investigates with the lossless transmission line, which means the attenuation constant α equals to zero, and (2.12) can be written in

$$v^+(t,z) = Re(V_0^+ \exp[j(\omega t - \beta z)]) \tag{2.14}$$

While the time dependence is included in the change of the complex amplitude crossing the line, (2.14) can be replaced by

$$v^+(z) = V_0^+ e^{-j\beta z} \tag{2.15}$$

Another critical factor to measure the RF network is reflection coefficient, Γ, describing the ratio of the reflected signal and the transmitted signal. The reflection coefficient at the load port can be expressed in

$$\Gamma_L = \frac{V_L^-}{V_L^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.16}$$

where $\Gamma_L = 0$ means the wave is transmitted without reflection and for 1, on the contrary, is fully reflected.

The transmission lines used in this work are considered as lossless, the impedance conducted by the lines is calculated in

$$Z_S = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l} \tag{2.17}$$

One of the conventional matching components used in this project, transmission line with physical length equals to $\lambda/4$, shows the convenient matching capability by adjusting the characteristic impedance in

$$Z_0 = \sqrt{Z_L Z_S} \tag{2.18}$$

2.2.3 Scattering Parameter

As shown in Figure 2.7, the two ports network is applied between the source and the load. Wave a_1 and a_2 are the waves from each port to another, and wave b_1 and b_2 are the waves reflected from each port. Scattering parameter is implemented to analyze the two ports network, which indicated the transmission and reflection coefficients for each port.

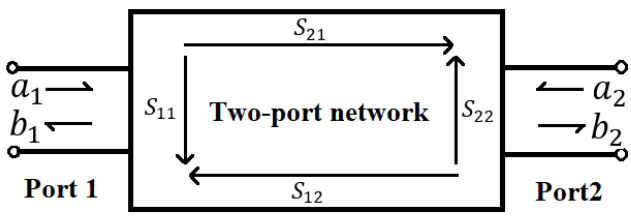


Figure 2.7: Singal flow in two ports network with corresponding transmission factor.

The relationship between the waves for each port and the S-parameter is explained by the following matrix:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.19}$$

Other derivative parameters, for instance, Y-parameter and Z-parameter, are the admittance and impedance for each port. In Figure 2.2, the intrinsic capacitance and extrinsic resistance can be solved by the Y-parameter and Z-parameter respectively [7], with

$$\begin{pmatrix} Y_{11}^i & Y_{12}^i \\ Y_{21}^i & T_{22}^i \end{pmatrix} \approx \begin{pmatrix} j\omega(C_{gs}+C_{gd}) & -j\omega C_{gd} \\ g_m - j\omega C_{gd} & C_{ds}+j\omega(C_{ds}+C_{gd}) \end{pmatrix} \tag{2.20}$$

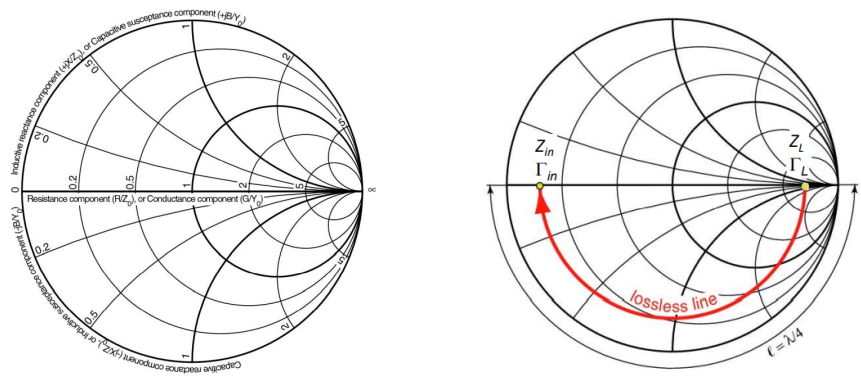
and

$$\begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \approx \begin{pmatrix} R_g+R_s & R_s \\ R_s & R_d+R_s \end{pmatrix} \tag{2.21}$$

However, the Y-parameter in (2.20) is calculated solely in the dot box in Figure 2.2, which shall be distinguished with the Z-parameter for the whole model.

2.2.4 Smith Chart

The Smith chart is a powerful tool to visualize the impedance or admittance and the reflection coefficient, assisting the matching in RF circuits. The x-axis and y-axis for origin coordinate are the resistance and the reactance, which mapping to the Smith chart by bending the y-axis to a circle, as 0 at the left for short circuit and as infinity at the right for open circuit, shown in Figure 2.8 (a).



(a) (b)

Figure 2.8: Smith chart (a) and a $\lambda/4$ lossless line transfer impedance by $Z_0 = \sqrt{Z_L Z_S}$ (b).

In addition, when mapping to the Smith chart, it is mostly transferred into normalized impedance by a characteristic impedance $Z_0 = 50\ ohm$. The positive resistance is loaded along the x-axis, while the upper half of the circle represents the inductive reactance and the lower half is for the capacitive reactance. An example of $\lambda/4$ transmission line with impedance changing is shown in Figure 2.8 (b).

2.3 Power Amplifier

Due to the long-distance transmission and power dissipation in propagation, the antenna is required to transmit with high output power, as shown in Figure 2.9. In order to increase the output power, power amplifier (PA), widely used in wireless communication design, is applied as the last component before the antenna. Thus, the gain, A_p, is used to quantify the amplification ability of the PA, in

$$A_p = 10\log_{10}(\frac{P_{out}}{P_{in}}) \tag{2.22}$$

With constant gain, although enlarging the input power is one possible method to increase the output power, it may bring the linearity problem toward PA. The linearity of the PA means the output and input power are linear until the compression point. The amplification is based on the DC supply and the output power is finite, therefore, the gain drops as the input power increases. The input power point that the gain drops 1 dB from a constant is called 1 dB compression point. In most of the designs, it is more preferable to operate with some backoff from that point to keep the PA linear which in this work is 3dB backoff.

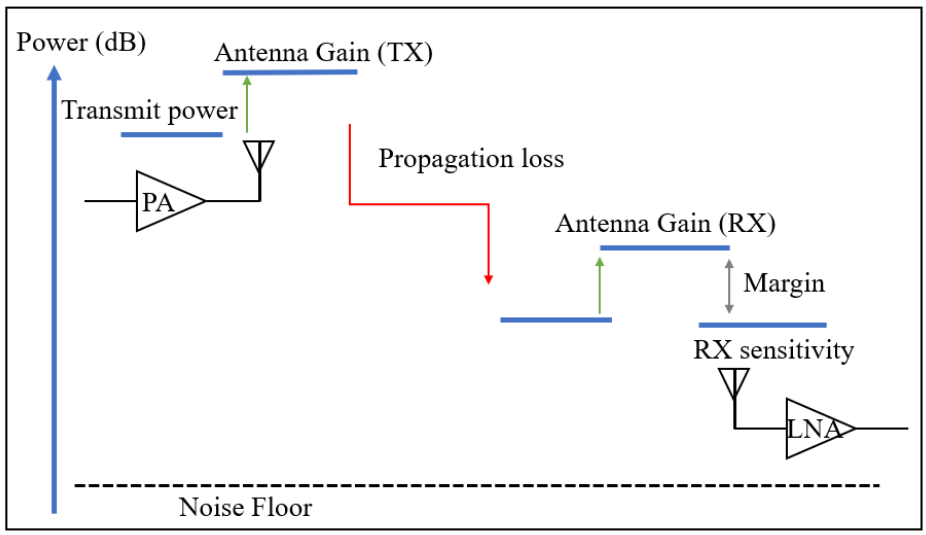


Figure 2.9: Wireless communication from transmitter to receiver and the power loss in propagation.

Another significant metric for PA, Power Added Efficiency (PAE), is defined by the ratio of the power gain and the DC input power. Since the PA amplify power by adding power from the DC power supply, PAE can directly present the contribution of the DC power to the PA.

$$PAE = 100\% \times \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.23}$$

An example of the relationship of the gain, 1dB Compression Point (1dB-CP) and PAE versus input power is shown in Figure 2.10.

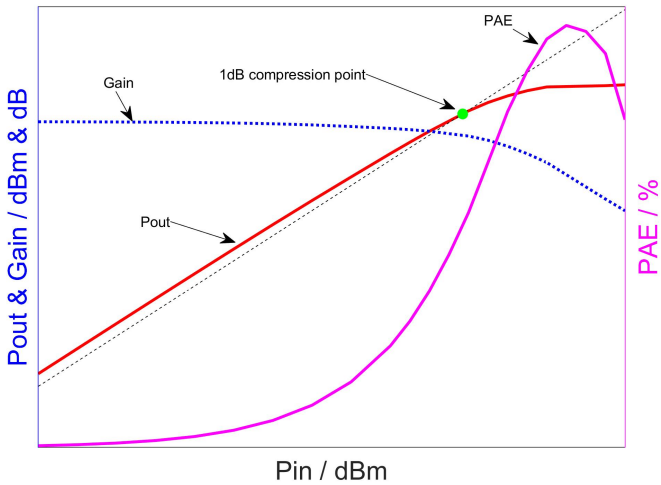


Figure 2.10: Example for the gain, 1dB-CP, output power and PAE in one plot and the maximum PAE usually shows up after the 1dB-CP.

2.3.1 Ideal Class-F Power Amplifier

Considering the PAE and the output waveform, PA can be classified into Class-A, Class-B, Class-AB, Class-F, etc. The conduction angle of each classification and relative PAE are shown in Figure 2.11 (a). Among them, Class-A to Class-C are distinguished by bias points, and class-D and above are distinguished by network configuration. This project solely investigates the behaviors of the Class-F power amplifier.

The drain voltage of the Class-F PA is in square waveform by setting infinite odd harmonic tanks at the output stage, as shown in Figure 2.11 (b). For the drain current in half-sinusoid waveform is achieved by setting even harmonics instead [13]. Both harmonic tuning shall use a Class-A bias point. Thus, the drain voltage and current can be expressed in

$$V_D = V_{DD} + V_m \sin \omega t + \sum_{n=3,5,7\ldots}^{\infty} V_{mn} \sin(n\omega t) \tag{2.24}$$

and

$$I_D = I_{dc} + I_m \sin \omega t + \sum_{n=2,4,6\ldots}^{\infty} I_{mn} \sin(n\omega t) \tag{2.25}$$

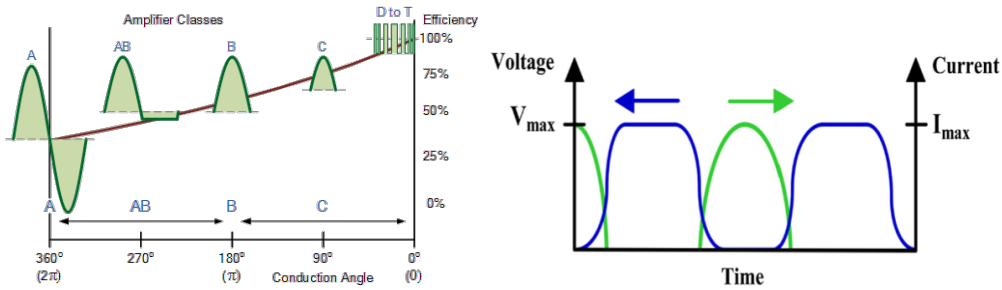


Figure 2.11: Power amplifiers work in Different classes and the corresponding PAE (a) [12] and Class-F Power amplifier voltage waveform in blue and current waveform in green (b) [13].

The relative circuit for ideal Class-F PA is shown in Figure 2.12. It results in zero impedance for even harmonics and infinity impedance for odd harmonics at the output matching network, leaving the impedance at the baseband matching to the load. Therefore, there is no harmonic power transmitted to the load, which the PAE theoretically reaches to 100%. However, due to the complexity and the efficiency of increasing the order of harmonic tanks, there is ordinary a 3^{rd} order or 5^{th} order applied in practice, with PAE lower than 100%.

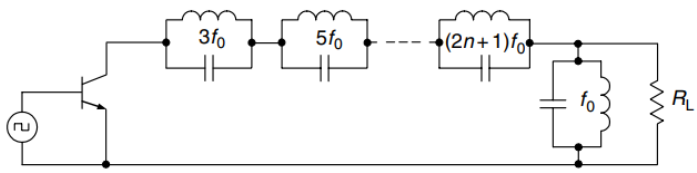


Figure 2.12: Ideal Class-F power amplifier circuit with parallel LC resonate tanks [14].

2.3.2 Class-F Power Amplifier with Series Quarter-wave Transmission Line

As shown in Figure 2.13, the resonate tanks in Figure 2.12 can be replaced by a $\lambda/4$ transmission line. In theory, the transmission line provides short circuit for the even harmonics and open circuit for the odd harmonics. This structure is normally used in high frequency operation, which is difficult to realize lumped elements but easy to achieve the millimeter wavelength level transmission lines. [14]. Ideally, lossless quarter-wave TL conducts the pure resistive impedance. The characteristic impedance can be expressed by (2.18).

When at the low input level, the device is driven in voltage-controlled current source mode. As the input increase, the device works in non-linear mode,

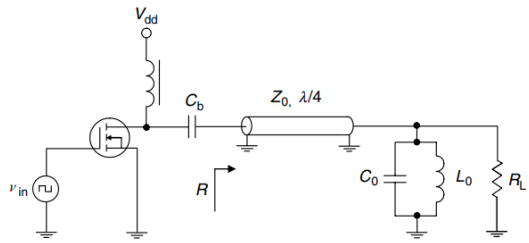


Figure 2.13: Class-F power amplifier circuit with series $\lambda/4$ TL and a parallel LC resonate tank [14].

and both power and voltage are saturated, leading to all the harmonic weights increase. Thus, with output network configuration in Figure 2.13, the output voltage waveform at V_{ds} port can be driven into square wave and the current waveform becomes half-sinusoid. The output signal at R_L can remain the sinusoid waveform at the high input voltage due to even harmonics are shorted and odd harmonics are reflected at the LC resonate tank.

Chapter 3

Methods

This work contains design and simulation the basic single-pole double-throw (SPDT) RF switch operating in E-band, and load pull simulations to obtain the optimum load impedance of the PA. Subsequently focusing on the behaviors of the up-link band, which is the PA path of the switch, and adjusting the output matching to achieve Class-F PA.

The simulation tools, including Keysight Advanced Design System (ADS) and Matlab, are used in this work, together with the NW transistor developed by the Division of Electromagnetics and Nanoelectronics, LTH, Lund university. Since the switch operates in E-band, the bandwidth for this work only needs to cover from 71 GHz to 86 GHz, in which the central frequency is set to $f_c = 78$ GHz.

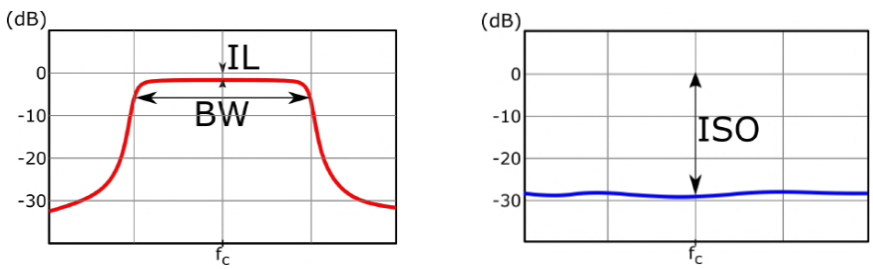


Figure 3.1: IL in the on-path shall be low within the bandwidth (BW) (a) and high ISO in the off-path (b) [10].

Two important parameters, insertion loss (IL), and isolation (ISO), decided the main performance of the RF switch. Since there are two paths in the switch, when one is ON, the power dissipation of the path shall be low, representing low IL, and the other is OFF, it shall reject the signal passing through this path, representing high ISO. The basic concepts of the IL and ISO is illustrated in Figure 3.1, where $IL = 1/S_{21,ON}$ and $ISO = 1/S_{21,OFF}$ [15].

3.1 Basic SPDT RF Switch Design

This project focuses on the SPDT switch with one input port connected to antenna and two output ports connected to LNA and PA, as shown in Figure 3.2.

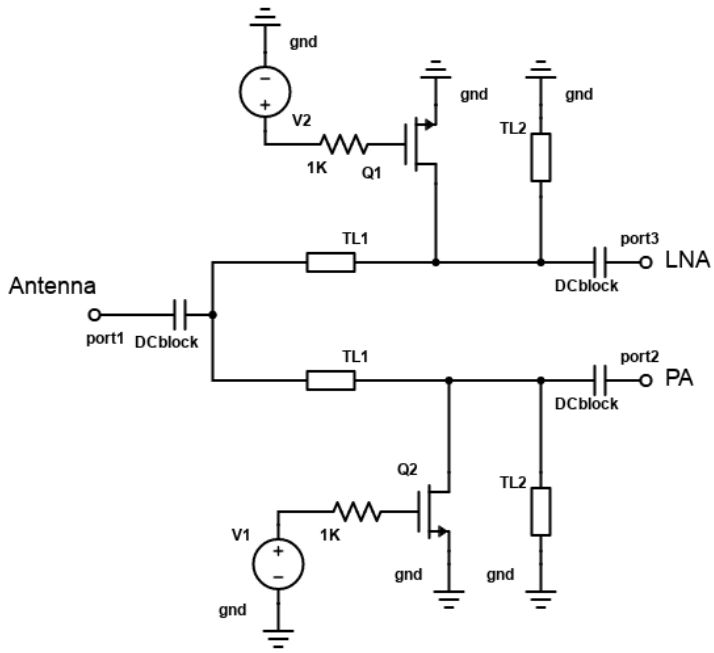


Figure 3.2: A basic SDPT RF switch schematic with quarter wave transmission line TL_1 and inductive short-stub TL_2. The input port is connected to the antenna and output ports are connected to LNA and PA.

Conventionally, the antenna is matched to 50 ohms within a limited bandwidth. For instance, the central frequency f_c and bandwidth BW are 78 GHz and 15 GHz respectively, thus, the quality factor, Q, as illustrated in Section 2.2.1, is at around 5. Thus, there is a $\lambda/4$ transmission line between the input port and the transistor to match the load impedance. Two transistors are derived by the external control signal and only one transistor is turned on at a time. The transistor in the off-state and on- state works in the cutoff region and the linear region respectively. In the on-path, the transistor is in the off state, then the resistance of the transistor R_{off} shall be as large as possible while the capacitance C_{off} shall be minimized. Since the R_{off} is generally in thousand ohms level, it is ignorable when connects to the parallel characteristic impedance at 50 ohms. Thus, the C_{off} is the critical factor that affects the matching. On the contrary, for the off-path, the transistor is in on state with corresponding resistance R_{on} and capacitance C_{on}. In this case, R_{on} is the dominant factor that affect the off-path of the switch which shall keep low. As

mentioned in Section 2.2.3 and Section 2.1.2, the small signal model for the switch transistor can be simplified in Figure 3.3, where

$$R_{on} = \frac{1}{g_d} \approx R_s + R_d \tag{3.1}$$

and

$$C_{off} \approx C_{gd}||C_{gs} + C_{ds} \tag{3.2}$$

In order to eliminate the leakage of the RF signal, the control signal in the gate is in series to a 1k ohms resistor [15]. When doing the simulation in ADS, R_{on} can be calculated by sweeping V_{ds} at $V_{gs} = 0.5$ V and solving the slope of the curve at V_{ds} around 0, while C_{off} is acquired by Y-parameter analysis.

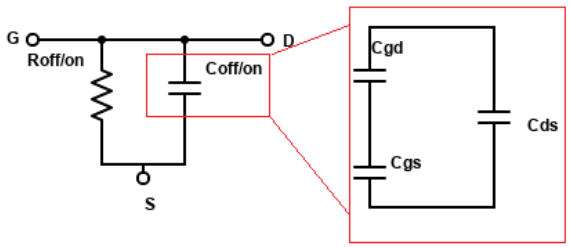


Figure 3.3: Simplified small signal model for the transistor in RF switch with a 1k ohms resistor at the gate. The $C_{off/on}$ consists of C_{gd}, C_{gs}, and C_{ds}, where $C_{ds} << C_{gd}||C_{gs}$.

The parallel transmission line short-stub in Figure 3.2 with proper length configuration can be seen as an inductor, which is resonant with C_{off} at the central frequency f_c. Thus, as (2.9), when the circuit operating around f_c, the imaginary part of admittance in on-path is compensated to reach around zero. The length of the lossless short-stub lower than $\lambda/4$ can be transformed from (2.17),

$$l_{stub} = \frac{\lambda}{2\pi} \arctan(\frac{\omega L_{stub}}{Z}) \tag{3.3}$$

where Z is the characteristic impedance of the short-stub, which is set to the typical value, 50 ohms, in this project.

3.2 DC Bias Point Analysis

DC bias is mostly set to the input and output ports of the transistor, raising the DC voltage to meet the requirements of RF operation. In the common source (CS) amplifier, although setting DC bias to the extreme conditions, for instance, setting maximum V_{gs} and maximum V_{ds} to achieve the maximum delivered gain and maximum PAE respectively, it may lead to risks for the overloaded devices or unstable operation. The best bias point for transistor in the most case is the

midpoint between saturation and cutoff. In this work, the bias point Q for the NW transistor with $NW = 500$ and $NF = 10$ is shown in Figure 3.4, with the optimum $V_{gs} = 0.4V$ and $V_{ds} = 0.7V$.

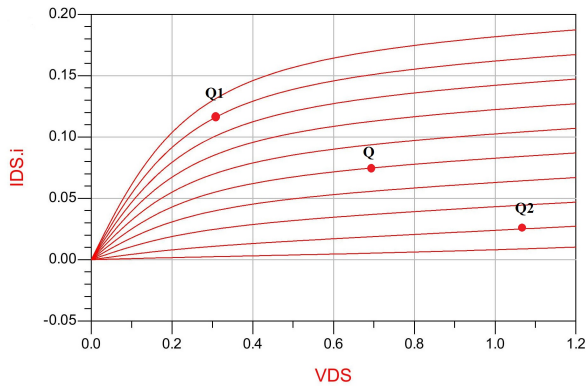


Figure 3.4: DC sweep for $NW = 500$ and $NF = 10$ NW transistor. The Q point is at $V_{gs} = 0.4V$ and $V_{ds} = 0.7V$, Q_1 is at $V_{gs} = 0.8V$ and $V_{ds} = 0.3V$, and Q_2 is at $V_{gs} = 0.1V$ and $V_{ds} = 1.1V$.

The bias point will stick to these values in different sizing of the transistor, instead, there will be two control groups with bias points in Q_1 and Q_2 while doing the load pull simulation.

3.3 Load Pull Simulation

Load pull simulation is a common RF analysis tool which measures the behaviors of the device under test (DUT), usually a transistor, under different load impedances. A common setup interface for two-tone load pull simulation in ADS is shown in Figure 3.5 [16]. The started source impedance is set to a low value, 10 ohms, while the harmonic impedances are set to a high value, 1000 ohms. Once obtained the optimum load impedance, the source pull can be done if necessary, and turn to load pull again with the optimum source impedance. This process may be repeated several times in order to improve accuracy. Sometimes a small signal matching on the input side is sufficient for less complex analysis.

The Smith chart in the upper-right corner in Figure 3.5 contains the number of load impedance points, and all of the points shall be covered within the circle with tunable center and radius. The result of the PAE and output power will be displayed in a contour plot, in Figure 3.6 (a), while the maximum PAE and maximum output power can be found at the center. Therefore, with mapping to the contour plot, the relative optimum load impedance is extracted by Figure 3.6 (b).

For each input power, there is one optimum impedance point. As a result, sweeping the input available power, P_{avs}, can simulate PA's behaviors as intro-

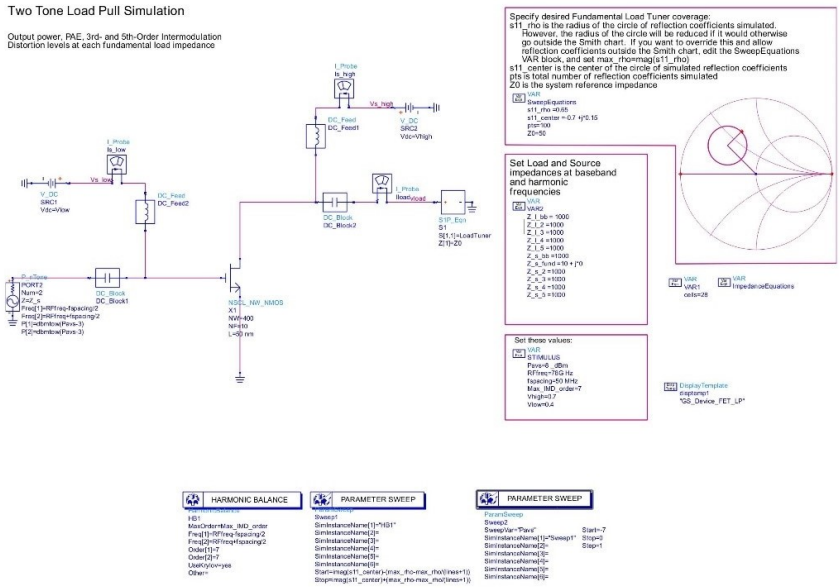
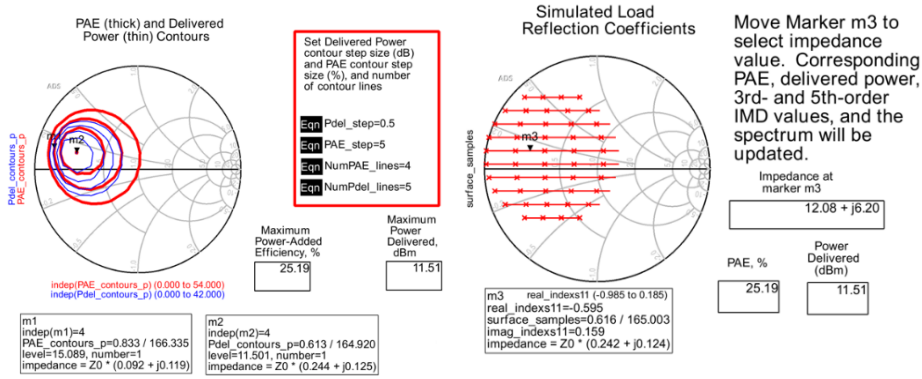


Figure 3.5: Two-tone load pull simulation interface in ADS.



(a) (b)

Figure 3.6: An example for the main part of the load pull simulation result in ADS, consisting of PAE and delivered gain contours in (a) and reflection coefficients and corresponding impedance at specific selected point in (b).

duced in Section 2.3. However, due to the restriction of ADS, high P_{avs} may cause results unable to converge, which will influence the results in the next Chapter. The final step is to sweep the size of the NW transistor, recording and comparing the results with each other to obtain a reasonable size.

3.4 RF Switch with Class-F PA Load

As mentioned in Section 2.2.2 and Section 3.1, the load impedance of the RF switch in the PA path will be conjugate matched to the result from load pull simulation. However, the characteristic impedance of the transmission line (TL), expressed in (2.18), will be lower than 50 ohms, leading to the low ISO at the PA path. The real part of the load impedance, thus, is considered to be more than 10 ohms. Besides, increasing the size of the NW transistor in the PA path is also a feasible solution to compensate the ISO. In order to compensate this effect, there is a simulation which replace the PA load impedance from 50 ohms to the load pull result before implementing a true Class-F PA load.

The overall schematic of RF switch with Class-F PA load is shown in Figure 3.7. Compared to Figure 3.2, a new short-stub, TL_3, is implemented to compensate the imaginary part of the PA load. A new LC resonate tank at the central frequency f_0 is implemented to filtered out the harmonics. Furthermore, the matching network in the black rectangular is not only used for the RF switch, but also dealing with the odd and even harmonics at the output of PA, realizing a Class-F PA.

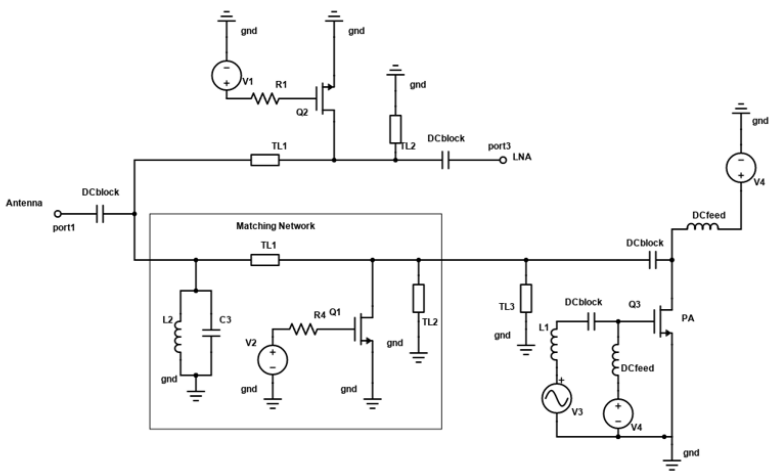


Figure 3.7: Schematic for RF switch with Class-F PA load which output matching network filtering odd harmonics.

3.5 Simulation Setup

In this work, the component TLIN used in ADS can be seen as ideal transmission line with the length transformed to degree by (2.17). The ideal wavelength at 78 GHz is equivalent to 3.8 mm which will be reduced by $\sqrt{e_r}$ if implemented on-chip. The central frequency f_c is set to 78 GHz, as a rough midpoint in the E-band. The length of the NW transistors in this work is set to $L_g = 50$ nm. The control voltage that switches the NW transistor will alternate between 0 V or 0.6 V, representing the OFF and ON states, respectively.

Table 3.1 shows the metrics of interest for NW transistors with different sizing, where $R_{on}C_{off}$ is the product of R_{on} and C_{off}, intuitively presenting the performance of the switch.

NW	$R_{on}(\Omega)$	$C_{off}(fF)$	$R_{on}C_{off}(fs)$	$L(pH)$	$Length(\lambda)$
400	7.6	20.8	158	200	0.17
800	3.8	41.6	158	100	0.12
1200	2.5	62.1	155	67	0.09
1600	1.9	83.3	158	50	0.07
2000	1.5	104.1	156	40	0.06

Table 3.1: Different metrics of NW transistors and the corresponding compensated inductance with conversion to the short-stub length.

Apart from the parameter setup, the simulation method setup in ADS is to sweep the S-parameter with one input port and two output ports from 0.5 GHz to 120 GHz in 0.5 GHz step size. The schematic in ADS is shown in Figure 3.8, where the IL and ISO can be measured at once as long as the schematic is symmetrical. In this work, the DC block and DC feed are used under ideal conditions with infinity capacitance and infinity inductance, respectively.

Figure 3.9 shows the schematic of RF switch with a PA load in ADS. The fundamental band is matched by a short-stub and the $\lambda/4$ TL with different impedance. The input AC signal of the PA uses a 10 ohms source impedance and the input frequency at 78 GHz. Both transient and harmonic balance simulation are added in order to measure the output waveform and harmonic performances. The remaining settings for PA depend on the load pull simulation. In addition, as the PA path transferring signal from port 2 to port 1, the forward transmitted coefficient will be inverted to S_{12}. At last, a new inductor is implemented for input matching of the Class-F PA, further improving the performance. In order to investigate the performances of the RF switch and Class-F PA directly, the circuit will be separated into two parts if necessary.

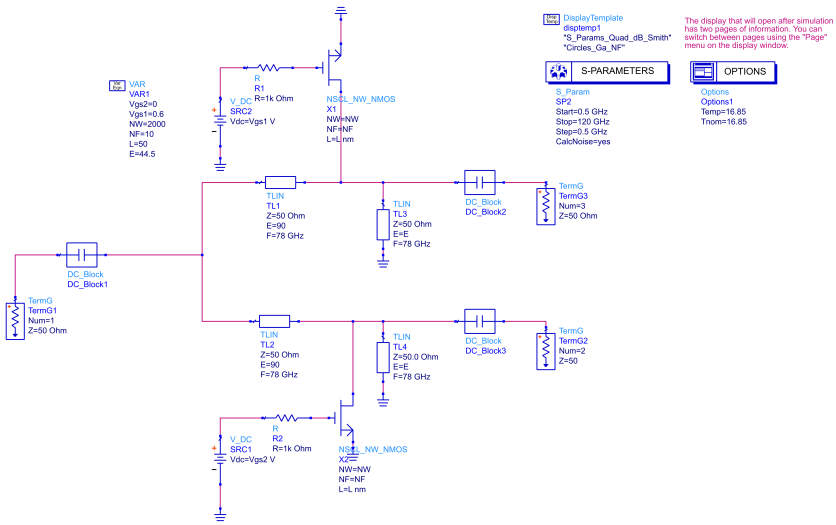


Figure 3.8: Schematic and simulation settings for Basic RF switch.

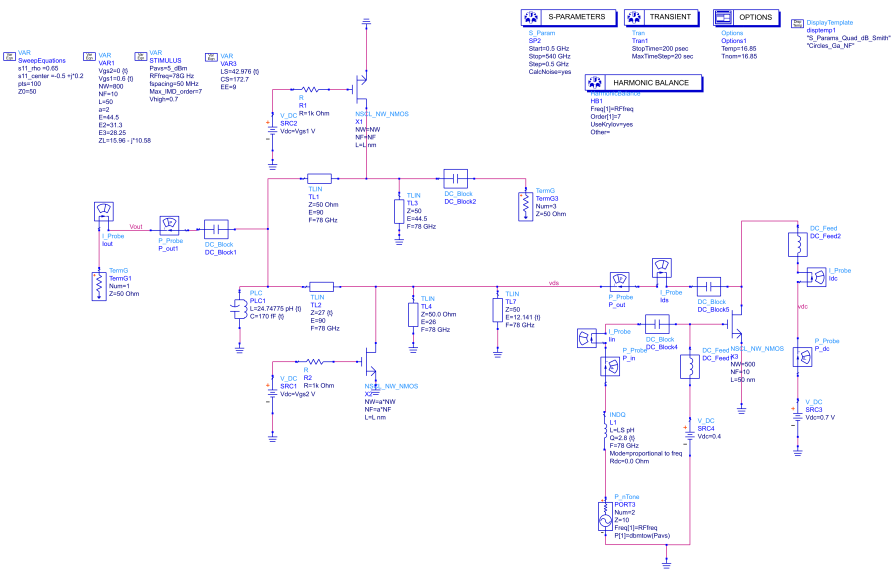


Figure 3.9: Schematic and simulation settings for RF switch with Class-F PA load.

Chapter 4
Results

4.1 Basic RF Switch Simulation

For the basic RF switch schematic, the S-parameter are shown in Figure 4.1, with port 1 connected to the antenna and port 2 connected to the PA. The input reflection, S_{11}, falls to the bottom at 78 GHz, while the output reflection, S_{22}, maintains the lowest level from 65 GHz to 90GHz. The IL and ISO are represented by S_{21_ON} and S_{21_OFF}. In general, the results are in line with expectations, with the best performance at 78 GHz with 2.3 dB IL and 27 dB ISO, and high performance in the E-band. Since the basic RF switch circuit is fully symmetric, these results are applicable for the LNA path.

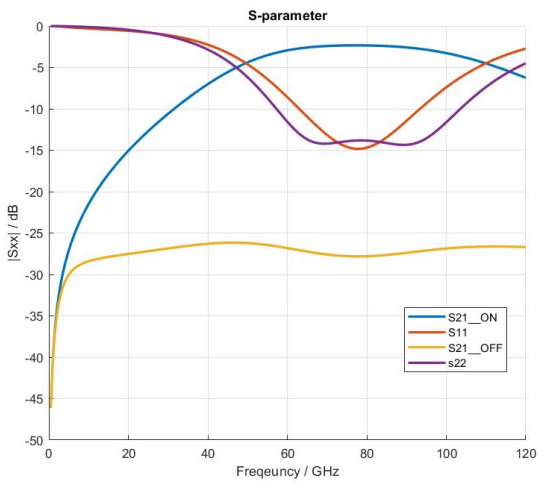


Figure 4.1: Basic schematic simulation result for 800 NW and 10 NF transistor.

As explained in Table 3.1, when increasing the size of the transistor, the relative Ron decreases, leading to better ISO in the off-path. However, the cost is higher IL due to the increasing C_{off}. From Figure 4.2, the IL can be seen as a linear degradation with respect to the transistor size. Additionally, the ISO improves

significantly when the transistor size increases from 400 to 800, followed by an approximate linear relationship from 800 to 2000. In this work, the switch will focus on the performance of the PA path, which means the IL will be one of the critical factors in designing the circuit. Consequently, small size transistors with lower IL may be the object of attention.

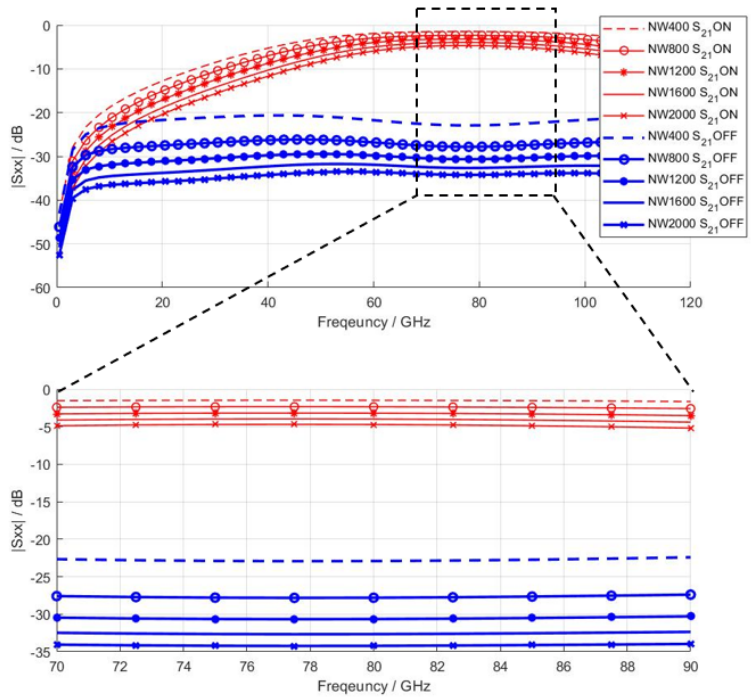


Figure 4.2: IL and ISO results for different size transistors and its zoom in version in E-band.

4.2 Load Pull Simulation

From the DC sweep in Section 3.2, the bias voltage V_{gs} and V_{ds} are 0.4 V and 0.7 V respectively. Load Pull simulation can draw PAE contour and evaluate the load impedance that makes the maximum PAE and output power. Figure 4.3 shows output power versus input power on the 400 NW and 10 fingers model. Due to the high input power, mostly higher than the 1dB-CP, it cannot converge that lead to output power at exactly 30 dBm and they shall be considered as dummy points. In this case, Matlab tool can help to interpolate the data and trace back the origin points. For the rest of figures shown in this thesis, the dummy points are all fixed.

1dB-CP, PAE, and gain results for NW from 400 to 800 and NF from 5 to 20 are shown in Figure 4.4 Increasing the NW improves the 1dB-CP by around 1 dBm / 100 NW, while increasing the NF may cause a slight drop on the contrary. There

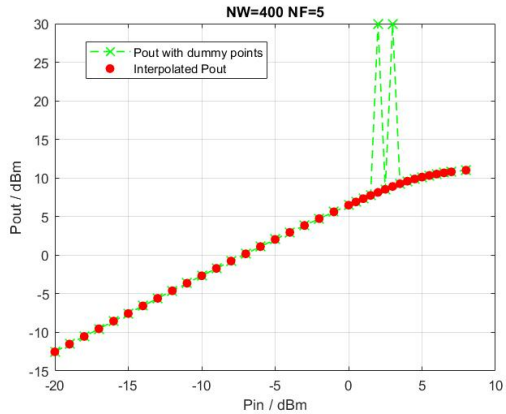


Figure 4.3: Example of output power with error and fixed by interpolation.

is a significant improvement for PAE from 5 NF to 10 NF, while that from 10 to 20 is narrowly changed until high input power. Additionally, the gain remains the same level for all transistor sizes because of the same topology of the CS amplifier.

Although increasing NWs can acquire more gain and power added efficiency apparently, the price is the decrease of the impedance in real part. This can be critical when doing matching network to the switch, especially in the LNA path, as explained in Section 3.4 In addition, it is often necessary to back off a few dBm below the 1 dB compression point to keep the linear operation, especially in quadrature amplitude modulation (QAM) [17]. Although there is no specification for the backoff power, 3 dB is adequate for 16-QAM. Table 4.1 indicates PA's behaviors for each model which input backs off 3 dB from the 1dB-CP. The corresponding load impedance trace in Smith chart is shown in Figure 4.5

NW	Pin(1dBCP) /dBm	NF					
		5		10		20	
		Pout /dBm	PAE/%	Pout /dBm	PAE/%	Pout /dBm	PAE/%
400	-5.0(-2.0)	4.73	8.15	4.85	8.41	4.88	8.48
500	-4.0(-1.0)	6.13	8.93	6.33	9.42	6.38	9.55
600	-3.4(0.4)	6.91	9.09	7.19	9.82	7.27	10.04
800	-1.5(1.5)	8.78	10.33	9.28	11.90	9.40	12.22

Table 4.1: Pout and PAE results for sweeping the transistor sizes and Pin has 3 dB backoff at each 1dB compression point.

Since this work only represents the output stage of the PA, there is no need to design a high gain amplifier, more than 5 dB may be sufficient for the design. Considering the load impedance is preferable to be greater than 10 ohms, the transistor with 500 NW and 10 NF is applied for the following design.

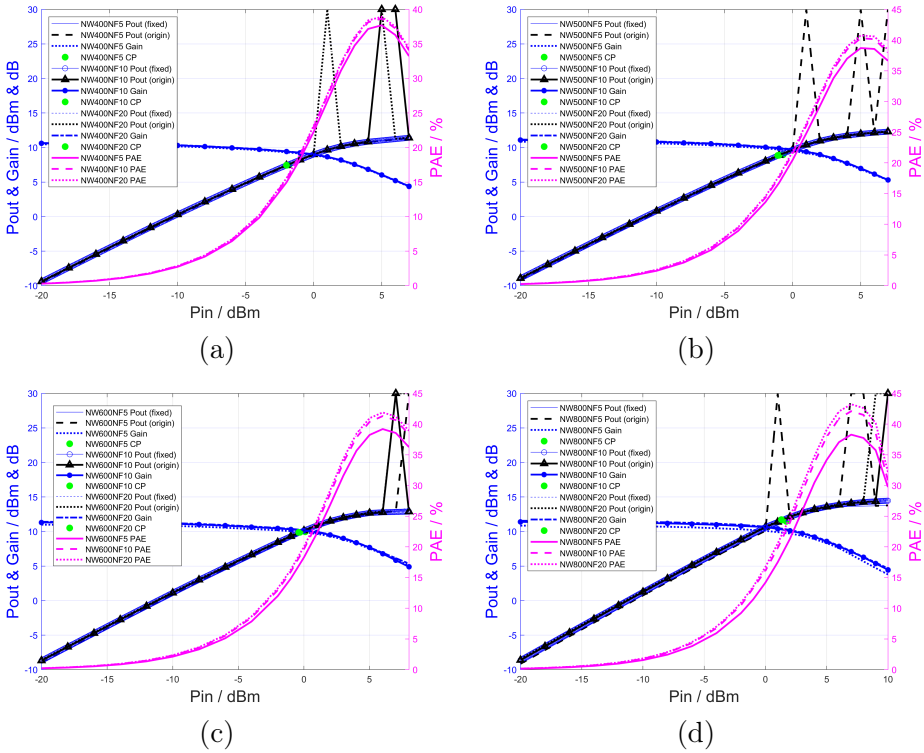


Figure 4.4: Load pull simulation results for PAE, Gain, 1dB-CP and Pout both in origin and interpolated lines for 400 NW (a), 500 NW (b), 600 NW (c), and 800 NW (d).

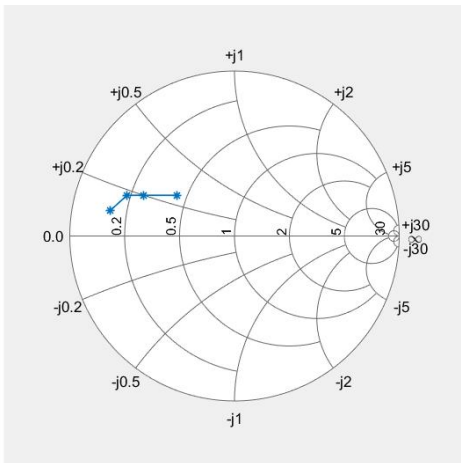


Figure 4.5: Output impedance for 400, 500, 600, 800 NW transistor from right to left respectively. Besides, the impedance will not be change according to the number of fingers.

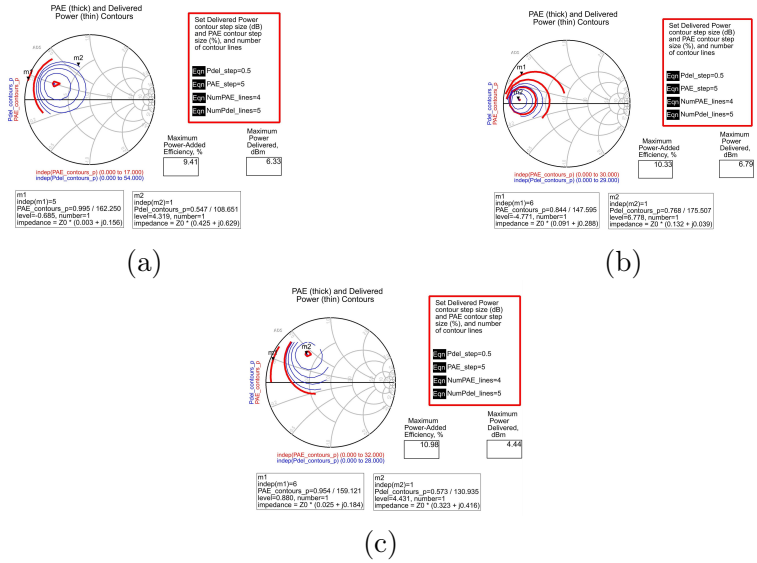


Figure 4.6: PAE and Pout contours in ADS for Q (a), Q_1 (b), and Q_2 (c).

The load pull simulation results above are based on the DC bias point at $V_{gs} = 0.4V$ and $V_{ds} = 0.7V$, which is the Q point in Figure 3.4. Simulation results of different DC bias points Q_1 and Q_2 with input power 3 dB lower than 1dB-CP are shown in Figure 4.6. Compared to the Q point, the Q_1 point has less operation space for the upper level of the input signal, while the lower level for Q_2, instead. From Table 4.2, the P_{out} and PAE are at the same level for three operating voltage. The 1dB-CP of Q_1 increases while the gain drops drastically, which is not enough for the PA design. On the contrary, the results for Q_2 have higher gain and lower 1dB-CP. Furthermore, High V_{ds} may result in heavy workload for the transistor. In fact, the bias point Q_2 is used for Class-B amplifier with a theoretical PAE peak at 78.5%.

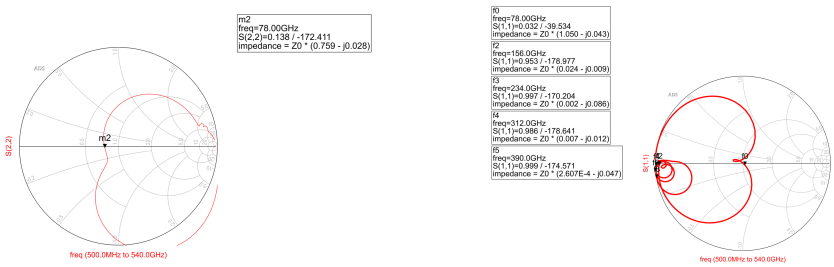
Operating voltage /V	Pin(1dBCP) /dBm	Pout /dBm	PAE /%	Gain /dB
$Q, V_{gs} = 0.4, V_{ds} = 0.7$	-4(-1)	6.33	9.42	9.88
$Q_1, V_{gs} = 0.8, V_{ds} = 0.3$	4(7)	6.79	10.33	2.79
$Q_2, V_{gs} = 0.1, V_{ds} = 1.1$	-8(-5)	4.44	10.98	12.44

Table 4.2: Load pull simulation results for different bias points, Q, Q_1 and Q_2, at $NW = 500$ and $NF = 10$.

4.3 RF switch and Class-F PA

In this section, the setup values of the PA is originated from the load pull simulation, which shall be 500 NWs and 10 NFs. The load impedance is $12.9 + 10.0i\ \Omega$ at the central frequency and the DC biasing for the transistor is $V_{gs} = 0.4$ and $V_{ds} = 0.7$.

With appropriate tuning of the input matching and output matching for the circuit in Figure 3.9, the input and output reflective coefficients are shown in Figure 4.7 a and Figure 4.7 (b) respectively. However, the input matching simply uses one inductor with quality factor 2.8 at 78 GHz, leading to the defective matching result. Considering the PA in this project is limited in the output stage, there will be an more complicated intersection matching between driven stages and the output stage in practice. The output matching at the antenna port is matched to 50 Ω at the central frequency f_0 and shorted for the odd and even harmonics f_2 to f_5. It is different from the output port of the PA, V_{ds} port, which is shorted for even harmonics and opened for odd harmonics, as shown in Firgue 4.8.



(a) (b)

Figure 4.7: Input reflection coefficient at the PA input port (a) and output reflection coefficient at the antenna port (b).

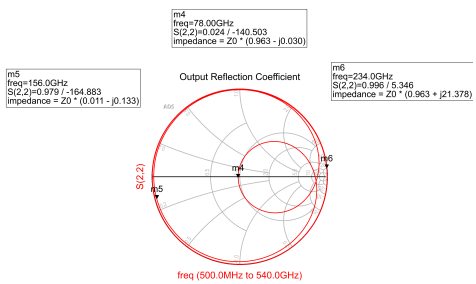


Figure 4.8: Output reflection coefficient at V_{ds} port.

Compared to the load pull simulation results in Figure 4.4, the Class-F PA shows superior performances on PAE and maximum output power P_{outmax}, as shown in Figure 4.9. The maximum PAE rises from 42% to 52% and the maximum output power rises from 12 dBm to 19 dBm.

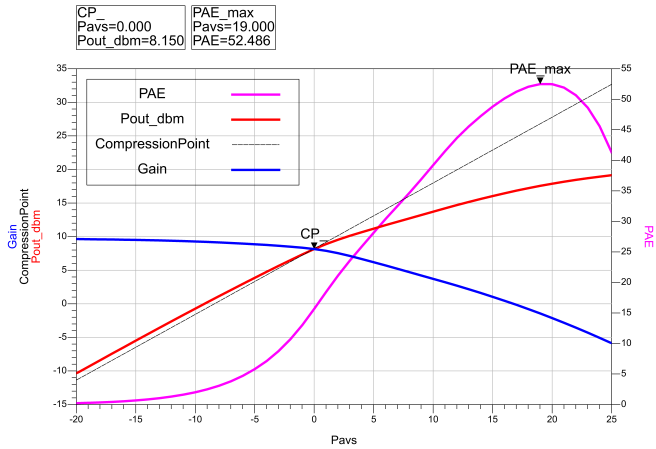


Figure 4.9: PAE, 1dB Compression Point, Gain and P_{out} for the Class-F PA.

Figure 4.10 shows the overall comparison for the input and output voltage and V_{ds}. Figure 4.11 shows the output waveforms and their relative harmonics for V_{ds} port and the antenna port, V_{load}. The input power is at 6 dBm, which is 6 dBm higher than the 1dB-CP. The PA with such input power obviously operates in the non-linear region, resulting in increased harmonics. Class-F PA suppresses even harmonics and reflects odd harmonics to V_{ds} port. Therefore, the output voltage gradually becomes a square waveform, and the output current shows a half-sinusoidal wave. For the antenna port, even harmonics are shorted to the ground while odd harmonics are reflected back to V_{ds}, as a result, only fundamental wave transfers to the antenna.

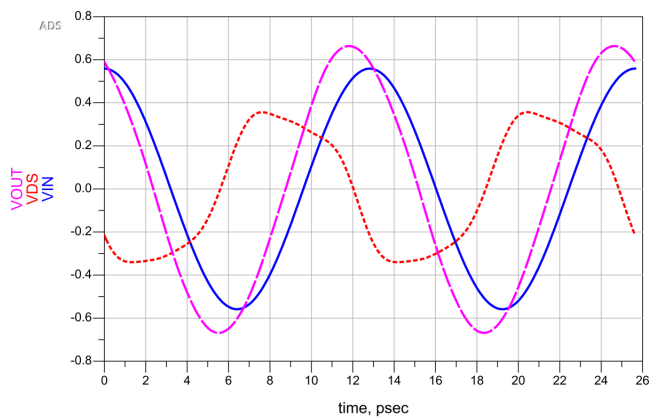


Figure 4.10: Output voltage waveforms for V_{in}, V_{ds} and V_{load}.

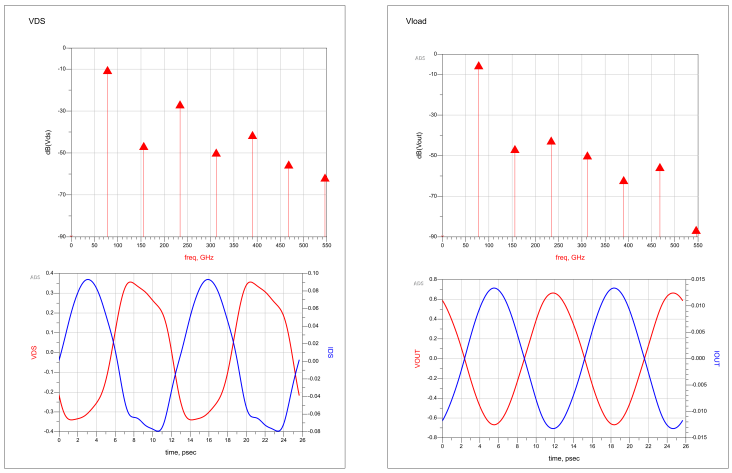


Figure 4.11: Output voltage and current waveform and their relative harmonics at V_{ds} port and the antenna port with $P_{in} = 6dBm$.

For the RF switch with Class-F PA load, the insertion loss and the isolation are different for the PA path and the LNA path due to the asymmetrical design. Figure 4.12 presents the performances of RF switch with Class-F PA load, including a comparison path from basic RF switch in Figure 4.1. The IL of PA path has slightly improvement for the up-link band from 71 GHz to 76 GHz and the ISO is almost 3 dB lower than that of basic RF switch. However, the performances of LNA path are degraded due to the compromise to the performances of PA path.

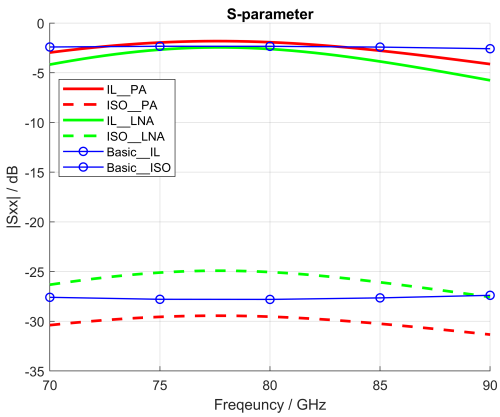


Figure 4.12: IL and ISO results of RF switch with Class-F PA load for different paths.

4.4 Benchmarking

The results in this works are from simulation results, which include a bunch of ideal components and conditions and are unverified in the real circuit. Nevertheless, this work proofs the feasibility of using RF switch as an output matching network to Class-F PA.

In this section, there are two benchmarkings for the RF switch itself and the Class-F PA as shown in Table 4.3 and Table 4.4 respectively.

Ref.	Topology	Process	BW (GHz)	IL (dB)	ISO (dB)
(This work)	$\lambda/4$-shunt (basic)	Vertical III-V NW	58-105	2.3	27
(This work with Class-F PA load)	$\lambda/4$-shunt (PA path)	Vertical III-V NW	66-93	1.8-4.8	29-31
(This work with Class-F PA load)	$\lambda/4$-shunt (LNA path)	Vertical III-V NW	68-89	2.4-5.4	25-27
[15]	$\lambda/4$-shunt	50nm InGaAs mHEMT	52-168	2.1-5.1	35-52
[18]	$\lambda/4$-shunt	90nm CMOS	50-70	<2	>27
[19]	Distributed 5 shunt HEMT's	GaAs PHEMTs	40-85	<2	>30

Table 4.3: SPDT RF switch performances comparison.

	(This work)	[20]	[21]	[22]	[23]	[24]
Topology	Single stage Class-F	Single stage Class-F	Stacked transistors Class-E	Fully-integrated 3-stage PA	2-stage double-stacked Class-F^{-1}	2-stage Class-AB
Process	Vertical III-V NW	500nm InP HBT	90nm SiGe BiCMOS	130nm SiGe BiCMOS	130nm SiGe BiCMOS	22nm FinFET
Vdd (V)	0.7	2.2	4.4	2.3	4	1
Frequency (GHz)	78	101	85	90	38	75
Peak PAE (%)	52.4	25.4	19.1	15.4	30.1	26.3
Gain (dB)	10	5	17	10.6	22.1	16.6
1dB-CP (dBm)	0	>6	2	9	-3	-10
Psat (dBm)	19	11	22	19.6	21.2	12.8

Table 4.4: Power Amplifier performances comparison.

Chapter 5
Conclusion

This work mainly investigates the single-pole double-throw RF switch with Class-F power amplifier operating in E-band. The fundamental circuit consists of two NW transistors with each transistor connects to a $\lambda/4$ transmission line. Using load pull simulation to search for optimum load impedance for the PA. Finally, this work demonstrates the feasibility of Class-F PA using RF switch a output matching without losing too much performance of the RF switch.

There is a trade-off between insertion loss and isolation when sizing the switch transistor. In order to focus on the behaviors of the PA path, the transistor is chosen in relatively small size, 800 NW. However, this work does not repudiate the possibility of the other transistor sizes, which can be further researched in the future.

The load pull simulation compares PA performances varying the transistor sizes. Although the transistor with larger size may contribute higher performance, it can be problematic when connected to the RF switch. Thus, the 500 NW 10 NF transistor is used for common source PA, with load impedance equaling to $12.9 + 10.0i\ \Omega$.

The combination of RF switch and Class-F PA shows great success in this project. The output matching networks of Class-F PA is successfully achieved by using $\lambda/4$ TL from RF switch, with maximum PAE reaching 52%. The problem caused by asymmetric impedance is solved by doubling the size of switch transistor. The performance of the LNA path is slightly degraded, while the performance of the RF switch is biased towards the PA path, which is in line with the initial design goals.

However, most of the components are set in ideal conditions, which are impossible to realize in practice. The input matching of the PA is designed in single stage, which may cause unstable results or other unnecessary problems. The Class-F PA is designed solely in the out stage, leaving room for multi-stage designs. All these inadequacies in this work can be new topics for future discussion.

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