Design and Modeling of $In_xGa_{(1-x)}As/InP$ based Nanosheet Field Effect Transistors for High Frequency Applications

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Design and Modeling of $In_xGa_{(1-x)}As/InP$ based Nanosheet Field Effect Transistors for High Frequency Applications

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Abstract

The advancement of CMOS technology has been fueled by the need to satisfy Moore's law by shrinking transistors to progressively smaller sizes and increasing the transistor density per unit area [1]. The dimension of the state-of-the-art MOSFET is now down to a few nanometers. However, with continued device scaling, the performance of Integrated Chips (ICs) starts to deteriorate, making it essential to implement novel technology solutions. The novel technologies, such as reshaping the devices' geometries in [2], achieved better excellent electrostatic performance than planar technologies. For example, 3D finFETs or tri-gate architectures showed improved electrostatic control and necessitated further scaling of the transistor length. Nanosheet FETs showed higher drive currents than FinFET technology at a given fin pitch and can further provide gate length scaling [3]. The geometry of the nanosheets allows all-around gate contact offering excellent electrostatic integrity. Power dissipation in CMOS applications is getting worse due to aggressive scaling [4]. One can overcome this by adding material to the channel with higher transport qualities, such as InGaAs [5]. The higher carrier mobility compared to Si enables high current at low operating voltages.

In this thesis, InGaAs nanosheet FETs high-frequency performance is investigated. The wider and thinner nanosheets are considered for analysis and are modeled with quasi 2D ballistic model. The device's extrinsic part, such as extrinsic capacitance, is modeled using electrostatic model in COMSOL. The intrinsic and extrinsic parts are combined, and the high-frequency metrics such as transition frequency, f_T, and the oscillation frequency, f_{max}, are evaluated. The device is optimised in terms of nanosheet width, thickness, separation between two stacks, source/drain spacer distance, the number of stacked channels and the composition of the material are optimized to get the best performance.

Popular Science Study

The continuous improvement of electronic devices is limited by certain challenges. One such challenge is the emergence of short channel effects when scaling down the size of device channels [1]. However, a new type of transistor called FinFET shows promise in overcoming these limitations. FinFETs have a thin body and superior scalability due to gate control on the channel from three sides. They offer better electrostatics, lower power consumption, and higher performance compared to traditional planar bulk metal oxide semiconductor field effect transistors (MOSFETs). In recent studies, researchers have successfully achieved a better performance by integrating a new material layer into the conventional high-k metal gate process [6]. However, FinFETs face challenges in terms of patterning, device performance, layout, and cost for further scaling [1]. As device pitches decrease, thinner and taller fin structures are required, which raises concerns for both performance and manufacturing processes.

To address these challenges, nanowire structures are being considered as a potential solution [7]. Nanowires offer better short-channel control and higher current density, enabling further device scaling. One limitation is their lower drive currents due to the inherently smaller effective channel width. However, this can be compensated by stacking several nanowires vertically. Recently, nanosheet field effect transistors (NSFETs) have been proposed as a continuation of device scaling [8]. In nanosheets, the width of the silicon body is not limited by fin pitch and quantization, allowing for more flexibility in achieving the desired effective channel width. The sheet-to-sheet spacing in nanosheets is determined by epitaxial processes, unlike the lithographically controlled fin pitch in FinFETs [6]. Moreover, multiple sheets can be stacked in the vertical direction to achieve the desired effective width per footprint.

Nanosheet structures has the superior gate control, lower mismatch in subthreshold swing and drain-induced barrier lowering, and better frequency response. They also offer better flexibility to self-heating effects. However, NSFETs may require more complex modeling designs compared to FinFETs.

In conclusion, nanosheet structures show promise for future transistor manufacturing and device optimization. They offer advantages in terms of channel control, scalability, and performance. Further research is needed to determine the optimal parameters and explore potential avenues for improvement.

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Acronyms

ALD Atomic Layer Deposition.

CMP Chemical Mechanical Planarization.

DG Dummy Gate.
DIBL Drain-Induced Barrier Lowering.
DUT Doped Ultra-Thin.

EUV Extreme Ultraviolet.

FEM Finite-Element Modeling.
FGA Forming Gas Annealing.
FinFET Fin Field Effect Transistor.

HKMG High-k Metal Gate.

GAA Gate All Around.
GP Ground Plane.

HARP High Aspect Ratio Process.
HEMT High Electron Mobility Transistor.
HSQ Hydrogen Silsesquioxane.

ILD Iterlayer Dielectric.
IPA Isopropyl Alcohol.

LER Line Edge Roughness.
LPCVD Low Pressure Chemical Vapor Deposition.

MNSFET Multi-Nanosheet Field-Effect Transistor.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

MOVPE Metal-Organic Vapor Phase Epitaxy.

NC PFINFET Negative Capacitance P-Type FinFET.

NSFET Nanosheet FET.

NWFET Nanowire FET.

RF Radio Frequency.

RIE Reactive-Ion Etching.

RMG Replacement Metal Gate.

RO Ring Oscillator.

RPCVD Reduced Pressure Chemical Vapor Deposition.

RTA Rapid Thermal Annealing.

SHE Self-Heating Effect.

SNSFET Si Nanosheet FET.

SS Subthreshold Swing.

STI Shallow Trench Isolation.

TCAD Technology Computer-Aided Design.

TMAH Tetramethylammonium Hydroxide.

PTS Punch-Through Stopper.

Symbols

α Non-parabolic parameter.

C_{gg} Gate capacitance.

C_q Quantum capacitance.

C_{gsp} Gate to source parasitic.

C_{gdp} Gate to drain parasitic.

C_Σ Equivalent capacitance.

E_1 First subband-energy level.

E_g Energy bandgap.

E_n Energy levels.

ε_{ox} Relative permittivity of the gate oxide.

ε_r, k Relative permittivity/dielectric constant.

ε_{tw} Relative permittivity of the channel material.

f_T The maximum cut-Off frequency.

f_{max} The maximum oscillation frequency.

$g_{d,i}$ Intrinsic output conductance.

$g_{m,e}$ Extrinsic transconductance.

$g_{m,i}$ Intrinsic transconductance.

H_{ns} Channel thickness.

I_{OFF} OFF current.

I_{ON} ON current.

k_x, k_y, k_z Wave vector in x, y and z direction.

L_g Gate length.

$m_n^\star$ Effective mass of a sub-band with index n.

ΔN The total electron density at the top of barrier.

$No.$ The number of sub-bands.

U_L Laplace potential at the top of the barrier.

U_P Potential energy due to the mobile charge.

V_T Threshold voltage.

W_{EFF} Effective channel width.

x The percentage of indium composition.

Constants

h **Planck's constant** $6.62607015 \times 10^{-34}$J.S

$\hbar$ **Reduced Planck's constant** $1.05457182 \times 10^{-34}$ m^2 kg/s

q **Electron charge** $1.602176634 \times 10^{-19}$C

k_B **Boltzmann constant** 1.380649×10^{-23}J. K^{-1}

m_0 **Free electron mass** $9.1093837015 \times 10^{-31}$ kg

ε_0 **Vacuum permittivity** 8.854×10^{-12} F/m

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Chapter 1

Introduction

The continuous scaling down of device channel length for improved electrostatics is constrained by the emergence of short channel effects in scaled technology nodes [9]. FinFETs, as thin body transistors, offer superior scalability, enhanced channel electrostatics, improved subthreshold swing (SS), lower power consumption, and higher performance compared to planar bulk metal oxide semiconductor field effect transistors (MOSFETs). Another approach to achieving super-steep SSs is through negative capacitance field-effect transistors, which incorporate a ferroelectric film into the gate stacks [6]. Conversely, full depletion FinFETs with multi-gate control generally exhibit steeper SS characteristics than planar FETs. In [9], super-steep SSs were achieved in negative capacitance P-Type FinFETs (NC p-FinFETs) with various gate lengths by integrating a 3 nm-thick $Hf_{0.5}Zr_{0.5}O_2$ layer into the conventional High-k Metal gate (HKMG) process, thanks to low interface trap density and optimal channel electrostatic integrity. However, further scaling of FinFETs poses challenges in terms of patterning, device performance, layout, and cost. With shrinking pitches, the need for tighter, taller, and thinner fin structures arises, raising concerns for both performance and manufacturing processes [10]. On the other hand, nanowire structures offer better short-channel control and higher current density, enabling further device scaling. While the lower drive currents resulting from inherently smaller effective channel width (W_{EFF}) in nanowires can be compensated by stacking multiple nanowires vertically, this approach is limited by parasitic capacitances similar to the use of taller fins in FinFETs. Recently, nanosheet field effect transistors have emerged as a potential solution for continued scaling.

In nanosheets, the nanosheet width, which refers to the width of the silicon body, is not constrained by fin pitch and fin quantization, providing greater flexibility in achieving sufficient effective width (W_{EFF}). However, the increased cross-sectional area of the nanosheet simultaneously impacts drive current, electrostatics, and parasitic components [10]. Therefore, it is crucial to evaluate different device design options for Nanosheet FETs. The spacing between nanosheets (analogous to fin pitch in FinFETs) is determined by epitaxial processes instead of lithographically controlled fin pitch in FinFETs. Moreover, effective device width per footprint can be achieved in nanosheets by utilizing multiple sheets in the vertical direction, as opposed to FinFETs that utilize multiple fins in the horizontal direction [6]. The impact of line edge roughness (LER) on the electrical characteristics of Nanosheet FETs (NSFETs) and Nanowire FETs (NWFETs) is discussed in [11]. A comparison of the structure and electrical performance of NSFETs, FinFETs, and NWFETs under a 5 nm technology node is presented in [3]. The geometry of these different technologies is depicted in Figure 1.1. The comparison reveals that NSFETs exhibit higher immunity to mismatch in ON current (I_{ON}) compared to NWFETs. Additionally, when compared to other nano-dimensional transistors, NSFETs demonstrate superior control due to their gate-all-around structures, while NWFETs exhibit lower mismatch in subthreshold swing (SS) and drain-induced barrier lowering (DIBL). NWFETs, with their cylindrical structure, offer better gate control over the channel than FinFETs and NSFETs. Furthermore, NSFETs exhibit excellent frequency response (faster) and support the possibility of multi-threshold voltage [7]. They also provide improved flexibility in dealing with self-heating effects (SHE) compared to FinFETs [8]. However, NSFETs require less complex modeling designs compared to FinFETs [4].

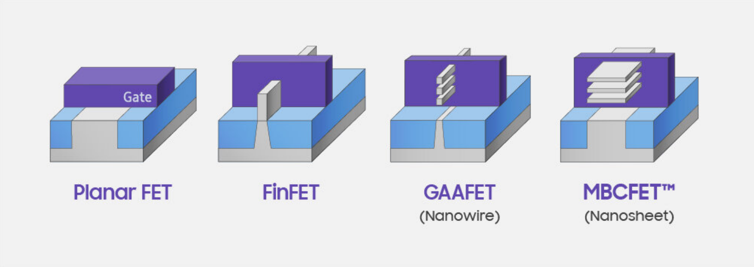


Figure 1.1: Planar FET, FinFET, NWFET and NSFET geometry[12].

The nanosheet structure maximizes the area where the channel interacts with the gate by transforming the wire-shaped channel into a nanosheet. This ensures that the channel width is wide enough to facilitate a significant current flow while maximizing gate control over the channel. However, a drawback arises due to the occurrence of punch-through caused by short channel effects (SCE) in the lower segment of the channel, which is not enclosed by the gate, leading to significant leakage current. To mitigate this issue, the current multi-nanosheet transistor incorporates a punch-through stopper (PTS) doping to limit leakage current, albeit at an increased production cost [13]. In an effort to reduce costs and simplify the process, an insulator is introduced in the lower part of the source and drain regions [13]. The nanosheet structure provides tighter gate control by surrounding the channel from all sides, resulting in lower output conductance (g_{ds}). This also indicates that the drain has comparatively less influence over the channel compared to FinFETs. Consequently, the parasitic capacitance component formed between the gate metal and the source/drain epi region becomes more significant in the multi-fin FinFET structure. A study in [6] demonstrates that the desired effective width (W_{EFF}), dictated by the I_{on} requirement for RF applications, can be achieved through various combinations of stack structures and sheet widths. Additionally, a comprehensive analysis in [14] investigates the comprehensive effects of these parameters on the electrical characteristics of the devices.

This thesis seeks to explore the benefits of the nanosheet structure and investigate its potential for future manufacturing, including mass production. It aims to achieve this by precisely defining the structure, size, and material parameters associated with the nanosheet structure. The following chapters provide a comprehensive overview of the research conducted in this field. Chapter 1 summarizes previous studies on optimizing the structure of Field-Effect Transistors (FETs). By examining the size and material characteristics, this research seeks to define the parameters necessary for efficient production in the future. In Chapter 2, the overall fabrication process is outlined, along with a theoretical model for estimating performance. This chapter serves as a guide to understand the practical implementation of the nanosheet structure. Chapter 3 focuses on performance optimization. It takes into account factors such as gate drive capability and parasitic capacitance to ensure optimal functionality. Additionally, the chapter investigates a high-frequency model using parameters such as f_T and f_{max}, to determine the ideal gate length for Radio Frequency (RF) applications of this structure. The conclusion presented in Chapter 4 provides insights into the size and parameter choices necessary to achieve optimized performance. This includes considering the intrinsic and extrinsic parts of the nanosheet structure, as well as its high-frequency performance. Furthermore, the chapter discusses the future direction for IC chip sizing and potential avenues for further optimization. In summary, this thesis delves into the nanosheet structure, its advantages, and its potential for future manufacturing. By examining various factors and models, it identifies the optimal parameters required for achieving high-performance FETs. The findings presented in this research contribute to the ongoing development and optimization of IC chip technology.

1.0.1 Literature survey

To enable further scaling down to the 5 nm and 3 nm nodes, GAA nanosheet devices have been evaluated as a potential replacement for the FinFET device architecture at the 7 nm ground rule. Previous studies have explored this topic extensively, as summarized below. In [15], researchers investigated different device geometries and nanosheet widths using TCAD simulations, focusing on both DC and AC performance. They compared the ballistic performance of FinFETs and NW-FETs at sub-7 nm node dimensions. The findings from [15] indicate that Nanosheet-FETs exhibit greater robustness in heavily loaded circuits compared to nanowire-FETs, while their performance in lightly loaded ring oscillator (RO) circuits is similar. Additionally, Nanosheet-FETs offer more flexibility in optimizing the nanosheet width for the drive current, without being limited by the fin pitch or fin quantization, particularly when Extreme Ultraviolet (EUV) lithography is utilized. The study presented in [16] employed the MINIMOS NT tool to conduct two-dimensional Schrodinger Poisson simulations, successfully predicting the impact of carrier confinement in silicon nanosheets at 3 nm technology nodes. In order to minimize parasitic capacitance, [14] identified the importance of optimizing the gate height and cap. The study also analyzed the source-drain distance and emphasized that the design of the gate-drain spacing primarily relies on the influence it has on the breakdown voltage.

In [6], researchers conducted a comprehensive study on the effects of stack spacing and the number of stacks on device performance. They proposed a substack design to enhance RF performance. Furthermore, [6] demonstrated that nanosheets exhibit a lower degradation rate in subthreshold swing (SS) due to their superior gate control. Compared to FinFETs, nanosheets demonstrate superior electrostatic control over the channel, resulting in higher I_{ON}/I_{OFF} ratios and reduced drain-induced barrier lowering (DIBL) at scaled lengths. To ensure accurate analysis of the channel region and drift-diffusion simulation for MNS-FET devices, researchers in [13] performed calibration using Monte Carlo simulation. Regarding nanowires (NWs), [17] highlighted that horizontal NWs are a natural extension of RMG FinFETs, while vertical NWs necessitate more disruptive technology changes. The study focused on fabricating GAA Si NWFETs on bulk Si substrates using an adapted replacement metal gate (RMG) FinFET flow, addressing integration challenges specific to bulk substrates such as low-temperature STI processing and parasitic channel suppression. The self-heating characteristics of horizontally stacked three-layer GAA nanosheet transistors were investigated in [18] using 3-D FEM simulation. The study provided valuable insights into layout design, thermal management, device performance, and thermal-aware reliability prediction for the GAA-stacked structure. In [4], the benefits of scaling using double and single-stack nanosheet structures were illustrated. By relaxing the pitch, it becomes possible to match the effective width (W_{EFF}) of aggressively scaled FinFETs. Moreover, when wide nanosheets are used, there can be a significant 30% increase in W_{EFF}. The maximum gain in W_{EFF} is achieved by employing a single wide nanosheet stack, as this structure spans the entire active footprint, assuming successful fabrication of wide sheets.

While many studies have focused on the design aspects of NSFETs for logic applications, exploring their high-frequency performance is also of great interest. Key metrics for high-frequency operation include the maximum cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) [19]. These metrics are influenced by various device electrical parameters, such as transconductance (g_m), contact resistances (R_S, R_D, R_G), g_{ds}, and the gate capacitance (C_{gg}), which encompasses both intrinsic and parasitic components. As technology nodes shrink, the impact of parasitic components becomes more significant and can lead to performance degradation and increased delay times in devices and circuits. Earlier research often focused on optimizing specific factors, resulting in trade-offs between different criteria. Interestingly, the relationship between gate length reduction and the maximum oscillation frequency is non-monotonic. While f_T typically increases as the gate length decreases, f_{max} starts to decrease after a certain gate length reduction. This is due to the reduction in the gate cross-sectional area, which increases gate resistance. To address this issue, [16] proposed a solution for simultaneously improving both f_T and f_{max} by introducing a gate cap on the gate top while keeping the gate length unchanged. This approach effectively mitigates the increase in gate resistance caused by gate length reduction. However, the introduction of the gate cap also leads to an increase in gate parasitic capacitance, which subsequently impacts the degradation of f_T.

Gate capacitance is a critical parameter that significantly impacts the high-frequency performance of MOSFET devices. It consists of two types: intrinsic gate capacitance and parasitic gate capacitance. Among the two, the parasitic gate capacitance is typically larger and dominates the total gate capacitance of the MOSFET [20]. The parasitic gate capacitance can be divided into different components. Fringe capacitance components include the capacitance between the gate and the source/drain extension region or spacer region, both from the sides and the top. Additionally, there is capacitance between the gate and the source/drain epi region, again from the top and the sides. Parallel plate capacitance components include the capacitance between the gate and the side of the source/drain epi region, which encompasses all sides of the sheet and specifically between the gate metal of the bottom sheet and the side of the source/drain epi. Furthermore, there is capacitance between the base metal and the substrate. Multi-stack structures, similar to the multi-fin FinFET structure [3], also exhibit stack-to-sheet coupling capacitance, although it's not depicted here. To enhance the MOSFET device's performance, minimizing the parasitic gate capacitance is crucial. This can be achieved through several approaches, including optimizing the device layout, reducing device dimensions, and employing advanced fabrication techniques to mitigate the effects of parasitic capacitances.

In the current phase of MOSFET scaling, known as "power-constrained scaling," the dissipated power density in logic chips has reached approximately 100 Wcm^{-2}. Further increases in power density would lead to excessive packaging and cooling costs, rendering these chips impractical for most applications. To maintain advancements in transistor density, reducing the operating voltage is necessary. However, this approach results in slower switching speeds. As a result, the operating voltage for CMOS transistors has remained around 1 V for some time. To enable future scaling, additional breakthroughs are required. To address this challenge, researchers are focusing on a promising group of materials: group III–V compound semiconductors [21]. These materials, with their exceptional electron transport properties, hold great potential for developing nanometer-scale logic transistors. The semiconductor materials based on GaN exhibit superior properties such as high mobility, high electron saturation velocity, and high critical breakdown field strength. Group III and V elements from the periodic table are combined to create III-V compound semiconductors, including alloys like GaAs, AlAs, InAs, and InP. Certain III-V compounds possess unique optical and electrical characteristics, making them ideal for applications in lasers, light-emitting diodes, and optical communication devices. Among these compounds, GaAs, InGaAs, and InAs stand out due to their exceptional electron transport characteristics. Transistors made from these materials are widely used in high-speed and high-frequency electronic systems. Indium-rich InGaAs, for instance, exhibits electron mobility more than ten times higher than silicon at similar sheet density [22]. III-V transistors are also recognized for their excellent frequency responsiveness. In logic transistors, high-speed switching is achieved by having a high current in the "on" state (I_{ON}), while minimizing the off current (I_{OFF}) is crucial to reduce standby power consumption.

Criticism has been raised regarding the limitations imposed on the highest achievable sheet electron concentration due to a low effective mass. Recent research has indicated that High Electron Mobility Transistors (HEMTs) fabricated from InGaAs and InAs exhibit significantly higher electron effective mass than their bulk counterparts. This can be attributed to the pronounced non-parabolicity of the conduction bands in these materials, the quantization of electrons in the small channel, and the biaxial compressive stress resulting from lattice mismatch with the InP substrate. The unique quantum structure of the channel in InAs and InGaAs HEMTs effectively confines electrons and leads to a steep subthreshold behavior, distinguishing them from silicon MOSFETs of comparable nature. However, it is important to note that narrowing the channel to improve mobility encounters limitations due to the worsening dispersion and deteriorating transit. Experimental studies on mobility reveal that the electron mobility in an InAs HEMT decreases from 13,000 $cm^2v^{-1}s^{-1}$ to 10,000 $cm^2v^{-1}s^{-1}$ when the channel thickness is reduced from 10 nm to 5 nm [23]. On the other hand, the impact is far less significant for short-gate-length transistors, as demonstrated in [5]. This can be attributed to the expectation of ballistic transport when the gate length of the transistor is sufficiently short. Therefore, it is feasible to scale down a thin quantum-well design to extremely small dimensions.

III-V HEMTs have strengthened the case for III-V CMOS technology, although they are not suitable for standalone logic applications due to their high gate leakage current [23]. Nonetheless, HEMTs offer valuable design features for future III-V MOSFETs, including a junctionless design with an InAs-rich quantum well that is thin, undoped, and extends beneath the device's extrinsic region, covered by elevated source and drain regions. Popular ALD high-k dielectrics such as Al_2O_3 and HfO_2 are utilized in III-V MOS structures [24]. Channel mobility is a crucial consideration in high-k III-V MOS structures, with a surface-channel device featuring the oxide directly on top of the channel being optimal for scaling. However, this configuration suffers from reduced mobility caused by interface roughness, coulomb scattering from interface states, remote phonon scattering from the high-k oxide, and other factors. To address this issue, a buried-channel device can be employed, where the channel and oxide are separated by a thin wide-bandgap semiconductor. This approach mitigates the impact of interface roughness, remote phonon scattering, and coulomb scattering from charged interface and bulk oxide states, resulting in enhanced mobility. It is important to note that the oxide/semiconductor composite barrier structure must be extremely thin to control short-channel effects, which limits the effectiveness of this technique. Nonetheless, this approach leads to improved mobility as a desirable outcome.

The most advanced III-V MOSFETs reported so far have employed ALD TiSiO as the dielectric and InGaAs buried-channel architectures with an InP barrier layer, as mentioned in [25]. Remarkably, a 75 nm gate-length device achieved an exceptional combination of current drive and subthreshold properties, surpassing the performance of contemporary silicon MOSFETs. In CMOS technology, minimizing parasitic capacitance and resistance between different areas of the structure poses a significant challenge. It is unlikely that scaled III-V and silicon MOSFETs would exhibit distinct parasitic capacitances. While group III-V compounds, such as InP HEMTs and III-V quantum well MOSFETs, offer high electron mobility and fast switching speeds, their slightly higher permittivity compared to silicon (approximately 10% higher for GaAs) plays a minor role as devices continue to shrink in size. Instead, the influence of parasitic fringe capacitance associated with the gate sidewalls becomes increasingly significant. Nanowire MOSFETs also provide high switching speeds and low power consumption, further expanding the available options for high-frequency applications.

This thesis explores several techniques and options to achieve high on-current and low gate capacitance in a nanosheet transistor, with a specific focus on assessing its suitability for RF applications. The device structure parameters, including the gate structure, sheet structure, high-k dielectric, and spacer thickness, are studied using the FEM software COMSOL. The investigation begins by reducing the gate length to enhance the device's small-signal performance. Subsequently, the influence of the sheet structure is examined, determining the optimal sheet width, thickness, and separation. The dimensions of the access region, including the analysis of spacer thickness and source-drain distance, are also investigated. Through this research, a quantitative understanding of the factors impacting the device characteristics is revealed from the perspective of device structure design.

Chapter 2

Theoretical model description

In this chapter, we discuss the complete device modeling. The schematic of the device design used in this work with highlighted intrinsic and extrinsic parts is shown in figure 2.1. The intrinsic device is the central active part of the device where the gate controls the carrier flow in the channel and can be modeled using the top of the barrier model to estimate the current and transconductance values. In comparison, the extrinsic part of the device is nothing but the extra part, which adds additional resistance and capacitance to the device. As discussed before, as the device dimensions become smaller, the extrinsic capacitance and resistances become dominant even in HEMTs and FinFET technologies [26].

2.1 Fabrication flow of NSFET

2.1.1 Fabrication

The fabrication process of the $In_xGa_{(1-x)}As/InP$ nanosheet FET follows the conventional integration flow used for FinFETs, as described in [4]. Several specific elements differentiate it from FinFETs, including multilayer channel epitaxy for stacked sheets, inner spacer formation, channel release, and replacement metal gate integration. The release of stacked nanosheet channels occurs after removing the dummy gate in the standard replacement gate integration process. Fabrication of NS FETs presents various challenges related to yield. Optimizing the contact depth and inner spacer thickness is crucial for the source/drain modules. Unlike bulk FinFETs, NS FETs have a parasitic channel beneath the first-floor nanosheet, resulting in increased parasitic effects despite having multiple channels surrounded by metal gates (GAA). To mitigate this, the application of a ground plane region has been suggested to effectively attenuate the parasitic channel effect [27]. However, the fabrication process for NS FETs is highly sensitive, and steps such as ion implantation and rapid thermal annealing for ground plane region formation can lead to undesirable non-uniform doping profiles. The shortcomings of FinFETs and gate-all-around nanowire transistors have led to the development of nanosheet transistors. Traditional methods used for suppressing parasitic sub-fin channels, such as halo implantation for planar devices and punch-through stop doping for bulk FinFETs, are not suitable for GAA NS devices. New strategies are required to reduce parasitic sub-fin channel leakage and enhance device subthreshold char-

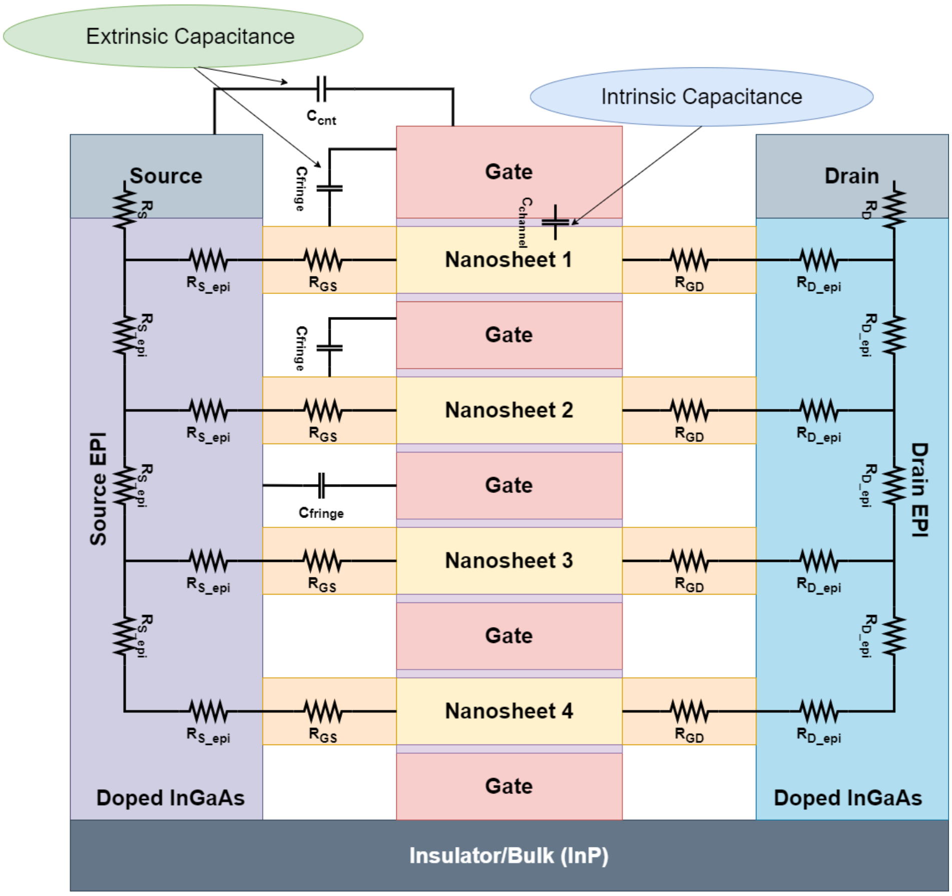

Extrinsic Capacitance
Intrinsic Capacitance
Ccnt
Cfringe
Cchannel
Source
Drain
Gate
Nanosheet 1
Nanosheet 2
Nanosheet 3
Nanosheet 4
RS
RD
RS_epi
RGS
RGD
RD_epi
Source EPI
Drain EPI
Doped InGaAs
Doped InGaAs
Insulator/Bulk (InP)

Figure 2.1: Nanosheet FET with four sheets stacked vertically. Intrinsic and extrinsic parts are highlighted separately.

acteristics. Optimal GAA Si NS channels and device structures were achieved by optimizing the NS release mechanism in stacked GAA Si NS devices, as discussed in [8]. The impact of ground implantation (GP) doping on device electrical characteristics was extensively explored in [28] through experiments and TCAD simulations. In summary, the fabrication of nanosheet transistors involves four main steps: epitaxial growth of multilayers, inner spacer integration, nanosheet channel release, and replacement metal gate integration. The process of manufacturing a transistor from a simple substrate is time-consuming and involves multiple processing steps. This chapter provides a detailed description of the geometry and fabrication of InxGa(1-x)As-based nanosheet field-effect transistors (NSFETs) proposed in this diploma work. Refer to Figure 2.2 for the corresponding device fabrication process.

2.1.2 Key fabrication steps

Because the structure has not been fabricated, the process flow here is just a theoretical approach. The general process described below includes some recurrent steps, which will be mentioned with less detail after their initial description.

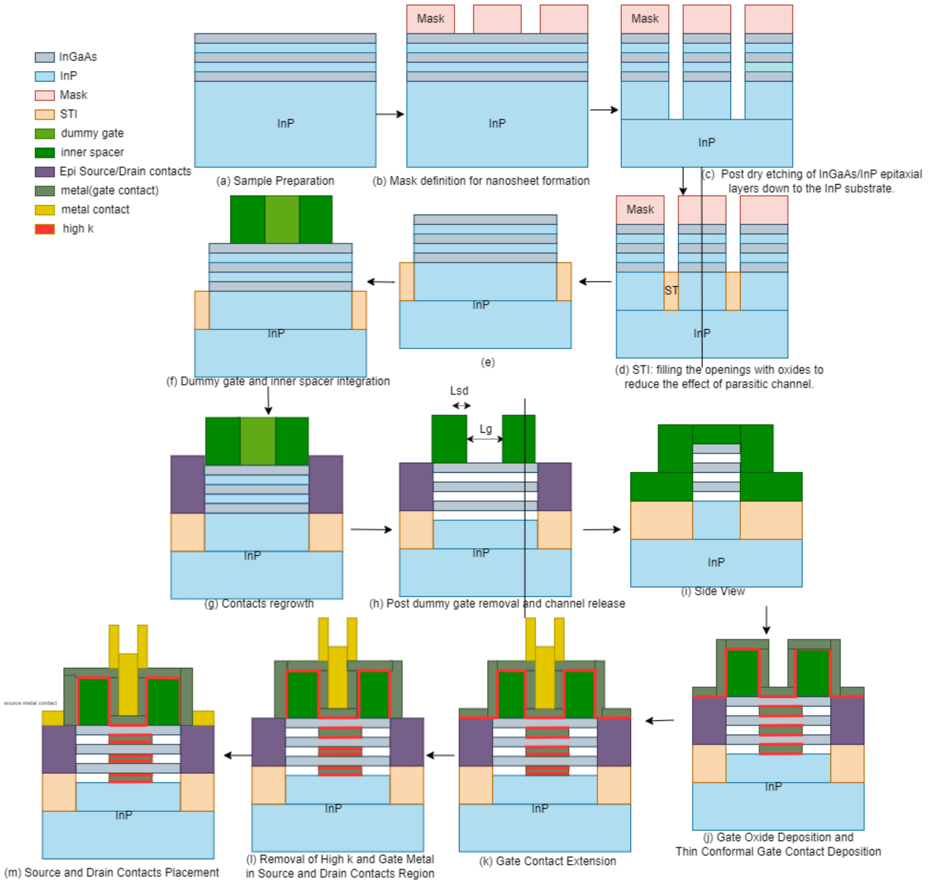

InGaAs
InP
Mask
STI
dummy gate
inner spacer
Epi Source/Drain contacts
metal(gate contact)
metal contact
high k
InP
(a) Sample Preparation
Mask
InP
(b) Mask definition for nanosheet formation
Mask
InP
(c) Post dry etching of InGaAs/InP epitaxial layers down to the InP substrate.
Mask
ST
InP
(d) STI: filling the openings with oxides to reduce the effect of parasitic channel.
InP
(e)
InP
(f) Dummy gate and inner spacer integration
InP
(g) Contacts regrowth
Lsd
Lg
InP
(h) Post dummy gate removal and channel release
InP
(i) Side View
InP
(j) Gate Oxide Deposition and Thin Conformal Gate Contact Deposition
InP
(k) Gate Contact Extension
InP
(l) Removal of High k and Gate Metal in Source and Drain Contacts Region
source metal contact
InP
(m) Source and Drain Contacts Placement

Figure 2.2: Proposed NSFET process flow

Stacked Fin arrays definition

The vertical nanosheets, which make up the MOSFET channel, are the first structures to be processed. The device channel is defined by the epitaxial growth of multilayers of InP and $In_xGa_{(1-x)}As$ during the manufacturing of nanosheet transistors, as shown in (a) in figure 2.2. The final spacing of stacked GAA $In_xGa_{(1-x)}As$ NS channel MOSFETs is determined by the thickness of the InP layer in $In_xGa_{(1-x)}As/InP$ stacks, and this impacts the channel morphology and filling properties of High-K and metal contacts. Nanosheet transistor fabrication differs from CMOS devices because it grows channels on a different lattice than materials that are epitaxially grown. Electron beam lithography technique is used to define the a single nanosheet stack width, length, and separation between two stacks as shown in figure 2.2(b). The layers are etched down to substrate by dry etching in the mask openings as shown in figure 2.2(c). To reduce oxidation-induced fin deformation and boost the drive current and speed gain capabilities of nanosheet transistors, some people have suggested adopting shallow trench isolation, as show in figure 2.2(d). After low-temperature shallow trench isolation annealing, the surface was then flattened with chemical mechanical planarization. Wet oxidation will be used to create this structure, which is known as filed oxide. The hard mask is removed revealing nanosheet stack arrays in figure 2.2(e).

Dummy gate formation and Inner spacer integration

Following the nanosheet channel process, the heavily doped drain and source contacts are incorporated. To prevent the contact layer from extending over the nanosheets, a hydrogen silsesquioxane strip, known as a dummy gate, is applied to cover the nanosheet array and define the MOSFET's gate length (Figure 2.2(f)). Constructing a nanosheet transistor requires the inclusion of an inner spacer, which acts as a dielectric barrier between the gate and the source/drain regions. This deposition must be conformal, covering all three sides of the nanosheets to safeguard these areas during the subsequent step of highly doped contact growth.

Epi-contacts growth

In Si process, highly doped contacts are formed by ion-implantation which is high energy and high temperature process and is not recommended for narrow bandgap semiconductors such as InGaAs. Instead, highly doped contacts can be be regrown using epitaxial method, such as Metal organic chemical vapor depositions (MOCVD). The schematic of the contacts profile is shown in figure 2.2(g).

Nanosheet channel formation/release

The nanosheets within the channel are separated by an InP barrier layer, which is selectively etched to create freestanding nanosheets. This step, depicted in Figure 2.2(h), is referred to as channel release. Figure 2.2(i) provides a side view of the released channel. In the case of multi-layer $In_XGa_{(1-X)}As/InP$ stacks, high-temperature processes can lead to rapid atom diffusion and the degradation of the interfaces between the layers. These effects can have an impact on the structure, morphology, and quality of the resulting nanosheets.

Gate oxide and contact deposition

The gate oxide deposition is a crucial step in transistor fabrication as it serves to separate the gate from the channel and prevent leakage. To enhance device performance, high-k materials are commonly employed as gate oxides. Figure 2.2(j) illustrates the deposition of this oxide using atomic layer deposition, which utilizes precursor gases at elevated temperatures. Prior to oxide deposition, it is necessary to remove the native oxide and passivate the samples. Passivation is a chemical process that renders the surface unreactive to air. During the gate contact formation, a metal is deposited around and between the nanosheet layers. This step is of utmost importance as the work function difference between the metal and the high-k dielectric material can impact the threshold voltage. High-k dielectrics possess a higher permittivity, leading to an increased gate capacitance even with a thick gate oxide. However, this high permittivity also reduces the required gate voltage for a given electric field strength, resulting in a lower threshold voltage. Therefore, careful selection of a metal with an appropriate work function is crucial to achieve optimal device performance in nanosheet FETs.

Gate formation

Figure 2.2(k) depicts the gate contact positioned above the gate oxide. In order to minimize gate resistance, a T-gate structure is employed, indicated by the yellow part. The advanced replace metal gate module encompasses the intricate process steps involved in forming a high-k/metal gate (HK/MG) by replacing the original dual gate (DG). Chemical mechanical planarization is utilized for global planarization, effectively separating the gate. The integration of the replacement metal gate is a crucial step that contributes to the speed enhancement of nanosheet transistors while maintaining a consistent power level.

2.2 Intrinsic device model

Scaling down includes decreasing channel length and reducing the dimension of cross section, the gate becomes more difficult to control the electrons in channel. The device can be conductive between source and drain without gate control. Consider any device from FinFET, NWFET or NSFET can be simplified as figure 2.3 shown, we will use top of the barrier model to calculate current-voltage characteristics of our FET. We will use MATLAB to solve these equations. The left contact can be considered as source and the right contact can be drain. The part in the middle called "channel", which characteristics are modeled with respect to three terminals, and we also consider source and drain that they are in thermal equilibrium. We consider wide nanosheets where, the width is approximately at least 10 times larger than the thickness in this work, and thus electric filed from the sides is negligible compared to vertical field and wider NSFET is considered as 2D FET.

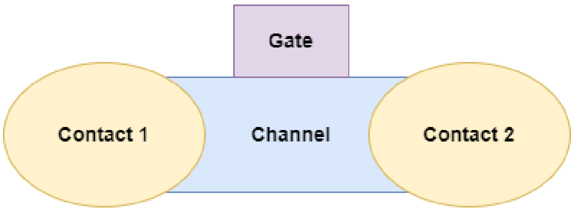


Figure 2.3: The simplified model of FET.

2.2.1 Schrödinger equation and E-K relation

For electronic parameters, the electron wave function in a semiconductor is obtained by solving stationary Schrödinger equation, as below

$$-\frac{\hbar^2}{2m^\star}\nabla^2\psi(\mathbf{r}) + U(\mathbf{r})\psi(\mathbf{r}) = E\psi(\mathbf{r}) \tag{2.1}$$

where $m^\star$ is mass effect of electron. E is the total energy of electron, $U(\mathbf{r})$ is the Lattice periodic potential, and $\psi(\mathbf{r})$ is the Bloch wave function. The electron energy in bulk is given by

$$E = E_c + \frac{\hbar^2}{2m^\star}\left(k_x^2 + k_y^2 + k_z^2\right) \tag{2.2}$$

where E_c is the conduction band energy and second term represents the kinetic energy. At higher wave number, the band become non-parabolic and the E-K relation is given below [29]-[31]

$$E(1+\alpha E) = \frac{\hbar^2}{2m^\star}\left(k_x^2 + k_y^2 + k_z^2\right) \tag{2.3}$$

where α is a non-parabolic parameter of the bands which is given by [32]

$$\alpha \approx \frac{1}{E_g}\left(1 - \frac{m^\star}{m_0}\right)^2 \tag{2.4}$$

where the E_g is direct bandgap. The m_0 is free electron mass. In 1-D confined structures such as here wider nanosheets with thickness of H and widths at least 10 times of the thickness, the electrons are confined in the thickness direction and can move freely in the remaining directions. The nanosheet orientation considered in this work is illustrated in the Figure 2.4. Here we can use quasi 2-D ballistic modeling to calculate currents. For a nanosheet device, by following [33], we defined that (here it is confined in z direction so only k_z is quantized), $k_z = n{\cdot}\pi/H_{ns}$, where n is the energy sub-band index and H_{ns} is the nanosheet thickness.

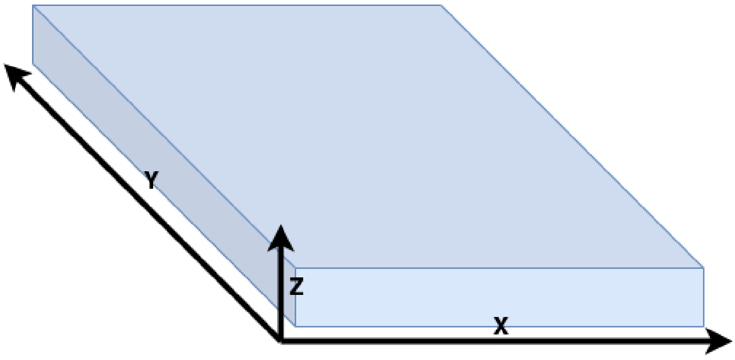


Figure 2.4: The nanosheet length is along y direction, width is in x direction and thickness is in z direction. As the nanosheet is considered quasi 2-D, electrons are confined only in z direction.

We used 8 band Kronig-Penney ($k \cdot p$) theory to solve for electronic parameters for quantum wells. The electronic parameters used such as energy levels, effective mass and non-parabolic of the nanosheets for various composition and thickness are calculated in the simulation.

2.2.2 The density of states and Fermi function

To get estimate of carrier concentration, we need to know the available states per energy, i.e, density of states and the probability with that these states are occupied at a given temperature set by Fermi-Dirac distribution.

According to [34], the expression density of states in quasi 2-D has been shown as

$$D_{2D}(E, E_n) = \sum_{E_n} \frac{m_n^\star}{\pi \hbar^2}(1 + 2\alpha_n(E - E_n)) \cdot u(E - E_n) \tag{2.5}$$

where E_n is sub-band energy level, $m_n^\star$ is the corresponding sub-band effective mass, α_n is the non-parabolic factor of the sub-band. For both two functions, $u(E - E_n)$ is a unit step function which has been listed as below

$$u(E - E_n) = \begin{cases} 1 & \text{if } E > E_n \\ 0 & \text{if } E < E_n \end{cases} \tag{2.6}$$

The probability of a state occupancy is explained by Fermi-Dirac distribution which is a function of electron energy, Fermi - energy level (E_f) and temperature. For a system, the equilibrium of Fermi-Dirac Distribution is given by a function as [34]

$$f_0(E, E_f) = \frac{1}{1 + e^{(E - E_f)/k_B T_L}} \tag{2.7}$$

where k_B is Boltzmann constant, and T_L is absolute temperature.

2.2.3 The capacitance

The capacitance involved in the gate stack are the gate oxide capacitance (C_{ox}) and charge centroid capacitance (C_c) and quantum capacitance (C_q). The wider nanosheet GAA device can be approximated by double gate MOSFET.

The oxide capacitance is parallel plate capacitance between the gate contact and channel with gate oxide as dielectric and is given by

$$C_{ox} = \frac{2 \cdot \varepsilon_{ox} \cdot \varepsilon_0}{t_{ox}} \tag{2.8}$$

where ε_{ox} is the relative permittivity of gate oxide. ε_0 is vacuum permittivity which is equal to 8.85×10^{-12} F/m. The t_{ox} is oxide layer thickness.

The C_c has the relation to the channel thickness and material permittivity. The carriers in the quantum well leads to band bending in the channel and this leads to charge centroid capacitance. The C_c is calculated from the energy shift in first energy level using the first order perturbation theory in a low carrier density limit which is given by:

$$C_c = \frac{\varepsilon_{tw} \cdot \varepsilon_0}{0.18 H_{ns}} \tag{2.9}$$

where ε_{tw} is the relative permittivity of channel material, and H_{ns} is the nanosheet channel thicknesses.

In this model, ε_{ox} is a constant value, $\varepsilon_{ox} = 18$. The oxide thickness, t_{ox} is fixed to 5 nm, and channel thickness, H_{ns} is varied from 3 nm to 10 nm. The ε_{tw} depends on the indium composition which fulfill

$$\varepsilon_{tw} = 13.10 + 1.10x \tag{2.10}$$

where x is the indium composition constant in the nanosheet. We will also investigate the device performance when changing the indium composition in follow-up research. The quantum capacitance is given by

$$C_q = \frac{q^2 \cdot m^\star}{\pi \cdot \hbar^2} \tag{2.11}$$

The C_Σ is defined as the equivalent capacitance which is series combination of these two capacitors. And $C_{\Sigma,norm}$ is the normalized value.
Unnormalized equation

$$C_\Sigma = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_c}} \tag{2.12}$$

Normalized equation

$$C_{\Sigma,norm} = \frac{C_\Sigma}{\alpha_G} \tag{2.13}$$

where α_G is coupling factor for gate.

2.2.4 The quasi 2-D ballistic current

To construct the semiconductor model, the potential energy at the top of barrier should be resulted which is the sum of U_L and U_P[35]. U_L is the Laplace potential at the top of the barrier due to terminal biases which is given by

$$U_L = -q\left(\alpha_G(V_G - V_T) + \alpha_D V_D + \alpha_S V_S\right) \tag{2.14}$$

where α_G, α_D and α_S are three parameters which control the Laplace solution. Their functions are given by

$$\alpha_G = \frac{C_G}{C_\Sigma} \quad \alpha_D = \frac{C_D}{C_\Sigma} \quad \alpha_S = \frac{C_S}{C_\Sigma} \tag{2.15}$$

In a perfect electrostatic situation, $\alpha_G = 1$, $\alpha_D = 0$ and $\alpha_S = 0$.

U_P is the potential energy due to the presence of mobile charge which is given by

$$U_P = \frac{q^2}{C_\Sigma} \Delta N \tag{2.16}$$

where ΔN is the total electron density at the top of barrier when there is a bias within the device.

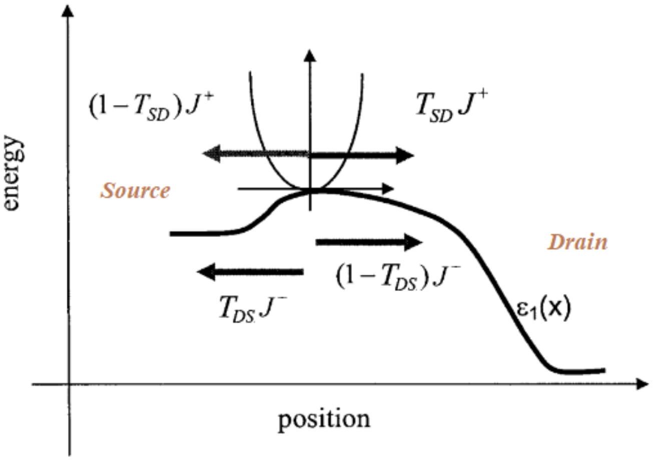


Figure 2.5: Channel potential energy profile at the top of the barrier in scattering situation[34], where T_{SD} is the transmission coefficient from source to drain. The T_{DS} is the transmission coefficient from drain to source. ($T_{SD} = T_{DS}$)

Figure 2.5 shows the energy level from source to drain in the scattering situation. The energy U_{scf} is the point at the top of the conduction band profile. Where the function of U_{scf} is given by
Ballistic limit

$$\begin{aligned} U_{scf} &= U_L + U_P \\ &= -q\left(\alpha_G(V_G - V_T) + \alpha_S V_S + \alpha_D V_D\right) + q^2 \frac{n_0\left(E_{fs}\right) + n_0\left(E_{fd}\right)}{2C_{\Sigma_{Norm}}} \end{aligned} \tag{2.17}$$

Quasi ballistic limit

$$U_{scf} = -q(\alpha_G(V_G - V_T) + \alpha_D V_D) + q^2 \frac{(2-T)\cdot n_0\left(E_{fs}\right) + T\cdot n_0\left(E_{fd}\right)}{2C_{\Sigma_{Norm}}} \tag{2.18}$$

where T is the transmission coefficient. For a perfect electrostatics model, $\alpha_G = 1$, $\alpha_D = 0$ and $\alpha_S = 0$. Due to the short channel effect, for a non-ideal electrostatics model, $\alpha_G < 1$ and α_D becomes a non-zero parameter. α_S will not be considered in this case. E_{fs} and E_{fd} are their corresponding Fermi levels from source and drain, which satisfy the function is given by

$$E_{fd} = E_{fs} - qV_{DS} \tag{2.19}$$

The carrier density on the source side is given by $n_0(E_{fs})$ [35]

$$n_0(E_{fs}) = \sum_n \int_{E_n}^{\infty} D_{2D}(E, E_n) f\left(E, E_{fs}\right) dE \tag{2.20}$$

By following [36], the generalized expression for current in quasi ballistic limit is

$$I = \frac{2q}{h} \int T \cdot M(E) \cdot (f_s - f_d)\, dE \tag{2.21}$$

where T is the transmission coefficient which defines the probability of carrier transmission from source to drain. Following [36], the function of T is given by

$$T = \frac{\lambda}{\lambda + L_g} \tag{2.22}$$

where λ is the mean free path and L_g is gate length. Mean free path is defined as the average distance an electron may travel between successive collisions. This function will be used in calculation with current I_D.

$$\begin{cases} \text{Diffusive:} & L \gg \lambda & T = \frac{\lambda}{L_g} \ll 1 \\ \text{Ballistic:} & L_g \ll \lambda & T = 1 \\ \text{Quasi-ballistic:} & L_g \approx \lambda & T < 1 \end{cases} \tag{2.23}$$

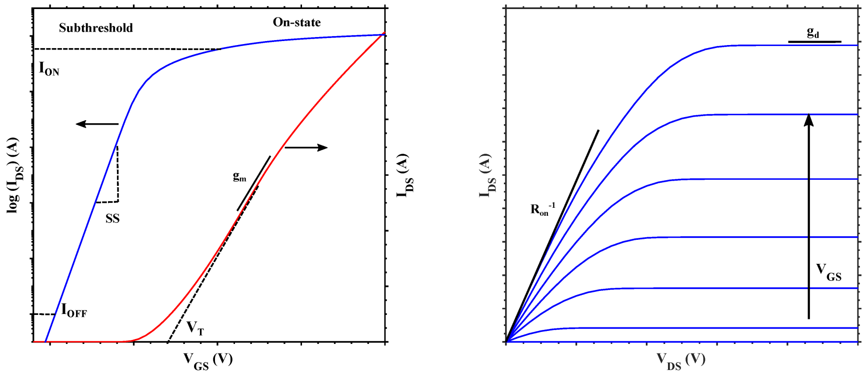
The $M(E)$ is the integer number of effective parallel channels available for conductivity at energy E. For our project, the 2-D number of modes, $M(E)$ is given by equation 2.24.

The f_s and f_d indexed with s and d are Fermi level from two contacts, source and drain, which are calculated by Fermi function mentioned by previous equation 2.7.

$$M(E, E_c) = \frac{\sqrt{2m_n^\star (E - E_c) \cdot (1 + \alpha_n (E - E_c))}}{\pi \hbar} \cdot u(E - E_c) \tag{2.24}$$

where E_c is the conduction band energy. And $u(E - E_c)$ is a unit step function. Therefore, the current I_{DS} in this project can be calculated as below

$$I_{DS} = \sum_{E_n} \frac{2q}{h} \int_{E_n} \frac{\lambda}{\lambda + L_g} M(E, E_c) \left(f_0(E, E_{fs}) - f_0(E, E_{fd}) \right) dE \tag{2.25}$$



(a) (b)

Figure 2.6: (a) Transfer characteristics, drain current dependence on V_{GS} and at a constant V_{DS}. (b) Output characteristics, drain current dependence on V_{DS} for different V_{GS}.

Typical transfer and output characteristics are shown in figure 2.6(a) and 2.6(b), respectively. The DC performance metrics such as sub threshold swing (SS), transconductance (g_m), on and off current(I_{on}, I_{off}), ON resistance(R_{on}), output conductance (g_d) are illustrated.

2.2.5 DC performance evaluation

Transconductance

For the evaluation part, transconductance g_m is one of the most important criteria. The function of $g_{m,i}$ for intrinsic part is given by

$$g_{m,i} = \left.\frac{dI_{\mathrm{DS}}}{dV_{\mathrm{GS}}}\right|_{V_{DS}} \tag{2.26}$$

which shows the ratio between the change in current at the output and the change in input voltage between gate and source. The extrinsic transconductance is calculated by inclusion of extrinsic source and drain resistances.

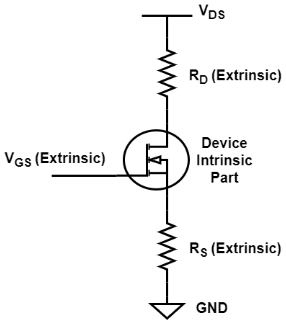


Figure 2.7: MOSFET with extrinsic resistances, R_S and R_D.

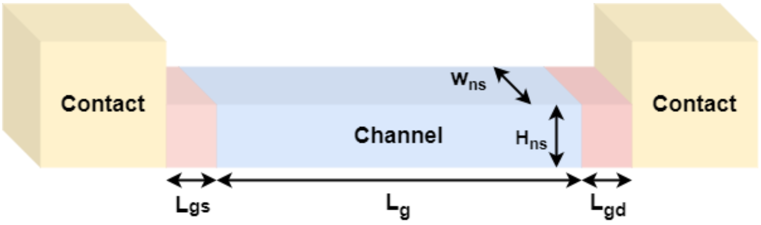


Figure 2.8: Nanosheet channel schematic with dimensions.

The analysis could be divided into two parts, intrinsic and extrinsic. For intrinsic, the conductance could be calculated by differential equation which has given by function 2.26. As shown in figure 2.7, to calculate the extrinsic transconductance, the resistance R_D from drain and R_S from source should be considered.

The dimension of a channel has been shown in figure 2.8. Due to the nanosheet structure, the sheet resistance could be calculated by

$$\varrho = \frac{1}{q \cdot n_{3D} \cdot \mu} \tag{2.27}$$

$$R_{sheet} = \frac{\varrho}{H_{ns}} \tag{2.28}$$

where q is electron charge. The n_{3D} is the equilibrium electron density for quasi 2-D structure. The μ is electron mobility. Where H_{ns} is the nanosheet channel thickness. Thus, the resistors R_D and R_S could be calculated by

$$R_D = R_{sheet} \cdot \frac{L_{gd}}{W_{ns}} \tag{2.29}$$

$$R_S = R_{sheet} \cdot \frac{L_{gs}}{W_{ns}} \tag{2.30}$$

where L_{gd} and L_{gs} are separation between gate to drain and gate to source, respectively. And W_{ns} is the width of channel. The NSFETs proposed in this work are symmetric, hence $L_{gs} = L_{gd}$. The extrinsic conductance is given by

$$g_{m,e} = \frac{g_{m,i}}{1 + g_{m,i}R_S + g_{d,i}(R_S + R_D)} \tag{2.31}$$

where $g_{d,i}$ is the conductance related with I_{DS} and V_{DS} which is given by

$$g_{d,i} = \left. \frac{dI_{\mathrm{DS}}}{dV_{\mathrm{DS}}} \right|_{V_{GS}} \tag{2.32}$$

We calcualted the extrinsic transcondutance assuming negligible $g_{d,i}$.

ON resistance

The resistance value between drain and source of a device when it conducts which called ON resistance, R_{on}. It is in general, taken in the linear operating region of MOSFET. The equation is given by

$$R_{on} = \left. \frac{dV_{\mathrm{DS}}}{dI_{\mathrm{DS}}} \right|_{V_{GS}} \tag{2.33}$$

Sub-threshold swing

The sub-threshold swing is an important feature of the rate at which a transistor switching between on and off states. It represents the amount of change in gate voltage required to change the source-drain current by ten times. The function of sub-threshold swing is given by

$$SS = \frac{dV_g}{d\log I_{ds}} \tag{2.34}$$

A lower value of sub-threshold swing means a faster switching states between ON and OFF. The theoretical limit of SS is $60mV/dec$ at room temperature set by boltzmann statics, and which can increase due to short channel effects.

2.3 Extrinsic device model

The COMSOL Multiphysics is used to model extrinsic capacitances of NSFETs and estimate the optimum device dimensions to achieve the lowest parasitic capacitances. All simulations were performed using the Electrostatic model in AC/DC module, and electrostatic potential distributions and capacitances were calculated numerically. The numerical simulations of the capacitances are obtained without considering the effect of frequency on the calculated capacitances. The AC/DC module uses FEM (finite element method) and BEM (boundary element method) to solve Maxwell's equations. FEM is a numerical method of solving significant mathematical problems and is often used in engineering. To answer the equations for each smaller component of the issue, the problem is divided into discrete elements. A rough solution to the full problem is then made up of these sub-solutions.

In multi-nanosheet transistors, nanosheet are stacked vertically, and the gate surrounds the channel in all directions. The channel seems to be a horizontal sheet, and hence the area of the channel is increased. Silicon dioxide (SiO_2) is taken as a spacer having a thickness (T_{SD}) of 5 nm, and a bilayer Al_2O_3/HfO_2 is used as a gate oxide with permittivity ranging from 15 to 20 depending on the stoichiometry, and thickness, $t_{ox} = 5$ nm. Here, the bilayer dielectric constant ($\varepsilon_r = 15$) and SiO_2 dielectric constant ($\varepsilon_r = 4$) are used. The thickness (H_{ns}) and width (W_{ns}) of each sheet are taken as design variables to determine optimum RF characteristics. We have also simulated the separation between vertical spacing between two nanosheets (S_{ns}). Moreover, all simulations keep the offset from the substrate to the first sheet constant at 30 nm unless otherwise stated. From [4], a specific feature of stacked nanosheet devices is the inner spacer that functions as the effective device spacer for self-aligned junction formation. Normalized inner spacer formation is required for the integrity of the epitaxy. Here L_{gs}, which is equal to L_{gd}, defines the the access region, which is set to 50 nm initially. Furthermore, the separation between two stacks, called S_{ns} in the model, is set to 20 nm.

The extrinsic capacitances are calculated by only simulating the extrinsic part of the device. Table 2.1 summarizes considered key parameters for the target sub-7 nm technology.

2.4 High frequency model of the device

The cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) are essential performance indicators for high-frequency operation of a device. f_T represents the frequency at which the short circuit current gain of a device reaches 1 or 0 dB, while f_{max} denotes the frequency at which the power gain equals 1, as explained in [37]. These characteristics provide valuable insights into the device's high-frequency performance.

It is obvious that improving electron saturation velocity or decreasing gate length (L_g) will improve device performance at high frequencies. Although the high electron mobility and high electron saturation velocity can be achieved by utilizing high indium content channels, the reduced gate length can be attained by using electron beam lithography technique. However, the ballistic expression

Name	Value(nm)	Description
T_{sub}	100	Thickness of substrate
W_{sub}	70	Width of substrate
L_{sub}	100	Length of substrate
T_{Source}	96	Thickness of source
W_{Source}	60	Width of source
L_{Source}	100	Length of source
T_{Drain}	96	Thickness of drain
W_{Drain}	60	Width of drain
L_{Drain}	100	Length of drain
L_g	20	Length of gate
W_g	56	Width of gate
T_{SD}	20 (10-100)	Thickness of S/D spacer
L_{SD}	200	Distance between S/D spacer
W_{ns}	30 (10-100)	Width of nanosheet
L_{ns}	50	Length of nanosheet
S_{ns}	10 (10-50)	Separation between two stacks
H_{ns}	5	Height of nanosheet

Table 2.1: Key parameters for COMSOL simulation

for g_m can be used to assess a quasi-ballistic device. The f_T equation for quasi-ballistic transistors is distinct from the f_T equation for conventional transistors. The following equation is used to determine f_T in the classical limit for quasi-ballistic transistors.

$$\frac{1}{2\pi f_T} = \frac{C_{gs}+C_{gd}}{g_m+g_d} + \frac{C_{gs}+C_{gd}}{g_m+g_d}(R_s+R_g)g_d + (R_s+R_g)C_{gd} \tag{2.34}$$

$$f_{max} = \frac{f_T}{2\sqrt{(R_s+R_g)g_{ds} + 2\pi f_T R_g C_{gd}}} \tag{2.35}$$

where, C_{gs} and C_{gd} includes the sum of intrinsic and extrinsic capactiances. Also, gate resistance R_g is considered to be 10 Ω. In the model used to analyze the high frequency performance in this thesis, the gate length ranges from 10 nm to $1\mu m$ to see the high frequency trend. Although increasing L_g decreases g_m and increases capactiance, decreasing L_g increases g_m and decreases C_g, the capacitance's charge adds a delay. The simultaneous increase in g_m and decrease in oxide capacitance is the cause of the quadratic dependence of f_T on L_g. However, the gate capacitance may frequently be dominant due to dominant parasitics at short gate lengths, which has a significant impact on these scaling properties. Here equation (2.36) is the equations we used to calculate the intrinsic gate capacitance

$$C_{gg,i} = \frac{1}{C_{ox}^{-1} + C_q^{-1} + C_c^{-1}} * A = \frac{1}{C_{ox}^{-1} + C_q^{-1} + C_c^{-1}} * L_g * 2 * (W_{ns} + H_{ns}) \tag{2.36}$$

where C_{ox}, C_q and C_c represents oxide capacitance, quantum capacitanc and charge centroid capacitance separately, and L_g, W_{ns} and H_{ns} is gate length, width of the nanosheet and the height of the nanosheet, separately.

2.5 The material parameters

The nanosheets could behave as quasi-2D systems if the width of the sheet is at least ten times the thickness. The energy levels (E_n), effective mass ($m_n^\star$) and non-parabolic factor (α_n) of $In_xGa_{(1-x)}As$ sheets are calculated for free-standing quantum well using 8-band k·p theory model.

The device's semiconductor (channel and highly doped contacts) was considered a distributed capacitance limited by the density of states in our simulations. The quantum capacitance for 2D systems is given by equation (2.37). Here $m_n^\star$ means the n^{th} subband effective masss and we consider only one subband for capacitance. Given that the sub and separation is large at room temperature and effect of higher sub bands can be neglected. This is valid is free standing thin quantum wells. The effective mass is calculated from the 8-band k·p theory for various nanosheet compositions, and the values are shown in table 2.2.

Width(nm)	InAs	$In_{0.53}Ga_{0.47}As$	$In_{0.8}Ga_{0.2}As$
3	0.0522	0.114	0.0945
5	0.0382	0.0721	0.0602
7	0.0328	0.0583	0.048
10	0.0290	0.0501	0.0401

Table 2.2: Effective mass for various nanosheet width and composition

$$C_q = \frac{q^2 \times m_n^\star}{\pi \times \hbar^2} \tag{2.37}$$

$$C = \frac{\varepsilon_r \times \varepsilon_0}{d} \tag{2.38}$$

where q, $\hbar$, d, ε_r and ε_0 is the absolute value of the dielectric charge, reduced planck constant, dielectric thickness, relative dielectric constant and free space permittivity respectively.

Using the aforementioned effective masses, C_q is calculated for various sheet heights and compositions. This is equated for parallel plate capacitor in equation (2.38) with d =1 nm and ε_r is calculated and summarized in the table 2.3.

Width(nm)	InAs	$In_{0.53}Ga_{0.47}As$	$In_{0.8}Ga_{0.2}As$
3	3.9481	8.6166	7.1465
5	2.8921	5.4492	4.5529
7	2.4805	4.4116	3.6317
10	2.1890	3.7868	3.0341

Table 2.3: Relative dielectric constant calculated for various quantum well thickness and compositions.

Chapter 3

Simulation Results and Discussion

3.1 Intrinsic device performance analysis

Since a single nanosheet carries less current, nanosheet transistors are used as multi-channel structures to increase the driving current. For an nanosheet, the performance of a device could be extremely affected by the dimension of a nanosheet or the material of a device, which can change the carrier mobility.

In the intrinsic model, two sub bands are considered for current calculations and their respective parameters, such as effective mass, sub-band energy and non-parabolicity are listed in Appendix A. Nanosheet performance in terms of indium composition, channel thickness and DC performance metrics disc used in the previous chapter are explored further.

3.1.1 Study of indium composition (x)

In this section, the purpose of this experiment is to study the effect on performance by changing the indium composition within the material. The object material for this project is $In_xGa_{1-x}As$. Where x is the percentage of indium composition. Electric current and transconductance will be the criteria for performance evaluation. In this scenario, we set electron mean free path $\lambda = 100$ nm, gate length $L_g = 20$ nm and channel thickness $H_{ns} = 5$ nm. With the given λ and L_g, the transmission probability becomes, $T = 0.83$. Figure 3.1 and figure 3.2 show the effect on current and transconductance when changing indium composition at 300 K absolute temperature.

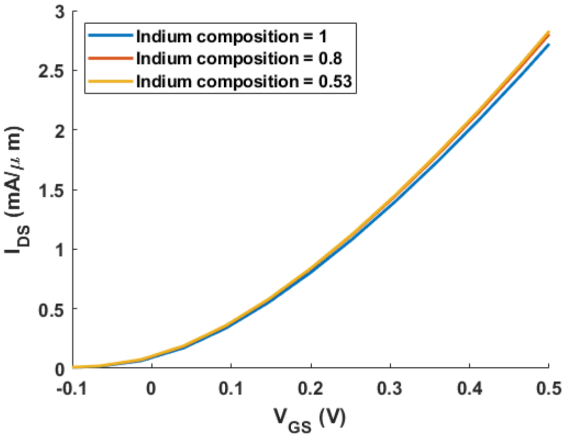


Figure 3.1: The transfer characteristics with various indium compositions.

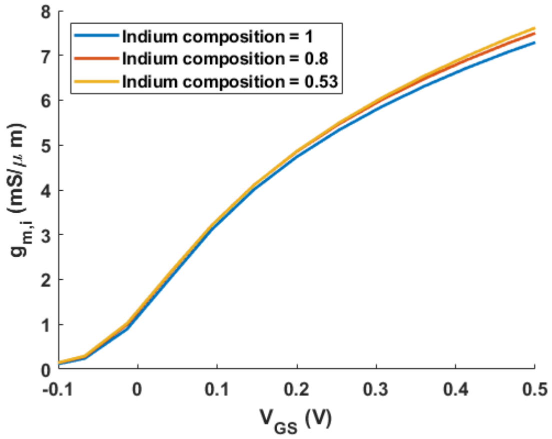


Figure 3.2: Transconductance ($g_{m,i}$) vs voltage from gate to source (V_{GS}) with indium composition variation.

According to the results, by reducing the indium composition, the ability to conduct current is improved. This is due to the increased density of states at the composition has reduced and hence current increases. For a $InGaAs$ material device, as we are considering same mean free path for all indium composition, and thus lower indium content channel has higher $g_{m,i}$.

3.1.2 Study of channel thickness (H_{ns})

In this scenario, the purpose of this experiment is to study the effect on performance by changing the channel thickness. Electric current and transconductance will be the criteria for performance evaluation as well. We keep the mean free path $\lambda = 100$ nm, indium composition $x = 1$ and gate length $L_g = 20$ nm. Figure 3.3 and 3.4 show the effect on current and transconductance when changing channel thickness at 300 K absolute temperature.

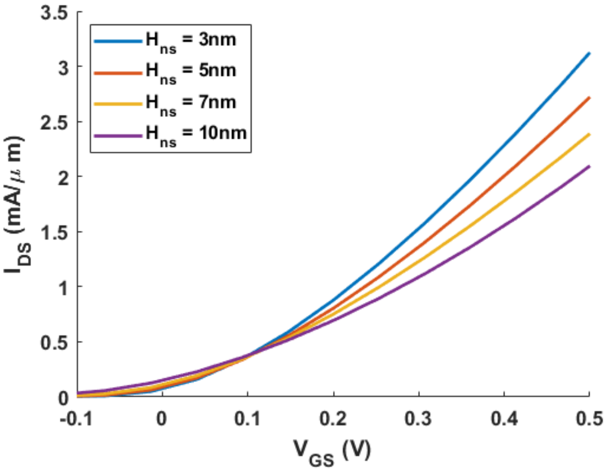


Figure 3.3: Transfer characteristics of the InAs NSFET with various channel thickness.

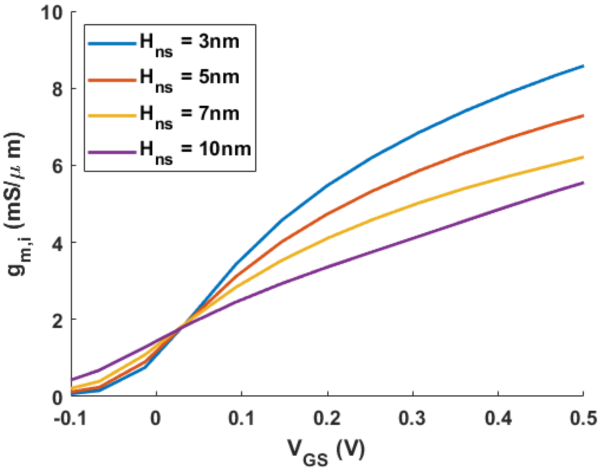


Figure 3.4: Transconductance ($g_{m,i}$) vs voltage from gate to source (V_{GS}) with channel thickness variation.

In this section, we increase the channel thickness H_{ns} from 3 nm to 10 nm. By researching I_{DS} and $g_{m,i}$, increasing of H_{ns}, the performance of I_{DS} and $g_{m,i}$ is gradually decreasing. when $H_{ns} = 3$ nm, the device has the best performance. We can also observe that the sub-threshold swing increases or current in the off-state increases as the sheet thickness increases. This could be due to poor control of gate on the channel.

3.1.3 Study of gate length (L_g)

As for this section, the purpose is to study the effect on performance by changing the gate length. We keep the mean free path $\lambda = 100$ nm, indium composition $x = 1$ and channel thickness $H_{ns} = 5$ nm. Figure 3.5 and figure 3.6 show the effect on current and transconductance when changing gate length at 300 K absolute temperature.

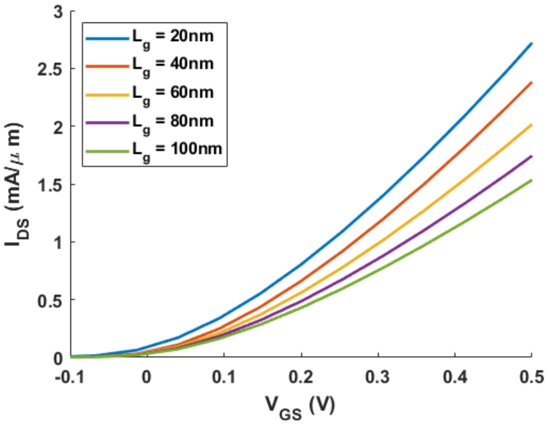


Figure 3.5: Transfer characteristics of InAs NSFET with various L_g

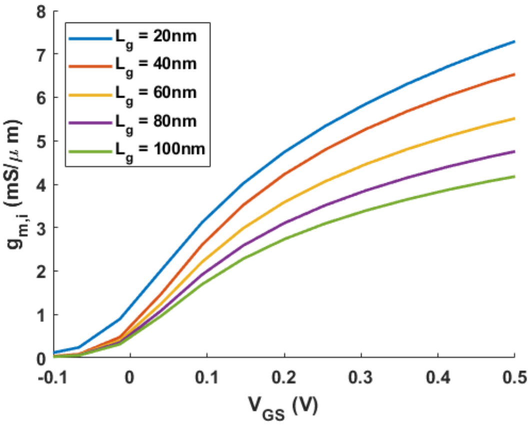


Figure 3.6: Transconductance ($g_{m,i}$) vs voltage from gate to source (V_{GS}) for various gate lengths.

The gate length is shorter, the performance is better. The best gate length is 20 nm in this experiment. In the next section, the experiment will continue to the gate length study.

3.1.4 Study of intrinsic transconductance from gate tor source & gate length ($g_{m,i}$ - L_g)

Mean free path (λ)

In this section, we will focus on the impact on intrinsic transconductance when changing mean free path λ of a device. We keep the factors indium composition $x = 1$, channel thickness $H_{ns} = 5$ nm and the gate length L_g variation from 10 nm to 120 nm. The transconductance is taken at an overdrive voltage of $V_{GS} - V_T = 0.3$ V and $V_{DS} = 0.5$ V. Figure 3.7 shows the conductance with different mean free path respectively when the absolute temperature at 300 K.

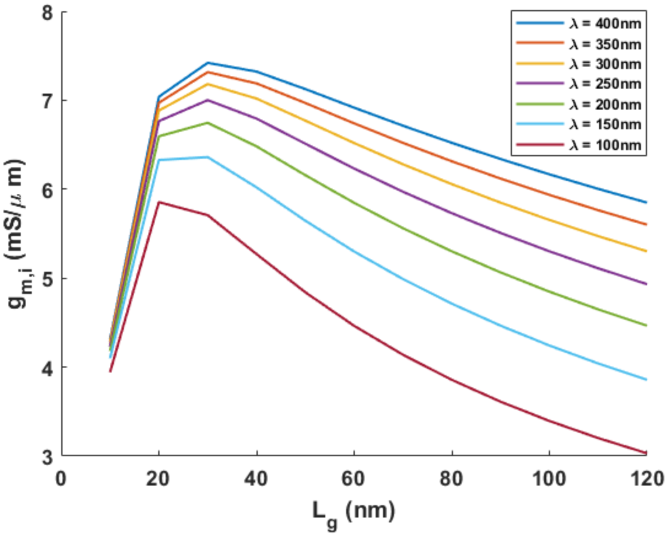


Figure 3.7: Transconductance ($g_{m,i}$) vs gate length (L_g) for various mean free paths, when V_{GS}-$V_T = 0.3$ V and $V_{DS} = 0.5$ V.

The device with 400 nm mean free path has the best performance which has the largest intrinsic conductance. The one with 100 nm mean free path has the lack performance. According to the results, it indicates the a larger mean free path will have a larger conductance. And this will lead to pure ballistic device performance.

Indium composition (x)

In this section, the model will focus on researching the effect on performance by changing indium composition x. The transconductance will be the criteria for performance evaluation. The device will be observed at $V_{GS} - V_T = 0.3$ V, $V_{DS} = 0.5$ V and $V_T = 0.5$ V when changing gate length from 10 nm to 120 nm. Keeping H_{ns} equal to 5 nm. Figure 3.8 and Figure 3.9 show the results in absolute temperature at 300 K and 12 K.

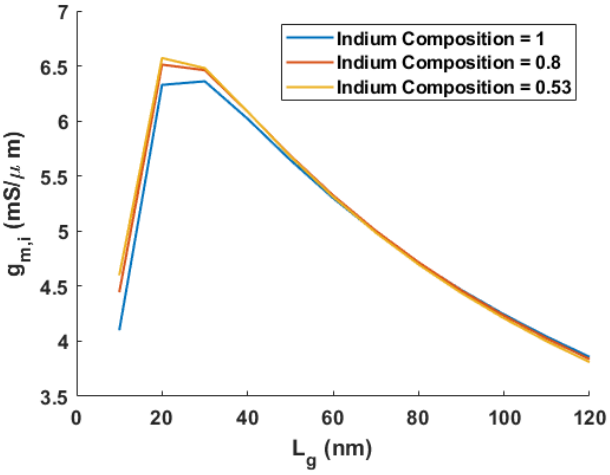


Figure 3.8: Transconductance ($g_{m,i}$) vs gate length (L_g) for various nanosheet channel compositions.

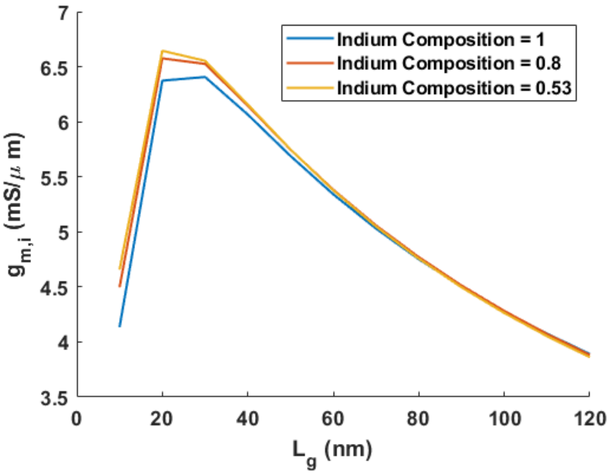


Figure 3.9: Transconductance ($g_{m,i}$) vs gate length (L_g) for various nanosheet channel compositions at T = 12 K.

There are small differences between the curves of the two graphs. According to the results, the $g_{m,i}$ gets the best performance when indium composition $x = 0.53$

in any of two different temperatures. A lower temperature will lead to better performance.

Channel thickness (H_{ns})

In this section, the model will focus on researching the effect on performance by changing channel thickness H_{ns}. The device will be observed at $V_{GS} = 0.8$ V, $V_{DS} = 0.5$ V and $V_T = 0.5$ V when changing gate length from 10 nm to 120 nm as well. Keeping indium composition x equal to 1. Figure 3.10 shows the result of intrinsic transconductance when absolute temperature at 300 K. Table 3.1 shows the best $g_{m,i}$ in different parameters respectively.

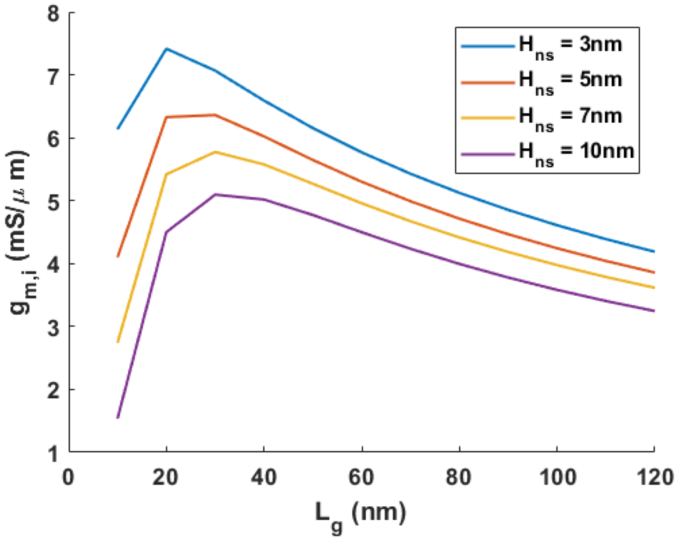


Figure 3.10: Transconductance ($g_{m,i}$) vs gate length (L_g) with channel thickness variation.

g_m(mS/μm) / H_{ns}	L_g(nm)	$g_{m,i}$
3 nm	20	7.414
5 nm	30	6.361
7 nm	30	5.773
10 nm	30	5.095

Table 3.1: The maximum value of $g_{m,i}$ with different channel thickness at 300 K absolute temperature.

The table have shown the maximum $g_{m,i}$ for channel thickness H_{ns} and gate length L_g respectively in this experiment. And it shows that smaller channel thickness and shorter gate lengths give better performance.

3.1.5 Study of on-resistance & gate length (R_{on} - L_g)

Indium composition (x)

In this part, on resistance, R_{on} will be the study purpose. According to the power equation, a lower R_{on} leads to a lower power consumption. With the same scenario, the lower R_{on} device will have a better performance. In this project, the factors used are kept, channel thickness H_{ns} = 5 nm and mean free path λ = 100 nm. The gate length L_g varieties from 10 nm to 120 nm. Figure 3.11 shows the on resistance curves respectively with different indium composition when changing gate length at absolute temperature 300 K.

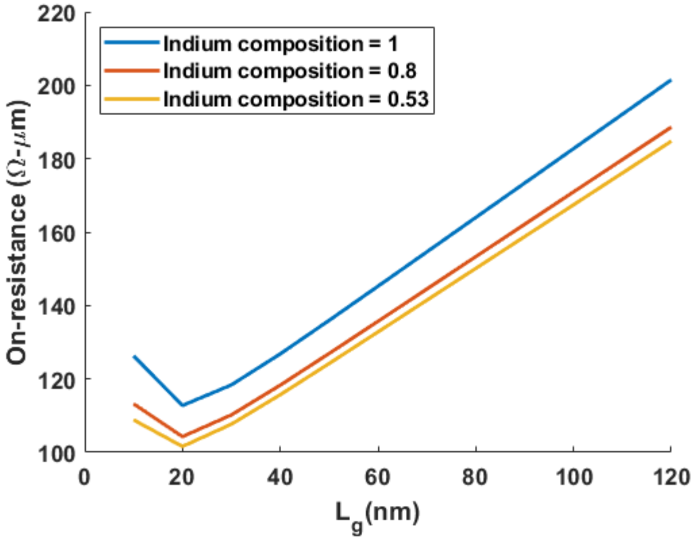


Figure 3.11: On-resistance (R_{on}) vs gate length (L_g) for various indium compositions.

Smaller on-resistance can reduce the power consumption extremely which means better device performance. In figure 3.11, the device with 0.53 indium composition has the lowest on resistance.

Channel thickness (H_{ns})

The same criteria will be observed in this section, changing study objective from indium composition into channel thickness. Where indium composition $x = 1$ and mean free path λ = 100 nm. Figure 3.12 shows the on resistance curves respectively with different channel thickness when changing gate length at absolute temperature 300 K.

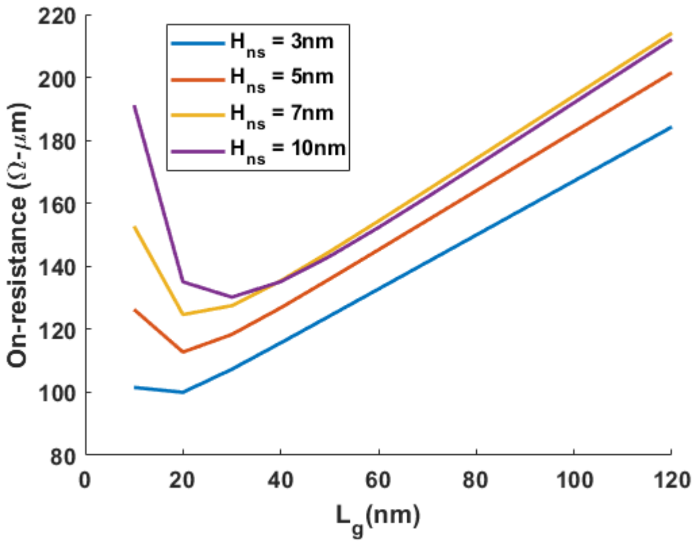


Figure 3.12: On-resistance (R_{on}) vs gate length (L_g) with channel thickness variation.

In summary, as the gate length increases, the thinner channel thickness will be more advantageous in terms of on resistance. When H_{ns} is equal to 3 nm, it will have a lowest on resistance in general.

3.1.6 Study of intrinsic transconductance from drain to source & gate length ($g_{d,i}$ - L_g)

Indium composition (x)

In this section, $g_{d,i}$ variation with gate length will be the study purpose. The criteria of $g_{d,i}$ has given by function 2.32 which defined by I_{DS} and V_{DS}. Where channel thickness $H_{ns} = 5$ nm and mean free path $\lambda = 100$ nm. Figure 3.13 shows the $g_{d,i}$ respectively with different indium composition when changing gate length at absolute temperature 300 K.

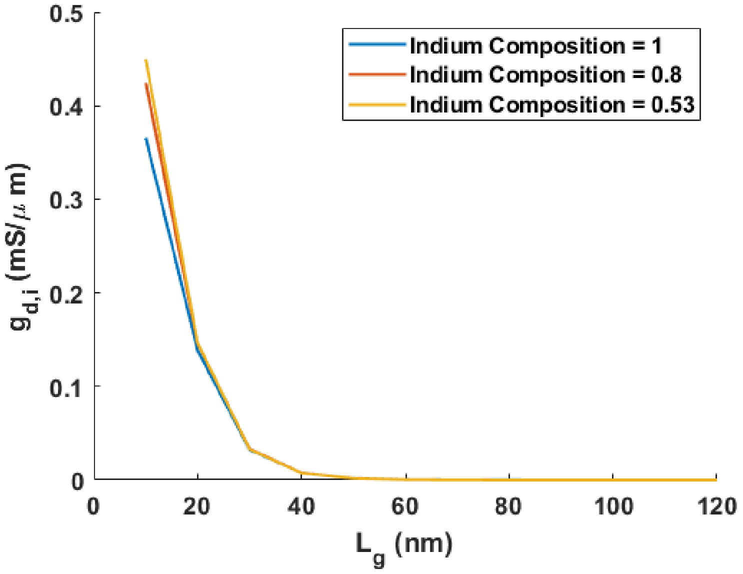


Figure 3.13: Transconductance $(g_{d,i})$ vs gate length (L_g) for various indium compositions.

Due to the short channel effect, the conductance $g_{d,i}$ between the source and drain will appear when the gate length is less than 50 nm. According to the results, the device with 0.53 indium composition has the largest $g_{d,i}$ value. It means the device with lower indium composition will be more conductive.

Channel thickness (H_{ns})

The same criteria will be observed in this section, changing study objective from indium composition into channel thickness. Where indium composition $x = 1$ and mean free path $\lambda = 100$ nm. Figure 3.14 shows the $g_{d,i}$ respectively with different channel thickness when changing gate length at absolute temperature 300 K.

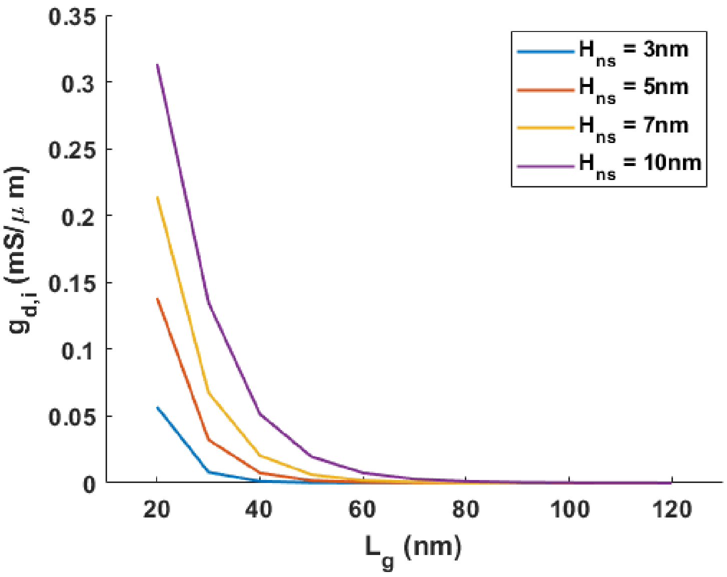


Figure 3.14: Transconductance ($g_{d,i}$) vs gate length (L_g) with channel thickness variation.

The conductance $g_{d,i}$ between the source and drain will appear when the gate length is less than 80 nm. The device with 10 nm channel thickness has the largest $g_{d,i}$ value. Thinner channel thickness will provide better conductivity. As the thickness of the channel increases, the gate control decreases. The device with 3 nm channel thickness will have the best performance.

3.1.7 Study of extrinsic transconductance ($g_{m,e}$)

In this section, we will focus on extrinsic transconductance which equation is given by equation 2.31. We changed mean free path $\lambda = 150$ nm. We keep indium composition $x = 1$ and channel thickness $H_{ns} = 5$ nm. The $InAs$ NSFET with channel thickness of 5 nm and access region of 20 nm is considered for $g_{m,e}$ calculations. Further, variation in $g_{m,e}$ for different channel widths and access region concentration is studied. The considered access region carrier concentrations are 3×10^{19} cm^{-3}, 1×10^{19} cm^{-3} and 1×10^{18} cm^{-3}, widths of the sheet are 100 nm and 500 nm. The electron mobility is 6000 cm^2/(V $\cdot$ s). The $g_{m,e}$ vs L_g of NSFET with width of 100 nm and 500 nm are illustrated in Figure 3.15 and figure 3.16, respectively.

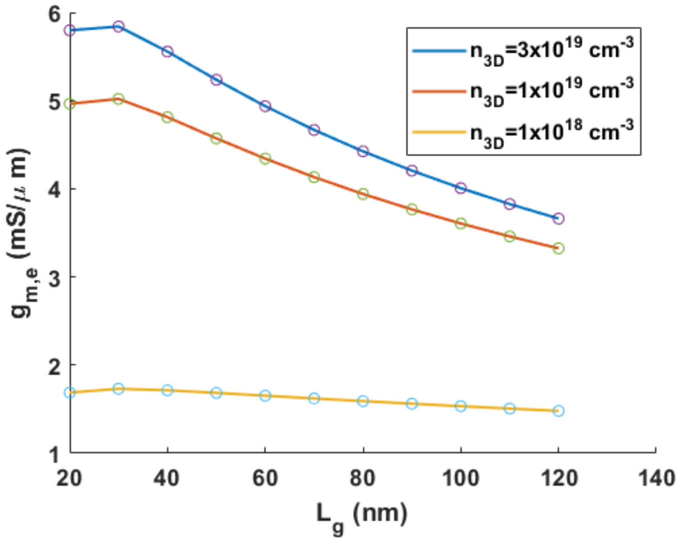


Figure 3.15: The extrinsic transconductance ($g_{m,e}$) vs gate length (L_g) with the carrier concentrations variation in the case of 100 nm channel width.

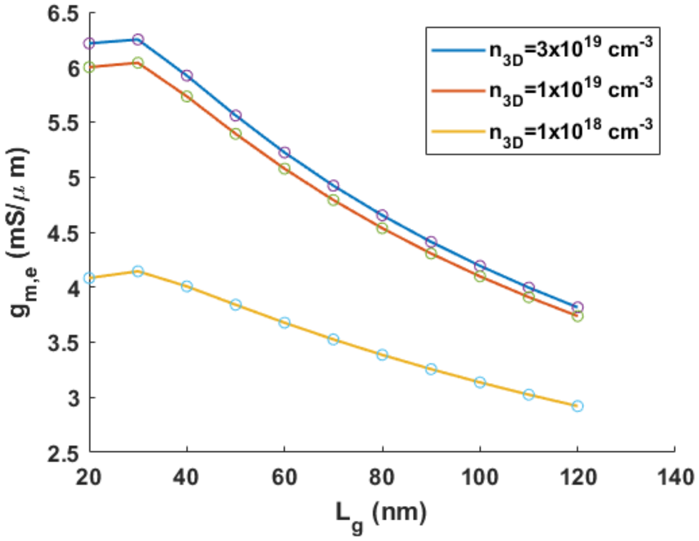


Figure 3.16: The extrinsic transconductance ($g_{m,e}$) vs gate length (L_g) with the carrier concentrations variation in the case of 500 nm channel width.

According to the results, a high carrier concentration device will get a better conductivity. A wider channel width will narrow the gap in conductance performance between devices with low carrier concentration and devices with high carrier concentration.

3.1.8 Study of sub-threshold swing (SS)

Sub-threshold swing will tell about the short channel effects or the gate electrostatic control on the channel. Ideal, SS in a MOSFET in Boltzmann limit at room temperature is 60 mV/dec. If SS is higher than the lowest limit, it is the result of poor gate control. SS vs L_g for $InAs$ NSFET with channel thickness 5 nm at 300 K is plotted in figure 3.17.

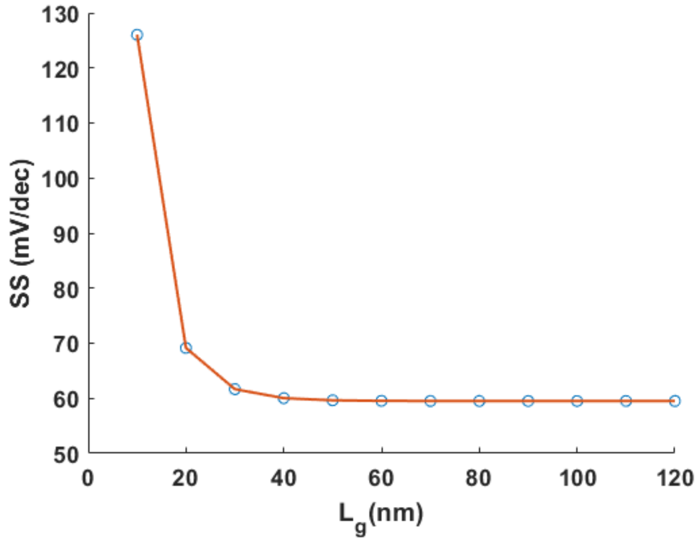


Figure 3.17: The sub-threshold swing with the with various gate length at 300 K.

It is observed from the above figure that, as the gate length becomes smaller than 20 nm, SS started to increase. In real, experiments, SS will be higher than this due to interface traps, which is neglected in this work.

3.1.9 Output characteristic

Figure 3.18 shows the output characteristics of NSFET with gate length $L_g =$ 10 nm. Figure 3.19 shows the $V_{DS} - I_{DS}$ of NSFET with gate length, $L_g = 80$ nm.

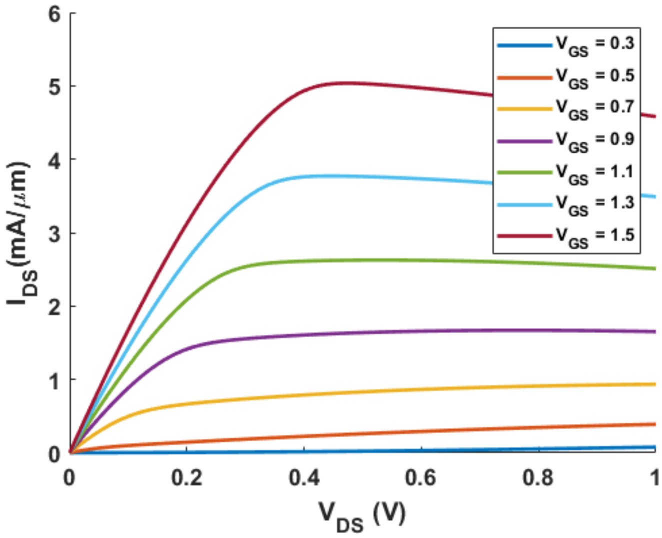


Figure 3.18: The output characteristic when gate length $L_g = 10\ \mathrm{nm}$ with the absolute temperature at 300 K.

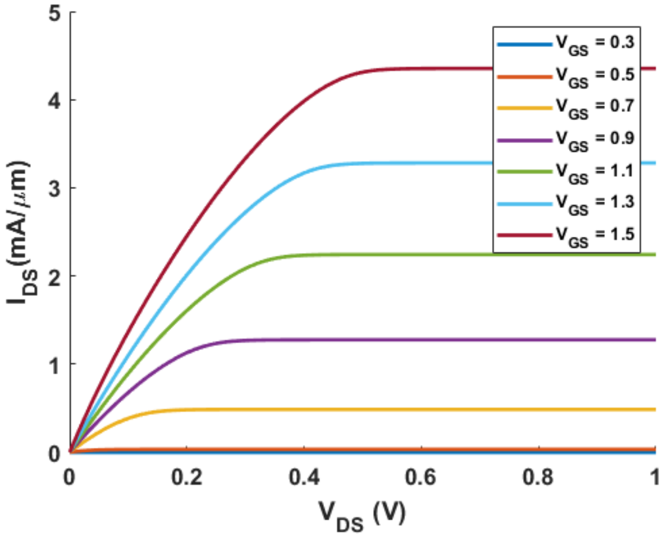


Figure 3.19: The output characteristic when gate length $L_g = 80\ \mathrm{nm}$ with the absolute temperature at 300 K.

3.2 Extrinsic device performance analysis

To get estimate of extrinsic capacitances, only device parasitic part is considered. Also, the respective electric filed contour plot of the 4 nano sheets vertically stacked are plotted in figure 3.20 and figure 3.21.

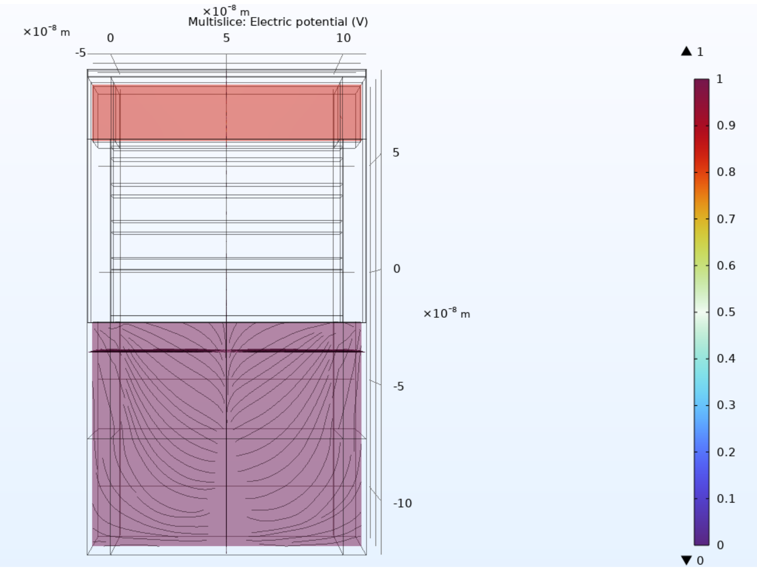


Figure 3.20: The electric field contour in single stack with four-nanosheets.

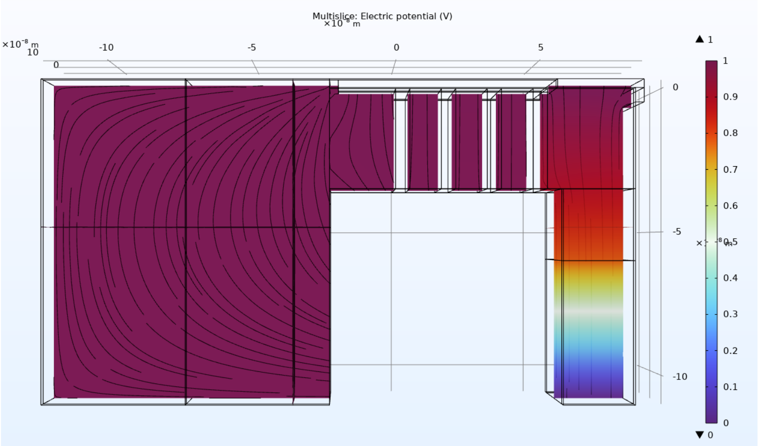


Figure 3.21: Side view of the electric field contour in single stack with four-nanosheets.

The parasitic capacitances have been calculated. The simulation is based on geometry optimization and changing the ε_r of the spacer material. The relative permittivity (ε_r) of the embedded material is chosen to be 3.9, which corresponds to the expected relative dielectric constant value of the Hydrogen Silsesquioxane (HSQ) spacer. Periodic boundary condition in the transistor unit cell was considered to estimate the capacitances of a single nanosheet stack. The obtained capacitance is normalized to number of sheets in a stack and nanosheet perimeter. In the beginning, it was interesting to study how the parasitic capacitances of the modeled 3D structures depend on the permittivity of the spacer material. The NSFET is symmetric around the gate length, which means $L_{gs} = L_{gd}$, hence gate-to-source parasitic is equal to gate-to-drain parasitic capacitance, $C_{gs,p} = C_{gd,p}$, as a function of the relative permittivity, that is varied between 2.00 and 9.00. It is noted that the capacitance is linearly dependent on ε_r, and a minimized capacitance is obtained for smaller ε_r. It is preferable to keep the relative permittivity of the insulating material as low as feasible in order to reduce the parasitic capacitances.

The capacitance is estimated for various nanosheet sizes and compositions in the following subsections. The goal is to optimize the device design to get the lowest possible parasitic capacitances. In general, for HEMTs or MOSFETs, the parasitic capacitance typically falls within the range of 0.25 $fF/\mu m$ to 0.4 $fF/\mu m$. In our simulation results, we observe that the parasitic capacitance values are relatively low. It is important to note that this is an estimate, and the actual capacitance in practice might be slightly higher. This phenomenon is primarily associated with the screening of electric fields.

3.2.1 Sheet width

For FinFETs, the utilization of multi-fin structures is employed to achieve this objective [28]. By increasing the number of fins in a multi-fin FinFET transistor, the effective channel width is enlarged, resulting in enhanced drive current and transconductance. However, as the number of fins increases, gate capacitance increases proportionally while parasitic resistance decreases inversely. Consequently, the influence of layout-dependent parasitic resistances and fin-to-fin coupling capacitances on device performance varies with the number of fins.

The MBCFET, a variant of GAAFET, exhibits superior performance compared to conventional GAAFETs [38], offering improved gate control of the channel, enhanced DC performance under specific conditions, and enhanced design flexibility, enabling straightforward conversion from FinFETs to GAAFETs. By employing a direct modeling approach, different nano-sheet widths of MBCFET can be fabricated on the same wafer. Narrow nano-sheet widths are suitable for low-power applications or Static Random Access Memory (SRAM), while wider widths are advantageous for high-performance scenarios. Therefore, optimizing device performance can be achieved by employing variable widths of the nano-sheet [39].

In conclusion, it is important to consider the impact of nanosheet width (W_{ns}) on parasitic capacitances, as an increase in W_{ns} generally leads to higher capacitance, which in turn negatively affects circuit delay ($\approx \frac{CV}{I}$). Additionally, W_{ns} influences the active area (footprint) of the device, thereby impacting para-

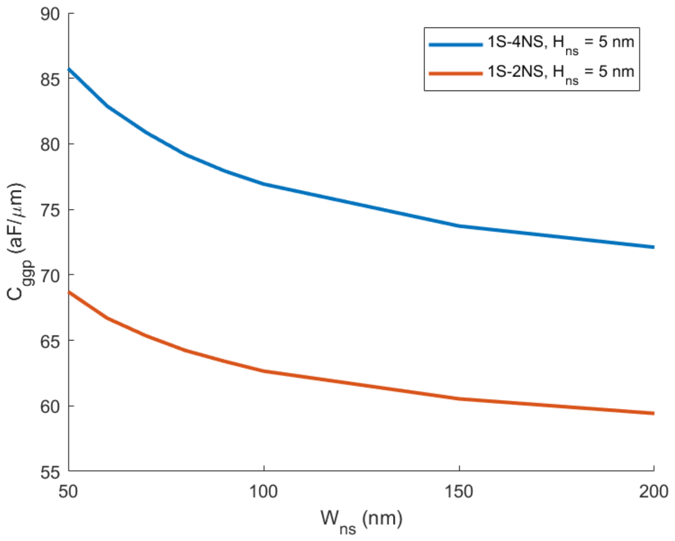


Figure 3.22: The normalised gate parasitic capacitance vs nanosheet width for two scenarios: 1 stack with 4 NS vertically stacked and 1 stack with 2 NS vertically stacked.

sitic components. To gain a comprehensive understanding of devices with varying nanosheet widths, it is crucial to carefully evaluate the number of fins and stacked nanosheet channels while maintaining the same footprint.

From our simulation results, parasitic capacitance increases with width of the nanosheet, as shown in figure 3.22. Here, 1S-4NS means 1 stack with 4 nanosheets stacked vertically and 1S-2NS means 1 stack with 2 nanosheets stacked vertically. It is also observed that the device height increase lead to more parasitic capacitance. So the nanosheet architecture provides flexibility to tune the channel width, giving more freedom in design. Instead of increasing the drive current, we can reduce the component size to acquire lower capacitance. The parasitic capacitance between the layers can be reduced with a narrower channel design.

According to [40], the wide and single fin NSFET demonstrates the highest drive current gain, while the narrow and multiple fin NSFET exhibits significantly lower drive current. However, as the gate length decreases, the wide nanosheet width suffers from poorer SS, leading to degraded gain. The wide and single fin NSFET also experiences limitations in ring oscillator frequency due to increased channel and parasitic capacitances, despite its larger drive current. The extension resistance decreases with increasing nanosheet width, but the contact resistance becomes more significant due to reduced contact area in multiple fins. Additionally, the multi-fins NSFET has higher parasitic resistance, necessitating careful control of extension doping. In terms of capacitance, the multi-fin NSFET offers advantages, with larger nanosheet width resulting in increased channel, overlap, and fringe capacitances. However, at iso-footprint, the parallel plate capacitance remains relatively similar. Therefore, while the wide and single fin NSFET may

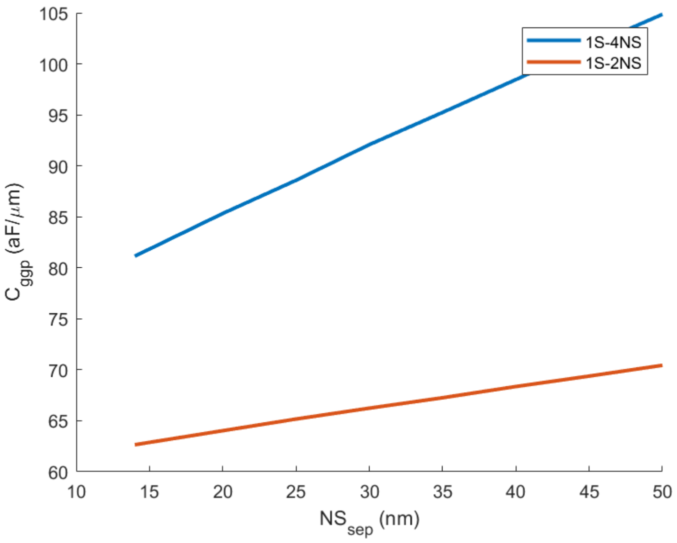


Figure 3.23: Normalised gate parasitic capacitance vs sheet separation for two different nanosheet stack configuration.

offer optimal DC performance, the presence of larger parasitic capacitances diminishes its circuit performance gain at the same footprint.

3.2.2 Sheet separation

If the sheet separation is reduced, it will result to perpetuation of proper electrostatics. The narrow vertical spacing between the sheets will screen the electric field and parasitic capacitance reduces, as shown in the figure 3.23.

3.2.3 Sheet thickness/height

The effect of H_{ns} is similar with W_{ns}, as shown in figure 3.24, and $InAs$ nanosheets are considered. With the increase of H_{ns}, the area of Nanosheet will increase, so the the current per nanosheet will also increase. But because of the increase of the contact area between nanosheet channel/ extension source(drain) spacer and gate, the corresponding parasitic capacitance will also increase.

3.2.4 Source/drain spacer

L_{sd} is the total separation between source to drain contact, which is sum of gate to source separation (L_{gs}), gate length, and gate to drain separation (L_{gd}). Here the device is symmetric, and the whole channel length L_{sd} is 200 nm, so $L_{gs} = L_{gd} = 100$ nm. From above analysis, parasitic capactiance increases with stack spacing. Figure 3.25 and figure 3.26 show that the parasitic capacitance decreases with the increase in the gate source distance for various spacer dielectric

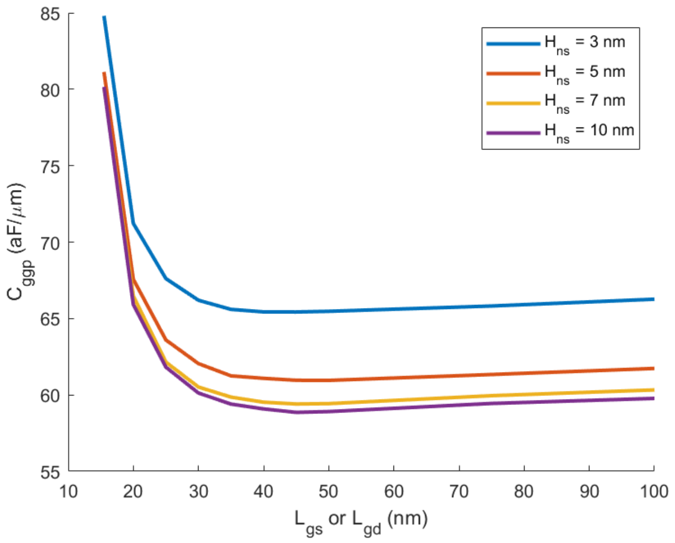


Figure 3.24: Normalised gate parasitic capacitance vs gate to source or drain separation for various nanosheet heights at a constant vertical separaiton.

constants and various nanosheet composition. Total gate parasitic capacitance vs L_{gs} or L_{gd} is calculated for various channel thickness, inner spacer dielectric and channel composition and are plotted in figure 3.24, 3.25 and 3.26 respectively. It is noticed that, in all cases $C_{gg,p}$ decreases with increase in L_{gs} or L_{gd}. Hence, for optimum capacitances, larger L_{gs}, thinner sheets and smaller device height is desired.

To calculate the capacitance in this case, the dielectric constant is also taken into account. The outcome agrees with equation (2.38), showing that capacitance decreases with smaller inner spacer dielectric constant. Different compositions correlate to various dielectrics; x is the composition percentage of In in $In_xGa_{(1-x)}As$. Table 2.3 displays the equivalent dielectric constant. The composition proportion of 0.53 is better to obtain a larger capacitance because of larger density of states compared to higher indium composition channels, as shown in figure 3.26, and this should be the guideline for selecting the material.

3.2.5 Single vertical stack height

Increasing the number of stacked nanosheet channels is a favorable approach for enhancing the drive current, although it results in increased parasitic capacitance due to the greater device height. To address this issue, reducing the vertical pitch can help alleviate the impact. The gate parasitic capacitance, denoted as $C_{gg,p}$, exhibits sensitivity to the spacing between adjacent stacks, as it expands the source/drain epi-regions, contributing to the overall parasitic capacitance. Consequently, $C_{gg,p}$ rises with the increasing number of stacks, indicating that a min-

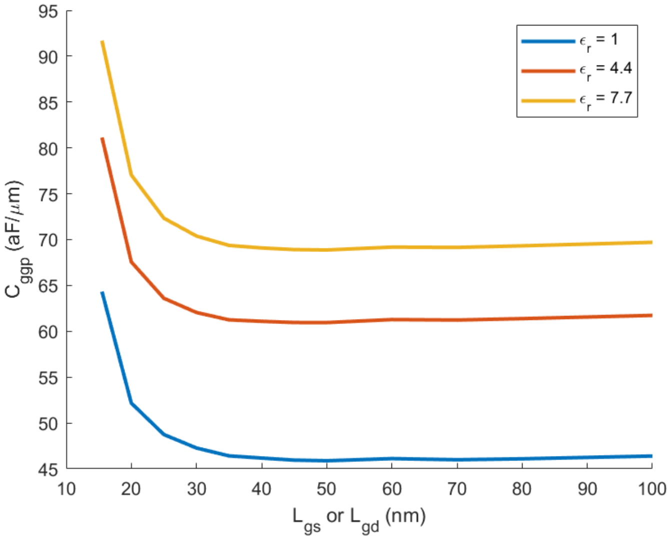


Figure 3.25: $C_{gg,p}$ vs L_{gs} for various spacer dielectric constants at room temperature.

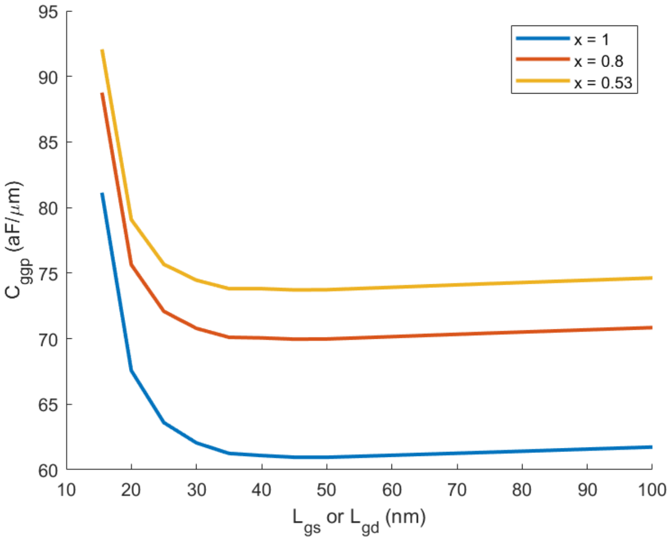


Figure 3.26: $C_{gg,p}$ vs L_{gs} for various nanosheet compositions when the spacer dielectric constant is 1. The indium composition in the channel changes the density of states and hence the capacitance variation is observed.

imal stack number is desirable for optimal design. In this study, we calculate the parasitic capacitance for a single vertical stack containing both two and four nanosheets, as illustrated in Figure 3.22 and Figure 3.23. To facilitate comparison, we utilize the normalized parasitic capacitance of a single stack. Notably, nanosheet transistors exhibit a significantly higher normalized parasitic capacitance compared to III-V HEMTs, owing to their three-dimensional structure and the presence of the gate-all-around (GAA) configuration. However, the drive current can be improved by increasing the number of stacked nanosheet channels, while reducing the spacing between adjacent stacks can help mitigate the challenge posed by high parasitic capacitance. Ongoing efforts are focused on fabricating densely packed nanosheet structures, which hold the potential to reduce stack spacing and enhance RF performance.

3.3 High frequency performance analysis

The following figure illustrates the f_T and f_{max} changes along the gate length under the fixed parameter settings.

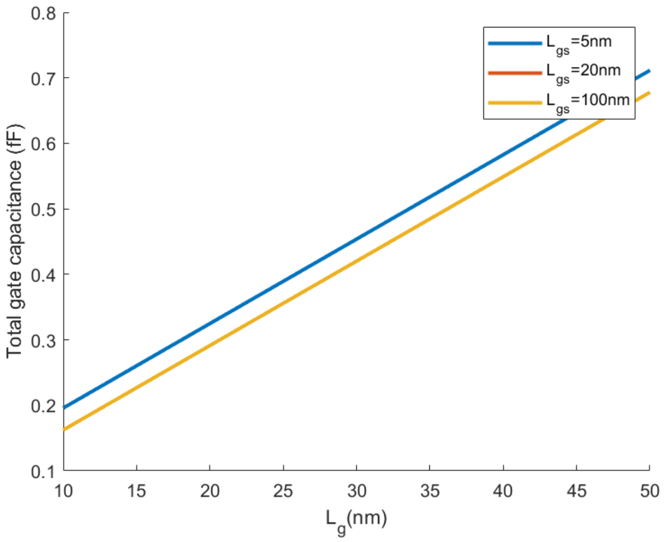


Figure 3.27: The gate total gate capacitance vs L_g for various L_{gs} of 5 , 10, 20 nm. The plots for $L_{gs} = 20\ nm$ and 100 nm overlap on top of each other.

Device with gate length 20 nm and width 10 μm and nanosheet width is 100 nm, horizontal separation between two stacks is 14 nm giving approximately 88 stacks. The total device area is $number of sheet * L_g * 2(H_{ns} + W_{ns})$. The access region between either gate to source or gate to drain is 5 nm, 20 nm and 100 nm separately and total access resistance $R_s + R_d$ is 7, 28 and 139 Ω separately. The total $g_{m,e}$ is around 3.4 $mS/\mu m$, 4.9 $mS/\mu m$, and 1.2 $mS/\mu m$ separately and they are taken at $V_{DS} = 0.5V$ and $V_{GS} - V_T = 0.3V$. The total gate capacitance is sum of intrinsic capacitance and extrinsic capactiance. The total gate capactiance C_{gg} vs L_g for various L_{gs} are plotted in Figure 3.27. There are only two plots for $L_{gs} = 5\ nm$ and $100\ nm$, the parasitic capacitance is almost the same for $L_{gs} = 20\ nm$ and $L_{gs} = 100\ nm$. After certain L_{gs} increase, the fringe capacitance saturates and we don't gain much with larger access region or L_{gs}, so it matters only in short gate length devices. The equations (2.34) and (2.35) are used to calculate the f_T and f_{max} for various device gate lengths. The high frequency relation with different gate length is plotted in the figure 3.28 and figure 3.29. It is notices that both f_T and f_{max} increase as the L_g decreases. This is explained by increase in $g_{m,e}$ and decrease in intrinsic gate capacitance. However, at shorter gate lengths, the effect of gate parasitic capacitance and resistance appear. f_T is large for devices with $L_{gs} = 20\ nm$ compared to $L_{gs} = 5\ nm$ and it is due to decrease in parasitic capacitance. However, $L_{gs} = 100\ nm$ device suffers from larger extrinsic resistances and has smaller f_T at shorter L_g. Unlike f_T, f_{max} depends on few more other parameters like smaller gate to drain capacitance, smaller $g_{d,e}$ and smaller R_g gives larger f_{max}. As the R_g and g_d are constant for a given L_g below $100\ nm$, only the effect of $C_{gd,p}$ and extrinsic resistances can be seen.

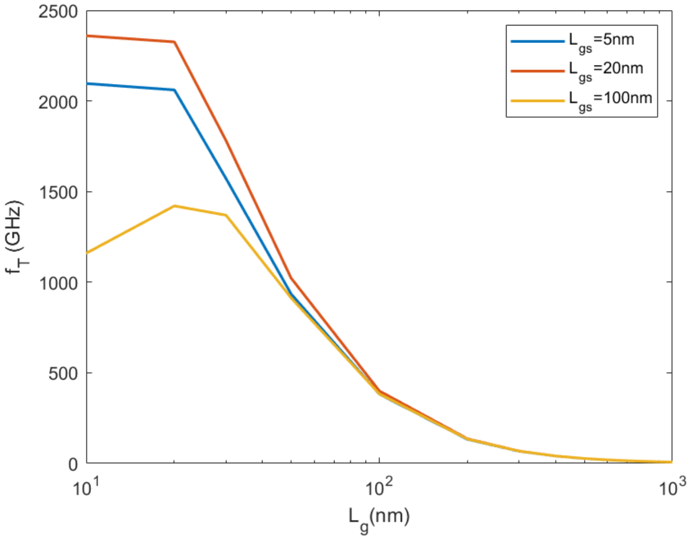


Figure 3.28: The transition frequency (f_T) vs L_g at 300 K for various L_{gs}.

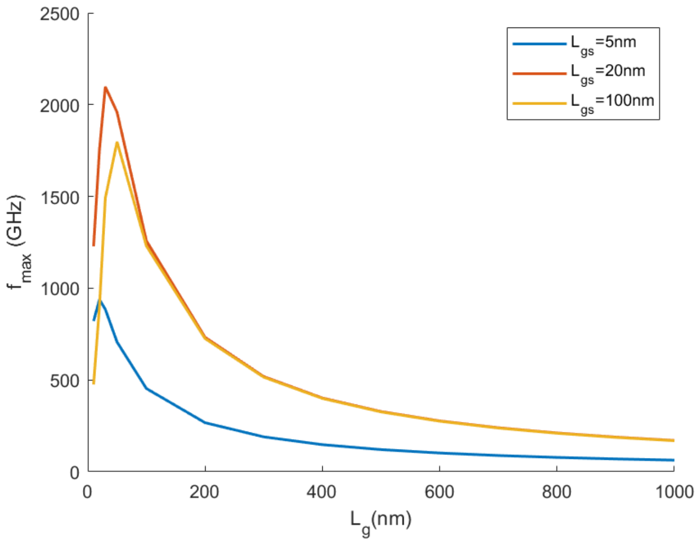


Figure 3.29: The transition frequency (f_{max}) vs L_g at 300 K for various L_{gs}.

Chapter 4

Conclusion and Future work

By studying the distribution of electrons in the channel, a III-V compound nanosheet device intrinsic part has been modeled. And in the course of the research, different sizes and different temperatures were simulated to study the performance of the device in terms of the current, transconductance and subthreshold swing. This will help in selecting high performance channel dimension for nanosheet applications. Similarly, the same experiment was simulated at 12 K and 300 K absolute temperature respectively. Temperature research will also help to study the stable working environment of the device.

Furthermore, research and calculations have been done on the parasitic capacitances in vertical nanosheet transistors. It has been demonstrated that as the distance between the nanosheets reduced, parasitic capacitances are reduced to a minimum. The electric field between the sheets is screened more thoroughly in dense nanosheet arrays. The majority of parasitic capacitance, based on our observations, increases with sheet width, thickness, sheet separation, and STI width, but decreases with source and gate separation. Therefore, it is preferable to employ multi-stacked nanosheets with narrower, thinner, and denser sheets for reduced capacitance and greater performance. To further reduce parasitic capacitance, a smaller spacer dielectric constant and a higher In composition in $InGaAs$ could be employed.

For high frequency circuit, device with higher f_T and f_{max} is a better choice. According to the simulations, a smaller gate length can be used to acquire a larger f_T and f_{max}, such as 20 nm, where f_T could reach 3450 GHz and f_{max} could be 2250 GHz when the L_{gs} is 20 nm.

Appendix A

Electronic parameters of InGaAs NSFET

A.1 Indium composition $x = 1$:

H_{ns}	No.	$m^\star$	E_1	α
3nm	1	0.0522147135872787	1.06618321193555	1.4246
	2	0.149480903841096	1.85240716742656	0.9707
	3	0.250058268496825	2.71438169424118	0.7547
	4	0.328317010081031	3.66113243248657	0.6604
5nm	1	0.0382479760730793	0.923531185354211	2.1007
	2	0.0893802672775955	1.34413881179939	1.3038
	3	0.150643027326401	1.81770251077953	1.1343
	4	0.212998450406476	2.30595103757644	1.082
7nm	1	0.0328055954275140	0.867455199046153	2.25
	2	0.0656770507756168	1.14316992867206	1.6116
	3	0.107021969742892	1.46855834487474	1.4721
	4	0.151137277961047	1.80363928961151	1.0347
10nm	1	0.0289504471431968	0.828026518697966	2.7237
	2	0.0492522786928460	1.00083104939028	1.6710
	3	0.0760798861787328	1.21739531603394	1.5781
	4	0.105332642764020	1.44544617042573	1.2947

A.2 Indium composition $x = 0.8$:

H_{ns}	No.	$m^\star$	E_1	α
3nm	1	0.0945137480181476	1.39290463567938	0.6738
	2	0.289986054218374	2.28816308287555	0.3107
	3	0.729533920995655	3.29129166473010	0.25
	4	1.96057513135361	4.37507324988198	0.3792
5nm	1	0.060213618759712	1.13756791112703	1.0761
	2	0.139443941023532	1.62073087098082	0.6767
	3	0.270182899685620	2.16938307262117	0.3245
	4	0.484069629523636	2.75406563347775	0.1622
7nm	1	0.048030507724735	1.03909787721269	1.3259
	2	0.094246596212338	1.35513490341652	0.7802
	3	0.163593633999310	1.72422664106341	0.5118
	4	0.261692555296921	2.11883971709856	0.3988
10nm	1	0.040126642920527	0.973424777045629	1.5428
	2	0.066664986812252	1.16917475810491	0.9481
	3	0.104749192838261	1.40866767049677	0.671
	4	0.154285661938180	1.66861562246663	0.5988

A.3 Indium composition $x = 0.53$:

H_{ns}	No.	$m^\star$	E_1	α
3nm	1	0.113955623746157	1.66168716372682	0.3895
	2	0.319238517534564	2.58063493475950	0.1807
	3	0.799727739994583	3.60234584230419	0.18
	4	2.431623121318251	4.70022967513303	0
5nm	1	0.072066496998488	1.36753197367436	0.6523
	2	0.150036570588999	1.85646032949688	0.3763
	3	0.277469522660927	2.41434913673922	0.2225
	4	0.485705957220856	3.00948730580227	0.1127
7nm	1	0.058344653182972	1.25985746112165	0.7701
	2	0.102333945349827	1.57210970886656	0.5249
	3	0.168179097859467	1.94363077776011	0.338
	4	0.260751743574167	2.34375143647637	0.267
10nm	1	0.050081263201672	1.19225117124206	0.9738
	2	0.074285955569948	1.37815146778978	0.6165
	3	0.109539967708303	1.61386442407014	0.4278
	4	0.155494366178171	1.87415198124336	0.3848

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