Digitally Controlled Oscillator Topologies for mm-Wave Pulsed Coherent Radar

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Digitally Controlled Oscillator Topologies for mm-Wave Pulsed Coherent Radar

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Abstract

The advancement of future generations of wireless communication and radar sensing warrants the need for mm-wave digitally controlled oscillators (DCOs) with high-frequency trade-offs in consideration. The purpose of this project is to investigate DCO topologies inspired from scientific literature. The DCO is an electronic component that takes a digital code as input to tune the output operation frequency. Acconeer's application, a pulsed coherent radar system, sets unconventional performance requirements on the DCO compared to continuous wave systems. A specific type of oscillator core, namely the cross-coupled differential-pair harmonic oscillator, has been investigated. The performance of this oscillator is subject to special trade-offs in the DCO implementation. A strategy of multiple stages was used to guide the work. First, possible solutions were crudely investigated, then promising solutions selected, and finally pre- and post-layout simulation results of said solutions were provided. Five solution alternatives were identified and benchmarked with respect to a digital equivalent of the cross-coupled differential-pair LC-VCO. These solutions present different opportunities to relax trade-offs in the design of the DCO. Benchmarking the post-layout results of the solutions with literature revealed competitive performance, considering requirements set by the radar application, which is the context of this work. The analysis of this investigation provides a foundation and suggestive guidelines of future action for Acconeer. This work also captures the state-of-the-art of DCOs for pulsed coherent radar, priming further research within the field.

Popular Science Summary

In the hunt for faster wireless communication and more advanced radar technology, the design of digital oscillators is of utmost importance.

Consider a regular day in your life, such as today. It is likely that you made or will make a phone call. Even more likely is that you will use the mobile phone that is in your pocket right now to search the web or simply scroll through social media. Even though not every single person has these habits, a large portion of today's society relies on being connected wirelessly. Wireless communication can be defined as the act of transferring information seemingly instantly, at the speed of light, from one device to another. As the technological advancement of the human race progresses, the demand for faster data transfer rates increases, which is achieved by increasing the bandwidth and modulation complexity of the transmitted electromagnetic waves. Larger bandwidths are available at higher frequencies. The frequencies in use in today's technology are typically in the gigahertz (GHz, one billion oscillations per second) region. The wavelength of a wave with a frequency of a few tens of GHz is in the order of a few millimeters, hence the name millimeter wave (mm-wave) technology. Additionally, research is currently underway to support the sub-terahertz (THz, one trillion oscillations per second) region.

The properties of electromagnetic waves can also be used for sensing applications, and the most relevant for this work, radar. Radar is a technique where electromagnetic waves are sent out, reflected on objects, and then received. The properties of the reflected light, as well as the time it took for the light to return, can be used to determine properties about the surroundings, such as position, shape, and speed of objects. The capabilities of radar increases as support for higher frequencies is developed. In the next generation of wireless communication, 6G, there's talk about integrating wireless communication with sensing to achieve ultra high data transfer rates.

When creating devices for wireless communication and radar technologies, a lot of different components must be designed. A commonly known component is the antenna, which is used to transmit and receive wireless signals. Another less commonly known component, which is also at the focus of this work, is the oscillator. An oscillator is a component that generates a periodic electric signal, and is important for the functions of the wireless communication devices. The

fundamental operation of the electrical oscillator is analogous to that of a classic pendulum. As the position of the pendulum is changing from left to right, the energy is constantly converted between kinetic energy and potential energy. The same is true for an electrical oscillator, but the position is instead a voltage value, and the energy alternates between being stored in the magnetic field of a coil and the electric field of a capacitance. However, in practice, a pendulum will ultimately stop due to some of the energy being lost to air resistance and friction between the anchor and rope. The same is true for the electrical oscillator, but the energy is instead lost to unforeseen resistance in the metal wires and components of the circuitry. The design of an electrical oscillator is fundamentally about working against the resistive parts that makes the oscillator stop. You add other components that add energy to the circuit, which keeps the oscillation stable. This is like adding a mechanism that pushes the pendulum a tiny amount on each swing to keep it from stopping.

Ultimately, this work aims to shed light on these design considerations and trade-offs under certain conditions that may turn out as useful information for this research field as well as for the host company Acconeer.

Preface

This project has been the final part of the author's educational pursuit of a Master's Degree within high frequency and nanoelectronics. The project is the author's Master Thesis project, which appropriately acts as the culmination of the contents and learning of the author during the past five years of academic endeavors. Besides its summative purposes, the thesis should act to further the research within the researched area. The project was carried out at the company Acconeer AB, and a special amount of gratitude is awarded to Stefan Andric, who has acted as the industrial supervisor of the project. Lars Ohlsson Fhager also deserves a thank you, as the academic supervisor from Lund University. Without the advice and guidance of Stefan and Lars, the project simply would not be possible.

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Chapter 1
Introduction

1.1 Motivation and Purpose

1.1.1 Wireless connectivity and Joint Communication and Sensing (JCAS)

The life of an average person today is incredibly connected. Social interactions are made wirelessly through digital means. The demand for smartphones, which just a few decades ago would be deemed a supercomputer, is steadily increasing and most people have one in their pockets at all times throughout the day. Five billion people rely on the ability to stay connected in their everyday lives [1]. The fifth generation of broadband cellular communication (5G) networks is currently being implemented, and the development of research is already investigating alternatives for 6G networks. The increase in frequency used brings new possibilities of using radar-like technologies for highly accurate sensing opportunities [2]. The concept of leveraging the capabilities of wireless communication networks for sensing to optimize the network itself is called Joint Communication and Sensing (JCAS). Currently, researchers within this area are working towards finding methods of integrating communication and sensing to ultimately increase the performance of the wireless systems of tomorrow [3][4]. Performing accurate mm-wave radar sensing is integral as the development towards realizing JCAS systems progresses.

1.1.2 Acconeer

Acconeer is a company that aims to design competitive products characterized by low power consumption, low cost and small size [5]. Their main product as of writing this thesis is their A121 pulsed coherent radar sensor, working in the operating frequency 60 GHz [6]. Acconeer's goals for their applications warrants the use of components and systems that provide state of the art performance.

1.1.3 Purpose

The aims of this thesis is to uncover information that would benefit radio frequency integrated circuit (RFIC) design research and the progression towards JCAS in pulsed coherent systems. The work also aims to bring useful insights to Acconeer about possible improvements to their current solution. The investigated solutions

is to be designed at an operation frequency of 60 GHz. The multi-faceted purpose of this project can be summarized as follows

1. Review and analyze literature on differential oscillator topologies
2. Perform simulations and determine performance in order to present possible alternatives in the same technology node as the current solution
3. Benchmark investigated solutions with DCO solutions in literature

1.2 Outline

Chapter 1 provides relevant context in terms of motivation and purpose that led to this work being conducted.

Chapter 2 provides relevant theory about fundamental harmonic oscillator theory as well as a detailed description about the characteristics, operation, and design of the voltage controlled oscillator.

Chapter 3 provides a description of the chosen method to complete the goals of this work. First, a summation of the used strategy and design flow is presented. Second, a presentation of the tools and resources used during the work is given, followed by a detailed walk-through of the conditions surrounding the simulations conducted to achieve the results of this work. Finally, the scope and limitations of the work is defined and presented.

Chapter 4 consists of a presentation of the results with corresponding analysis and discussion. The results of an investigation into possible solution alternatives are presented in the form of the selected solution, with accompanying description and motivation behind selecting the solutions. The primary results of the schematic simulations are then presented and analyzed. Next, the layout work is presented, along with results and analysis of the post-layout simulations conducted. Finally, an attempt to benchmark the results with solutions in literature is conducted through a comparison of key metrics.

Chapter 5 is the final chapter, and presents the reader with an outlook on suggestive action for Acconeer and future research work. Finally, a short conclusion of the contents of the work is presented.

Chapter 2
Theory

2.1 Conceptual introduction to one-port LC oscillators

The underlying theory of constructing electrical oscillators are described here. While there are a number of ways to achieve an oscillating electrical signal, the focus of this section is of the harmonic oscillator. The section begins by introducing the concept of the LC circuit, and the fundamental equations that dictate its oscillating behavior. The discussion is then brought to the LC circuit in practice, and the effects that challenges the engineer's intentions to use the circuit as an oscillator. Following this is a description of a common driver solution, the cross-coupled transistor pair, which offers a way to stabilize the oscillation of the LC circuit by introducing a negative resistance as well as generating a differential signal.

2.1.1 The LC-oscillator

The ideal LC-oscillator

In a harmonic oscillator, the properties of the passive inductor and capacitor are used, hence the name "LC"-oscillator (also called harmonic oscillator). These components share the fact that they introduce a reactive impedance to the circuit. This can also be explained by the storing of energy, in different forms. The inductor stores energy in the form of a magnetic field, induced by current in the coil, and the capacitor stores energy in the form of an electric field between the charges stored on its two opposite nodes. The oscillation, i.e. either a voltage or current changing direction between a certain value and its negative counterpart, is in turn provided by this varying form of storing energy. The energy is constantly switched between being stored in the inductor and the capacitor, similar to how the energy of an arm of a pendulum is switched between the different potential energy and kinetic energy.

Consider the circuit of an inductor and a capacitor coupled together, shown in Figure 2.1. If we look at either of the nodes at a point in time t, Kirchoff's current law tells us that the sum of the currents flowing through the inductor and capacitor must equal 0,

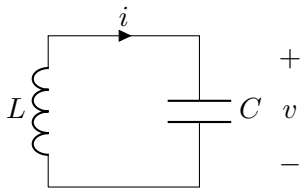

Figure 2.1: An ideal LC-circuit

$$C\frac{dv(t)}{dt} + \frac{1}{L}\int v(t)\,dt = 0. \tag{2.1}$$

To properly find a solution to $v(t)$ that we can physically interpret, we need to use the Laplace transform $\mathcal{L}$.

$$\mathcal{L}\{(2.1)\} \Leftrightarrow sCV(s) - CV(0) + \frac{1}{sL} = 0 \Leftrightarrow V(s) = \frac{s}{s^2 + \omega_0^2}V(0), \tag{2.2}$$

where $\omega_0 = 1/\sqrt{LC}$. Using the inverse Laplace transform, an expression of the voltage as a function of time $v(t)$ can be derived, given an initial voltage of V_0,

$$\mathcal{L}^{-1}\{V(s)\} \Leftrightarrow v(t) = V_0\cos(\omega_0 t). \tag{2.3}$$

Equation 2.3 shows that the qualitative analysis of the LC circuit results in a time varying voltage signal, with cosinusoidal characteristics and peak voltage V_0 as large as the initial voltage. This feature of the LC circuit can be imagined through a set of subsequent steps as follows

1. A voltage V_0 is present across the two terminals of the LC circuit
2. The voltage induces a current through the inductor, which eventually results in 0 voltage across the capacitor and maximum current flowing through the inductor
3. The flowing current is opposed by the inductor, which results in an induced voltage of opposite polarity accumulating on the capacitor plates
4. The accumulating voltage eventually reach $-V_0$ when the current reaches 0.
5. The same process resets, except with opposite directions
6. Back to step 1.

This thought process is analogous to the claim that energy is oscillating between being stored in the inductor's magnetic field and the capacitor's electric field. When the voltage reaches its peaks the energy is theoretically all stored as the capacitor's electric field, and when the current reaches its peaks the energy is theoretically all stored as the inductor's magnetic field. The initial voltage V_0 is an important concept in practice, since just like a pendulum, you either have to start the pendulum off with a nudge from it's stationary position, or by lifting it to a certain amplitude and dropping it.

The LC-oscillator in practice

If the analogy of the pendulum is reused, an observer that starts the pendulum off at a certain amplitude will notice that the pendulum does not return to its exact starting position. Eventually, the pendulum will stop swinging and stay stationary. This is an effect that's caused by friction in the air, which means that in between the conversions from potential to kinetic energy and kinetic to potential energy, all of the energy is not converted. Some of the energy is dissipated due to the pendulum's collision with air molecules (i.e. air resistance) and friction between the pendulum arm and the joint.

An analogous rule applies to an LC oscillator, since the electrical circuit also falls victim to unwanted dissipations during the energy conversion between the inductor and capacitor. In practice, the inductor is basically a certain arrangement of a conductor, which in itself has a resistance. The capacitor keeps the voltage potential across its plates in theory, but in practice the insulating material between the plates actually have a small conductance. These effects can be described by considering the circuit as it will act in practice in Figure 2.2.

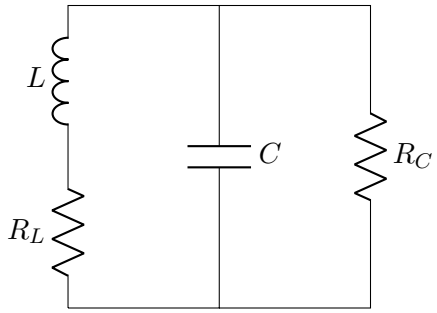

Figure 2.2: The LC circuit with accompanied resistive elements.

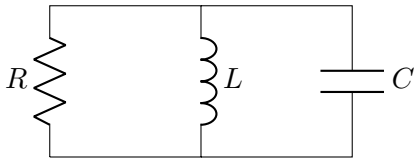

Figure 2.3: The same circuit as in Figure 2.2 after transformation.

If R_L is transformed to a parallel resistance and subsequently added with R_C in parallel, an equivalent first order RLC circuit is realized as in Figure 2.3. Essentially what is wanted is to effectively remove R, which can be achieved if an element with value $-R$ was added in parallel with the circuit,

$$R_{R||-R} = \frac{1}{\frac{1}{R} - \frac{1}{R}} \to \infty. \tag{2.4}$$

An infinite resistance in parallel would effectively mean that the influence of the resistive elements of the inductance and capacitor would be removed. What's left in theory is a pure LC-oscillator, which should have characteristics close to those described in Section 2.1.1. In practice, from a small-signal perspective, an excess of negative resistance is needed to start the oscillation. This description of the operation of an oscillator is often referred to as the one-port view, shown in Figure 2.4.

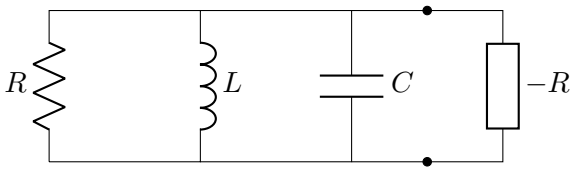

Figure 2.4: The one-port view of oscillators

Cross-coupled NMOS pair

A negative resistance element, $-R$, supplies energy to the circuit. This requires active circuit elements, such as transistors. The cross-coupled NMOS pair comes in handy here, and it will be shown below how this circuit can effectively add a negative resistance. The circuit of the cross-coupled pair is shown in Figure 2.5.

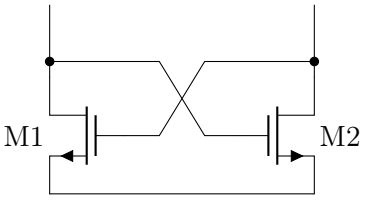

Figure 2.5: The cross-coupled NMOS pair

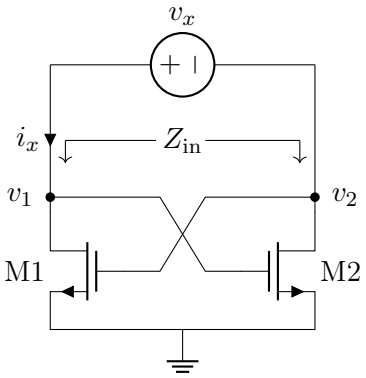

Figure 2.6: Port impedance of the cross-coupled NMOS pair

To qualitatively analyze the port impedance of the circuit, Figure 2.6 shows how that analyses would take place. The input impedance Z_{in} can be extracted from the division v_x/i_x. The small signal equivalent circuit of Figure 2.6, excluding any reactive elements, is shown in Figure 2.7.

The current i_x can be expressed due to KCL

$$i_x = g_m v_2 + \frac{v_1}{r_o}, \tag{2.5}$$

where g_m denotes the transconductance and r_{o} is the output resistance of the transistor. As can be seen in Figure 2.7, the voltage v_2 can be expressed as $-v_1$ due to the symmetry of the circuit. Considering this, v_x can be expressed as $v_x = v_1 - (-v_1) = 2v_1$. Using this leads us to an expression for $1/Z_{\text{in}}$

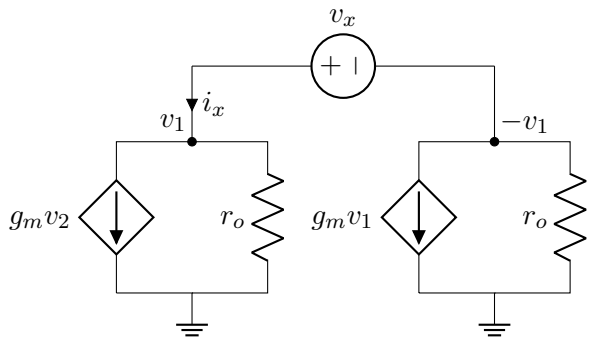

Figure 2.7: Small signal equivalent of the cross coupled NMOS pair

$$1/Z_{\text{in}} = \frac{i_x}{v_x} = \frac{v_1/r_o - g_m v_1}{2v_1} = -\frac{g_m}{2} + \frac{1}{2r_o} = -\frac{g_m}{2}(1 - \frac{1}{g_m r_o}), \tag{2.6}$$

where the denominator $g_m r_o$ is the intrinsic gain of the transistor, which can safely be assumed to be $>> 1$. This leads to further simplification of Equation 2.6

$$\frac{1}{Z_{\text{in}}} \approx -\frac{g_m}{2}(1-0) = -\frac{g_m}{2} \iff Z_{\text{in}} = -\frac{2}{g_m}. \tag{2.7}$$

This results shows that the input impedance of the cross-coupled pair can be considered a negative resistance. Furthermore, that negative resistance is determined by the transconductance g_m, which is a property that is tunable by changing the dimensions or biasing of the transistors in the cross-coupled pair. For high-frequency analysis, the capacitances of the FETs should be considered as well, and a qualitative analysis of this case will lead to an input impedance with a negative real part, together with an intrinsic capacitive element, which for the purposes of the oscillator still leads to the desired case demonstrated in Equation 2.4. The complete cross-coupled differential-pair oscillator is shown in Figure 2.8. The use of the cross-coupled transistor pair is often featured in the designs of mm-Wave oscillators [7]. The ideal passive components of the oscillator, i.e. the L and C components, are often referred to as the LC-tank, where the capacitance of the differential pair is included as a part of the tank circuit.

2.2 The voltage-controlled oscillator (VCO)

A voltage controlled oscillator (VCO) is as the name implies an oscillator which output frequency can be controlled by applying a certain voltage as input. The need for a controllable oscillator can be easily realized, and is particularly needed in transmitter and receiver circuits. A phase-locked loop is a prime example, where the phase offset converted to a voltage level is fed through a feedback loop to be used to generate a certain reference frequency. Looking at the circuit in Figure

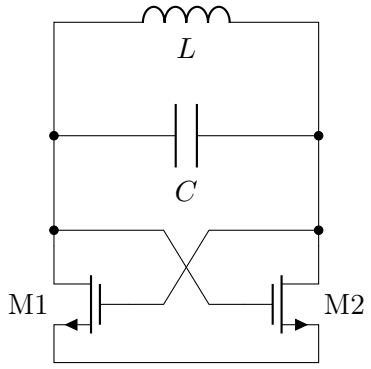

Figure 2.8: The cross-coupled differential-pair LC oscillator

2.8, the frequency generated is controlled by the L and C values of the tank (where C also includes the parasitic capacitance of the cross-coupled transistor pair)

$$f_0 = \frac{1}{2\pi}\frac{1}{\sqrt{LC}}. \tag{2.8}$$

By simply tuning either the value of L or C, the center frequency can be tuned. Usually, a typical VCO also features a few alterations to the structure in Figure 2.8. To properly bias the transistors M1 and M2 in the cross-coupled pair, the inductor is usually transformed into an equivalent circuit where two inductors with value $L/2$ are connected to a drive voltage V_{DD}. The sources of M1 and M2 are also connected to a common tail current source, which supplies a proper current into the two branches of the oscillator, effectively ensuring biasing of the transistors. Finally, to achieve capacitive tuning, the capacitance is replaced by a variable capacitance, or varactor, that can have its capacitance set by a voltage control signal. The commonly used VCO architecture, commonly referred to as the cross-coupled differential-pair LC-VCO, can be seen in Figure 2.9.

For any value of the applied control voltage V_{ctrl}, the capacitive value of the varactors, C_{tank}, combined with the parasitic capacitances of all interconnects and transistors, C_{par}, inductance value L has to be tuned as to take into account the total capacitance $C_{\text{tank}} + C_{\text{par}}$. An important quantity of the VCO is the so-called quality factor, Q. Q is a measure that is applied to any resonant circuit, in this case the LC-tank of the VCO. It can be defined as a measure of how much of the energy of each oscillation cycle is dissipated in the reactive elements compared to the resistive elements. Ideally, the quality factor is infinite, which would theoretically imply no loss in the oscillator's tank. While there are many definitions of Q, Equation 2.9 presents the most fundamental [8]

$$Q = 2\pi\frac{\text{maximum instantaneous energy stored in the network}}{\text{energy dissipated per cycle}}. \tag{2.9}$$

A way to imagine the quality factor's meaning is realizing that it can also be applied to a system that isn't necessarily an electrical resonator. A harmonic

swinging pendulum could have a Q, where the value would be higher if the friction and air resistance was lower. For our purposes however, namely a parallel LCR circuit, the quality factor can be calculated

$$Q = \frac{R}{\omega_0 L} = R\omega_0 C. \tag{2.10}$$

2.2.1 Cross-coupled differential-pair LC-VCO Operation and Considerations

Operation

Other than presenting the description of the cross-coupled pair through the one-port view as an addition of a negative resistance (as in Section 2.1.1), it's of value to go through the details of the transistors' operation. As previously described, the role of the cross-coupled pair is to add energy into the LC-tank to account for the intrinsic loss in the tank circuitry. Again, the analogy to the swinging pendulum is useful. To keep the pendulum swinging, a fan is added to each side of the pendulum, and the fans should ideally only blow on the pendulum for the duration in which the pendulum is swinging in the appropriate respective direction. The operation of the tail-biased (role of tail current source will be detailed later in the section) cross-coupled pair is such that the current I_{SS} is either all running through M1, or all running through M2, each during one half of the oscillation cycle [9]. The drain currents injected from either branch are therefore ideally, as seen in Figure 2.10, square waves.

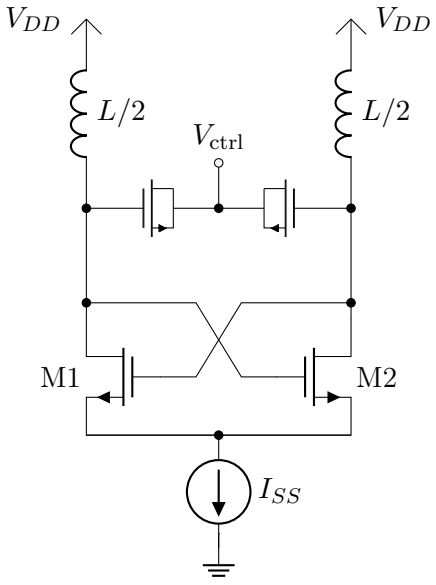

Figure 2.9: The cross-coupled differential-pair LC-VCO topology

The higher harmonics of the square wave will be attenuated by the LC-tank, while the fundamental harmonic will be dissipated in the resistive part of the tank, R (not shown in Figure 2.9, but can be seen as a resistance parallel to the varactors, or two half as large resistances $R_p = R/2$ in parallel with each inductor).

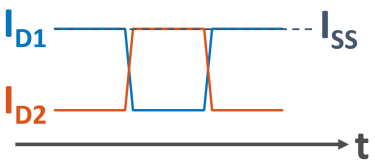

Figure 2.10: Drain currents of the cross-coupled transistors.

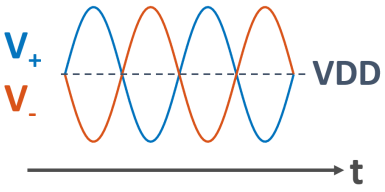

Figure 2.11: Single-ended voltage output swings.

To find the single-ended voltage swing, one must account for the fundamental harmonic of a square wave with an amplitude A. A Fourier series expansion gives the first harmonic with an amplitude of $4A/\pi$. The peak current calculated will flow through $R/2$, since that would be the resistance in parallel with one of the inductances. With $A = I_{SS}/2$, the resulting differential output peak can be calculated

$$v_{\text{diff,pk}} = \frac{4}{\pi}\frac{I_{SS}}{2}\frac{R}{2} \cdot 2 = \frac{2}{\pi} I_{SS} R. \tag{2.11}$$

The resulting single-ended voltage swings can be seen in Figure 2.11. This operation is known as the current limited regime of operation. Ultimately, when the biasing current I_{SS} is increased enough, the maximum voltage output swing $2V_{DD}$ is reached, entering the so-called voltage limited regime [10]. Furthermore, the role of the current source is important to achieve this described operation. One might consider simply grounding the sources of the cross-coupled pair, as shown in Figure 2.12.

There are a number of reasons why a tail current source is a good idea. Firstly, when considering the biasing conditions of M1 and M2, the structure in Figure 2.12 is reliant on V_{DD}, which leads to a strong dependency on unwanted factors such as temperature and threshold voltage [11]. Also, if looking at the operation of the VCO, during a full oscillation cycle the low impedance to ground topology allows for a decrease in the average Q factor of the tank during an oscillation cycle by introducing a path through one of the transistor's g_{DS} respectively for current to leak to ground when the differential voltage is increasing or decreasing. In the tail-biased solution, the Q-factor is preserved since no current can leak through the g_{DS} of either transistor during an oscillation cycle [12].

Tuning Range

The tuning range of the VCO is dependant on the characteristics of the tuning mechanism in the LC-tank. Tuning the inductance of the tank is traditionally

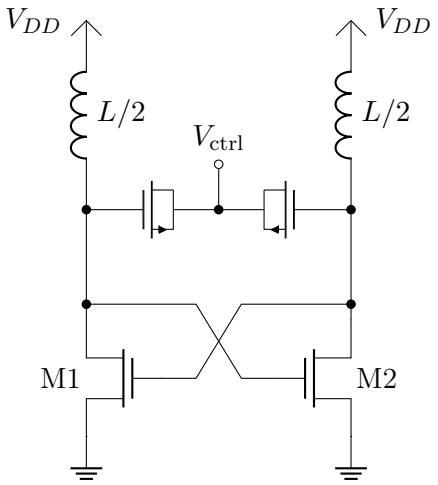

Figure 2.12: Cross-coupled VCO with low impedance to ground

difficult. The most common use is the MOS varactor, which is also in use in Figure 2.9. The MOS varactor's capacitance is dependant on the voltage across the varactor, and the capacitance range between the inputs 0 V and V_{DD} is $C_{\max}$ to $C_{\min}$. The difference $C_{\max} - C_{\min}$ determines the magnitude of the frequency tuning range. The tuning range is in turn limited by the dimensions of the MOS varactors. A larger $C_{\max} - C_{\min}$ and thereby tuning range can be achieved by increasing the channel of the varactors. However, a longer channel reduces the contribution from the overlap capacitances C_{GD} and C_{GS}, which in turn lowers the Q of the tank. There's therefore a trade-off between the overall tank Q and $C_{\max} - C_{\min}$, which translates to a trade-off between the VCO's tuning range and tank Q [11].

The wanted operation of the tuning range of a VCO is shown in Figure 2.13.

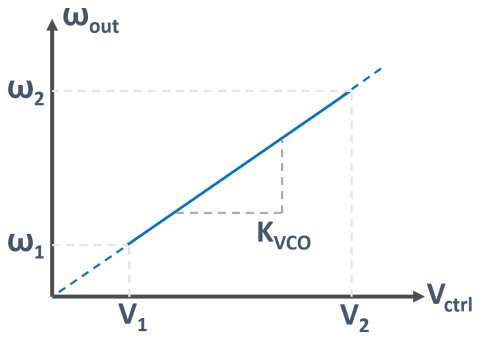

Figure 2.13: Behavoir of a VCO's tuning range.

The slope of the VCO output is denoted as K_{VCO} with a unit of rad/Hz/V. For

a certain applied v_{ctrl} between the minimum V_1 and maximum V_2, the frequency output of the VCO changes in a linear fashion between the minimum output frequency ω_1 and maximum output frequency ω_2. What this means is that the desired operation of the VCO is that K_{VCO} remains somewhat linear within the whole range of V_1 to V_2. A higher K_{VCO} would mean a larger tuning range, and lower K_{VCO} would mean a smaller tuning range.

Phase noise

The circuitry used to design analog circuits fall victim to the effects of noise. Some noise is caused by thermal activity, and some are caused by impurities as well as generation and recombination of charge carriers in a conductive channel. In the case of oscillators, many different noise sources contribute to the so-called phase noise. Phase noise can be interpreted in the time-domain as jitter. Jitter is the growing statistical uncertainty of an oscillation's zero crossings as more time passes. In the frequency domain, phase noise presents itself as other frequencies present at a certain offset to the oscillator (carrier) frequency. Ideally, the oscillator should generate a single frequency at f_0, the resonant frequency of the LC-tank, as in Figure 2.14. In practice, the oscillator output will have a noise skirt, where the noise level decreases as the offset frequency increases, as seen in Figure 2.15. The unit used to describe phase noise is dBc/Hz, at a certain offset f_{offset}. Figure 2.15 illustrates how dBc/Hz is measured. It gives the power level relative to the carrier level, measured at a 1 Hz bandwidth.

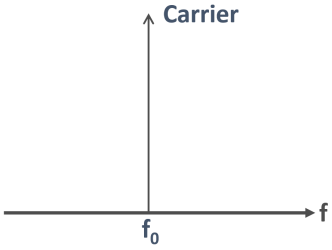

Figure 2.14: Ideal oscillator output with no noise.

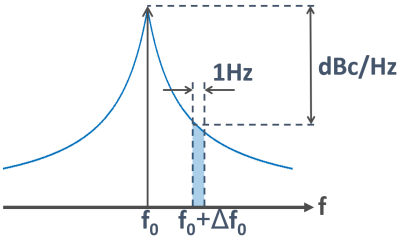

Figure 2.15: Oscillator output with noise.

In 1966, Leeson provided a theory without proof of oscillator phase noise that provides a description of different phase noise regions at different offsets from the carrier frequency [13]. Leeson's proposed model is shown in Equation 2.12,

$$\mathcal{L}(\Delta f) = 10\log\left[\frac{FkTB}{2P_{\text{sig}}}\left(1+\left(\frac{f_0}{2Q\Delta f}\right)^2\right)\left(1+\frac{\Delta f_c}{\Delta f}\right)\right], \tag{2.12}$$

where F is the active device noise factor, k is Boltzmann's constant, T is temperature in Kelvin, B is the bandwidth of the noise integration (in our case set to 1 Hz), P_{sig} is the carrier power, f_0 is the oscillation frequency in Hz, Q is the tank's loaded quality factor, Δf is the offset frequency, and Δf_c is the flicker noise corner. While Leeson's model was a heuristic model with no formal proof, later

research efforts have confirmed the theory and also provided the noise factor F [14]. A graphical representation of Leeson's model is shown in Figure 2.16.

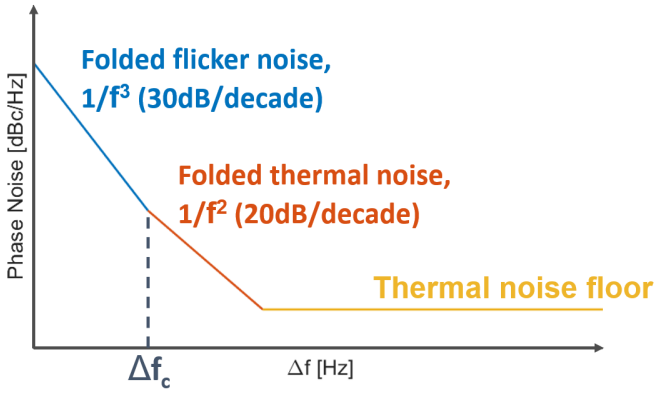

Figure 2.16: The different regions of phase noise at different offset frequencies.

Leeson's equation reveals that there's three main regions of phase noise. At smallest offsets from the carrier, the noise is dominated by folded transistor flicker noise (upconverted $1/f$ noise). At the flicker noise corner frequency Δf_c, the noise is instead dominated by folded thermal noise, with a distinct $1/f^2$ behavior. At very high offsets from the carrier, the thermal noise floor dominates. Flicker noise is present in the cross-coupled pair transistors, as well as the current source if that current source is a transistor. The upconversion of flicker noise is attributed to the cyclostationary noise modulation of the cross-coupled pair transistors. As the transistors operation varies during a period of oscillation, the net phase change, and thereby phase noise additive nature, is changed [11] [15].

Design Implications

Analyzing the resulting effects of tuning range and phase noise, it's clear that there's a design trade-off between the two parameters. Consider the VCO in Figure 2.9, and imagine that the tuning range wishes to be increased. One would then go on to alter the varactor dimensions, leading to a higher tuning range, which leads to a lower Q, and ultimately (according to Equation 2.12) a higher phase noise. Imagine instead that one wishes to improve phase noise performance. Without using alternative topologies and technologies, this would be realized by increasing the Q of the tank, and therefore lowering the tuning range. While designing the oscillator, one needs sufficient g_m to achieve proper negative resistance of the cross-coupled pair, which would ultimately increase power consumption. The trade-off between phase noise, tuning range and power consumption is present at all design phases of VCO design, and present literature introduce ways of relaxing this trade-off to achieve optimal performance metrics in all fields.

2.2.2 The digitally controlled oscillator (DCO)

The digitally controlled oscillator, or DCO, is a variant of the VCO where the input signal is applied as a digital signal of N bits. A fairly easily implemented solution is to add N varactor pairs for a digital input of N bits, where the capacitance value and therefore size of the varactors are scaled in binary fashion (i.e. widths 1, 2, 4, 8, ...). This so-called binary-weighted capacitor bank could also be implemented with regular capacitors with an enabling switch, but this kind of structure would be difficult to implement in mm-wave frequencies due to the added parasitics. The binary input signal is to be applied to the varactor bank, with the least significant bit on the smallest varactor and most significant bit on the largest varactor. A capacitance bank of this type is illustrated in Figure 2.17.

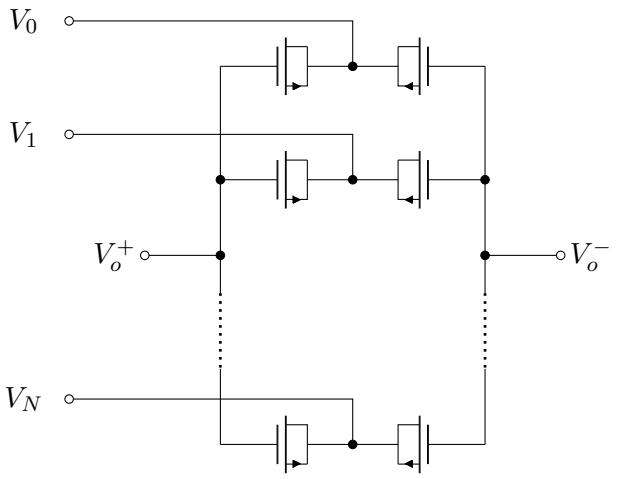

Figure 2.17: Common digital capacitance bank architecture, where the input is a digital signal of N bits.

Ideally, the sizes of the varactors are tuned such that equal step size is achieved, i.e. the input range 0 to $2^N - 1$ yields a linear frequency output. The relatively simple solution of using a bank of capacitances or varactors do fall victim to unwanted effects at high frequencies. At mm-wave frequencies, the parasitic capacitances of the surrounding circuitry can risk being in the same range as the tuning capacitances, which obviously presents an issue to the designer, as the frequency selection becomes inhibited. Another solution to the use of MOS varactors is a switched capacitance bank, but adding switch circuitry and fixed capacitances also falls victim to the parasitic effects [10].

Chapter 3
Method

3.1 Workflow and Initial Strategy

3.1.1 General Approach

The strategy used to complete this project was one that was adapted to the skills of the student as well as needs of Acconeer. The starting point of the project was an existing solution with certain requirements, and a wish to optimize this design. In projects which has received input from different designers throughout a significant period of time (so-called legacy projects), it's not uncommon for the current designers to lack certain insights about the current solution. A visual diagram representing the strategy is shown in Figure 3.1.

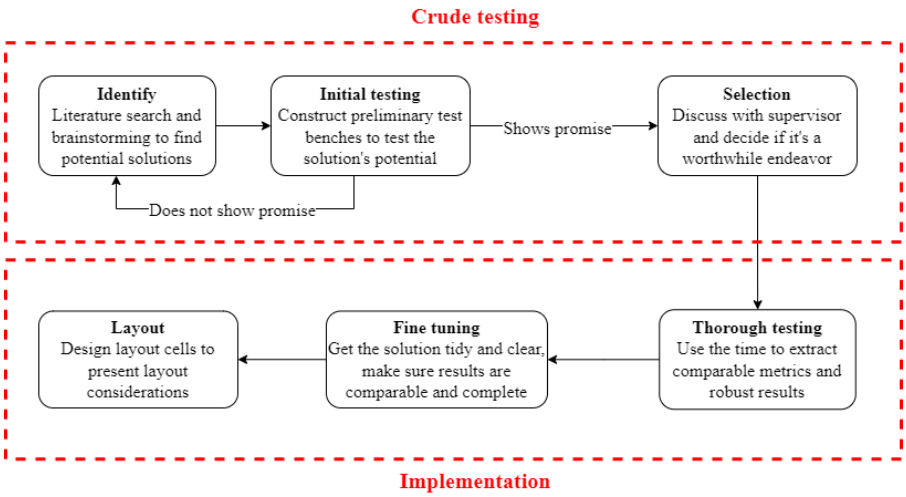

Figure 3.1: Visual representation of the strategic approach of the project.

What characterizes this strategy is that the goal is not to find the one perfect solution. Although such a result would be welcome, the goal was rather to investigate several alternatives and present their opportunities and challenges, ul-

timately leading to insights about the current solution and new solutions to see if any change would be worthwhile.

3.1.2 Oscillator design flow

A specific set of steps that ensured optimal design of the oscillators were not in place. This would have been difficult to achieve, as several different topologies that require different considerations were designed. The designs of the oscillators were achieved through an iterative process, where the knowledge of theory (especially theory regarding design trade-offs as described in Section 2.2.1) was leveraged to reduce the amount of iterative steps needed to obtain a design of satisfactory performance. As mentioned in Section 3.1.1, the goal was not to find the one perfect solution, but rather a multitude of possible alternatives to the current solution. This affected the design flow in that when oscillation was obtained and the acquired metrics were within a ball-park of what was desired, the design was deemed as finished. Practically, the dimensions of the varactor bank was to remain static. Therefore, the design flow was limited to the remaining parts of the circuit, namely amount of bias current, amount of g_m from the cross-coupled pair(s) and inductance value of the tank.

3.2 Tools and Resources

The main tool that was used to design and simulate the solutions was Cadence Virtuoso. The necessary CAD environment was provided by Acconeer. The ADE Explorer view, which is integrated with the Spectre Simulation Platform, was used to run the schematic simulations to get most metrics presented in this work. For the layout work, the Layout XL suite was used. The parasitic extraction was made using Calibre PEX as well as Keysight's Momentum. Other than the EDA tool Cadence Virtuoso, Acconeer also provided the a technology library of a 40 nm CMOS node, which included mm-wave component models of sufficient maturity. Other than these tools, Acconeer also provided office space, computer, computer mouse and mentoring.

3.3 Circuit Simulations

Using the EDA tool Cadence Virtuoso, several different types of circuit simulations can be analyzed to retrieve performance metrics of the investigated oscillator topology.

3.3.1 Simulation setup

The simulation setup used is presented in Figure 3.2. The VCO element is an abstraction that basically represent all elements within the VCO, including LC-tank, cross-coupled pair, biasing, depending on the different topologies.

The simulation setup was altered some depending on the simulation that was to be run and solution that was tested. Different solutions required different start-up

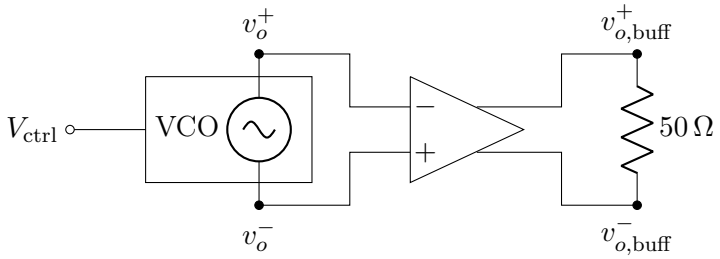

Figure 3.2: The simulation setup used for the results presented in this section.

conditions. For the solutions which do not feature a specific start-up mechanism, and for harmonic balance analysis which requires static conditions, a 5 mV offset was set on one of the gates of the cross-coupled pair transistors.

A simple buffer represented in Figure 3.3 was used for all designs. The buffer design consists of a common-source amplifier on each differential output. The load used was a 50 Ω resistive load, and an attempt to match the output to the load was made for the reference design using inductors to V_{DD}.

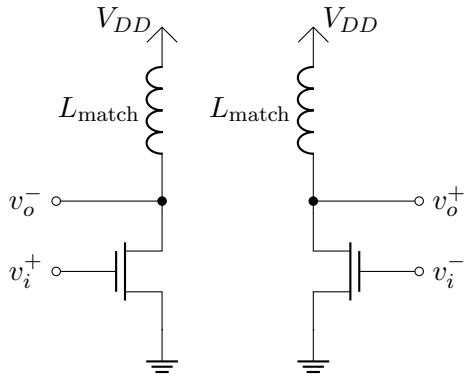

Figure 3.3: The buffer design used for the tested solutions.

Passive tank components

The choice of passive elements of the LC-tank remain constant throughout all tested solutions of this work. The inductor used was a mm-wave model of a slow-wave co-planar wave-guide (SW-CPWG), illustrated in Figure 3.4.

The SW-CPWG features two ground planes and one signal line at a higher thick metal layer to alleviate the effects of parasitic resistive elements. The orange and yellow structure below represents floating metal lines running perpendicular to the signal and ground lines, acting as shielding (not connected to AC ground).

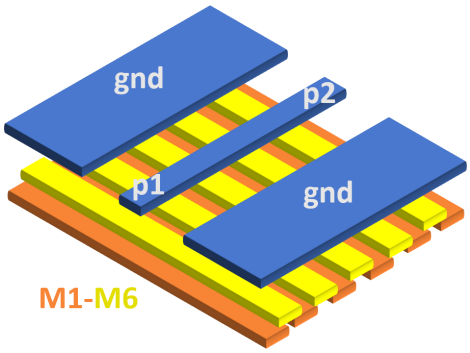

Figure 3.4: Illustration of the SW-CPWG used as tank inductors.

The illustration does not exactly represent the structure, but shows the principle. One of the oscillator nodes would be coupled to p1 or p2, and V_{DD} connected to the other node. The length of the inductors was scaled for the different solutions as a way to tune the inductances, and thereby acquire the wanted oscillation frequency. The capacitive element of the LC-tank was a set of ten mm-wave models of binary-weighted thick oxide Ncap varactors. These varactors were then coupled in pairs, and connected as seen in Figure 2.17. An illustration of the varactor can be seen in Figure 3.5.

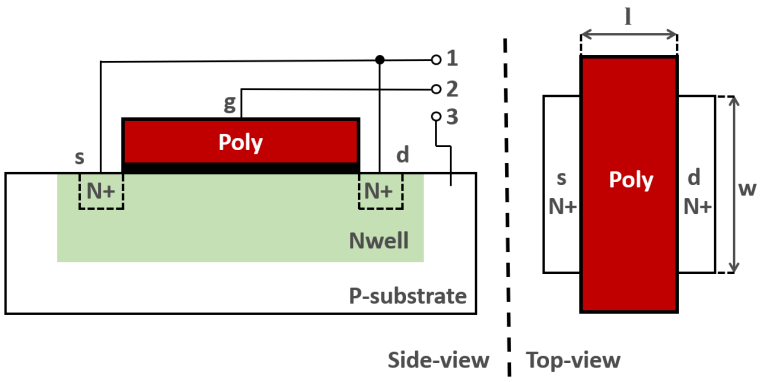

Figure 3.5: Illustration of the mm-wave Ncap varactor.

The numbers 1, 2 and 3 represent the different ports of the varactor. The port 1 was connected to V_{DD}, port 2 was connected to an oscillator node, and port 3 connected to ground. The capacitance value is realized by tuning the dimensions l and w. The width is scaled by introducing N_k amount of fingers where $N_k = 2^k$, and $k = [0, 3]$. This scaling is meant to provide the binary-weighted nature of the varactor bank. The dimensions of the varactor bank was kept constant for all investigated solutions.

3.3.2 Transient analysis

A transient analysis (`tran`) runs the circuit through a time-domain simulation, considering any initial conditions and then simulating how the circuit would act through the course of time. The transient analysis uses a stop time given in seconds as its main parameter, and gives the observer insights into the time-varying transients of the investigated circuit. For the purposes of this work, the transient analysis was used to derive several metrics from different investigated oscillator topologies. These metrics are detailed in Table 3.1.

Metric	Unit
t_s	s
t_d	s
P_{dc}	W

Table 3.1: The different oscillator metrics derived from transient analysis, including their units.

The start-up time, t_s, was measured at the 10-90% rising edges of the signal envelope. The trigger delay, t_d, was measured as the time between $t = 0$, which was also when the trigger pulse was applied, and 90% of the signal envelope's rising edge. The dynamic power consumption, P_{dc}, was measured for the core, buffer as well as the total consumption. Additionally, the transient analysis also allowed for investigation of the oscillator output waveform. The output voltage swing could thereby be determined, and operation of the oscillator evaluated.

While not being traditionally incorporated in oscillator benchmarking, the start-up time is of high importance for Acconeer's applications. A conventional oscillator design usually does not warrant the need for a fast start-up. However, in the case of pulse-coherent radars, the start-up time's importance becomes apparent.

Transient Noise (Jitter)

The jitter of the oscillation, σ_{jitter}, serve as a complement to the analysis of the noise performance of the different oscillator solutions. A transient noise analysis is a regular transient analysis but with added device noise, such as flicker noise and thermal noise. In order to measure σ_{jitter} of the oscillator in the time domain, this noise has to be incorporated. Figure 3.6 illustrates the extraction of σ_{jitter}.

Figure 3.6 represents the measurement of a tail-biased VCO, and the green plot represents the biasing applied to thereby provide current and start the oscillator. In this work, different start-up mechanisms have been discussed, and these start-ups would also be applied at the same time as the biasing voltage. The quantity $t_{\mathrm{N,jitter}}$ represents the delay which at the presence of jitter would be measured to be slightly different each measurement. The time delay is extracted by measuring the time between the start-up pulse rising edge and a certain rising zero crossing after N periods. The simulation works by repeating start-up and shutdown of the oscillation repeatedly, and measuring $t_{\mathrm{N,jitter}}$ for each iteration. The collected

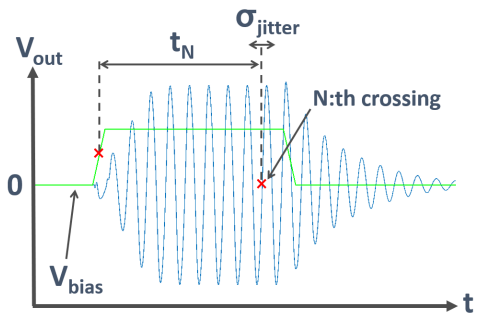

Figure 3.6: Visual demonstration of the time delay used to measure σ_{jitter}.

delays of a certain number of oscillations are then collected into a histogram, where the distribution's standard deviation can be calculated, i.e. σ_{jitter}. For all simulations, the value for N that was used was $N = 50$. Additionally, to properly simulate a realistic start-up and shutdown, the rise and fall times of all rising and falling edges of start-up and bias voltages were 10 ps.

The transient noise simulation can also be used to investigate the phase coherency of the oscillation. The jitter simulation described in this section will confirm that the used start-up mechanism consequently does not start the oscillator in anti-phase. If that would be the case, then the attained jitter values would be strongly deteriorated, since the obtained jitter is in the order of fs, which is an order of magnitude smaller than the signal period, having ps values. However, a test that evaluates the statistical deviation of the signal phase in the time-domain has not been included in the scope of this work.

3.3.3 S-parameter analysis

When analyzing high frequency circuits, the two-port network representation is highly useful. Figure 3.7 shows the representation with incident and reflected power waves, a_k and b_k.

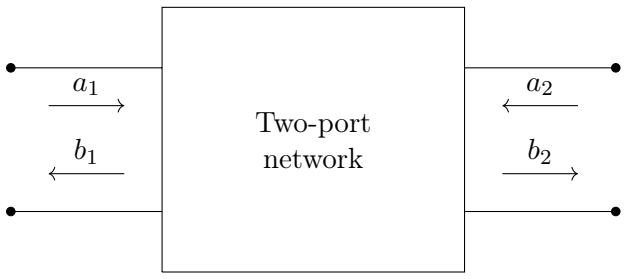

Figure 3.7: Two-port parameter representation.

The two-port network itself is simply an added level of abstraction, and can

contain any circuit that connects the outside ports. This effectively turns the two-port representation into a useful starting point of analysis, since it presents a way to investigate impedance at any arbitrary node along any circuit. This way, you can effectively use a one-port representation and for instance check for the impedance seen between the nodes in Figure 3.9.

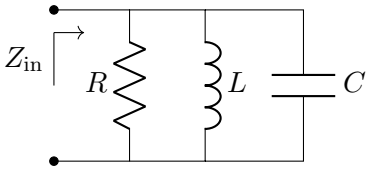

Figure 3.8: An arbitrary circuit impedance.

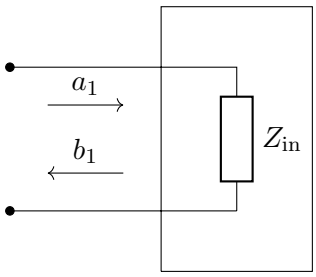

Figure 3.9: One-port parameter representation.

This technique was used extensively during the design of the oscillator, since looking into two nodes and seeing the impedance (most cases translated to capacitance at a certain frequency) is needed when balancing the LC-tank and cross-coupled pair, for instance.

3.3.4 Harmonic Balance

The harmonic balance analysis (`hb`) is a analytic method to find steady-state solution to nonlinear systems in the frequency domain. The simulation process uses an iterative approach that does not stop until a solution with an error within a set tolerance is reached [16]. Harmonic balance is well suited for analysis of oscillators and their nonlinear components. In order to simulate the noise performance of the oscillator, a derivation of the harmonic balance analysis (`hbnoise`) was used. The `hbnoise` analysis was configured to run a Lorentzian analysis. For the purposes of this work, the harmonic balance analysis was used to derive several metrics from different investigated oscillator topologies. These metrics are detailed in Table 3.2.

Metric	Unit
f_0	Hz
Tuning range	Hz or %
Phase Noise at Δf	dBc/Hz
Output Power	dB

Table 3.2: The different oscillator metrics derived from harmonic balance analysis, including their units.

The phase noise (PN) was measured at offsets 100 kHz, 1 MHz and 10 MHz. The output power was measured by extracting the output power spectrum across

the load at the buffer output.

3.4 Limitations and Scope

Given the scope and time allocated for this work, a few restrictions to the investigated solutions was set early in the investigative crude testing phase. Firstly, the LC-tank design was to be subject to small changes, i.e. the components used was not to be altered in any significant way in order to ensure that the solutions presented were actually tangible options for Acconeer to consider, and that the results of different solutions would be comparable. Secondly, the alterations to the current solution to be tested should be in the domain of the cross-coupled differential-pair oscillator and its neighbouring solutions. In other words, solutions such as the three-point oscillators (most notably Colpitts) won't be considered, although being elegant solution alternatives.

Furthermore, the tests involved in the schematic simulation during the testing phases will focus on extracting the basic metrics for the solutions, and no corner analysis or Monte-Carlo simulations will be made. Since the purpose of the work is more focused on bringing potential solution improvements to Acconeer, these simulations, although important, will have to be left for Acconeer to consider. Also, no fabrication of the solutions will be made, since this basically would be part of the scope of a larger project. The insights gained for Acconeer from robust performance metrics will be sufficient to creating the value intended.

3.4.1 Peripheral circuitry

The focus of this work lies mainly in optimizations in the core of the oscillator, and elements therein, such as the cross-coupled pair or the biasing circuitry. The output stages of the oscillator, mainly the buffer and the load, are needed to get a reasonable context for the output power and noise analyses, so a simple buffer design was implemented. The value for L_{match} and dimensions of the transistors was swept while looking at the output waveform of the oscillator until satisfactory and reasonable results were met. Although not an ideal matching procedure, since the focus of the work was not on peripheral circuitry this analysis was sufficient.

For all following analyses incorporating the buffer and the load, the buffer parameters such as transistor width was swept to ensure that none of the retrieved metrics were significantly affected by poor design of the peripherals. Also, at the event of unexpected results, the biasing of the buffer was checked by rerunning with a couple of bypass capacitors on the input.

Chapter 4
Results and Discussion

4.1 Literature review and solution selection

As detailed under Section 3.1.1, this work's strategy aimed to single out promising solutions for Acconeer to potentially pursue. The section details the selected solutions, and presents the reasoning behind investigating said solution. The tank elements in the schematic figures of this section represents the components described in Section 3.3.1.

4.1.1 Common tail (CT)

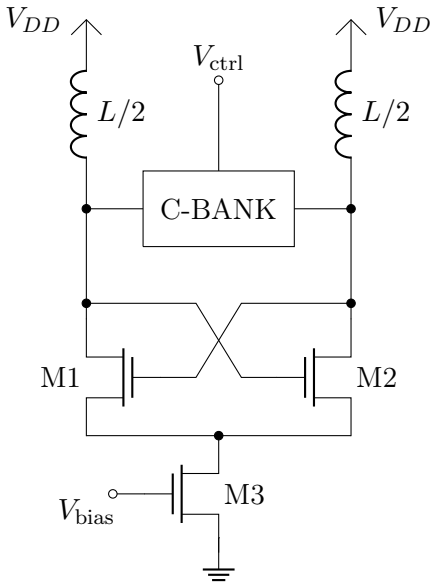

Figure 4.1: Cross-coupled DCO with tail bias transistor.

As described in Section 2.2, the tail-biased cross-coupled differential-pair LC-VCO is a common alternative for mm-wave harmonic oscillators. The common

tail solution is an attempt to realize this common VCO structure as a DCO, to set a foundation for other solutions that depend on a tail-bias transistor. Additionally, this solution will act as a reference point when presenting the results of the remaining solutions. The physical realization of the current source is commonly a transistor with appropriate bias voltage applied to the gate [9], and this is the implementation of the current source that was implemented in the common tail solution, as seen in Figure 4.1

The tail biased DCO does present limitations for our purposes. With a fully symmetric circuit, control of the start-up time and phase is difficult to realize. Although these problems would be detrimental for Acconeer's purposes, there's interest in looking into this solution since many other solutions in literature use this topology as a starting point. Therefore, it acts as a good reference point for comparison with other solutions. All in all, investigating this solution can lead to a significantly larger potential of exploring new improvements to the topology.

4.1.2 Common tail, current injection (CTCI)

Using the DCO for pulsed coherent radar introduces the need for a start-up mechanism that can effectively set the outgoing phase and fast start-up of the oscillator. Acconeer's current solution satisfies these requirements, but if any of the tail-biased topology options are to be considered, a robust start-up mechanism for these solutions would need to be considered. Therefore, a current injection solution was developed, similar to an injection technique demonstrated in 45 nm CMOS SOI [17].

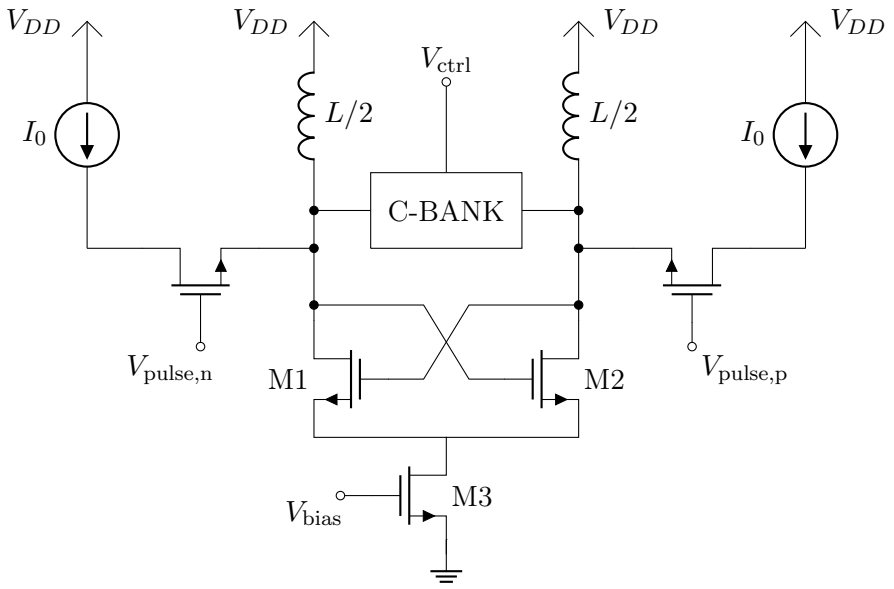

Figure 4.2: Schematic of the common tail current injection solution.

This solution was developed as an attempt to see if this novel start-up mechanism could for the specific technology, and with the basic topology that was selected, provide a robust start-up.

A schematic showing the idea can be seen in Figure 4.2. The start-up mechanism can be characterized by inspection of the branches leading into the outputs of the oscillator. Ignoring the implementation of the current source and origin of the pulses, the idea is that an initial current injected into one of the branches, while the other branch remains untouched. This injection locking technique should provide a significant amount of current in inductors to kick-start the process described in Section 2.1.1. However, instead of a voltage V_0 applied across the tank terminals, we apply a current I_0, basically starting of at step 2 instead of 1 in the enumerated list in Section 2.1.1. A deeper analysis of optimal values of current magnitude, pulse shape and pulse width will be reserved for future research. As for this work, an ideal square wave voltage pulse of magnitude V_{DD} and rise and fall times of 1 ps will be applied, and the width of that pulse w_{pulse} as well as magnitude of I_0 was determined empirically by sweeping the values and selecting the optimal start-up times. The optimal values found after empirical investigation was an injected current of $I_0 = 8\,\text{mA}$ and a pulse width of $w_{\text{pulse}} = 20\,\text{ps}$. Interestingly, the trigger delay as a function of w_{pulse} was found to have local maxima at multiples of the oscillation period T_0, as seen in Figure 4.3. This indicates that values of $w_{\text{pulse}} = nT_0$ should be avoided. The start-up time showed a similar behavior.

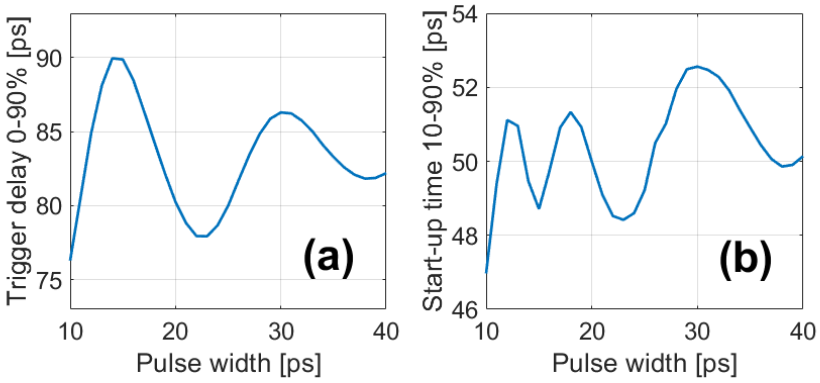

Figure 4.3: Plots showing (a) the trigger delay and (b) the start-up time for different injected current pulse widths.

4.1.3 Common tail, current injection with tail filter (FILT)

This solution is based on the principle developed by Abidi, Hegazi and Sjöland [12]. The tail current source transistor contributes to a worsened noise performance through its' intrinsic flicker noise. This phase noise is characterized as noise at $2\omega_0$, and it was therefore theorized and proven that providing a high tail impedance at this frequency will prevent the differential pair from loading the LC-tank with

induced noise from the tail transistor, thereby lowering the phase noise. This so-called tail filter would consist of two fundamental elements.

1. An inductor placed between the common tail node of the cross-coupled pair and the tail transistor will provide a high impedance at $2\omega_0$. By identifying whatever capacitance is present at the common tail node, the inductor is designed to resonate with this capacitance at $2\omega_0$
2. A capacitor placed across the tail-bias transistor will remove noise at $2\omega_0$ by providing a low impedance to ground, as well as providing signal ground to the filter inductor

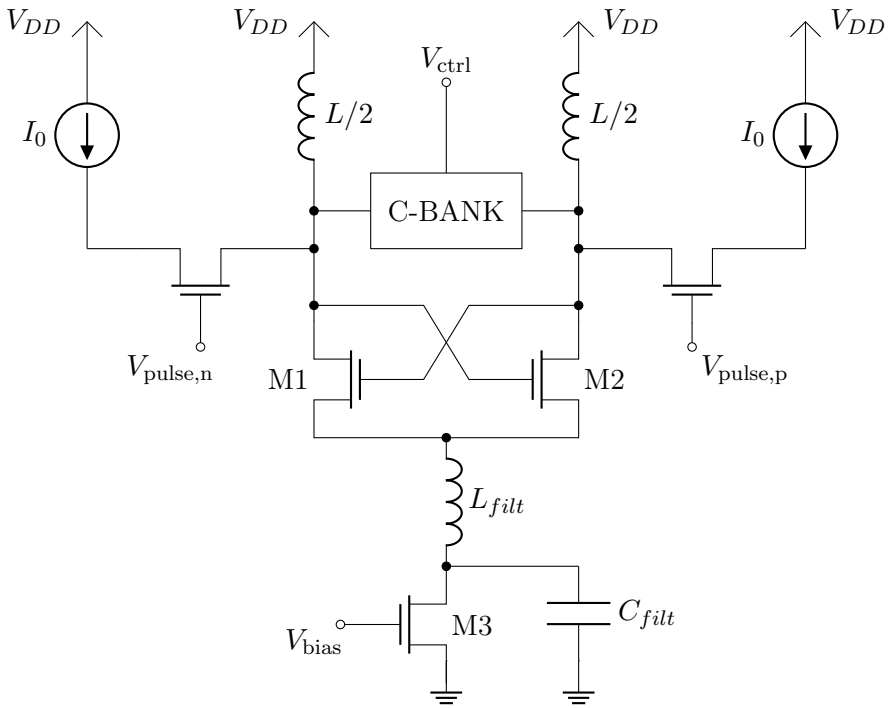

Figure 4.4: Schematic of the common tail, current injection with tail filter solution.

Although the filtering technique is tested at a few GHz in [12], it has been shown in that the principle should provide significant phase noise improvement in mm-wave frequencies as well [18]. Since Acconeer's purposes warrants a oscillator start-up that's both fast and controllable in phase, the tail filter solution is applied to the solution CTCI described in Section 4.1.2 above. A schematic featuring a cross-coupled DCO with the tail noise filter and current injection branches is shown in Figure 4.4.

To find the values of L_{filt} and C_{filt}, the oscillator was first designed and balanced without the noise filter (in fact, the design from Section 4.1.2 was used).

Then the impedance at the common tail node was investigated to see what parasitic capacitance existed at that node. By adding a port to that node to ground and using S-parameter analysis (as described in Section 3.3.3), the reactance X_C at $2\omega_0$ and thereby capacitance could be found

$$X_{C,2\omega_0} = -\frac{1}{2\omega_0 C_{par}} \iff C_{par} = -\frac{1}{2\omega_0 X_C}. \tag{4.1}$$

The value for L_{filt} was then calculated to resonate with C_{par} at $2\omega_0$ by using Equation 2.8, i.e. $L_{filt} = 1/4\omega_0^2 C_{par}$. C_{filt} is in turn designed to provide low impedance at $2\omega_0$, which is most easily achieved empirically. The value for C_{filt} was therefore swept, to find that capacitors larger than 200 fF tended to provide a small increase in performance. The final values were calculated to $L_{filt} = 12\,\text{pH}$ and $C_{filt} = 530\,\text{fF}$. A larger value of the filter capacitance increased the filter performance, however not significantly. An implementable size was therefore chosen. These value were later confirmed practically by sweeping the values to see any performance changes. As was detailed in Section 4.1.2, the values used for I_0 and w_{pulse} was investigated and found to have similar relation as in Figure 4.3 even with a tail noise filter. The used value for the injected current was therefore chosen as $I_0 = 8\,\text{mA}$ and $w_{\text{pulse}} = 10\,\text{ps}$ for the pulse width. Lastly, the components used to implement the filter was mm-wave models of an inductor and a capacitor. The inductor was a symmetric two-port inductor with an octagonal shape, single turn, inner core diameter of 15 µm, and track width of 5.5 µm. The capacitor used was an alternative polarity MoM capacitor with a width and length of 12 µm.

4.1.4 PMOS cross-coupled pair (PMOS)

As discussed in Section 2.2.1, flicker noise in the transistors of the cross-coupled pair is one of the main sources of noise at close offsets to the generated oscillation output. Amount of flicker noise is an intrinsic trait of transistor's, dependant on factors such as impurities and carrier mobility of the channel. In an effort to reduce the intrinsic flicker noise of the transistors, which ultimately results in worsened phase noise performance, PMOS transistors can be used instead of NMOS transistors [11]. PMOS transistors famously feature a lower level of flicker noise, which makes for a good prerequisite for a low phase noise oscillator. The topology tested is a bottom biased PMOS cross-coupled differential-pair LC-DCO, as shown in Figure 4.5.

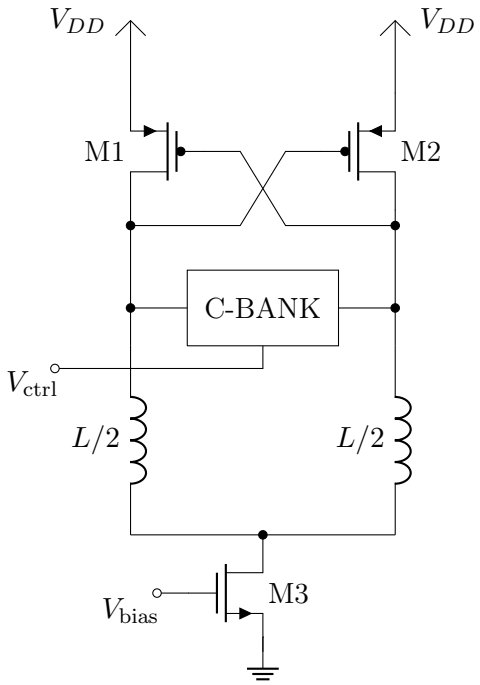

Figure 4.5: Schematic of the PMOS solution.

4.1.5 Double switching pair (DBL)

One of the components in the oscillator design trade-off is power consumption. Acconeer's applications warrants the use of low-power consuming circuits, and it's therefore of interest to explore solutions that might provide lower power consumption. A topology that can be used for this purpose is the double switching pair cross-coupled LC-VCO [9]. The topology is characterized by an additional PMOS cross-coupled pair applied to the oscillator nodes, together with an NMOS cross-coupled pair, as shown in Figure 4.6.

The double switching pair can be shown to give low-power performance in mm-wave frequencies [19]. As described in Section 2.1.1 and the one-port representation of the LC-oscillator, the role of the cross-coupled pair is to introduce $-R$, or equivalently add energy, to compensate for the LC resonator pair's resistive loss. The principle of the double switching pair solution works by introducing additional negative resistance with the PMOS cross coupled pair. The transconductances of the MOSFETs are the parameters contributing to the $-R$ element, and this method effectively introduces the possibility to increase the transconductance without increasing biasing current, and thereby power consumption. Basically, the current is re-used in the PMOS transistors.

The addition of a cross-coupled PMOS pair does not come without changed conditions. The added cross-coupled pair does add flicker noise, as well as additional parasitic capacitance that governs the need to tune LC-tank properties.

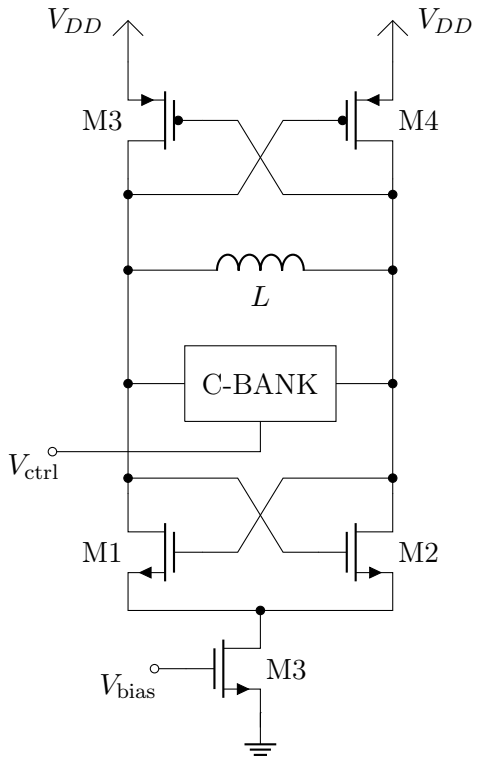

Figure 4.6: Schematic of the double switching pair solution.

Since the varactor bank is fixed, the desired oscillation frequency was attained by tuning the inductance of the tank. Also, the operation described in Section 2.2.1 is changed. Since the PMOS transistors short the path to V_{DD} during half of each oscillation cycle, the single ended output swings V_+ and V_- in Figure 2.11 are limited to V_{DD}. Effectively, this results in the waveforms of Figure 2.11 being clipped at V_{DD}, ultimately resulting in an output voltage swing between 0 and V_{DD} at the maximum, and not $2V_{DD}$ as with the operation described in Section 2.2.1. To account for this, a supply voltage of 1.5 V was used for the DBL solution's schematic simulations, as opposed to 1.2 V for the remaining solutions.

4.2 Schematic Simulation Results

This section features a presentation of the results pre- and post-layout, discussion of the results' origins as well as a benchmarking with DCO solutions in literature. All solutions' metrics were derived using harmonic balance and transient simulations, in accordance with Table 3.1 and 3.2. Furthermore, the oscillation frequencies f_0 presented in this section are all in the range of 63-64 GHz, but the goal frequency was 60 GHz. This is because a certain amount of parasitics from the interconnects between components were anticipated.

4.2.1 Tuning range

The tuning ranges were attained by running a `hb` analysis while sweeping the frequency control input between 0 and 31. The frequency control was in turn the input of a decimal to binary instance, which converts the signal to a 5-bit bus with values either 0 or logic high, with logic high set to the same level as V_{DD}. Plots showing the output oscillation frequency at applied digital input 00000 (code 0) to 11111 (code 31) can be seen in Figure 4.7.

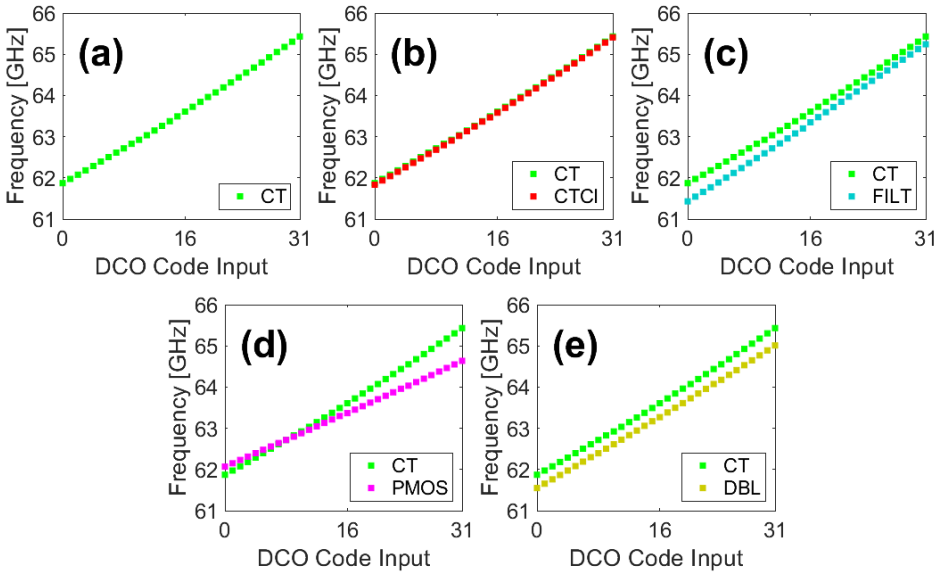

Figure 4.7: Tuning ranges presented for (a) the CT solution, (b) the CTCI and CT solutions, (c) the FILT and CT solutions, (d) the PMOS and CT solutions, and (e) the DBL and CT solutions.

Figure 4.7a shows the tuning range of the CT solution as reference. The remaining Figures 4.7b-e contain the tuning ranges of the investigated solutions, with the CT solution included as well. Table 4.1 shows the tuning range performance of the different solutions.

Solution	f_0 [GHz]	FTR [GHz]	FTR [%]	Resolution [MHz]
CT	63.61	3.56	5.6	111
CTCI	63.53	3.58	5.6	112
FILT	63.35	3.86	6.0	121
PMOS	63.37	2.57	4.1	80
DBL	63.27	3.46	5.5	108

Table 4.1: The resulting tuning range results from schematic simulations of the solutions.

Other than the FILT solution and the PMOS solution, the tuning range remain relatively equal to that of the CT solution. All solutions showed a linear behavior, i.e. a significantly constant K_{VCO}. The dimensions of the varactors in the bank was kept constant in all cases. The PMOS solution performed worst, featuring a lower K_{VCO} as can be seen in Figure 4.7d. For the PMOS performance, the added capacitance from the PMOS cross-coupled pair resulted in the tank transmission lines having to be scaled down to shorter lengths relative to all other solutions. This increase in constant parasitic capacitance relative to the tank inductance in turn reduced the effect of $C_{\max} - C_{\min}$ for the varactor bank, leading to a smaller tuning range. This effect would seem to affect the DBL solution, since this solution also features a PMOS cross-coupled pair (in addition to an NMOS pair). However, the DBL solution also featured a need for smaller current biasing, leading to a reduction in parasitic capacitance from biasing source. The other difference that distinguished the DBL solution was that the inductance was placed between the two oscillator nodes, and not split in half and connected to the tail biasing as in the PMOS solution. The characteristics of the transmission line might have played a role in affecting the tuning range here as well. The FILT solution performed best, featuring a slightly higher K_{VCO} as can be seen in Figure 4.7d. Since it is identical to the CTCI solution other than the added noise filter, this improvement must be attributed to the added filter. The filter effectively removes parasitic capacitance at the common source node of the cross-coupled pair, which have lead to an increase in the effect of $C_{\max} - C_{\min}$ of the varactor bank.

4.2.2 Phase noise and jitter

The phase noise plots attained through `hbnoise` analysis as described in Section 3.3.4 is shown in Figure 4.8. First, the attained phase noise plot for the CT solution is shown in Figure 4.8a. The remaining four plots shown in Figure 4.8b-e contain each of the investigated solutions with the CT solution included as well for comparative purposes.

As mentioned in Section 3.3.4, the Lorentzian `hbnoise` analysis was used to derive the plots in Figure 4.8. This analysis gives rise to the plateau at low offset frequencies and corresponding corner frequency where the noise plot starts decreasing towards higher offsets. The reason for this analysis artifact is that if the simulator would plot the given noise plot towards lower and lower offsets, the slope

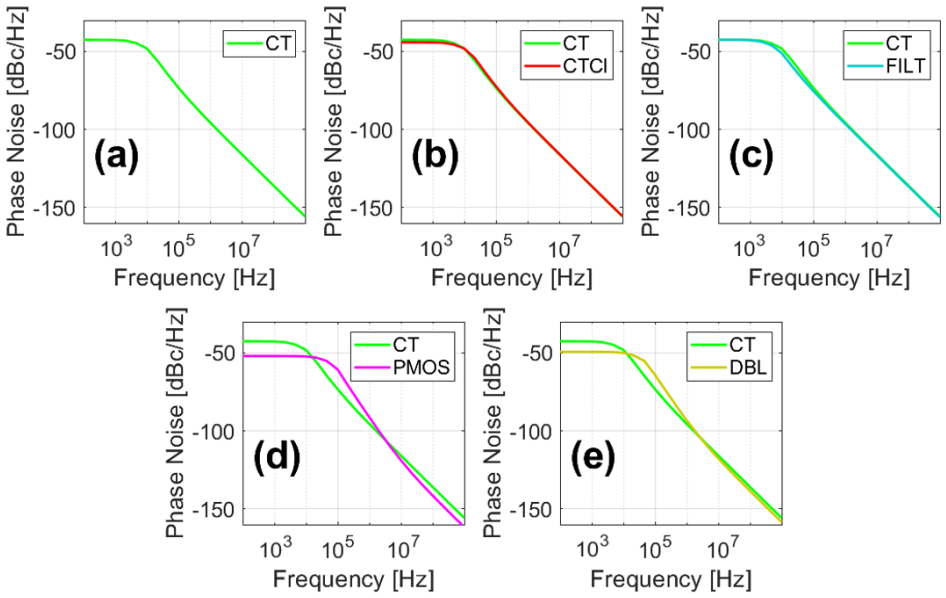

Figure 4.8: Phase noise at different offset frequencies for (a) the CT solution, (b) the CTCI and CT solutions, (c) the FILT and CT solutions, (d) the PMOS and CT solutions, and (e) the DBL and CT solutions.

would result in positive values for the phase noise which is unphysical (noise power relative to the carrier cannot be higher than the carrier). The area beneath the phase noise curve is an indicator towards the resulting jitter in the time-domain. The corresponding values for the jitter and phase noise at offsets 100 kHz, 1 MHz and 10 MHz are presented in Table 4.2.

The solutions CT, CTCI and FILT compared comparatively equal as seen in Figures 4.8b-c. CTCI showed slightly worse performance compared to CT. This could be attributed to added parasitic capacitance of the CTCI solution. Adding the noise filter was an attempt at increasing noise performance to potentially outperform the CT solution. It did work to some extent, increasing performance of about 3.1 dB at 100 kHz, 1 dB at 1 MHz, and 0.7 dB at 10 MHz compared to CTCI. However, the comparison made by [18] at 60 GHz showed an empirical improvement of 5 to 12 dB. Although their results were presented for a VCO at a different technology node and not a DCO, the proposed performance enhancement of the filter solution is partly hidden behind the slightly increase in tuning range. The increased tuning range presents the opportunity to slightly decrease the varactor lengths to get a comparable K_{VCO} and thereby tuning range as the CT solution, but ultimately resulting in higher tank Q and better noise performance. Furthermore, not reaching the empirically shown improvements can also be attributed to poor filter design or filter component choice. A different choice of filter inductor with higher Q could prove to serve the purposes of the filter better. The used

Solution	PN @ 100 kHz [dBc/Hz]	PN @ 1 MHz [dBc/Hz]	PN @ 10 MHz [dBc/Hz]	σ_{jitter} [fs]
CT	-73.2	-95.5	-115.8	NA[1]
CTCI	-72.2	-95.2	-115.7	97.4
FILT	-75.3	-96.2	-116.4	61.9
PMOS	-60.5	-92.5	-119.7	NA[1]
DBL	-64.1	-93.1	-117.6	NA[1]

[1] No jitter value for this solution.

Table 4.2: The resulting phase noise and jitter results from schematic simulations of the solutions.

technique of measuring the Z-parameters at the common tail node to derive the capacitance present at the node could also be flawed, and this value could have been confirmed by coming to the same conclusion analytically through adding the parasitic capacitances of the different elements in the oscillator.

The PMOS and DBL solutions showed worse performance in lower frequencies, but comparable and even promising performance at 10 MHz offset. The deteriorated performance at lower frequencies could be attributed to poor oscillator design, but the method of analysis can also be questioned. The results are difficult to properly analyze when comparing to the presented theory in Chapter 2, due to the previously mentioned effect of the Lorentzian analysis. In all solutions, the simulation could have been compared to an equivalent periodic steady state simulation. The preferred way, of course, would be to manufacture each solution and compare the performance through actual measurement, but this was outside the scope of this work.

As for the jitter results, the CT, PMOS and DBL solutions did not use a specific start-up mechanism other than added circuit asymmetries, and the controlled start-up and shutdown of the oscillators that is required in the method described in Section 3.3.2 were not available. Therefore, the jitter results were not attainable for these solutions, hence the NA values in Table 4.2. The analysis of jitter vales were therefore limited to CTCI versus FILT. The addition of a noise filter evidently improves the value of the jitter at the selected 50:th crossing.

4.2.3 Output waveforms

The output waveforms from each solution is presented in Figure 4.9. Each output waveform has their corresponding buffer output overlayed in a slightly darker color.

All solutions presented a sinusoidal behavior. The oscillators are all in the voltage limited regime, as can be seen by the peak voltage being approximately $2V_{DD}$ (only V_{DD} for DBL). The solutions were simulated with a few different start-up mechanisms. CT, PMOS and DBL are all symmetrical oscillators that do not feature a specific start-up mechanism, and were thereby started using a 5 mV offset on one of the gates of the cross-coupled pair. CTCI and FILT used

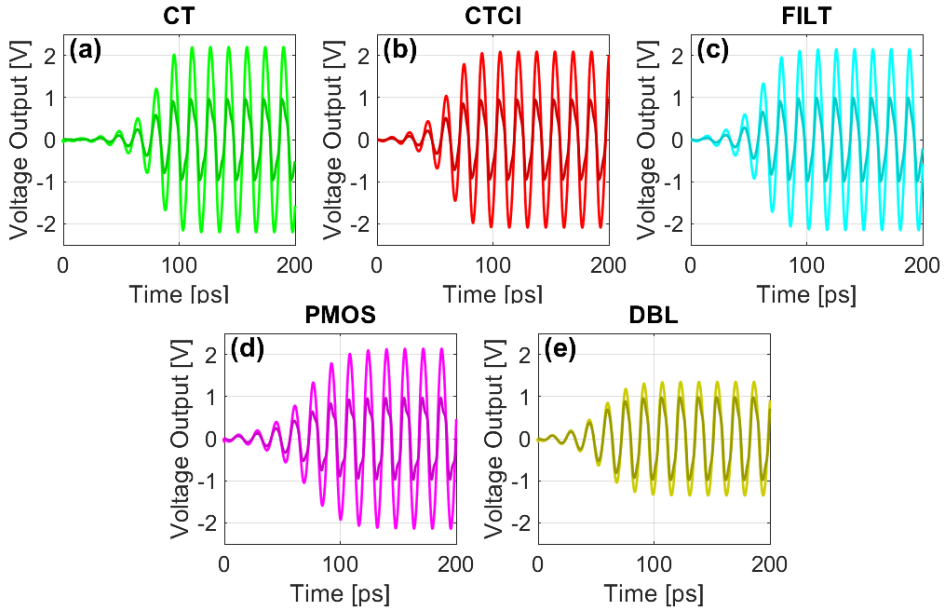

Figure 4.9: Waveform outputs of the oscillator and buffer for (a) the CT solution, (b) the CTCI solution, (c) the FILT solution, (d) the PMOS solutoin, and (e) the DBL solution.

the proposed start-up mechanism of branch current injection. The DBL solutions suffers from the limitation that the oscillation output is voltage-limited to V_{DD}, as can be seen in Figure 4.9e. With an increased buffer transistor size, the same buffer output as the remaining solutions could be reached. Table 4.3 presents the values for start-up time, dynamic power consumption and output power of all solutions.

Solution	t_s 10-90% [ps]	t_d 0-90% [ps]	P_{core} [mW]	P_{buff} [mW]	P_{tot} [mW]	P_{out} [dBm]
CT	45.8	95.0[2]	23.2	41.1	64.3	9.2
CTCI[1]	50.0	80.3	12.0	41.2	72.4	9.0
FILT[1]	49.5	77.7	11.7	42.6	73.6	9.2
PMOS	71.8	102.1[2]	24.6	35.8	60.4	7.9
DBL	60.0	79.6[2]	12.0	38.7	47.9	9.3[3]

[1] $P_{\text{tot}} \neq P_{\text{core}} + P_{\text{buff}}$ [2] No physical injection mechanism, starting from 5 mV offset [3] Larger buffer size to attain this

Table 4.3: The resulting values for start-up time, power consumption and output power from schematic simulations of the solutions.

To further investigate the start-up transient of all solutions, Figure 4.10 presents the signal envelopes of all solutions. The output envelopes are obtained by taking the peak values of each oscillation period (i.e. the peaks in Figure 4.9) and plotting them against time.

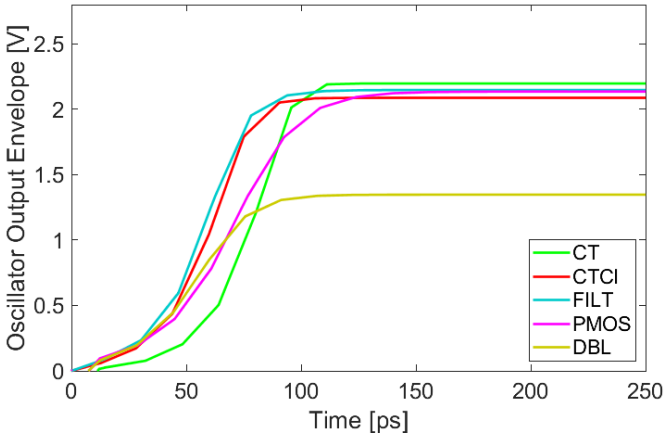

Figure 4.10: Waveform output envelopes of all solutions.

CT, CTCI and FILT show the fastest start-up times. Note that the addition of the noise filter to CTCI does not deteriorate start-up time, which speaks well for the FILT solution. The 10-90% response highlights the slow nature of the PMOS transistors, which is a trade-off that comes with the lower flicker noise performance. The DBL solution also displays slower start-up times. This is likely a result due to the use of PMOS transistors, but might as well have resulted from mismatch within the oscillator core. The trigger delay is mostly relevant for the two solutions with actual start-up mechanisms, namely CTCI and FILT. The remaining solutions featured intentional circuit asymmetries, and therefore the trigger delay does not tell much for these solutions. Comparing CTCI and FILT however, it is discovered that the trigger delay is not deteriorated with an introduction of a tail filter, which is an important conclusion.

During the simulations, a trade-off between start-up time and power consumption could be seen. Increasing the bias currents, which increases power consumption, resulted in faster start-ups. Worth noting is the low total power consumption of the DBL solution due to the re-use of current in the PMOS cross-coupled pair, which was the intention with introducing this solution. The values for P_{core} of CTCI and FILT were relatively low. However, the current sources in the branches also consume current. Since the current sources provide a current of 8 mA, the additional power consumption would be $2 \cdot 8\,\text{mA} \cdot V_{DD} = 19.2\,\text{mW}$. Although, note that the pulse is short, so this power is consumed at a very small amount of time, meaning that the average power over one bias cycle will be very low. A likely reason for the reduced core power consumption is the added branches' effect on the biasing point of the cross coupled pair, causing them to change current and power consumption. Lastly, PMOS did not show any remarkable improvement or

deterioration of power consumption compared to CT.

As for the output power, this metric was measured through the `hb` analysis, by extracting the output power spectrum across the $50\,\Omega$ load at the buffer output. The results show that all solutions, except PMOS, show equivalent output power performance. The PMOS solution originally showed unexpectedly low values of output power. The biasing of the buffer was suspected to be the culprit, and after adding bypass capacitors of 500 fF the conditions were improved. However, as the buffer design was not included in the focus of this work (as mentioned in Section 3.4.1), and so any further investigation into this matter was not made.

4.3 Layout and Post-Layout Simulations

4.3.1 Layout design

A layout design of the oscillator core, i.e. LC-tank and cross-coupled NMOS pair, was carried out. The layout design was performed with high frequency parasitics in mind, using the thickest metal layers for routing that carried the signal. Design rules, such as a minimum number of vias in parallel to avoid any resistive bottlenecks, were in place during the design to guide the designer to less parasitic inducing choices.

Two different methods of extracting post-layout effects were used after layout DRC rules and LVS check was clean. The first was a parasitic extraction (PEX) of the NMOS cross-coupled pair using Siemens' Calibre. This tool enables analysis of parasitic elements of the circuit, such as resistances and capacitances, which needs to be included in order to obtain an accurate representation of the circuit. The second tool was Momentum, which is an electromagnetic (EM) simulator. Momentum was used to get an accurate representation of the high-frequency EM field interactions between the interconnect metal structures of the circuit. A wrapper cell which contained only the high-frequency signal paths of the circuit (i.e., layers such as the digital frequency control inputs was ignored) was constructed for the Momentum simulation. To achieve a reasonable simulation time, the vias were merged and all polygons flattened. The results from PEX and Momentum simulations could then be used to retrieve post-layout results, enabling investigation of the solutions' performance in a more realistic setting. The layout designs themselves are proprietary designs of Acconeer, and can therefore not be shown in the report.

4.3.2 Limitations with layout design

Before the post-layout results are presented, a discussion into the limitations of the performed layout design and parasitic extraction is appropriate. The layout design that was used was the design for the oscillator core only. The interconnects connecting tail biasing and buffer was not included. Therefore, while collecting the results for post layout simulations, the parasitic extraction were not completely correct for every solution. For example, layout for the branches for CTCI and FILT were not included at all. Since the PMOS and DBL solutions feature completely different core designs, they were not included in the post-layout simulations.

All in all, the design has been done in such a way that it would enable application to different solutions, with sufficient accuracy. While the design aspects exclude some details, the overall picture of the parasitics is in place. Therefore, the results are an indication of how the solutions would perform in the presence of layout parasitics, but not an attempt to accurately predict post-layout performance. Properly constructing interconnect layouts and other necessary post layout simulations for all solutions is an aspect that would require more attention.

4.3.3 Simulation results with parasitics

After layout, the circuit's tank inductance was slightly tuned to achieve an oscillation frequency of 60 GHz. Table 4.4 shows the pre- and post-layout simulation results for the oscillation frequency f_0, frequency tuning range FTR and phase noise for offsets 100 kHz, 1 MHz and 10 MHz.

Solution	f_0 [GHz]	FTR [%]	PN @ 100k [dBc/Hz]	PN @ 1M [dBc/Hz]	PN @ 10M [dBc/Hz]	σ_{jitter} [fs]
CT	63.6	5.6	-73.2	-95.5	-115.8	NA[1]
	60.0	5.2	-73.9	-95.7	-115.9	NA[1]
CTCI	63.5	5.6	-72.2	-95.2	-115.7	97.4
	60.0	5.2	-74.0	-95.6	-115.8	76.8
FILT	63.4	6.0	-75.3	-96.2	-116.4	61.9
	60.0	5.6	-75.7	-96.7	-116.8	137.1

[1] No jitter value for this solution

Table 4.4: Pre- vs. post layout simulation results for tuning range and phase nosie metrics. Pre-layout results are presented in black, and post-layout results are presented in red.

All solutions have a tuning range deterioration of approximately 0.4 percentage points, which can be attributed to added parasitic capacitance and inductance. With a larger presence of static capacitance and inductance, the effect of $C_{\text{max}} - C_{\text{min}}$ of the varactor bank decreases, ultimately resulting in a smaller tuning range. The phase noise values have not changed significantly, although the CTCI solution present an improvement of almost 2 dB at 100 kHz. As mentioned in Section 4.3.2, the post-layout results should be taken with a grain of salt, so since no major performance deterioration has taken place in regards to these metrics the post-layout effects can be said to have not affected the phase noise performance of the solutions significantly.

Looking at the jitter values however, the CTCI solution has seemed to improved in performance, and the FILT solution decreased in performance. This behavior is certainly confusing, but can be attributed to the fact that this is not continuous wave jitter, but rather a jitter at an early crossing of the start-up. Therefore, it might be wise to not take the phase noise performance as a complete predictor for jitter performance as we have measured it. It is likely that the filter has some unexpected effects due to filter design mismatch and ultimately worse jitter in post-layout. Also, simulation accuracy might be at fault, and the setup

might not accurately represent the actual conditions and jitter that one would see during measurements of the actual oscillators. Lastly, the discussion in Section 4.1.2 about the trigger delay and start-up time as a function of pulse width indicated that the quality of the oscillation started by the current injection mechanism has a particular relationship to the pulse width of the injection pulse. A crude investigation was made post-layout and a similar relationship was found as in Figure 4.3. However, the relationship $w_{\text{pulse}} = nT_0$ is slightly shifted since T_0 is slightly changed post-layout, so the pulse widths had to be corrected slightly. It is however likely that more investigation is needed to properly determine the effects of injected current level and injection pulse width.

Table 4.5 presents the pre- vs. post-layout simulation results for the remaining metrics.

Solution	t_s 10-90% [ps]	t_d 0-90% [ps]	P_{core} [mW]	P_{buff} [mW]	P_{tot} [mW]	P_{out} [dBm]
CT	45.8	95.0[2]	23.2	41.1	64.3	9.2
	57.4	108.4[2]	21.5	41.2	62.7	8.4
CTCI[1]	50.0	80.3	12.0	41.2	72.4	9.0
	58.0	99.8	12.1	41.0	72.3	8.3
FILT[1]	49.5	77.7	11.7	42.6	73.5	9.2
	63.1	99.6	11.1	42.4	72.7	8.5

[1] $P_{\text{tot}} \neq P_{\text{core}} + P_{\text{buff}}$
[2] No physical injection mechanism, starting from 5 mV offset

Table 4.5: Pre- vs. post-layout simulation results for start-up time, trigger delay, power, and output power. Pre-layout results are presented in black, and post-layout results are presented in red.

The power consumption seems to be kept fairly stable for all solutions. The start-up times are deteriorated in similar amounts for all solutions, as well as the trigger delay, which an added parasitic resistance and capacitance can be expected to cause. Finally, it can be noted that the output power also seems to be deteriorated in a similar amount for all solutions. This is also true for the FILT solution. This indicates that the introduction of the tail filter does not significantly affect the start-up time, which shows promise for such implementation in pulsed oscillator circuits.

To summarize, the post-layout simulation shows that deterioration of most notably tuning range and start-up time should be expected when considering to go forward with the CT, CTCI or FILT solution.

4.4 Comparison with DCO solutions in literature

In order to benchmark the viability of the investigated solutions, the solutions are compared to solutions in literature. An arbitrary selection of implemented DCO's were made, and Table 4.6 shows a comparison of a selection of metrics with these works. The CT, CTCI and FILT solutions were presented with their post-layout results, while the PMOS and DBL solutions are presented with pre-layout, as no

post-layout results exist for these solutions. Worth noting is that the comparison is made with pre- and post-layout results for the proposed solution versus manufactured and measured results for the literature solutions. Although this might cause risk of unfair comparison, the given comparison serves as an indication towards the expected comparative performance of the proposed solutions. A figure of merit ($\mathrm{FoM_T}$) is used to provide a reference for comparison between the different solutions, and is calculated as

$$FoM_T = \mathcal{L}(\Delta f) - 20\log\left(f_0/\Delta f \cdot FTR/10\right) + 10\log\left(P_{dc}/1\,\mathrm{mW}\right), \tag{4.2}$$

where $\mathcal{L}(\Delta f)$ is the phase noise at frequency offset Δf, f_0 is the oscillation frequency, FTR is the tuning range and P_{dc} is the dc power consumption.

Solution	CMOS	f_0 [GHz]	FTR [%]	Res. [Hz]	PN @ 1 MHz [dBc/Hz]	$\mathrm{FoM_T}$ @ 1 MHz [dBc/Hz]	P_{core} [mW]	V_{DD} [V]
CT	40 nm	60	5.2	98M	-95.7	-172.3	21.5	1.2
CTCI	40 nm	60	5.2	98M	-95.6	-174.6	12.1	1.2
FILT	40 nm	60	5.6	105M	-96.7	-176.7	11.1	1.2
PMOS	40 nm	63	4.1	80M	-92.5	-166.9	24.6	1.2
DBL	40 nm	63	5.5	108M	-93.1	-173.1	12.0	1.5
[20]a	90 nm	60	10.0	160K	-93.0	-177.9	12.0	1.2
[20]b	90 nm	60	9.8	2.5M	-94.0	-177.9	14.0	1.2
[21]	90 nm	53	4	1.8M	-116.5[1]	-179.2[1]	2.3	1.2
[22]	65 nm	60	14.2	300K	-92.5[2]	-180.0[2]	18.0	1.2
[23]	65 nm	60	24.1	39K	-95.1[2]	-186.4[2]	10.0	1.0
[24]	90 nm	61	9.3	2.3 bit	-90.1	-174.9	10.6	1.2

[1] at 10 MHz [2] Best value chosen

Table 4.6: Comparison of benchmarks of the investigated solutions with solutions in literature.

The phase noise performance is comparable to those presented in literature. The power consumption seem to be slightly higher for the proposed solutions. However, even though the phase noise are comparable in level, and even high for the FILT solution, investigation of the $\mathrm{FoM_T}$ reveals a shortcoming of the proposed solutions. The tuning ranges, as well as resolution, would require further improvement. Given that the tuning range is smaller and resolution broader, the proposed solutions should in theory be able to leverage this to gain better noise performance, which is not really the case. This could point to a need to investigate new implementations for the LC-tank. However, an important aspect to take into account in this discussion is the fact that start-up time isn't presented in any of the chosen solutions in literature. The case is often that the applications do not warrant the need for a fast and controllable start-up and shutdown, which is in fact the case of this work. Fast start-up and stability of the oscillation during a short pulse rather than a continuously running operation warrants the need to over design the oscillator. Therefore, the increased power consumption and worse tuning ranges could be seen as the price to pay to be able to achieve the fast and

controllable start-ups needed for the applications within the contexts of this work, namely pulsed coherent radars.

Chapter 5

Outlook and Conclusion

5.1 Suggestive action for Acconeer

5.1.1 Viability of the investigated solutions

Analyzing the results of the schematic simulations compared to measured results of solutions in literature, a few solutions stand out as possible alternatives as a DCO topology. The FILT solution shows promise, exhibiting a $\mathrm{FoM_T}$ that is 4.4 dB lower than CT. The FILT solution do however add significant area on-chip since the filter components require somewhere to be placed. If there's area for compensations in other areas of the chip, then the FILT solution is a viable option for Acconeer. A proper layout design and post-layout simulation, including the passive filter components and injection branches, should in that case be conducted. The PMOS solution does provide opportunities to lower the phase noise of the DCO. However, this increased noise performance might not be able to compensate for the slow start-up time and low tuning range. Since the start-up time is a valuable metric for Acconeer, choosing PMOS might lead to a significant increase in power performance to achieve the desired start-up time. Also, a proper start-up mechanism has to be developed for the PMOS solution, as the solution tested here does not feature any such mechanism. The DBL solution presents an opportunity to lower the power consumption of the core, however at a price of worse start-up time and possible deterioration of noise performance. Again, this might lead to a need to compensate and ending up with the same or larger power consumption than before.

Acconeer's next step should be to compile the shortcomings they experience with the current solution to see if any of these proposed solution indicate towards a possible course of action that can amend these shortcomings. The proposed solutions do not provide complete packages of solutions, but might point towards ways of relaxing trade-offs currently in place. If any such ways can be identified, further investigation consisting of proper layout designs and possible manufacture and physical measurements should be taken in order to solidify that the solution is in fact going to improve performance.

5.1.2 LC-tank considerations

The proposed solutions did not investigate any change of the LC-tank features, except for a change in inductance value in some cases. Some state of the art DCOs do however feature other alternatives to co-planar waveguides and a binary-weighted varactor bank which might be worth considering. For example, a possible alternative to the current LC-tank structure as presented in [20]. This paper introduces the use of passive resonators, i.e. a transmission line, inductor or transformer, that are configurable thanks to several metal strips beneath the structures. A thermometer code indexing is used to determine which lines to be activated to achieve a certain value.

It is likely that any solution that proposes new LC-tank structures such as that of [20] will also imply drastic changes to current solution that would take significant amount of time to implement. Therefore, it's recommended to consider if the time and effort that inevitably comes with a similar solution is worth the possible benefits. When considering drastic changes, the effect that the changes will have on the ability to control the start-up and shutdown transients should also be part of the equation.

5.2 Future work

Several aspects of this work could be the subject of future work into the subject. Firstly, the proposed current branch injection mechanism have only been investigated using a minimum-sized transistor and ideal current source. Alternative configurations for optimal performance, as well as the realization of the current source and pulse, could be the subject of investigation in future work. Secondly, the context of this work warrants the need for start-up mechanisms that have control of not only the start-up time, but also the signal phase. This work did not focus on investigating this metric. Instead, as described in Section 3.3.2, phase coherency is only approximated to have any detrimental effects if the transient noise simulation presented jitter values that were way off. This metric could therefore be a focus in a continuation of this work. Furthermore, deeper investigation of the peripherals and surrounding context of the solutions were not investigated in this work. Future work could evaluate the performance of the proposed solution when incorporated within surrounding circuitry. Finally, as stated in Section 5.1.2, the subject of future work could be to use the currently existing structure, and investigate alternatives to the current LC-tank solution.

5.3 Conclusion

Several alternatives to Acconeer's current DCO topology have been identified, analyzed, and benchmarked. The viability of these alternatives have been evaluated through comparison of schematic simulation results with a digital equivalent of the common cross-coupled differential-pair LC-VCO, as well as benchmarking by comparison with state of the art DCO solutions in literature. The results from post-layout simulations of the solutions perform comparatively well to solutions

in literature, and different possibilities in terms of suggestive actions is thereby provided to Acconeer. Finally, future work that can act as continuation of this work is suggested.

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